*YOUR NAME*______________________________

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

Exam No. 2

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V. You may also approximate [(kT/q) ln 10] as 0.06 V.
2. Open book: 6.012 text and up to 10 lb. of notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all ten (10) pages of this exam booklet, and make certain that you write your name at the top of this page and pages 2, 5, and 8 in the spaces provided.
7. The exam is long, but has numerous small parts, many of which are independent. Most answers are worth 3 pts. (a few are worth 2 or 4 pts). Don't spend too much time on any one question; move on and come back to it later.

6.012 Staff Use Only			
	PROBLEM 1	____________	(out of a possible 38)
	PROBLEM 2	____________	(out of a possible 34)
	PROBLEM 3	____________	(out of a possible 28)
	TOTAL		

Problem 1 - (38 points)

This question has three independent parts, each with several sub-parts.

a) You have two npn bipolar junction transistors, BJT A and BJT B, that are identical except that BJT A has base and collector doping levels that are twice those of BJT B, i.e., N_{AB}(BJT A) = 2 N_{AB}(BJT B) and N_{DC}(BJT A) = 2 N_{DC}(BJT B).

i) Which BJT has the larger Early voltage, and why?

O BJT A O BJT B O Neither

because

ii) Which BJT has the larger forward alpha, α_F, (and β_F, too), and why?

O BJT A O BJT B O Neither

because

iii) Which BJT, when biased in its FAR with V_{CE} = 4 V, has the larger C_μ, and why?

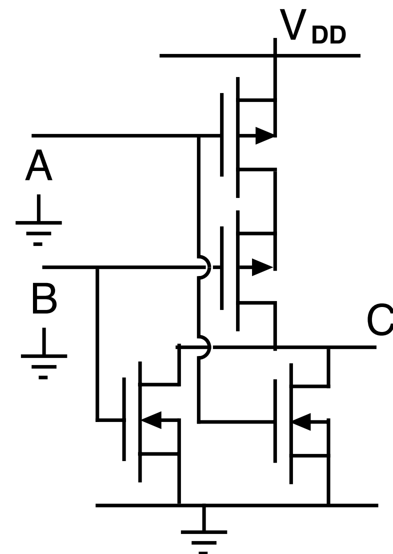
O BJT A O BJT B O Neither

because

iv) Which BJT, when biased in its FAR with I_C = 1 mA, has the larger g_m, and why?

O BJT A O BJT B O Neither

because



b) Consider the two-input CMOS logic gate above at right.

i) When both inputs are low, what is the output, C?

O High O Low O Can't say, because

Problem 1 continues on the next page

Problem 1 continued

ii) When input A is high and input B is low, what is the output, C?
O High O Low O Can't say, because

iii) Compare the time it takes the output to switch from high to low (discharging cycle) when both inputs are abruptly changed from low to high, with the time it takes when only one input is abruptly changed from low to high? Is it faster, slower, or similar? Explain.

O Faster O Slower O Similar

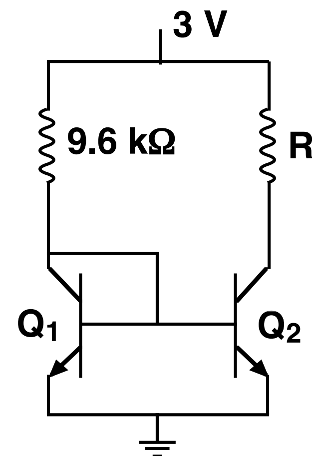
because

iv) When both inputs are low and the both p-channel MOSFETs are "on" they behave together like a transistor with a gate length, L, that is the sum of the gate lenghts of the individual transistors, i.e., 2 L_{min} in this case. How wide should the p-channel MOSFETs be in terms of W_n, the width of the n-channel MOSFETs, to make the low-to-high output switching time (charging cycle) of this gate as least as fast as the slowest high-to-low output switching. Assume $\mu_e = 2\ \mu_h$.

Width: ____________________

c) Consider the current mirror on the right below. Both transistors have $v_{BE,ON} = 0.6$ V, $v_{CE,SAT} = 0.2$ V, and $\beta_F = 100$, but the transistor on the right has twice the area as the one on the left (they are otherwise identical). You may neglect the base currents in the first three sub-parts of this question.

i) What is the collector current of Q_1?



$I_C(Q_1)$ = ____________________

Problem 1 continues on the next page

Problem 1 continued

ii) What is the collector current of Q_2, assuming Q_2 is in its FAR? Recall that the areas of Q_1 and Q_2 differ.

$I_C(Q_2)$ = ________________

iii) What is the range of values for R over which Q_2 remains in its FAR?

_________ $<$ R $<$ ___________

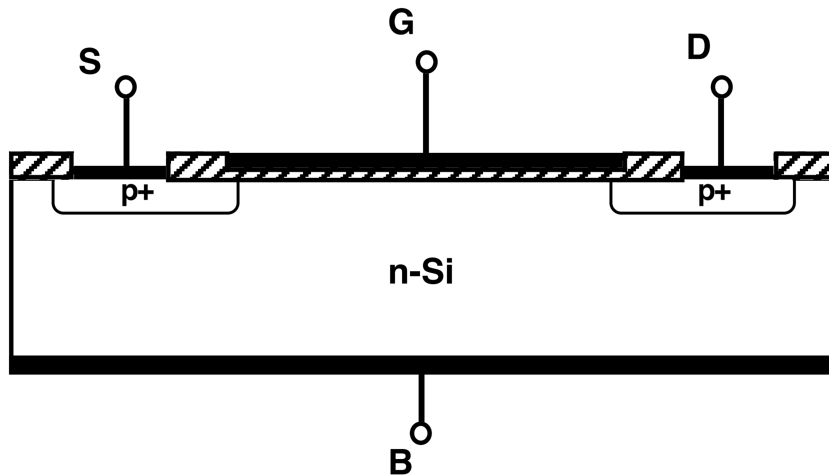
iv) What are the base currents of Q_1 and Q_2?

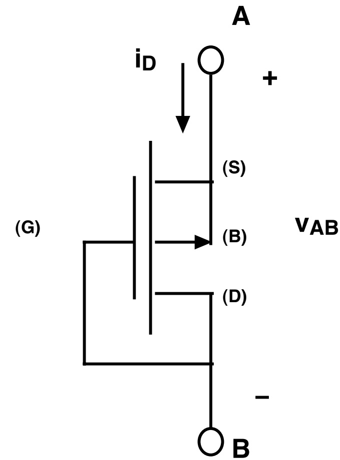
$I_B(Q_1)$ = ________________

$I_B(Q_2)$ = ________________

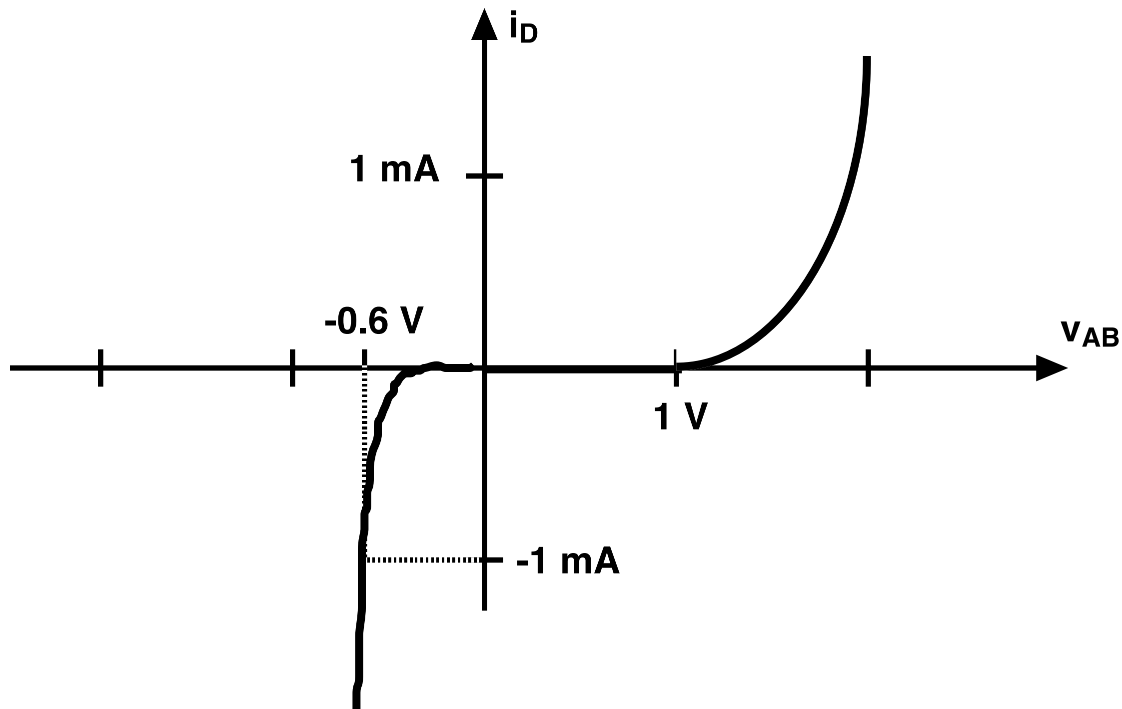
End of Problem 1

Problem 2 (34 points)





This problem concerns the p-channel MOSFET illustrated on the left above. You are told that the drain current of this MOSFET can be written as $-1000(v_{GS} - V_T)^2$ μA, when $v_{DS} < v_{GS} - V_T < 0$, but your are not told V_T. You are told, however, that when its gate and drain are connected together, and its source and substrate are also connected together, as is shown above on the right, the current-voltage characteristic of this "diode" looks like that shown below:



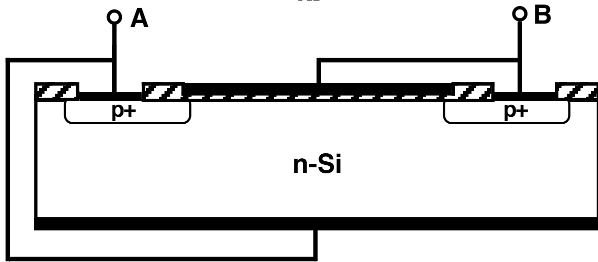
a) What is the threshold voltage, V_T, of this MOSFET?

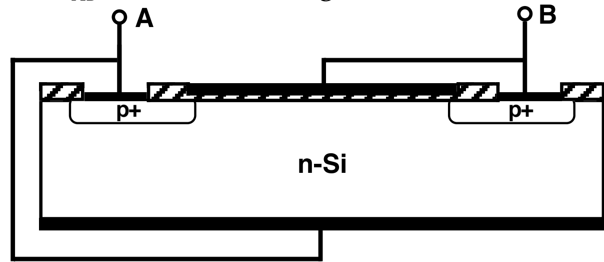
V_T = ________________ Volts

Problem 2 continues on the next page

Problem 2 continued

b) On the small device cross-sections below indicate the primary current path through the structure when $v_{AB} < 0$ V (on the left), and when $v_{AB} > 1$ V (on the right)





i) Current path when $v_{AB} < 0$ V

ii) Current path when $v_{AB} > 1$ V

c) Write an expression for i_D as a function of v_{AB} in each of the three ranges defined below:

i) Range I: $v_{AB} < 0$ V

$i_D =$ ______________________________

ii) Range II: $0\text{ V} < v_{AB} < 1$ V

$i_D =$ ______________________________

iii) Range III: $1\text{ V} < v_{AB}$

$i_D =$ ______________________________

d) In the space at right draw a quasi-static one-element linear equivalent circuit model for this "diode". By "quasi-static" we mean that you can ignore charge stores and base your linear equivalent circuit on only the static current-voltage model.

e) Determine the value of the element in your linear equivalent circuit at each of the following three bias points:

i) $i_D = +1$ mA

Value: ________________

Problem 2 continues on the next page

Problem 2 continued

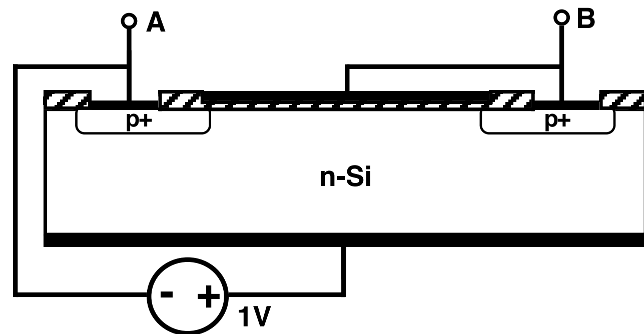
ii) $v_{AB} = +0.5$ V

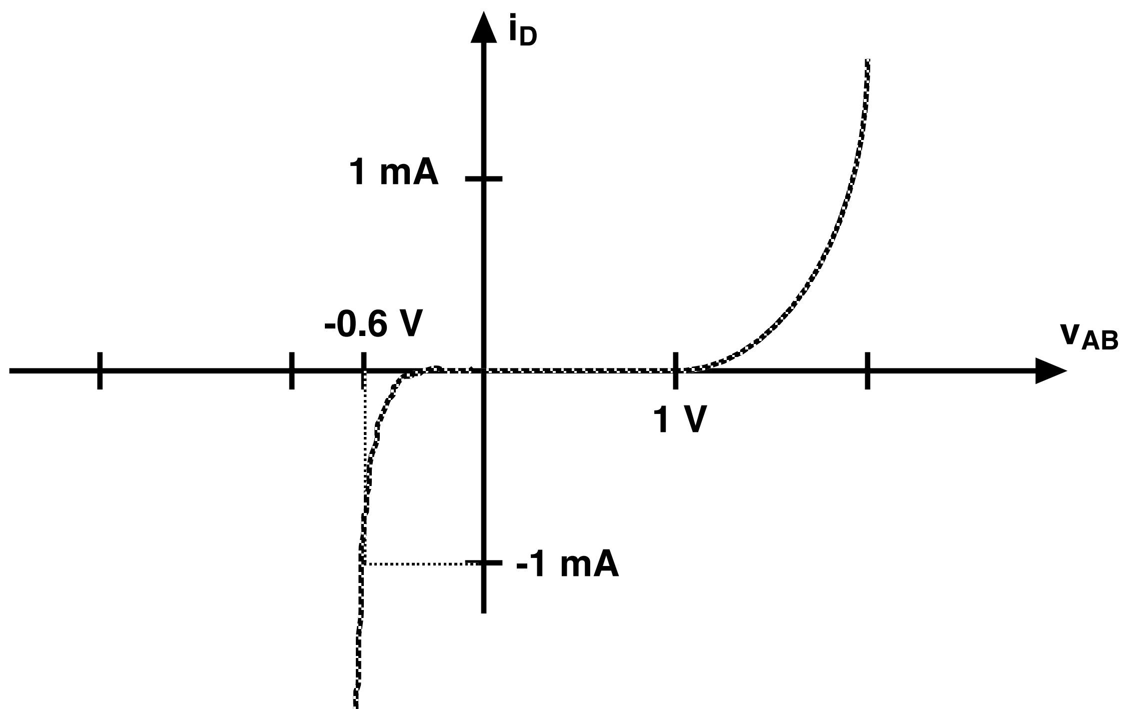
Value: ________________

iii) $i_D = -1$ mA, $v_{AB} = -0.6$ V

Value: ________________

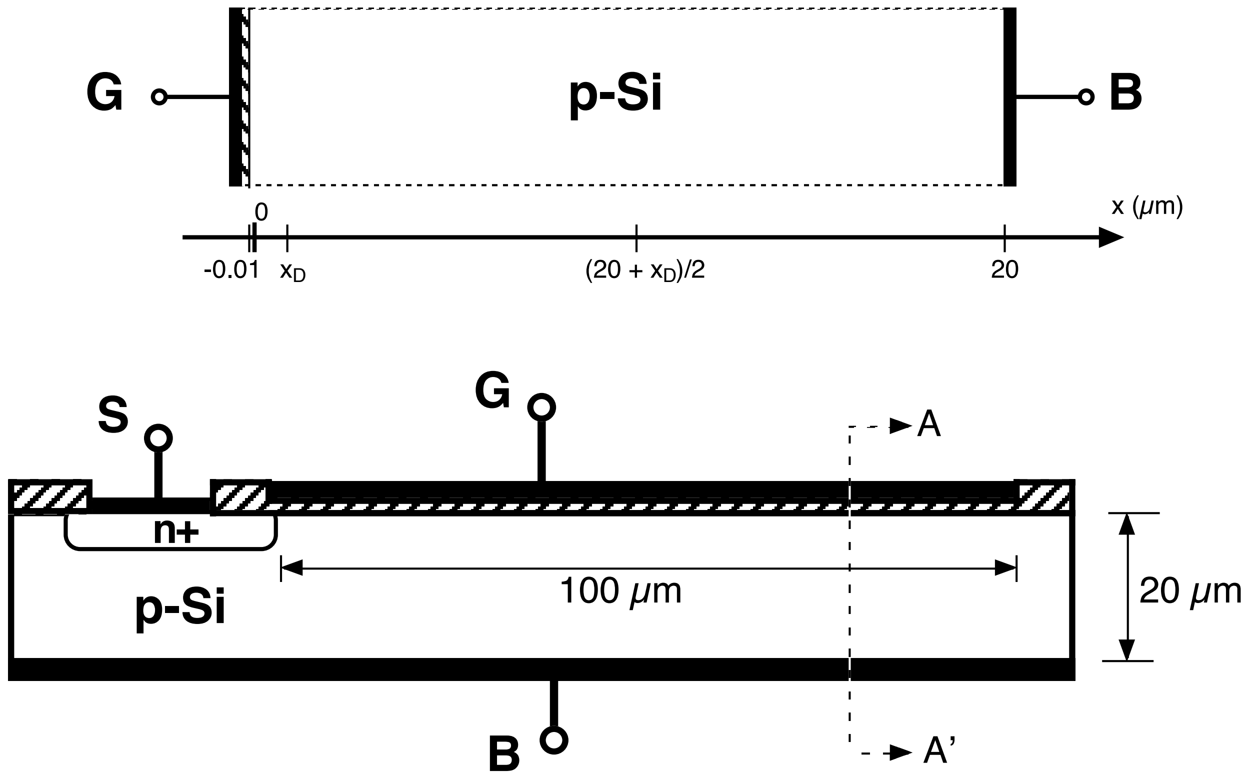
f) Draw on the axes below the characteristics of this two-terminal "device" when a 1 V voltage source is inserted between the substrate contact and the source contact as indicated in the figure to the right. The dashed line on the axes is the earlier curve of the characteristics when the source and back contact are shorted.





End of Problem 2

Problem 3 - (28 points)



This question concerns the MOS capacitor structure above. This device was fabricated using state-of-the-art technology on p-type Silicon, $N_A = 10^{17}$ cm^{-3}, and has a gate oxide 10 nm thick. The dielectric constant of the gate oxide is 3 x 10^{-11} F/cm, and the electrostatic potential of the gate metal, ϕ_m, is 0.35 V relative to intrinsic Si. In the lower figure, x_D is the edge of the depletion region under the gate.

a) What is the flat-band voltage, V_{FB}, of this structue?

V_{FB} = ____________________

b) When $v_{BS} = 0$, what is the electrostatic potential drop, $\Delta\phi$, in the silicon at threshold, i.e. when $v_{GS} = V_T$?

$\Delta\phi$ in Si ($v_{GS} = V_T$, $V_{BS} = 0$) = ____________________

Problem 3 continues on the next page

Problem 3 continued

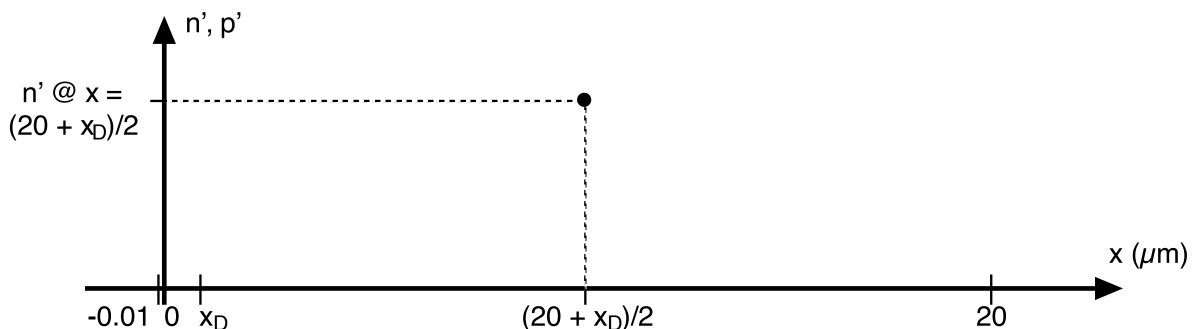
c) Now consider what would happen if V_{BS} was -2 V.
   i) What would the electrostatic potential drop, $\Delta\phi$, in the silicon be now at $v_{GS} = V_T$?

$\Delta\phi$ in Si ($v_{GS} = V_T$, V_{BS} = -2V) = ____________________

   ii) Is $|V_T|$ larger or smaller now, i.e., when V_{BS} is -2 V instead of 0 V? Explain
   O Larger   O Smaller   O Similar
   because

d) The "diode" between the n-type channel and the p-type Si will act like a photodiode if it is illuminated. For example, suppose that this structure is illuminated with light that generates M hole-electron pairs per square centimeter per second in the plane under the gate half-way between the edge of the depletion region, x_D, and the back, i.e., at $x = (20 + x_D)/2$ μm. Assume that the minority carrier diffusion length is much greater than 10 μm, that M is 6×10^{18} pairs/cm^2-s, and that the size of the illuminated area under the gate is 100 μm by 100 μm (10^{-2} cm by 10^{-2} cm). Ignore any lateral diffusion of carriers, i.e., they only diffuse in the x-direction. Finally, set $v_{BS} = 0$ as it was in Part b. The boundary conditions are then as follows:
   When it is in the flat-band condition ($v_{GS} = V_{FB}$) the surface of silicon under that gate behaves like a reflecting boundary.
   When $v_{GS} > V_T$, the inversion layer of electrons that is formed (i.e., the channel) acts like the n^+-side of a p-n^+ junction and is a sink for excess electrons in the p-type Si.
   The back contact at x = 20 μm is an ohmic contact.

   i) On the axes below sketch the minority carrier density, n'(x), in this device when $v_{GS} = V_{FB}$. Assume low-level injection conditions pertain and that n' at $x = (20+x_D)/2$ μm is the value indicated on the figure.



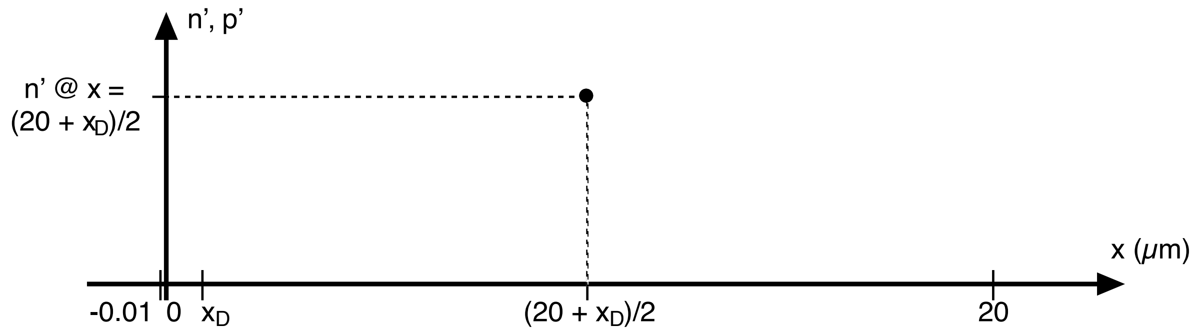
   ii) What is the short circuit current between the contacts S and B under the conditions of part (i), i.e. when $v_{GS} = V_{FB}$?

I = ____________________

Problem 3e continues on the next page

Problem 3e continued

iii) On the axes below sketch the minority carrier density in this device when $v_{GS} > V_T$. Assume low-level injection conditions pertain and that n' at x = $(20+x_D)/2$ μm is the value indicated on the figure.



iv) What is the short circuit current between the contacts S and B under the conditions of part (iii), i.e. when $v_{GS} > V_T$? You may assume $x_D << 20$ μm if you feel you need to know x_D.

I = ___________________

End of Problem 3; End of Exam