

Chapter 5. Nanostructures Technology, Research and Applications

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5.1 NanoStructures Laboratory

The NanoStructures Laboratory (NSL) at MIT develops techniques for fabricating surface structures of integrated circuits (IC) with feature sizes in the range from nanometers to micrometers, and uses these structures in a variety of research projects. The NSL includes facilities for lithography (photo, interferometric, electron beam, ion beam, and x-ray), etching (chemical, plasma and reactive-ion), liftoff, electroplating, sputter deposition, and e-beam evaporation. Much of the equipment and nearly all of the methods utilized in the NSL are developed in-house. Generally, commercial IC processing equipment cannot achieve the resolution needed for nanofabrication, and it lacks the required flexibility. The research projects fall into four major categories: (1) development of submicron and nanometer fabrication technology; (2) short-channel semiconductor devices, quantum-effect electronics, and optoelectronics; (3) periodic structures for x-ray optics, spectroscopy, atomic interferometry and nanometer metrology; (4) crystal-line films on nonlattice-matching substrates.

5.2 Scanning Electron Beam Lithography

Sponsors

Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038
Semiconductor Research Corporation
Contract 94-MJ-550

Project Staff

Scott E. Silverman, Juan Ferrera, Professor Henry I. Smith

Figure 1 is a photograph of the scanning electron beam lithography (SEBL) system (VS-PL) located in Room 38-185 at MIT. This instrument was donated from IBM in November 1993. It is an experimental system based on many years of IBM technology development of SEBL. In 1994, a novel pattern generator was fabricated and installed on the system. The pattern generator is based on RISC parallel processor technology, enabling the generation of arbitrary shapes, including curved geometries.

The VS-PL system is the cornerstone of a newly established facility for high performance electron-beam lithography. The goals of the new facility are (1) to provide the MIT research community with an in-house SEBL capability for writing directly on

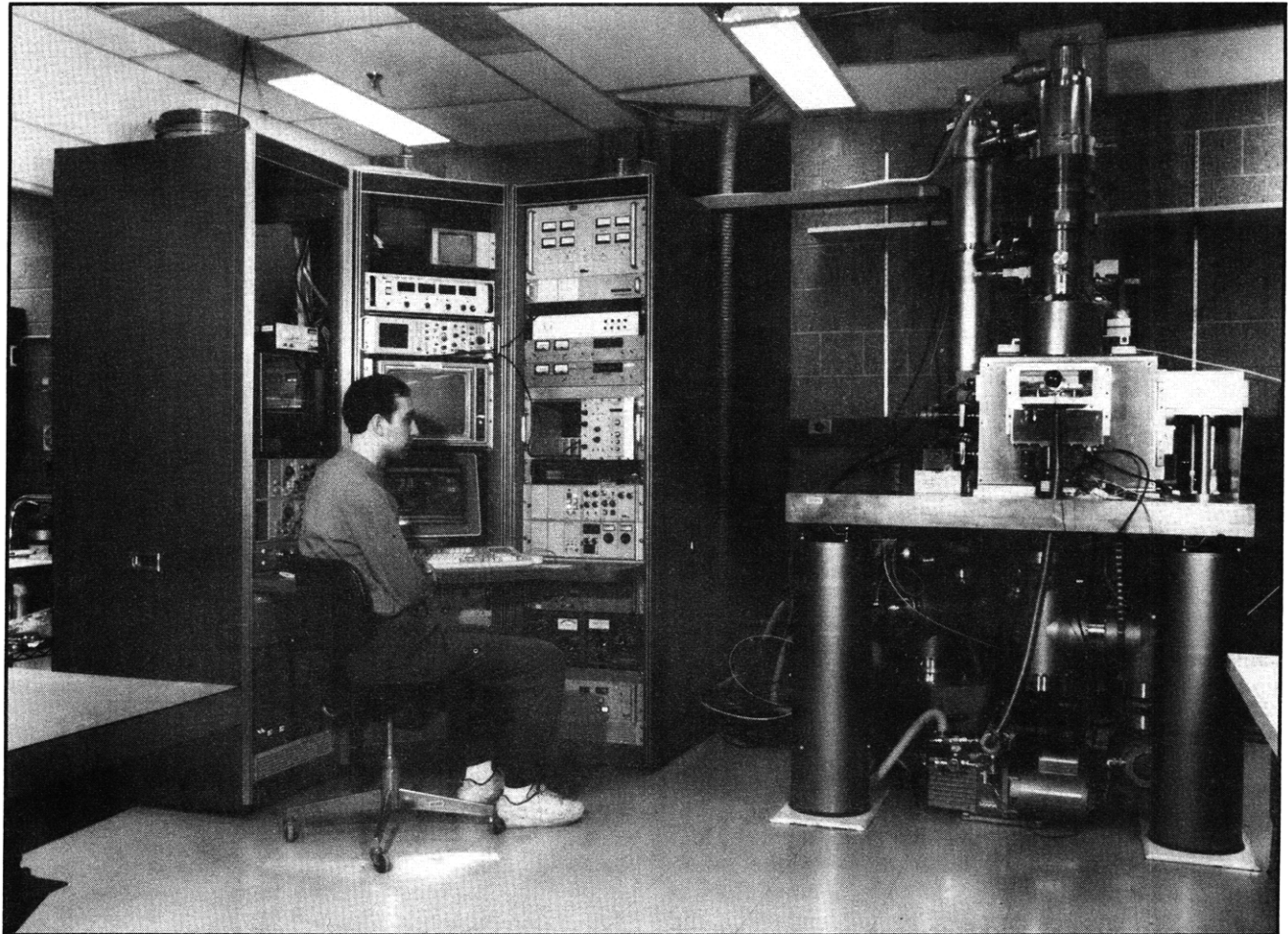


Figure 1. Photograph of the new VS-PL scanning-electron-beam lithography system, obtained as a donation from IBM in November 1993. The operator is Research Engineer Scott E. Silverman. (Photo by John F. Cook)

experimental device substrates; (2) to advance the state-of-the-art in SEBL, particularly with regard to pattern placement accuracy and long-range spatial-phase coherence; and (3) to pattern x-ray nanolithography masks for in-house use. Our approach to improved pattern placement accuracy is based on a new technique, invented at MIT, called spatial-phase locking. It is expected that the new SEBL facility will concentrate on sub-100 nm electronic and quantum-effect devices, and optoelectronic devices such as DFB lasers and channel-dropping filters for wavelength-division multiplexing in optical communication systems.

5.3 Spatial-Phase-Locked Electron-Beam Lithography

Sponsors

Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038

National Science Foundation
Grant ECS 94-07078
Semiconductor Research Corporation
Contract 94-MJ-550
U.S. Army Research Office
Contract DAAL03-92-G-0291

Project Staff

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It is well known that scanning-electron-beam lithography can write extremely fine lines, ~ 10 nm in thin PMMA and ~ 1 nm in AlF_3 . However, because writing fields in electron-beam lithography are quite small ($\sim 10^4$ beam steps), large-area patterns must be created by stitching together the small fields, using a laser interferometer to provide X-Y positioning information. However, it is often overlooked that, due to instability, drift, and a variety of other problems, the precision with which this can be done is much poorer than the resolution. Typically,

stitching errors of 30 to 100 nm are observed at field boundaries.

To solve this problem, we are developing a technology called spatial-phase-locked electron-beam lithography (SPLEBL), which will provide pattern placement accuracy and precision finer than the resolution. The basic idea behind SPLEBL is to create on the substrate a fiducial grid and conduct all e-beam lithography with reference to it. The fiducial grid is produced by interferometric lithography to ensure long-range spatial-phase coherence. We are investigating two modes of implementation, the global fiducial grid and the segmented grid. In the latter approach, the grid is transferred onto the substrate only in small regions ($2 \times 2 \mu\text{m}$ square) at the corners of each e-beam scan field. Spatial-frequency-domain techniques

are used to achieve sub-pixel alignment and scaling. In the latter approach the fiducial grid is transparent to the exposing e-beam and covers the entire top of the resist film. By collecting the emitted secondary electrons, a computer will keep track of the e-beam position at all times and correct for any drift or spurious displacement.

In order to demonstrate the efficacy of SPLEBL, x-ray masks for optical filters were fabricated in collaboration with IBM's Thomas J. Watson Research Center. These classes of devices have linewidths of ~ 100 nm and span many fields of the e-beam lithography system. They require field stitching errors of ~ 1 nm for highest performance. Figure 2 illustrates the repeatability of spatial-phase locking using the VS-6 e-beam lithography system at IBM Yorktown Heights.

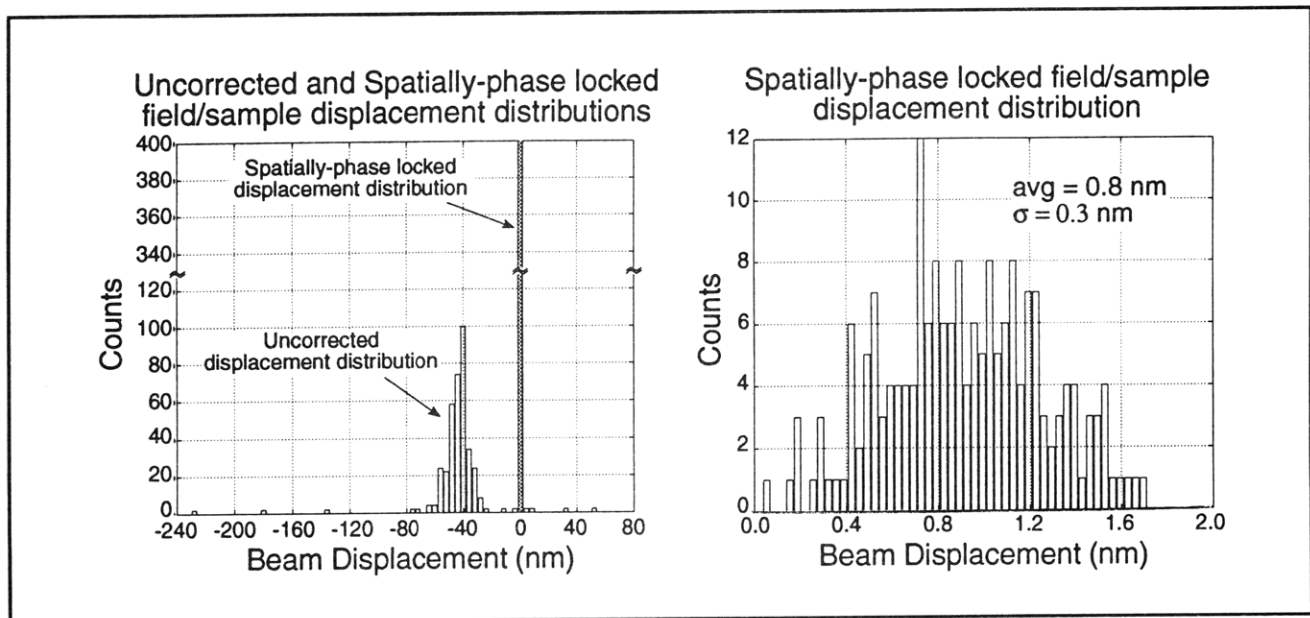


Figure 2. Histogram illustrating the repeatability of spatial-phase locking, and, for comparison, e-beam placement precision without spatial-phase locking. The right panel is a magnified display of the spatial-phase locking results, showing a mean displacement of 0.8 nm and a standard deviation of 0.3 nm. With spatial-phase locking, field-stitching errors below 1 nm appear feasible, an improvement of nearly 2 orders-of-magnitude over conventional technology.

5.4 X-Ray Nanolithography

Sponsors

Advanced Research Projects Agency/
Naval Air Systems Command
Contract N00019-92-K-0021
Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038

Project Staff

James M. Carter, Scott D. Hector, Euclid E. Moon, Gabrielle M. Owen, Mark L. Schattenburg, Vincent V. Wong, Isabel Y. Yang, Professor Henry I. Smith

For several years, we have been developing the tools and methods of x-ray nanolithography (i.e., sub-100 nm features). We have explored the theoretical and practical limitations and endeavored to make its various components (e.g., mask making, resists, electroplating, sources, alignment, etc.) reliable and "user friendly". Because of the critical importance of the x-ray mask technology, we discuss this separately in section 5.5.

Our sources for x-ray nanolithography are simple, low-cost electron-bombardment targets, typically Cu_L ($\lambda = 1.32 \text{ nm}$), separated by a $1.4 \text{ }\mu\text{m}$ -thick SiN_x vacuum windows from helium-filled exposure chambers. In the future, we hope to replace the Cu_L sources with higher flux plasma-based x-ray sources.

For most applications that require multiple mask alignment, we currently use a simple microscope-based system which provides about $0.3 \text{ }\mu\text{m}$ superposition precision. We are also developing a high precision mask alignment system (see section 5.6) that should provide overlay approaching 1 nm .

In earlier research, we showed that for x-ray wavelengths longer than $\sim 0.8 \text{ nm}$, the range of the photoelectron emitted when an x-ray photon is absorbed in resist does not limit the resolution. Down to feature sizes $\sim 20 \text{ nm}$, diffraction is the major concern. By means of accurate electromagnetic calculations, taking into account the vectorial character of the electromagnetic field and the dielectric properties of the absorber, we have shown that when source spatial coherence is optimized, diffraction does not limit resolution as severely as had been predicted by simple Fresnel diffraction calculations. Figure 3 plots the maximum mask-to-sample gap G versus minimum feature size W for two values of the parameter α which connects gap and feature size: $G = \alpha W^2/\lambda$. Modeling and experiment verify that α can be between 1 and 1.5 while retaining good process latitude.

For gaps below $10 \text{ }\mu\text{m}$, the mask and substrate must be optically flat (see section 5.5) and dust particles must be detected and eliminated. To accomplish this, we use a jet of frozen CO_2 micropellets impinging on the substrate or mask at a low angle. The pellets knock off adhering dust particles while leaving no residue, and the CO_2 gas also tends to remove thin layers of organic contamination.

For the linewidth range from 70 to 20 nm , mask-substrate gaps must be below $5 \text{ }\mu\text{m}$. This is not a problem in a research setting, but may be unacceptable for manufacturing. For this reason, we have investigated the feasibility of using arrays of zone plates for projection imaging with x rays of either 4.5 nm or about 1.0 nm wavelength.

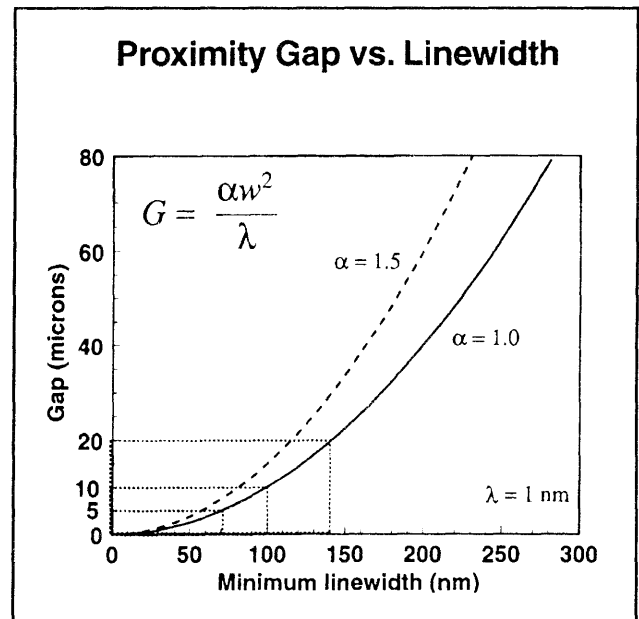


Figure 3. Plot of maximum mask-sample gap G versus minimum feature size W for two values of the parameter α .

5.5 Improved Mask Technology for X-Ray Lithography

Sponsors

Advanced Research Projects Agency/
Naval Air Systems Command
Contract N00019-92-K-0021
Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038

Project Staff

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At feature sizes of 100 nm and below the mask-to-sample gap G must be less than $\sim 10 \text{ }\mu\text{m}$. We have developed a mask configuration compatible with this requirement in which the mask membrane is flat to less than 250 nm . We continue to make incremental improvements in this technology as illustrated in figure 4. A novel, low-gradient furnace was developed to achieve such high levels of mask flatness.

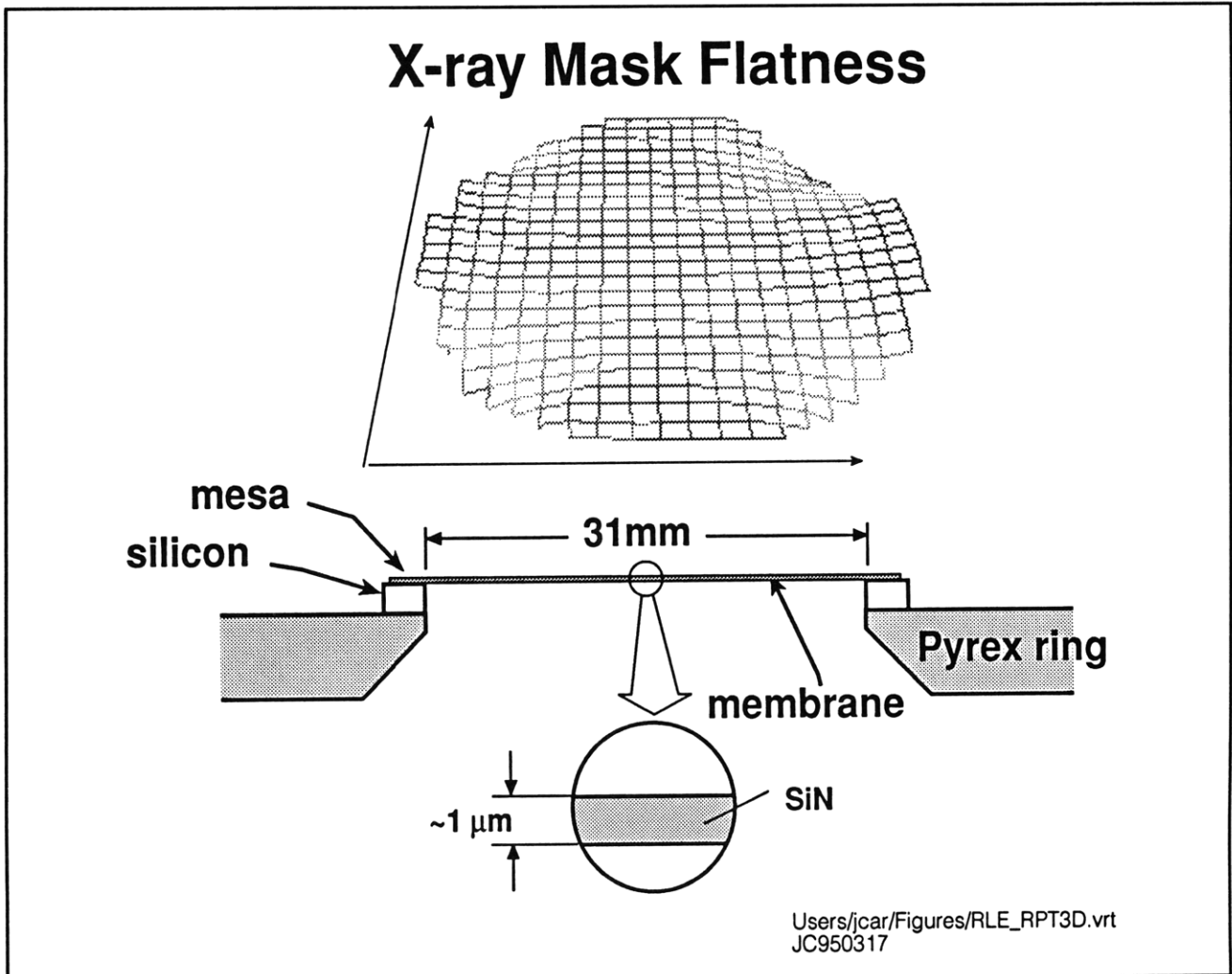


Figure 4. Schematic of mesa-style x-ray mask combined with a plot of mask flatness for a 31 mm-diameter SiN_x membrane. Stress at the Si-Pyrex interface causes some twisting. However, the membrane is tensile and flat to within 200 nm.

Our mask technology is based on low-stress, Si-rich silicon nitride, SiN_x . This material is produced in the IC Laboratory at MIT in a vertical LPCVD reactor. The resulting films are clean and uniform, and x-ray mask membranes made from them are extremely robust. These mask membranes can be cleaned and processed in conventional stations. Radiation hardness remains a problem at dose levels corresponding to production (i.e., millions of exposures) but is quite suitable for the purpose of research material.

For absorber patterns, we use both gold, Au, and tungsten, W. Both can be obtained with near-zero

stress (i.e., $< 10^7$ MPa), which implies that pattern distortion should be negligible (i.e., < 1 nm). The gold is electroplated onto the membrane after resist exposure and development using a specially designed apparatus. The W is sputter deposited and patterned by reactive-ion etching. During sputter deposition, the plasma environment leads to a nonuniform temperature distribution, which, in turn, causes nonuniform stress. In order to ensure uniform W stress over an entire membrane, a He-backside temperature-homogenization apparatus is used. This produces stress that is uniform to within our measurement error of ± 5 MPa (figure 5).

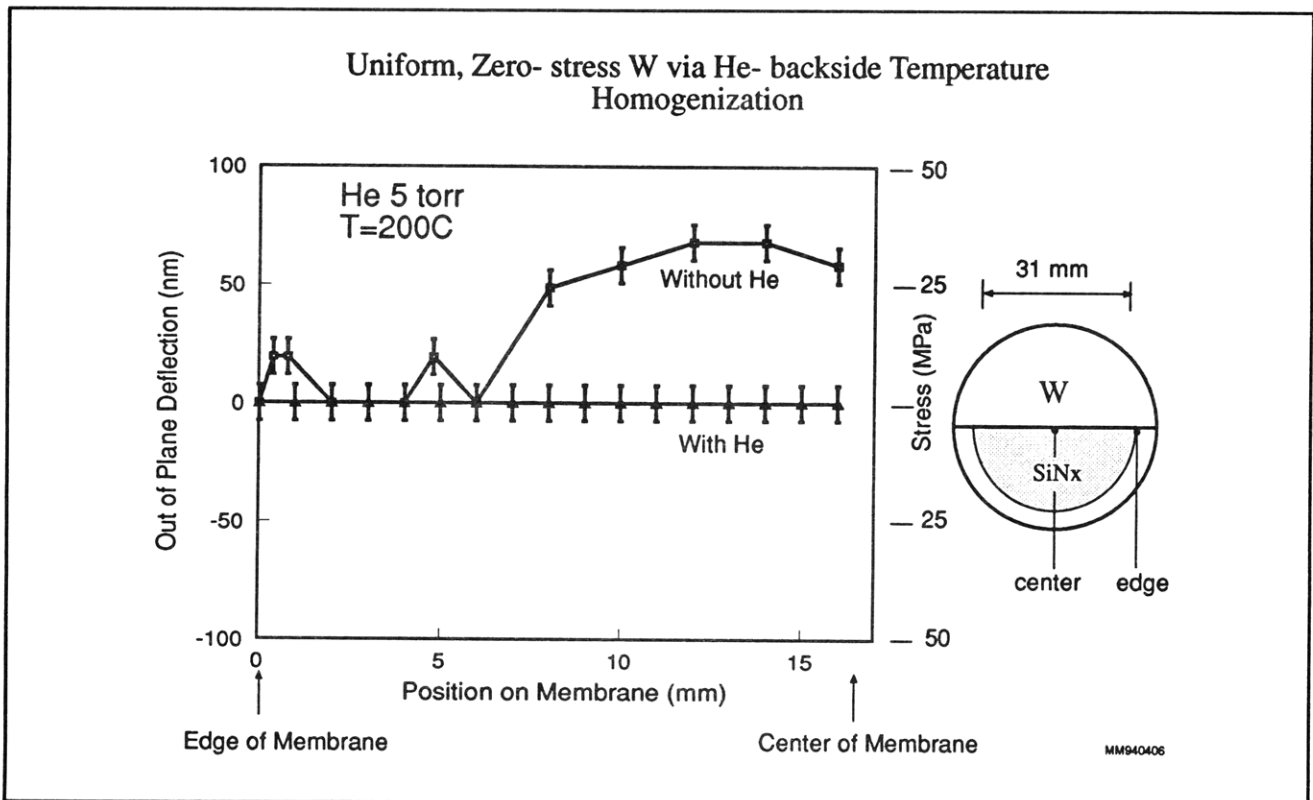


Figure 5. Plot of out-of-plane deflection (left ordinate) and stress (right ordinate) versus radial position for 300 nm-thick W, sputter deposited at 200°C onto a SiN_x x-ray mask membrane, with and without He backside temperature homogenization. A uniform zero stress is achieved with He, whereas stress is nonuniform without the He.

The He Pressure on the backside of the membrane for heat transfer also enables us to monitor the stress by measuring the change in the bulge of the membrane during W deposition. With this *in situ* scheme, we hope to achieve a stress in the neighborhood of 5×10^6 MPa, with good repeatability.

Patterning of x-ray masks is done by interferometric lithography for periodic structures, but for patterns of arbitrary geometry, it is done by e-beam lithography, either in the MIT e-beam facility or in collaboration with NRL or IBM. We use CAD tools at MIT and convert the data into formats compatible with the e-beam exposure systems. Data is shipped to NRL or IBM by electronic network. After e-beam exposure, masks are shipped back to MIT by express mail where development and Au electroplating are carried out. This collaboration has already demonstrated that patterning x-ray masks by e-beam can be done remotely, and, by

implication, that university researchers with limited facilities can have access to nanolithography via x ray alone and do not need to own or even visit an e-beam lithography facility.

Figure 6 illustrates the sequence followed in most cases. The master mask written by e-beam lithography is replicated into a daughter mask of opposite "polarity". This daughter mask is then replicated onto a GaAs device substrate.

For etching W absorber patterns on x-ray masks, a reactive-ion-etching process is required, which puts considerable power into the membrane substrate. Since membranes have very low thermal mass and conductivity, we use He-backside cooling in a reactive ion etcher. Membranes can be cooled to below -20°C . At such low temperatures the isotropic etching component is suppressed leading to highly directional etching.

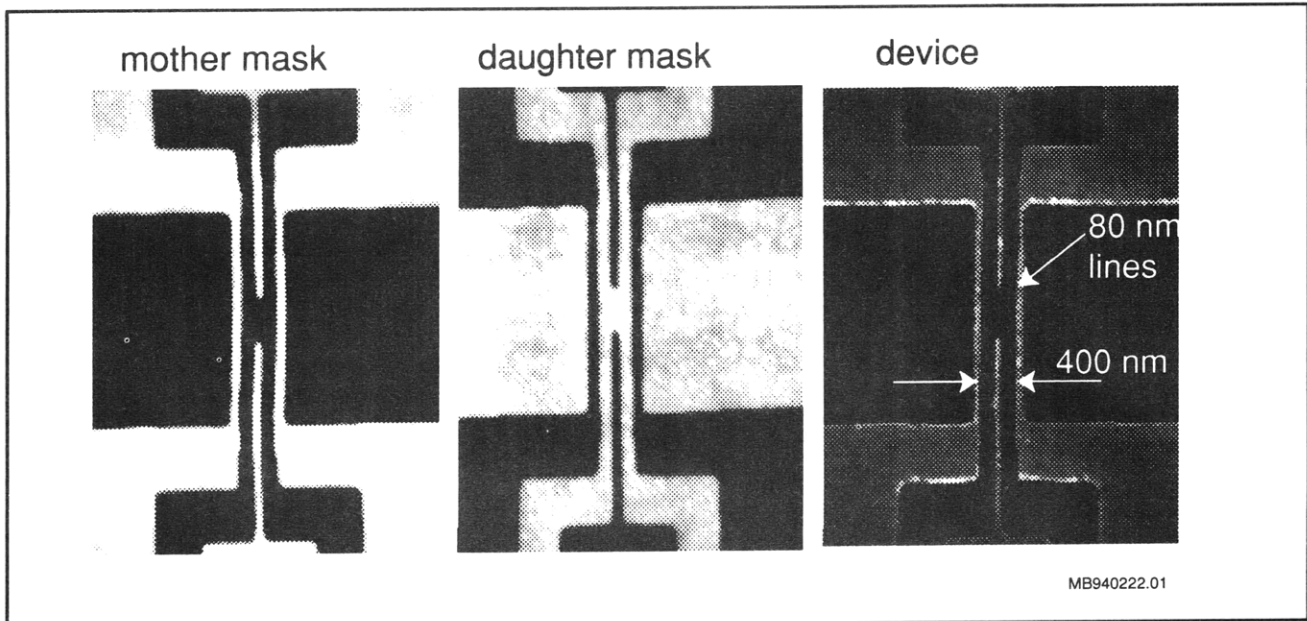


Figure 6. Masks used to fabricate a quantum tunneling device by x-ray nanolithography. (a) A "mother" mask is first written by e-beam lithography at the Naval Research Laboratory, and electroplated in Au at MIT. (b) This mask is then replicated onto a second x-ray mask to produce a "daughter" of opposite polarity, and electroplated to 200 nm Au thickness. The final device on a GaAs substrate is produced by liftoff of Al following x-ray exposure and development.

5.6 A High-Precision Mask Alignment System

Sponsors

Advanced Research Projects Agency/
Naval Air Systems Command
Contract N00019-92-K-0021
Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038

Project Staff

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In order for any lithographic technique to be of general utility, a compatible alignment technique must also be provided. The technique must be capable of superposition precision that is a small fraction of the minimum feature size. Previously, we demonstrated a new scheme for aligning x-ray masks to substrates that was based on the principle of on-axis interference from gratings on the mask and substrate that differ in spatial period (e.g., p_1 on mask, p_2 on the substrate). The interference pattern was compared in spatial phase to a fixed

fiducial on the mask using a CCD camera and frequency domain image analysis. An alignment standard deviation of 6 nm was achieved. The goal of the present work is threefold: first, to improve the superposition precision by an order of magnitude; second, to fully automate the alignment process; and third, to make the system compatible with industrial x-ray lithography sources and steppers. In order to improve the superposition precision, a new alignment mark was designed that consists of two adjacent gratings on the mask (p_1 and p_2) facing two complementary gratings on the substrate (p_2 and p_1). The resulting on-axis interference pattern consists of two sets of fringes of the same spatial period which move in opposite directions. By matching them in spatial phase, one achieves alignment. We believe that in conjunction with a CCD and appropriate image processing, a superposition precision below 1 nm can be achieved.

The alignment system under development is shown in figure 7. It incorporates a large-travel closed-loop wafer stage that can accept eight-inch wafers and a six-axis mask stage which uses closed-loop piezos to achieve subnanometer positioning. All stages are under unified computer control.

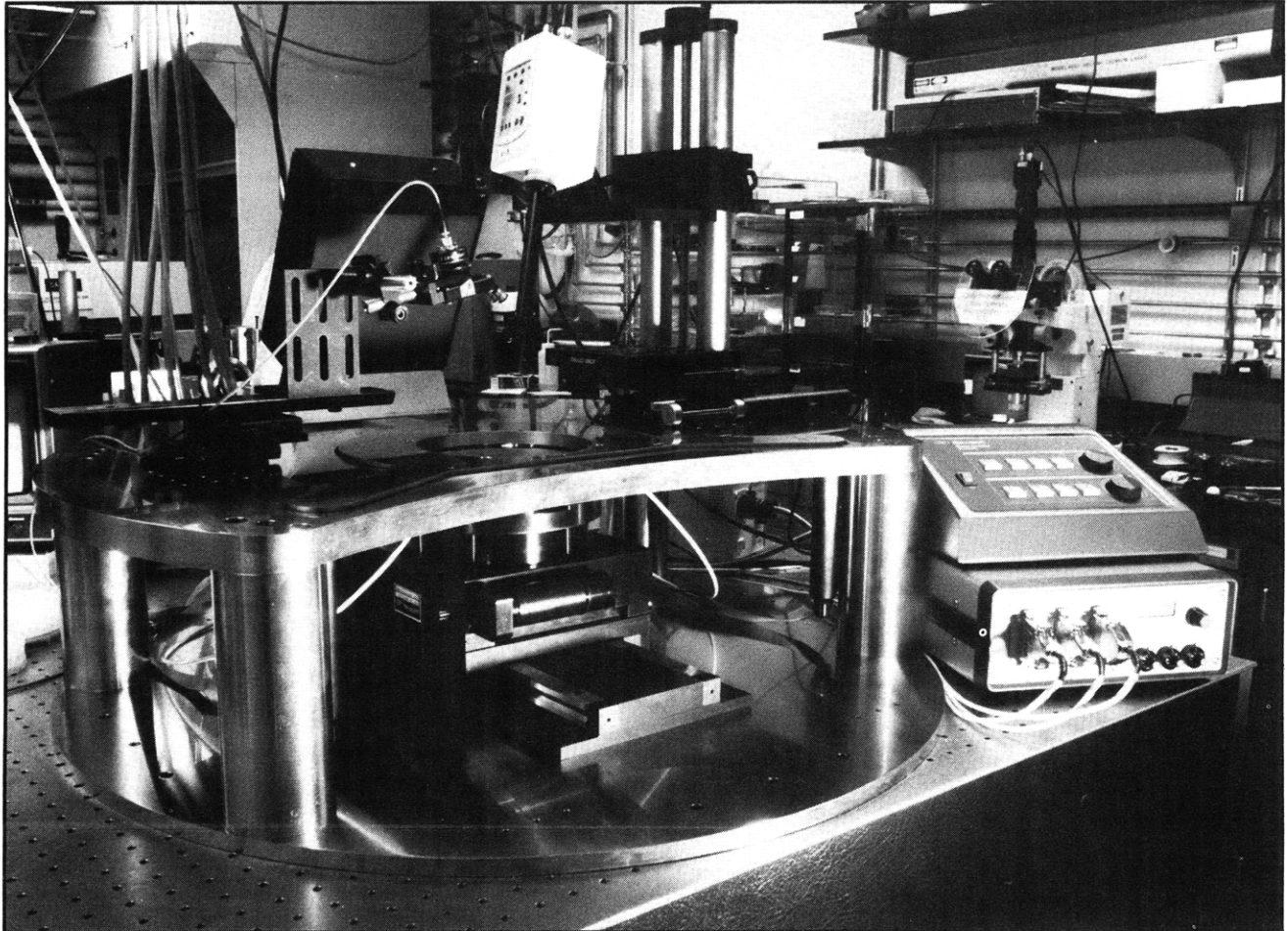


Figure 7. Photograph of the x-ray mask alignment system under development. The six-axis mask stage, which can accept up to eight-inch wafers, is controlled by closed-loop piezos. Light beams are brought in from the side onto grating type alignment marks. Alignment is determined by interpreting the resulting back diffracted fringe pattern. The system should be capable of nanometer alignment. The x-ray source, not shown, is located above the staging. (Photo by John F. Cook)

A collimated, polychromatic laser beam is diffracted by a pair of gratings on the mask and wafer. The gratings are arranged so that counterpropagating interference patterns are imaged with a compact microscope and CCD in an off-axis configuration, as shown in figure 8. The microscope can be positioned in a variety of ways, depending on the type of alignment mark in use. In all cases, the microscope is positioned out of the way of the x-ray beam. This configuration is compatible with industrial practice. A further advantage of the off-axis setup is that the reflected component of the incident

beam is not part of the alignment signal. This dramatically increases the contrast of the image, which, in turn, yields higher accuracy and faster phase detection.

For any alignment scheme to be useful in VLSI manufacturing, it must be highly accurate and insensitive to overlayers on the wafer, such as resist, SiO_2 , or polysilicon. We have demonstrated that due to the symmetric combination of the diffracted orders in the interference pattern, the relative and absolute phase of the alignment fringes are unaffected by dielectric overlayers.

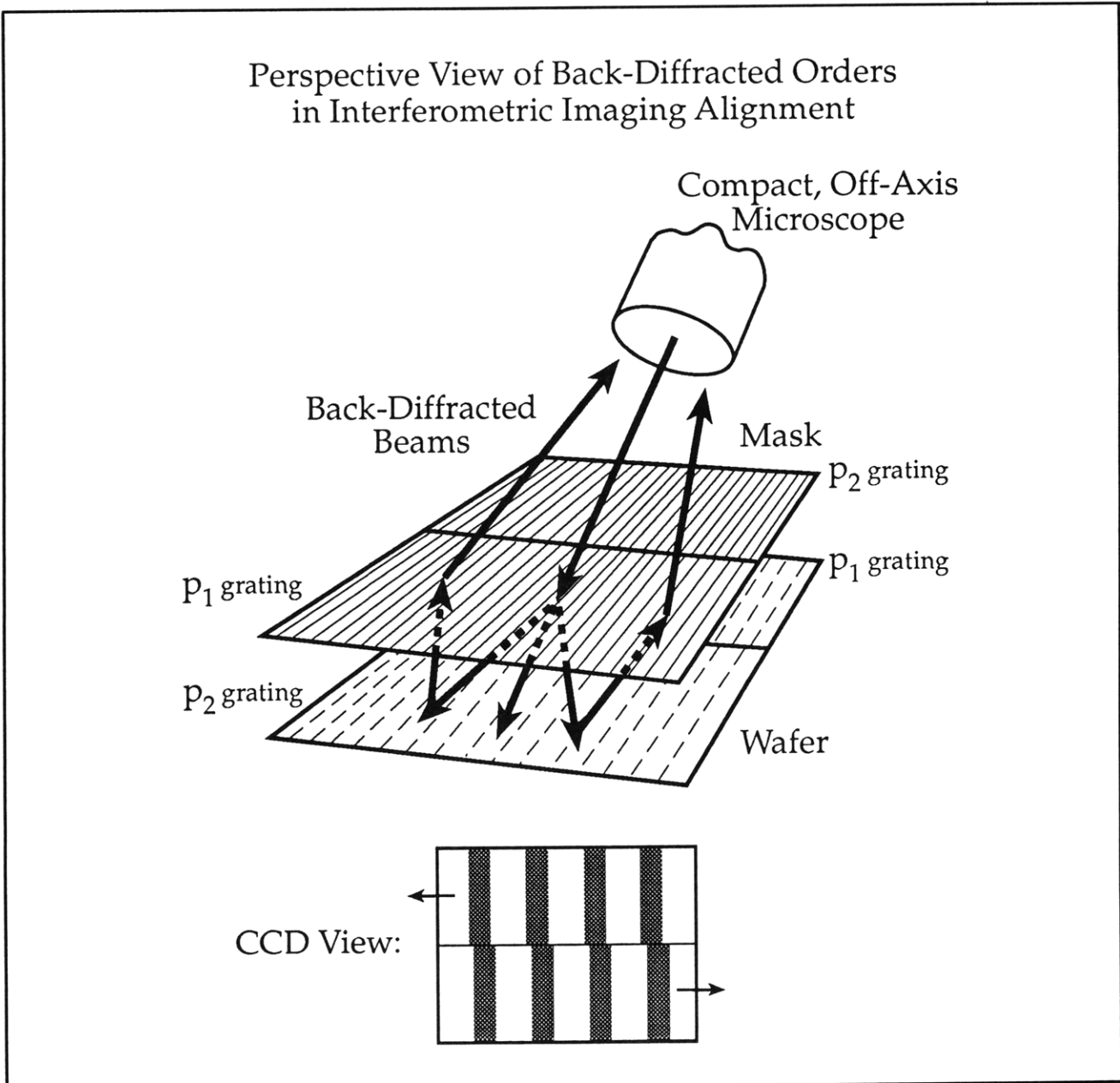


Figure 8. Schematic of the principle of the interferometric imaging alignment scheme showing the grating pairs and the beams back diffracted into the alignment microscope.

5.7 Interferometric Lithography

Sponsors

Joint Services Electronics Program
 Contract DAAL03-92-C-0001
 Grant DAAH04-95-1-0038
 National Aeronautics and Space Administration
 Contract NAS8-36748
 Grant NAGW-2003

Project Staff

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Interferometric (also called holographic) lithography schemes are preferred for the fabrication of periodic and quasi-periodic patterns that must be spatially coherent over large areas, and free of phase errors. For spatial periods down to 200 nm an argon ion laser is used in a Mach-Zender configuration, with a unique fringe-locking feedback system. This

produces large area (10 cm diameter) gratings with long-range spatial-phase coherence, free of phase errors or detectable distortion. The fringe locking ensures reproducibility of exposure. A multiple exposure moiré technique is used to verify freedom from distortion.

For spatial periods below 200 nm, light sources with wavelengths below 200 nm must be used. Such sources have limited temporal coherence, and thus one is forced to employ an achromatic scheme such as shown in figure 9. The source is an ArF

laser (193 nm wavelength). A collimating lens and a slit scanning system are interposed between the source and the interferometer in order to achieve reasonable depth-of-focus. We also use a white light interference principle to ensure that the gap between the two quartz plates is equal to the gap between the second plate and the substrate. Using this system, gratings of 100 nm period (nominally 50 nm lines and spaces) are obtained in PMMA on top of a specially designed antireflection coating. As shown in figure 10, such patterning is successfully transferred into Si_3N_4 .

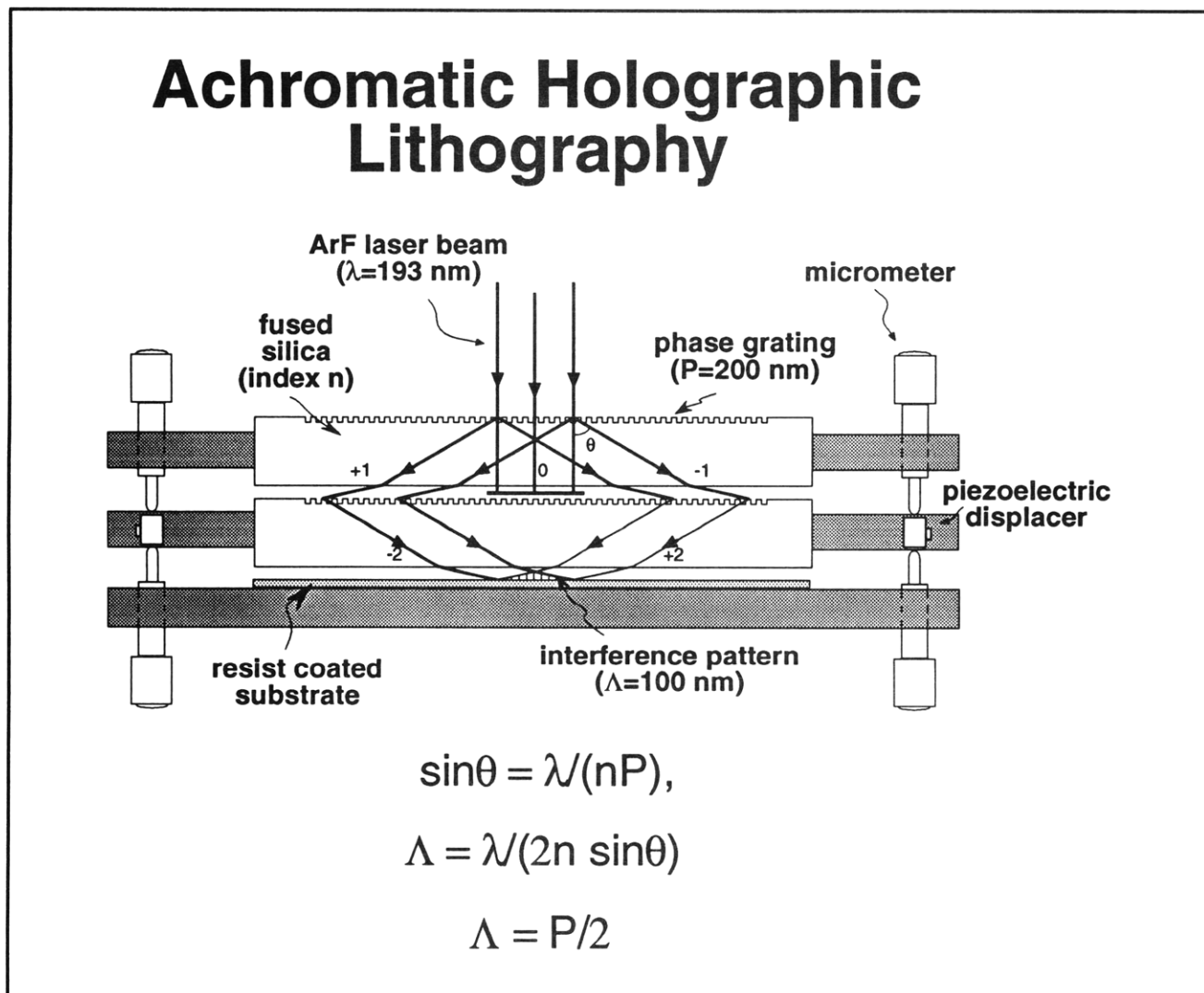
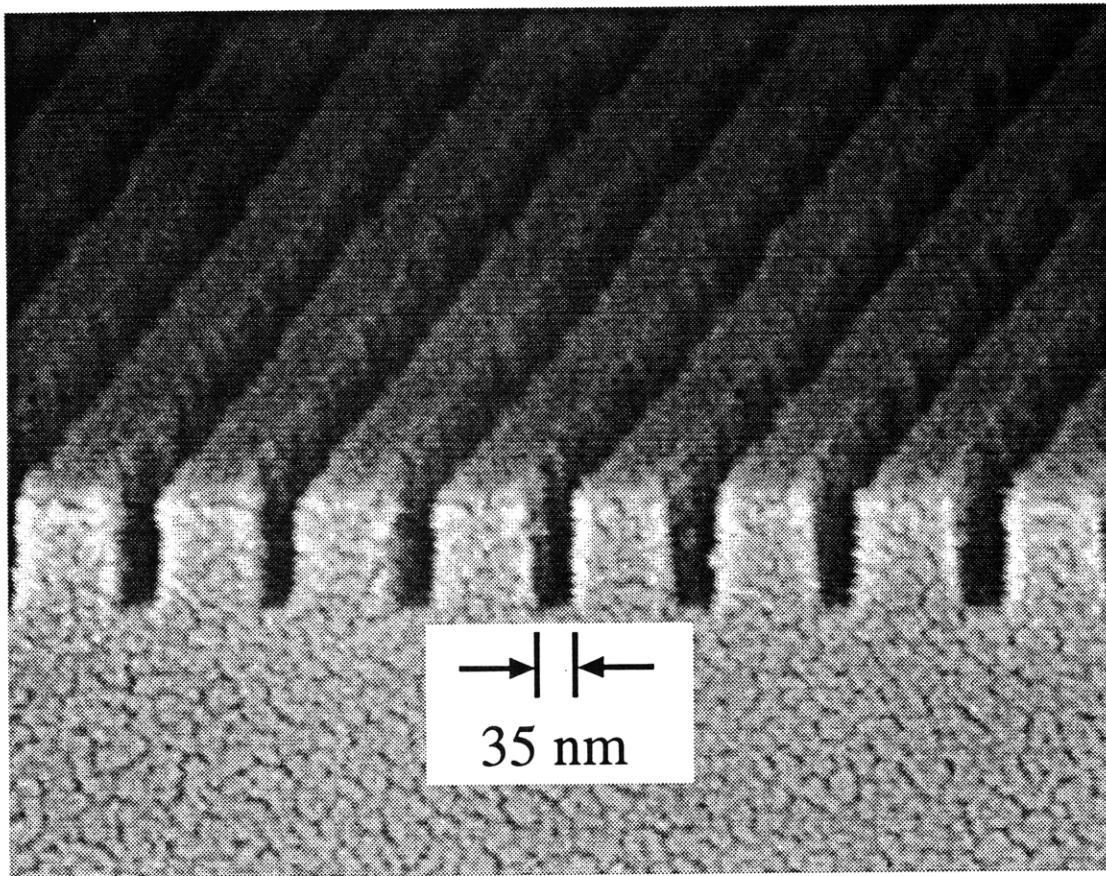


Figure 9. Achromatic interferometric lithography (AIL) configuration.



100 nm-Period Grating in Si_3N_4 on Si

Figure 10. Scanning electron micrograph of a 100 nm period grating, exposed in PMMA on top of a specially designed antireflection coating, and transferred into Si_3N_4 by reactive ion etching.

5.8 Ion-Beam Lithography

Sponsor

Joint Services Electronics Program
 Contract DAAL03-92-C-0001
 Grant DAAH04-95-1-0038

Project Staff

Scott E. Silverman, Anto Yasaka, Professor Henry I. Smith

Focused-ion-beam (FIB) systems are potentially useful as nanolithography tools because of the near absence of backscattering, which is a significant problem in electron-beam lithography, especially on high-atomic-number substrates. We currently work with Si^{++} and Be^{++} ions and have demonstrated 50

nm lines and spaces. We are investigating the feasibility of combining spatial-phase-locking with FIB lithography. This could prove to be the superior technology for making x-ray nanolithography masks based on W absorbers, at linewidths below 70 nm.

5.9 High-Performance Self-aligned Sub-100 nm MOSFETs Using X-ray Lithography

Sponsors

Advanced Research Projects Agency/
 Naval Air Systems Command
 Contract N00019-92-K-0021
 IBM Corporation
 Contract 1622

Joint Services Electronics Program
 Contract DAAL03-92-C-0001
 Grant DAAH04-95-1-0038

Project Staff

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 Professor Dimitri A. Antoniadis, Professor Henry I. Smith

We have fabricated sub-0.1 μm N-channel MOSFET devices on bulk Si using x-ray lithography. Extremely well controlled short-channel

effects were achieved through appropriate channel and source/drain engineering. Figure 11 shows the device schematic. The retrograde channel doping profile was accomplished using shallow indium and deep boron implants. The source/drain halo extensions were formed using a low-energy arsenic implant with indium preamorphization and counter-doping. The self-aligned polysilicon gates were fabricated using x-ray nanolithography and an anisotropic etching process. The aligned microgap x-ray exposures were carried out using mesa-etched SiN_x x-ray masks with Au absorber pattern. Figure 12 shows the I-V characteristics of an 85 nm channel length MOSFET.

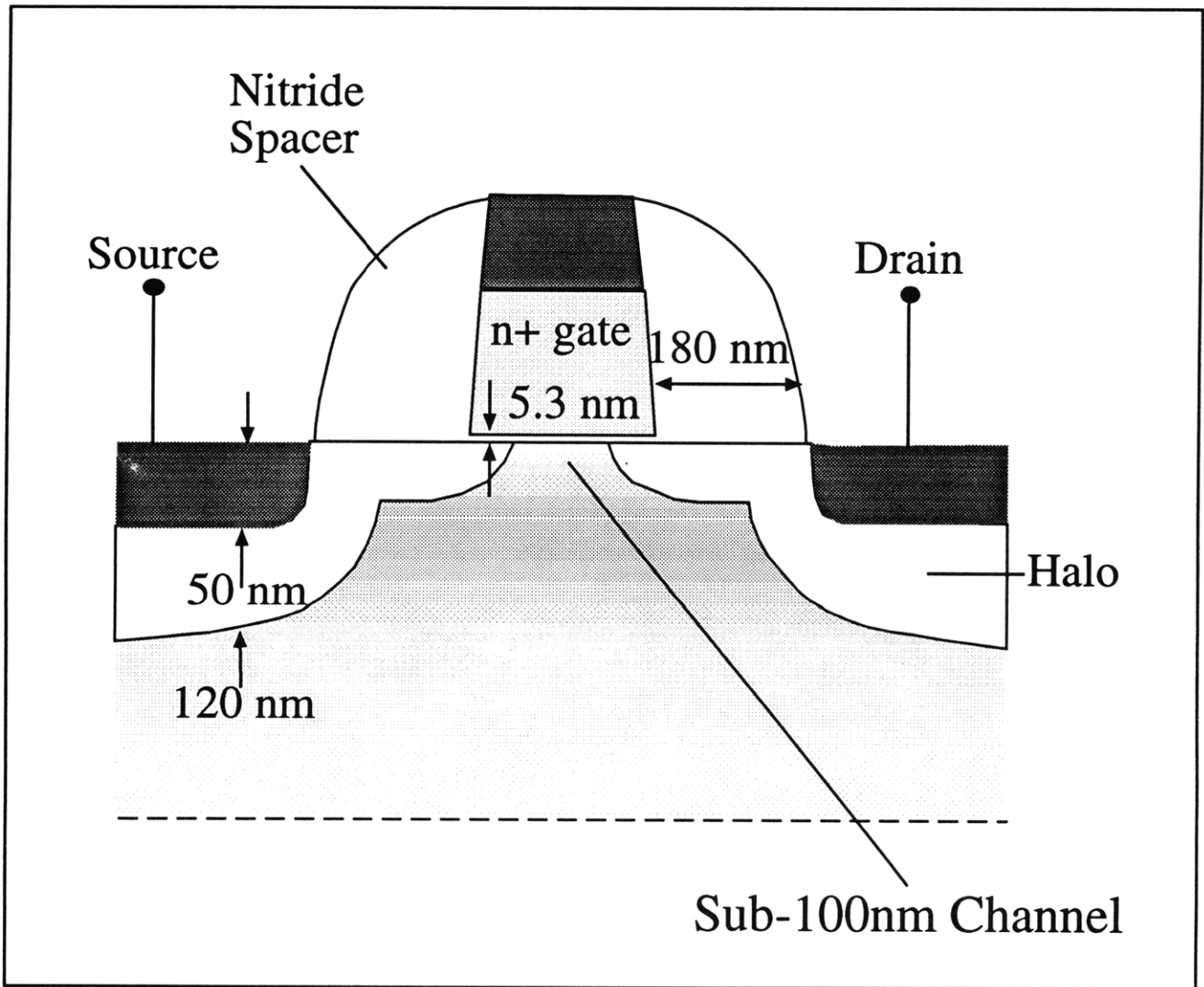


Figure 11. Schematic of 0.1 μm channel-length self-aligned NMOSFET.

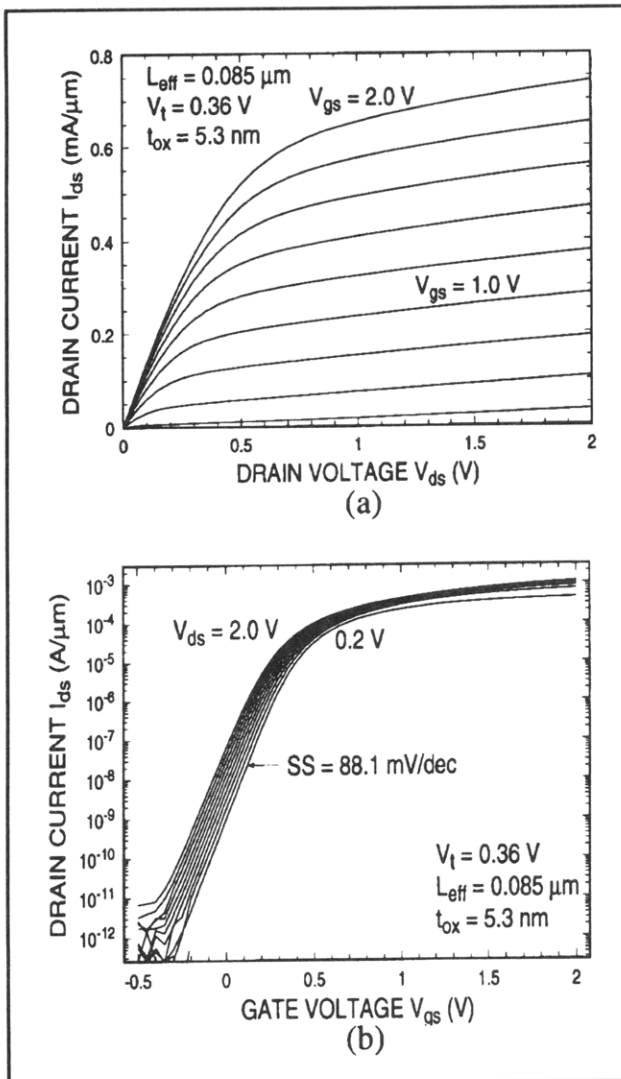


Figure 12. I-V characteristics of an 85 nm-channel-length NMOSFET.

Our current work involves the extension of this technology to a full CMOS line on bulk as well as on SOI substrates. Two different device structures are explored on the SOI substrates. One is the conventional structure on SOI, and the other is the double-gated structure with a deep submicron dimension top gate and a wider bottom gate. Our first effort is to get a fundamental understanding of these devices in DC; i.e., short channel effects, drain-induced barrier lowering (DIBL), coupling of the backgate to the front gate, etc. Currently, the backgate is defined by ion implantation through the top using optically exposed thick resist as the mask. The top gate is then aligned over this bottom gate via x-ray lithography. The technology issue here is the mixing and matching of the optical stepper to the e-beam tool which writes the patterns on the x-ray masks. We have developed a technique to do this matching that also saves e-beam writing time. Figure 13 shows this process in which the coarse patterns, e.g., pads and e-beam field alignment marks, are first transferred onto a chrome coated quartz wafer using the optical stepper. The pattern is then transferred into chrome by a wet etch. A one-to-one pattern transfer of the coarse features onto the x-ray mask is then done using proximity 240 nm UV exposure. The coarse patterns and the field alignment marks are then plated up in Au and sent to the e-beam for fine pattern writing. The final patterns on the mask will have coarse features patterned by UV proximity printing and fine features written by e-beam lithography, as depicted in figure 13(c).

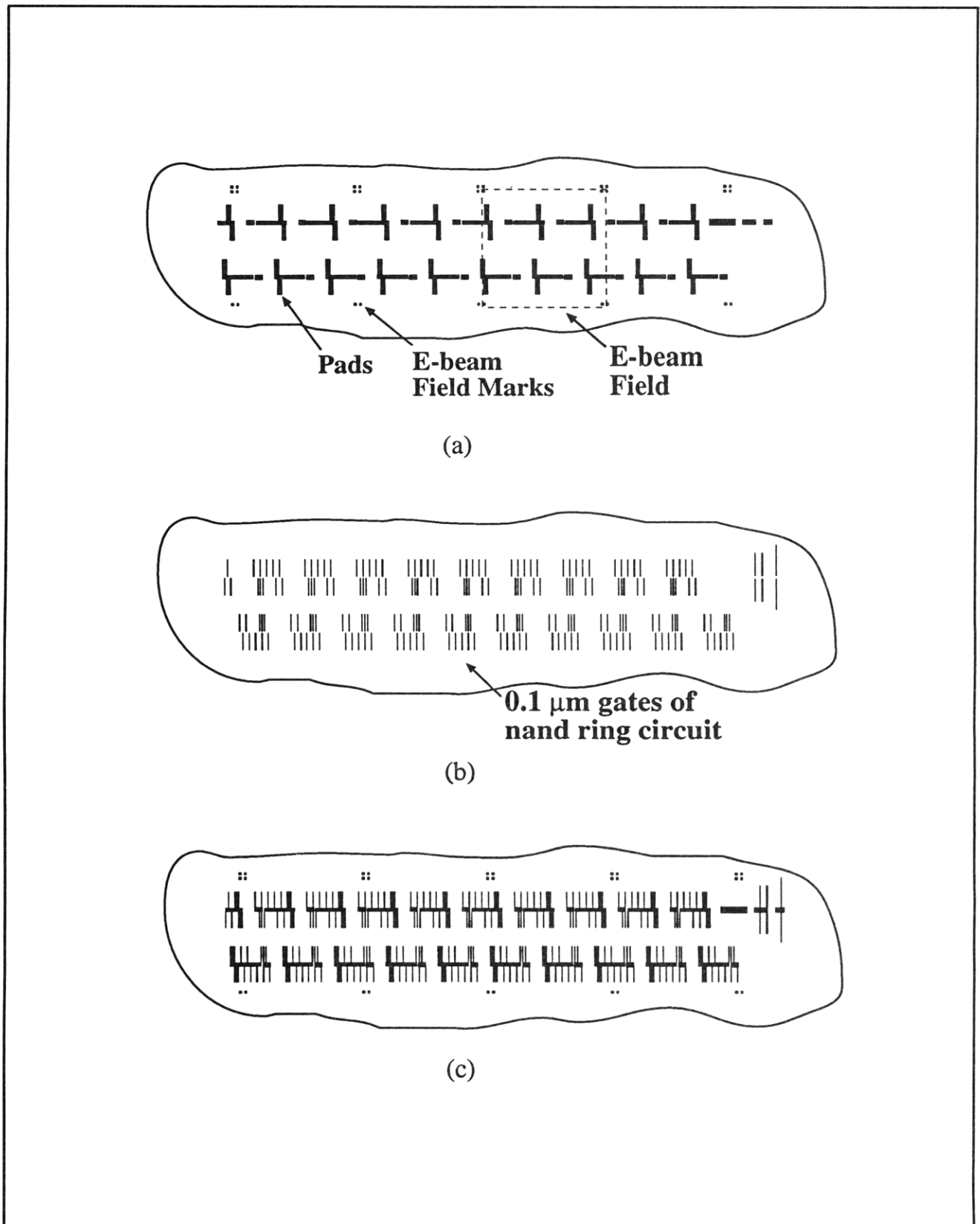


Figure 13. Sketch of a small portion of the chip showing: (a) a pattern of coarse features (pads) transferred onto the x-ray mask by deep UV lithography; (b) fine features written by e-beam lithography; (c) composite of fine and coarse features on the x-ray mask. The pattern is a nand ring circuit.

5.10 Fabrication of T-gate Devices using X-ray Lithography

Sponsor

U.S. Army Research Office
Grant DAAH04-94-G-0377

Project Staff

Nitin Gupta, Professor Henry I. Smith

Monolithic microwave integrated circuits (MMICs) have potential applications in automobile navigation, collision-avoidance, and personal wireless communication systems. High-speed MODFET devices require very short gate lengths, while preserving low resistance. Large gate widths are required for high current drive. To meet these conflicting demands, so-called "T-gate" and "gamma-gate" processes are used in which the base of the gate is very short (~100 nm) while the upper part is large and overlaps the short base, similar to a mushroom, or the letters T or Γ . Such structures are readily achieved using direct-write electron-beam lithography (EBL). However, this technology is expensive, slow, and unlikely to meet future production volume needs. For these reasons, we are developing a process for fabricating T-gates using x-ray lithography.

Previously, we reported on a tri-level PMMA-based process for fabricating T-gate devices using x-ray lithography. Recently, we have pursued a more robust process, offering the advantages of throughput as well as large process latitude. SAL-601, a commercially available negative chemically-amplified resist, is used. In order to maintain a large process latitude the time and temperature of the baking steps used in the fabrication are tightly controlled by means of vacuum-chucked hotplates, with the temperature monitored using thermocouple junctions integrated into a Si wafer. The result is a stable, robust process.

The fabrication sequence is shown in figure 14. The first layer defines the footprint of the gate, the critical parameter for a field-effect device. After developing this fine-linewidth feature, the resist is baked to increase the degree of cross-linking, thereby making the resist insoluble in its own casting solvent. A second layer of SAL-601 or ordinary photoresist is spun on and used to define the upper portion of the gate. This may be aligned symmetrically to the lower feature, or shifted to

achieve the Γ -gates used in high-end microwave devices. Following development, metal is evaporated and liftoff completed. Results are shown in figure 15.

There are a number of interesting directions that may be followed once a high latitude process is established. For manufacturable MMIC systems, both MESFETs and HEMTs are required for low-noise and power applications. Initially, relatively simple GaAs MESFETs will be studied, followed by GaAs and InP HEMTs of varying degrees of complexity. Further studies could include low-temperature-grown GaAs MESFETs for high breakdown voltages, self-aligned devices, or gate materials other than Au, such as W.

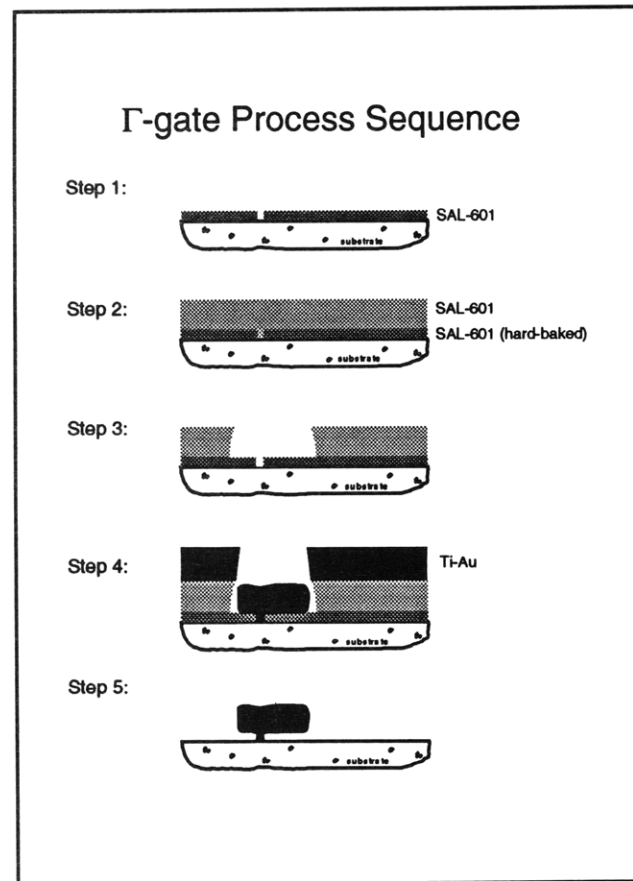


Figure 14. Depiction of the steps of the T-gate process: (1) chemically amplified resist is applied and exposed using x-ray lithography, (2) the exposed resist is hard-baked and a second layer of resist applied, (3) the second layer is exposed using either UV or x-ray lithography, (4) metal is deposited, typically Ti/Au, (5) liftoff, i.e., the resist is removed.

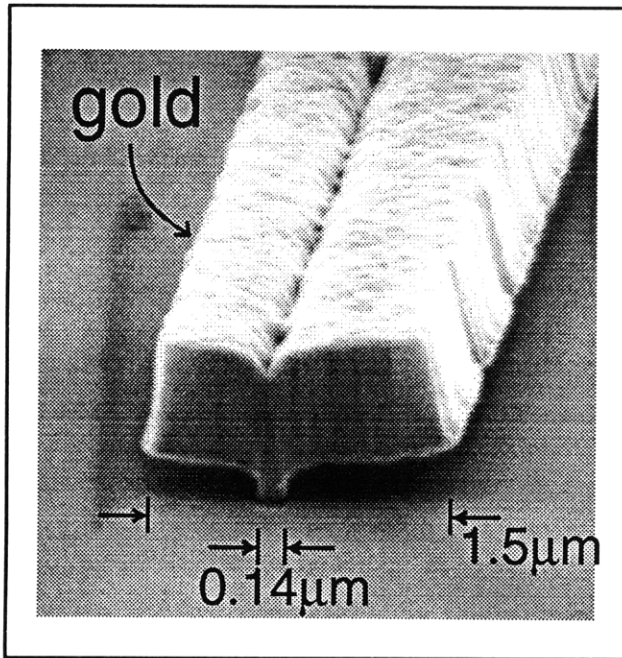


Figure 15. Scanning-electron micrograph of a T-gate obtained by the process depicted in figure 14.

5.11 Studies of Coulomb Charging Effects and Tunneling in Semiconductor Nanostructures

Sponsors

Joint Services Electronics Program
 Contract DAAL03-92-C-0001
 Grant DAAH04-95-1-0038
 U.S. Air Force - Office of Scientific Research
 Grant F-49-620-92-J-0064

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Quantum-effect devices, whose minimum feature sizes are comparable to the Fermi wavelength (about 50 nm in a typical inversion layer), have promising potential in novel electronics applications. Quantum-dot devices have drawn particular atten-

tion. In such devices an electron gas is confined electrostatically in all three dimensions, forming a small "island" of electrons ~ 100 nm, bounded on all sides by potential walls. This small electron "island" resembles an atom in that there can be only an integer number of electrons, and these electrons can occupy only certain discrete energy levels. If two dots are coupled, a structure resembling a molecule is obtained. The conductance of the dot, when connected to leads through tunneling barriers, exhibits strong oscillations as the voltage of the gate is varied. Each successive conductance maximum corresponds to the addition of a single electron to the dot. At temperatures in the mK range, the conductance decreases by orders of magnitude between adjacent conductance maxima because there is a large energy cost for an electron in the lead to enter the dot. This energy cost can be removed by changing the gate voltage, resulting in the observed periodic dependence of the conductance on gate voltage. This depends on how fast the chemical potential within the dots is changed for a change in gate voltage. For two arbitrary dot sizes and very low temperature, the conditions for conductance through the dots are arbitrary, and conductance events are expected to be stochastic.

A quantum dot device that provides control over the size of the dot was fabricated and measured in various biasing situations. Figure 16 shows an SEM micrograph of the device, and a schematic of the biasing configurations. A two-dimensional electron gas (2DEG) is formed at the interface of a GaAs/AlGaAs heterostructure approximately 55 nm below the sample surface. A negative voltage applied to Schottky gates at the surface depletes the 2DEG below, forming the quantum dot. With this structure it is possible to produce dots of 200, 400 or 600 nm length. The 200 and 400 nm dots can be biased simultaneously, producing a coupled dot system. The conductances are measured at 300 mK and plotted for these four cases in figure 17. The change in gate voltage necessary to add one electron to a quantum dot depends on the magnitude of the coupling capacitance between the dot and the gate. Accordingly, the distance between conductance peaks becomes very large for very small dots and small capacitances.

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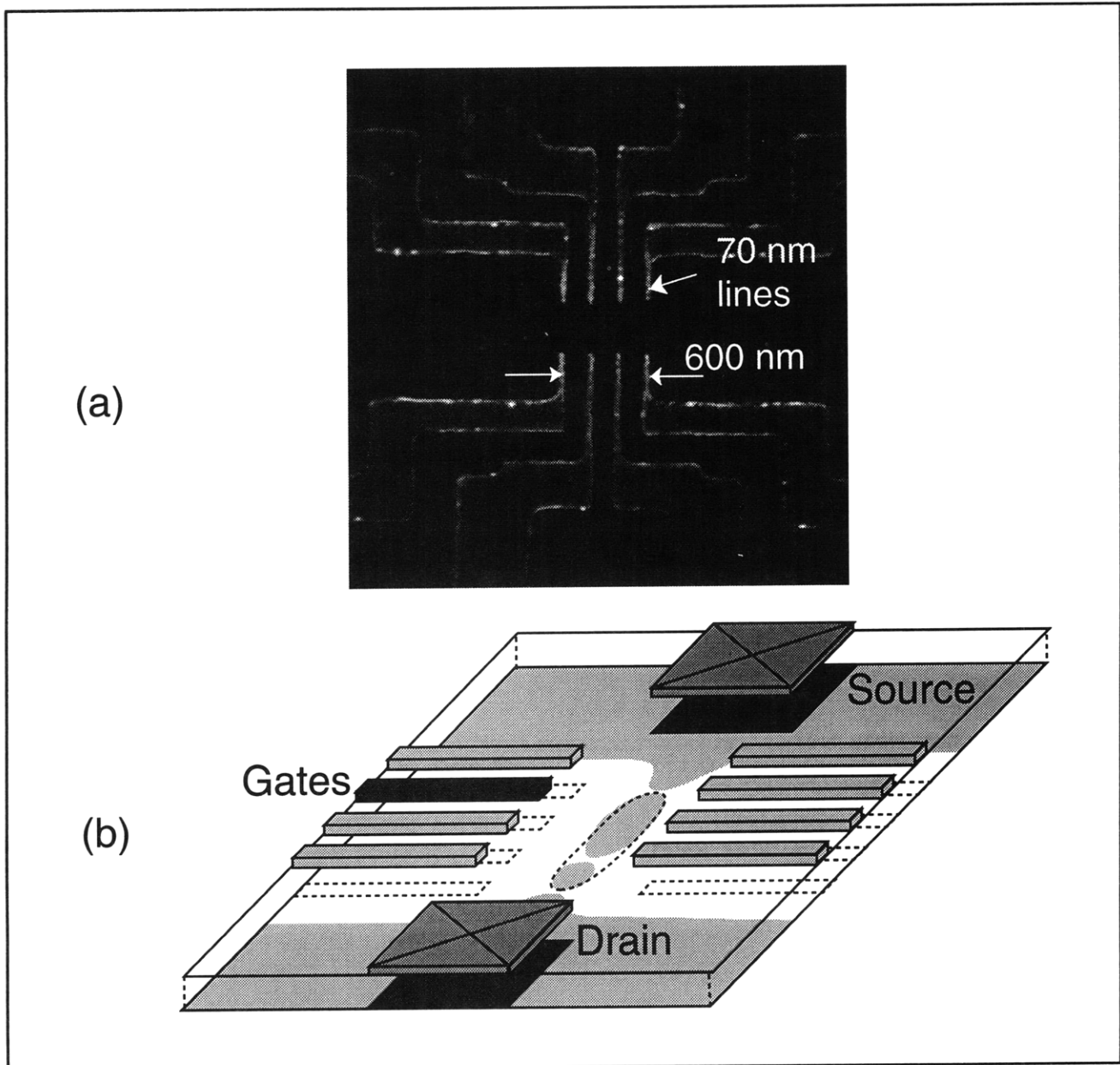


Figure 16. (a) Variable sized quantum-dot device made using x-ray nanolithography. (b) The device can be biased to achieve several different dot-sizes. The center-to-center distance between tunneling barriers can be set to 200, 400, or 600 nm. Alternatively, the biasing can produce two coupled quantum dots in series.

For two quantum dots in series, the conductance peaks are sparse for very negative gate voltages because the small dot suppresses conduction. For less negative voltages, the conductance maxima are spread due to the opening of the tunneling bar-

riers, and the smaller dot becomes conducting between the peaks, similar to the small dot measured by itself. In this case, we observe a modulation of the long periodicity of the small dot and the short periodicity of the larger dot.

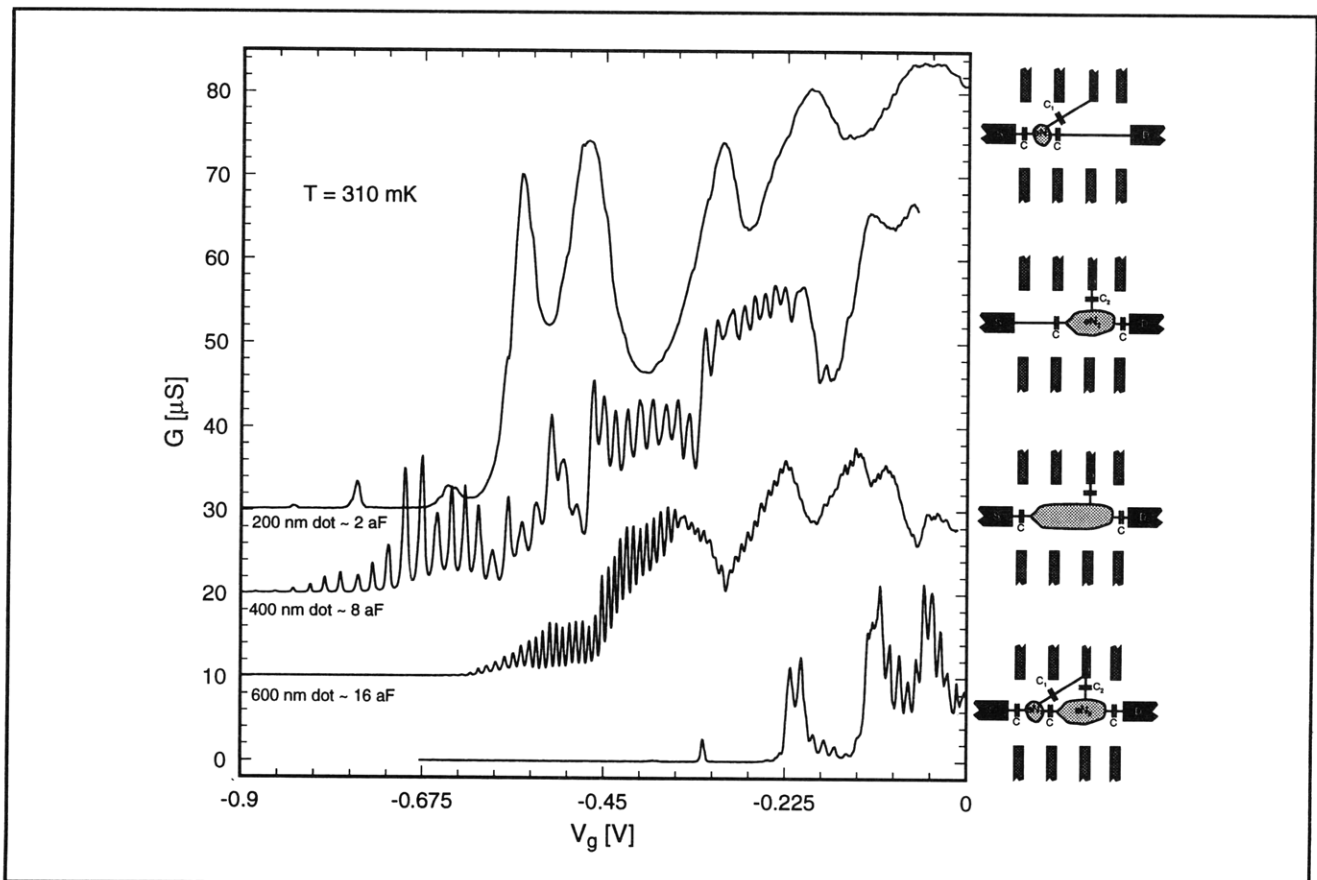


Figure 17. Conductance as a function of gate voltage for three different quantum-dot sizes and for a double dot system. The distinct peaks correspond to adding a single electron to a dot.

5.12 Superconductor/Semiconductor Interface of V_3Si and Si

Sponsor

Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038

Project Staff

James J. Hugunin, Professor Dimitri A. Antoniadis, Professor Terry P. Orlando, Professor Henry I. Smith

Superconductor/semiconductor contacts are fabricated between V_3Si and Si by a solid-phase reaction between SiO_2 and V. Auger spectroscopy is used to confirm the presence of the V_3Si phase, and the sheet resistance versus temperature of the device is measured to determine a superconducting transition temperature of 14 K.

The electrical properties of the V_3Si/Si interface are examined for cases where the V_3Si is in both

normal and superconducting states. The first two measurements are performed at room temperature and investigate the two forms of transport for normal electrons, either through or over a Schottky barrier. The second set of measurements are performed between 17 K and 0.3 K and examine the properties of this interface as the superconducting energy gap increases in the V_3Si . Each of these three experiments shows a Schottky barrier height of about 0.16 eV for the V_3Si/Si interface. In addition, the low temperature measurements confirm that this interface is that of a superconductor/semiconductor.

There are two anomalies in this experiment. First, the current flow through the contacts is approximately 10^6 times smaller than that expected for contacts of the given area, indicating some flaw in the fabrication process. Second, low temperature measurements reveal unexpected structure near 0.5 meV. It is speculated that this is related to the presence of a superconducting phase of another vanadium compound.

5.13 Laterally-Coupled Distributed-Feedback Lasers Fabricated by X-Ray Lithography

Sponsors

Joint Services Electronics Program
 Contract DAAL03-92-C-0001
 Grant DAAH04-95-1-0038
 U.S. Army Research Office
 Contract DAAL03-92-G-0291

Project Staff

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 Smith

Distributed feedback (DFB) lasers are essential components in future wavelength-division-multiplexed systems. These systems require transmitters that are tunable, that oscillate in a single longitudinal mode with narrow linewidths, and that are integrable with electronic circuitry such as detectors and field-effect transistors. In the fabrication of a typical DFB laser, an epitaxial regrowth step is carried out on top of the grating, a process that is often of low yield. In particular, because of etch back, the coupling constant after epi-growth can be difficult to predict. Figure 18 illustrates a

novel laterally-coupled DFB laser structure in which gratings are etched on both sides of the ridge waveguide. This structure eliminates the need for regrowth, and maximizes the utility of ridge-waveguide devices, which are much simpler to fabricate. Furthermore, the materials growth, grating fabrication and waveguide fabrication are decoupled, which should increase device yield.

We are working in collaboration with Lasertron, a commercial semiconductor-laser vendor in Burlington, Massachusetts, to fabricate both the first-order quarter-wave-shifted (QWS) and second-order uniform DFB lasers. First-order QWS-DFB lasers are attractive because they emit a single, well defined wavelength whereas uniform first-order DFB lasers can oscillate in one of two degenerate modes. In second-order uniform DFB lasers, the above degeneracy is broken by mode discrimination through radiation loss normal to the surface. Presently, we are working to better understand this phenomenon. The current view is that the discrimination arises from interference between the radiating waves. That is, on one side of the stopband these waves interfere destructively, while on the other side of the stopband they interfere constructively. The lasing wavelength emerges on the side on which the destructive interference occurs because of the lower radiation losses.

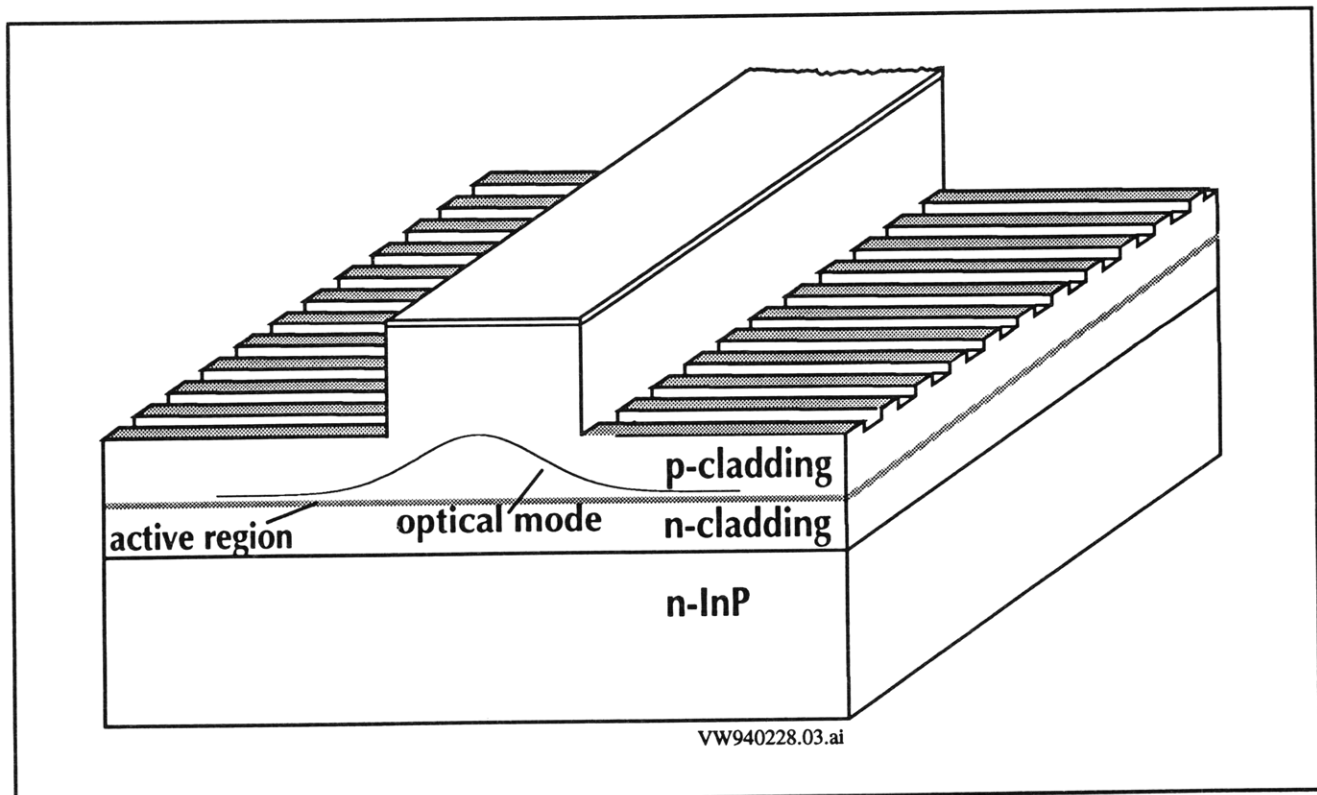


Figure 18. Schematic of a laterally-coupled distributed feedback laser.

To achieve laser action in the laterally-coupled DFB structure (figure 18) as well as reliable control of coupling from device-to-device, the lateral gratings should run right up to the ridge sidewall. Figure 19 shows the dependence of the coupling κ on the proximity δ of a first-order lateral grating ($\Lambda \sim 235$ nm) to the ridge sidewall of a 1.1 μm -high ridge waveguide laser structure for grating duty cycles (DC) of 0.5, 0.6, and 0.7. The ridge width and grating depth are 2.0 μm and 200 nm, respectively. As expected, the coupling decreases as the lateral gratings move away from the ridge sidewall. This decrease is attributable to the decreased overlap between the optical field and the grating. For reasonable values of κ ($\sim 20 \text{ cm}^{-1}$), the lateral gratings must be within 100 nm of the ridge sidewall. Lateral gratings that reside closer to the ridge sidewall also relax the tolerance on the grating duty cycle.

For deep-ridge waveguides, spun-on resist tends to build up significantly next to the sidewall, which at thicknesses greater than 1 μm presents a problem even for x-ray lithography. We are developing a process that uses ion implantation to eliminate such highly nonuniform resist thickness variations. By controlling the energy of the ion species one can

tailor the depth these ions penetrate a film, which in our case is PMMA. The proposed process is as follows. First, a thick planarizing layer of PMMA is spun onto the substrate containing the deep-ridge waveguides (i.e., 1.5 to 2 μm deep). Next, the substrate is implanted. The accelerating voltages are chosen so ions penetrate a certain depth into the PMMA, and the dose of the implantation is chosen so that enough energy is delivered to the PMMA film to cause chain scissioning. After development, a thin layer (~ 500 nm) of PMMA is left behind. This layer will have fairly uniform thickness up to the edge of the ridge sidewall, which alleviates the problem of varying x-ray absorption. Furthermore, it is equally applicable in cases where electron-beam lithography is performed over such deep topography.

Figure 20 shows experimental results from three separate phosphorous implantations into 1.5 μm -thick layers of PMMA. As expected, the depth removed can be tailored with accelerating voltage. Furthermore, negligible development occurs after 30 s, which implies precise depth control. Presently, we are collaborating with researchers at Genus, Inc., of Newburyport, Massachusetts, in developing this process.

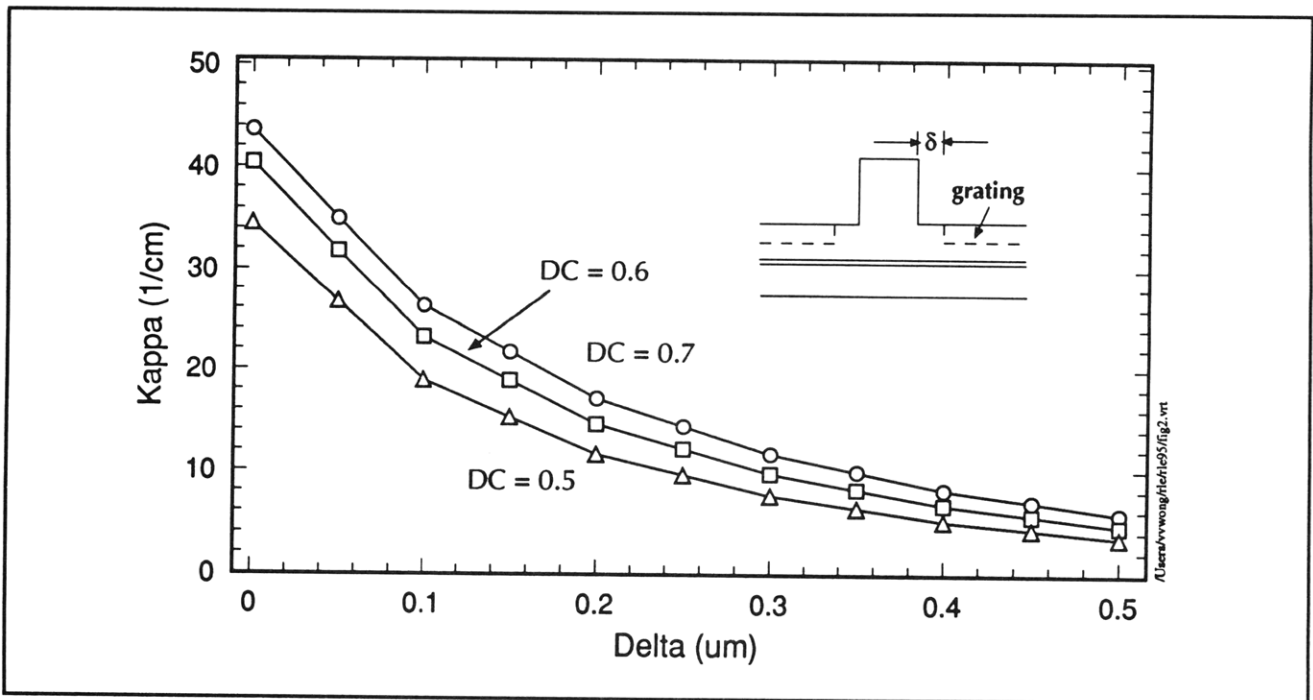


Figure 19. Coupling coefficient κ versus proximity δ of lateral grating to the ridge sidewall for a 1.1 micron-high ridge waveguide and grating duty cycles of 0.5, 0.6 and 0.7. The ridge width and grating depth are 2.0 microns and 0.2 microns, respectively.

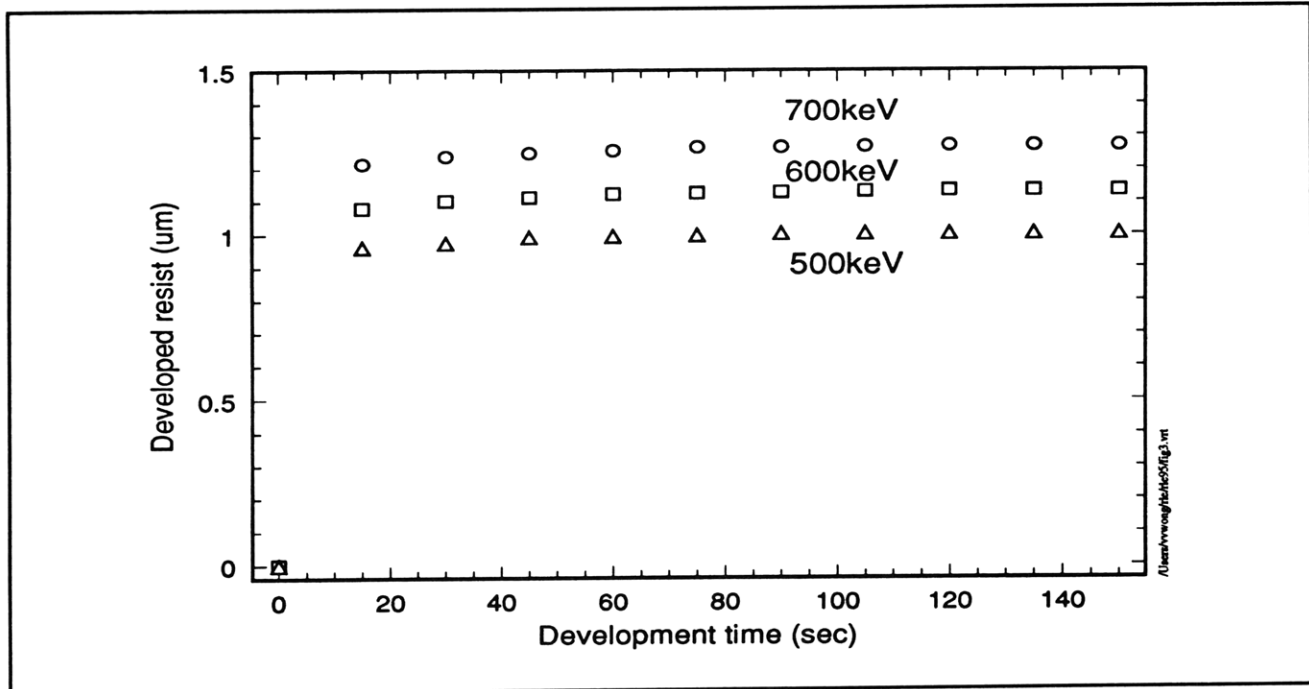


Figure 20. Plot of developed resist versus development time for three Phosphorous (P+) implantations into PMMA at energies of 500, 600, and 700 keV. The dose in all cases was 10^{13} cm^{-2} .

5.14 Combined Spatial-Phase-Locked Electron-Beam, X-ray, and Optical Lithography for Channel-Dropping Filters

Sponsor

Joint Services Electronics Program
 Contract DAAL03-92-C-0001
 Grant DAAH04-95-1-0038

Project Staff

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 Professor Hermann A. Haus, Professor Henry I.
 Smith

The integrated resonant channel-dropping filter (figure 21) was first proposed by Professor Hermann A. Haus in 1991 for use in wavelength-division multiplexed (WDM) fiberoptic communication systems. The function of the filter is to spatially separate, or "drop", just one channel from a WDM bit stream without terminating or otherwise disturbing the remaining channels. The WDM bit stream is carried along the center rib waveguide. Only that channel, or wavelength band, that excites the side-coupled quarter-wave shifted distributed Bragg reflector resonators is removed from the bus to the leftmost waveguide. The remaining channels travel through undisturbed.

As the first step towards demonstrating an integrated resonant channel-dropping filter we have fabricated highly coherent, high-Q, quarter-wave shifted distributed-feedback reflector (QWS-DBR) resonators in silicon-dioxide/silicon-nitride/silicon-dioxide (figure 22) and investigated their transmission characteristics. The grating patterns were written on an x-ray mask using spatial-phase-locked electron-beam lithography and transferred to the rib waveguides using x-ray nanolithography. With the first test chip we studied the grating strength, filter finesse, radiation loss, and spectral response as a function of grating length, depth, and width. A grating strength of 75 cm^{-1} , corresponding to a 3.6 nm-wide stopband, a maximum Q of 50,000, and a device-to-device resonant-location-repeatability of $\leq 0.05 \text{ nm}$ were demonstrated.

The selection of grating period and waveguide dimensional parameters for the in-line resonator in figure 22 were determined prior to fabrication by calculating the grating strength and effective index across a parameter space that spanned waveguide width and etch depth, given a set of core and cladding film thicknesses. Figure 23 maps contours of constant grating strength and period as a function of waveguide width and etch depth. A rib width of $2 \mu\text{m}$ and depth of $0.2 \mu\text{m}$ is expected to give a grating strength of 100 cm^{-1} and a center Bragg wavelength of 1550 nm for a 511 nm grating period.

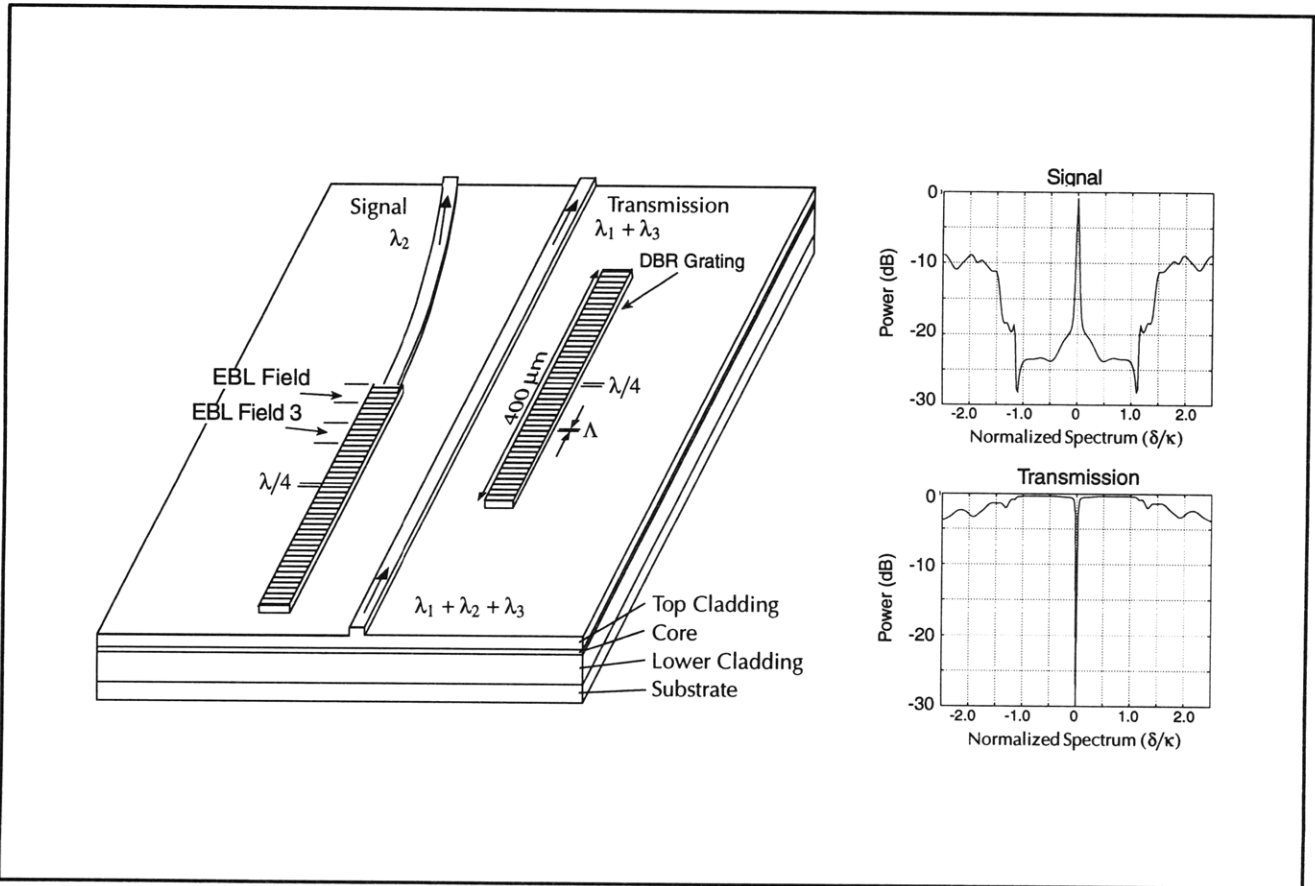


Figure 21. Schematic of the integrated resonant channel dropping filter (CDF).

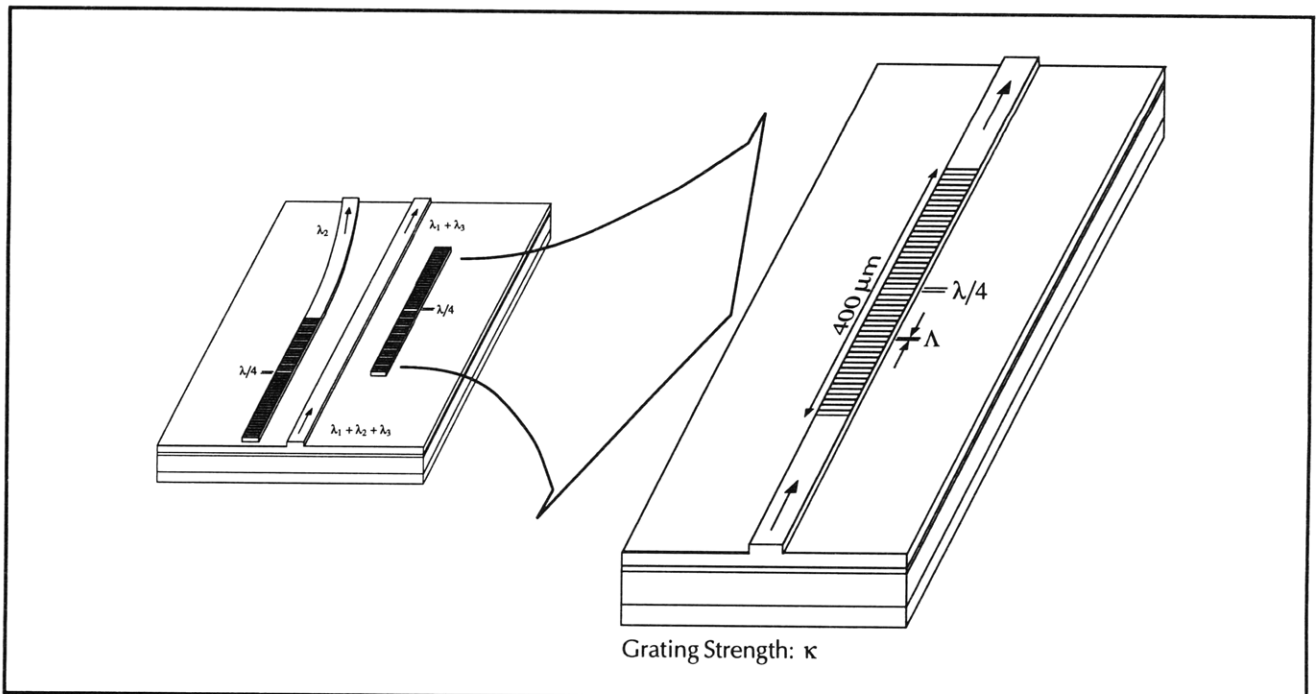


Figure 22. Left: The integrated resonant channel-dropping filter. Right: The key element of the filter, the quarter-wave shifted distributed Bragg resonator.

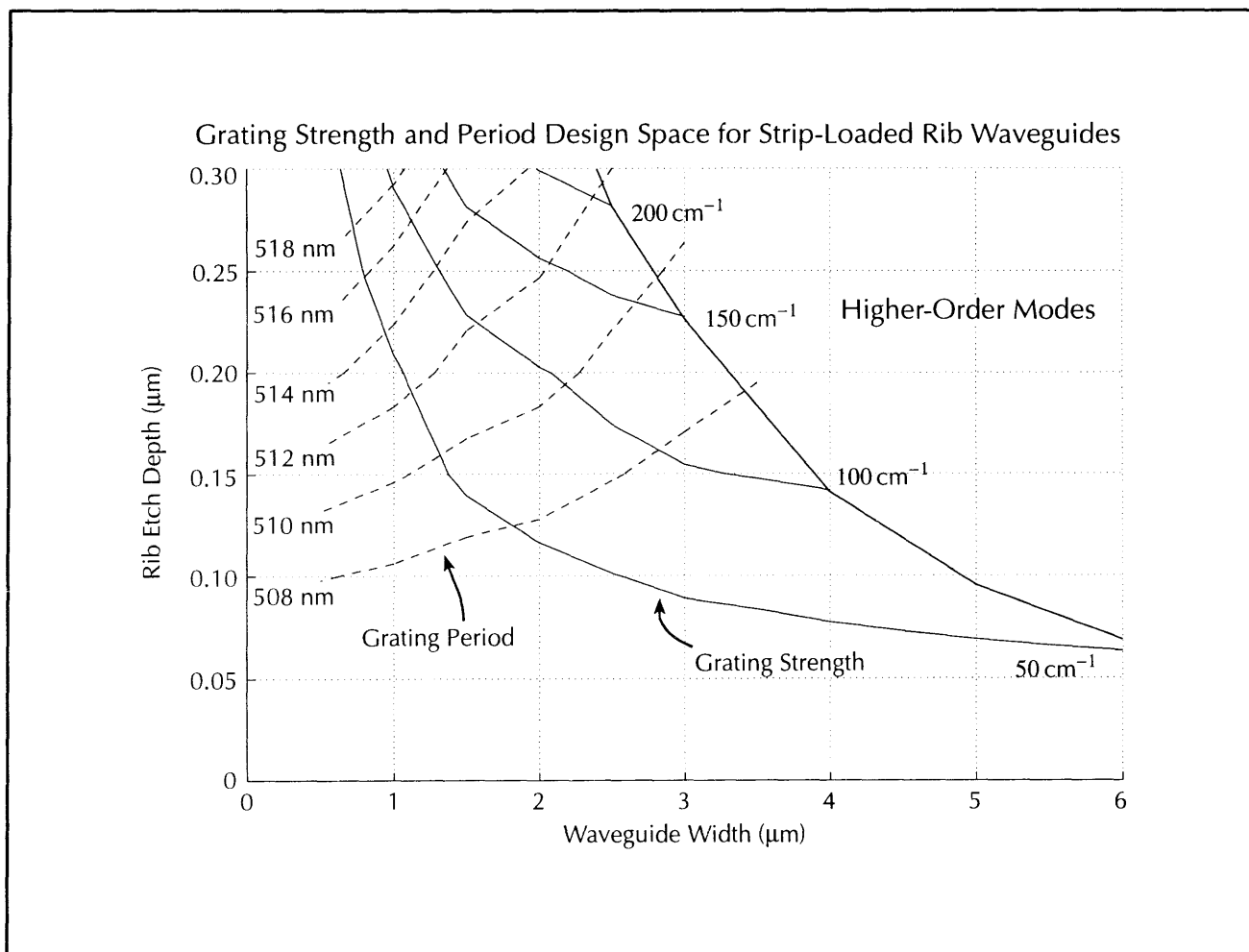


Figure 23. Design study of grating strength and grating period for a Bragg grating etched on top of a rib waveguide to a depth of one-half the rib etch depth. The Bragg wavelength is 1550 nm.

In order to achieve grating period control and arbitrary quarter-wave shift placement, the grating corrugation patterns must be produced by electron-beam lithography (EBL). However, in order for an EBL field to be sufficiently free of distortion and have small enough inter-pixel distance for the channel-dropping filter, the EBL field cannot be larger than about 100 μm. Since the grating lengths required by the channel-dropping filter extend beyond one EBL field, the grating patterns must be composed by stitching together several adjacent EBL fields. It has been calculated using a stochastic model that the standard deviation of EBL field placement precision must be better than 12 nm for a 511 nm period grating to have better than a

90 percent chance of writing a resonator with a line-width broadening of ≤ 10 percent and an offset of the spectral location less than one-quarter of the stopband width. Such high-coherence requirements demand the use of spatial-phase-locked e-beam lithography, which has demonstrated a field placement precision of $\sigma \leq 2$ nm.

The grating patterns are written on an x-ray mask for subsequent transfer to the rib waveguides. A self-aligned method is used to localize the grating patterns to the top of the rib waveguides and to simplify the alignment procedure. The devices were die-saw cut at a 6 degree angle with respect to the waveguide perpendicular axis and the facets were polished.

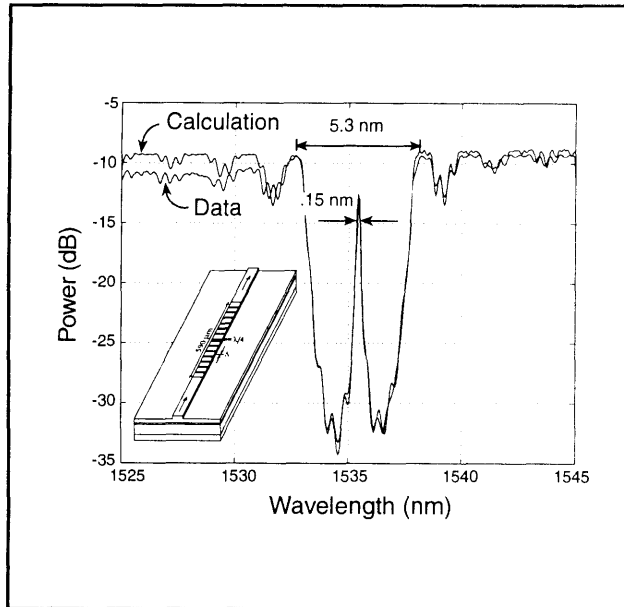


Figure 24. Overlay of measured and calculated transmission response of a 590 μm long, 9-e-beam-field resonator. The modulation fringes are due to Fabry-Perot effects. The resonance linewidth and stopband width are 0.15 nm and 5.3 nm, respectively. The deviation between the data and calculation on the blue side of the spectrum is due to grating-induced radiation loss.

Figure 24 shows an overlay of the transmission response of a QWS-DBR resonator with a full calculation of the expected response. The modulation fringes, present in the data and included in the calculation, are due to the Fabry-Perot cavity established between the grating end that faces the front facet and the front facet itself. Note that the resonance is very well centered within the stopband. The degree to which the resonance is centered is strongly dependent on the magnitude of the stitching errors between fields.

Figure 25 (inset) shows the resonance offset as measured on twelve resonators of different κL products and grating periods. The resonance deviations from center are within ± 1 percent of the stopband width. It is estimated from this data that the stitching errors along the gratings are $\sigma \leq 4$ nm, or $\leq \lambda/250$. These gratings are the most highly coherent e-beam-written Bragg gratings reported to date.

Figure 26 shows the transmission spectrum of five 513 nm-period resonators 5, 7, 9, 11, and 13 e-beam fields long. The resonance location of each device is 1535.4 nm. The Q-value ranges from 3,000 to 50,000 while the in-band baseline level is measurement limited.

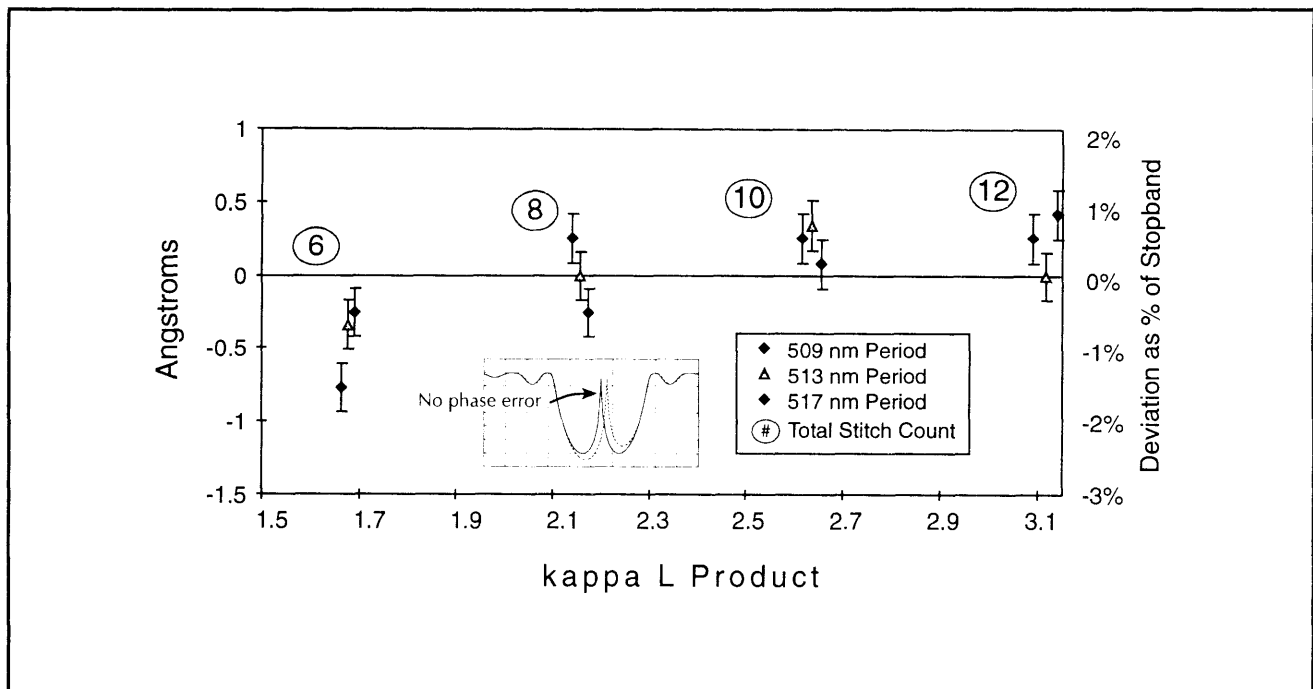


Figure 25. Measured resonance deviation from center of stopband for twelve devices with different periods and grating lengths. A 1 percent deviation corresponds to $\delta/\kappa = 0.02$. Inset shows the effect of a large stitching error (dashed) on the location of the resonance within the stopband.

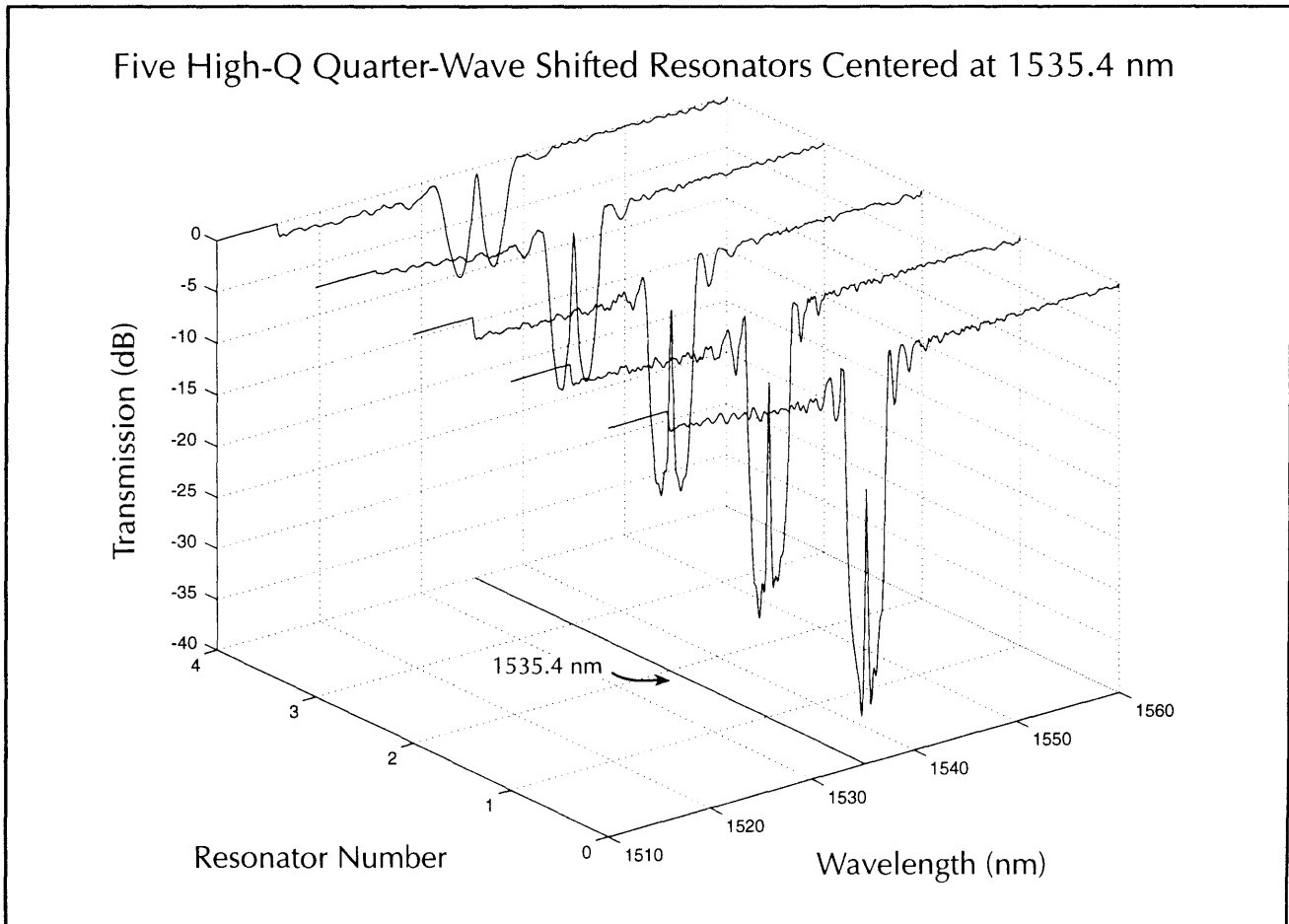


Figure 26. Five quarter-wave-shifted Bragg resonators 5, 7, 9, 11, and 13 EBL fields long, with 128 grating corrugations per field. The resonance location deviates by less than 0.05 nm from device to device.

5.15 High-Dispersion, High-Efficiency Transmission Gratings for Astrophysical X-ray Spectroscopy

Sponsor

National Aeronautics and Space Administration
Contract NAS8-36748
Grant NAGW-2003

Project Staff

Richard J. Aucoin, Robert C. Fleming, Dr. Mark L. Schattenburg, Professor Claude R. Canizares, Professor Henry I. Smith

Through a collaboration between the Center for Space Research (CSR) and the NanoStructures Laboratory (NSL), transmission gratings are provided for the Advanced X-ray Astrophysics Facility (AXAF) x-ray telescope, scheduled for launch on the NASA Space Shuttle in 1998. Many hundreds of large area, gold transmission gratings of 200 nm and 400 nm periods are required. In order to

achieve spectrometer performance goals, the gratings must have very low distortion. The gratings will provide high resolution x-ray spectroscopy of astrophysical sources in the 100 eV to 10 keV band.

The need for high grating quality and an aggressive production schedule demand the development of a robust, high-yield manufacturing process. We have adopted a scheme involving interference lithography with tri-level resist, followed by cryogenic reactive-ion etching and gold electroplating. A chemical etching step then yields membrane-supported gratings suitable for space use. The gratings undergo extensive testing before being released for use in the spectrometer.

A new cleanroom fabrication facility (the Space Microstructures Laboratory) on the 4th floor of Building 37 (adjacent to the Gordon Stanley Brown Building), has been constructed in order to fabricate the AXAF gratings. The proximity of the new lab to the MTL proper has allowed the lab to share many MTL services, such as DI, as well as process

water, nitrogen, process vacuum, and waste drains. The laboratory space includes 1700 sq-ft of Class 100 and associated support areas. A large complement of new equipment has been purchased and installed, and production of flight gratings is underway.

5.16 Submicrometer-Period Transmission Gratings for X-ray and Atom-Beam Spectroscopy and Interferometry

Sponsors

Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038
National Aeronautics and Space Administration
Contract NAS8-36748
Grant NAGW-2003

Project Staff

James M. Carter, Jeanne M. Porter, Timothy A. Savas, Dr. Mark L. Schattenburg, Satyen Shah, Professor Henry I. Smith

Transmission gratings with periods of 100-1000 nm are finding increasing utility in applications such as x-ray, vacuum-ultraviolet, and atom-beam spectroscopy and interferometry. Over 20 laboratories around the world depend on MIT-supplied gratings in their work. For x-ray and VUV spectroscopy, gratings are made of gold and have periods of 100-1000 nm, and thicknesses ranging from 100-1000 nm. They are most commonly used for spectroscopy of the x-ray emission from high-temperature plasmas. Transmission gratings are supported on thin (1 μm) polyimide membranes or made self-supporting ("free standing") by the addition of crossing struts (mesh). (For short x-ray wavelengths membrane support is desired, while for the long wavelengths a mesh support is preferred in order to increase efficiency.) Fabrication is performed by interferometric lithography combined with reactive-ion etching and electroplating. Progress in this area tends to focus on improving the yield and flexibility of the fabrication procedures.

Another application is the diffraction of neutral atom and molecular beams by mesh supported gratings. Lithographic and etching procedures have been developed for fabricating free-standing gratings in thin silicon nitride (SiN_x) supported in a Si frame. Figure 27 shows a free-standing 100 nm-period grating in 100 nm-thick silicon nitride.

We have recently established a collaboration with the Max Planck Institute in Goettingen Germany, in which they will utilize our gratings of 200 and 100 nm period (see section 5.7) in diffraction and interferometer experiments using He atom beams. In addition, free-standing zone plates for use in atom focusing experiments will also be fabricated in SiN_x .

5.17 GaAs Epitaxy on Sawtooth-Patterned Silicon

Sponsor

Joint Services Electronics Program
Contract DAAL03-92-C-0001
Grant DAAH04-95-1-0038

Project Staff

Sean M. Donovan, Dr. Khalid Ismail,² Professor Leslie A. Kolodziejski, Professor Henry I. Smith, Professor Carl V. Thompson

The growth of GaAs on Si offers the possibility of combining high-speed and optoelectronic GaAs devices with Si integrated-circuit technology. Ordinarily, the 4.1 percent mismatch between the two materials leads to high dislocation densities. However, it has been shown here at MIT that when GaAs is grown on sawtooth-patterned Si substrates the dislocation density is less than $10^5/\text{cm}^2$, orders of magnitude lower than in GaAs films grown on planar Si substrates. We investigate this effect both for its potential of greatly improving the quality of GaAs on Si and as a model for understanding the mechanism of dislocation reduction. Oriented gratings of 200 nm period are fabricated in Si_3N_4 on (100) Si substrates using holographic lithography. Anisotropic etching in KOH is then used to produce sawtooth-profile gratings in the Si. Then these serve as substrates for GaAs growth by gas source MBE.

² Professor, Cairo University, Cairo, Egypt.

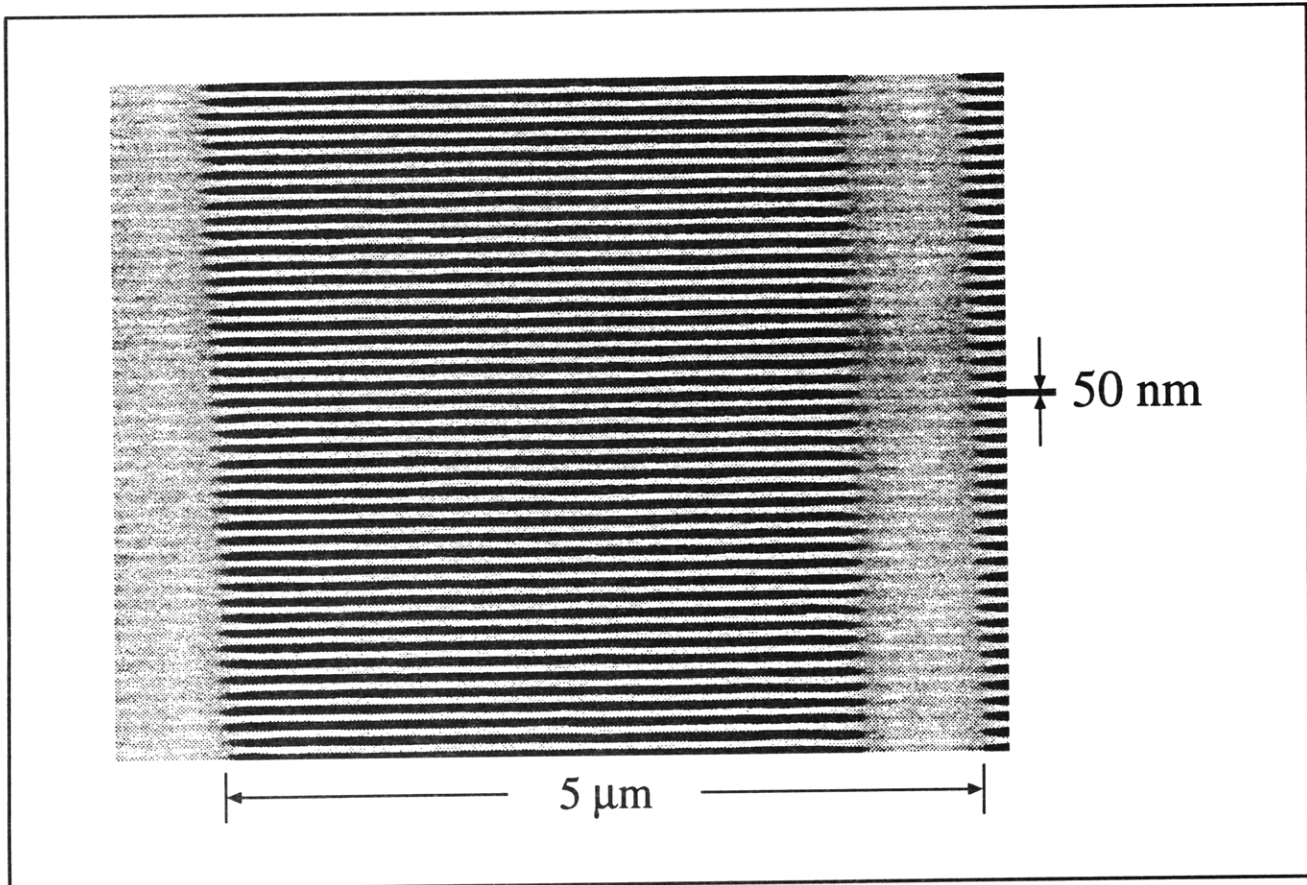


Figure 27. Scanning electron micrograph of a portion of a free-standing 100 nm-period grating in a silicon nitride membrane of area 200 μm by 5 mm.

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5.18.2 Conference Proceedings

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