

**Part I Solid State Physics, Electronics
and Optics**

Section 1 Materials and Fabrication

Section 2 Quantum-Effect Devices

Section 3 Optics and Devices

Section 4 Surfaces and Interfaces

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Section 1 Materials and Fabrication

Chapter 1 Compound Semiconductor Materials and Devices

Chapter 2 Physics of Heterostructure Field-Effect
Transistors

Chapter 3 Gas Source Molecular Beam Epitaxy of
Compound Semiconductors

Chapter 1. Compound Semiconductor Materials and Devices

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1.1 Epitaxy-on-Electronics Integration Technology

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Epitaxy-on-electronics (EoE) is a monolithic, heterojunction device, very-large-scale-integration (VLSI) technology. In the EoE technique, device heterostructures are grown by molecular beam epitaxy (MBE) in dielectric growth windows (DGWs)

on foundry-processed GaAs MESFET integrated circuit chips. Manufactured by Vitesse Semiconductor, these circuits are known to withstand extended temperature cycles of up to 470 degrees C without significant change in electronic performance. Using gas source molecular beam epitaxy (GSMBE), high-performance LED and laser diode material has been grown within the EoE time-temperature envelope. Using solid source MBE multiquantum well modulators and SEED structures, and resonant tunneling diodes have also been grown under these conditions. Through an interactive foundry service begun by our group known as the OPTOCHIP Project, eight university research teams now have the opportunity to design optoelectronic integrated circuits (OEICs) incorporating LEDs, photodetectors, and VLSI-density enhancement and depletion-mode GaAs MESFET logic gates. Because the OPTOCHIP Project requires a robust EoE process and well characterized optoelectronic devices, development of this technology has been our goal.

A major advance in EoE technology in the past year has been the development of an effective DGW preparation method. DGW formation is complicated by the need to etch through the thick (> 6 μm), highly nonuniform dielectric stack without

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damaging the underlying GaAs substrate. Prior attempts using reactive ion etching alone resulted in undesirable damage to the GaAs substrate, while wet etching frequently damaged nearby electronics. A new procedure utilizing directional dry etching to a metal etch-stop layer roughly $0.5 \mu\text{m}$ above the surface and a combination of wet and plasma etching to the substrate, is now used to obtain an undisturbed GaAs surface without affecting the electronic circuitry.

Another major advance was made in the area of in situ surface cleaning prior to epitaxy. In earlier work, we had used a hydrogen plasma to remove the oxides on the surface of GaAs wafers at temperatures as low as 350 degrees C (normal thermal oxide desorption is done at 600 degrees C). However, a hydrogen plasma source is expensive, and the energetic ions involved in the process may cause surface damage. Recently, we have shown that atomic hydrogen, obtained in situ using an economical, high-temperature cracker cell installed on Professor Kolodziej's GSMBE works equally well. A similar cell will soon be installed on the solid-source MBE.

Work in 1996 will focus on (1) gaining a better understanding of the consequences of doing epitaxy on the ion-implanted, semi-insulating substrates intrinsic to the EoE process, (2) quantifying and controlling the lateral infringement of defects from the DGW edges into the epitaxial regions, (3) obtaining statistical data on defects and yield, and (4) refining and improving the post-epitaxy processing sequences.

1.2 High Peak-to-Valley Ratio Resonant Tunneling Diodes on GaAs Substrates

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Resonant tunneling diodes have traditionally had relatively low peak-to-valley current ratios (PVCRs) when grown on GaAs. Resonant tunneling diodes relying on lattice-matched and/or pseudomorphic heterostructures on GaAs have achieved PVCRs as high as seven at room temperature, whereas pseudomorphic heterostructures on InP have achieved values as high as 50. Based on these observations, a number of research groups have grown high-indium-fraction heterostructures on GaAs in attempts to obtain some of the improve-

ments seen using InP substrates and have achieved a limited amount of success, achieving PVCRs as high as 9.3 at room temperature. Still, these recent results fall short of the PVCr of ten or more needed to make development of many RTD circuit applications attractive. We have taken an approach that can be viewed as combining features of several recent reports and have achieved PVCRs on GaAs as high as 13 at room temperature. The idea was to use (1) fully relaxed buffer layers and x-ray studies to confirm that the layers are indeed fully relaxed; (2) an increased In fraction, but not more indium than can be accommodated by the buffer layer composition steps; and (3) pseudomorphic AIAs barriers, rather than metamorphic layers.

Strain-relaxed $\text{In}_x\text{Ga}_{1-x}\text{As}$ step buffers were used in the present work. The structure was grown by solid-source molecular beam epitaxy (MBE) system using $\langle 100 \rangle$ GaAs n^+ substrates. Mesa diodes with areas ranging from $25 \mu\text{m}^2$ to $90 \mu\text{m}^2$ were processed using standard photolithography and wet etching techniques. The I-V characteristics of the devices were measured at room temperature and 77 K. The maximum peak current density was 22.8 kA/cm^2 . The maximum PVCr measured was 13:1 at room temperature and 27.5:1 at 77 K.

The good intrinsic performance of the devices indicates that resonant tunneling structures are robust and can withstand the presence of some dislocations within active layers, although care clearly must be taken to keep their density down. The devices were grown under conditions compatible with epitaxy on commercial GaAs VLSI. With reduction of their series resistance, they will be suitable, for example, for realizing high-density, low-power static random access memory arrays.

1.3 Monolithic Enhancement of MESFET Electronics with Resonant Tunneling Diodes

Sponsor

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Project Staff

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Using the epitaxy-on-electronics (EoE) integration technique, we have monolithically integrated relaxed-buffer InGaAs/AIAs resonant tunneling diodes (RTDs) with GaAs MESFET VLSI circuits to

build static random access memory (SRAM) cells. We have performed material characterization and electrical characterization of the integrated RTDs, and our results show that RTD heterostructure material grown on GaAs VLSI circuits is comparable in quality to that grown on epi-ready GaAs substrates. We also evaluated the critical RTD parameters for this application (i.e., the peak and valley voltages and current densities) over a 25 mm² integrated circuit to quantitatively establish circuit design rules. Finally, in the past year we have demonstrated the first RTD memory cells monolithically integrated on GaAs integrated circuits.

The lack of a compact, low-power memory cell has been an important limitation of GaAs MESFET integrated circuit (IC) technology. Because of large junction leakage currents, dynamic memory cells of the type widely used in silicon integrated circuits are not viable in GaAs ICs, and designers are forced to use static cells based on flip-flop circuits. These cells involve many transistors (a minimum of six, but more typically ten), consume a great deal of power, and occupy a lot of chip space. A compact, low-power static memory cell formed with two tunnel diodes and a single transistor has been proposed as an alternative by several groups. Other groups have proposed integrating tunnel diodes with resonant hot electron transistors (RHETs) and heterojunction bipolar transistors (HBTs) to produce low-power III-V logic circuits.

A major problem with these proposals is that they would require the development of an entire VLSI technology to be implemented. It is in this aspect of the problem that the EoE technology offers its solution. By building on the multimillion dollar, multithousand man-year investment in technology development made by such companies as Motorola and Vitesse Semiconductor in developing their commercial GaAs VLSI production facilities, the EoE process leap-frogs the basic issue of developing a VLSI technology and focuses on the issues involved in complimenting that technology with monolithic heterostructure devices, in the present case, with resonant tunneling diodes.

The uniformity of device performance across an integrated circuit chip of EoE RTDs and the similarity of that data to that of RTDs formed on bulk material, has important implications for optoelectronic device integration as well. Figure 1, for example, compares the forward characteristics of roughly 50 devices measured on an integrated circuit, and the same number on an epi-ready substrate. The spreads in peak and valley current and voltage levels in each case is comparable; this is very good. On the other hand, there is a difference in the current levels, which are consistently a factor

of two lower on the integrated circuit. A possible explanation is that defects originating from the ion implanted DGWs on the IC deplete portions of the RTD heterostructure, reducing the active area by two, but not otherwise affecting device performance.

The next issues to address in this program will be the minimum size of a growth well and the ultimate packing density of RTD memory cells. These issues are also being addressed with respect to optoelectronic integration.

1.4 Integrated InGaAsP/GaAs Light Emitting Diodes and Surface-Emitting Laser Diodes

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National Science Foundation
Graduate Fellowship

Project Staff

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The epitaxy-on-electronics (EoE) integration technique allows for the growth of optical devices in foundry-opened dielectric growth windows (DGWs) on fully processed GaAs MESFET integrated circuits. But to prevent the degradation of the electronic circuit performance, epitaxy must be done at temperatures below 470 degrees C. InGaAsP, which can be grown by gas-source molecular beam epitaxy (GSMBE) and solid-source molecular beam epitaxy (SSMBE) at these temperatures, is preferred over InGaAlAs for EoE emitter applications. We are actively researching the fabrication of light emitting diodes (LEDs) and surface emitting laser diodes (SELS) in this materials system.

LEDs utilizing InGaP/GaAs double heterostructures have been grown and characterized (electroluminescent efficiencies are typically 3 $\mu\text{W}/\text{mA}$), with recent efforts directed toward improving their electrical and optical performance. Various doping profiles have been implemented to reduce device bulk resistivity and to improve the current spreading in order to obtain more uniform optical emission. Incorporated into the LED design have been various etch-stop layers to permit selective etching of mesa type structures. A wet-etch process has been developed on campus using these etch stops,

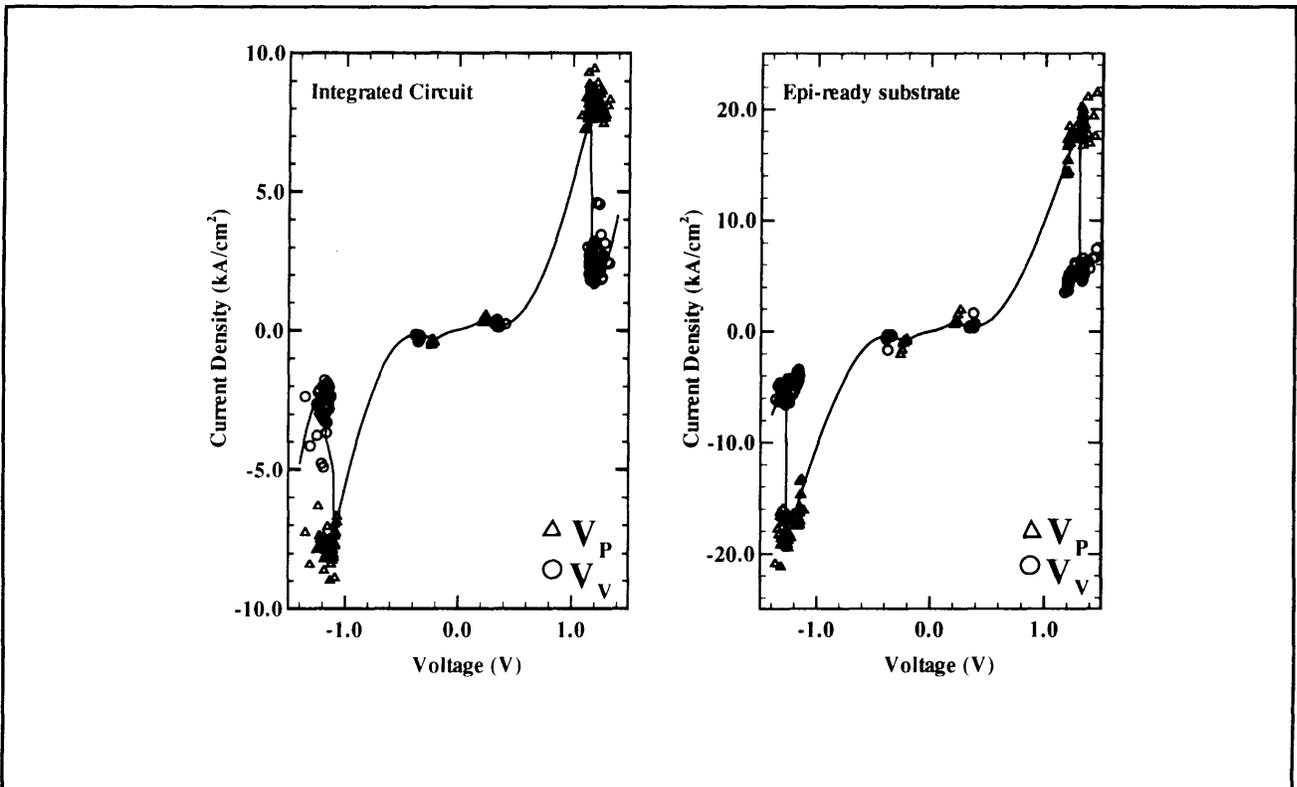


Figure 1. The variations in peak and valley current and voltage measured on fifty resonant tunneling diodes on an integrated circuit (left) and on an epi-ready GaAs substrate (right). Based on these results, we conclude that EoE integration yields devices with uniformity comparable to bulk growth. For proper operation, an integrated memory cell using the $n = 1$ resonance must accommodate up to a 9 percent variation in peak current, and one that uses the $n = 2$ resonance must accommodate a 15 percent variation.

and our collaborator, Dr. William Goodhue at MIT Lincoln Laboratory, has recently developed a dry-etch process for these materials using ion-beam assisted etching, and we will be applying this technique to mesa LEDs soon. A variety of top contacts have also been investigated, including indium tin oxide, transparent metals, and "finger" patterns.

Efforts have also been directed on several fronts at the development of SELs for integration. Broad-area, in-plane lasers grown at 470 degrees C show current thresholds of 200 A/cm², and our immediate goal is to use such material to fabricate in-plane surface-emitting lasers (IPSELs). To this end, we are collaborating with Dr. Goodhue and Professor Steve Forrest at Princeton University to adapt their respective IPSEL processes to this materials system.

Ultimately, we hope to develop a vertical-cavity, surface-emitting laser (VCSEL) integration technology. We are collaborating with Professor Dan Dapkus at the University of Southern California on oxidation of AlAs to form distributed Bragg reflec-

tors (DBRs). A 33-pair InGaP/AlAs DBR fabricated in our laboratory displayed a reflection coefficient spectrum that closely matched theoretical calculations, and oxidation of AlAs layers has been successfully accomplished, thereby enabling the fabrication of highly reflective DBRs with fewer reflector periods. Recognizing that the performance of future VCSELs depends strongly on the DBR quality and strict cavity length control, an in situ spectroscopic ellipsometer will be utilized during the fabrication of future DBR heterostructures.

1.5 Integrated Photodetector Standard Cells

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NTT Corporation

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In the epitaxy-on-electronics (EoE) optoelectronic integration process, it is desirable to use photodetectors fabricated utilizing the basic MESFET process, rather than epitaxially, so that the epitaxial heterostructures can be reserved and optimized exclusively for emitters. Consequently, we have begun to design, process through MOSIS, and characterize various photodetector structures. These studies involve individual photodetectors, as well as photodetectors with associated electronics (e.g., transimpedance amplifiers), which taken together can be viewed as optical bond pads for inputting signals optically to chips.

Three types of cells involving detectors fabricated during the standard MOSIS/Vitesse HGaAs₃ process have been investigated to date: (1) optically-sensitive field effect transistors (OPFETs), (2) OPFETs with depletion-mode field-effect transistor (DFET) loads, and (3) metal-semiconductor-metal (MSM) photo-detectors. The spectral response of these devices was measured and found to match closely the absorption spectrum of gallium arsenide. The measured output current of the MSM detectors is linear as a function of input light power, while the OPFETs show a logarithmic dependence of their voltage on the input current level, as predicted by the theory of a floating gate OPFET. The current response is 7.5 A/W at 880 nm and increases to over 400 A/W at wavelengths shorter than 800 nm. The MSM response is 0.1 A/W at these shorter wavelengths.

Measurements of the dynamic response of the detectors is still underway, and improvements need to be made in our system to permit measurements at higher frequencies. To date, the devices have been mounted in 40-pin integrated circuit packages along with chip preamplifiers to provide enough signal with a high speed light emitting diode as the input. The OPFETs are found to be relatively slow, with response times of several tens of microseconds. This is consistent with earlier work done on these devices by our collaborators at CalTech, and represents the gain-bandwidth trade-off inherent in these devices. The MSM devices, on the other hand, are much faster detectors; presently we are limited by our measurement system in characterizing MSMs to response times of 0.1 μ s.

Our immediate objective is to improve our measurement system to perform high-frequency characterization, evaluate the effects of backgating on OPFET and MSM response, and develop and eval-

uate high-performance transimpedance amplifiers for use with MSM detectors.

1.6 Microwave Characterization of Optoelectronic Devices

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Graduate Fellowship

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The investigation of the high-frequency and high-speed performance of optoelectronic devices and integrated circuits has been initiated. The optical and electrical components will be characterized separately, afterward the entire optoelectronic integrated circuit (OEIC) will be characterized. There are certain significant issues arising in optoelectronic integration that directly affect the high-frequency/high-speed performance of the OEICs. These issues are to be explored in the course of the investigation.

A scattering (S) parameter measurement facility has been designed and implemented for the high frequency characterization of the optical components of the OEIC. This facility permits the characterization of individual photonic devices and subsequently the characterization of the full OEIC.

The set-up consists of Hewlett-Packard 8510B automatic network analyzer equipped with an S-parameter test set, a modified Cascade Microtech on-wafer probe station, and a New Focus high speed photodetector. This is a broadband photodetector (400-1650 nm) operating from DC to 26 GHz, 17 ps rise time and 5 V/W. The responsivity of this photodetector is approximately 0.2 A/W over the entire wavelength. It is planned to make measurement of laser diodes and light emitting diodes over this frequency range. On wafer probing eliminates problems with packaging parasitics, and the Cascade microwave probe station has been modified so that it is suitable for the constant temperature probing of both edge and surface emitting devices. Future modifications for the probing of photodetecting devices such as photodiodes and MSM detectors are being designed.

Simultaneously, the issue of novel methods of instrument calibration is being addressed. Calibration techniques which take into account the optical components such as the fibers are under investigation for the optimization of accuracy. This calibration will be equivalent to the electrical open-short-line method used for electrical calibration.

This facility will permit the full characterization of optical and electrical devices as well as the circuits. Measurements will be performed for the extraction of model parameters and equivalent circuits to design optimized devices.

1.7 Growth of Distributed Bragg Reflector and Multiple Quantum Well Heterostructures at Reduced Temperature

Sponsors

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Technology
National Science Foundation
Graduate Fellowship

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Growth of optical devices on commercially available VLSI GaAs electronic circuits via the epitaxy-on-electronics (EoE) integration technique employing molecular beam epitaxy (MBE) requires growth temperatures below 470 degrees C to avoid deterioration of the underlying circuitry. Furthermore, a growth temperature even lower than 470 degrees C is required to growth thick, and therefore lengthy growth sequences of optical devices such as vertical cavity surface emitting lasers (VCSELs) and self electro-optic effect device (SEED) modulators.

An important issue to be addressed is whether the reduced-temperature MBE growth can produce high quality optical devices and how the optical quality at low-growth temperatures can be optimized. We are currently investigating lowered-temperature growth of distributed Bragg reflectors (DBRs) and multiple quantum wells (MQWs), which are constituent elements of VCSELs and SEEDs. We are also growing complete VCSELs and SEEDs. The growth temperature constraint does not allow fully optimized quantum well formation and ideal

interfacial quality in superlattices during conventional MBE. Therefore, we are exploiting alternative methods of low-temperature epitaxy, such as atomic layer epitaxy (ALE) via MBE, pulsed-arsenic MBE, and stoichiometric (unity group III to group V flux ratio) MBE. By reducing the arsenic overpressure while still staying above unity V/III flux ratio, we have demonstrated (Al, Ga)As DBRs with growth-temperature independent reflectivity down to a growth temperature as low as 400 C (see figure 2).

In addition to high optical quality mirrors, low modulation-voltage MQWs are also essential for integration with low-voltage digital circuits which typically have 0 V and -2.0 V rails. SEED devices grown at 500 degrees C have been fabricated and function well with an 8 V voltage swing. Asymmetric integrated with enhancement- and depletion-mode MESFET VLSI circuits, which were designed as a part of the EoE multiproject chip, to produce dual-rail digital optical logic circuits which will effectively compete with depletion-mode only MESFET-SEED technology.

1.8 Monolithic Integration of Self-Electrooptic-Effect Devices on Very Large Scale Integrated GaAs Electronics

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Technology
National Science Foundation

Project Staff

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Benefiting from the novel epitaxy-on-electronics (EoE) optoelectronic integration technique, the pursuit of integrating self-electrooptic-effect devices (SEEDs) with both enhancement- and depletion-mode MESFET VLSI circuits has become feasible.

Dedicated SEED MESFET VLSI circuits have been designed and fabricated as part of the MIT EoE multiproject chips, which includes optical logic gates such as a SEED receiver, NOR gate, transmitter, and more complicated logic combinations. In addi-

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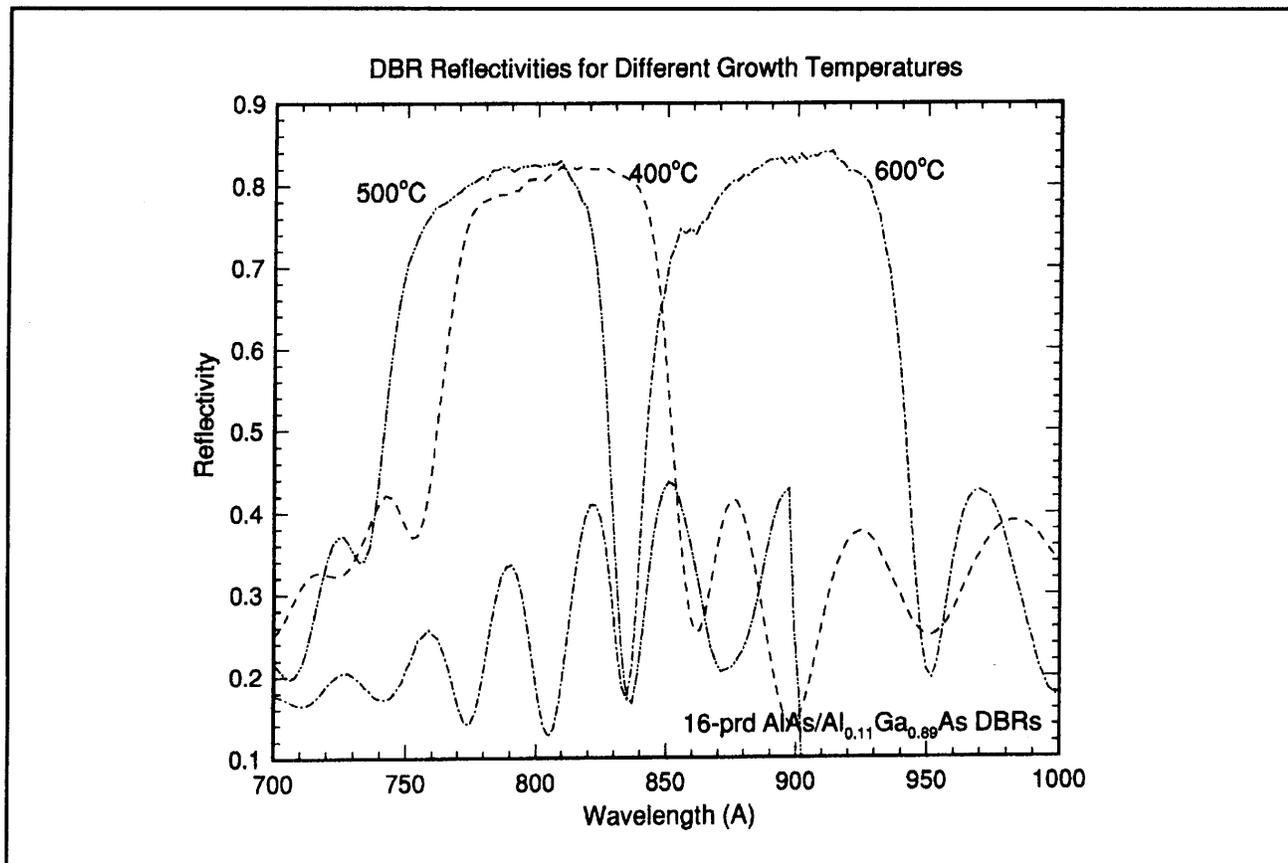


Figure 2. Reflectivities of 16 periods' AlAs/Al_{0.11}Ga_{0.89}As DBRs grown at temperatures ranging from 600 degrees C down to 400 degrees C. The shift in wavelength of the pass band is due to a calibration error and is not related to the growth temperature differences.

tion, a 10 x 10 SEED optical bump circuit array has been designed by our collaborators at Caltech. After several SEED growth/fabrication efforts, the first working low-temperature integrated SEED has been demonstrated on a chip. A useful contrast ratio of 2.2:1 was obtained for a monolithically integrated device while even a better contrast ratio of 3.27:1 was obtained for the bulk monitor at 10V bias (see figure 3). Further improvements of regrowth crystal quality are currently under investigation.

One very important issue addressed in our research is how to achieve low-temperature substrate cleaning prior to molecular-beam epitaxy growth. The EoE integration technique demands that we not expose the VLSI chip to a temperature higher than 470 degrees C to avoid degradation of the underlying circuitry. However, conventional MBE growth involves thermal oxide removal at 580 degrees C prior to epitaxy, which poses serious problems for the survival of the electronics. Our current research is exploiting alternative methods of low-temperature oxide removal, such as in situ chemical etching of GaAs substrates by gaseous

HCl, or GaAs substrate cleaning using atomic hydrogen. With these efforts, fully functioning high density optoelectronic SEED circuitry will soon be achieved with performance superior to current depletion-mode-only FET-SEED technology.

1.9 Compact Integrated Optics Structures for Monolithic Integration

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Recently, due to the fiberoptic telecommunications boom, much work has been done on integrating semiconductor optical devices, such as modulators, detectors, and lasers, with driving electronics made up of MESFETs, MODFETs, or HBTs. However,

the necessity to optimize both the optical and electronic devices simultaneously makes the progress slow. Our project is to integrate mature GaAs electronic ICs with integrated optics components by selectively growing (MBE) our optical devices on open areas of commercial GaAs IC chips. This epitaxy-on-electronics (EoE) technique has already been successfully achieved for integrating LED arrays with driver circuits. Our goal is to demonstrate a working integrated optics circuit fabricated on and integrated with a GaAs IC chip. The basic optical components of this system are passive waveguides, phase modulators, and detectors. The electronics will consist of driving and amplifying circuit for the modulators, and detectors, as well as signal processing and control digital circuits. Since the area of the GaAs VLSI chip is expensive, the conventional gradual bends, necessary to change the propagation direction of guided light will be replaced by abrupt 90 degree bends with deep etched total internal reflection (TIR) mirrors (see figure 4).

In our first attempts at EoE integrated optics, we have used lowered temperature AlGaAs/GaAs heterostructures, grown at 500 degrees C, so that drastic deterioration of the IC performance is not

caused. However, the material quality of AlGaAs is poor: we have measured waveguide losses greater than 20 dB/cm. Therefore, lattice matched InGaP/GaAs heterostructures will be used since InGaP grown at 470 degrees C is higher quality. Currently, etching techniques for InGaP material are being investigated. In particular, dry etching methods for creating deep openings with smooth vertical walls in InGaP/GaAs heterostructures are being developed. Such smooth vertical walls are necessary for the low loss TIR mirror waveguide bends.

In addition to optical device design, circuit design is also being carried out. Several versions of modulator driver circuits have been designed, fabricated at the Vitesse MOSIS foundry, and tested. These circuits are able to drive the modulators with a 10 V swing output with DCFL inputs of 0-0.6 V, and speeds of up to 5 MHz driving external circuit board lines. Since the HSPICE simulation suggests 200 MHz performance, we expect a drastic improvement in performance for these circuits driving on chip interconnections. (The simulations were done using Vitesse HSPICE device parameters.) Complementing the modulator driver design, such fundamental issues for high voltage MESFET

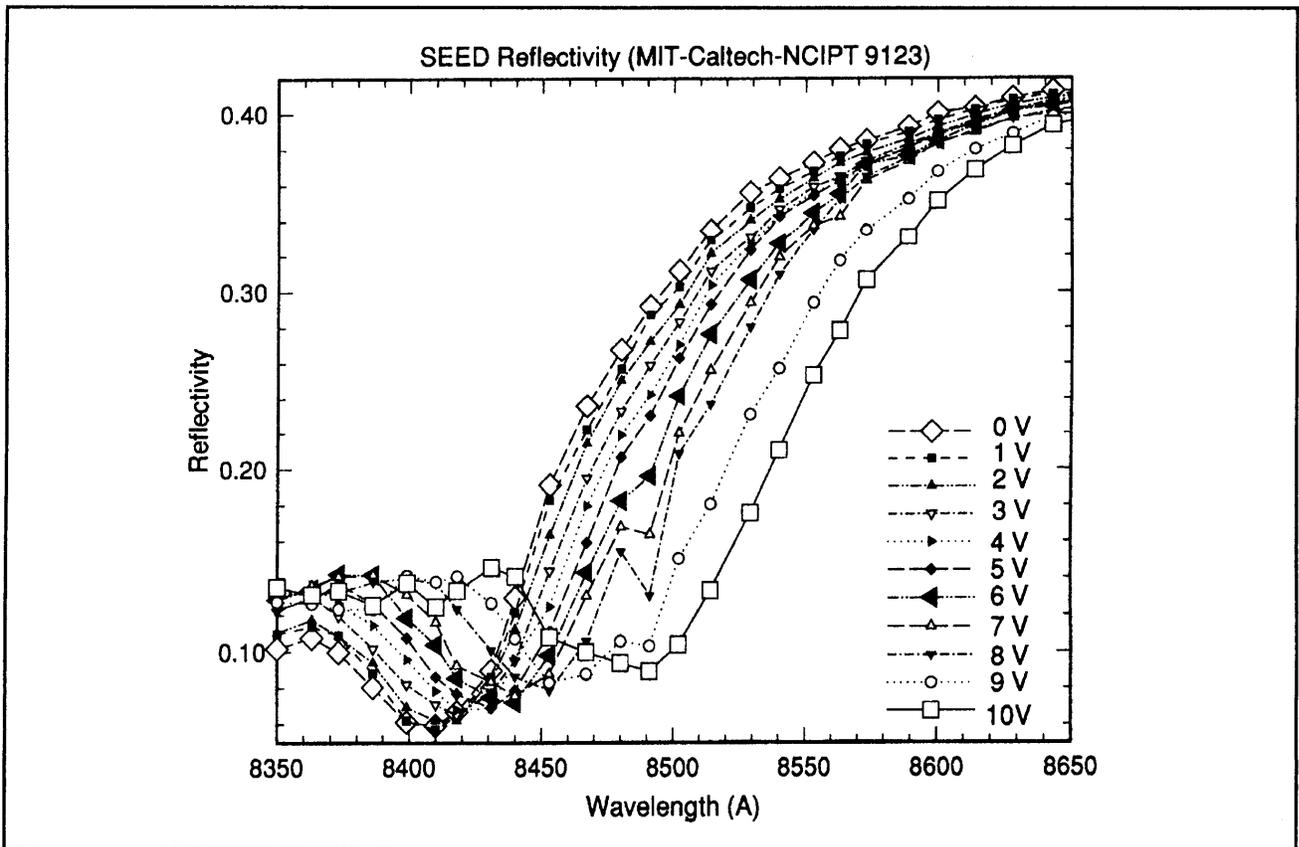


Figure 3. The measured reflectivity spectrum between 835 and 865 nm of a SEED modulator at selected voltages between 0 and 10 volts.

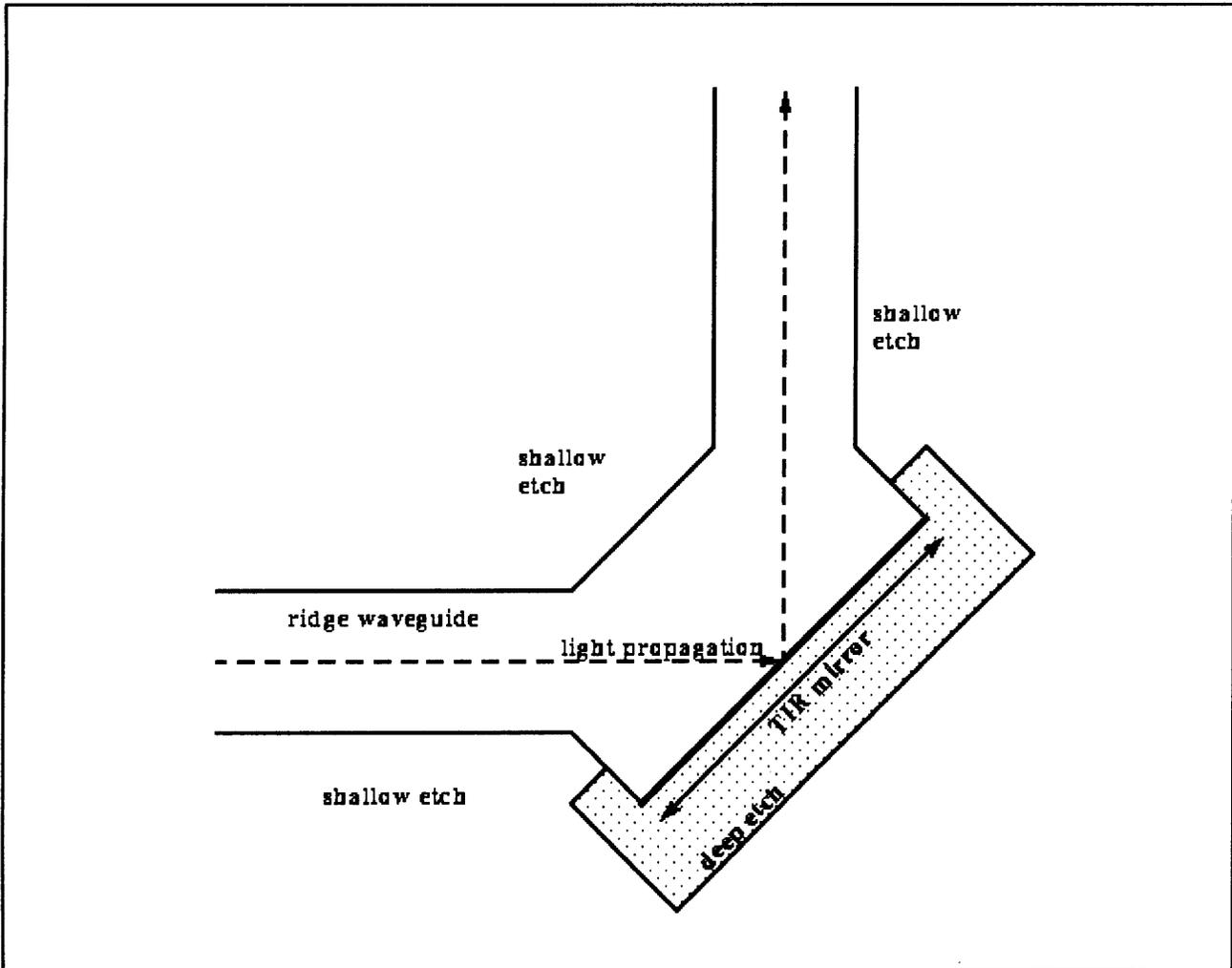


Figure 4. Waveguide bend with total internal reflection (TIR) mirror.

circuit design such as backgating and gate breakdown are being investigated. Structures with depleted isolation barriers have been shown to eliminate backgating. Finally, a library of digital circuit cells is being compiled for the control logic needed in the demonstration project.

1.10 The OPTOCHIP Project and other Multigroup OEIC Chips

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The OEIC Platforms Project is a directed technology project within NCIPT focused on developing an optoelectronic integration technology based on commercially available gallium arsenide integrated circuits. This technology, named epitaxy-on-electronics (EoE), involves the epitaxial growth of optoelectronic device heterostructures on fully metallized GaAs MESFET VLSI electronics. In addition to developing this OEIC technology, the project has the goal of making this technology available to the broad academic and research communities.

Progress has continued in all major areas of the OEIC Directed Project: (1) continued work on reduced-temperature epitaxy (RTE) of low-threshold InGaAsP laser diodes (GS-MBE growth), (2) use of atomic hydrogen to prepare surfaces for epitaxy at 350 C, (3) demonstration of the first monolithically

integrated SEED and other window modulator structures, (4) initiation of integrated optics (fiber-coupled geometry) projects, (5) realization of the second multiproject OEIC chip, and (6) inauguration of the OPTOCHIP project.

The NCIPT multiproject OEIC chips are our vehicle for involving many NCIPT groups and members of the outside community epitaxy-on-electronics OEIC chips. These chips, of which there are now two generations, involve OEIC and test cell designs (over 50 in total) from five universities. Included are cell designs for both smart pixel (i.e., surface-normal configuration) OEICs and integrated optics (i.e., in plane, fiber-coupled configuration) OEICs. The chips are being used as the foundation for epitaxial growth and device processing for a variety of device types and structures and for realization of a wide variety of OEICs.

The OPTOCHIP Project was launched in Fall 1995 to involve the smart pixel community in an epi-on-electronics multiproject OEIC chip through a foundry-like mechanism. A total of eight diverse groups have been selected to participate from over twice that number of applicants. The offering will involve LEDs, detectors, and MESFETs. Chips designs will be completed in May 1996, and chips will be returned to participants in October 1996.

1.11 Normal Incidence Single- and Dual-Band Quantum-Well Intersubband Photodetectors

Sponsors

National Science Foundation
U.S. Navy - Office of Naval Research

Project Staff

Paul S. Martin, Janet L. Pan, Professor Clifton G. Fonstad, Jr., and P. Kannam

Quantum-well intersubband photodetectors (QWIPs) are attractive devices to compete with HgCdTe for use in focal plane arrays. QWIPs can take advantage of the established technology for growing and processing GaAs optical devices to improve device uniformity and array yield.

We have demonstrated the first TE-active normal incidence QWIPs based on InGaAs/AlGaAs quantum wells grown pseudomorphically strained on GaAs. Our best devices consist of five 45 Å quantum wells of In_{0.13}GaAs doped n-type at $5 \times 10^{17} \text{ cm}^{-3}$ and separated by 510 Å of unintentionally doped Al_{0.30}GaAs. The measured responsivity is shown in figure 5. The peak signal to noise ratio of

680 occurred for a bias of 3.2 V giving a peak wavelength of 6.4 μm, a peak responsivity of 200,000 V/W (25 mA/W) and a D_λ of $6 \times 10^9 \text{ cm}^{-1} \text{ Hz}^{1/2} \text{ W}$ for a 100 μm square mesa device measured at 77 K. The FWHM of the response is 1.0 μm typical of bound to quasi-bound intersubband signals and very attractive for potential multi-band QWIP applications. The D_λ of $6 \times 10^9 \text{ cm}^{-1} \text{ Hz}^{1/2} \text{ W}$ for this unoptimized device is within a factor of two of the value at which uniformity of the QWIP array and not D^* becomes the limiting factor in performance as measured by NEDT. This highlights our emphasis on TE active devices which eliminate the need for additional processing to implement gratings for other TM coupling mechanisms and removes the additional processing nonuniformity these TM couplers cause.

We are currently working to improve the responsivity of our detectors and to integrate a second detector on top of another vertically. Because no gratings are needed to couple the normally incident light into the active detectors, these dual band detectors are relatively simple to design and emphasize the advantages of the simple TE mode device design.

1.12 Integrated Quantum-Well Intersubband Photodetector Focal Plane Arrays

Sponsor

U.S. Navy - Office of Naval Research

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The monolithic integration on GaAs circuits of normal-incidence-active (TE-mode) quantum well infrared photodetector (QWIP) focal plane arrays (FPAs) is expected to increase the yield and processing simplicity of infrared photodetector FPAs. This is very important because QWIP and other infrared photodetector FPAs are currently limited by the uniformity of the performance over an entire FPA and not by detectivity of each pixel in the array.

Monolithic integration means that there is no thermal mismatch between different substrate materials, as there is in a hybridized technology of GaAs QWIPs bump bonded to Si circuits. Processing is also simplified because intricate and expensive In bump bonding is not needed. Normal incidence active QWIPs do not require gratings to be coupled to the normally incident radiation. The use of GaAs

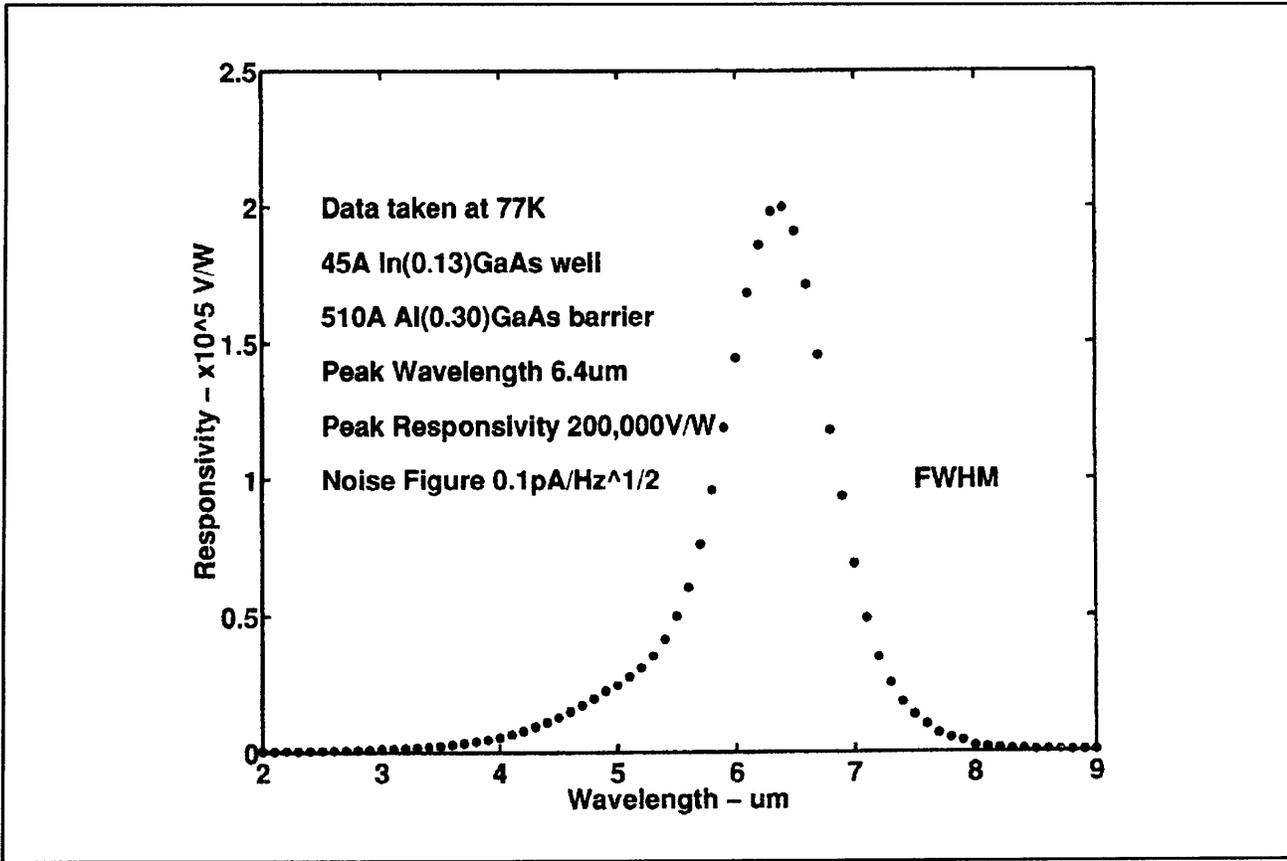


Figure 5. The normal incidence responsivity measured at 77K for a pseudomorphic InGaAs QWIP consisting of five periods of 4.5 nm of $\text{In}_{0.13}\text{Ga}_{0.87}\text{As}$ and 51 nm of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$.

as the substrate material offers advantages of: (1) a mature processing technology; (2) the existence of large, low cost, highly uniform and reliable substrates, as compared with mercury cadmium telluride detectors; and (3) the intrinsic radiation hardness of GaAs, as compared with Si. The elimination of In bump bonding and grating fabrication, as well as the use of a GaAs substrate, allows for high yield and low cost QWIP FPAs.

In addition to the simplified processing steps discussed above, the cost of using QWIP FPAs can be lowered by increasing the QWIP operating temperature. We are investigating two possible approaches to doing this. First, band gap engineering will be used to design QWIPs whose upper state lifetimes are greatly increased. This would increase the detectivity, and thus the temperature of the background limited performance, of each QWIP. Second, microlenses will be used to increase the ratio of the photocurrent to the dark current at a given QWIP size by concentrating more of the incident photon flux onto each QWIP pixel. Microlenses increase the detectivity at a given QWIP

size, as well as allowing more of the space between QWIP pixels to be used for circuits.

1.13 Intersubband Transitions in Narrow Quantum Wells

Sponsors

National Science Foundation
Toshiba Corporation

Project Staff

Norio Iisuka, Professor Clifton G. Fonstad, Jr.

Intersubband transitions are very attractive phenomena because they are applicable to lasers, photodetectors, optical modulators and other novel photonic devices. In this project, we focus our effort on research on quantum wells in which the intersubband wavelength is $1.55 \mu\text{m}$ shorter, which is optimal for optical communication. To achieve such intersubband transitions, we are growing $\text{In}(\text{Ga})\text{As}/\text{AlAs}$ quantum well structures where on InP or GaAs substrates the well width is as narrow as a few monolayers.

The well width in these structures is so narrow that the quality of interface between the barrier and the well is critical. Interface roughness will cause the transition energy to shift. To achieve good quality of interface, we are trying to adapt migration enhanced epitaxy (MEE) to this problem. Another material problem is that the critical thickness of a barrier layer or a well layer is very small because of the large difference in the lattice constants of the barrier and the well materials. Consequently, it is difficult to grow multiple-quantum-well structures which give the light and quantum wells more time to interact than a single quantum well structure does. To overcome this difficulty, the strain compensated structure, which consists of InAs and AlAs on InP substrate, will be tested.

In actual materials, absorption due to undesirable energy levels such as a surface level are sometimes confused with absorption due to intersubband transitions. We have found that there is the specific region of cap layer thickness in which the effect of surface states can be eliminated in absorption measurements made on the waveguide configuration. With this thickness of the cap layer, very little of the incident light exists in the cap layer, which is confirmed by calculating the distribution of the light intensity. A self-consistent electronic state calculation program is also being developed. The calculation will give us information about what the quantum well structure is like, what the subband levels are, and how many electrons populate the well region. Accordingly, it will become a useful tool for the design of novel devices using intersubband transitions.

1.14 Kinetic Beam Etching of Semiconductor Nanostructures

Sponsors

Defense Advanced Research Projects Agency/
National Center for Integrated Photonics
Technology
AT&T Bell Laboratories
Graduate Fellowship

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Since it became necessary to grow compound semiconductor epitaxial layers upon an already existing integrated circuit, it became crucial to minimize or eliminate surface damages caused by conventional etching techniques using plasma sources. To find a solution to the problem of process-induced damage, we have begun a project investigating the use of molecular-beam (hot neutral

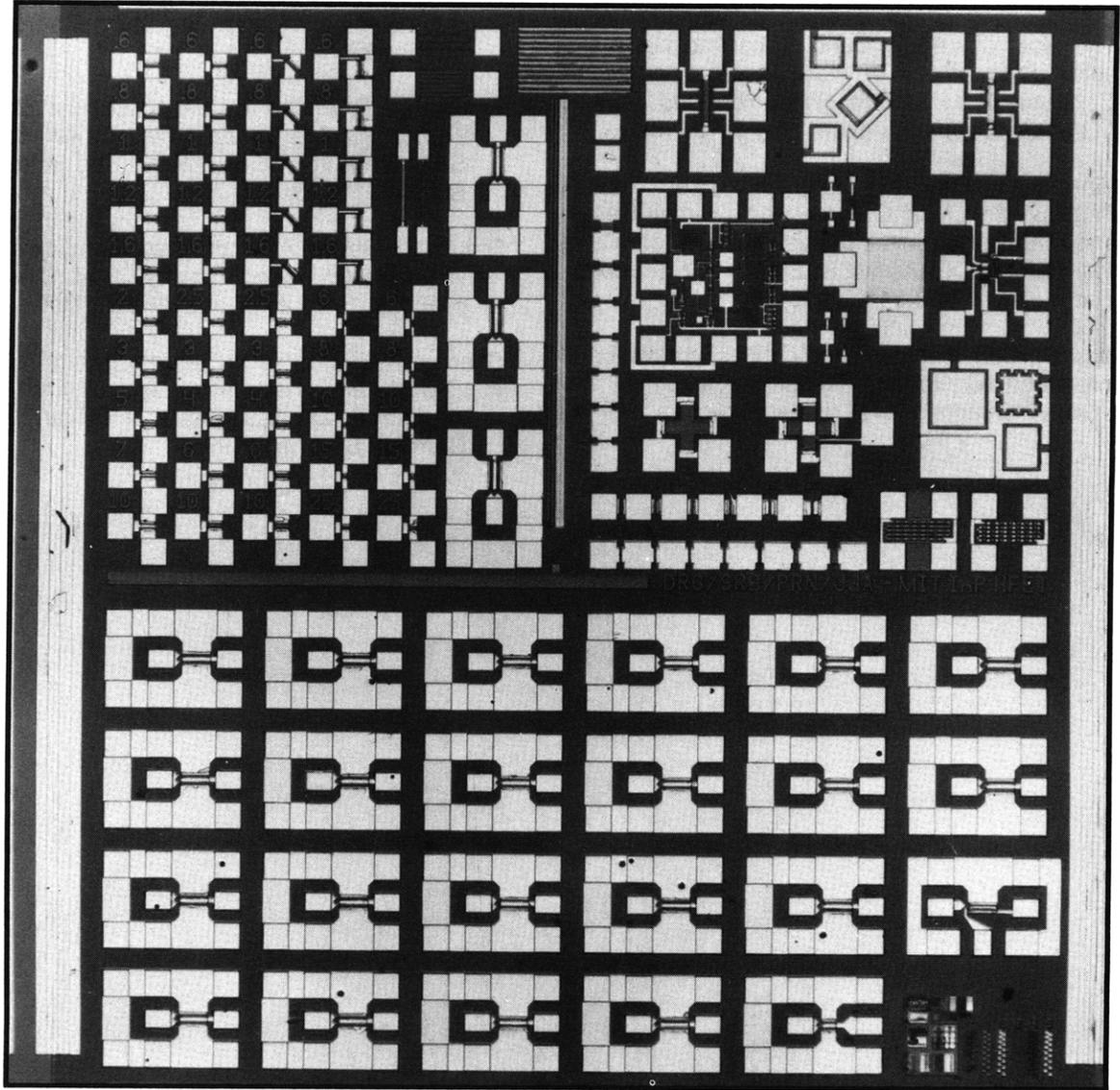
beam, also known as kinetic beam) techniques to etch and clean III-V substrates and heterostructures with a minimum of surface damage and allowing maximum flexibility in attaining various etch profiles. Depending on the gas combination, it is anticipated that low energy (0.1 to 10 eV) kinetic beams can be used to (1) both directionally and isotropically etch-pattern III-V heterostructure wafers with no damage; (2) clean surfaces allowing epitaxial growth on wafers that have been removed from the UHV environment for external processing; and (3) selectively remove masking materials and clean surfaces suitable for subsequent overgrowth.

A differentially pumped UHV kinetic beam etch (KBE) system design to use a methane-hydrogen gas mixture using a supersonic beam has been designed and constructed. The initial function tests of the KBE system are currently underway. Subsequently, a full-scale characterization of the ability of the KBE system will be performed, mainly concentrating on etch rate, etch profile, and surface damage assessment. The extent of surface damage, if any, will be determined through electrical and optical characterizations of heterostructure devices grown by solid-source MBE. Once the KBE system is fully characterized, it will be connected to the existing MBE system through a UHV transfer tube.

1.15 Publications

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- Braun, E. *Elevated Temperature Stability of Gallium Arsenide Integrated Circuits*. S.M. thesis. Dept. of Electr. Eng. and Comput. Sci., MIT, 1995.
- Shenoy, K.V. *Monolithic Optoelectronic VLSI Circuit Design and Fabrication for Optical Interconnects*. Ph.D. diss. Dept. of Electr. Eng. and Comput. Sci., MIT, 1995.



Photomicrograph of InAlAs/InGaAs High-Electron Mobility Transistor test chip fabricated at MIT.