Part I Solid State Physics, Electronics, and Optics

Section 1 Materials and Fabrication

Chapter 1. Compound Semiconductor Materials and Devices

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1.1 Introduction

Heterostructure devices, such as laser diodes and high electron mobility transistors, play an increasingly important role in our lives. These devices are the key, enabling the develoments of the components of as compact disk players, cellular telephones, fiber communication links, and direct broadcast television receivers. The impact of heterostructure devices would be even greater, however, their use was not limited to applications involving single devices or combinations of a few devices because of the enormous cost of developing an integrated circuit technology comparable to what now exists for silicon. Addressing this bottleneck, researchers in Professor Clifton Fonstad's research group in the RLE have recently made major advances in integrating complex compound semiconductor heterostructures with commercial VLSI (very-large-scale integration) electronic circuits. The epitaxy-on-electronics (EoE) technology they have developed in collaboration with Professor Leslie A. Kolodziejski, promises to make practical the fabrication of complex integrated heterostructure systems such as image recognition sensors, massively parallel neural computers, and handheld retinal scanners. These and similar items are now more commonly associated with science fiction than reality.

The following sections describe Professor Fonstad's research program and key results obtained during the past year; highlights include successful completion of the OPTOCHIP project making EoE optoelectronic integrated circuits (OEICs) available to the user community through a research foundry offering, and new results on surface-emitting laser diodes, 1550 nm photodetectors on GaAs, and quantum-well intersubband photodetectors. Work is also reported on ion beam assisted dry etching of aluminum-free laser diode structures, on hyperthermal molecular beam etching of GaAs and InP, and on microwave device characterization.

1.2 Epitaxy-on-Electronics Integration Technology

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The development of optical interconnects has been hampered by the lack of a viable source of complex optoelectronic integrated circuits (OIECs), circuits which will ultimately need to contain thousands of optoelectronic devices tightly integrated with VLSI-complexity electronics. Hybriding, wafer-bonding, and epitaxial lift-off have made progress in addressing this need; however, issues of density performance, reliability, and yield suggest that monolithic integration is the best answer, as it has been in conventional microelectronics manufacturing. To answer this need, we have developed epitaxy-on-electronics (EoE), a process for monolithically integrating optoelectronic devices on commercially pro-cessed gallium arsenide ICs.

The EoE process begins with custom-designed GaAs VLSI circuits. The electronics technology (the Vitesse Semiconductor $HGaAs_3$ process) provides enhancement- and depletion-mode MESFETs and four layers of aluminum-based electrical interconnect, as well as optical field-effect transistor (OPFET) and metal-semiconductor-metal (m-s-m) photodetectors. Molecular-beam epitaxy (MBE) is used to grow device heterostructures on regions of the GaAs substrate which are exposed by cutting through the interconnect dielectric stack. Established fabrication techniques complete the integration procedure. The unrestricted placement of the optoelectronic devices occurs as part of the routine layout of the integrated circuit; the interconnect dielectric stack in the regions designated for these devices is partially etched at the GaAs foundry forming dielectric growth windows (DGWs). The etch is completed, exposing the underlying GaAs substrate, upon receipt of the ICs from the manufacturer; the design of the DGW structure and of the technique for producing a damage-free GaAs starting surface are among the latest innovations in the EoE process. The source/drain implant is used as the bottom n-contact of the optoelectronic device. Epitaxial material is then grown in the DGWs, while polycrystalline material is deposited on the overglass. Standard processing techniques are then used to remove the polycrystalline material, to fabricate the optoelectronic devices, and to interconnect the top-side electrical contacts of the devices to the electronics.

As in standard silicon technologies, the gallium arsenide VLSI process uses aluminum-based electrical interconnects. We have shown that these interconnects degrade when exposed to temperatures in excess of 475°C. Conventional MBE practice uses a 580°C temperature excursion to desorb the native oxide on the GaAs surface prior to growth, and even this brief high temperature exposure (which was used in previous EoE work) results in appreciable damage to the interconnect lines. Interconnect degradation is now effectively eliminated by using cracked hydrogen to remove the native oxide at as low as 350°C.

Also owing to the electrical interconnect thermal instability, the epitaxy must be carried out below 475°C. This restriction is not compatible with the growth of high quality AlGaAs suitable for emitters (although it can be used in passive applications) due to aluminum's high affinity for oxygen. The performance of previous monolithic EoE light emitting diodes involving AlGaAs heterostructures was thus compromised. To circumvent this difficulty, current EoE efforts use the aluminum-free InGaAsP materials system, which is routinely grown a reduced temperatures.

Process innovations in the areas of DGW preparation, low temperature GaAs native oxide removal, and gas-source MBE growth of EoE compatible optoelectronic devices have removed limitations present in previous EoE demonstrations. Ring oscillator measurements made before and after EoE processing have verified stable sub-100 picosecond gate delays, consistent with subnanosecond, multigigahertz electronics operation. Present EoE technology is being applied to a presently, variety of applications benefiting from the integration of high-performance heterostructure devices with VLSI-complexity electronics.

4 Vitesse Semiconductor Corporation, Colorado Springs, Colorado.

5 MIT Lincoln Laboratory, Lexington, Massachusetts.

1.3 InGaAsP/GaAs Light Emitting Diodes Monolithically Integrated on GaAs VLSI Electronics

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While surface-emitting lasers are ultimately desired in optical interconnect applications because of their large bandwidth, efficiency, and directionality, recent EoE work has been restricted to the integration of LEDs, with comparatively relaxed growth and fabrication demands, in order to focus attention on the EoE-specific process development. Mesa-confined GaAs/InGaP double-heterostructure LEDs are used in this demonstration of monolithic, emitter-based OEICs.

LEDs are fabricated following epitaxy and removal of the polycrystalline deposits. The fabrication process is nearly identical to that of similar devices on bulk wafers. The primary difference is in the use of thick photoresists (3 to 4 μm) which are needed in order to assure step-coverage over chip-surface non-planarities. Contact lithography is readily used to pattern 2 to 3 μm minimum feature sizes. Step coverage also requires the use of aluminum interconnect metalization. To avoid the undesirable reaction of aluminum with a gold-based ohmic contact, Ti/Pt ohmic contacts are used.

An aluminum interconnect line links the Ti/Au/Ni p-contact to nearby electronics. An optical shield around the DGW perimeter is formed by stacking interconnect metals up to Metal-3. The purpose of this shield is to prevent coupling of LED emission to nearby electronics. Two shield designs (referred to as #1 and #2) differing in the sizing and placement of metal and via patterns, and consequently differing in surface non-planarity above the shield, were implemented around 50 mm DGWs. Unshielded 85 mm DGWs were also used.

The nominal LED emission wavelength is 873 nm, corresponding to the bandgap of the GaAs core. The angular distribution of the output light is Lambertian, i.e., intensity proportional to the cosine of the normal angle.

Operation of the LED-based OEICs can be illustrated through the example of a simple "optical inverter" on the chip. The input element is an OPFET. With no applied light, the OPFET is in its off state and pulls the output of an inverter loading it to the DCFL high level of 0.6 V. Following three inversions, the signal arrives at the gate of a pull-down EFET as a low. The drain of this off-state EFET rises to 3 V, and 2 V remains across the LED. There is no significant LED current and the optical output is off. When the incident power reaches just above 0.1 μW, the OPFET switches on. The inverter output is now pulled to a DCFL low level of 0.1 V. This signal cascades through the three inverter stages and turns on the pull-down EFET. The drain of this EFET now drops to 0.8 V. With 4.2 V across the LED, the EFET sinks 4.6 mA of current corresponding to an optical output power of 2 μW. This power level is 13 dB above the 0.1 μW optical input threshold. This level of optical gain allows EoE-integrated LED-based OEIC to meet the realistic system requirements of many optical interconnect architectures. In fact, this 13 dB figure represents a lower bound on the optical gain achievable with these OEICs. Using an 85 mm DGW LED would increase this optical gain to roughly 20 dB.

1.4 The OPTOCHIP Project

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6 Vitesse Semiconductor Corporation, Colorado Springs, Colorado.

The OPTOCHIP project is a research foundry offering intended to provide prototype OEICs to selected university groups doing research on optical interconnect systems. The first generation OPTOCHIPs use In GaPGaAs light emitting diodes (LEDs) monolithically integrated using the epitaxy-on-electronics (EoE) technology on commercially fabricated GaAs integrated circuit chips containing optical field effect transistor (OPFET) and metal-semiconductor-metal (m-s-m) photodetectors, and enhancement- and depletion-mode metal-semiconductor field effect transistors (MESFETs). A solicitation for participation was made in late 1995 and in early 1996 nine groups from eight universities were selected to participate; the universities represented are California Institute of Technology, Colorado State University, George Mason University, McGill University, Texas Christian University, University of Southern California, and University of Washington. These groups began work in February 1996 on the designs for 2 mm x 2 mm OEIC chips which were combined into a larger die and submitted to the MOSIS service in May 1996. The chips were fabricated by Vitesse Semiconductor Corporation, Camarillo, California, in Summer and Fall 1996, and the EoE integration process was initiated early in 1997. Fabrication of the integrated LEDs was completed in May 1997; and the completed OPTOCHIP die were sawn into individual 2 mm chips and returned to the designers for deployment in their optical interconnect architectures.

Electrical tests on the completed OPTOCHIP die show that there was no degradation in the electrical performance of the circuitry due to the EoE process. The performance and yield of the LEDs were poorer than had been achieved on previous test runs due to problems in the growth system, but several functional die were provided to each participating group. The amount of work done with the completed chips varies between the various groups, but several groups have performed extensive testing of their OEIC chips and have successfully employed them in systems-level situations. In one case, communication between a pair of OPTOCHIPs has been demonstrated. Work is continuing on the testing of the chips, and our group at MIT is working to be able to supply the participants with another set of die processed using the new GaP phosphorous source recently installed on our MBE.

The completed, overall 7 mm x 7 mm-square OPTOCHIP die each contain over 200 LEDs integrated with numerous different circuits and subsystems containing thousands of transistors. As such they represent some of the most complex LED-based monolithic OEICs ever fabricated. The OPTOCHIP project was also unique in (1) the OPTOCHIP die incorporate designs from a diverse selection of groups, and (2) minimal constraints were placed on the circuit designs.

We intend to offer OPTOCHIPs in the future. The processing of subsequent OPTOCHIPs will be done on a semi-professional basis using the facilities of the Technology Research Laboratory (TRL) of the Microsystems Technology Laboratory (MTL) at MIT. We are eager to make surface-emitting lasers (SELs) available to OPTOCHIP users in the near future; self-electro-optic effect devices (SEEDs) are another option, but our primary focus is on emitter-based OEICs containing LEDs or SELs.

1.5 Low-Temperature Growth of Aluminum-Free InGaP/GaAs/InGaAs LED and Laser Diode Heterostructures by Solid Source MBE using a GaP Cell

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MIT Lincoln Laboratory

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Dr. P. Aitor Postigo, Professor Clifton G. Fonstad, Jr., in collaboration with Dr. David Braddock[7]

The use of InGaP instead of AlGaAs for the fabrication of light emitting heterostructures as light emitting diodes (LEDs) and laser diodes (LDs) presents important advantages, such as the reduction of deep donor levels and lower InGaP/GaAs interface recombination velocity. In addition, InGaP is more suitable for the reduced-temperature molecular beam epitaxy (MBE) required for the epitaxy-on-electronics integration technology (475°C), since it is aluminum-free.

The use of phosphorous in MBE has traditionally been done through the introduction of phosphine (PH_3) as a gaseous source. However, the use of a solid source is also very attractive since it is easier to implement and to maintain in the MBE system, but it

7 EScience, Inc., Hudson, Wisconsin.

must be a solid source which gives a very high ratio of dimers to tetramers, i.e., P_2 to P_4. The dimers have a higher sticking coefficient and are much better for MBE growth. Two methods have been used to produce P_2 from solid sources. One is based in a two-zone-cracker cell where the P_4 is cracked in P_2 by a very high temperature section (>1000°C) and where the source is solid red-phosphorous. The other method is based on the sublimation of phosphorous from phosphides as GaP, which produces the best P_2 to P_4 rate (around 170 compared to the 3.5 to 6 of the thermal cracker). The GaP decomposition cell has the same design as a common group-III effusion cell that operates at high temperatures (the typical temperature used for phosphide growth is around 1000°C), and it can be operated as a regular group-III cell. However, this type of cell can produce some residual amount of Ga, that can be reduced through an special design. This design implements a dome-shaped and disk-shaped pyrolytic boron nitride (PBN) cap on top of the normal crucible, that acts as a trap for the Ga atoms. In collaboration with Dr. David Braddock, from EScience Inc., we have successfully demonstrated a high-capacity (100 gr) GaP decomposition source that has produced high quality epitaxial InP and InGaP. The epilayers have been analyzed by double-crystal x-ray diffraction (DCXR), photoluminescence spectroscopy (PL), and secondary ion mass spectroscopy (SIMS). The high purity of the P_2 beam obtained through this method and the good behavior of the cell have been used to produce InP/InGaAs photodetectors and InGaP/GaAs/InGaAs LEDs heterostructures at low growth temperature (475°C). Further work will focus on using this P_2 source for reduced-temperature growth of InGaP/GaAs/InGaAs laser diodes for integration on GaAs VLSI chips using the epitaxy-on-electronics process.

1.6 Dry-Etch Technololgy for Aluminum-free InGaP/GaAs/InGaAs Laser Diode Facets and Deflectors

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Aluminum-free InGaAsP/GaAs/InGaAs laser diodes are receiving a great deal of attention currently because of their superior performance and reliability in comparison to more conventional AlGaAs/GaAs/InGaAs laser diodes. Our own interest in these devices is driven by their compatibility with the epitaxy-on-electronics (EoE) monolithic optoelectronic integration technology we are developing (described elsewhere in this report). In particular, high quality aluminum-free laser diodes can be grown at temperatures below 475°C, which are compatible with the EoE technology whereas laser diodes with aluminum in or near their active regions cannot be grown at such low temperatures.

An important challenge with aluminum-free heterostructures is dry etching vertical end-mirror facets and angled deflector structures because of the very different chemical make-up of the layers. In particular, the wider bandgap InGaAsP layers contain significant amounts of In and P, and relatively little or no As, whereas the narrow-gap GaAs and InGaAs layers contain roughly 50% As, no P, and relatively little or no In. Conventional chlorine-based and methane-based dry etch techniques do not work well with the aluminum-free heterostructures. We find, for example, that ion-beam assisted chlorine etching of InGaP is very slow at room temperature; at elevated temperatures where the InGaP etches satisfactorily, GaAs layers are etched without the ion beam, and severe lateral etching occurs, i.e., the etch is not directional and not anisotropic. While we can make use of this feature in the EoE process for removing polycrystalline deposits, it is not useful for facet etching.

The solution to this problem lies in changing the etchant from chlorine to bromine because the vapor pressures of the relevant bromides are much more similar than are those of the corresponding chlorides. Consequently, it is possible to find etch conditions for which the etch rates of InGaP and GaAs are sufficiently similar that vertical mirror facets can be successfully etched. We have used these results to produce the first etched-facet aluminum-free laser diodes. The threshold current densities of broad-area etched-facet laser diodes are a factor of two higher than adjacent cleaved-facet lasers.

The performance of the current etched-facet lasers is limited primarily by the quality of the etch mask, which we feel is in turn limited by the aligner used.

8 MIT Lincoln Laboratory, Lexington, Massachusetts.

Consequently a projection aligner has been acquired for use on this program; and preliminary indications are that its use significantly improves mask quality, i.e., edge definition and smoothness. Future work will combine this new tool with continued work refining the etch chemistry through the combination of both chlorine and bromine in the ion-beam assisted etch system (which is located in MIT Lincoln Laboratory). A heated, rotatable substrate stage has also been installed on the system in preparation for work on etching curved deflectors. These, along with the vertical end facets, are the key to producing the in-plane, surface-emitting lasers (IPSELs) we propose to integrate on GaAs integrated circuit chips using the epitaxy-on-electronics (EoE) process.

1.7 Monolithic Integration of Vertical-Cavity Surface-Emitting Laser Diodes on GaAs VLSI Electronics

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Vertical-cavity surface-emitting lasers (VCSELs) are particularly suitable as light sources for optoelectronics integration technologies, such as our epitaxy-on-electronics (EoE) process. The compact, vertical geometry and the completely epitaxial growth of VCSELs make mass fabrication and testing convenient and economical. The small size of the active region results in low threshold currents. Finally, the surface-emitting property results in an excellent beam profile of the emission, which simplifies coupling to optical fibers. VCSELs are emerging as ideal light emitters for high-density free-space interconnection.

VCSELs consist of several active quantum wells, sandwiched between two highly reflective distributed Bragg reflectors (DBRs). These DBRs are realized by epitaxial growth of AlGaAs layers, lattice-matched to GaAs, with varying aluminum and gallium compositions.

The production of VCSELs is not without its own set of challenges. Unlike in-plane semiconductor lasers, light in VCSELs resonates in the direction perpendicular to the thin quantum wells. In order to achieve laser action, the quantum wells must have high radiative efficiency and be situated inside a cavity with a high Q-factor. This requires the DBRs to have very high reflectivities and low total losses; they typically consist of many periods. Several design and growth concerns are important: First, the large number of layers creates numerous heterojunctions which require careful design such that the impedance of the whole device is minimized, and the threshold current and operating voltage remain low. Second, the growth conditions need to be controlled precisely while the structure is being grown, which typically takes four to five hours. Finally, the reflectivities of the top and bottom mirrors need to be carefully designed to strike a balance between high Q-factor and high external efficiency.

Presently, the goal is to achieve flat-bands for carriers in the DBR mirrors as part of the effort to arrive at a low threshold current. This can be achieved by gradually changing the aluminum and gallium compositions with a parabolic profile across the interfaces, while simultaneously maintaining the doping in the span of the grading regions at a much higher level than in the rest of the mirror stack. We focus our effort on p-type top mirrors, since holes have an effective mass eight times more than that of electrons, and thus are much more vulnerable to potential barriers at the heterojunction interfaces.

The optimal design for the grading regions is a compromise between a short enough length and a adequately gradual grading. Short grading regions lower the free carrier absorption resulting from the high doping level and maintain a high overall DBR reflectivity. Gradual grading yields lower impedance mirrors with smaller doping level. The transient behavior of the cells has also to be studied to determine maximum grading speed, because effusion cells used in MBE systems cannot control the flux accurately when the change is too fast.

VCSELs grown on bulk GaAs under normal growth conditions and in-plane lasers with similar quantum wells will be fabricated to compare basic material qualities and growth capabilities. We will also assess the impact of a reduced growth-temperature on the gain of the active region and on the conductivity of the DBR mirrors. This is critical for the adoption of this structure to our EoE technology.

1.8 Hyperthermal Molecular Beam Dry Etching of III-V Compound Semiconductors

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A novel ultra-high vacuum (UHV) compatible etch reactor has been designed, constructed, and characterized. The etch mechanism is dependent solely on the chemical reactivity of the neutral etchant gas, enhanced by its kinetic energy, and does not utilize any plasma or ion source in obtaining directionality or acceleration. As described in a recently completed PhD thesis, this work also reported the first demonstration of molecular chlorine etching of InP, this being done at chlorine pressures of 1 x 10^{-7} Torr with no ion, plasma, or e-beam assistance. It is expected that this etching technique will introduce very little damage in specimens, unlike the situation with ion-beam and plasma techniques.

The etchant gas in the present system is accelerated to supersonic speeds through the use of a free-jet expansion nozzle, skimmer, and differentially-pumped vacuum chamber. By varying the nozzle temperature and the concentration of chlorine in the gas matrix, the energy of the incident beam can be varied. The directionality of the molecular beam produced is maintained by using it in a UHV environment with background operating pressures of 1 x 10^{-7} Torr, or less. Since the translationally-activated molecules contribute to collision-induced dissociative chemisorption, a chemical reaction can be initiated in this way in an otherwise unreactive material system.

Both indium phosphide and gallium arsenide were etched using a translationally-activated molecular chlorine beam. Both directional and (111) crystallographically-preferential etch profiles were observed. The preferential etch was found to be the predominant etch profile at low beam energies, while directional etching was achieved when the beam energy was increased. Etch rates ranging from 0.2 microns per hour to 2.0 microns per hour were obtained at substrate temperatures ranging from 200°C to 350°C under various beam conditions.

Two quantitative in-situ process monitoring methods were also devised for this work: (1) a surface roughness measurement method which uses the reflected intensity of a 633 nm He-Ne laser beam, and (2) a technique for calibrating the substrate holder thermocouple at low-temperature which is based on monitoring the vacuum background pressure during the initial stages of the substrate temperature ramp.

It was found that under certain etch conditions an aluminum compound was deposited on the specimens which subsequently interfered with the etch process, thereby limiting the range of parameters and conditions which could be investigated. Subsequent study revealed that the source of the deposit was an aluminum ring holding the skimmer in position. This ring has recently been replaced. Funds are presently being sought to continue the development and application of this etch tool.

1.9 Microwave Characterization of Optoelectronic Devices

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The microwave device characterization capability has been expanded so that optoelectronic devices may be characterized using the automatic network analyzer and the on-wafer probe station. The objective was to do a complete characterization of the high speed performance of light emitting diodes (LED) both discrete and integrated on chip. The aim of preliminary measurements was to model the high frequency behavior of the LED and to determine the frequency limits of the desired characteristics. A comparison of the behavior of discrete and integrated devices is important to the understanding of the issues that are unique to the epitaxy-on-electronics integration technology. An accurate estimation of device performance together with physical modeling will result in the efficient application of LED as emit-

ters in OEIC's and will be the basis of proposed future investigations of high speed surface-emitting lasers.

To this end, measurements were performed on discrete light emitting diodes (LED) and LED integrated on the OPTOCHIP. The microwave reflection and transmission properties of the LED were measured using the HP 8753C network analyzer with a frequency range of 300 kHz to 3 GHz. This range was appropriate for the test devices which operated at frequencies under 3 GHz. The DC bias is applied with an HP 4145B semiconductor parameter analyzer. The optical output from the LED is collected by a high bandwidth detector which is placed close to the emission field of the LED to improve the collection efficiency. A Hamamatsu S5972 p-i-n photodiode with a 3 dB bandwidth of 500 MHz was used as a detector. The electrical signal from the detector was amplified using a Melles Griot high frequency amplifier. The scattering parameters were measured using this experimental arrangement.

Current-voltage (I-V) and light-current (L-I) characteristics were measured initially for a DC analysis. With reverse bias, the bulk devices had a higher leakage current than the integrated devices. It was concluded that lateral confinement was provided by dielectric growth wells in the integrated device on OPTOCHIP. With forward bias, both types of LED's show a turn-on current which is larger than expected. A 4-element model has been proposed to describe these effects The model explains the observed diode characteristics and indicates that the difference in turn on currents is associated with material quality. The difference in efficiencies is due to the different values of the non-radiative recombination coefficient and bimolecular recombination coefficient in the devices measured.

Since the LED is a two terminal device, measurements of S21 were used to determine the frequency response. A DC bias was applied to the LED and an RF signal was superimposed with enough RF power for small signal modulation of the LED about the bias level. The bias was varied, and the response was measured at each bias level. The frequency response of bulk and integrated devices was measured. The integrated devices on OPTOCHIP had a higher bandwidth than the bulk LED at comparable bias levels.

Our modeling indicates that the nominally undoped active regions of the LEDs was in fact quite n-type, and that significantly higher efficiency and bandwidth will be obtained if the active region is made narrower and is intentionally doped p-type. Such design modifications will be explored to enhance the performance of the LED's. The investigations will then be extended to vertical cavity surface emitting lasers (VCSEL).

1.10 Monolithic Integration of 1550 nm Photodetectors on GaAs Transimpedance Amplifier Chips

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Haifeng Wang, Professor Clifton G. Fonstad, Jr., in collaboration with Dr. Roe B. Hemenway, Jr.,[9] Robert Deming, James Mikkelson[10]

High data rate optical communication systems require increasingly complex integration of high performance electronic circuits with sophisticated optoelectronic devices. In the short run these needs can be met by hybrid assemblies. However, the cost, performance compromises, reliability concerns associated with hybrid integration, and the increasing need for specialized subcircuits which are not commercially available make development of the monolithic integrated circuit technology extremely desirable.

We are using several techniques to monolithically integrate 1550 nm photodetectors with gallium arsenide (GaAs) transimpedance amplifiers (TIAs) to form monolithic optoelectronic integrated circuits (OEICs) for fiber-based systems. Both epitaxy-on-electronics (EoE), described elsewhere in this report, and selective area semiconductor wafer bonding, also described elsewhere in this report, will be utilized. In the EoE process, optical devices are epitaxially grown on fully processed GaAs integrated circuits. For this application, high-speed photodetectors based on the lattice-mismatched InGaAs/GaAs material system are being developed and evaluated. For the wafer bonding process, fully lattice-matched photodetector heterostructures, grown under optimal conditions on InP, will be bonded onto the same

9 MIT Lincoln Laboratory, Lexington, Massachusetts.

10 Vitesse Semiconductor, Corporation, Camarillo, California.

GaAs circuits. After EoE epitaxy or wafer bonding, the device heterostructures will be processed and monolithically integrated with the pre-existing electronics, yielding high speed, compact, reliable monolithic OEIC's.

The GaAs transimpedance amplifier test chip (MIT-OEIC5/LL-MORX1), which incorporates modified versions of a commercial Vitesse transimpedance amplifier, has been designed and submitted to MOSIS for processing. Included on this chip are polarization diversity heterodyne photoreceivers, dual-balanced photoreceivers, and other functional cells; the chip is suitable for both EoE epitaxy and wafer bonding.

Initial results from measurements on 1550 nm photodiodes grown on GaAs have been obtained. The performance of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ pin photodiodes grown on GaAs substrates using linearly graded buffers were compared with those using graded short-period superlattice (GSSL) buffers. Detectors on linearly-graded buffer are found to be superior to those on GSSL buffer. However, the best dark current levels seen (5 μA for 50 μm square detectors at 2V bias) must to be reduced for final integration.

Several approaches to the reducing the leakage are being investigated simultaneously. A side-wall passivation technique using polyimide has been proposed and the required mask set is being generated. A second method is to replace the wide gap InAlAs with electrically superior InP. New heterostructures using InP as cladding layers have been grown and are being processed. Thirdly, we have lowered the indium concentration grading rate from 17% per micron to 10% per micron, aiming at lowering threading dislocation density in the absorption layer. Finally, a novel structure, the Uni-Travelling-Carrier Photodiode (UTC-PD), is being considered for both dark current reduction and speed enhancement.

Optimized detector MBE growths have been carried out on both n-GaAs and n-InP substrates for a comparative study of the effects of lattice mismatch. Photodetectors will also be grown on p-InP substrates in order to be bond onto the GaAs chips. Wafer bonding using both direct bonding of InP and InGaAs to GaAs by atomic rearrangement, and bonding with palladium assistance will be investigated. The method yielding the best electrical characteristics will be chosen to bond the detectors onto OEIC5 chips.

Future work will expand the effort to include integration of 1550 nm light emitters as well as detectors, which requires significant work on direct wafer bonding of InP-based materials onto GaAs chips and/or work on high quality lattice-mismatched InGaAs/InP epi-layers on GaAs.

1.11 Design and Analysis of VCSEL-Based Resonant Cavity Enhanced Photodetectors

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University of Ulm, Ulm, Germany

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Dr. Thomas Knoedl, Henry K. Choy, Joseph F. Ahadian, Professor Clifton G. Fonstad, Jr.

It is extremely desirable for monolithic optoelectronic integration to have emitters and detectors operating at the same wavelength, which can be fabricated from the same basic heterostructures. To this end we have modeled and studied (theoretically at this stage) the design of resonant cavity enhanced photodetectors (RCEPs) using heterostructure designed primarily for vertical cavity surface emitting lasers (VCSELs).

A transmission matrix model was developed to compute the optical electric field and power in a complex, multi-layered heterostructure. The input to the program is the composition profile of the structure, and the program calculates the spectral response of the detector after first calculating the appropriate refractive indices, absorption coefficients, etc. The program can accommodate graded interfaces and doping profiles, hyperation as well as variations in temperature and in incident angle.

Simulation indicates that the most important parameter for the device designer is the top mirror reflectivity. As expected, there is a direct competition between the peak quantum efficiency of an RCEP and its spectral bandwidth. It is clear from the analysis that the narrow spectral bandwidth inherent in achieving a useful peak quantum efficiency from a single-resonant-cavity RCE fabricated from a modified VCSEL structure, and the significant shift of the resonance to longer wavelength seen with increasing temperature, that the usefulness of simple RCEP/VCSEL combinations is very limited. Consequently,

we have also studied VCSEL-based RCEPs with broadened response spectra created by depositing additional, multiple-resonance mirror stacks on the top surface, after first modifying the original VCSEL top mirror stack. Initial indications from these studies, which are still in progress, indicate that this approach is very attractive.

A simple model allowing one to make a first order approximation to estimate the high speed behavior of RCEPs was also developed. The indication is that RCEPs can be twice as fast as PIN detectors with comparable quantum efficiencies.

This research was conducted by Dr. Thomas Knoedl during a six-month stay in our laboratories at MIT and was presented as his minor thesis (Studienarbeit) to the University of Ulm in January 1998. It is planned that Dr. Knoedl will return to MIT in summer 1998 to continue with an experimental investigation of resonant cavity enhanced photodetectors fabricated from VCSEL heterostructures.

1.12 Si-on-GaAs: Monolithic Heterogeneous Integration of Si CMOS with GaAs Optoelectronic Devices using EoE, SOI, and MEMS Techniques

Sponsor

General Motors Corporation Fellowship

Project Staff

Joanna London, Joseph F. Ahadian, Professor Clifton G. Fonstad, Jr.

As electronic technology becomes faster and denser, electrical interconnects (wires) have begun to limit the performance of the systems that depend on them. In order to alleviate this problem, optical interconnects are being considered as an alternative. Some of the benefits of optical interconnects include higher speeds of operation with low-drive requirements and minimal power dissipation; reduced size, weight, and cost; freedom from electromagnetic interference, crosstalk, and eavesdropping; and ease of layout and routing.

In order to implement optical interconnects, optoelectronic integrated circuits (OEICs), which integrate both electrical device (transistors) with optical devices (optical detectors and emitters), must be created. Silicon is the dominant material used in electronic integrated circuits such as digital signal processors, microcomputers, and memory. However, due to the intrinsic structure of silicon, this material is not capable of emitting light efficiently. Compound semiconductors such as gallium arsenide, on the other hand, can be used to make light emitting devices such as light emitting diodes and lasers. Engineers have been trying without success for some time to develop the technology that would support the monolithic integration of these two types of semiconductors.

A new technology has been proposed by our group at MIT which will combine silicon and gallium arsenide substrates by wafer bonding. This process builds upon pre-existing expertise at MIT in the area of wafer bonding silicon substrates. Yet, due to the vastly different composition of gallium arsenide, this process will have to be significantly modified in order to result in success.

Two other technologies, which have been studied at MIT, are silicon on insulator MOS technology (SOI) and epitaxy on electronics (EoE). SOI is a method of fabricating CMOS transistors in a thin layer of silicon, which is separated from the silicon substrate, by an insulating layer of silicon dioxide. SOI has become important recently because this process is able to significantly reduce stray capacitances, and this will ultimately lead to higher performance devices. EoE, which is described in more detail elsewhere in this report, is a technology in which optoelectronic devices are monolithically integrated with gallium arsenide electronics by growing optoelectronic device heterostructures epitaxially directly on fully processed integrated circuits. The EoE technology has been perfected using electronic devices made in gallium arsenide. However, to obtain wide scale acceptance in industry, silicon electronics must be used instead. This will now become possible by combining wafer bonding, SOI, and EoE techniques.

After the silicon and gallium arsenide are bonded, electrical devices will be fabricated in the silicon. Windows will be etched through the silicon to the underlying gallium arsenide so that optical device heterostructures can be grown following standard EoE techniques.

Wafer bonding, SOI, and EoE will allow us to overcome the previously insurmountable problems caused by the large thermal expansion coefficient mismatches and lattice mismatches between silicon and the compound semiconductors. By taking

advantage of these recently developed techniques, it will now be possible to monolithically integrate state-of-the-art silicon CMOS electronics and high performance III-V optoelectronics devices producing OEICs of unprecedented complexity and performance. The successful demonstration of this technology will have significant technological and economic ramifications and make practical many applications of optical interconnects that have long been anticipated, but have yet to be realized.

1.13 Aligned, Selective-Area Wafer-Scale Bonding of Optoelectronic Devices on GaAs Integrated Circuits

Sponsors

Lockheed-Martin Corporation

National Science Foundation

Project Staff

Donald S. Crankshaw, Professor Clifton G. Fonstad, Jr.

The purpose of the OPTOCHIP project is to create optical devices on commercially fabricated electronics. The electronics portion of the chip is processed at Vitesse, leaving wells open for either LED or VCSEL devices. Previous work has successfully produced LEDs inside these wells by MBE growth. VCSELs, however, are more challenging, requiring higher quality than the LEDs. Wafer bonding offers an alternative method. Wafer bonding is the method for attaching two semiconductor wafers face-to-face, so that they may be considered one wafer. Using this technique, the lasers can be grown in bulk on a separate substrate, then processed into pillars to fit inside the wells. The pillars may then be bonded into the wells and separated from the original substrate.

Some of the common bonding methods in use are epitaxial lift off (ELO), Palladium bonding, and wafer fusion. The most attractive alternative is wafer fusion. Wafer fusion uses heat and pressure to bond the wafers, creating covalent bonds between the atoms of the two semiconductors. This gives the best optical properties, as well as excellent mechanical and electrical properties.

One of the unique aspects of this research is that the bonding is done over a very small area. Wafer bonding is generally done over the relatively large area ranging from a 20 mm^2 chip to a full wafer. This project requires the fabrication of pillars on these chips of areas around 10 to a 100 μm in width. This structure and the extraordinarily small area raises some unique problems. First, the small area can make it difficult to accurately apply a force which corresponds to an appropriate pressure. This can mean that extraordinary pressure is applied to the surface, possibly causing damage. Added to this is mass transport, the diffusion associated with mobile atoms of Group III elements at elevated temperature. Deformations in the structures have been observed, most likely due to these factors, but they are small compared to the scale of the features and unlikely to cause difficulty.

Another unique feature of this research is the requirement that the two wafers be aligned prior to fusion. The pillars must be aligned with the wells before the wafers are placed together and subsequently fused. This project seeks to demonstrate that alignment of III-V materials is possible using the same infrared alignment techniques used to align silicon wafers for bonding.

1.14 Normal-Incidence Quantum Well Intersubband Photodetectors (QWIPs) for Monolithic Integration

Sponsors

Lockheed-Martin Corporation

National Science Foundation

U.S. Navy - Office of Naval Research

Project Staff

Janet L. Pan, Professor Clifton G. Fonstad, Jr.

Band gap engineering allows us to design the peak responsivity of a quantum well intersubband photodetector (QWIP) to be at anywhere in the infrared region beyond about 2 μm. This wavelength region is useful for spectroscopy and identification of unknown gases, as well as for imaging in the Earth's atmosphere in the transparent spectral regions of 3 to 5 μm and 8 to 12 μm. The narrow spectral responsivity of QWIPs allows for the use of lenses, which are cheaper and smaller than mirrors, in the optical systems used to focus infrared radiation onto the detectors. This flexibility in the location of the peak in the responsivity spectrum, as well as the narrow spectral width of the responsivity, are also useful in the design of dual band and dual color QWIPs. Detection of the infrared radiation emanating from an object at two

different wavelengths makes it possible to ascertain the absolute temperature of the object and to distinguish it from "The surrounding clutter".

Modern epitaxy techniques can achieve high uniformity of semiconductor parameters across entire III-V (GaAs and InP) wafers, which allows for the realization of large focal plane arrays (FPAs) of QWIPs with low spatial (fixed) pattern noise. Furthermore, the growth of QWIPs on GaAs substrates is compatible with the monolithic integration of QWIPs with standard GaAs detector circuits. Monolithic integration would remove the need for indium bump bonding, an extra processing step which contributes to increased expense and reduced yield, and monolithic integration is one of the important objectives of our program. Specifically, our goal is to fabricate QWIPs which can be monolithically integrated with standard GaAs detector circuits using the epitaxy-on-electronics (EoE) process.

QWIPs which can respond to normally incident radiation will eliminate the need for an optical grating and for thinning of the devices, thus simplifying the processing and increasing the processing yield for such devices. However, the intersubband absorption of normally incident radiation is in general very weak; it depends on the size of the electron's transverse wave vector or the size of the bulk spin-orbit interaction. By paying special attention to such issues, we have successfully demonstrated the first n-type QWIP (n-QWIP) which responds to normally incident radiation without the use of an optical grating. Such QWIPs are observed to have a conversion efficiency of about 3 percent. While this is an important result, the quantum efficiency of such devices can be increased further by utilizing a transition which exhibits even stronger absorption of normally incident radiation. We are currently investigating strained, pseudomorphic p-type QWIPs for this purpose.

Whereas tactical missions in the past have required focal plane arrays to detect targets which are brighter than the background, with about 10^{16} photons/cm^2-s reaching the detector, recently, there has been a shift in the applications of quantum well infrared photodetectors towards detection in space of faint targets at large distances of several thousand kilometers with only about 10^{13} photons/cm^2-s reaching the detectors. Future work on QWIPs must not only focus on increasing the photoconductor conversion efficiency, but also on the more stringent requirements on FPA uniformity, linearity, and dark current of such applications. Faint targets require larger pixel sizes and better uniformity across the fewer pixels. Better linearity is also needed in situations where absolute radiometry is required. Device modeling is now being carried out in an effort to increase the ratio of the photocurrent to the dark current by increasing the ratio of the photoconductive gain to dark current gain.

1.15 Publications

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