Memory and Data Communication Link Architecture for Micro-Implants

by

Harneet Singh Khurana

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Computer Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2010

Author .....
Department of Electrical Engineering and Computer Science
January 8, 2010

Certified by .....
Joel Dawson
Associate Professor of Electrical Engineering
Thesis Supervisor

Accepted by .....
Terry Orlando
Chairman, Department Committee on Graduate Theses

Memory and Data Communication Link Architecture for Micro-Implants

by

Harneet Singh Khurana

Submitted to the Department of Electrical Engineering and Computer Science
on January 8, 2010, in partial fulfillment of the
requirements for the degree of
Master of Science in Computer Science and Engineering

Abstract

With the growing need for the development of smaller implantable monitors, alternative energy storage sources such as high density ultra capacitors are envisioned to replace the bulky batteries in these devices. Ultracapacitors have the potential to be integrated on a silicon wafer, and have the benefits of an unlimited number of recharge cycles and extremely rapid recharging times. However, they present an essential challenge in that the voltage drops rapidly with energy drain. In this thesis, we explore a data storage memory that is compatible with ultracapacitor energy storage. In addition, we propose and demonstrate a low-power wireless link that exploits RFID techniques as a way of uploading the stored data.

Thesis Supervisor: Joel Dawson
Title: Associate Professor of Electrical Engineering

Acknowledgments

First of all I want to thank my research advisor Prof. Joel Dawson for giving me an opportunity to be part of the Dawson Research Group and the chance to gain from his experience and advice. I want to thank him for always being the source of encouragement to improve and excel, whether it was in analyzing a problem or improving performance of a device and even in improving my presentation skills. Thank you Prof. Dawson.

Secondly I want to thank everyone at the Dawson Research Group including Philip Godoy, William Sanchez, Tania Khanna, Zhen Li, Jose Bohorquez, Taylor Barton, Eric Winokur, Sungwon Chung, Muyiwa Ogunnika, Jack Dong, and Jon Spaulding for making my experience at MIT memorable.

I am extremely thankful to my dad for being the source of inspiration and constant guidance. Thank you dad for everything. I want to thank my mom who stays in my heart through each day of my life. I want to thank her for the learning direction she showed at my early stage of life which has guided me to this point and will continue to do so in future. Thank you mom.

And, I want to give many many thanks to my fiancée for always being there for me. You have throughout been extremely supportive. See you very soon!

Thank you God for everything provided.

Contents

List of Figures

List of Tables

Chapter 1

Introduction and background

The evaluation and effective treatment of patients suffering from movement disorders such as Parkinson's disease, restless legs syndrome, and others require continuous monitoring and reliable data collection [7]. For determination of the correct medication dosage, doctors need to know both the intensity and duration of the tremors reliably. The tremors are usually in the frequency range of 5-10 Hz. To differentiate the limb movement of a healthy person from that of a person afflicted with Parkinson's or some other disease, filtering and algorithms can be used to reject false data and store only the data due to tremors. This has been accomplished previously using wrist-band style monitoring equipment [10]. However, the accuracy of the data collected depends critically on the patient to wear the gadget at all times. For some patients, this need for compliance stands as a very real barrier to meaningful data collection. Another issue is that the batteries these devices use have a limited number of recharge cycles, and the recharging operation itself can be time consuming. To overcome these challenges, our group is doing extensive research and developing a system-on-chip providing sensing, power management and energy storage in high energy density ultracapacitors to serve as a platform for monitors that are small enough to be implanted.

Ultracapacitors are promising for the implant application. These are capacitors with orders of magnitude more effective surface area in the same volume that an ordinary capacitor has, giving them a higher capacitance to store charge. This is ac-

complished by using porous coatings on electrodes or similar techniques that increase charge holding area.

Ultracapacitors have many potential advantages over batteries for implant applications, despite their considerably smaller energy density. They show promise of being able to be integrated on a silicon die, resulting in a smaller form factor for the implant. Also ultracapacitors can be quickly recharged without a need for complicated recharge circuitry.

For the chip to be injectable the size will be approximately 2x2x5mm encapsulated in a bio-compatible material, about the size of a grain of rice. This form factor allows the device to be implanted using an outpatient procedure which qualifies as "minimally invasive [3]. These minimally invasive on-chip devices will be used for the sensing and recording of tremors in a patient. The data collected from tremors is stored in a memory and later uploaded to an external base-station. The idea of such micro-implantable device is depicted in Fig. 1-1.

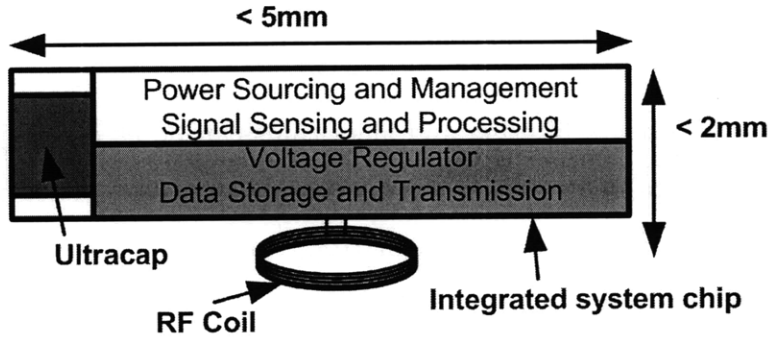

Figure 1-1: Conceptual drawing of the future product

In this thesis I have studied and designed an SRAM (Static Random Access Memory) to work with such system-on-chip implants and integrated an RFID based data link to upload the data to an external reader. The system block diagram of the design is shown in figure 1-2. To effectively deal with the supply voltage variations inherent in using an ultracapacitor energy storage element, the SRAM chip has a voltage regulator to step down the voltage to reduce wasteful energy loss. The control circuitry is implemented on an FPGA.

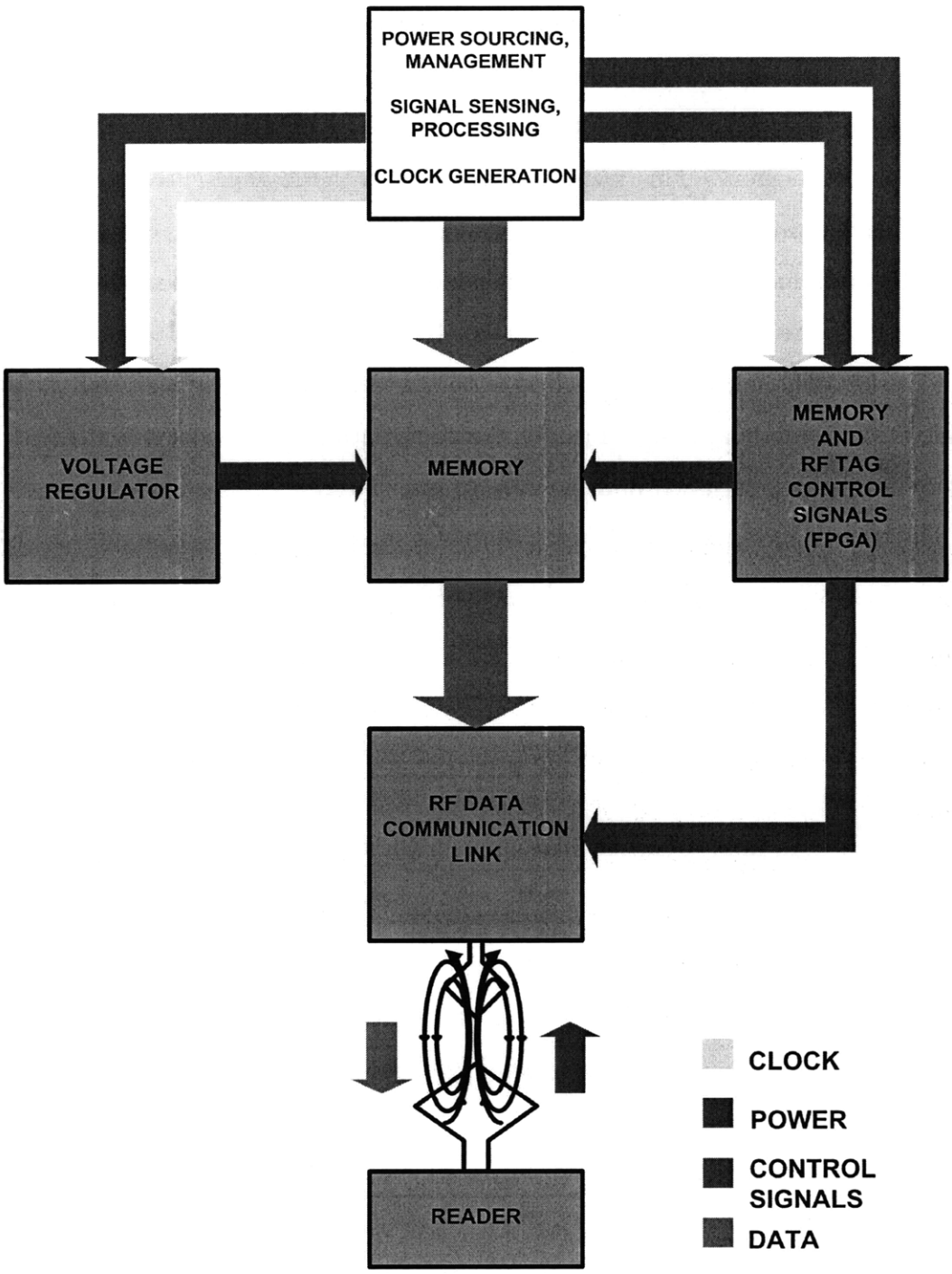

Figure 1-2: Block diagram of the system

The memory designed in this thesis is a 32-Kb SRAM (256 rows x 128 columns) with a 6-transistor bit cell configuration. The data is input to the memory 8 bits at a time on an 8 bit input bus. The 8 bit input is temporarily registered in registers

inside the memory. After 16 such 8 bits are received and registered, it gets copied to a row of the memory core (bit-cell memory matrix) at a time. An on chip voltage regulator steps down the high ultra-capacitor supply voltage to a quarter of it for supply to the memory. This lower voltage reduces the leakage currents in memory thereby saving precious charge on ultra-capacitors.

RFID data link is composed of a transponder and a reader along with their inductive coils. The reader and its coil generates RF field that couples to the coil on the implant side. The implant side modulates the carrier field by switching the implant's coil load. This modulated signal is interpreted as data on the reader side. This RFID based data link is discussed in a separate chapter later.

The control signals are generated by programming Xilinx FPGA on an Opal Kelly board. This generates a sequence of signals to accomplish write and read operation from memory. It also generates the modulation signal based on the stored data for transmission over RFID data-link. This is discussed in a later chapter.

This thesis is organized as follows. Chapter 2 is a discussion on the memory design. Chapter 3 is a discussion of the voltage regulator. Chapter 4 talks about the RFID based data link. Chapter 5 documents the test results. Chapter 6 concludes the thesis with the summary and possible future work.

Chapter 2

Memory

Micro-implants require storage memory to store the information gathered by on-chip sensors. This information is stored in the form of digital data that is later transmitted over a wireless link, such as a RFID link, when in close proximity to a reader. This chapter focuses on the design of memory for implants.

2.1 Memory types

Solid-state memories can be classified into volatile and non-volatile memories. While non-volatile memories are appropriate if the power source is unreliable [6] or for long time data storage due to zero power consumption during standby feature, it poses a challenge to writing the data in micro-implant application.

Non-volatile memories are based on a floating gate between the signal gate and the channel of a MOSFET transistor. The programming/ writing of data in a bit cell is accomplished by changing the charge trapped on the floating gate [6]. The presence of charge changes the threshold voltage of the transistor. This difference of threshold voltage due to presence or absence of the trapped charge can differentiate between a 1 and 0 stored in a cell. During read operation, this is done by applying a nominal voltage across the gate and source that is sufficient to turn on a low threshold device but not a high threshold device to discriminate between the two bit values. The floating gate stores the charge almost indefinitely if surrounded by a good dielectric.

This accomplishes the zero power loss feature of non-volatile memories as no power is needed for the data retention. However, during programming/ write, high gate-source and gate-drain voltages (about 10 V or more) are needed to provide the high fields for an avalanche injection and charge trap to occur. The high-voltage requirement is particularly onerous for the micro-implant application, which otherwise exploits low-voltage CMOS processes. In addition, the special processes needed to build these flash memories can raise the cost of the final product.

The other class of memory is the volatile memories that requires power at all times for data retention. The most common are the dynamic and static RAM. The dynamic memories again require special processes to construct the vertical capacitors that store a bit of data in each bit-cell. Also these require frequent recharge of the capacitors with the value stored to compensate for the stored charge lost due to leakage. This adds to the complexity of the memory and loss of energy. The other kind of volatile memory, static RAM (SRAM), requires more area to implement than the dynamic RAM but has lower leakage currents during data retention. Also it requires a fraction of the voltage required in non-volatile memories to write to each cell. In this thesis I have designed an SRAM for the application to bio-medical implants.

2.2 Basic operation

Before getting into the design details, let us look at the bigger picture of the operation of this memory. The data received on the input data bus is 8 bits at a time. They need to be temporarily stored and batched into a complete memory row before being written into a row of the memory. This batch writing row at a time requires fewer accesses to the memory matrix cells and saves energy. Therefore there are registers at the bottom of the memory matrix equal in number to the number of memory cells in a row.

This memory consists primarily of a bit-cell matrix, registers at the bottom periphery of the matrix, and the input-output data bus. The following sections details the steps for writing to and reading from the memory.

2.2.1 Writing the data received on the data bus

The following basic steps go into writing to this memory.

Step 0: The address counter is reset with the CLEAR signal to point at the first row of the memory matrix.

Step 1: The data is received in packets of 8 bits at a time on an 8-bit data bus. These are written to the 8 registers, one at a time at the negative edge of the CLK signal. The next 8-bits received go into the next 8 registers. Once all 128 registers have been written Step 2 is executed. This step is depicted in Fig. 2-1.

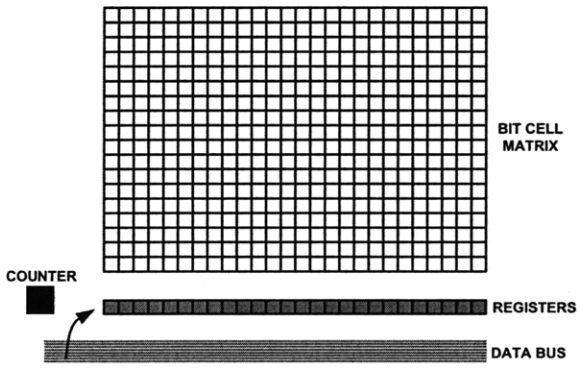

Figure 2-1: Basic write functionality: Step 1

Step 2: Once all 128 registers have been written with the input data, they are copied into the current row of the memory bit-cell matrix. The current row is the row currently addressed by the counter. After this the counter is incremented. This step is depicted in Fig. 2-2

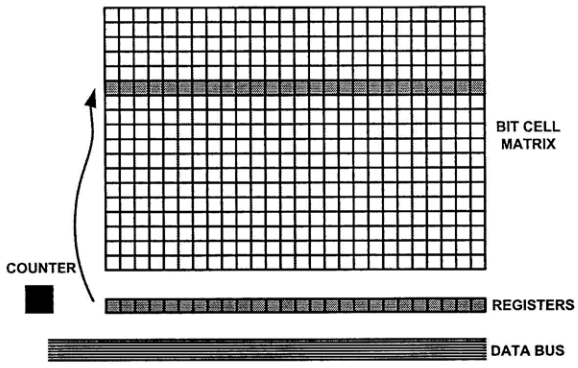

Figure 2-2: Basic write functionality: Step 2

2.2.2 Reading the data stored in the memory matrix

The following steps go into reading the data previously stored in this memory.

Step 0: The address counter is reset with the CLEAR signal to point at the first row of the memory matrix.

Step 1: The memory matrix row currently addressed by the counter is copied into the registers at the bottom of the bit-cell matrix. The registers containing the data are then connected to the data bus one at a time at the positive edge of the CLK signal. After all 128 registers have gone through this process, the counter is incremented to address the next row as the current row and Step 1 is repeated. This step is depicted in Fig. 2-3

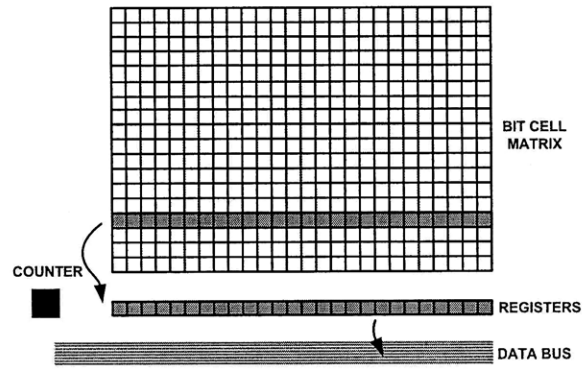

Figure 2-3: Basic read functionality: Step 1

2.3 Memory architecture

The architecture of the memory designed is shown in Fig. 2-4. The memory size is 256 rows by 128 columns totaling to 32768 bit-cell locations. The memory matrix is written or read a row at a time. The data is received by memory in chunks of 8 bits at a time, they are temporarily stored in the 128 registers at the bottom of the matrix. Once the 128 bits are registered, they are copied into the current row of the memory matrix. This reduces the energy overhead associated with charging the control lines by writing row at a time instead of 8 bits as received.

Besides registers the bottom periphery of the matrix has additional logic circuitry to decode the register address and to connect or disconnect the input and output of register to data bus and vertical bit-lines. Along the other side of the periphery on the left of the matrix is the logic circuitry that decodes the row address for each row of the matrix. The left side circuitry also includes the power management logic that simply turns off rows not yet written to conserve energy.

The row and register address is generated sequentially by the 15 bit counter. This address is pre-decoded locally with circuitry around the counter to minimize decoding logic alongside the periphery of the matrix. This enables smaller pitch spacing by decreasing the number of devices along the memory matrix periphery.

The memory is powered by an on-chip voltage regulator implemented using a stack of capacitors on the left side of the memory matrix that steps down the input supply voltage shown as Ultracap. This capacitor bank is switched between parallel and series configuration to reduce the high Ultracap voltage to quarter of it. This reduced voltage ensures minimal lower power losses both during data retention and while actively writing a bit-cell by minimizing leakages and switching energies respectively.

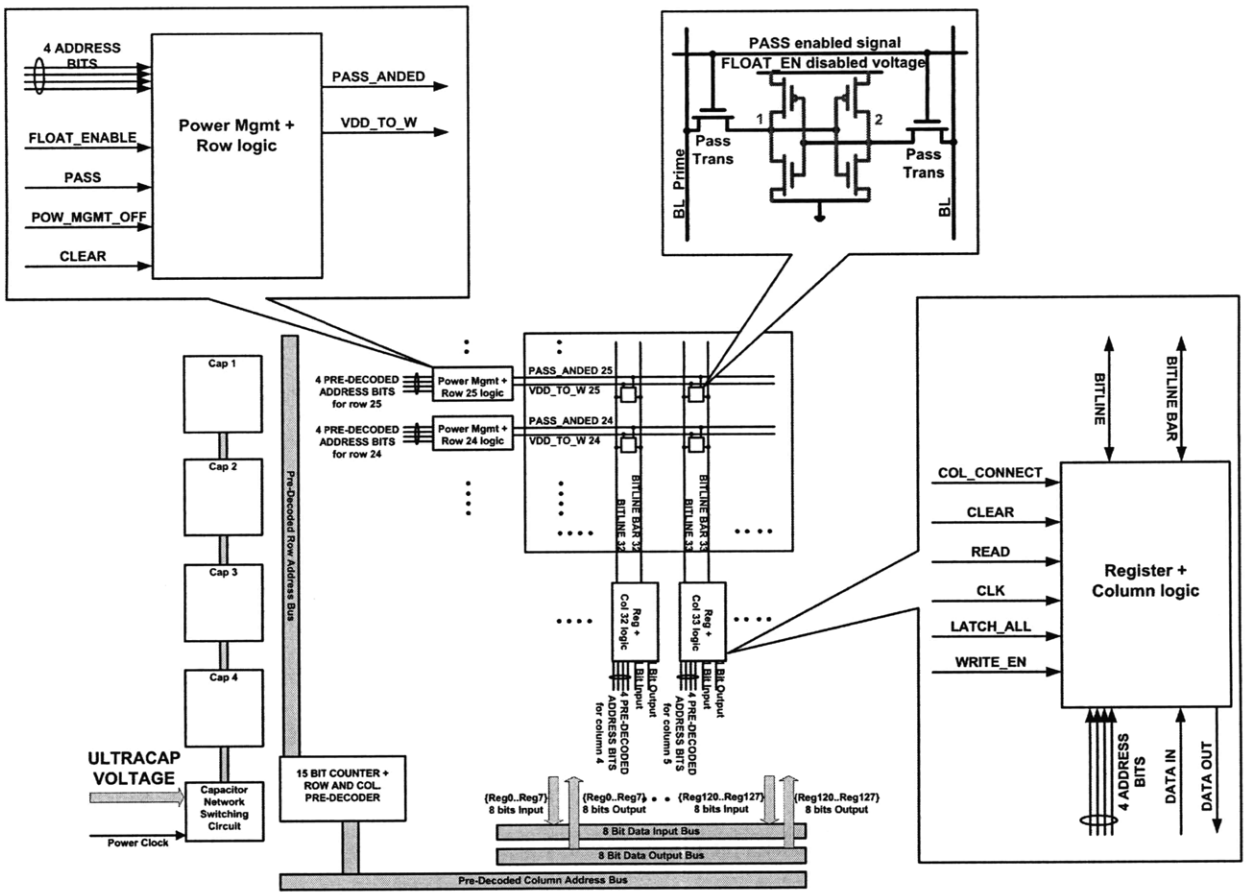

Figure 2-4: Memory architecture

2.4 Leakage

Leakage current is the drain current that arises with a zero voltage difference applied across the gate and source terminals of a transistor. This current increases with the width of the transistor as one would normally expect due to the lowering of the resistance with the increase in width. This effect is shown in the simulation Figs. 2-7 and 2-8 for NMOS and PMOS respectively for the National's 0.18 CMOS process used in this thesis.

Also one would expect this current to increase with decreasing length due to the expected monotonic lowering of the threshold voltage. However it is usually observed to first increase with decreasing length for moderately small L, before it decreases as expected [11]. This effect is called reverse short-channel effect. This contradicts the normal behavior of resistance decrease as length decreases. This effect is shown in simulation Figs. 2-5 and 2-6 for the NMOS and PMOS respectively for the National's 0.18 CMOS process.

In order to minimize the leakage current, I have used the minimum allowed transistor length and width for both NMOS and PMOS in the 6T bit-cell configuration to be discussed later.

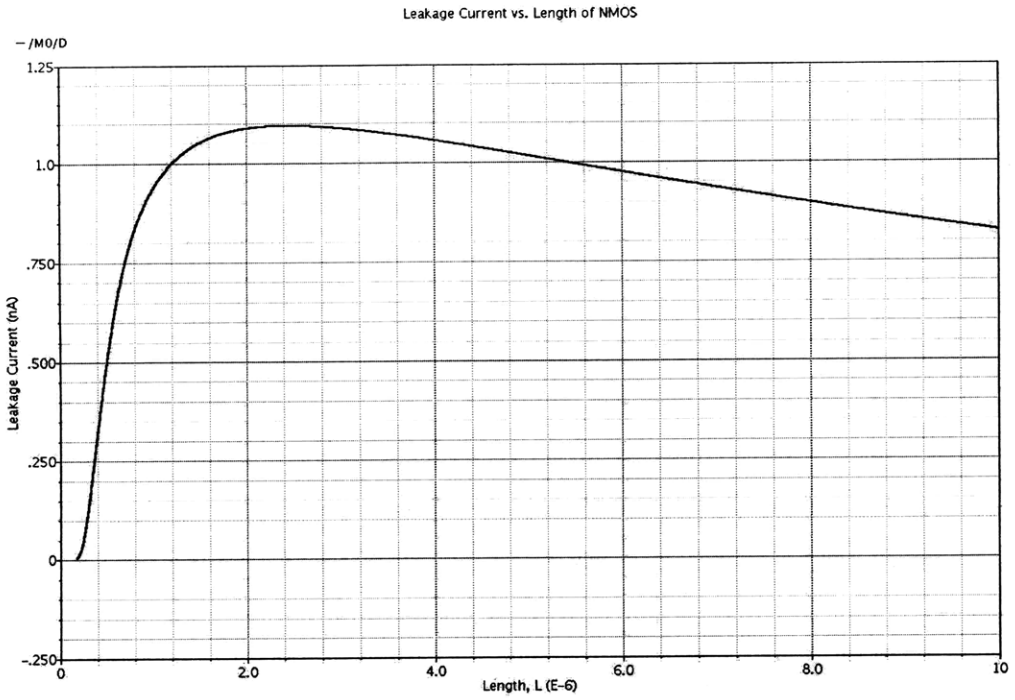

Figure 2-5: Leakage current versus length of NMOS transistor

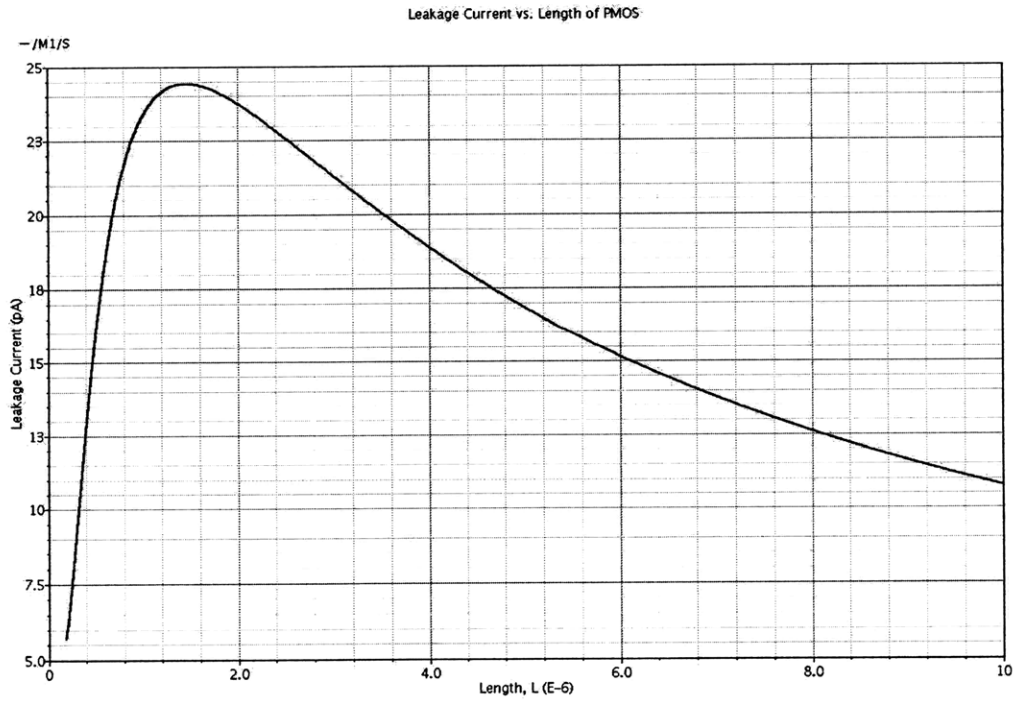

Figure 2-6: Leakage current versus length of PMOS transistor

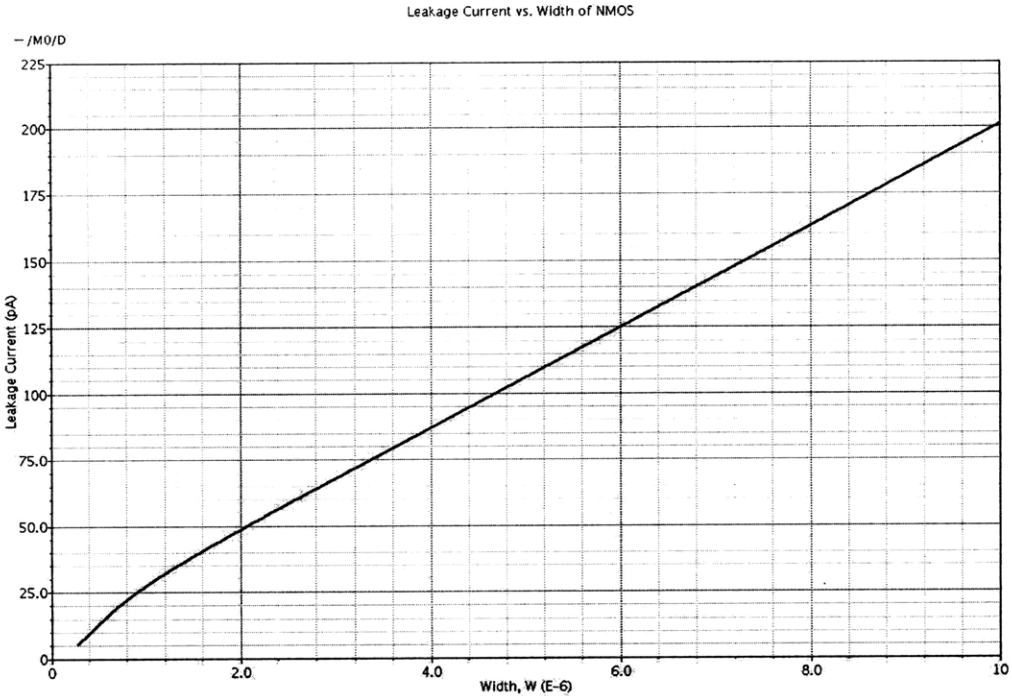

Figure 2-7: Leakage current versus width of NMOS transistor

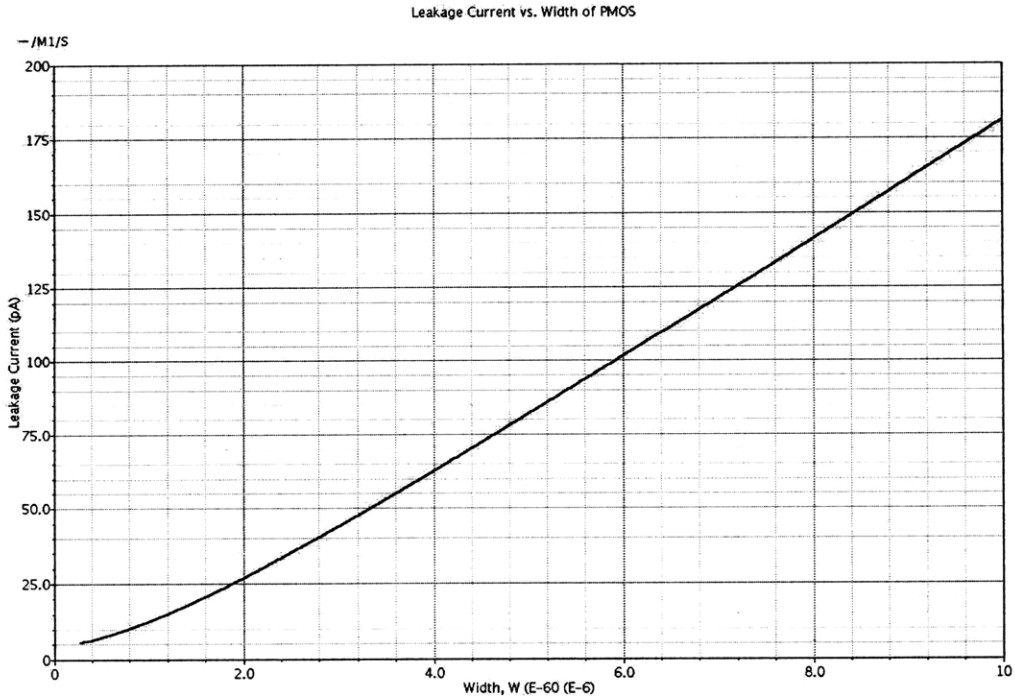

Figure 2-8: Leakage current versus length of PMOS transistor

2.5 Bit-cell

The SRAM 6T bit-cell consists of two CMOS inverters back to back with output of each connected to the input of the other as illustrated in Fig. 2-9. The input of each inverter is connected through a pass transistor to the vertical bit-lines that enables data written from or data read to the registers at the periphery of the memory matrix. The pass transistors allow controlled connection between the two inverter inputs and their respective bit-lines.

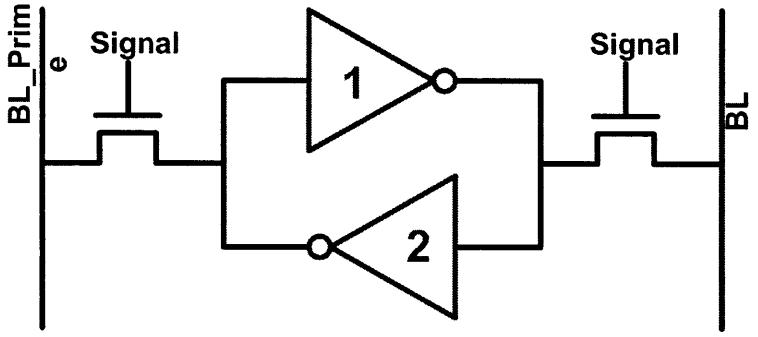

Figure 2-9: 6-transistor bit-cell configuration

In Fig. 2-10 are shown the generic DC inverter transfer functions of the two inverters 1 and 2. The intersection points are the only possible equilibrium solutions when the inverters form a loop. The inverter loop has three equilibrium points (points A, B, and C in the figure), only two of which are stable (A, B). If initially at point C, there is always some noise present that topples the loop state to assume one of the stable points A or B.

The same figure can help us understand the transient behavior. The intersection points are the equilibrium points after the transients have settled. Let us consider point A. For a small perturbation off point A, negative feedback returns the inverter loop to the same point. It is similar for point B. At point C a positive feedback prevails and any perturbation off it sends the inverter off the stable point towards A or B. To switch from A to B, either input 1 can be driven beyond point C or input 2 can be driven below point C or both. After doing this the loop can be left alone and positive feedback will send the loop to settle at point B. Similarly to switch from

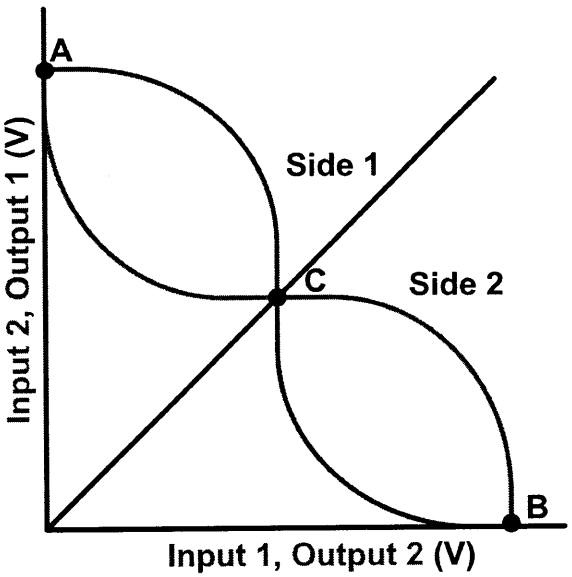

Figure 2-10: Inverter loop DC transfer function curves: Butterfly curve

B to A, either input 1 can be driven below point C or input 2 can be driven beyond point C or both.

2.5.1 Writing

Writing is accomplished by driving the bit-lines to the voltage levels corresponding to the bits to be written and then signaling the pass transistors to turn on. This connects the bit-lines to the inputs of the two inverters and forces the inverter inputs to be driven to their respective bit-line voltage levels. The voltage levels of the inverter nodes should be driven past the switch point of the inverter loop for a successful write. For example assume initially that the inverter loop is at state A in Fig. 2-10 and the loop was to be switched to state B corresponding to writing an opposite value to the one initially stored. For a successful write operation, the input of inverter 1 or inverter 2 or both should be driven at least beyond the switch point C towards the state B. The pass transistors can then turn off, allowing positive feedback in the inverter loop to take over and complete the change of state. This would require the NMOS pass transistor connected to the bit-line driven to zero to be stronger, that is, able to sink more current, than the PMOS can supply so that the node can be pulled low enough for switch to happen. This requires larger NMOS transistors. Another method is to shut down the supply voltage to the bit-cell, then drive the bit-lines with the value to be written, turn on the pass transistors connecting the bit-lines to their respective input nodes of the loop inverters, and then turn on the supply voltage to the bit-cell before turning off the pass transistors. In essence we pick the state of the inverter loop and then turn on the loop to maintain the new state. This technique of floating the supply line has been widely used [2]. Using this technique doesn't require the pass transistors to be stronger than the PMOS transistors and has been used in this design. This way we can still use the minimum sized transistors that give us lowest leakage as shown before. The bit-cell node data before and after successful write operation is shown in Figs. 2-11 and 2-12 respectively.

Before write operation:

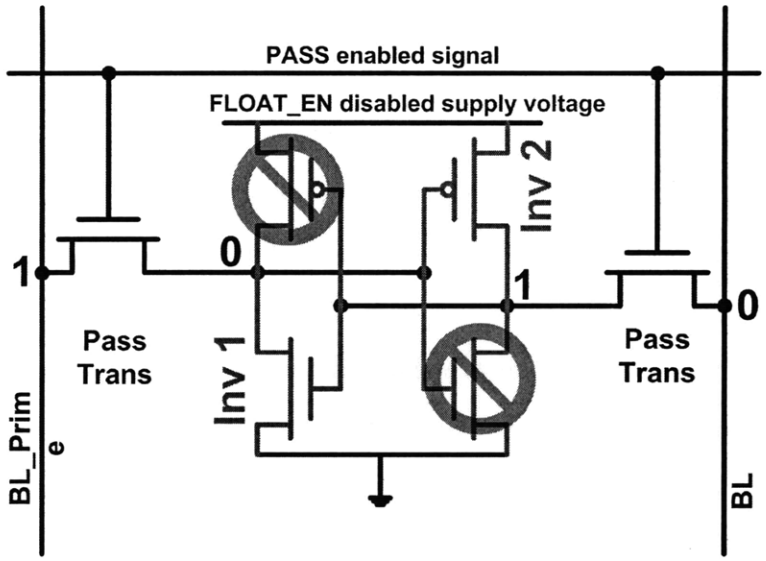

Figure 2-11: Bit-cell state before write

After write operation:

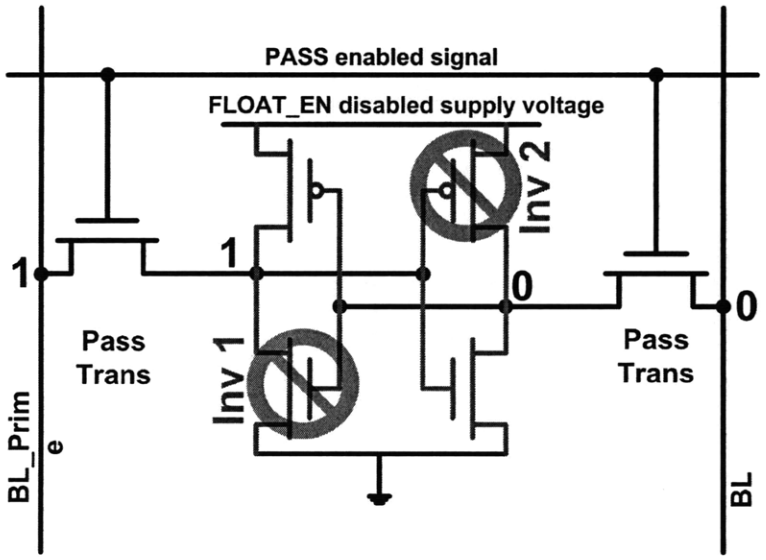

Figure 2-12: Bit-cell state after a successful write

2.5.2 Reading

To read the bits written previously to a memory bit-cell, both the bit-lines are pre-charged to the high voltage corresponding to a 1 and left floating at this value. Then the pass transistors are signaled to turn on. This connects the inverter inputs to their respective bit-lines through the pass transistors as shown in Fig. 2-13. The bit-line connected to the 0 node on the inverter loop discharges and the other bit-line stays at 1 since it is connected to the node at 1. A successful read is if the stored bit in a bit-cell is not corrupted by the pre-charged capacitive bit-lines. This is when the nodes of the inverter loop do not drift beyond the switch point. This would ensure that when the pass transistors turn off, the inverter loop will return to its original equilibrium state.

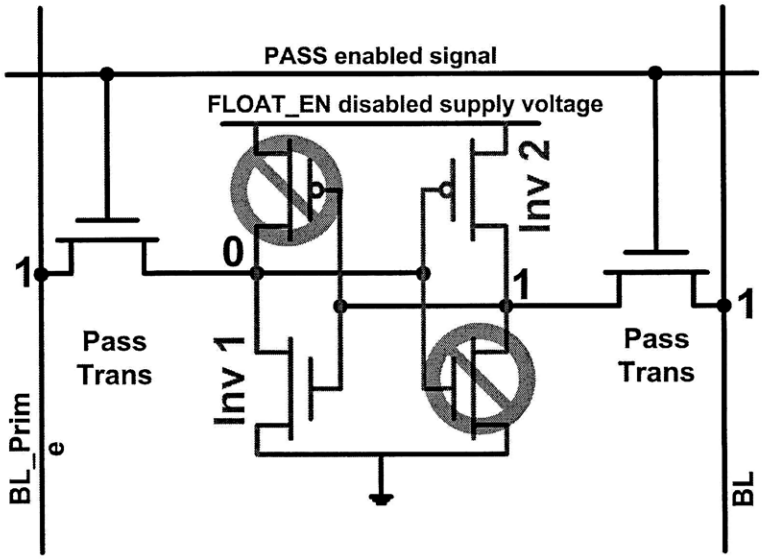

Figure 2-13: Bit-cell state during read

For example assume initially the inverter loop is at state A in Fig. 2-10. When the pass transistors are turned on, it connects the input nodes of the inverter loop to the bit-lines. The input node of inverter 1 is pulled up temporarily while the bit-line connected to it discharges. We want the input node of inverter 1 to remain below the switching point of the loop. This could be accomplished with sizing the NMOS of the inverter loop larger than the NMOS pass transistors. Also the body effect helps in keeping the inverter loop node close to zero volts and stops it from rising

beyond the switch point even when the NMOS pass transistor and NMOS in inverter loop are sized same. This is because the rising node is also the source of the pass transistor connected to it. This raises the threshold of the pass transistor and reduces the current with rising voltage. This increases the on resistance of the pass transistor and limits the rise of the node voltage. The equation governing the body effect in MOSFETS is:

$$V_t = V_{t0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \tag{2.1}$$

where γ is the body-effect coefficient, V_{t0} is the threshold at $V_{SB} = 0$, V_{SB} is the source-body voltage, and ϕ_F is the Fermi Potential.

The simulation results in the National's 0.18 CMOS process for the node voltages that appear at the output of inverter 1 of the inverter loop in Fig. 2-9 when connected to different supply voltages for the minimum sized transistors in a bit-cell are shown in Table 2.1. All NMOS and PMOS are of length 0.18um and width 0.28um.

Table 2.1: Bit-cell node voltage when connected to bit-line for different supply voltages while reading

Supply Voltage (mV)	Switch point (mV)	Inv Node Voltage (mV)
200	100	26.0
300	150	30.3
400	200	37.6
500	250	50.0
600	300	66.5

2.5.3 Robustness

In addition to being able to write and read back the data, it is important to give consideration to the presence of unwanted voltages induced in an inverter loop due

to coupling with adjacent circuits in any implementation of design. This induced voltage can corrupt the stored data by switching the state of the bit-cell.

Noise margin gives us an approximate quantification of the robustness of a bit-cell. One of the many definitions is the side of the largest square that can be fit in the inverter loop DC curve [9]. A larger square implies a higher voltage margin for the stored state voltage to drift off its equilibrium point before the coupling could cause an irreversible data loss.

Static noise margin

Static noise margin is when the pass transistors are off and bit-cell forms an inverter loop. This gives us the butterfly curve as shown in Fig. 2-14.

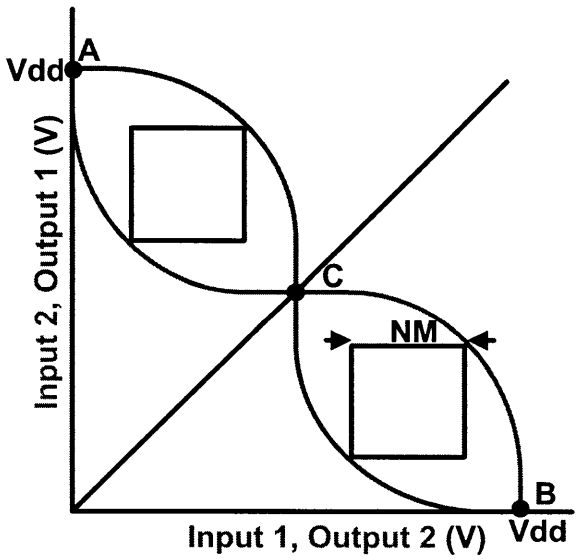

Figure 2-14: Depiction of static noise margin on the "butterfly curve"

Table 2.2 contains simulation results for the static noise margins for different process corners for supply voltages of 300 and 600 mV in the National's 0.18 CMOS process. All NMOS and PMOS are of length 0.18 um and width 0.28 um.

Table 2.2: Static noise margin for different process corners and supply voltages

Process corner	Noise margin for Vdd=300 mV	Noise margin for Vdd=600 mV
Typical	110.33	251.77
SF	77.09	225.60
FS	85.57	214.99
FF	106.79	233.38
SS	106.08	251.77

Read noise margin

The read noise margin is less than the static noise margin. Graphically this is due to the voltage at the inverter loop storing a 0 being pulled up slightly and the solution becomes the new intersection point. This is shown in Fig. 2-15. This reduces the side of the square that can fit between the curves and therefore means lower noise margins than the static noise margins. For example at point A in Fig. 2-15 input 1 is slightly above ground.

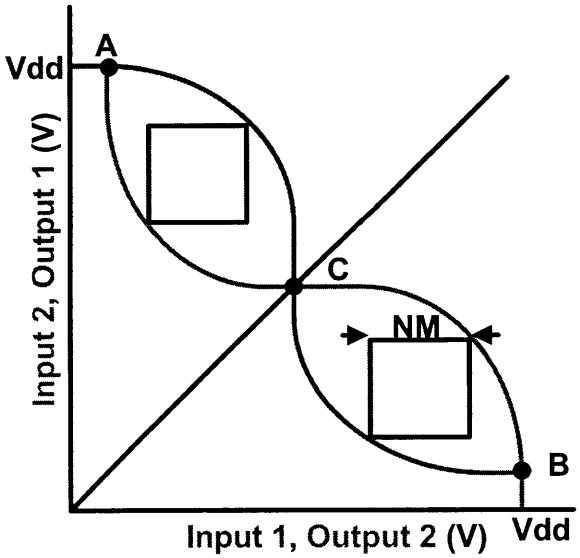

Figure 2-15: Depiction of read noise margin on the "butterfly curve"

Table 2.3 contains the simulation results of the read noise margins for different

process corners for supply voltages of 300 and 600 mV. All NMOS and PMOS are of length 0.18um and width 0.28um.

Table 2.3: Read noise margin for different process corners and supply voltages

Process corner	Noise margin for Vdd=300 mV	Noise margin for Vdd=600 mV
Typical	52.55	111.46
SF	69.73	151.34
FS	22.21	80.62
FF	44.84	95.47
SS	63.56	130.13

2.6 Peripherals

There are three peripheral blocks around the memory matrix that assist in read and write operation. The three blocks are the address generator and pre-decoder block, register block, and row decoder block. Their schematics are shown in the following subsections.

2.6.1 Address generator and pre-decoder block

Fig. 2-16 is the 15 bit sequential address generating Counter with pre-decoder. The pre-decoder shifts part of the burden of row and column decoding away from along side of each row and column of the memory matrix to the memory's corner. This enables a smaller memory matrix pitch [6].

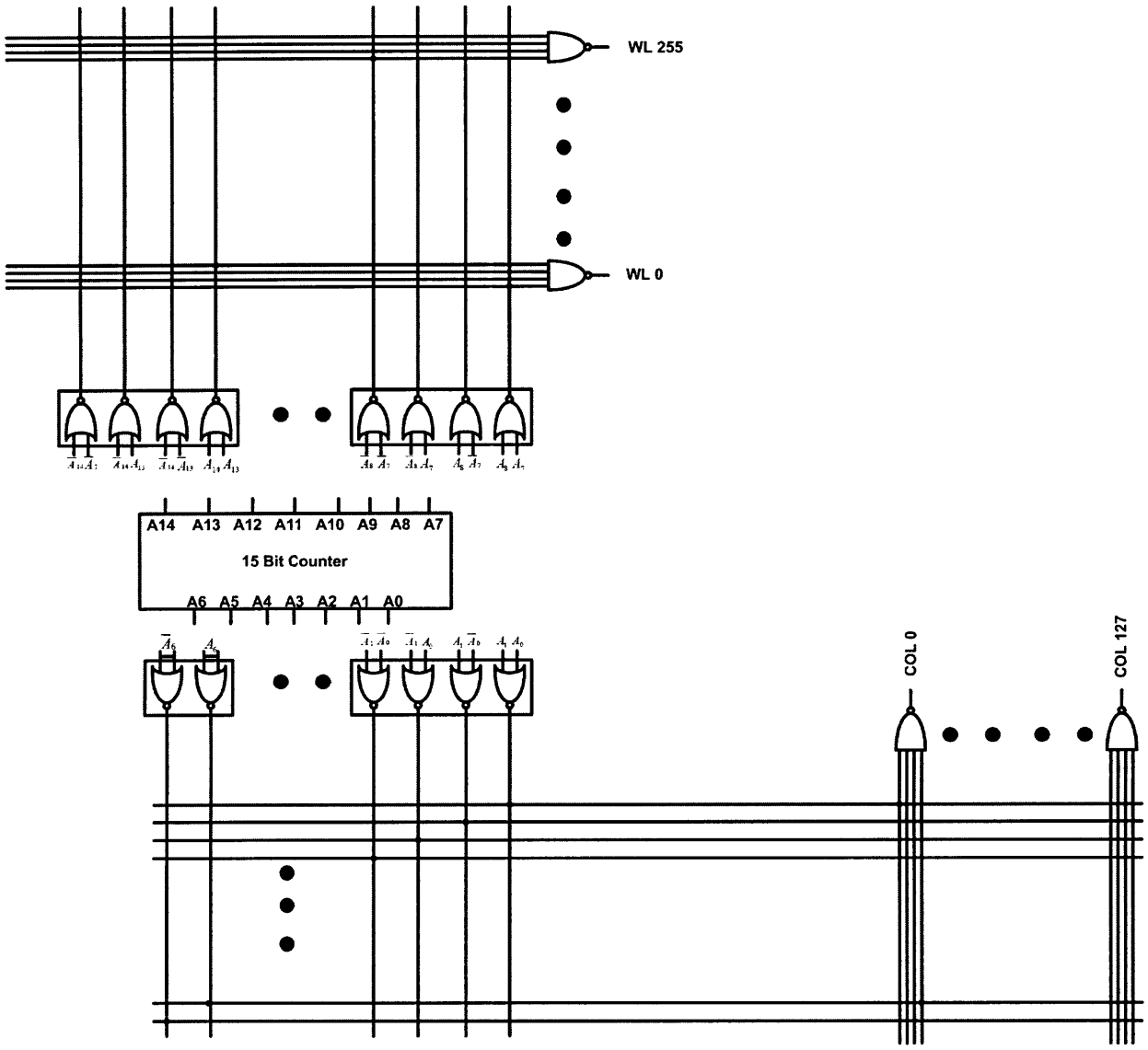

Figure 2-16: Schematic of the sequential address generator and pre-decoder

2.6.2 Register block

Fig. 2-17 shows the schematic of the block along the bottom periphery of the memory matrix. This contains registers and logic circuitry to decode the register address and to enable read and write operations.

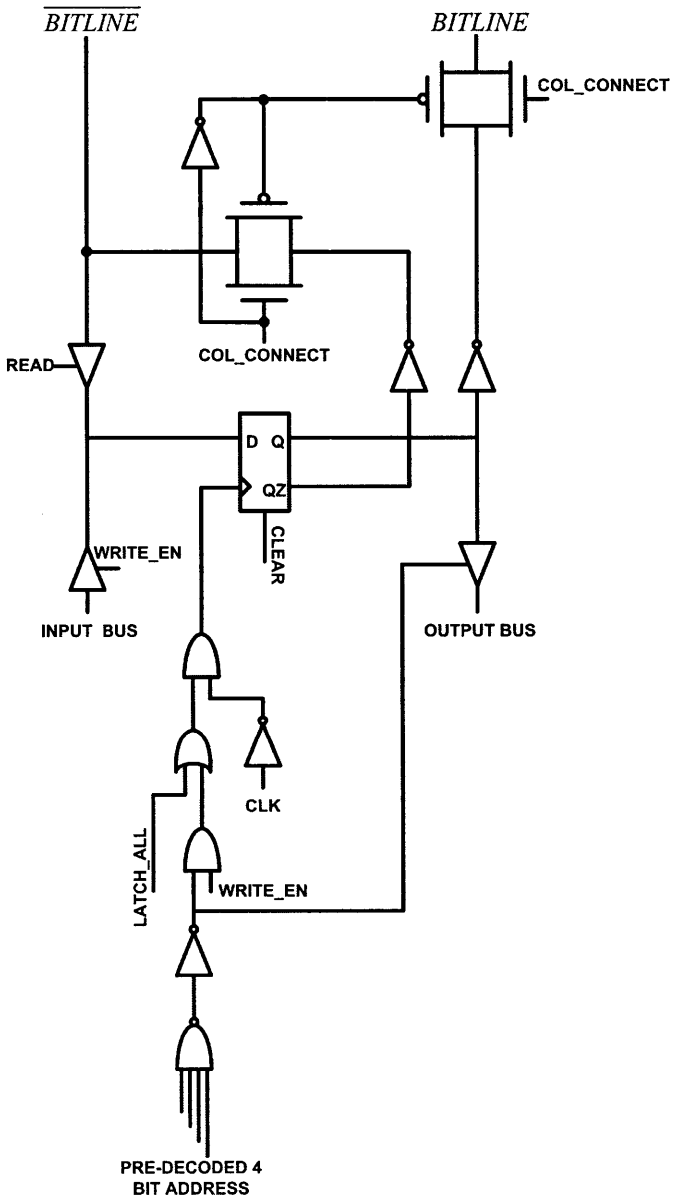

Figure 2-17: Schematic of a register block at the bottom of the memory matrix

2.6.3 Row decoder and power management switch block

Fig. 2-18 shows the schematic of the block that decodes the memory matrix row address and logic circuitry to enable read and write operations. This block also has power management switch (Fig. 2-19) that essentially has a bit of storage which is set when the memory row is accessed for write for the first time. This bit then keeps the row powered on for data retention. Before this first write the row stays turned off to reduce leakage currents.

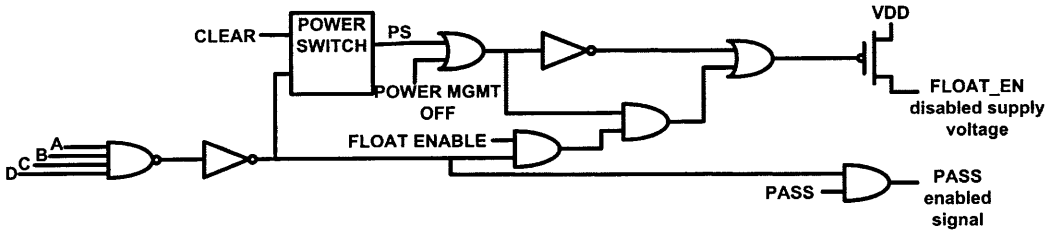

Figure 2-18: Schematic of the row decoder and power management switch for each row of memory matrix

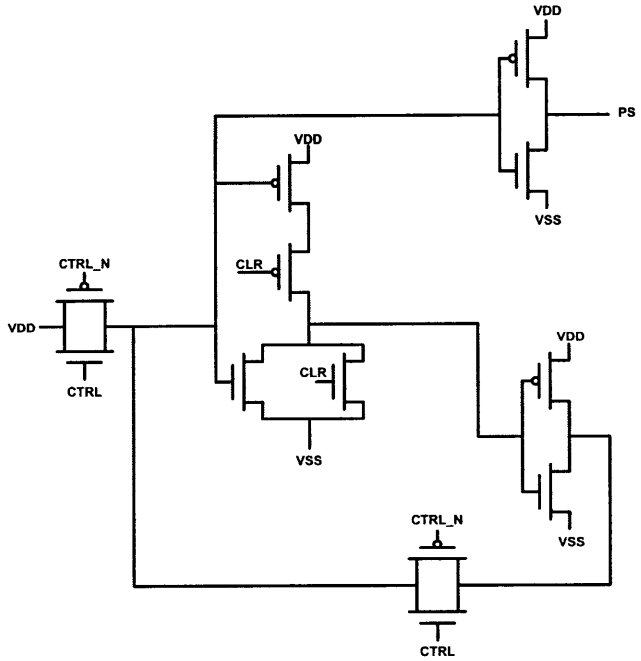

Figure 2-19: Schematic of the power switch for each row of memory matrix

The following section documents the signal descriptions and their timing sequence

that enables write and read operation, details on the bit-cell design, and peripheral circuitry that went into this memory.

2.7 Signals and their definitions

The following tables document the signals along with their definitions and timing sequence for the write and read operation to memory.

Input/ Output	
INPUT [7:0]	8 bit input bus. It is connected to the register inputs when WRITE_EN is high.
OUTPUT [7:0]	8 bit output bus. It is connected to the register outputs when READ is high.

Global signals	
CLK	Increments the counter/ address at the positive edge of CLK.
POWER_CLK	Switches the voltage regulator.
CLEAR	Clears the registers to zero and resets the counter to zero.
POWER_MGMT_OFF	When low this signal is de-activated and power management is on and only memory rows written are powered by supply for data retention.

Signals to write the registers with the values on the input bus	
WRITE_EN	Enables write operation by connecting the input bus to the register inputs and enabling the register to register values on the bus.
CLK	Registers latch the value on the input bus at the negative edge of the CLK signal.

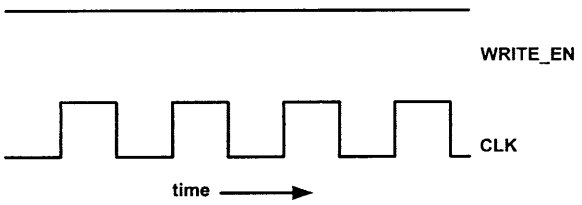

Figure 2-20: Timing diagram for signals to write the registers with the values on the input bus

Signals to write to a row of memory matrix with the values in the registers	
COL_CONNECT	Connects the register outputs to their bit-lines
PASS	Turns on the access transistors connecting the bit-lines to the inverter loop nodes.
FLOAT_EN	Disconnects supply to bit-cells in the selected memory row to be written.

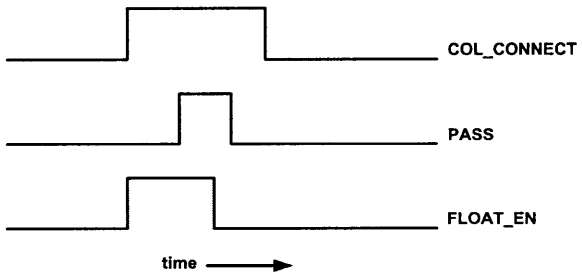

Figure 2-21: Timing diagram for signals to write to a row of memory matrix with the values in the registers

Signals to read a row of memory matrix into the registers	
PRE_CHARGE	Pre-charges the bit lines to a 1.
PASS	Turns on the access transistors connecting the bit-lines to the inverter loop nodes.
CLK	Registers register the value on the bit-lines at the negative edge of the CLK signal.
LATCH_ALL	Enables all registers to simultaneously latch a full memory row into the registers at the negative edge of a CLK.
READ	Enables read operation by connecting the bit-lines to the register inputs

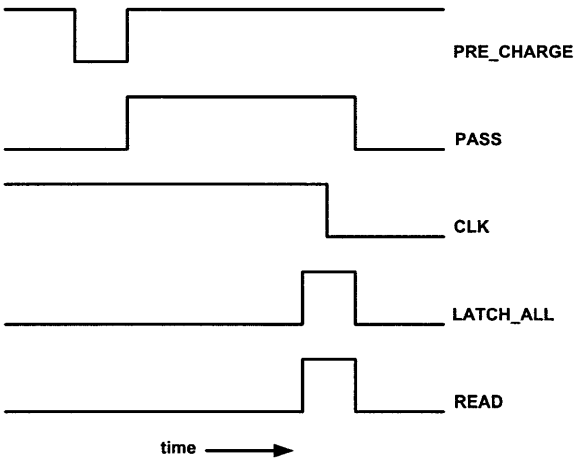

Figure 2-22: Timing diagram for signals to read a row of memory matrix into the registers

2.8 Summary

In this design I have chosen to use minimum-sized devices to reduce the leakage currents. But like any design it is a trade off. Minimum-sized devices reduce the bit-cell noise margins and make them more prone to loss of stored data and therefore increase in bit-error rate.

Chapter 3

Voltage Regulator

Long term monitoring using micro-implants can only be achieved with low power consuming devices both during active and standby modes. Due to their large number of transistors, memories are the dominant power consumer in microimplants during the standby mode. Due to the dependence of the leakage currents (currents flowing in a transistor with zero gate-source voltage) on the supply voltage, it is of paramount important to reduce the supply voltage to the minimum required for operation and retention of the stored data. Since in our application, the ultracapacitor voltage is considerably higher in between 2.4 and 1.2 V and SRAM can operate and retain data at very low voltages [6], it is desirable to have a voltage regulator to step down the voltage for low power consumption.

The SRAM memory spends time in either of the two states: Standby mode, when the memory cells are not accessed, and active mode, when the memory is written to or read from. In active mode, while writing, the transistors switch and there are energy losses proportional to the switching frequency times CV^2 where C is the capacitance as seen at the node storing a bit value. In standby mode the transistors are off and are tasked with only maintaining of the stored data. There is no direct path between the power supply and ground. Ideally we should have zero losses while in standby mode if the transistors were ideal. However in reality we have what are called leakage currents that leak current to the ground with a zero voltage difference across the gate and source of a transistor. The memory wastes less energy in both standby and active

modes when powered with a low voltage supply. Let us look at the leakage currents for the particular process used in this design.

Leakage current is a strong function of the drain-source voltage. High supply voltage puts high Vds on an off transistor thereby increasing the leakage current. The ultracapacitor voltage for the micro-implants is expected to swing from a high 2.4 V to a 1.2 V and back to 2.4 V. Figs. 3-1 and 3-2 for NMOS and PMOS respectively show that the leakage current increase with Vds. A low supply voltage below 0.6 V gives us about an order of magnitude lower leakage currents compared to at high voltages of 2.4 V.

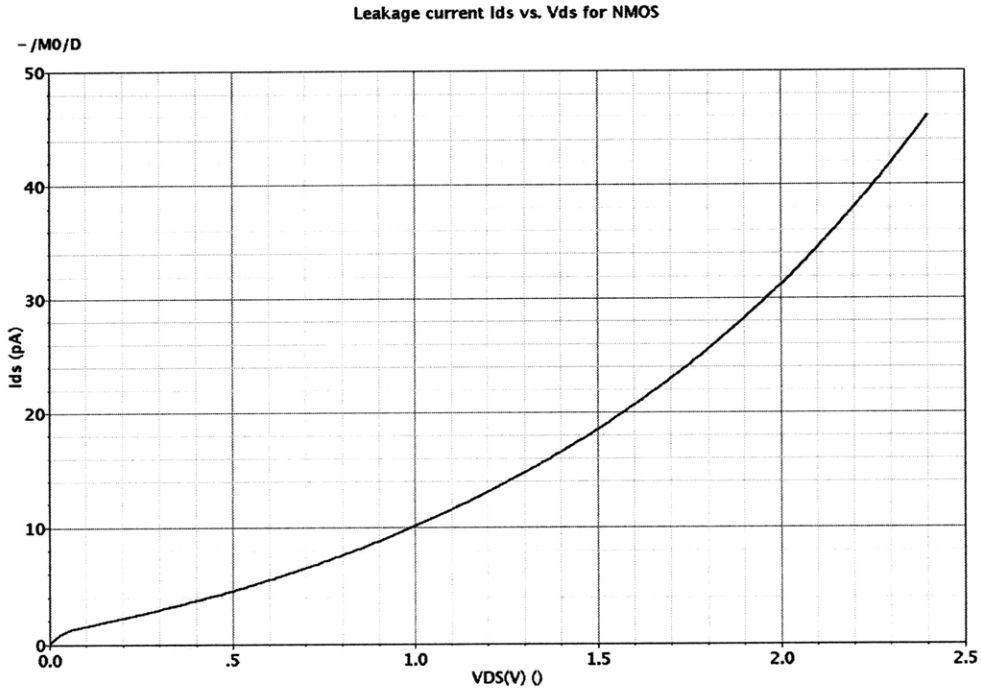

Figure 3-1: Simulation of leakage current versus Vds for NMOS transistor

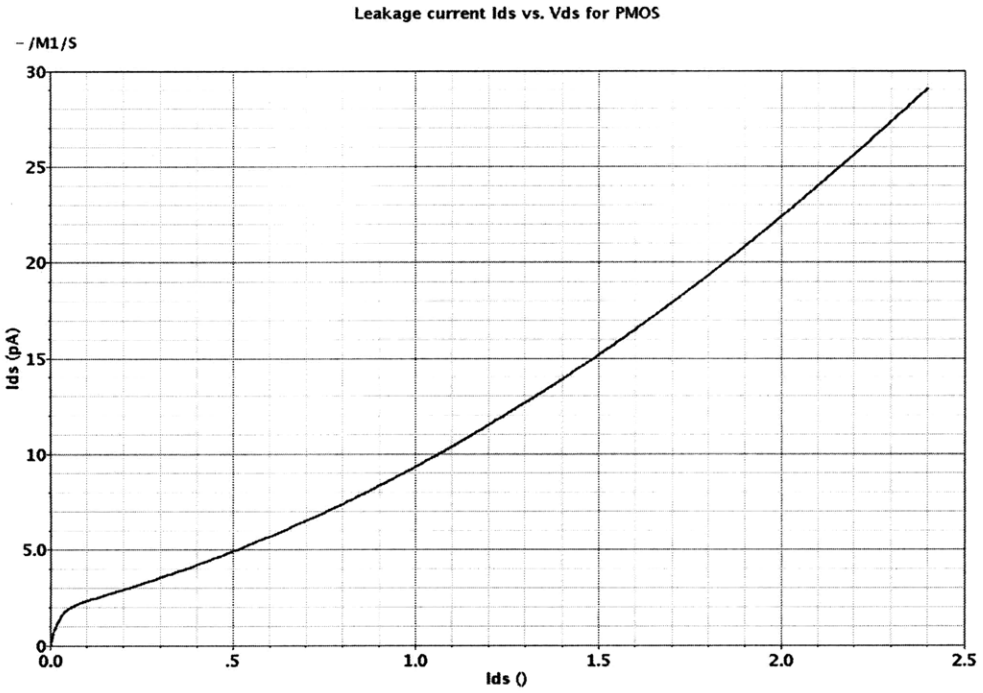

Figure 3-2: Simulation of leakage current versus Vds for PMOS transistor

3.1 Voltage Regulators

There are many ways to lower the voltage supply. These methods employ a capacitor and inductor and are called DC-DC buck converters [5]. These essentially alternate between grabbing energy from the source by storing it as magnetic energy in an inductor and with this stored energy re-charging a big capacitor supplying the load. The inductor integrates voltage and stores it as magnetic energy and a capacitor integrates the current supplied by the inductor and converts it into voltage. The voltage level can be adjusted by adjusting the duty cycle. Since only reactive components are employed, the conversion is efficient. However, due to non-availability of large inductors on chip, we will focus on techniques employing only capacitors.

Another common method for generating a lower voltage uses a diode [8]. This is shown in Fig. 3-3. Due to an exponential dependence of a diode current on a voltage across it, an on diode maintains an approximately constant voltage across it. However this comes with high quiescent currents that wastes a lot of energy. For example typically for a diode with scale current (Is) = 10E-12, that depends on the junction area, and n = 1 and turn on voltage = 0.7 V approximately 12 uA is wasted as quiescent current.

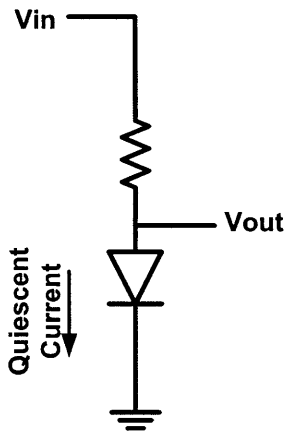

Figure 3-3: Voltage regulator using diode

3.2 Proposed methodology

The following proposal is an open-loop voltage regulator. Without feedback, as in a closed loop system, there is no need for a reference and the system is simple in design. Since on-chip capacitors can easily be fabricated, the following solution depicted in Fig. 3-4 is proposed to step down high ultra-capacitor voltage.

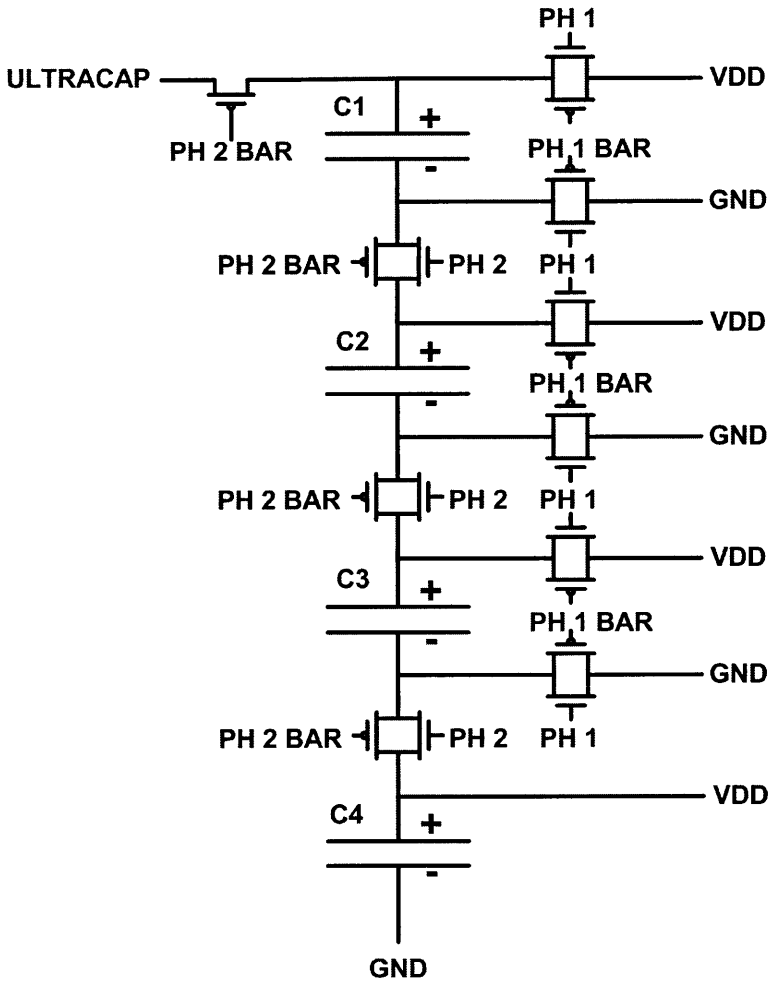

Figure 3-4: Voltage regulator schematic

This technique employs four capacitors stacked in series while charging from a high voltage ultra-capacitor source and then switched to a parallel configuration. While connected in series the top most capacitor C1 is connected directly to the Ultracap power supply. The bottom-most capacitor C4 is connected to the memory Vdd rail supplying power to the memory at all times. The PH1 and PH2 are the two phases of the clock signal, POWERCLK, that alternately turn high. The PH1 and PH1 BAR turn on the switches connected to them when the PH1 and PH1 BAR voltage levels go high and low respectively. Similarly PH2 and PH2 BAR turn on the switches connected to them when PH2 and PH2 BAR voltage levels go high and low respectively. When PH2 is high, the four capacitors C1 to C4 are stacked in series configuration as shown in the figure 3-5. When the PH1 goes high, the four capacitors are connected in the parallel configuration as shown in the figure 3-6. This technique gives us a voltage that is close to 1/4 the ultra-capacitor voltage without much swing if the switching rate is fast enough that the voltage drop between switching instants is negligible.

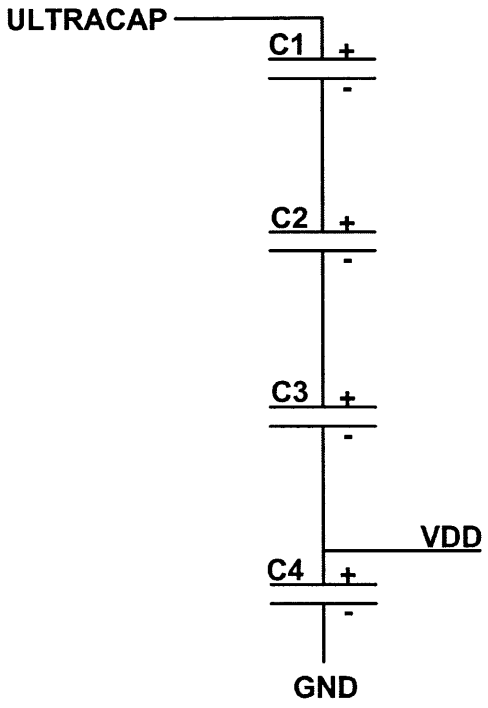

Figure 3-5: Voltage regulator in series configuration

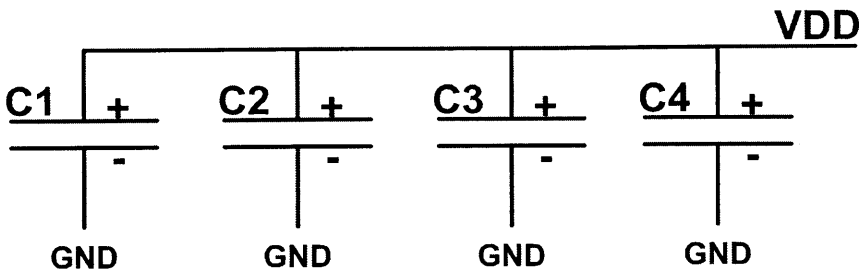

Figure 3-6: Voltage regulator in parallel configuration

3.3 Model

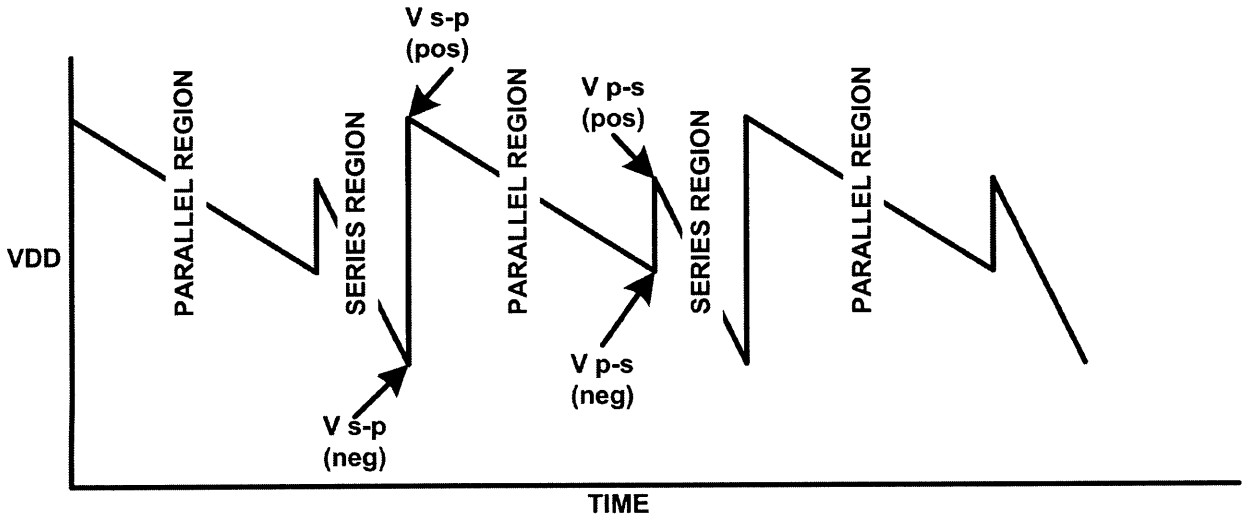

Figure 3-7: Voltage curve sketch on the regulator output, assuming the load is drawing a constant current

The derivation of a mathematical model for the voltage regulator for a steady state voltage level at the memory's Vdd rail is as follows. This derivation refers to the Fig. 3-7. Let us assume a constant current of I drawn by the memory from the node located between positive plate of C4 and negative plate of C3. Throughout this derivation, I will refer to the two transition points as parallel-to-series and series-to-parallel, and the two state configurations as series and parallel in this cyclic process of voltage conversion. It is assumed that $C_1 = C_2 = C_3 = C$ for simplicity and that

C_4 is different from C. The different value for C_4 is reasonable because C_4 is attached to the Vdd node and will be in parallel with the memory power rail capacitance anyways, making it different from C.

3.3.1 Series Configuration

When the capacitors are in the series configuration, the node between positive plate of C4 and negative plate of C3 supplies current to the memory. In the series configuration, the assumed constant leakage current I drops the voltage Vdd with a slope $S_1 = \frac{I}{C_4 + \frac{C}{3}}[V/s]$ as the current drawn by the memory sees $\frac{C}{3}$ in parallel with C_4.

During series configuration, the charge drawn from the node between the positive plate of C4 and the negative plate of C3 is:

$$Q_{out,series} = TID \tag{3.1}$$

where T is the period of switching clock signal and D is the duty or fraction of T that the system is in the series configuration.

The charge drawn from the capacitor C4 during this series configuration is:

$$Q_{out,C4,series} = \frac{C_4 Q_{out,series}}{C_4 + \frac{C}{3}} \tag{3.2}$$

The charge drawn from the ultra-capacitor during this series configuration is:

$$Q_{in,supply,series} = \frac{\frac{C}{3} Q_{out,series}}{C_4 + \frac{C}{3}} \tag{3.3}$$

3.3.2 Series to Parallel Transition

There is no charge drawn from the ultra-capacitor supply during the series-to-parallel transition as the switches disconnect the series configuration first and then the switches connecting the capacitors in parallel turn on. The charge on each capacitor in series just before this transition is redistributed on the capacitors after the transition from

series to the parallel configuration.

3.3.3 Parallel Configuration

In the parallel configuration, the assumed constant leakage current I[A] drops the voltage Vdd with a slope $S_2 = \frac{I}{3C+C_4}[V/s]$

During parallel configuration, the charge drawn by the memory is:

$$Q_{out,parallel} = TI(1 - D) \tag{3.4}$$

where (1-D) is the duty or fraction of T that the system is in the parallel configuration.

3.3.4 Parallel to Series Transition

Just before the transition from parallel to series configuration, the charge on each capacitor in parallel is determined by their common voltage $V_{(p-s)-}$ just before the transition.

The charge on each of the capacitors C1=C2=C3=C before step from parallel to series configuration is:

$$Q_{C,(p-s)-} = CV_{(p-s)-} \tag{3.5}$$

The charge on C4 before the transition from parallel to series is:

$$Q_{C4,(p-s)-} = C_4V_{(p-s)-} \tag{3.6}$$

After the transition from parallel to series configuration, the total voltage across the series connected capacitors C1,C2,C3,and C4 is instantly equalized to the ultra-capacitor voltage. The charge drawn from the ultra-capacitor is determined by the difference between the voltage on the ultra-capacitor and four times the common voltage on the capacitors in the parallel configuration just before the transition.

The charge input from the ultra-capacitor right after the transition from parallel to series is:

$$Q_{in,supply,p-s} = C_{series,1234}(V_{ultracap} - 4V_{(p-s)^-}) \tag{3.7}$$

3.3.5 Steady State Requirement

Under steady state conditions, after cycling through the two configurations, we should have the same voltage. In the following equations, D is the duty cycle of the process in the series configuration and T is the period of the switching clock.

The voltage just before the transition from parallel to series configuration is equal to the voltage due to the total charge on capacitors in parallel just after entering parallel configuration less the voltage fall due to the charge drawn from the parallel capacitors by the memory while in parallel configuration. This is described by the following equation.

$$V_{(p-s)^-} = \frac{Q_{total,parallel,(s-p)^+}}{3C + C_4} - T(1-D)S_2 \tag{3.8}$$

The total charge on entering in the parallel configuration in the above equation can be written in terms of the voltage just before the transition from parallel to series configuration. It is equal to the sum of the three terms enclosed in square brackets below. The first square bracket is the the charge on each of the capacitors C1,C2, and C3 just before the transition from parallel to series plus the charge intake from the ultra-capacitor during series configuration. There is a factor of three to account for the three equal capacitors. The second square bracket is the charge on the capacitor C4 just before the transition from parallel to series configuration less the charge drawn from it during the series configuration. The last square bracket is the charge intake from the ultra-capacitor during the transition from parallel to the series configuration. It has a factor of 4 to account for the four capacitors in series.

The following equations describes it in a simple form.

$$Q_{total,parallel,(s-p)^+} = 3\left[CV_{(p-s)^-} + Q_{in,supply,series}\right] + \left[C_4 V_{(p-s)^-} - Q_{out,C4,series}\right] + [4Q_{in,supply,p-s}] \tag{3.9}$$

Substituting equations 3.3, 3.2, and 3.7 in equation 3.9 and then substituting it into the equation 3.8 and then solving for $V_{(p-s)^-}$ we get:

$$V_{(p-s)^-} = \frac{V_{ultracap}}{4} + \frac{ITD}{16C_{series,1234}}\left[1 - \frac{C_4 - C}{C_4 + \frac{C}{3}}\right] - \frac{IT}{16C_{series,1234}} \tag{3.10}$$

There are four voltages at the transition points of the curve which ideally we would like them to be equal or close. They are the voltages just before and after the parallel to series transition, and just before and after the series to parallel transition. Final equations for these four voltages are:

$$V_{(p-s)^-} = V_{(p-s)^-} \tag{3.11}$$

$$V_{(p-s)^+} = V_{(p-s)^-} + \frac{(V_{ultracap} - 4V_{(p-s)-})(\frac{C}{3})}{\frac{C}{3} + C_4} \tag{3.12}$$

$$V_{(s-p)^-} = V_{(p-s)^+} - \frac{Q_{out,C4,series}}{C_4} = V_{(p-s)^+} - \frac{TID}{C_4 + \frac{C}{3}} \tag{3.13}$$

$$V_{(s-p)^+} = V_{(p-s)^+} + \frac{TI(1-D)}{3C + C_4} \tag{3.14}$$

These equations give us direction in terms of how to pick capacitors C1-C4. In our case, the objective is to get a division by four while minimizing the amount of supply ripple. This objective can be met by choosing $C_4 \approx C$ and $C >> IT$. By doing so we get:

$$V_{(p-s)^-} = \frac{V_{ultracap}}{4} \tag{3.15}$$

and

$$V_{(p-s)^+} \approx V_{(s-p)^-} \approx V_{(s-p)^+} \approx V_{(p-s)^-} \tag{3.16}$$

This is a desired result since it implies little voltage level fluctuation.

3.3.6 Matlab and Cadence simulation results

Following is the plot generated using the the mathematical model of the voltage regulator described by the above equations with the parameters $I = 1uA, T = 1\text{us}, D = 0.5, C1 = C2 = C3 = 50\text{pF}$, and $C4 = 150\text{pF}$.

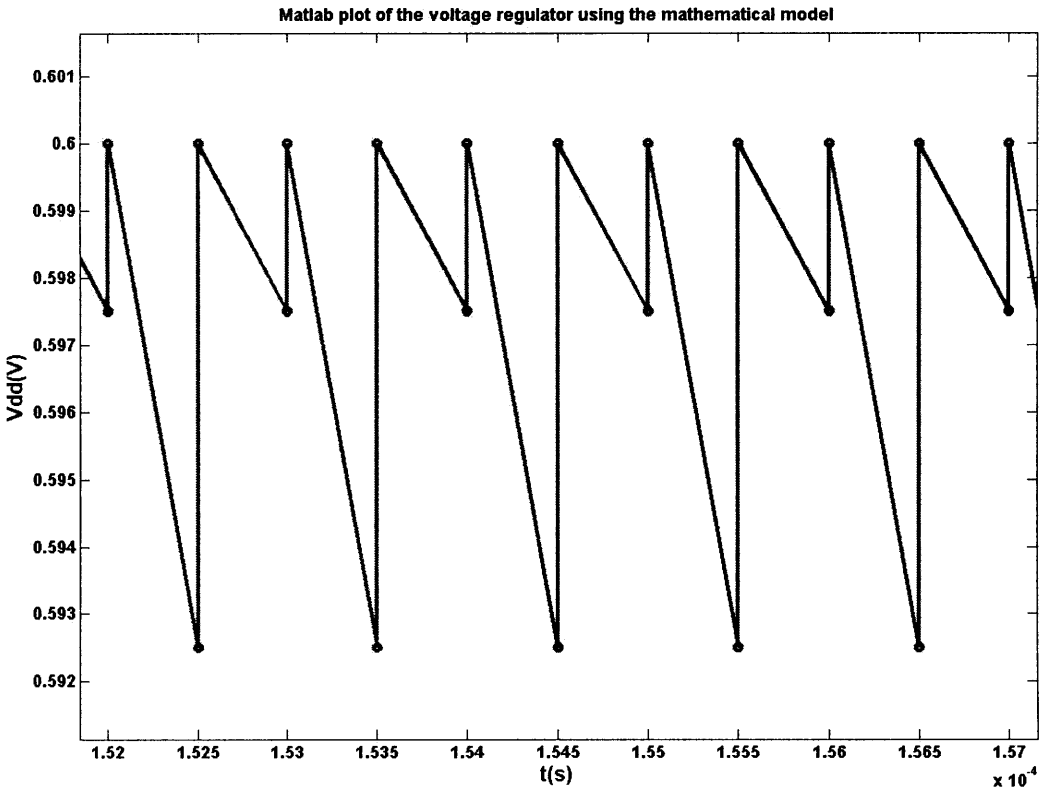

Figure 3-8: Matlab plot of the mathematical model of the voltage regulator

Using the same choice of parameters following is the simulation in Cadence using ideal switches and capacitances.

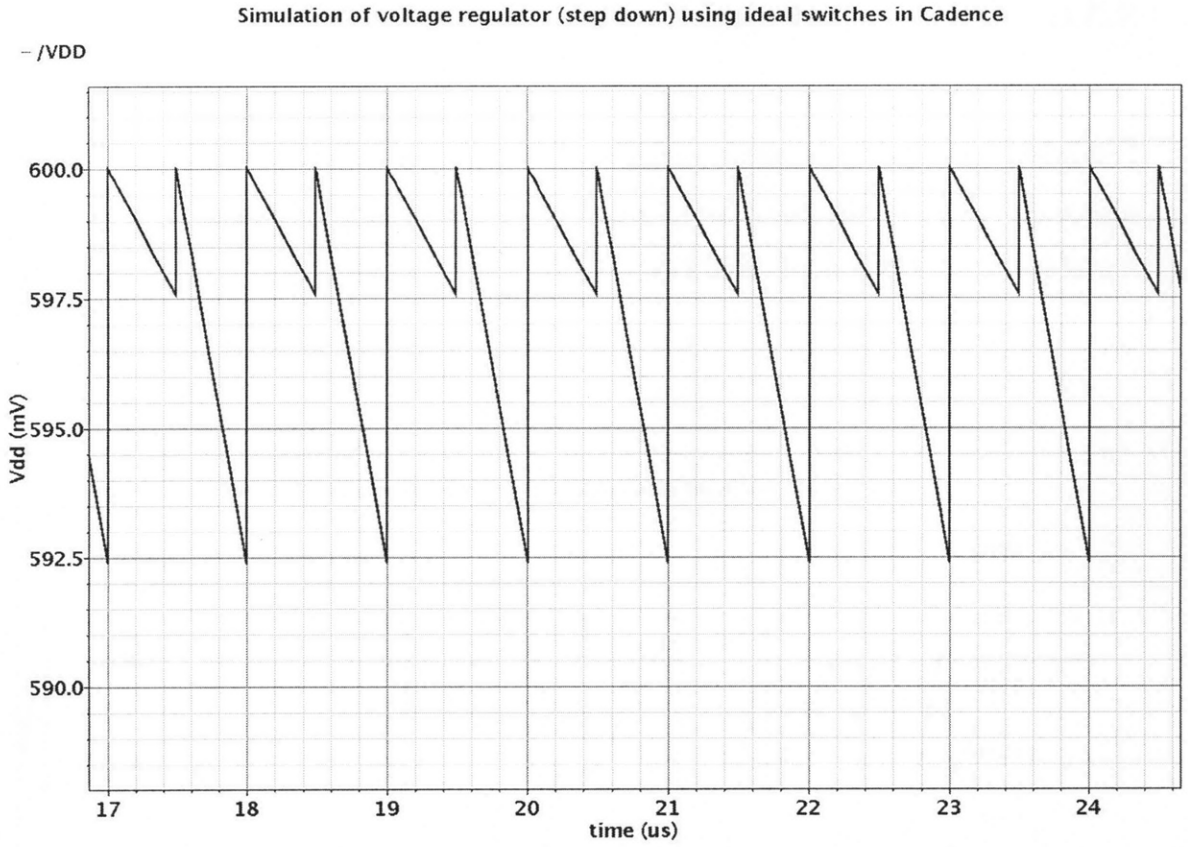

Figure 3-9: Simulation of voltage regulator using ideal switches in Cadence

3.3.7 Conclusion

The mathematical model as plotted in Matlab gives an exact replica of the waveform generated using ideal capacitances and switches in Cadence.

The leakage current is expected to be around 0.6 uA. Therefore if T is of order 1us and I is of order of 1uA and C larger than an order of 1pF, we get a very low voltage fluctuation around $V_{ultracap}/4$. This should give us a near constant stepped down voltage with slight variations.

Chapter 4

RF Communication Link

4.1 Introduction

A low power medical implant cannot power a conventional power amplifier for long-operating durations to transmit data over a radio link. On the contrary implants need power to recharge its small local power source.

RFID wireless technology has been around for a long time [4]. It consists of a passive tag and an active reader. RFID has been used mainly for tagging goods and animals for easy identification. In this project, we propose to use the same technology and integrate the tag to our system. Instead of sending fixed identification bits as in a conventional RFID system, we will send the data collected from the patient over the wireless link to the reader. To employ this technology in an optimum way for our micro-implant application, we need to have a model of this technology for analysis. Since our application requires the system to have a small form size, we would like to know what we trade-off this desired feature with.

4.2 RFID Link Theory

In near field, the basics of an RFID system can be understood using the transformer theory. The primary of this transformer-like system consists of the reader's coil that couples with the secondary side consisting of the tag's coil. As in a transformer, the

primary side is driven by a sinusoidal voltage source that couples to the tag's coil. This is illustrated in Fig. 4-1. Ignore tuning capacitors until two paragraphs later.

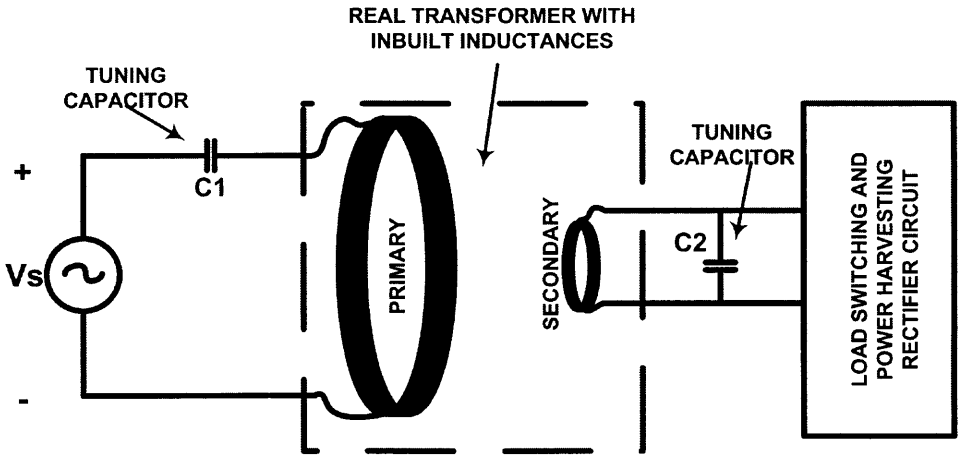

Figure 4-1: RFID basic transformer-like model

The field created couples the primary and secondary coils. The voltage induced on the secondary can be rectified to obtain DC voltage to drive the tag load or recharge a battery. Besides transfer of power from the primary to the secondary side, this link can be used to transmit data between the two sides. The data is transmitted from the secondary to the primary through load change on the secondary as shown in the box to the right of Fig. 4-1. The secondary coil can be shorted or connected to a load for instance. For the two different loads two different voltage amplitudes are detected on the primary. This corresponds to the binary states if an on-off modulation scheme is employed for data communication. Other more sophisticated modulation schemes such as Manchester modulation can also be used. This amplitude change is detected as a change in the amplitude of the sinusoidal voltage across the primary coil. The amplitude level is detected using a peak detector that discards the carrier frequency waveform.

The control or configuration signals can also be transmitted from the primary to the secondary side by turning off and on the field. Again these two states can be interpreted by the secondary as the two bit states. To avoid confusion between the actual data transfers and devices being out of range, a preamble is often sent before

the actual data transmission.

The rectifier on the secondary side requires high voltage to function. This requires high coupling fields. The coupling fields can be increased by increasing the current in the coils. Since the coupling coils come with inductances, they need to be tuned out using capacitors to generate high currents as shown in Fig. 4-1. This resonant circuit generate high currents that in turn induce high voltages on the secondary for a loosely coupled system, that is with a small coupling coefficient k. Loosely coupled systems make this first order introduction easier as we need not worry about the feedback in this case. To generate still higher voltages on the secondary, we connect a capacitor to the secondary coil to create resonance and take the voltage to the rectifier across the capacitor.

In a transformer, the currents in the primary and secondary coil contribute to the flux through each of the coils. The contributions to flux in primary due to the current in the primary is characterized by the inductance L1 and due to current in secondary is characterized by the mutual inductance Lm. Similarly the contributions to flux in the secondary due to the current in the secondary is characterized by the inductance L2 and due to the current in the primary is characterized by the same mutual inductance Lm. Let us model this simple RFID link using the transformer coupling equations as below where the lambdas are the flux linked to subscripted coil number.

$$\begin{pmatrix} \lambda_1 \\ \lambda_2 \end{pmatrix} = \begin{pmatrix} L_1 & L_m \\ L_m & L_2 \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}$$

Using Faraday's law differentiate the above equations to get the voltage across ideal transformer and add to it the voltage drop due to the resistance associated with the real coil windings to get voltages V1 and V2 across the primary and secondary coils of a real transformer.

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} L_1 & L_m \\ L_m & L_2 \end{pmatrix} \begin{pmatrix} \frac{d}{dt} i_1 \\ \frac{d}{dt} i_2 \end{pmatrix} + \begin{pmatrix} r1 & 0 \\ 0 & r2 \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}$$

Add to this model the capacitances on the primary and secondary side to create the resonances as shown in Fig. 4-2.

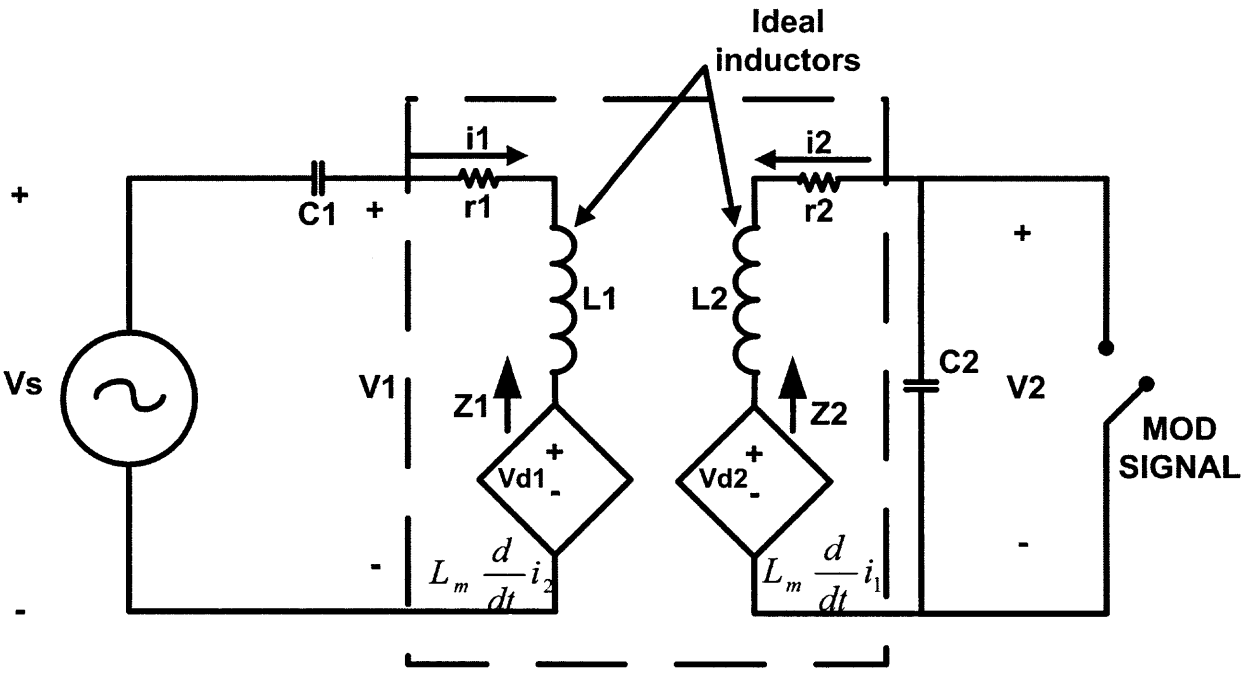

Figure 4-2: RFID model

Vs is a sinusoidal voltage source with the period the same as the desired period of the carrier wave. The MOD signal controls whether the switch is closed or open. When the switch is open, the secondary is a resonator with impedance Z2 comprising of L2, R2 and C2 in series as seen by the dependent voltage source at the secondary. When the switch is closed, C2 is shorted out and Z2 is simply L2 in series with R2 as seen by the dependent source. The dependent source at the primary sees Z1 comprising of L1, R1, and C1 in series under both switch conditions.

For a fixed carrier frequency that is also the resonant frequency, we are interested in seeing the impact of the design variables, inductances L1 and L2, and the coupling coefficient $k = L_m\sqrt{L_1 L_2}$ in this RFID system on the performance of data transfer rates and amplitude difference at the primary side for the two switch conditions. Due to load modulation, this circuit is linear and not time-invariant. This system is a different linear circuit for each switch state. We can do the linear analysis

in between the load switching. We can take a unilateral laplace transform on the circuit differential equations with the initial conditions due to the energy stored in the resonators just before the switch of load happens. But instead, since all we are interested in is the envelope of the waveform at the output, we will concentrate on the parameters that affect the magnitude of the waveform and how fast they decay or rise each time we switch loads.

The response of a sinusoidal input Vs into a linear circuit (in between switching) consists of the transient response and steady state response. The transient response consists of that due to the initial conditions that prevailed just before the switch of load happened and that due to the input adjusting the circuit to the new steady state. After the transients are gone, steady state prevails until next switch of load. The transients decay exponentially as determined by the characteristic equation of the circuit with the new load after the switch happened. To determine the characteristic equation and the poles, we can instead take the bi-directional laplace transform without the initial conditions for both switch conditions.

I have used the feedback technique in [1] on power optimization. While the paper talks about power optimization, here is a model and analysis suitable for data transmission. The following is the signal block diagram of the RFID system with output on the primary side across the primary winding. The mapping from the RFID model in Fig. 4-2 to the signal block diagram in Fig. 4-3 is as follows. There are three voltage sources in the model, one is independent voltage source Vs and two are current-dependent-voltage sources Vd1 and Vd2 on the primary and secondary side respectively as shown in Fig. 4-2. The difference between Vs and Vd1 on the primary side shows up across the impedance Z1 and generates the current i1. This current times a factor of sM causes a voltage Vd2 to develop across the load Z2 on the secondary side. This causes the current i2 to flow in the secondary side. The signal is labeled with a negative sign in the signal block diagram is the physical current generated by the dependent source is in the negative direction of i2 as shown in Fig. 4-2. This signal -i2 is multiplied with a -1 to convert it to i2 and sM to give us the dependent source voltage Vd1 on the primary side to complete the loop in the

signal block diagram. The current in the primary side i1 is multiplied with $1/sC1$ and subtracted from Vs to give V1.

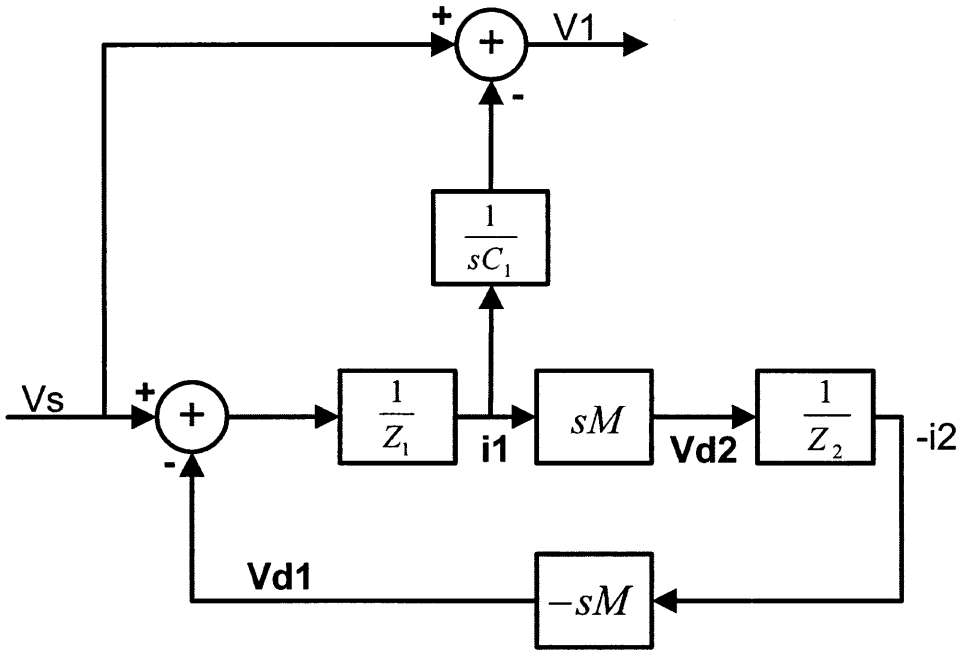

Figure 4-3: RFID Feedback signal diagram

To compare the amplitudes and find poles of the system it will be useful to write a generic expression for the transfer function and loop gain and then make it specific by plugging in the impedance on the secondary side that is different for each switch condition. Transfer function from the source voltage Vs to the V1 is:

$$\frac{V_1}{V_s} = 1 - \frac{1}{sC_1}\frac{1}{Z_1}\frac{1}{1 - L(s)} \tag{4.1}$$

L(s) in the above equation is the loop gain which works out to:

$$L(s) = \frac{s^2M^2}{Z_1(s)Z_2(s)} \tag{4.2}$$

It will be useful to have an expression for Z1 and Z2 and plug them later into Eq. 4.2 in later sections for the two switch conditions. Z_1 and Z_2 are impedances of the resonators alone on the source side and load side respectively as seen by the

dependent sources and can be written by inspecting Fig. 4-2 as:

$$Z_1(s) = sL_1 + R_1 + \frac{1}{sC_1} = \frac{L_1}{s}\left[s^2 + \frac{sR_1}{L_1} + \frac{1}{L_1C_1}\right] \tag{4.3}$$

$$Z_2(s) = sL_2 + R_2 + \frac{R_{load}}{sR_{load}C_2 + 1} \tag{4.4}$$

4.2.1 Switch is open

When the switch is open, R_{load} is infinite and we get for the loop transmission:

$$L(s) = \frac{s^2M^2\left[\frac{s}{L_1}\right]\left[\frac{s}{L_2}\right]}{\left[s^2 + \frac{sR_1}{L_1} + \frac{1}{L_1C_1}\right]\left[s^2 + \frac{sR_2}{L_2} + \frac{1}{L_2C_2}\right]} \tag{4.5}$$

or

$$L(s) = \frac{s^4k^2}{\left[s^2 + \frac{sR_1}{L_1} + \frac{1}{L_1C_1}\right]\left[s^2 + \frac{sR_2}{L_2} + \frac{1}{L_2C_2}\right]} \tag{4.6}$$

Under resonant conditions and switch open, Z_2 becomes purely R_2 at resonant frequency and we have:

$$\omega C_1 = \frac{1}{\omega L_1} \tag{4.7}$$

$$\omega C_2 = \frac{1}{\omega L_2} \tag{4.8}$$

Using the above resonant conditions, the transfer function from Vs to V1 can be written as:

$$\frac{V_1}{V_s} = 1 + \frac{j}{\omega C_1 r_1\left(1 + \frac{k^2\omega^2 L_1L_2}{r_1r_2}\right)} \tag{4.9}$$

4.2.2 Switch is closed

When the R_{load} is short, that is when the switch is closed we get:

$$L(s) = \frac{s^2 M^2 \left[\frac{s}{L_1}\right]\left[\frac{1}{L_2}\right]}{\left[s^2 + \frac{sR_1}{L_1} + \frac{1}{L_1 C_1}\right]\left[s + \frac{R_2}{L_2}\right]} \tag{4.10}$$

or

$$L(s) = \frac{s^3 k^2}{\left[s^2 + \frac{sR_1}{L_1} + \frac{1}{L_1 C_1}\right]\left[s + \frac{R_2}{L_2}\right]} \tag{4.11}$$

Under resonant conditions and switch closed, the capacitor is shorted out and the circuit is a LR circuit on the secondary side:

$$\omega C_1 = \frac{1}{\omega L_1} \tag{4.12}$$

$$\frac{V_1}{V_s} = 1 + \frac{j}{\omega C_1 r_1 \left(1 + \frac{k^2 \omega^2 L_1 L_2}{r_1 r_2 \left(\frac{j\omega L_2}{r_2} + 1\right)}\right)} \tag{4.13}$$

The envelope of the response will be determined by the poles of the L(s) that move with change in the k parameter.

4.2.3 Analysis

How fast the transients in a linear system die out is determined by the poles of the system for the chosen k parameter. So it would be worthwhile to do a root-locus of the L(s) for the two switch conditions with L2/R2 smaller than L1/R1 to determine the effect of the k parameter on how fast we can toggle between the two switch states. The root-locus plots are shown in Fig. 4-4.

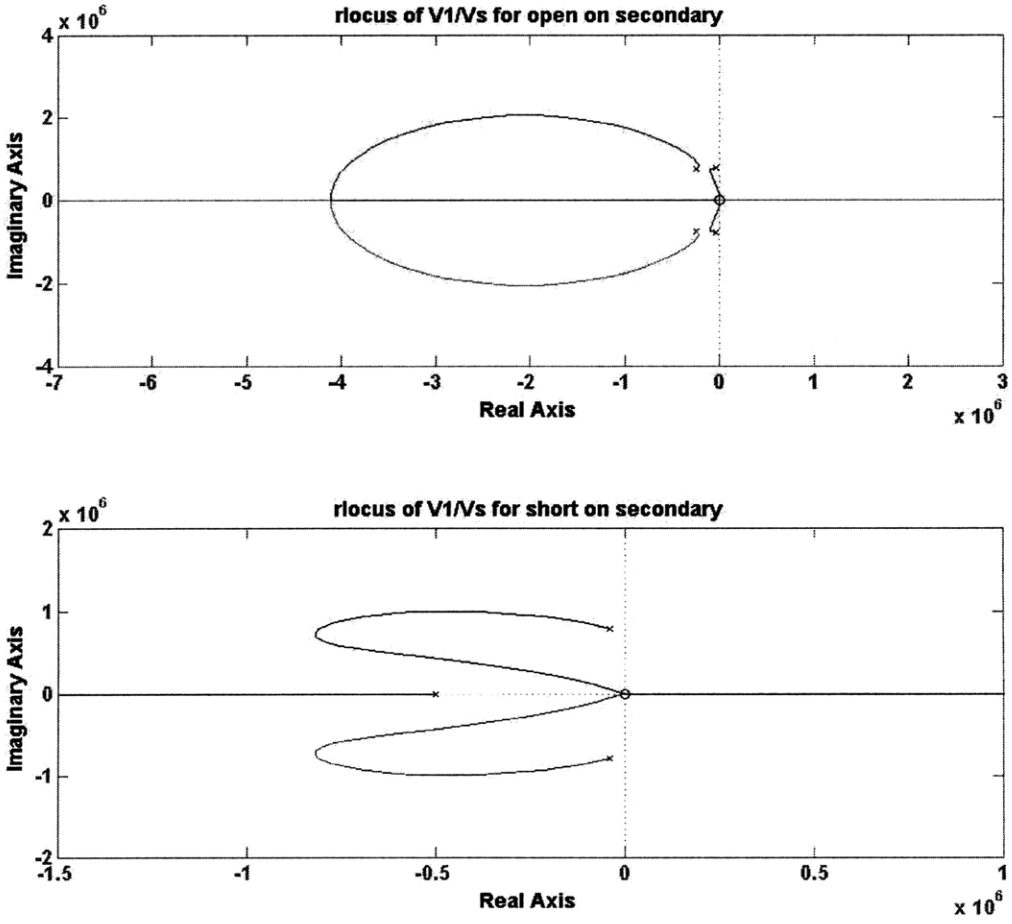

Figure 4-4: Rootlocus of loop gains with open and short

The open loop poles for the switch open condition have the real part as $-L_1/2R_1$ and $-L_2/2R_2$. The open loop poles for the switch closed condition have the real part as $-L_1/2R_1$ and $-L_2/R_2$. As the coupling coefficient k increases, k^2, the gain for

plotting the root-locus increases. The plot for switch open condition shows that the poles move closer as k increases before the slower poles due to the primary side heads for the origin and the faster pole due to the secondary side moves away from it. This means that initially coupling helps to make the system faster and then increasing it further makes the system slower. The poles for switch closed condition shows that as k increases the poles move away from the origin and the system gets faster.

Therefore the speed at which one can switch is determined by the poles due to the primary side and switch open condition. It is suitable to reduce the size of the primary coil at the reader for speed and size of the secondary coil on the implant to benefit both in terms of a smaller implant size and faster data transfer speeds. On the other hand the transfer function also shows that having a very small k, a small L1/R1, or L2/R2 makes the two expressions alike. Specifically making $\frac{jwL_2}{r_2}$ small makes the expressions alike for all values of L1/R1 and k. This reduces the difference between the amplitude of the envelope of the two states and makes it difficult to detect at the reader. Large difference between the two switch states is desirable.

Fig. 4-5 is plots the magnitude of the transfer functions at resonance using equations 4.9 and 4.13 for the two switch conditions of open and close respectively vs. the coupling coefficient k.

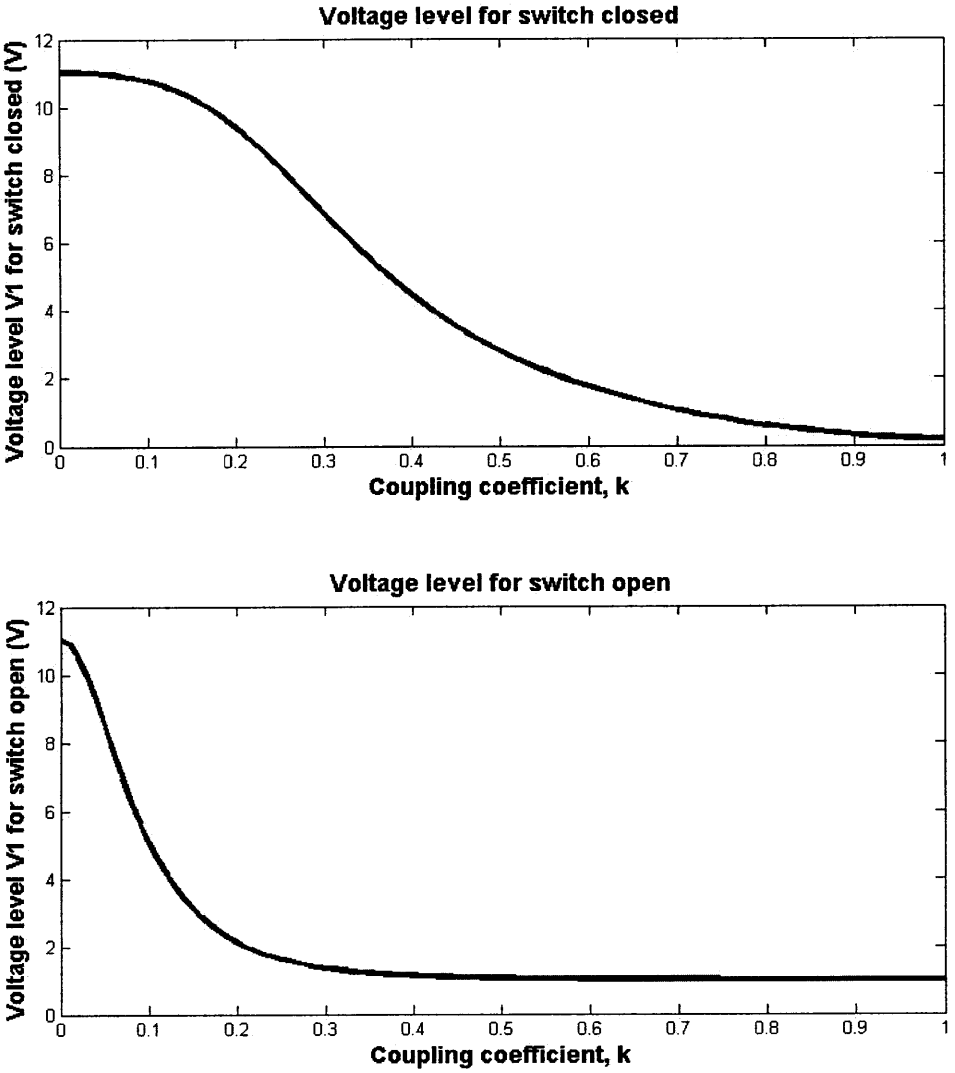

Figure 4-5: Voltage level V1 for the two switch states vs. coupling coefficient, k

The plot in Fig. 4-6 shows the difference in the magnitude of the transfer function equations 4.9 and 4.13 for the two switch states for various large and small combinations of L/R ratios on primary and secondary side. The plot shows that as coupling coefficient, k increases from zero as we bring the coils closer from far away, there is a peak in the voltage difference between the state followed by the drop. Increasing k further makes the difference go to zero before the difference increases again. Also for lower L1/R1 and/or L2/R2, the difference gets smaller.

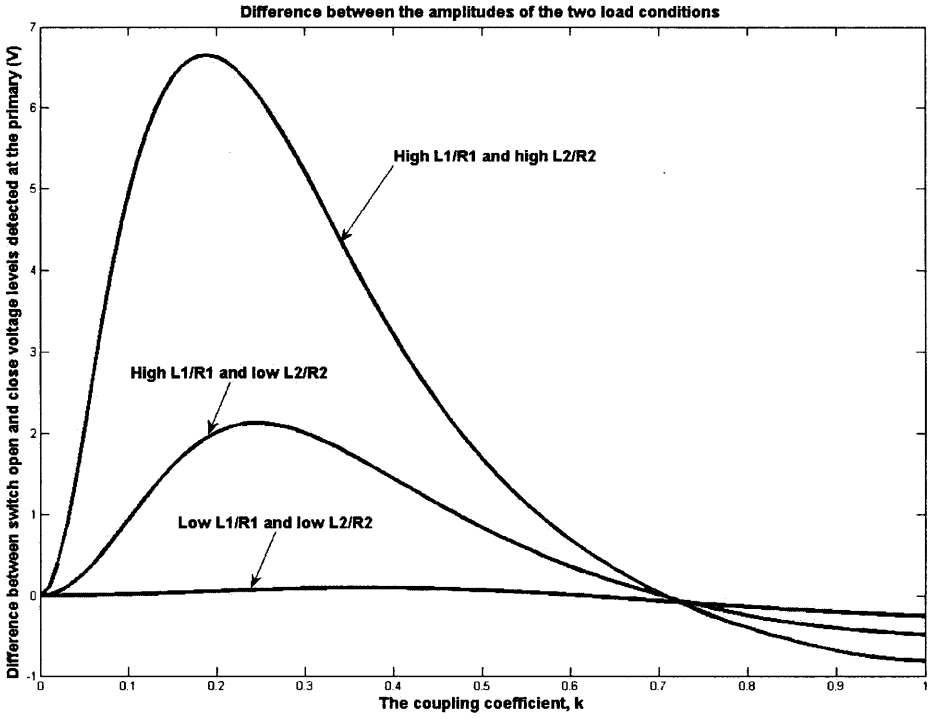

Figure 4-6: Difference between switch open and close voltage levels detected at the primary vs. coupling coefficient, k

Another consequence of decreasing L2/R2 and L1/R1 is that at constant resonant frequency, decreasing the L_2 value increases C_2 and similarly decreasing L_1 increases C_1. Just for comparison a capacitor value of 500pF implemented using multiple metal layer technique in a typical 5 metal layer 0.18 process could take about 1mm sq.

Since the memory is 32Kbits in size, we would at least want to upload the data

from the memory to the reader in less than 10s. This requires a transmission speed of about 4 Kb/s. We would like both L1/R1 and L2/R2 on the primary and secondary respectively to be less than 1/4000 seconds, that is 0.25 ms. For resistance of the order of Ohms, the inductance should be of the order of milli-henries or less.

In conclusion, decreasing the L_1/R_1 and L_2/R_2 increases the data transfer speeds and also makes the implant size smaller as inductances occupy more space than capacitors for a fixed resonant frequency. But doing so makes it difficult to discriminate the amplitudes of the modulated carrier wave for the two states at the reader. Also we do not want to place the two coils too close as high coupling decreases the difference.

4.3 Inductance and Coupling Coefficient Calculation

Inductance calculation for an N-turn multilayer circular coil can be calculated using the following formula [MICROCHIP]

$$L = \frac{0.31(RN)^2}{6R + 9h + 10b} \tag{4.14}$$

where R, h, b are in cms and L is in uH as shown in Fig. 4-7.

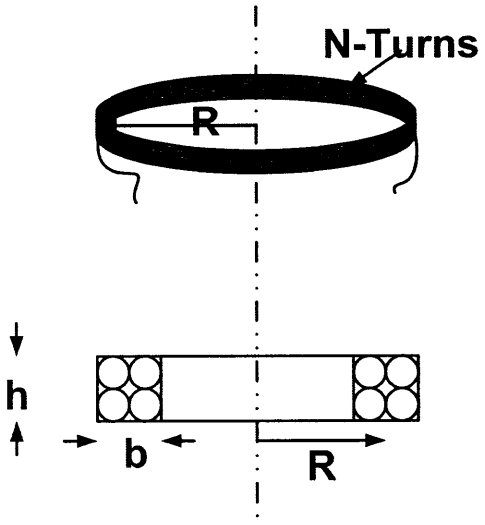

Figure 4-7: Inductance calculation

Since the secondary coil is smaller than the primary coil, the mutual inductance can be calculated by putting a current in the primary coil and assuming a constant field through the secondary coil area equal to the field along the axis connecting the coils. This assumption is good if the implant coil is smaller than the primary coil. Through reciprocity we have the same mutual inductance if current was put in the secondary coil, but this way is harder to calculate as in the first case. Refer to Fig. 4-8 for the mutual inductance and coupling coefficient calculation below.

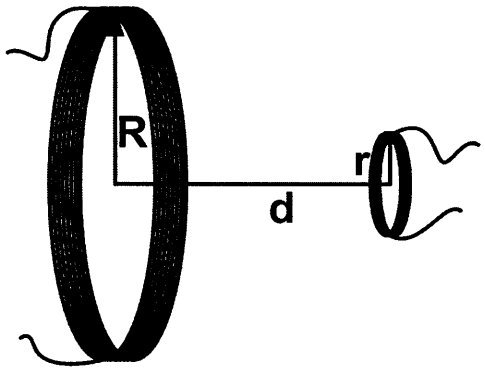

Figure 4-8: Mutual inductance and coupling coefficient calculation

B at the transponder due to the reader coil is

$$B = N_1 \mu_0 \frac{I_1 R_1^2}{2(d^2 + R_1^2)^{(3/2)}} \tag{4.15}$$

Therefore the mutual inductance is

$$L_m = N_2 B \pi R_2^2 I_1 = \mu_0 \frac{R_1^2}{2(d^2 + R_1^2)^{(3/2)}} \pi R_2^2 N_1 N_2 \tag{4.16}$$

Therefore the coupling coefficient is

$$k = \frac{L_m}{\sqrt{L_1 L_2}} = \mu_0 \frac{R_1^2}{2(d^2 + R_1^2)^{(3/2)}} \pi R_2^2 \frac{N_1 N_2}{\sqrt{L_1 L_2}} \tag{4.17}$$

Coupling coefficient k goes down as d^3 with everything else constant.

4.4 System

For the demonstration purpose the chosen carrier frequency is 125KHz due to availability of tag/transponder by Atmel that can be easily integrated with the implant system. For capacitors in pF range, the size of the inductors is very large for implant application. However the principles of RFID data link remain the same at higher frequencies and we will use Atmel's U3280 transponder interface and Atmel's U2270 reader for the demonstration due to availability. The RFID system is as shown in Fig. 4-9. The peak detector detects the envelope of the modulated RF carrier detected on the reader side.

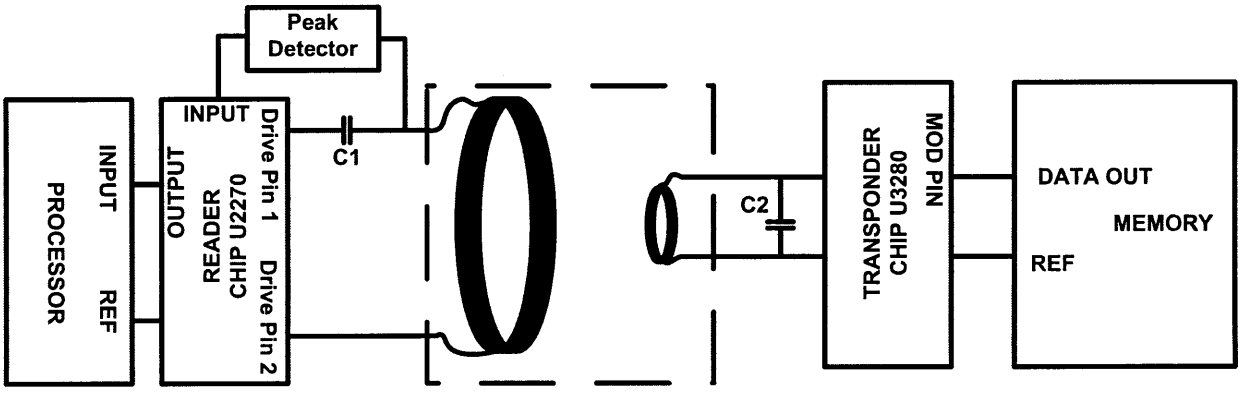

Figure 4-9: RFID system

Chapter 5

Test results

The memory integrated with the RFID data link was tested for different supply voltages. The following section describes the FSM implemented on FPGA for generation of control signals and interfacing the system to a PC for test purpose. The section after contains the simulation result of the memory in Cadence. The results are documented in the sections following simulation. Figure 5-1 shows the memory chip die and figure 5-2 shows the test setup.

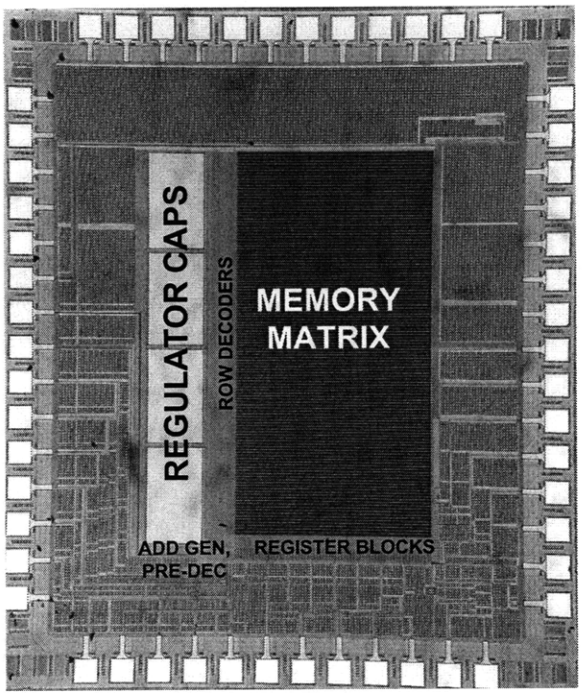

Figure 5-1: Chip die picture

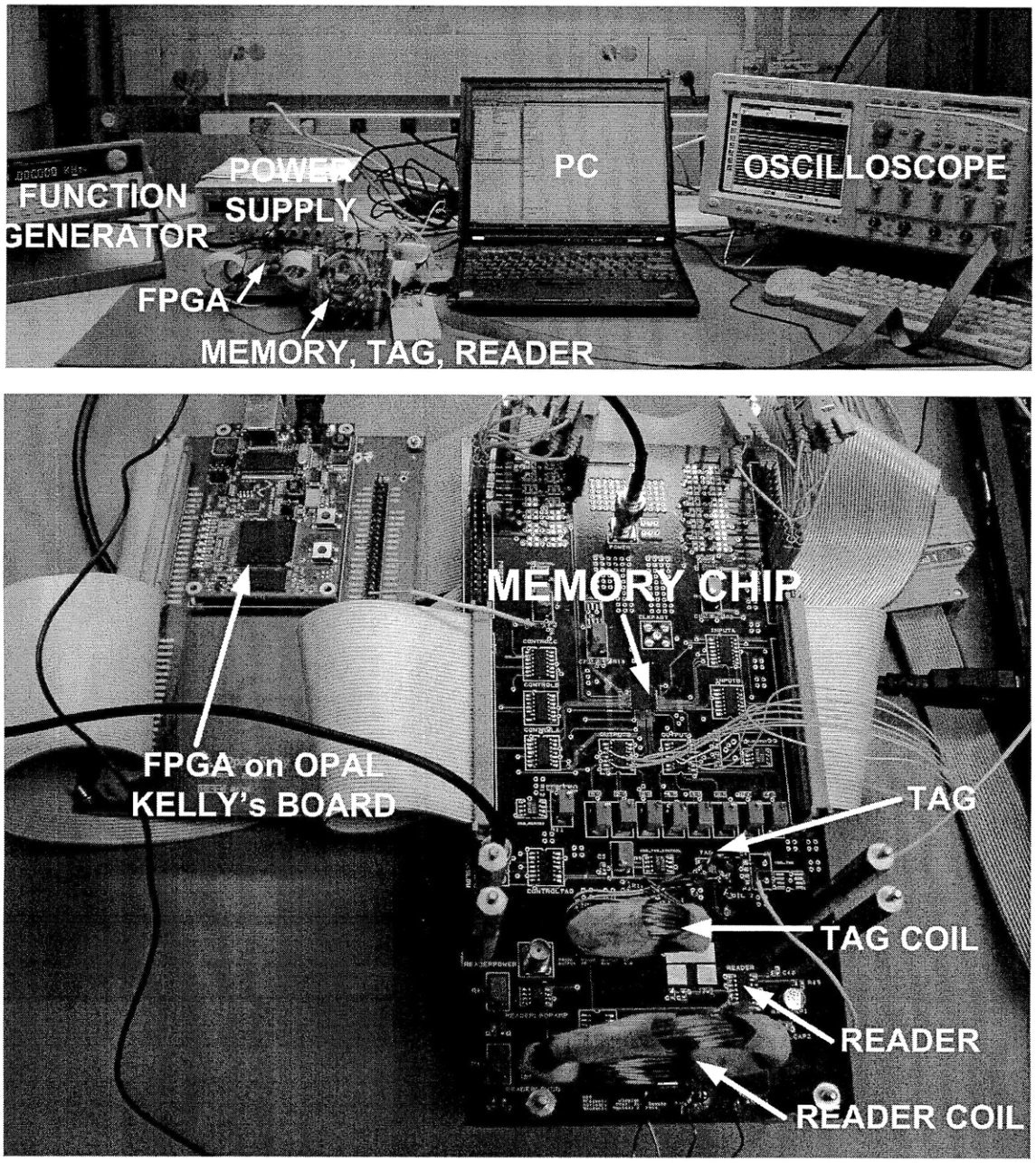

Figure 5-2: Test setup

5.1 Control

The control circuitry for the memory and RFID tag is implemented on a Xilinx FPGA on Opal Kelly board. The control circuitry is a Finite state machine (FSM) written in Verilog language using the Modelsim environment. The FSM diagram is shown in

Fig. 5-3. The compiled FSM runs on the FPGA to generate a sequence of signals that accomplishes write and read from the memory. While the memory signals are generated by the FSM on FPGA, the FSM itself receives high level signals, WRITE, READ, and RUN, from the PC using Opal Kelly's command library from inside Matlab. The WRITE and READ signals select the functionality while the RUN signal steps the FSM to the next state. For testing purposes the data to be written to the memory is generated randomly in 8-bit bursts from within Matlab and put on the INPUT[0:7] bus of the memory using Opal Kelly's interface through FPGA. The description of the control signals for the write and read operation and their sequence was mentioned in the chapter on memory. The FSM also generates the MOD signal for the RFID tag during the memory read operation to transfer the read data over RFID link. This signal modulates the RF carrier and this modulated carrier is interpreted as data by the reader on the other side of the RFID data-link.

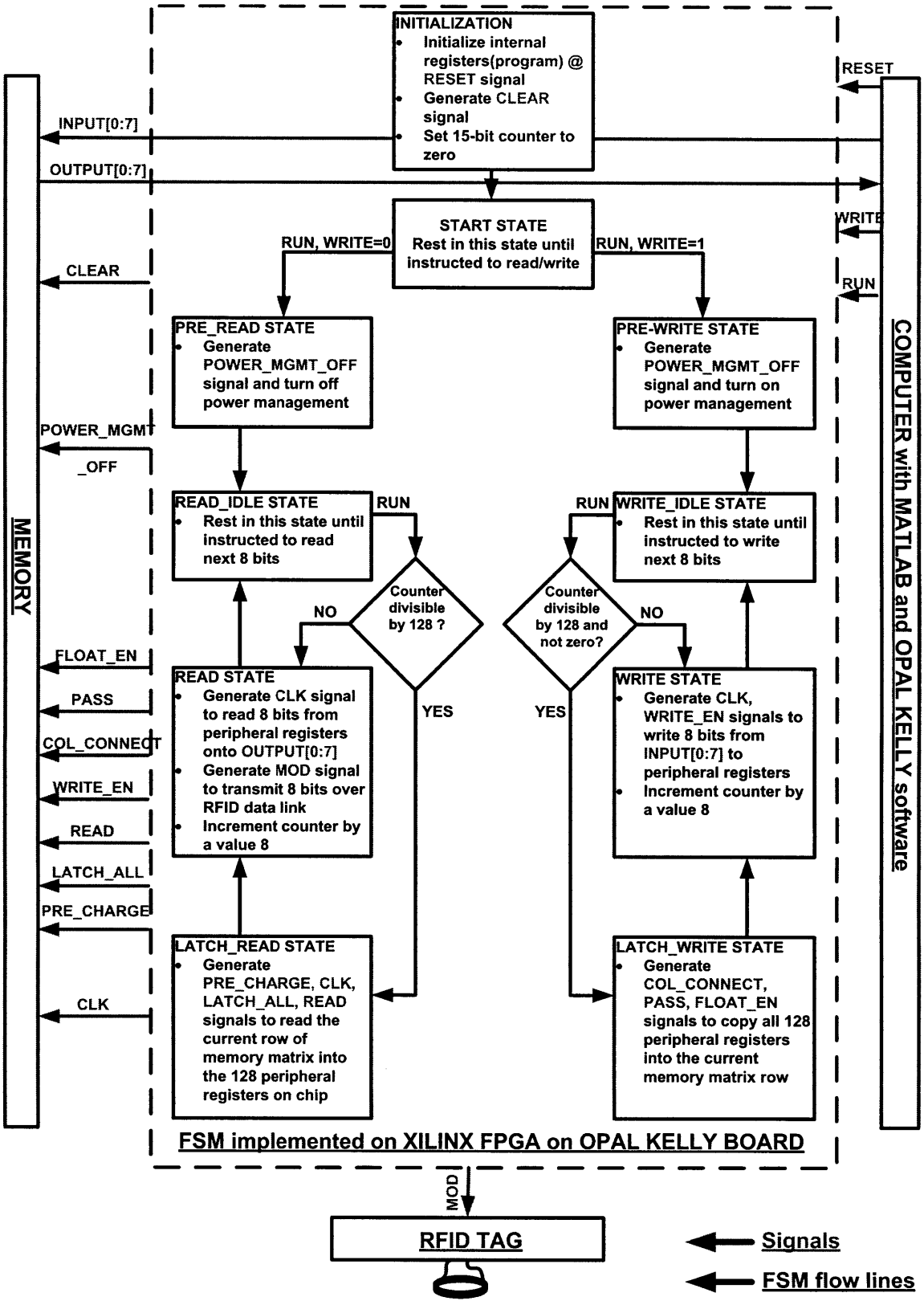

Figure 5-3: Finite state machine on FPGA for generation of control signals: Block diagram

5.2 Simulation of the memory

The simulation for the write and read back from the memory is shown in Fig. 5-4 and Fig. 5-5. The voltage regulator switching frequency was 1 MHz and ultra-capacitor supply voltage was 2 V. Fig. 5-4 shows a sequence of bits written from serialized input/output (serialization of an 8 bit parallel bus is done for simulation and easy viewing in the figure) to registers followed by collectively writing the registers to a row in the memory matrix. For simulation of write operation, the counter and registers are reset with a CLEAR signal followed by reading the memory matrix row into the register to be eventually put one at a time on the I/O as the counter increases with each CLK rising edge. Notice how the bit-cell stored voltage level falls in bit-cell 0 and 1 during the write from registers to the memory matrix. This is due to the signal FLOAT-ENABLE signal that temporarily floats the power supply lines to the bit-cells for an easy write as discussed in the chapter on memory. Fig. 5-5 shows the control signals required to achieve the write and read operation.

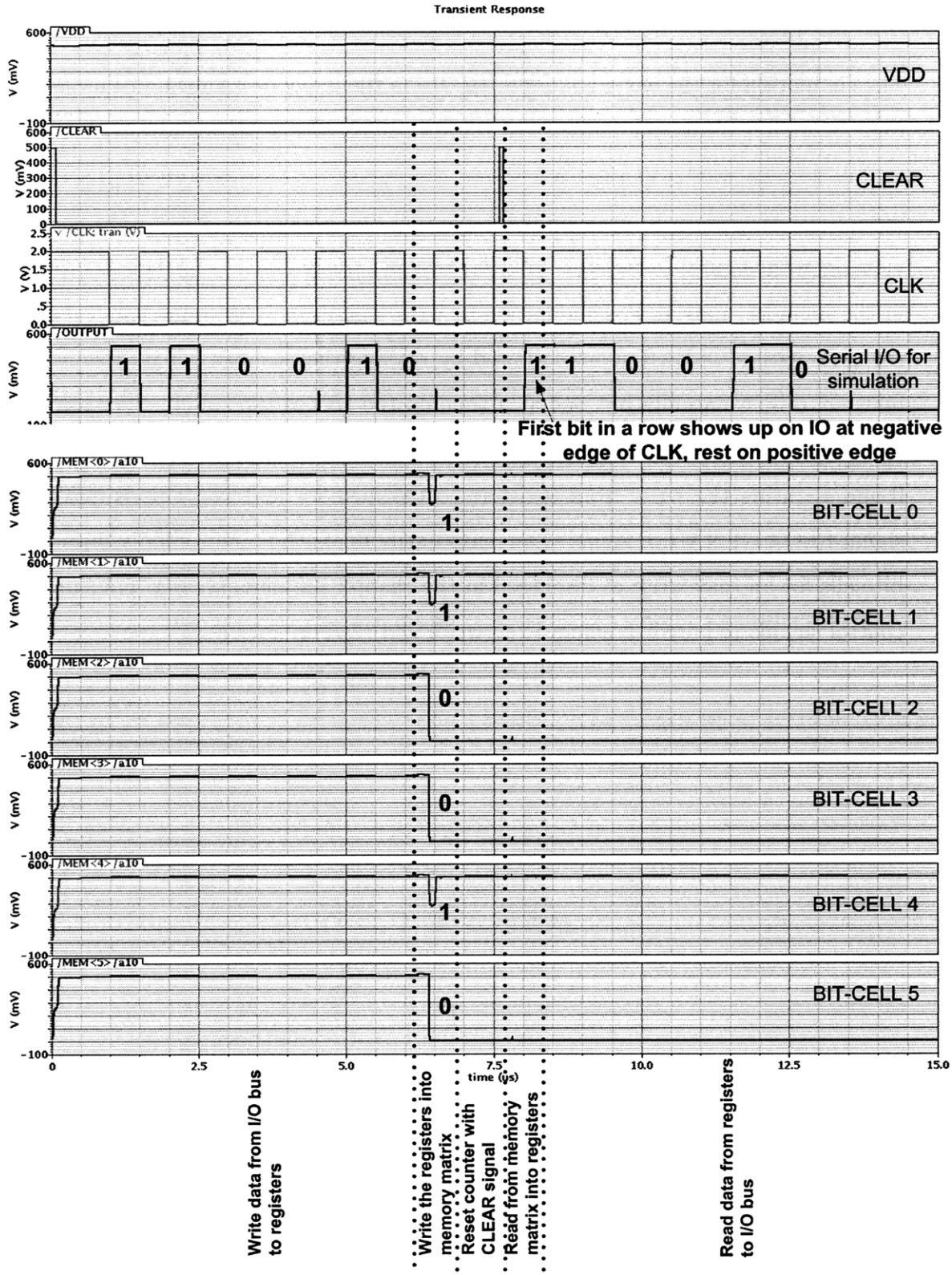

Figure 5-4: Memory write and read simulation

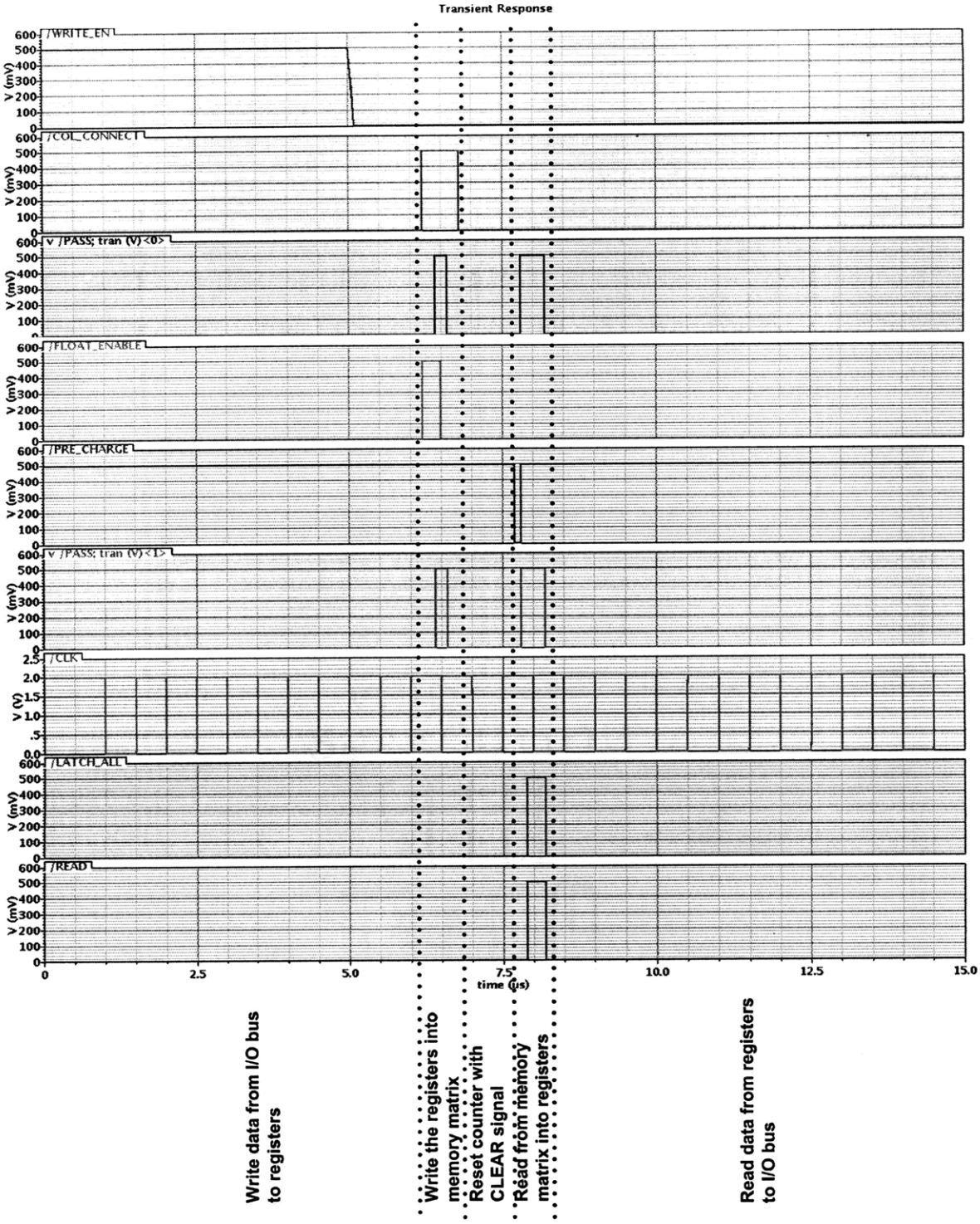

Figure 5-5: Control signals for simulation of memory write and read operation

5.3 Measurements

5.3.1 Memory

The memory control signals for the write operation generated by the FSM on FPGA are shown in figure 5-6 as recorded on a digital oscilloscope. The output bus shows the input data just registered by the memory on the registers for verifying that this step completed accurately. The bits are written to the memory matrix at the end of the oscilloscope capture in the figure.

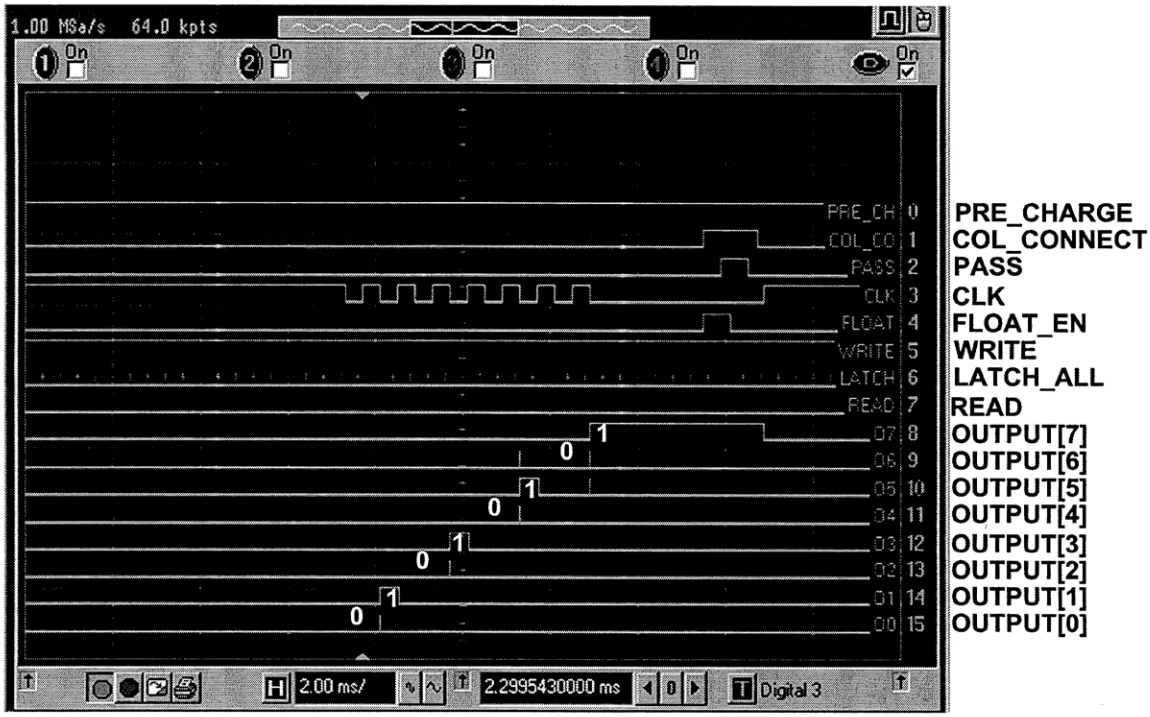

Figure 5-6: Control signals generated by FSM on FPGA for write operation

The memory control signals for the read operation generated by the FSM on FPGA are shown in figure 5-7 as recorded on a digital oscilloscope. Also shown is the data on the output bus of the memory that is send over RFID data-link. The modulated carrier detected on the reader side is also shown in the oscilloscope capture and figure 5-9.

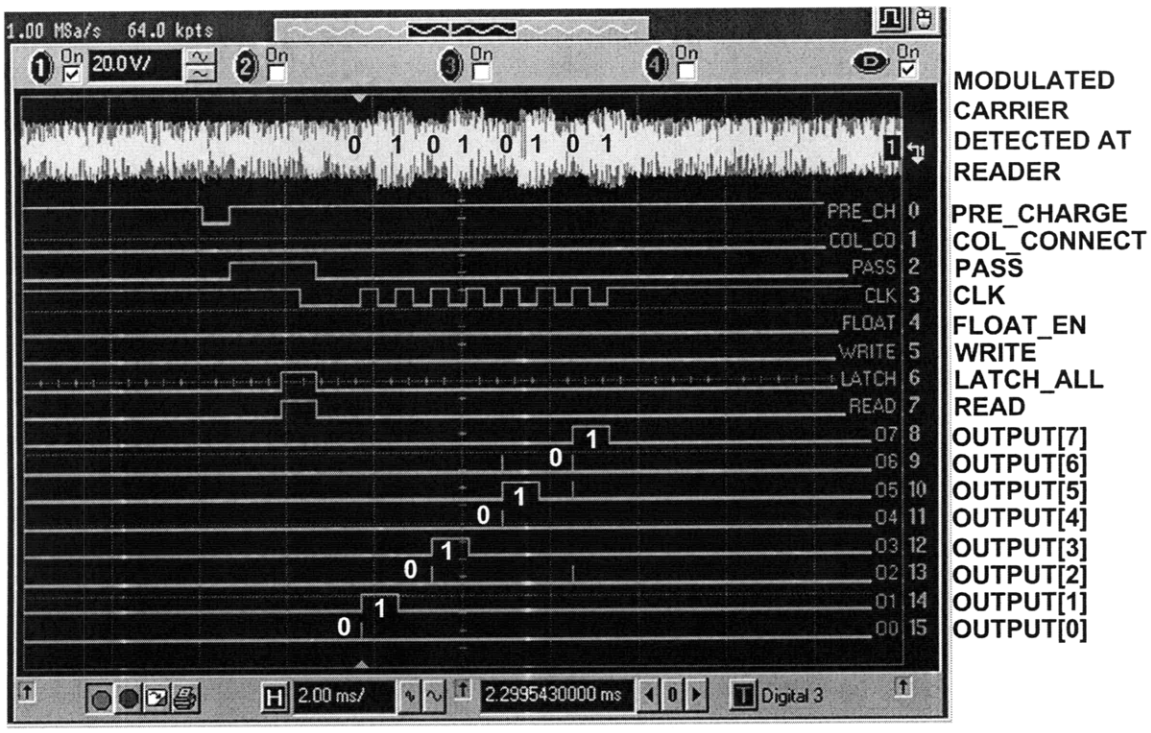

Figure 5-7: Control signals generated by FSM on FPGA for read operation. Also shown is the RFID modulated carrier detected on the reader side

The memory test was performed by writing random data generated in Matlab to the memory and then reading it back. Any discrepancy between the data to be written and that which was read back was recorded and presented in a color-coded bit-error rate grid diagram representing the physical memory matrix. The memory was tested at four voltages; 0.45, 0.50, 0.60, and 0.80 V. In figure 5-8 are shown the grid diagrams for supply voltage of 0.45 V and 0.6 V for comparison. Seemingly, the error rate is randomly distributed over the memory matrix.

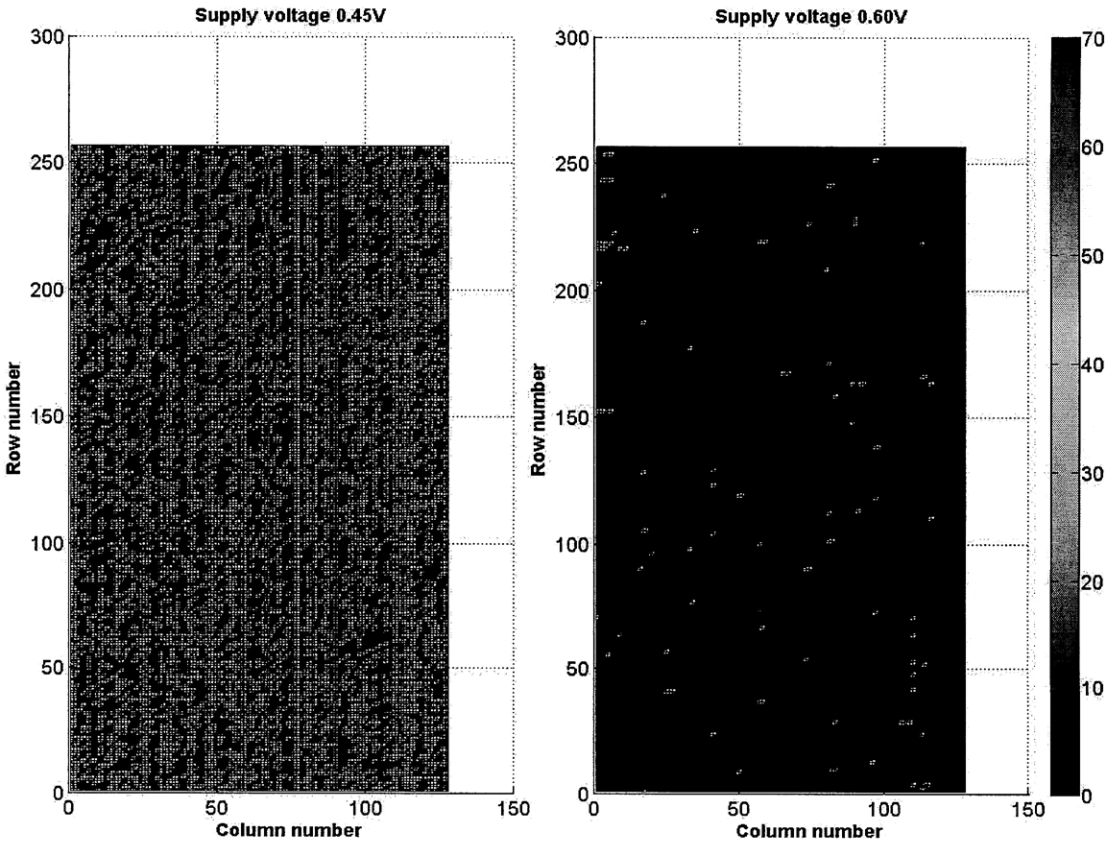

Figure 5-8: Memory matrix with color coded bit-error percentage for data write and then read back of random data

The bit-error rate increases as we lower the supply voltage from 0.80 V to 0.4 V. At 0.8 V the bit-error rate is zero for a finite number of runs. At 0.6 V, 0.5 V, and 0.45 V, the bit-error rate is 0.05 percent, 3.4 percent, and 8.6 percent respectively.

At 0.45 V the bit-error rate increases to 8.6 percent. The possible cause of this high bit-error rate at low voltages could be the low noise margins in the design as noise margins decrease with decreasing supply voltage.

The memory drew a current of 0.48 uA, 0.96 uA, and 2 uA at 0.33 V, 0.45 V, and 0.50 V respectively.

5.3.2 RFID data-link

In Fig. 5-9 is shown the oscilloscope capture of the modulated RF carrier detected on the reader side for a stream of bits 01010101 (chosen for ease of recognition) send from the tag side over the RFID data link.

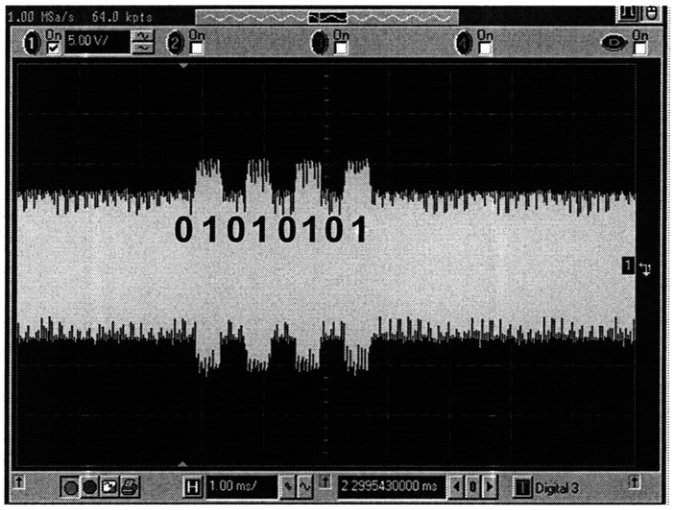

Figure 5-9: RFID modulated carrier detected on the reader side

Two different coils were used for the illustration of the impact of the selected coupling inductor on the tag side. The following figure shows the difference between size of the envelope detected on the reader side for the two sizes of inductor on the tag side as the distance between the reader and tag coil is changed. Inductance value of 206uH and 90uH were used on the tag side for a fixed reader coil of 573uH. Since the coils were self-wound, the calculated inductance is not very accurate but suffices for demonstration purpose. As shown in the figure 5-10 if we use a smaller size coil the difference between the peaks and troughs of the modulated carrier RF signal that is detected at the reader decreases. The RF carrier is only 125KHz and so the inductance values is large. At higher frequencies such as 900MHz the inductance would be substantially small but principles of RFID remain the same which have been demonstrated here.

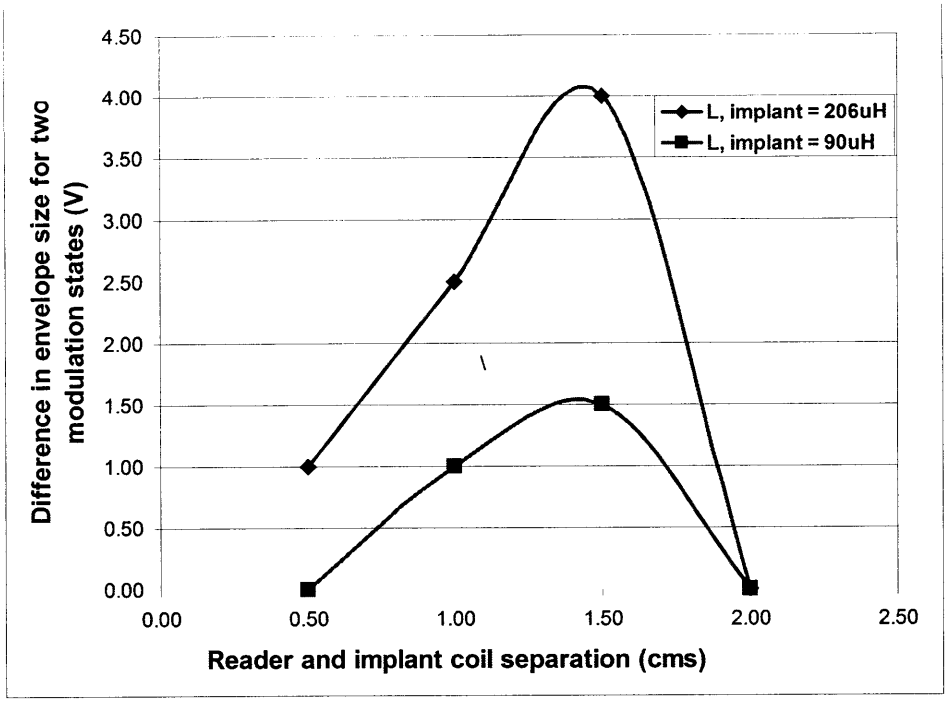

Figure 5-10: Difference in the envelope size of the carrier in the two modulation states for two different inductors on the implant side versus the separation between the reader and tag coils

5.3.3 Voltage regulator

On testing the voltage regulator output voltage did not follow the input ultra-capacitor at one-fourth ratio that is desired and expected. The voltage level at the voltage regulator output did not drop when the switches were held in either a parallel or a series configuration by holding the input clock signal at a high or low voltage. This is unexpected. If the input clock was toggled the output responded but not as in simulations. The ratio between the output of the regulator and the ultracapacitor input voltage started at about a quarter and rose to one-third and then to a half with a rise in ultracapacitor voltage. We expected it to stay constant at a quarter.

This unexpected result was traced back to a faulty connection in the chip layout. The body connections of the PMOS transistors in the voltage regulator were mistakenly connected to the VDD instead of the highest voltage which is the ultracapacitor

voltage. This faulty connection forward biases the P-N junctions of the MOSFET and leaks current from source and drain to the body. Since the body is connected to the VDD, this causes the voltage at this node to rise.

5.4 Conclusion

The designed memory had a zero percent bit-error rate for the finite number of write and read operation at about 0.8 V supply voltage. The bit-error rate of 0.05 percent at 0.6 V is acceptable. To achieve better performance at lower supply voltages, the noise margins need to be increased by sizing while maintaining lower power consumption by using different techniques. The RFID data link at 125 Khz provided a starting point for link at higher frequencies. It demonstrated the working of a RFID system and showed the significance of coil sizes on amplitude and speed at which data can be detected on the reader side.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this design I have chosen to use minimum-sized devices to reduce the leakage currents. But like any design it is a trade off. Minimum-sized devices reduced the bit-cell noise margins and made them more prone to loss of stored data and therefore increase in bit-error rate. At 0.8 V the memory gave no error for the finite number of write and read operations. To achieve better performance at lower supply voltages, the noise margins need to be increased by sizing while maintaining lower power consumption by using different techniques.

The mathematical model of the voltage regulator was derived and shown to match in the Matlab and Cadence simulation plots and will be implemented again in future versions of this chip.

The RFID data link was integrated with the memory and the coil size affected the data detection at the reader as the theory predicted. Decreasing the implant inductance and coil size made it difficult to discriminate the amplitudes of the modulated carrier wave for the two states at the reader. The RFID data link analysis and integration at 125 Khz provide a starting point for link at higher frequencies.

6.2 Future work

In future some of the possible improvements can be an increase of the read noise margin of the bit-cell that would extend the memory operation to the desired low supply voltage. The generation of control signals can be implemented on the memory chip itself. The RFID data link can be implemented at a higher carrier frequency which will reduce the inductor size. The RFID load switching circuit can also be implemented on chip in future versions.

Bibliography

[1] M.W. Baker and R. Sarpeshkar. Feedback analysis and design of RF power links for Low-Power bionic systems. *Biomedical Circuits and Systems, IEEE Transactions on*, 1(1):28–38, 2007.

[2] B.H. Calhoun and A.P. Chandrakasan. A 256-kb 65-nm sub-threshold SRAM design for Ultra-Low-Voltage operation. *Solid-State Circuits, IEEE Journal of*, 42(3):680–688, 2007.

[3] J.P. Conti. Getting under your skin. *Communications Engineer*, 5(2):28–33, 2007.

[4] Daniel M. Dobkin. *The RF in RFID: Passive UHF RFID in Practice.* Newnes, September 2007.

[5] John G. Kassakian, Martin F. Schlecht, and George C. Verghese. *Principles of Power Electronics.* Prentice Hall, facsimile edition, July 1991.

[6] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. *Digital Integrated Circuits.* Prentice Hall, 2 edition, 2003.

[7] A. Salarian, H. Russmann, C. Wider, P.R. Burkhard, F.J.G. Vingerhoets, and K. Aminian. Quantification of tremor and bradykinesia in parkinson's disease using a novel ambulatory monitoring system. *Biomedical Engineering, IEEE Transactions on*, 54(2):313–322, 2007.

[8] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits Revised Edition.* Oxford University Press, USA, 5 Har/Cdr edition, August 2007.

[9] E. Seevinck, F.J. List, and J. Lohstroh. Static-noise margin analysis of MOS SRAM cells. *Solid-State Circuits, IEEE Journal of*, 22(5):748–754, 1987.

[10] E.J.W. Van Someren, B.F.M. Vonk, W.A. Thijssen, J.D. Speelman, P.R. Schuurman, M. Mirmiran, and D.F. Swaab. A new actigraph for long-term registration of the duration and intensity of tremor and movement. *Biomedical Engineering, IEEE Transactions on*, 45(3):386–395, 1998.

[11] Yannis Tsividis. *Operation and Modeling of the MOS Transistor.* Oxford University Press, USA, 2 edition, June 2003.