Self-Aligned AlGaN/GaN Transistors for Sub-mm Wave Applications

by

Omair I. Saadat

B.S., Electrical Engineering (2007)
Stanford University

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

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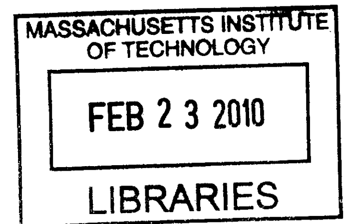

Master of Science in Electrical Engineering

at the

Massachusetts Institute of Technology

February 2010

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ABSTRACT

This thesis describes work done towards realizing self-aligned AlGaN/GaN high electron mobility transistors (HEMTs). Self-aligned transistors are important for improving the frequency of AlGaN/GaN HEMTs by reducing source and drain access resistance. The eventual fabrication of self-aligned transistors required the development of two different technologies that are described in this thesis. First, gate stacks that can survive the high temperature anneal necessary for forming ohmic contacts were demonstrated. Devices with three different gate stacks, composed of tungsten and a high-k dielectrics like HfO_2, Al_2O_3 and HfO_2/Ga_2O_3, were studied and compared with respect to DC transistor measurements, capacitor measurements and pulsed-IV measurements. Not only did these transistors survive the ohmic anneal but they showed superior performance with respect to transconductance, current density and dispersion than transistors with standard gates. Following the development of the gate stack, silicide-like technology where thin Ti-based films are deposited and annealed on the access regions to reduce access resistance was developed. Depositing and annealing thin Ti films were shown to reduce the sheet resistance by up to 30%. Finally, preliminary results regarding the fabrication of self-aligned transistors by using these gate stacks and the Ti-based access region metallization are reported in this thesis.

Thesis supervisor: Tomás Palacios
Title: Assistant Professor of Electrical Engineering

Acknowledgements

First and foremost, I would like to thank my advisor, **Prof. Tomas Palacios**, for all his help and support for the past two and a half years. I am grateful for his enthusiasm and patience. I can't count the number of times that Tomas have done above and beyond the call of duty to help me out by improving my writing and helping to figure out problems in research. Due to Tomas' tutelage and his, I really believe that I have grown a lot as a researcher. Thank you Tomas!

I would also like to thank my group mates in the Palacios Group. As the senior student in our group, **Will Chung** taught me the basics of device fabrication, e-beam lithography and transistor measurement. I would like to thank my officemate, **Bin Lu**, for all our discussions about anything and everything under the sun. I have learned a lot from Bin but importantly, he has shown me the importance of just plowing ahead and doing things. **Fred Mieville** and **Dr. Jose Tirado** also joined our group at the same time as me and we shared a very pleasant year together. **Han "Sir Han" Wang** and I have also have many discussions about Gallium Nitride, England, Cambridge and many other things. **Allen Hsu** was my fellow partner in crime with our new cryogenic probe station. I have had many productive discussions with **Dr. Mohamed "Mo" Azize** about materials growth, materials characterizations, and experimental thoroughness among other things. Finally, I would like to thank the rest of my groupmates (both past and present) for all their help and discussions: **Xu Zhao**, **Justin Wu**, **Daniel Piedra**, **Feng Gao**, **Benjamin Mailly**, **Dong Seup Lee** and **Dr. Kevin Ryu.** Last but certainly not least, our group administrator **Elizabeth Kubicki** for ensuring that our group runs in an efficient manner.

The great thing about being on the 6th floor of Building 39 and working in TRL are all the interactions with fellow graduate students and staff members. In particular, I would like to thank **John Hennessy** for teaching me the basics of atomic layer deposition. Also, **Dr. Ivan Nausieda** was always available to serve as a 24 hour buddy.

As everyone who has ever worked in the Microsystems Technology Laboratory (MTL) knows, the fab would not run without the dedication and hard work of all the staff. **Dave Terry** kept the photo and wet benches running without fail. **Bob Bicchieri** gave invaluable assistance with the Plasmaquest. Other staff members who were very helpful include (but certainly not limited to) **Donal Jamieson**, **Dr. Vicky Diadiuk**, **Kurt Broderick**, and **Paul Tierney** among others.

I also used facilities outside of MTL for this thesis work. I would also like to thank Mark Mondol for the phenomenal job he does with keeping the SEBL facilities running. At Harvard CNS, **Mac Hathaway** and **Nicholas Antoniou** kept the ALD tool and the FIB tool running smoothly.

Outside of work, my friends gave me invaluable companionship and support. First and foremost, I must recognize my roommate, **Daniel Prashanth Kumar**, for putting up with me and all my quirks for the past 30 months. My time here in Cambridge would not have been nearly as enjoyable were it not for him. Other dear friends here at

MIT and Boston include **Mohamed Abutaleb**, **Imran Shamim**, **Siddharth Bhardwarj**, **Zekeriyya Gemici**, **Eddie Eltoukhy** and **Victor Li**. I would also like to thank my friends from the EECS GSA and the MIT MSA for their companionship. Thank you all for your camaraderie and here is to many more enjoyable years ahead.

Sir Isaac Newton famously observed that "If I have anything, it is for I have stood on the shoulders of giants." Given how much I owe my mentors for helping me to get where I am today, this certainly holds true for me. My high school physics teacher, **Sgr. Marco Giordano**, first introduced me to the world of physics and research and I am immensely grateful to him for that. As an undergrad at Stanford, I had the opportunity to spend a wonderful summer at UC Santa Barbara working with **Prof. Andrew Cleland** and **Dr. David Wood**. Other mentors at Stanford include **Prof. Subhasish Mitra**, **Prof. Roger Howe** and **Dr. J Provine**.

Personally, I owe everything to my family. I would like to thank both my parents for all their love and support. My siblings **Zuhair**, **Jaafer** and **Noor-Aysha** were the best cheerleaders anyone could have. Finally, I would like to thank my fiancé, **Aysha Ismail**, for all her encouragement and love.

Lastly, I would like to thank God for everything is due to him.

Partial financial support was provided by Raytheon and by the American taxpayer through the Office of Naval Research (ONR) MINE MURI program.

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Chapter 1: Introduction and Motivation for Self-Aligned Transistors

Section 1.1: Improving Frequency Performance of AlGaN/GaN HEMTs

AlGaN/GaN High Electron Mobility Transistors (HEMTs) have been of great interest for high power and high frequency applications because of excellent transport properties and large critical electric field values [1]. Ever since M.A. Khan et al. demonstrated the first AlGaN/GaN HEMT in 1993 and measured the microwave performance of these HEMTs in 1994, the current densities and frequency performance of these transistors has been continually improving [2], [3]. Reducing gate lengths down to L_g = 30 nm have allowed for a unity gain frequency (f_T) as high as 181 GHz [4]. In addition, new designs like introducing InGaN back barriers to improve electron confinement have also led to frequency improvements, as demonstrated by transistors with gate lengths of 100 nm with an f_T of 153 GHz [5]. In order to further enhance the frequency performance of AlGaN/GaN based HEMTs, shrinking down the gate without other forms of scaling will not be enough [6]. For example, it is important to reduce the distance between the gate and the channel by scaling down the barrier thickness. Source and drain access resistances are also key for improving frequency performance.

The simplest expressions for f_T ignore all contributions due to source and drain parasitic resistance [7]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

In the expression above, g_m is the transconductance, C_{gs} is the gate-source capacitance and C_{gd} is the gate-drain capacitance. If we take the source and drain parasitic resistance into account, we get a circuit model as shown in Figure 1.

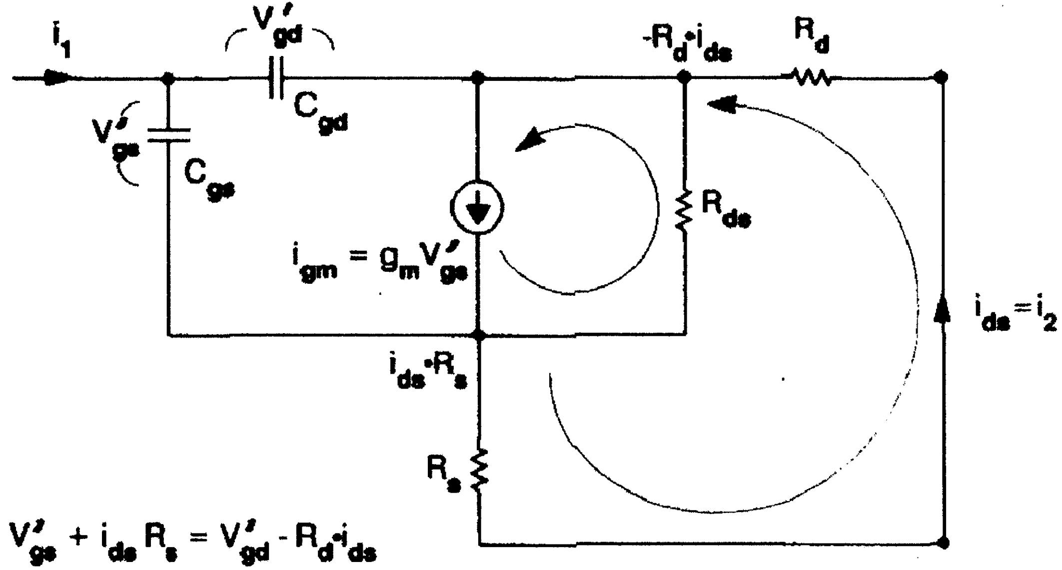


Figure 1: Small signal model that incorporates output resistance (R_{ds}) and parasitic source and drain resistance [7]

Based on this circuit model, if we incorporate the parasitic resistances, the expression for f_T becomes

$$f_T = \frac{g_m/(2\pi)}{\left[C_{gs} + C_{gd}\right] \times \left[1 + (R_s + R_d)/R_{ds}\right] + C_{gd} g_m (R_s + R_d)}$$

In the expression above, R_s is the source parasitic resistance, R_d is the drain parasitic resistance and R_{ds} is the output resistance of the transistor. We can also rewrite the expression for f_T in the following manner in order to better see the intrinsic and the parasitic delays

$$\frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} + \frac{(C_{gs} + C_{gd})(R_s + R_d)}{g_m R_{ds}} + C_{gd}(R_s + R_d)$$

The first term is composed of the intrinsic delay of the transistor while the next two terms are related to the parasitic delays. Due to these parasitic delays, the f_Ts of transistors,

especially deeply scaled transistors, are lower than what can be expected based on the intrinsic performance [7]. In particular for GaN based HEMTs, the access resistances are higher than for HEMTs fabricated in other material systems and C_{gd} is also high due to high carrier concentrations [8].

The effect of parasitic resistance on the frequency performance has been studied through low temperature measurements of high frequency devices [8]. At lower temperatures, the sheet resistance of the source and drain access resistance drops since the mobility increases. In GaN, electron mobility is limited by optical phonon scattering and scales as a function of temperature. The electron mobility increased by a factor of 4 as the temperature was dropped from 300 K down to 77 K. Figure 2 shows how the DC saturation current increases as a function of temperature, which can be attributed to the reduction in the access regions. As a result of the decrease in the access resistance, the f_T of these devices increased from 65 GHz to 80 GHz, as shown in Figure 3.

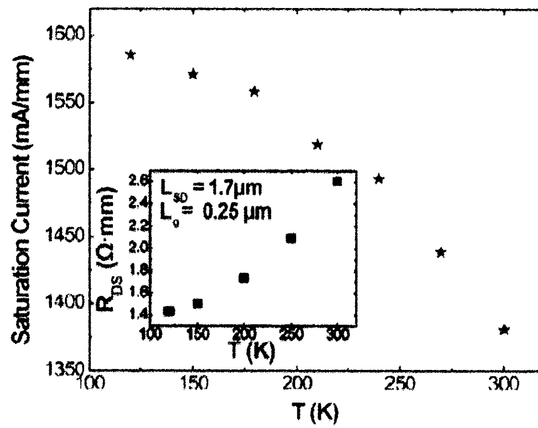


Figure 2: Main figure shows DC saturation current as a function of temperature. The inset is a plot of R_{ds} vs Temperature [8].

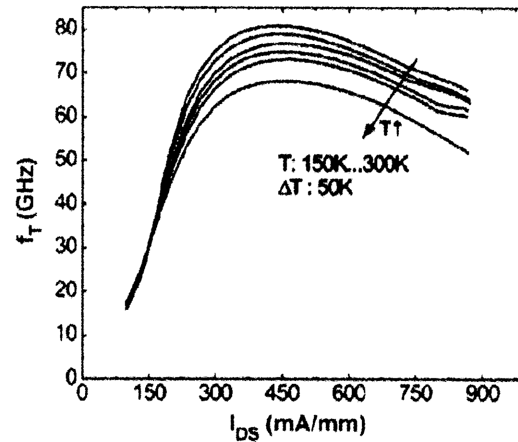


Figure 3: f_T vs. drain current density for different temperatures. Note how increasing the temperature reduces the max f_T [8]

A. Endoh et al. also reported increase in f_T for HEMTs with L_g = 45 nm and L_{sd} = 1.5 µm from 156 GHz to 194 GHz as the temperature was decreased from 300 K to 16 K [9]. The increase in f_T is again attributed to the increase in mobility and the decrease in access resistance.

The maximum oscillation frequency (f_{max}) is a figure of merit which corresponds to the frequency where the input power into the gate is equal to the output power at the drain. Figure 4 is a plot of predicted frequency performance for a device with a gate length of 50 nm and it shows that improving both f_{max} and f_T are dependant on reducing access resistance

Reducing the access resistances also lowers the knee voltage (the drain voltage at which the transistor transitions between the linear region and the saturation region for a fixed gate voltage) [10]. By lowering the knee voltage, higher on-currents can be achieved at lower drain voltages, which reduces the electric field present in the drain access region. High electric fields in the drain access region induce depletion, thus

contributing to drain delay [11], [12]. As shown in Figure 5, drain delay is a dominant component of the total delay in very short gate length transistors [13]. Therefore, lower access resistances will allow for reducing the drain voltage without sacrificing current density which in turn will reduce the drain delay and improve frequency performance.

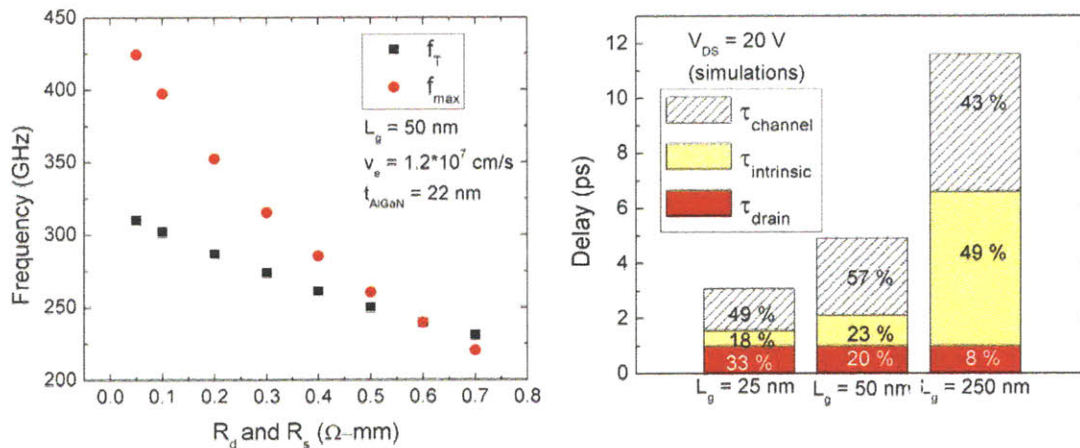


Figure 4: Frequency performance vs source and drain resistance. The on-current is assumed to be constant

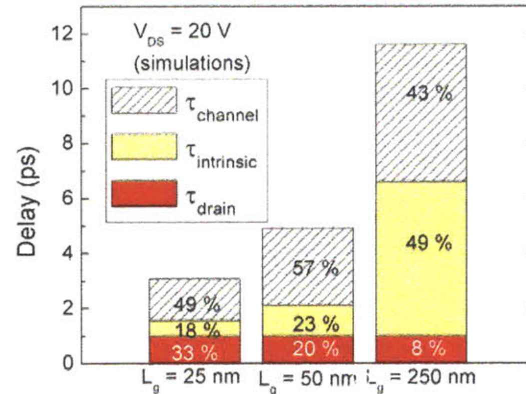


Figure 5: Various delays associated with transistor performance. Drain delay gets more dominant as gate lengths scale down [13]

Section 1.2: Summary of Self-Aligned Work

The first self-aligned Silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices were demonstrated in 1968 at Bell-Labs and were later used in production by Intel Corporation [14], [15], [16]. These self-aligned MOSFETs helped reduce the device geometries and eliminated the need of a critical photo-alignment step [17]. In order to fabricate these self-aligned gates, the Al gate was replaced with polysilicon gates so that the gate could survive the high temperature processing necessary for forming ohmic contacts to the source and drain[18]. Contacts to the source and drain

are formed by depositing metals and annealing them in order to form metal silicides. Figure 6 shows a simplified process flow for fabricating self-aligned silicon transistors.

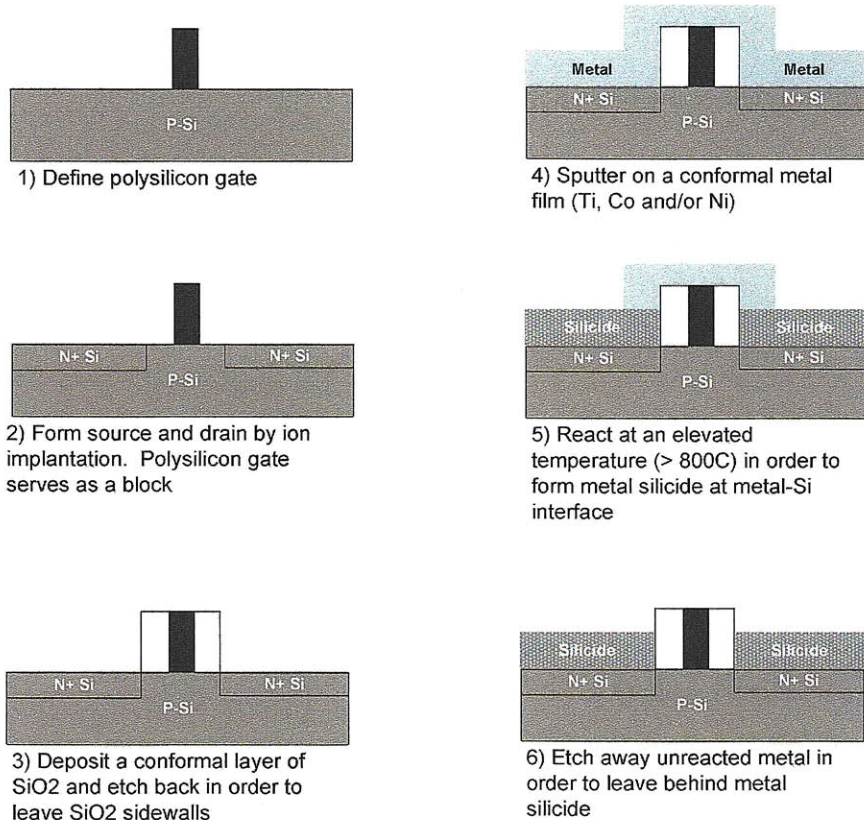


Figure 6: Process flow for self-aligned NMOS Si transistor with polysilicon gate

While the process flow shown in Figure 6 is for older transistor technologies with poly-Si gates, state of the art Si CMOS devices with high-k dielectrics and metal gates utilize a similar process flow. In a typical 45-nm device, a dummy polysilicon gate is fabricated and is removed and replaced by a metal gate only after the silicides are formed [19].

As discussed earlier, reducing access resistance is crucial for improving the frequency performance of GaN HEMTs. Given that it is currently difficult to grow AlGaN/GaN heterostructures with sheet resistances less than 250 Ω/□, the most effective way of reducing these access resistances is to reduce the source-gate and drain-gate

distances. Due to lithographic constraints, self aligning the drain and source to the gate is the most reproducible and robust way of reducing these access resistances. Therefore, there is great interest in developing self-aligned AlGaN/GaN HEMT technology.

One of the key challenges in a self-aligned GaN technology is to develop a gate stack that can survive the ohmic anneal. During the last few years, several research groups have developed different techniques for overcoming these challenges.

C-H. Chen et al from UC Santa Barbara demonstrated self-aligned AlGaN/GaN HEMTs which were fabricated through an ohmic regrowth process [20]. After fabricating a dummy SiO_2 gate on top of an AlGaN/GaN substrate, they etched away the AlGaN buffer while using the SiO_2 gate as an etch mask. Then, SiN spacers were deposited and GaN was regrown everywhere that was not covered by the SiO_2 gate. After the regrowth, the dummy gate was etched away and a metal gate was deposited. The regrown ohmic contacts allowed for a lower on-resistance.

A. Basu et al. from the University of Illinois developed a new ohmic metallization scheme that is composed of Mo/Al/Mo/Au [21]. After a pre-deposition $SiCl_4$ plasma treatment with a DC Bias of -300V and a $HCl:H_2O$ rinse, they deposited Mo(10 nm)/(Al 40 nm)/Mo(20nm)/Au(30nm) and annealed the contacts at 500°C for different times ranging from 30s to 4 min. The optimized ohmic contacts were annealed for 3 min at 500°C and had a contact resistance of 0.11 Ω-mm. V. Kumar et al used the Mo/Al/Mo/Au ohmic metallization scheme in order to fabricate self-aligned AlGaN/GaN HEMTs [22]. The gate overhangs of the T-gates were used as a shadow mask for the ohmic metallization. Given that the anneal temperature was 500°C, the Ni/Au T-gate survived the ohmic anneal. Also, the lower anneal temperature allowed for smooth

ohmic contacts, which prevented shorting as shown in Figure 7.

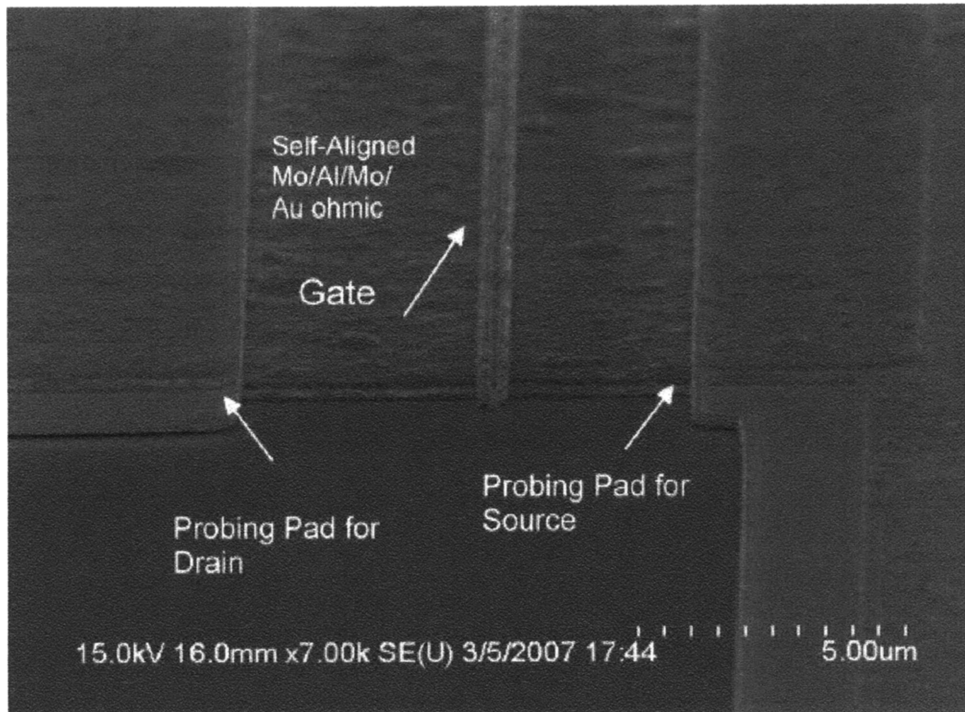


Figure 7: SEM image of 250 nm self-aligned gate with Mo/Al/Mo/Au ohmic contacts [22]

These devices had a gate length of 250 nm and a contact resistance of 0.35-0.6 Ω-mm. The f_T of these devices was 88 GHz and the f_{max} was 103 GHz. Non-self aligned devices were also fabricated on the same wafer and these devices had an f_T of 52 GHz and f_{max} of 85 GHz, which the authors attributed to the rise in source resistance from 5.7 Ω for the self-aligned devices to 9.4 Ω for the non-self-aligned devices.

There are other approaches towards fabricating self-aligned AlGaN/GaN HEMTs. J.Lee et al. used a double ohmic metal approach where they first put down non-self aligned ohmic contacts, annealed them, patterned the T-gate and then deposited a thin layer of Ti/Al/Ni/Au and then annealed at 750°C as shown in Figure 8[23]. However, the contact resistances were high at 0.95 Ω-mm which increased the total resistance and thus the f_T of a HEMT with a 0.25 μm long gate was only 38 GHz.

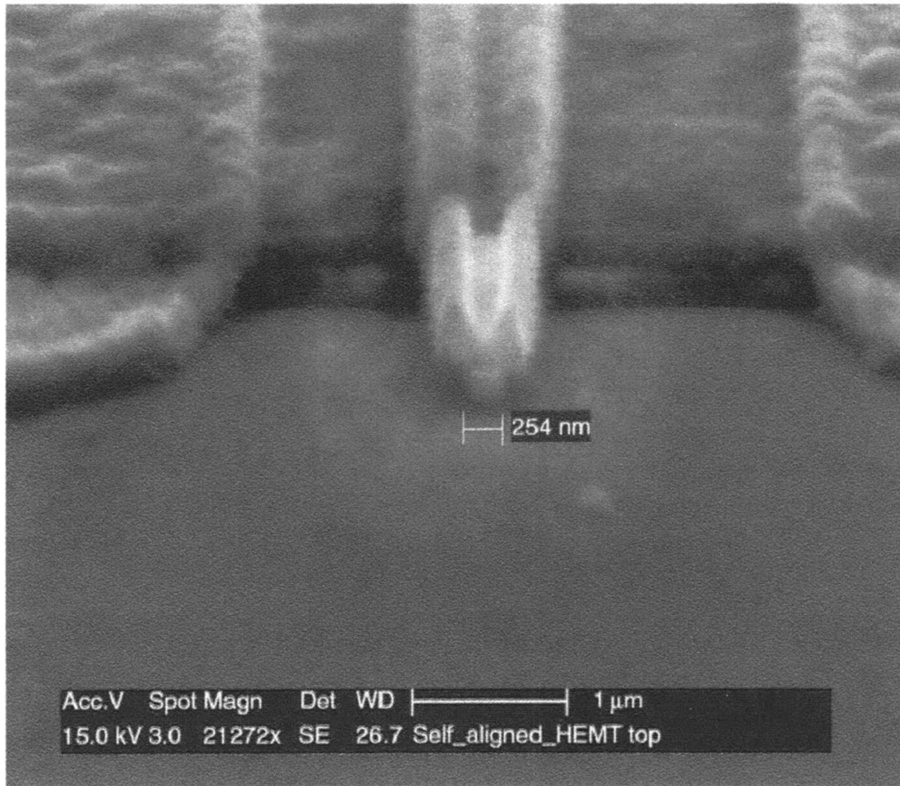


Figure 8: Schematic showing double ohmic metal process as described in [23]

J.S. Moon et al. of Hughes Research Lab (HRL) used an n^+ GaN source contact ledge in order to reduce the source access resistance [24]. An n^+ cap layer was grown in-situ on top of the AlGaN/GaN heterostructure. A source side contact ledge was defined in order to have a doped ledge extending from the source side. The n^+ cap layer was then etched away from the drain side in order to preserve high breakdown voltages and the maintain f_{max} values. After the ohmic contacts were patterned, 140 nm long gates were defined through the use of e-beam lithography. In comparison to devices without a n+ source ledger, the extrinsic transconductance increased from 350 mS/mm to 425 mS/mm and f_T increased from 50 GHz to 55 GHz.

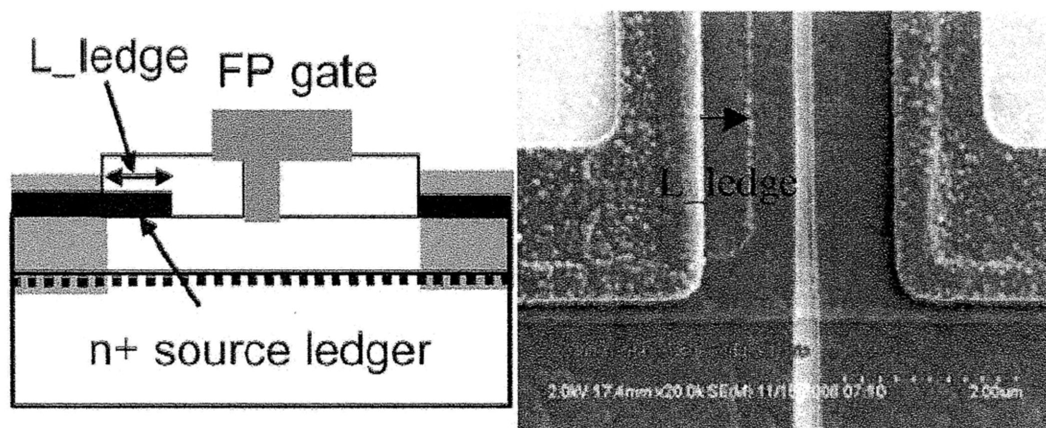


Figure 9: Schematic and SEM figure of device with n+ source ledger [24]

Recently, Nidhi et al demonstrated self-aligned HEMTs fabricated on N-face GaN HEMTs [25]. Cr/W/SiO_2 gates were first defined on the substrate and then SiN sidewalls were deposited, as shown in Figure 10. Then, graded InGaN was grown everywhere and non alloyed ohmic contacts were deposited in order to form the source and drain. As a result of the graded InGaN contacts, there was no energy barrier for electrons to get injected from the metal contacts to the GaN channel, as shown in Figure 11. The absence of an energy barrier contributed to a very low contact resistance in these transistors (i.e. 0.023 Ω-mm), which in turn contributed to the high on current of 2.3 A/mm. The f_T of these 130 nm gate devices was 132 GHz while the f_{max} was 17 GHz, which the authors attributed to the high resistance of the gate metal.

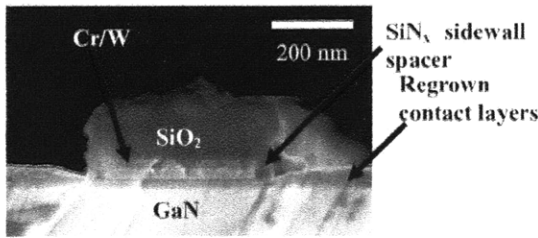


Figure 10: SEM cross section of HEMT described in Nidhi et al [25]

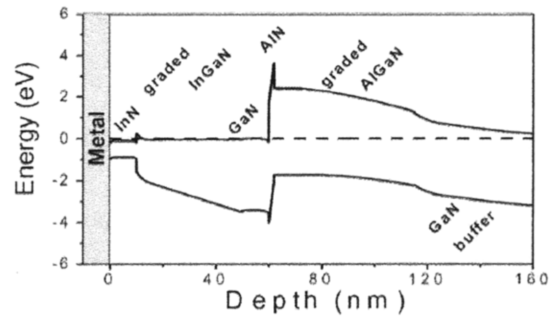


Figure 11: Band diagram of the access regions in the devices described in Nidhi et al. The lack of an electron barrier contributes to the low contact resistance and allows for non-alloyed ohmic contacts [25]

As summarized above, there has been substantial work on developing self-aligned transistors but all these approaches have tradeoffs. In the case of the low temperature ohmic process, these devices are limited in terms of the ohmic metallization scheme that can be used and the ohmic contact resistance is typically higher than in standard HEMTs. The devices described by Nidhi et al. were fabricated on N-face GaN/AlGaN heterostructures, which have a higher sheet resistance (600 Ω/□) than state of the art Ga-face AlGaN/GaN heterostructures (300-400 Ω/□). It also requires an epitaxial regrowth step which adds cost and complexity to the final device fabrication.

Therefore, the work in this thesis is aimed at developing technologies that will enable self-aligned transistors that can be processed at high temperatures on Ga-face heterostructures in order to reduce the source and drain access resistances without sacrificing process latitudes. There are three key parts necessary to achieve this:

1. Developing a gate dielectric to reduce the gate leakage of ultra-scaled transistors.
2. Developing a gate stack that can survive a standard (870ºC) high temperature ohmic anneal

3. Characterizing and optimizing the reduction in sheet resistance that can be achieved by depositing and annealing thin films of Ti on top of the source and drain access regions. These source and drain access regions would be very similar to the silicided contacts found in modern silicon MOSFETs.
4. Integrating the high temperature gate process with these thin Ti films to fabricate self aligned AlGaN/GaN HEMTs

The work described in this thesis describes all of the above. In Chapter 2-4, we discuss the development of a W/high-k dielectric gate stack that is capable of surviving the 870°C ohmic anneal. Chapter 2 describes the fabrication of devices with W/high-k dielectric gate stacks, Chapter 3 describes the characterization of the dielectric through the use of capacitor structures and Chapter 4 details the characterization of HEMTs with the W/high-k dielectric gate stack. In Chapter 5, work on reducing sheet resistance by depositing and annealing thin Ti based alloys is discussed and Chapter 6 describes preliminary work related to the fabrication self-aligned AlGaN/GaN transistors with these thin metal films.

Chapter 2: Fabrication of W/high-k MOS Devices

In order to fabricate self-aligned transistors, it is necessary for the gate stack to survive the high temperature ohmic anneal. Since conventional Ni/Au/Ni gates do not survive the high temperature anneals, it is necessary to develop W/high-k gate stacks. In this work, devices were fabricated on AlGaN/GaN structures that were grown by Nitronex Corporation by Metal Organic Chemical Vapor Deposition (MOCVD). The AlGaN barrier had an Al concentration of 26% and was 17 nm thick. The barrier was capped by a 2 nm unintentionally doped GaN layer. Further details about the growth technology can be found in [26]. Both high electron mobility transistors (HEMTs) and metal-insulator-semiconductor (MIS) capacitors were fabricated on these samples. We were interested in studying the effect of the dielectric on the interface between the gate and the semiconductor. In this chapter, we will describe the fabrication of MOS capacitors and transistors to study the dielectric properties. In Chapter 3, the results of the characterization of these capacitors is reported and in Chapter 4, the results of the transistor characterization are presented

First, mesa isolation was performed by electron cyclotron resonance (ECR) etching. After patterning the mesa isolation patterns with positive OCG-825 photoresist, the samples were etched with the conditions described in Table 1.

Table 1: Mesa etch properties

	Step 1	Step 2
BCl_3 (sccm)	10	20
Cl_2 (sccm)	0	5
Pressure (mTorr)	10	10
ECR (W)	100	100
RF (W)	25	25
Time	60	400

The high RF plasma power required to etch the GaN layers changed the properties of the photoresist and made it difficult to remove it with acetone. Therefore, the photoresist was removed by agitating in N-methyl pyrrolidone (NMP) for 15 min in a heated 40°C water bath. After the resist was removed, then the samples were ready for depositing high-k dielectrics. By performing the mesa etch before the dielectric deposition, the sidewalls are also covered by the dielectric, as shown in Figure 12. Otherwise, the gate metal will be in contact with the Two-Dimensional Electron Gas (2-DEG) and cause significant gate leakage at pinchoff, as shown in Figure 13.

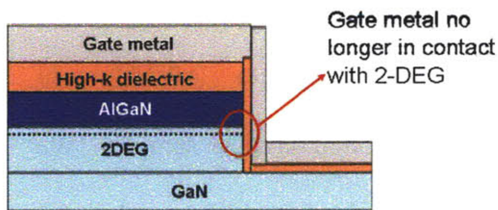


Figure 12: By depositing the dielectric after the mesa etch, the gate metal is not contacting the 2-DEG

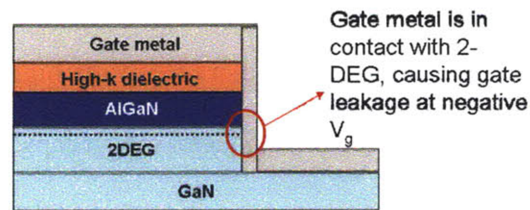


Figure 13: If the mesa etch is done after the dielectric deposition, there is no dielectric on the mesa side walls.

Seven samples were processed in order to assess the effect of different dielectrics compositions, as shown in Table 2.

Table 2: Summary of Gate Dielectrics and Fabricated Devices

Al_2O_3	HfO_2	$Ga_2O_3 + HfO_2$
15 nm	15 nm	3 nm + 12 nm
20 nm	20 nm	
25 nm	25 nm	

For the Al_2O_3 and HfO_2 devices, the dielectrics were deposited by using a Savannah Cambridge Nanotech atomic layer deposition (ALD) reactor. ALD relies on a self-limiting reaction, which ensures uniform dielectric thicknesses [27]. Each cycle

involves four basic steps. First, a precursor is pulsed inside the chamber and some molecules are adsorbed on the surface of the substrate (a GaN sample, in this work). Then, the chamber is purged but the precursor still remains on the surface. After the chamber has been purged, then the second precursor is introduced and pumped down again [27].

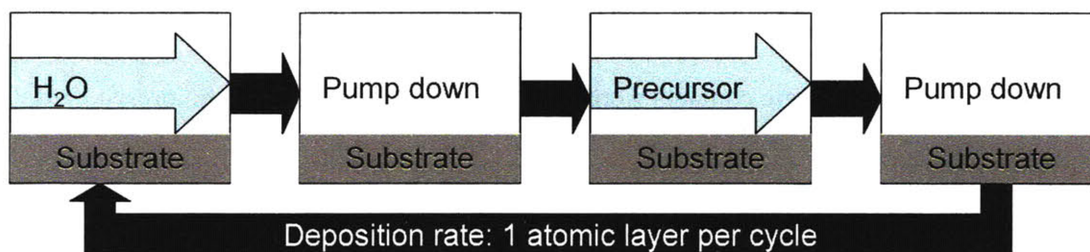


Figure 14: Schematic of Atomic Layer Deposition

The details of the depositions are detailed in Table 3.

Table 3: Details for ALD deposition

	Al_2O_3	HfO_2
Precursor # 1	DI- H_2O	DI- H_2O
Precursor # 1 pulse width	0.015s	0.015s
Precursor # 2	Trimethyl-aluminum	tetrakis dimethylamino-hafnium(IV)
Precursor # 2 pulse width	0.015s	0.3s
Time between pulses	5s	5s
Chuck Temperature	250	250
# Cycles for 20 nm	180	215

In one sample a thin Ga_2O_3 interfacial layer was grown by oxidizing in a barrel asher with a 1000 W oxygen plasma. Details for the oxygen plasma growth can be found in [28].

In order to verify the thickness of the Al_2O_3 and HfO_2 deposited in the ALD reactor, a J.A. Woolam spectroscopic ellipsometer was used [29]. Along with the AlGaN/GaN sample, a dummy piece of silicon was placed in the ALD reactor during each run. We used the ellipsometer to measure the thickness of the dielectric films

deposited on the silicon samples, with the assumption that the deposition rate of these high-k dielectrics was the same on silicon as on AlGaN and GaN. For the measurements, the sample was positioned at a tilt of 55, 65 and 75 degrees and different wavelengths of light ranging from 300 nm to 1000 nm were used at each of those tilts.

After the dielectric deposition, the gate pads were patterned by using AZ 5214 photoresist. 60 nm of tungsten was deposited by e-beam evaporations and the metal was lifted-off. Then, the ohmic contacts were patterned by using AZ 5214 photoresist. After the resist patterning, the dielectric was etched away by a 7:1 buffered oxide etch (BOE). For etching away the Al_2O_3 films, the sample was dipped in BOE for 30 s while the samples with HfO_2 films were dipped in BOE for anywhere from 6-8 min, depending on the thickness of the HfO_2 films. After the dielectric was removed, ohmic contacts consisting of 200A-Ti/1000A-Al/250A-Ni/500A-Au were deposited by electron-beam evaporation and then lifted-off. Finally, the ohmic contacts were formed by annealing the sample at 870°C for 30 s in an N_2 environment.

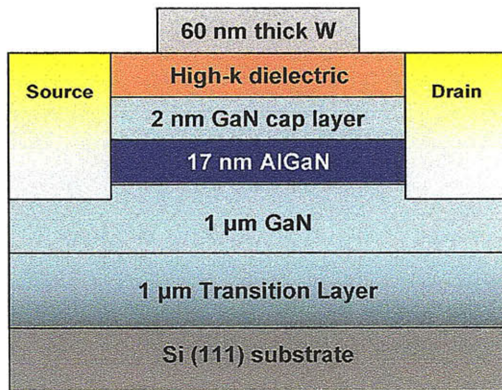


Figure 15: Finished device structure

Chapter 3: Characterization of W-high-k capacitors

In order to gain a better understanding of how the W-high-k gate differed from the standard Schottky Ni-Au-Ni rectifying gate, we fabricated capacitor structures as described in Chapter 3 (Figure 16). Diode IV measurements allowed us to understand the amount of gate leakage present in these devices, which we used to study the integrity of the gate insulator after a high temperature annealing. The high temperature anneal is necessary for forming ohmic contacts and also improves the quality of the dielectric/gate interface. Capacitance-voltage measurements allowed us to study the density of interface traps between the semiconductor and insulator, which was key to understand the effect of the insulator on the transistor behavior.

For the IV measurements, we used an Agilent 4155C Semiconductor Parameter Analyzer and the voltage was swept from a negative bias to a positive bias. The diode measurements for diodes with 15 nm of dielectric together with a diode without a dielectric are shown in Figure 17.

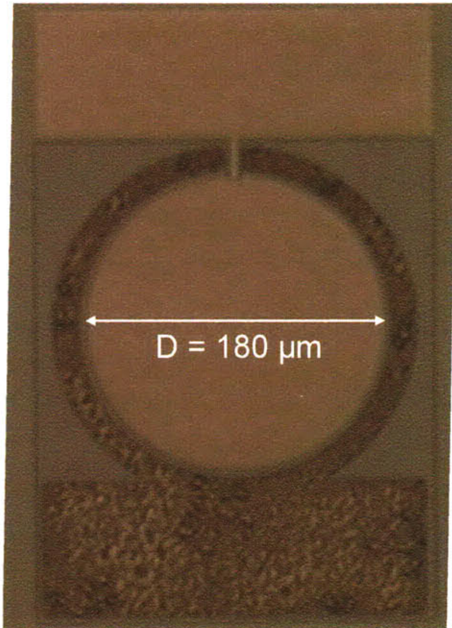


Figure 16: Picture of capacitor structure used for IV and capacitance measurements

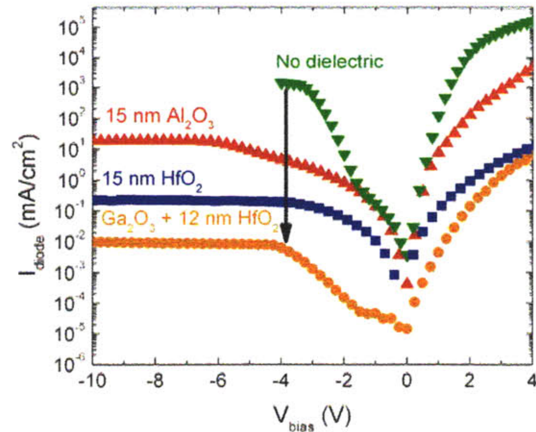


Figure 17: Diode measurements for diodes with 15 nm of dielectric and diode without dielectric layer. Note the 10000 X reduction in gate leakage for the diode with Ga_2O_3 + HfO_2

The diode structures with a dielectric exhibit a significant reduction in diode leakage compared to the Schottky diode. The reduction in the reverse bias leakage helps improve the reliability of these devices while the reduction in the forward bias leakage allows for applying for more positive gate voltages, which in turn increases the drain current densities

We then performed capacitance-voltage measurements by using an Agilent 4294A Impedance Analyzer with the parallel equivalent capacitance-parallel equivalent conductance measurement setting (C_p-G) [30]. For the purpose of the capacitance measurements, the oscillation voltage level was set to 50 mV. These transistors were measured at oscillation frequencies ranging from 500 Hz to 1 MHz. While the measured oxide capacitance did not change much as a function of frequency, the data shown in the subsequent figures correspond to an oscillation frequency of 20 KHz, unless otherwise

noted. The DC bias was swept from -10 V to 1 V. As shown in Figure 18, as the DC voltage bias is swept from negative bias to positive bias, the capacitor goes from depletion to accumulation. When the carriers in the 2-DEG are present, we are able to measure the capacitance of the oxide and the AlGaN layer. On the other hand, when the carriers are depleted from the carrier due to the negative bias, the measured capacitance is close to zero due to the absence of carriers in the 2-DEG. These measurements were performed on capacitor structures with different dielectric thicknesses, as shown in Figure 19.

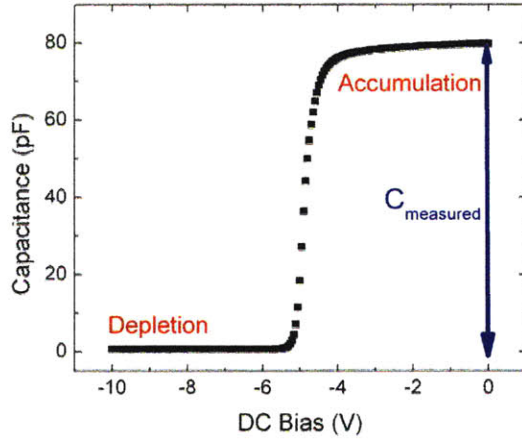


Figure 18: Capacitance-Voltage measurement for capacitor with 15 nm HfO_2 dielectric.

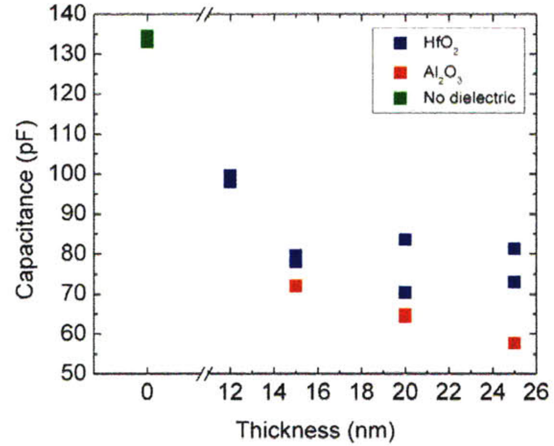


Figure 19: Measured Capacitances (as defined in Figure 18) vs. dielectric thickness

Neglecting the quantum capacitance, the total capacitance is composed of the capacitance of the AlGaN and the capacitance of the oxide, and it can be expressed by the following sum:

$$\frac{1}{C_{measured}} = \frac{1}{C_{ox}} + \frac{1}{C_{AlGaN}}$$

The capacitance of the oxide is given by:

$$C_{ox} = \frac{Ak\varepsilon_0}{t_{ox}}, \varepsilon_0 = 8.85 \times 10^{-12} F/cm$$

In the expression above, A is the area of the capacitor, ε_0 is the permittivity of free space, k is the dielectric constant and t_{ox} is the thickness of the oxide. As shown in Figure 21, we extracted the dielectric constant k for both HfO_2 and Al_2O_3. The dielectric constant for HfO_2 was determined to be 18.1 while the dielectric constant of the Al_2O_3 gate dielectric was around 10.8

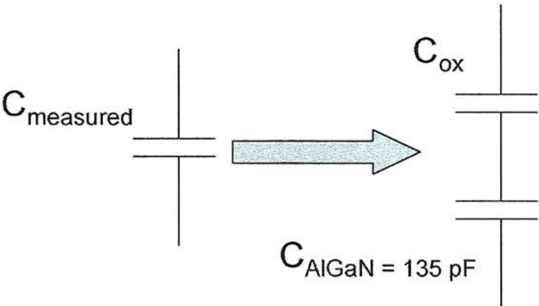


Figure 20: Schematic showing how measured capacitance is composed of the capacitance of the AlGaN layer and the capacitance of the oxide

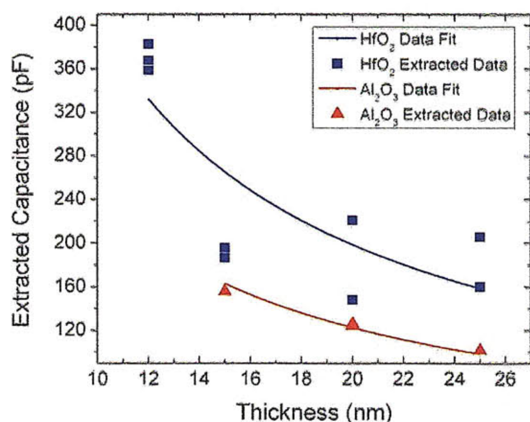


Figure 21: Extracted capacitances after accounting for capacitance of AlGaN. As per the data fit, the dielectric constant for Al_2O_3 is 10.8 and for HfO_2 is 18.1

The hysteresis was also measured in these capacitors by sweeping the DC bias from -10V to 0V and back to -10V. These hysteresis measurements were performed with a small signal frequency of 20 KHz and small signal voltage of 50 mV. As shown in Figure 22, the hysteresis of the capacitors with Al_2O_3 increased as a function of dielectric thickness.

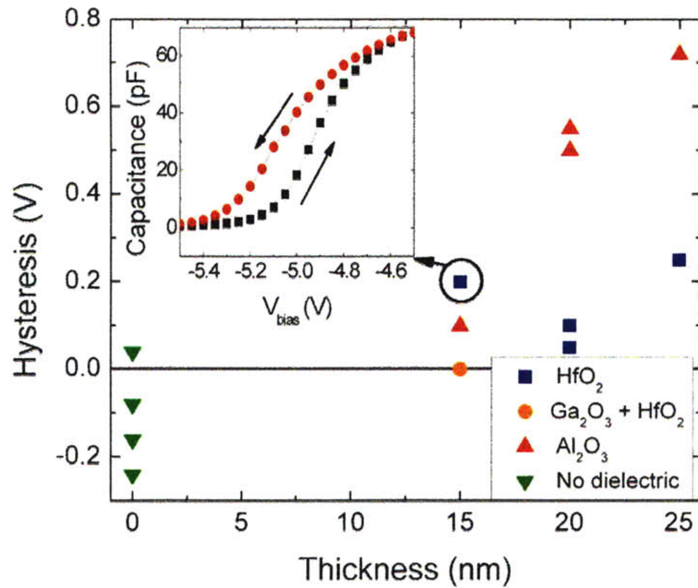


Figure 22: Hysteresis vs. Dielectric Thickness for different oxides. The inset shows an example of hysteresis

Hysteresis in MIS capacitors has been associated with slow traps with time constants as long as seconds [31]. From the measurements shown in Figure 18, Al_2O_3 based capacitors have more slow traps than HfO_2 based capacitors. It is also noteworthy that the hysteresis for the Al_2O_3 based capacitors increases as a function of dielectric thickness while there is no such correlation for the HfO_2 capacitors.

In order to get a better sense for high frequency traps, we used the conductance method in order to extract the concentration of interface traps [32]. As stated earlier, the impedance of these capacitors was modeled by the parallel capacitance – conductance method. A characteristic measurement curve is displayed in Figure 23. The peak of the conductance corresponds to the voltage level where there is the most charging and discharging of the interface states.

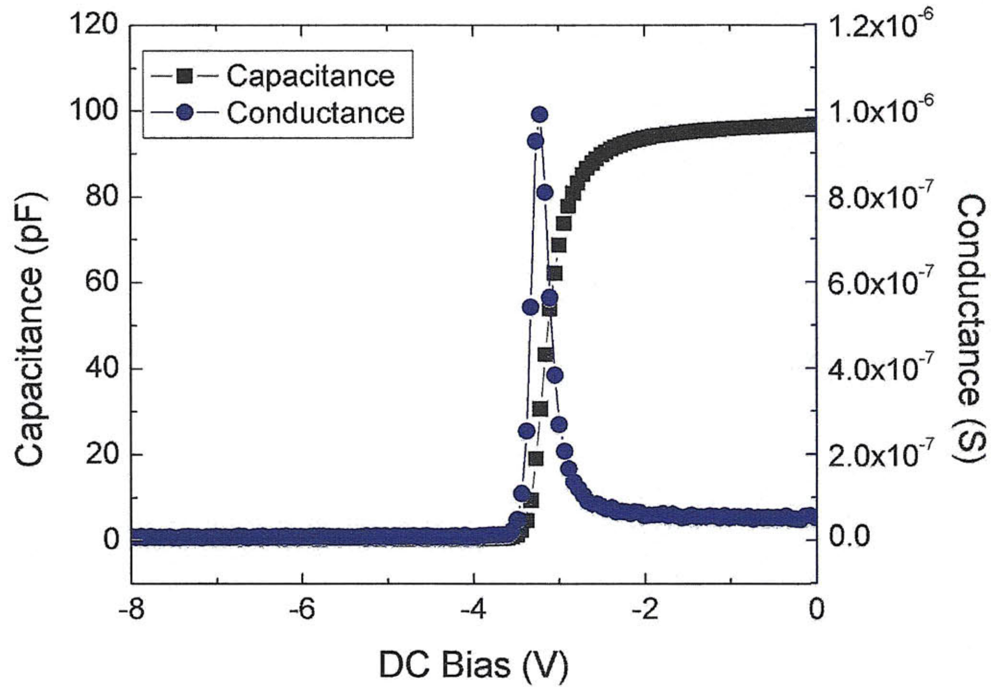


Figure 23: Characteristic capacitance-voltage and conductance-voltage curves for capacitor with Ga_2O_3 + HfO_2 dielectric. The peak conductance point is around -3.6 V and the oscillation frequency is 20 KHz.

We performed Conductance-Voltage measurements over a wide range of frequencies starting from 500 Hz to 1 MHz. An approximate expression relating the density of traps to the parallel conductance is:

$$D_{it} \approx \frac{2}{Aq}\left(\frac{G_{p,\max}}{\omega}\right)$$

Figure 24 shows a plot of D_{it} vs. frequency for all the capacitors and Figure 25 shows the maximum D_{it} for these devices. As shown in Figure 24, the capacitors with Al_2O_3 oxide is dominated by slow traps while the capacitors with Ga_2O_3 and HfO_2 exhibited fast traps. R. Stoklas et al. also reported that there are both slow and fast traps in Al_2O_3 based HEMTs [33], which is consistent with what we observe for Al_2O_3 based capacitors.

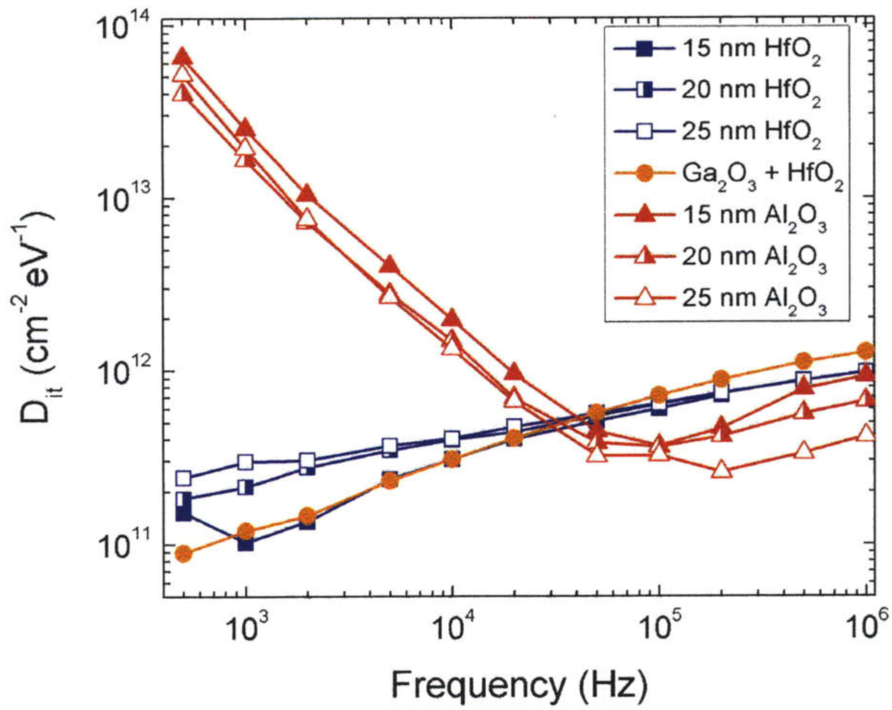


Figure 24: Plot of D_{it} vs. frequency for the different capacitors analyzed in this work.

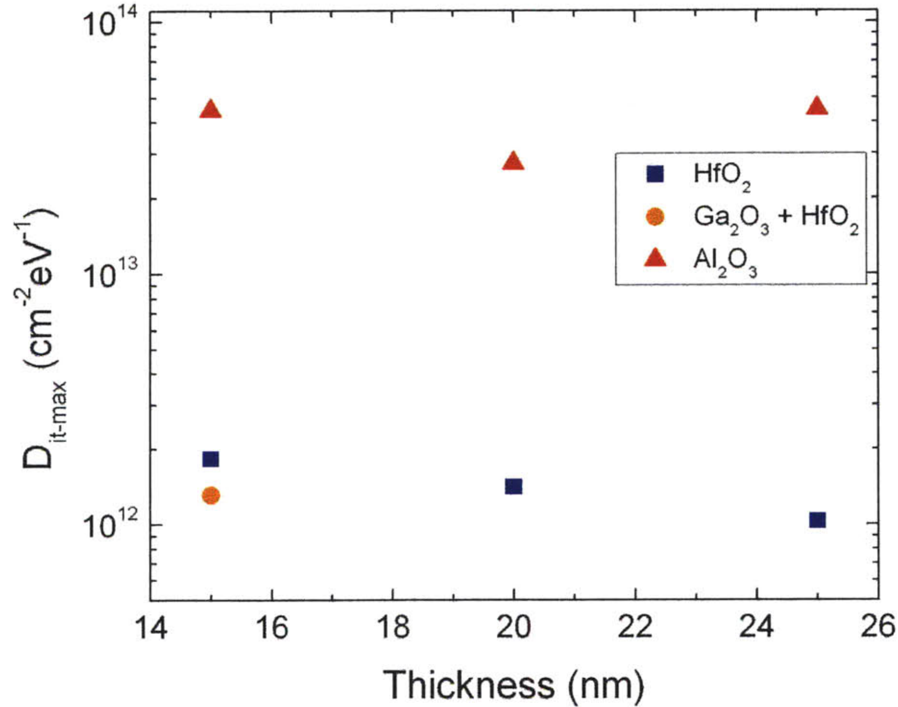


Figure 25: Maximum D_{it} for Capacitors with different dielectrics

Chapter 4: Characterization of W/high-k HEMTs

Section 4.1: Hall Measurements

As noted earlier, self aligned transistors require gates that can survive high temperature anneals. Therefore, we fabricated transistors with W/high-k dielectrics in order to test gates that were annealed with the ohmic contacts.

From transfer length measurements (TLM), we observed that the samples with dielectrics had sheet resistances of around 300 Ω/□, which was 10 % lower than the samples without dielectrics. In order to investigate the cause of the reduction in sheet resistance, we used Hall measurements to see the change in carrier concentration, mobility and sheet resistance resulting from depositing dielectrics on the samples. We did Hall measurements on 1 cm × 1 cm samples before and after dielectric deposition. Figure 28 shows the reduction in sheet resistance that results from depositing the different dielectrics on the samples. These results seem to indicate that the decrease in sheet resistance is due to an increase in carrier concentration as opposed to a change in electron mobility. It has been reported that Al_2O_3 dielectrics lead to mobility enhancement due to passivation effects [34]. It is also noteworthy that the thicker films result in a smaller reduction in sheet resistance. The reduction in sheet resistance may be due to both strain effects and mobility enhancement but the origins of this needs to be explored further.

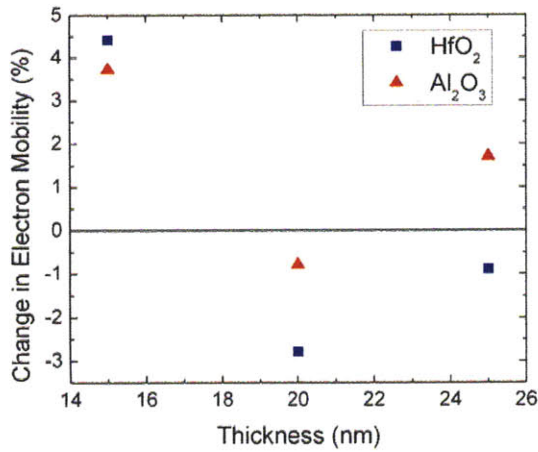


Figure 26: Change in Hall Mobility after dielectric was deposited on samples

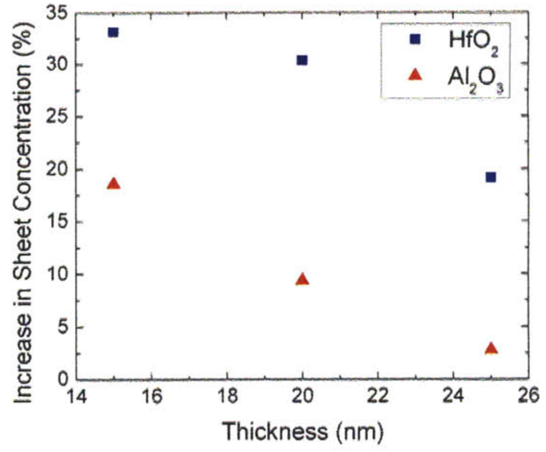


Figure 27: Change in Sheet Concentration after dielectric was deposited on samples

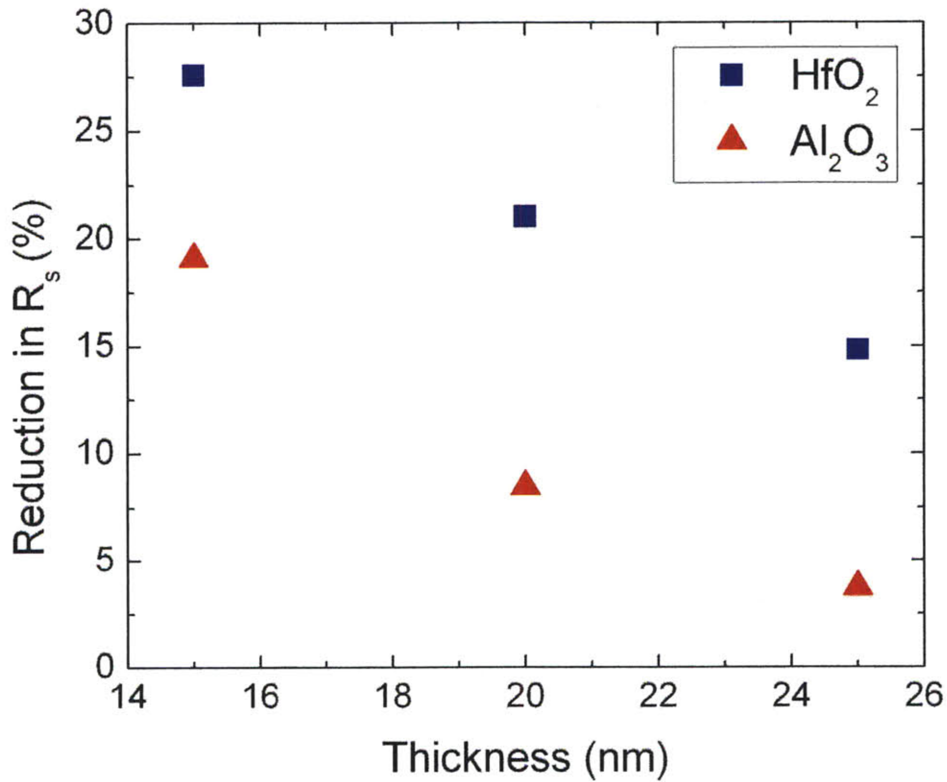


Figure 28: Reduction in sheet resistance, as measured by Hall measurements, after depositing dielectric on samples

Section 4.2: DC Characterization of W/higk-k HEMTs

After fabricating the HEMTs, an Agilent 4155C was used to measure the I_{ds}-V_{ds} output characteristics for the samples with the different dielectrics. Figure 29 shows representative output characteristic for the HEMT with Ga_2O_3 + 12 nm of HfO_2. In order to characterize the highest current densities possible for these devices, the gate voltage of each transistor was swept for the highest possible gate voltage without the gate leakage exceeding 0.1 mA/mm. As shown in Figure 30, the HEMTs with the gate dielectric have 30-40% higher $I_{ds,max}$ than in the standard devices since higher gate voltages can be applied.

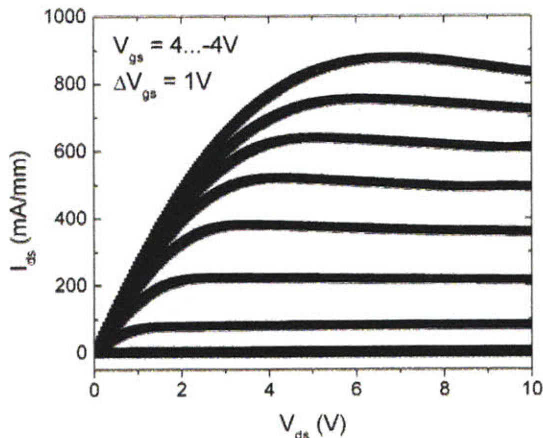


Figure 29: Id-Vds characteristics for HEMT with Ga_2O_3 + HfO_2 gate dielectric

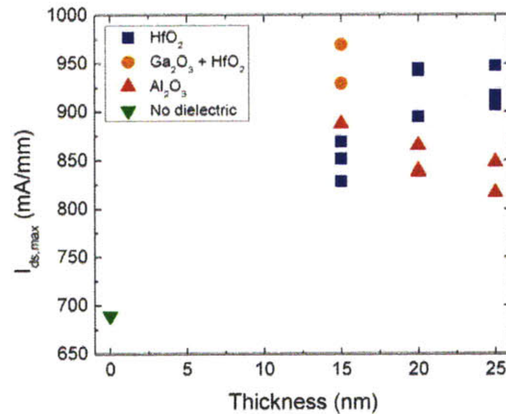


Figure 30: Maximum drain current densities vs. dielectric thickness. Currents measured at the highest V_{gs} where $I_g < 0.1$ mA/mm

We measured the threshold voltages of the HEMTs by sweeping the gate voltage as shown in Figure 31. We defined the threshold voltage as the gate bias point where $I_{ds} \leq 1$ mA/mm. As the dielectric thickness got thicker, the threshold voltage decreased since the gate capacitance was lower and a more negative voltage was required in order to deplete the 2-DEG

It is also noteworthy that the $I_{ds,max}$ for the HfO_2 HEMTs increases with the dielectric thickness while the $I_{ds,max}$ for the Al_2O_3 HEMTs decreases with the dielectric thickness. This behavior can be explained by considering the following expression for the maximum drain current:

$$I_{DS,\max} \propto \mu_e C_g \frac{W_g}{L_g}(V_{GS,\max} - V_T)^n$$

When we increase the gate dielectric thickness, the gate capacitance decreases but the available gate voltage swing increases since the maximum gate voltage is higher due to the lower forward gate bias. Therefore, assuming that the electron mobility is not a function of the dielectric thickness, the total current for a transistor with thicker dielectric can either increase or decrease with respect to the case of thinner dielectrics, depending on whether the rate of decrease in the capacitance is higher or lower than the rate of increase in available gate voltage swing. In the case of HfO_2, our measurements show that the gate voltage swing increases 52% when the HfO_2 thickness varies from 15 nm to 25 nm as shown in Figure 32. In the same devices, the capacitance only drops by 12%. This difference explains the 8% increase in the maximum current density in these devices. In Al_2O_3, however, the available gate voltage swing does not increase as much with dielectric thickness (only 26% when going from 15 nm to 25 nm) and the capacitance drops by 20% since Al_2O_3 has a lower dielectric constant. These two effects explain why the maximum current decreases with the thickness of Al_2O_3.

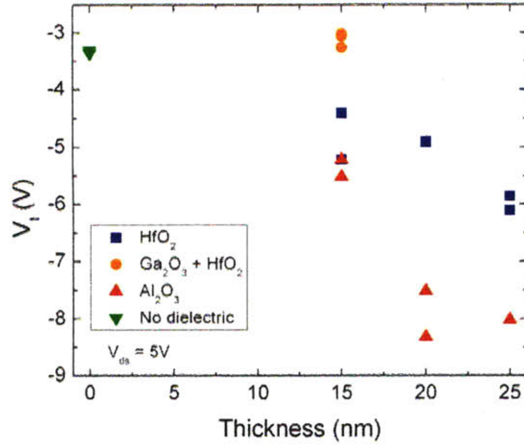


Figure 31: Threshold voltages for the different HEMTs. Vt is defined as Vg where Ids = 1 mA/mm with Vds = 5V.

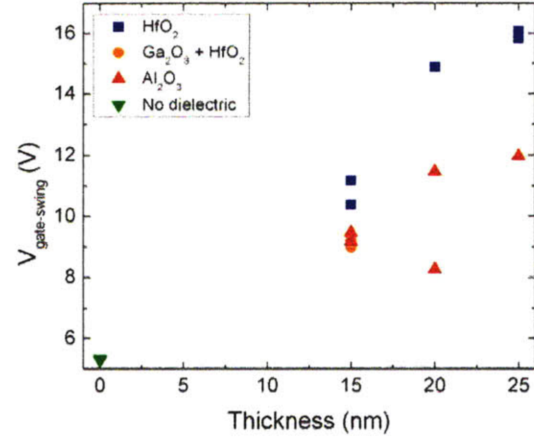


Figure 32: Available gate swing of the different HEMTs.

In addition, the transconductance of the HEMTs was measured by sweeping the gate voltage and holding the drain voltage constant. The drain current density changes as the gate voltage changes and the rate of change of the drain current density as a function of the gate voltage is the transconductance,

$$g_{m,e} = \frac{\partial i_{ds}}{\partial v_{gs}}$$

The transconductance is a measure of the gate modulation, which in turn is correlated with the frequency performance of transistors. To a first approximation, the unity gain frequency, f_T, can be expressed as the following [35]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

As shown in Figure 34, the transconductance of the MIS devices is higher than what would be expected considering the lower gate capacitance, even after taking the decrease in sheet resistance into account.

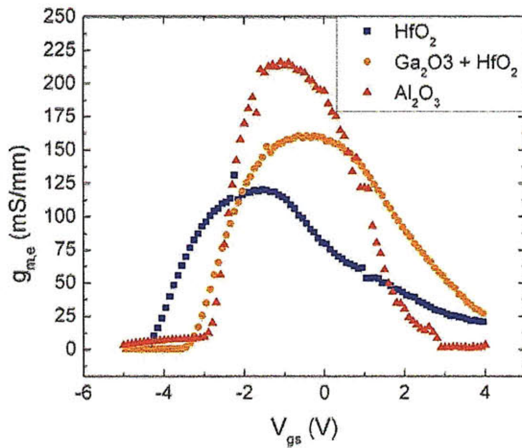


Figure 33: The transconductance of MIS devices with 15 nm of gate dielectric. The Al_2O_3 devices had the highest transconductance despite having the lowest gate capacitance. The Vds was 5 V.

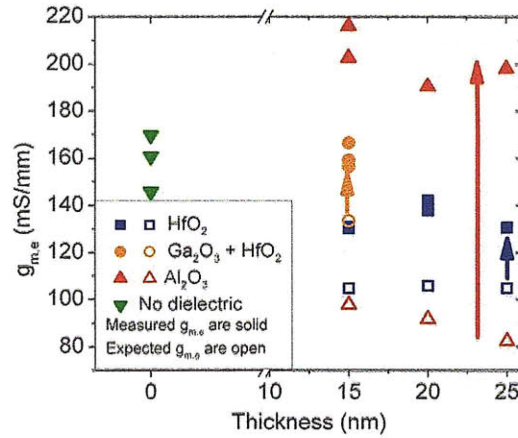


Figure 34: The transconductance of different MIS devices with different dielectric materials and thicknesses. The transconductance for MIS devices is higher than what can be expected

The intrinsic transconductance can be calculated by the following expression [36]:

$$g_{m,i} = \frac{g_{m,e}}{1 - R_s g_{m,e}}$$

The increase in the extrinsic transconductance is due to both the increase in the intrinsic transconductance and the decrease in the sheet resistance. The calculated instrinsic transconductance for the different devices is shown in Figure 35. Given that the instrinsic transconductance can be expressed as $g_{m,I} = C_{gs} \times v_e(E)$, we can see that there needs to be an increase in the relative electron velocity. The relative increase needed in order to help explain the increase in intrinsic transconductance is shown in Figure 36.

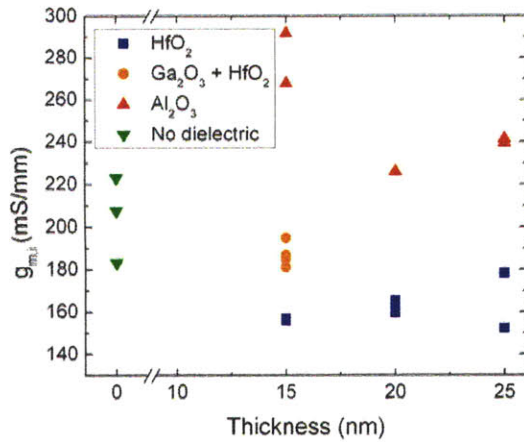


Figure 35: The maximum intrinsic transconductance of MIS devices. The Vds was 5 V.

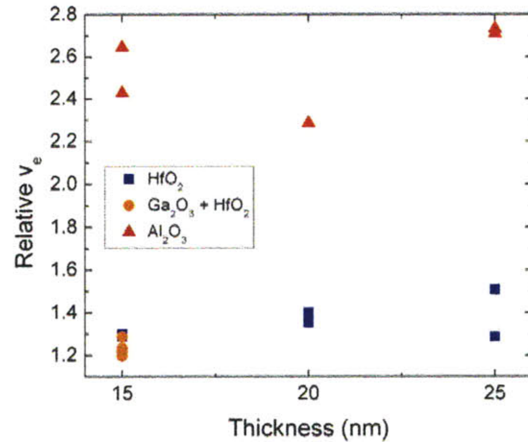


Figure 36: The relative increase in electron velocity necessary to justify the intrinsic transconductances of the MIS devices

Other groups have also reported an increase in transconductance and electron velocity due to the presence of gate dielectrics. Levinshtein et al. reported an experiment where they fabricated MOSHFETs with a 7 nm SiO_2 gate dielectric and HFETs with a rectifying Pt/Au gate on two different substrates: one with a 10 nm AlGaN barrier and the other with a 25 nm barrier. While the mobility for the devices with the 25 nm barrier did not change with the presence of the oxide, the mobility for the MOSHETs was measured to be 1400 $cm^2/V/s$ but only 600 $cm^2/V/s$ for the devices with the 10 nm AlGaN barrier [37]. Kuzmik et al fabricated different HEMTs with a 10 nm thick ZrO_2 gate insulator, 10 nm thick HfO_2 gate insulator and without gate dielectrics on an InAlN/AlN/GaN substrate [38]. They found that the HEMT with the ZrO_2 gate insulator had $g_{m,e}$ of 110 mS/mm as opposed to 105 mS/mm for the HEMT without the gate insulator and 95 mS/mm for the HEMT with the HfO_2 gate insulator. More significantly, D. Gregusova et al. fabricated different AlGaN/GaN HEMTs without a gate dielectric and with a 4 nm thin Al_2O_3 gate dielectric and found that the HEMT with the 4 nm of Al_2O_3 had $g_{m,e}$ of 120 mS/mm compared to 65 mS/mm of $g_{m,e}$ for the HEMT without the gate dielectric

[39]. This is consistent with our observations of the high $g_{m,e}$ of the W/Al_2O_3 HEMTs. In order to explain the increase in transconductance for HEMTs with Al_2O_3 gate dielectrics, R. Stoklas proposed that there is an enhancement of the effective carrier velocity in AlGaN/GaN HEMTs with Al_2O_3 gate oxide resulting from the suppression of the trapping states [40]. This is consistent with the Pulse-IV/dispersion measurements made on our devices as described in Section 4.3.

Section 4.3: Pulsed IV Measurements of HEMTs

We performed Pulsed-IV measurements on our HEMTs in order to study the frequency dependent dispersion in our devices. Frequency dispersion is a very important phenomenon in nitride HEMTs. As shown in Figure 37, when the gate is pinched off, electrons fill the surface traps on the AlGaN and form a virtual gate that depletes the channel [41]. There is a time constant associated with the discharging of these surface traps and therefore, the formation of a virtual gate. Pulsed-IV measurements are useful for characterizing the density of surface traps and also the degree of passivation on the surface [42]. We performed Pulsed-IV measurements by measuring the drain current of these devices as the gate was pulsed at different pulse widths. Table 4 shows the pulse widths and periods used to characterize dispersion while Figure 38 illustrates the different timing periods.

Table 4: Different timing settings for Pulsed-IV measurements used in this work.

	500 μs	80 μs	200 ns
Pulse Width	500 μs	80 μs	200 ns
Period Width	1 ms	1 ms	10 μs
Duty Cycle	50%	8%	2%

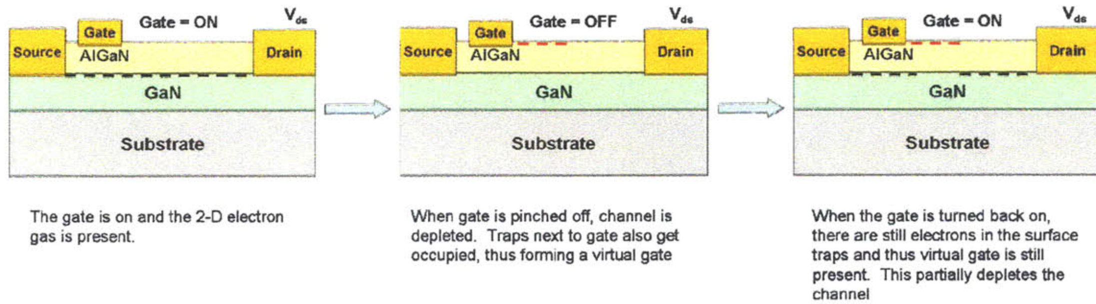


Figure 37: Formation of virtual gate and the resulting dispersion

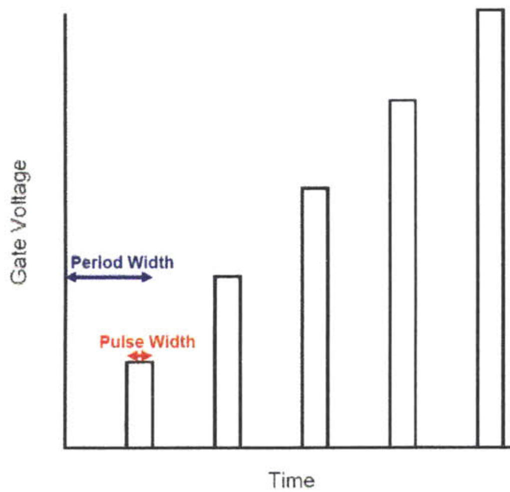


Figure 38: This timing schematic shows how the gate was pulsed as a function of time during the Pulsed-IV measurements

Figure 39 shows a general schematic for the experimental setup for the Pulsed-IV measurements. We used an Agilent 33250A signal generator in order to pulse the gate

while we supplied the Agilent E3631A DC power supply in order to apply a drain voltage. We measured the voltage difference across a 98 Ω resistor by using an Agilent 54642A oscilloscope. By knowing both the voltage difference across the resistor and the value of the resistance, we were able to compute the drain currents. Both the gate and the drain of the device were probed by using Picoprobe 40A-GSG-150-P probes with a 2.9 mm connector and a cutoff frequency of 40 GHz, which was much higher than the required bandwidth for the Pulsed-IV measurements.

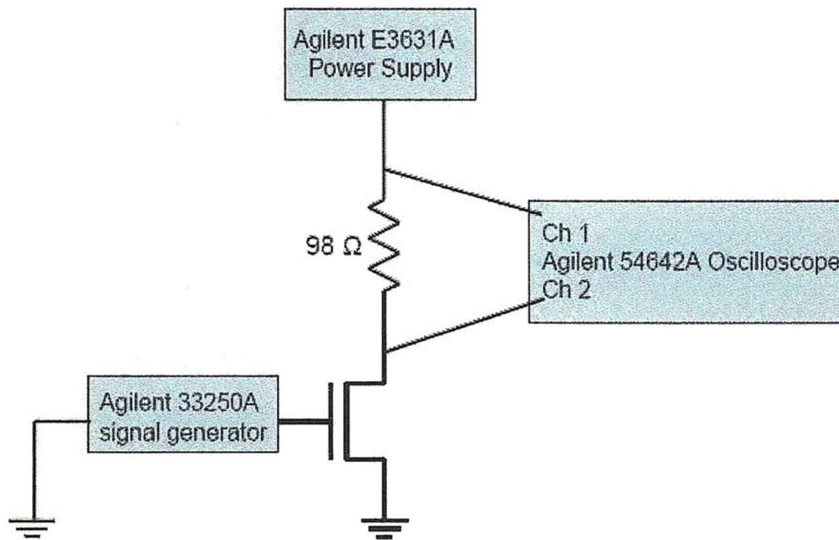


Figure 39: The measurement setup for Pulsed-IV measurements

Figure 40 shows the reduction in the drain current density as the gate pulse width was reduced from 1 ms to 200 ns. We can see that for the Al_2O_3 MIS HEMTs, the reduction in the drain current density is much less than that of the HEMTs without a dielectric or the HEMTs with HfO_2 dielectrics. Also, the amount of current collapse decreases as the dielectric thickness increases. The observed correlation between current collapse and dielectric thickness is consistent with what is observed for Si_3N_4 passivated devices [43]. Figure 41 shows the output characteristics of our devices with both 200 ns

pulsed gate bias and DC bias. The increase in current under the pulsed conditions demonstrates that the surface is well passivated by the Al_2O_3 in spite of the very small thickness of this passivation [40]. In contrast to the 80 nm of Si_3N_4 required to passivate the surface, 25 nm of Al_2O_3 is enough to allow for complete dispersion removal [43]. Thin passivation layers are desirable as they reduce the parasitic gate capacitances and thus improve frequency performance [44].

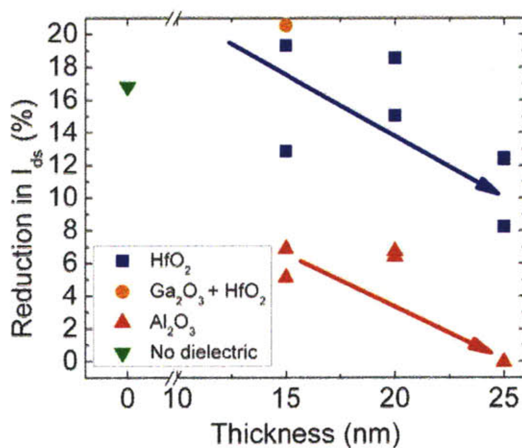


Figure 40: Reduction in drain current densities, resulting from the change in gate voltage pulse times from 1 ms to 200 ns. Note how increasing the thickness of the dielectrics improves the dispersion performance.

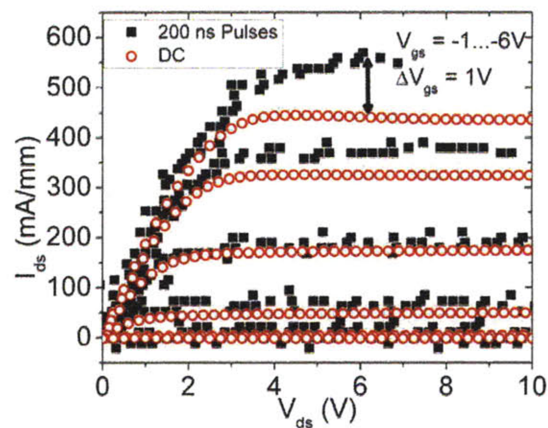


Figure 41: Output characteristics of 15 nm Al_2O_3 HEMT for both 200 ns pulsed gate bias and DC gate bias. The lack of current collapse demonstrates that e devices is well passivated.

It is interesting to note that Al_2O_3 based HEMTs exhibit much lower dispersion than the HfO_2 based devices despite having higher interface level traps. This can be explained by the fact that Al_2O_3 based devices are dominated by slow traps while in HfO_2 oxides fast traps dominate. More studies are currently underway which involve using Deep Level Transient Spectroscopy to study the nature of traps in Al_2O_3 and HfO_2 based devices.

Chapter 5: Development of a Silicide-like Access Region Metallization

Section 5.1: Material Properties of Ti-based Metallizations on AlGaN/GaN

Silicon based CMOS technology has been using metal silicides for source and drain contacts since the 1980's [18]. These materials have been key for fabricating self-aligned transistors with lower access resistances than transistors where the source and drain are composed simply of degenerately doped silicon. More importantly, these metal silicides have different chemical properties than the original metals, which enables highly selective wet etches in order to remove the unreacted metal.

GaN self-aligned transistors could benefit tremendously of a silicide-like technology. To develop this technology, it is instructive to look at the formation of ohmic contacts to GaN. Typically, ohmic contacts to AlGaN/GaN HEMTs are formed by alloying Ti/Al/Ni/Au metal stacks on top of the AlGaN layer. It has been reported that during the course of ohmic contact formation, the formation of TiN occurs [45]. As reported by multiple groups, the formation of TiN is key for the formation of ohmic contacts because TiN has a low workfunction and also because the formation of TiN forms nitrogen vacancies, which dopes the AlGaN barrier layer.

S.E. Mohney et al. performed experiments with Ti and TiN based ohmic contacts to GaN. They performed X-ray photoelectron spectroscopy (XPS) depth profiles of Ti on GaN contacts that had been annealed and they found that it was necessary to have TiN form in order to achieve ohmic contacts. This was attributed to the lower workfunction of TiN. However, when TiN was deposited directly on top of GaN and then annealed,

the contact resistances were higher. This was attributed to the fact that the direct deposition of TiN does not allow for the formation of nitrogen vacancies.

A.N. Bright et al. also performed transmission electron microscopy (TEM) based studies of Ti/Al/Ni/Au ohmic contacts in order to study the metallurgy and the formation of TiN and other metal phases [46]. Ohmic metals were deposited on three different samples, which were in turn annealed at 500°C, 700°C and 900°C. Then, the cross-sections of these ohmic samples were analyzed by TEM. They found that AlN and TiN formed at the interfaces, as shown in Figure 42 and Figure 43.

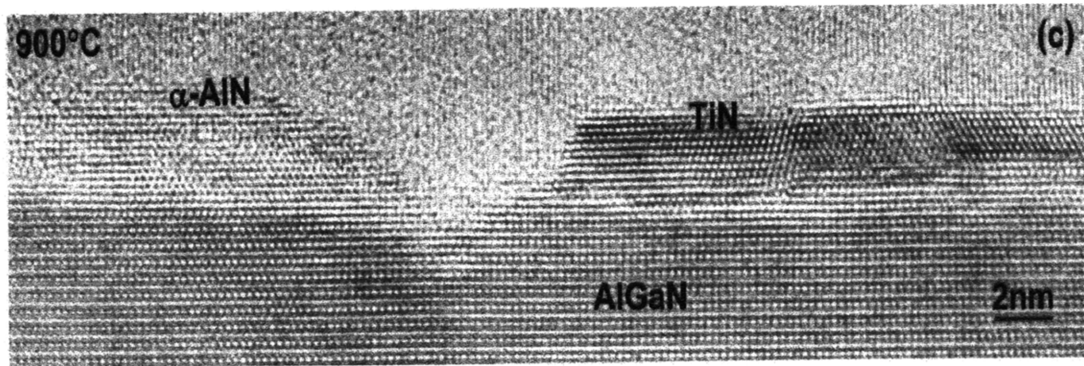


Figure 42: High resolution TEM of Ti/Al/Ni/Au contacts that have been annealed at 900°C. There is a TiN layer that formed at the interface [46].

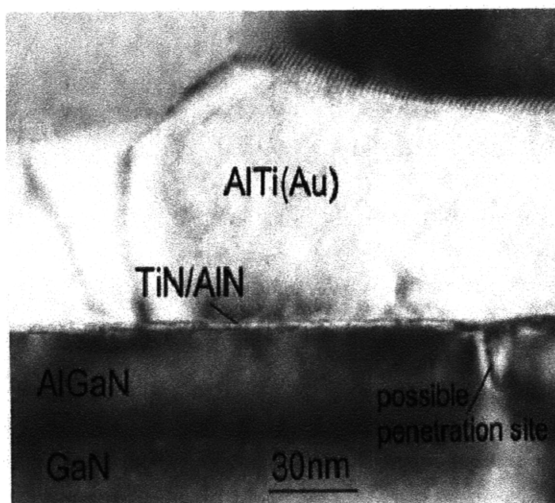


Figure 43: TEM image showing the formation of TiN. It is noteworthy that very little of the AlGaN was consumed in the anneal.

Section 5.2: Electrical Characterization of Ti-based Access Region Metallization

Based on these experiments, it is clear that depositing and annealing Ti on top of AlGaN/GaN heterostructures in the source and drain access regions is a promising way of reducing the access resistances. In order to characterize the reduction in sheet resistance, we fabricated different devices with transfer line method (TLM) patterns that are shown in Figure 44.

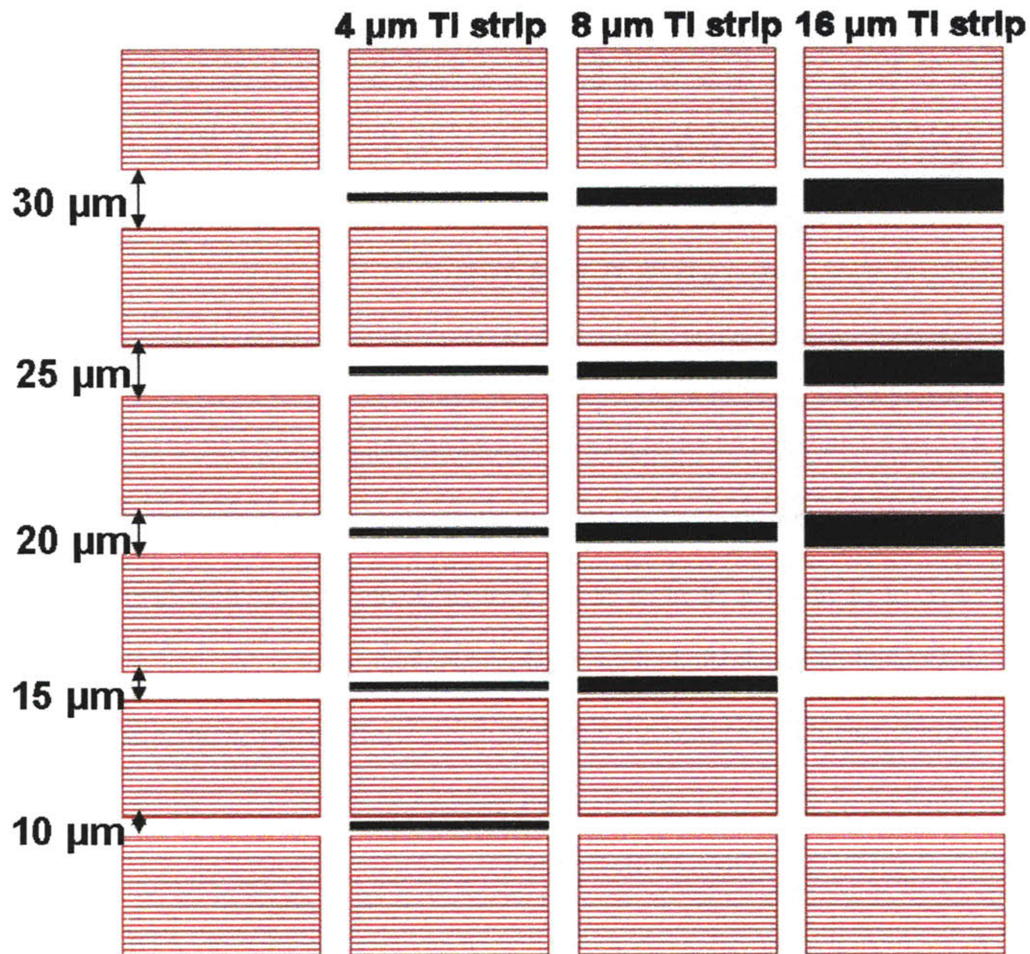


Figure 44: Schematic showing TLM pads used to measure the reduction in resistance due to depositng and annealing Ti. The pink squares are ohmic contacts and the black strips are the Ti strips

We performed a series of experiments in order to measure the reduction in sheet resistance that results from depositing and annealing Ti based metals. The total resistance that we measured can be modeled by the equivalent circuit shown in Figure 45.

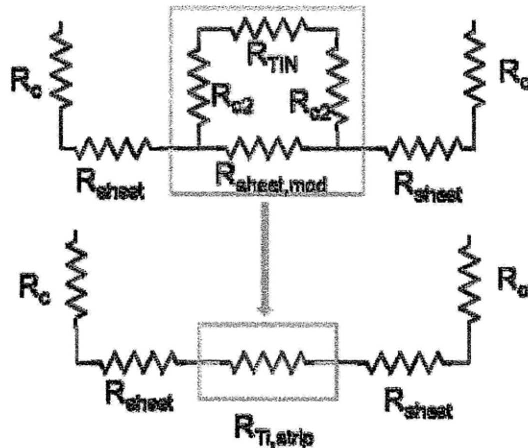


Figure 45: Model of the resistances in the Ti-doped regions

The top equivalent circuit is composed of 5 different resistances:

- R_c: This is the contact resistance of the ohmic contacts
- R_{sheet}: This is the sheet resistance of the AlGaN/GaN heterostructure
- $R_{sheet,mod}$: This is the sheet resistance of the AlGaN/GaN heterostructure underneath the annealed Ti region. This sheet resistance is different from R_{sheet} because when the Ti is annealed on top of the AlGaN, some of the AlGaN gets consumed as shown in Figure 42 and Figure 43
- R_{TiN}: This is the resistance of the TiN layer on top of the AlGaN
- R_{c2}: Given that the TiN is on top of the AlGaN layer and that the 2-DEG is at the bottom of the AlGaN layer, all current that passes through the TiN layer must also pass through the AlGaN layer. The resistance associated with this is called R_{c2}

Ultimately, we are interested in the net reduction of sheet resistance ($R_{Ti,strip}$) and therefore, we performed four series of experiments to quantify the reduction in sheet resistance as a function of the deposition and annealing conditions of the Ti thin films.

The first experiment involved a study of the change in sheet resistance as a function of the thickness of the deposited Ti thickness. All three samples were identical except for the thickness of the Ti layer, which were 10 nm, 25 nm and 40 nm for the different samples. Three different Nitronex AlGaN/GaN on Si samples were used for these experiments. First, standard Ti-Al-Ni-Au ohmic contacts were patterned lithographically and deposited by using e-beam evaporation. Then, mesa isolation was performed by ECR etching using the parameters described in Table 1. Following the mesa etch, the samples were ashed for 20 min in an O_2 barrel asher in order to remove the resist residue. After the photoresist residue from the mesa etch was etched away, the Ti strips were patterned on AZ 5214 photoresist and the surface was cleaned by dipping in de-ionized (DI) water, HCl:DI (1:1) and then in DI water. Immediately after the acid dip, all three samples were loaded in the e-beam evaporation tool and 10 nm of Ti was deposited. After 10 nm of Ti was deposited, the vacuum was broken and the samples were removed. Then, additional Ti was deposited on two samples in order to get 25 and 40 nm thick Ti layers. After the Ti depositions, the samples were annealed at 825°C in a N_2 environment in order to form the ohmic contacts and in order to have the Ti react to form TiN. After the anneal, the color of the Ti strips changed from silver to gold, which is indicative of TiN formation [47]

After these samples were fabricated, the sheet resistance of the samples was measured by using an Agilent 4155C semiconductor parameter analyzer for transfer line

measurements (TLM). Figure 46 shows the TLM measurement of the series of contacts without any Ti strips in the middle. From this TLM measurement, we can see that the sheet resistance is 390 Ω/□. We then did TLM measurements for the patterns with Ti strips in the middle and we calculated the resistance associated with the Ti strips as shown in Figure 47. The sheet resistance of the area under the Ti strips is 322 Ω/□ compared to 390 Ω/□ for regions without Ti strips.

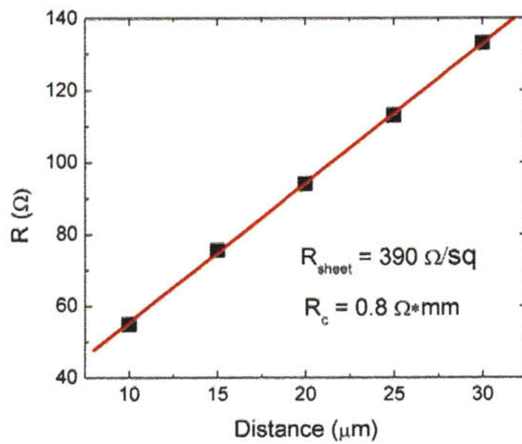


Figure 46: TLM measurement without any Ti strips in between

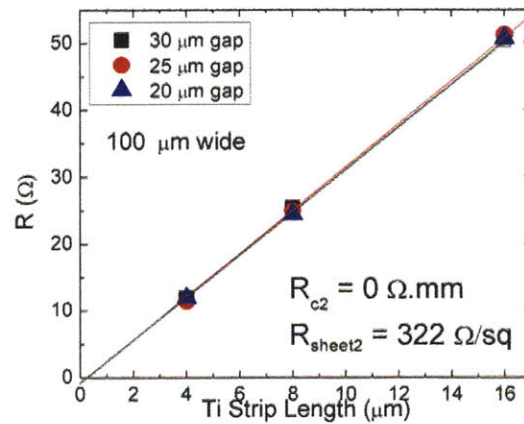


Figure 47: Resistance of Ti strips of different widths.

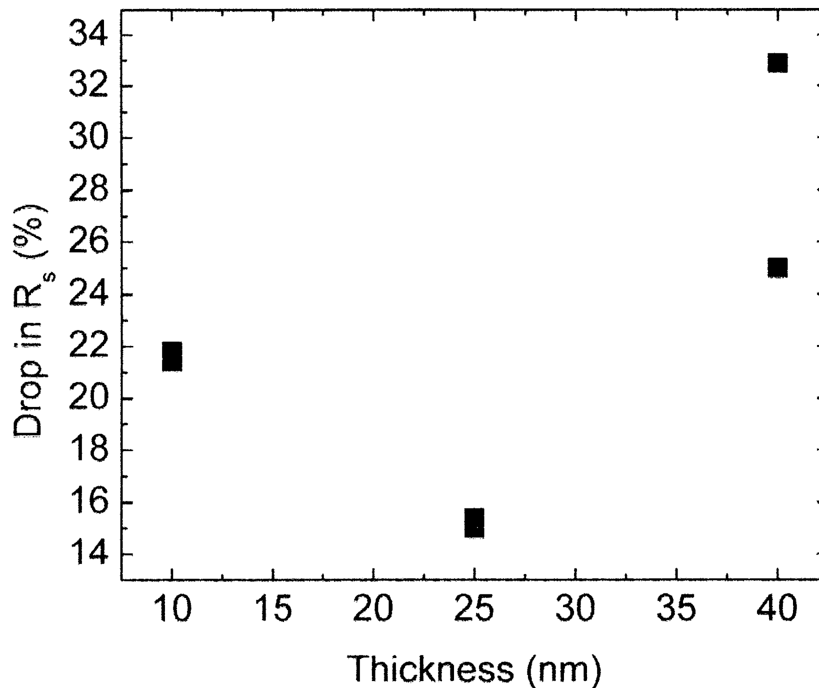


Figure 48: Reduction in Sheet Resistance resulting from depositing Ti and annealing it

Figure 48 shows the reduction in sheet resistance that results from depositing different thicknesses of Ti on the sample. It is noteworthy that the reduction in sheet resistance is less for 25 nm than it is for 10 nm. This may be due to the fact that for the thicker depositions, 10 nm was deposited initially and then the vacuum was broken before additional metal was deposited. Breaking vacuum probably caused oxidation of the Ti.

The second experiment studied the effect of etching down the AlGaN barrier before depositing the Ti layer. We processed three Nitronex samples. After patterning and depositing standard ohmic metals, the Ti strips were lithographically defined. Then, the samples were etched by an ECR etch with etch conditions listed in Table 5. The etch rate for this etch recipe is around 1 nm/min.

Table 5: Etch properties for etching AlGaN layer

	Step 1	Step 2
BCl_3 (sccm)	10	20
Cl_2 (sccm)	0	5
Pressure (mTorr)	6	6
ECR (W)	100	100
DC Bias (V)	75	75
Time (s)	60	0, 300s, or 600s

After the ECR etch, 15 nm of Ti was deposited by ebeam evaporation. After the deposition and the liftoff, the sample was annealed at 825°C in a N_2 environment. Finally, mesa isolation was performed by an ECR etch.

Again, the change in sheet resistance was characterized by performing transfer line measurements. The etching induced some lateral damage, which manifested itself as a second contact resistance between the regions with the Ti annealed on top and the AlGaN/GaN regions without the metals on top, as shown in Figure 49.

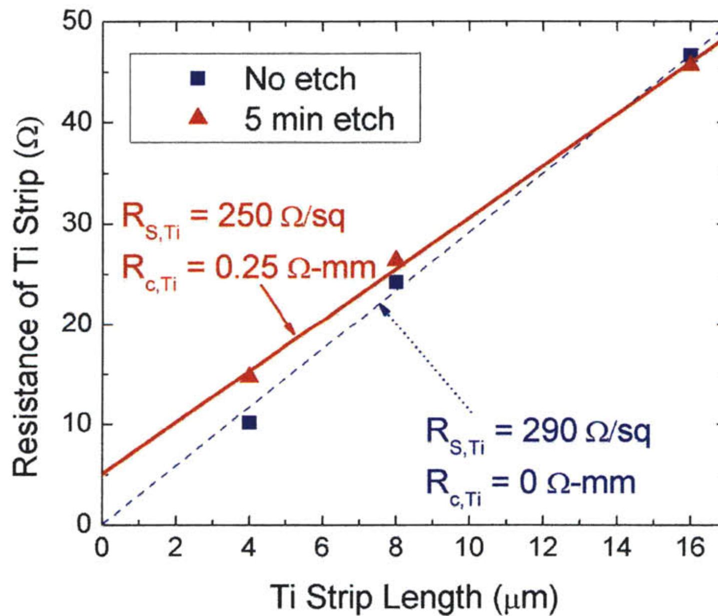


Figure 49: Resistance of Ti strips vs. strip length for both the unetched sample and the sample that was etched for 5 min

The sample that was not etched exhibited a reduction in the sheet resistance of 29 % while the sample that was etched for 5 min exhibited a reduction in the sheet resistance of 42%. While the etching damage did induce additional resistance, these results are promising since it shows that perhaps the reduction in resistance will be more pronounced for heterostructures with thinner AlGaN layers.

The third experiment that was conducted was almost identical to the second experiment except it involved depositing and annealing Ti/Si strips at 825°C. 15 nm of Ti and 15 nm of Si was deposited by e-beam evaporation. Annealing Ti and Si together is said to form Titanium silicide, which is reported to have a lower sheet resistance than Ti or TiN [48]. From transfer line measurements, the sample that was not etched had a reduction in the sheet resistance of 22 %. The sample that was etched for 10 min had substantial etch damage since the contact resistance was 5.5 Ω-mm while the reduction in sheet resistance was 25 %

The fourth experiment was designed to see the impact of changing the anneal temperature to 870°C and to compare the performance of 40 nm Ti strips to 20 nm Ti/20 nm Al strips. After the mesa etch and 20 min ashing to remove residue, standard ohmic contacts were deposited. Then, lithography for the thin metal strips was performed and before depositing the metals, the sample was dipped in DI water and HCl:DI (1:3) for 1 min each. The samples were put inside the deposition chamber immediately after the acid dip. From transfer line measurements, the areas with the Ti/Al had a 10% reduction in sheet resistance while the areas with Ti had a 6 % reduction in sheet resistance.

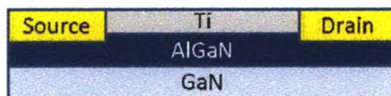
To summarize, we have achieved a reduction in sheet resistance of up to 30% without etching down the AlGaN barrier. More significantly, when the barrier was

etched, there was a reduction in the sheet resistance by up to 40%. These results are very promising towards the development of a silicide-like technology in nitride HEMTs, especially in highly scaled barrier devices were an even greater reduction in the sheet resistance is expected.

Chapter 6: Fabrication of Self-Aligned Transistors

Section 6.1: Gate Last Process for Self-Aligned Transistors

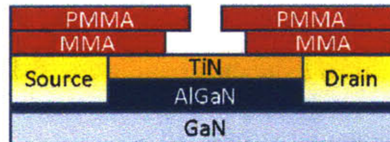
This chapter describes early attempts to fabricate self-aligned transistors that utilize the advantages of the gate first process described in Chapters 3-5 and the thin Ti strip silicide-like process described in Chapter 6. Two different approaches have been developed: A gate first approach and a gate last approach. A general process flow for the fabricating gate-last transistors is shown in Figure 50.



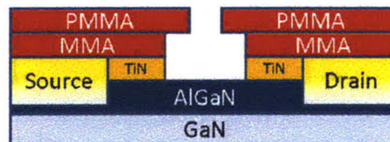
1) Deposit ohmic metals and Ti strip between contacts.

2) Anneal at 825C to form ohmic contacts and TiN.

3) Spin on ebeam resist



4) Expose ebeam resist. MMA is more sensitive, thus forming undercut.



5) Dry etch the TiN away. Due to isotropic etching, the TiN not covered by MMA gets etched away

6) Deposit gate metal. The gate is patterned based on the top PMMA pattern, thus leaving TiN free regions on the sides of the gate

Figure 50: Process flow showing Gate last process

Transistors were fabricated on the same Nitronex AlGaN/GaN on Si substrates that were described in Chapter 3. First, mesa isolation was performed by electron cyclotron resonance (ECR) etching. After patterning the mesa isolation patterns with positive OCG-825 photoresist, the samples were etched with the same etch conditions described in Table 1. Then, 20 nm of HfO_2 was deposited using ALD using the conditions described in Table 3. After the HfO_2 oxide was deposited, gate pads were patterned using an image reversal process for the AZ 5214 photoresist. 500 A of Ti and 3000 A of Au were deposited as the gate stack. Then, the ohmic contacts were patterned by using AZ 5214 photoresist. After the resist patterning, the dielectric layer was etched away by ECR etching. The etch conditions are shown in Table 6

Table 6: Etch conditions for etching HfO_2

CF4 flow (sccm)	40
O2 flow (sccm)	4
Chamber Pressure (mTorr)	10
ECR Power (W)	200
RF Power (W)	10
Time (s)	180

After the dielectric was etched away, ohmic contacts consisting of 200A-Ti/1000A-Al/250A-Ni/500A-Au were deposited by ebeam evaporation and then lifted off. Then, Ti strips were patterned using AZ 5214 photoresist and the HfO_2 was etched away by an ECR etch using the etch conditions detailed in Table 6. 15 nm of Ti was deposited by ebeam evaporation and lifted off by soaking in acetone. The substrate was annealed at 825°C in a N_2 environment in order to form the ohmic contacts and to form the TiN.

After the anneal, ebeam resist was spun on the sample. First, MMA(8.5)MAA EL11 from Microchem was spun on at 4000 rpm. Then, PMMA 950K A4 was spun on at 2000 rpm and a second layer of PMMA 950K A4 was spun on. This was to ensure that the ebeam resist that was spun on was thick enough to stand the TiN etch. Then, the ebeam resist was exposed in the Raith 150 e-beam lithography tool in the Scanning Electron Beam Laboratory (SEBL) at MIT.

Following the e-beam write, the TiN was etched away using an ECR etch. The same CF_4-O_2 based recipe detailed in Table 6 was used to etch away the TiN. Then, the gate stack was metallized by depositing 300A-Ni/2000A-Au/500A-Ni using electron beam evaporation.

Figure 51: SEM Image of Gate last transistor with magnification of 40000X. Note that TiN has been etched from the sides.

We then measured these transistors by using an Agilent 4155C semiconductor parameter analyzer as shown in Figure 52.

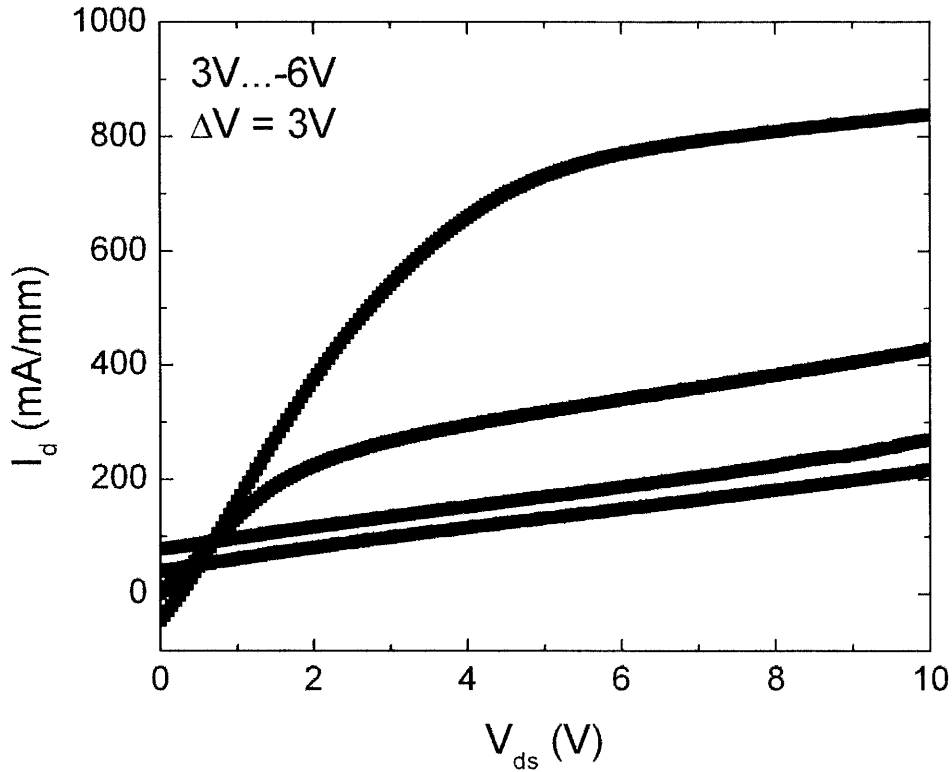


Figure 52: Id-Vds measurement for Gate last self-aligned transistor. Note that the device does not pinch-off due to gate leakage.

As shown in Figure 52, the transistor does exhibit some field effect behavior in that the on current is modulated by changing the gate voltage from 3V down to -3V. In addition, the IV curve indicates that there is no direct short between the source and the drain. However, the high gate leakage prevents the device from being completely pinched off.

Section 6.2: Gate First Process for Self-Aligned Transistors

We also fabricated transistors using a gate first method, as shown in Figure 53.

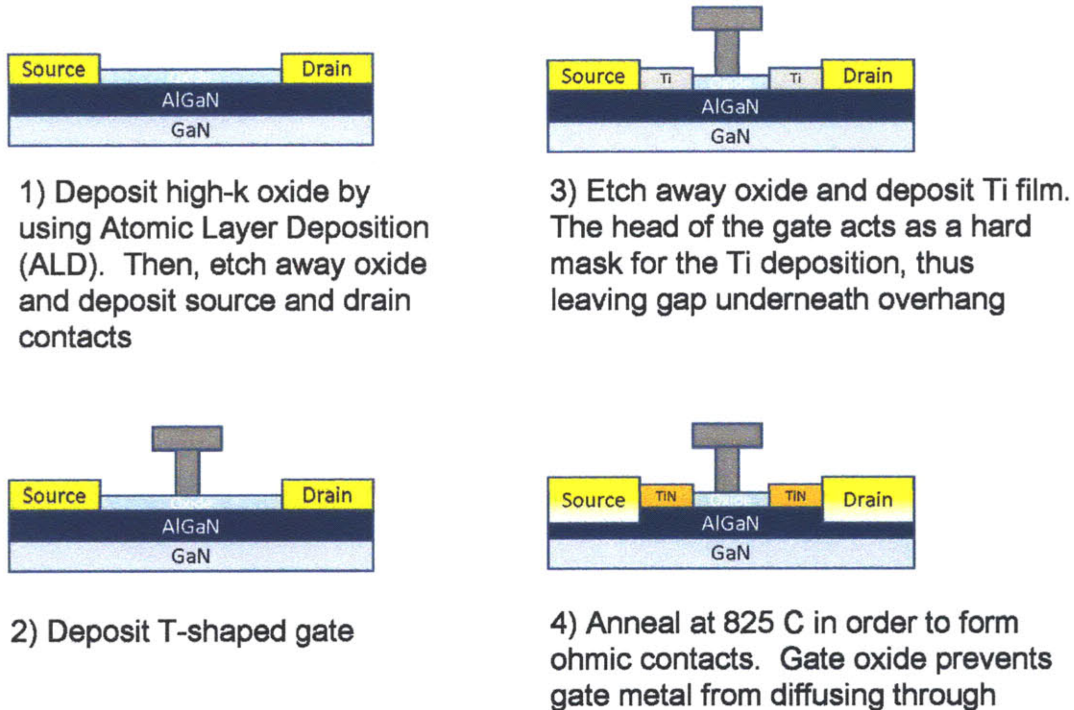


Figure 53: Process flow for the gate first self aligned HEMT process developed in this project.

Transistors were fabricated on the same Nitronex AlGaN/GaN on Si substrates that were described in Chapter 3 using a similar process to that of fabricating gate last self aligned transistors. Mesa isolation was performed by ECR etching and then 20 nm of HfO_2 was deposited. Then, gate pads composed of 500 A of Ti and 3000 A of Au were deposited. After the gate pads, ohmic contacts were deposited.

Then, ebeam resist was spun on in order to pattern T-shaped gates. In order to ensure tall gate feet, two layers of PMMA 950 K A4 were spun on at 2000 rpm. This was followed by spinning on a layer of MMA(8.5)MAA EL 11 at 4000 rpm and then by spinning on a final layer of PMMA 950 K A4 at 4000 rpm. Following the ebeam

lithography write and development, ebeam gates were metallized by depositing 500 A of Ti following by 5000 A of Au in an e-beam evaporator. After the e-beam gate metallization, 15 nm thick Ti was deposited everywhere between the source and drain access regions. Finally, the substrate was annealed at 825°C in a N_2 environment.

The fabricated devices were however shorted. As shown in Figure 54, there was a ring of metal that was deposited on the edge of the Ti strip pattern. As a result, the gate was shorted between the source and the drain.

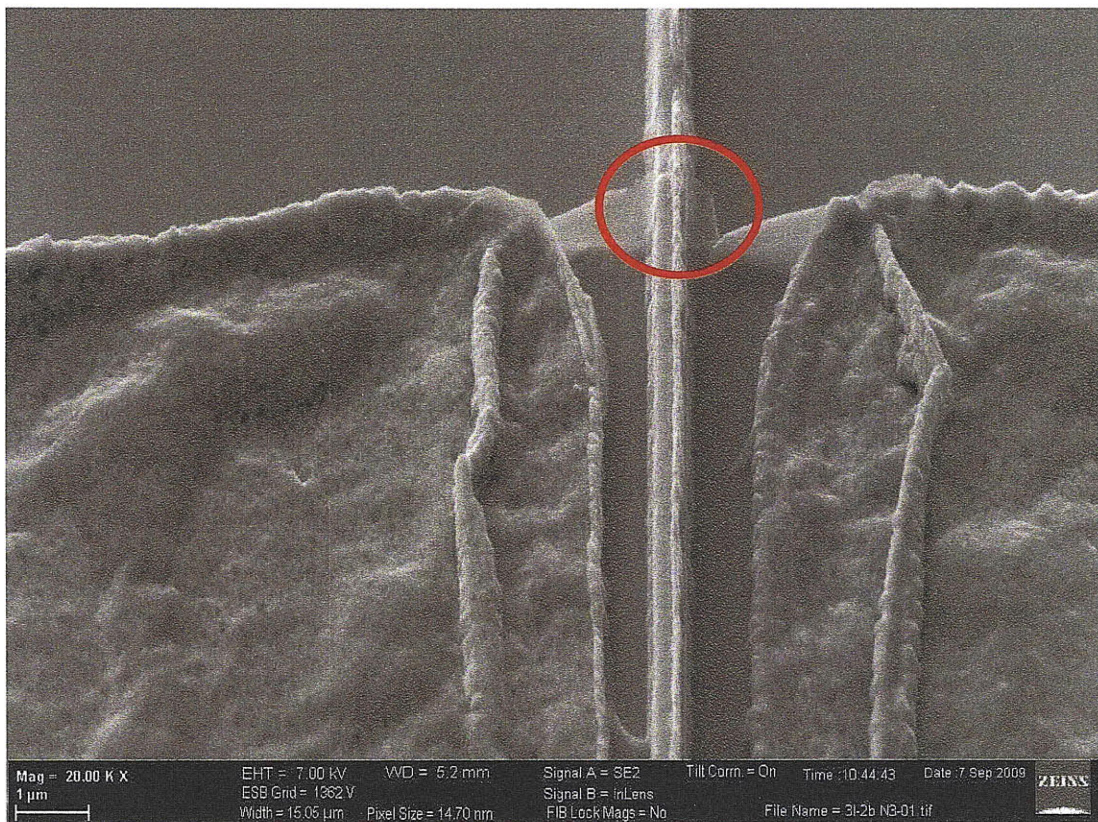


Figure 54: SEM Image of gate first transistor (081909_A) with magnification of 20 KX. Note that ring of metal is shorting the gate with the source and drain

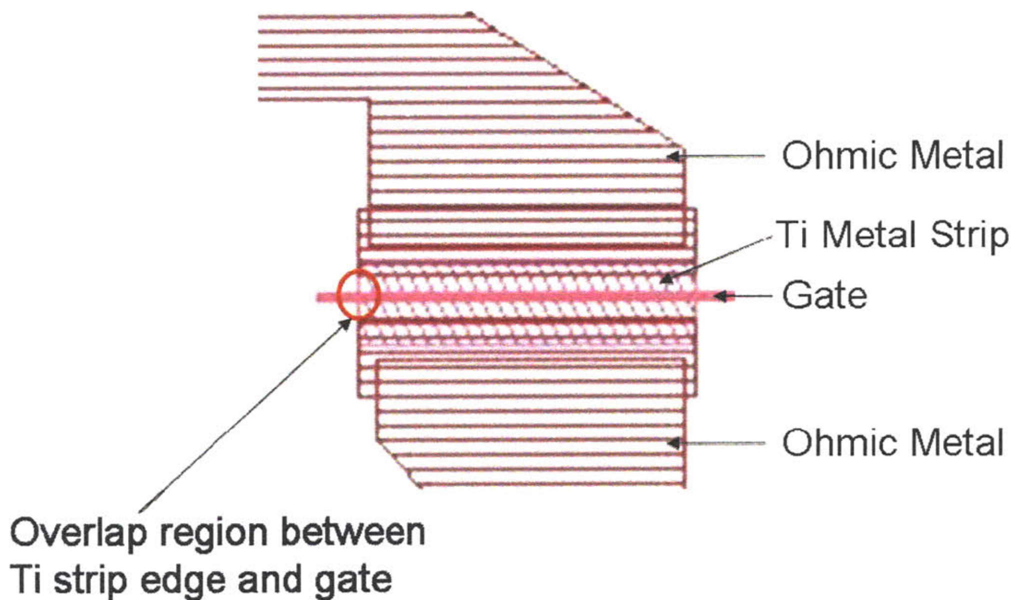


Figure 55: Schematic showing how Gate first self-aligned transistors look when fabricated with SaadatTiDopingMaskI mask. The Ti metal strip pattern's edge overlaps the gate as indicated in the figure.

In order to solve this problem, we redesigned the mask as shown in Figure 56. The Ti strips extends laterally in order to avoid having any edges intersect the gate. However, the excess Ti needs to be etched in order to prevent a short between the source and drain. We fabricated gate first self-aligned transistors using this new mask and we etched away the excess Ti by and ECR etch. The etch parameters were the same as that which were used to etch TiN and are detailed in Table 6

Figure 57 shows a completed gate first transistor made using the SaadatTiDoping-II mask. While we eliminated the problem with the Ti metal ring shorting out the device, the gate shape was not T-shaped and thus the gate was shorted with the source and the drain. We anticipate that with a T-shaped gate, we will avoid this shorting problem.

In summary, we have developed a gate last self-aligned process and a gate first self-aligned process. We were able to measure the output characteristics of a transistor fabricated using the gate last approach. Based on the high gate leakage, it seems that the

gate has a short due to incomplete removal of the TiN. There needs to be further investigation as to the most effective method of removing the TiN completely. As for the gate-first approach, there were problems with rings of metal depositing on the sidewalls of the resist, which caused shorts between the gate and the ohmic contacts. This problem has been solved with a new mask design and it is anticipated that once transistors with a T-shaped gate are fabricated, self-aligned transistors will be successfully fabricated.

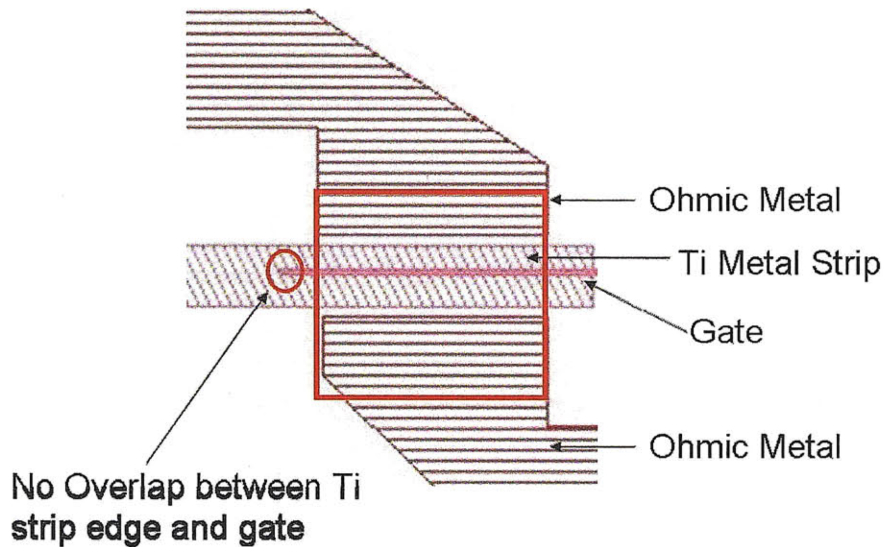


Figure 56: Schematic showing how Gate first self-aligned transistors look when fabricated with SaadatTiDopingMaskII mask. The gate does not overlap with the etch of Ti strip. However, in order to prevent shorts, all the Ti outside the red square is etched away by an ECR etch.

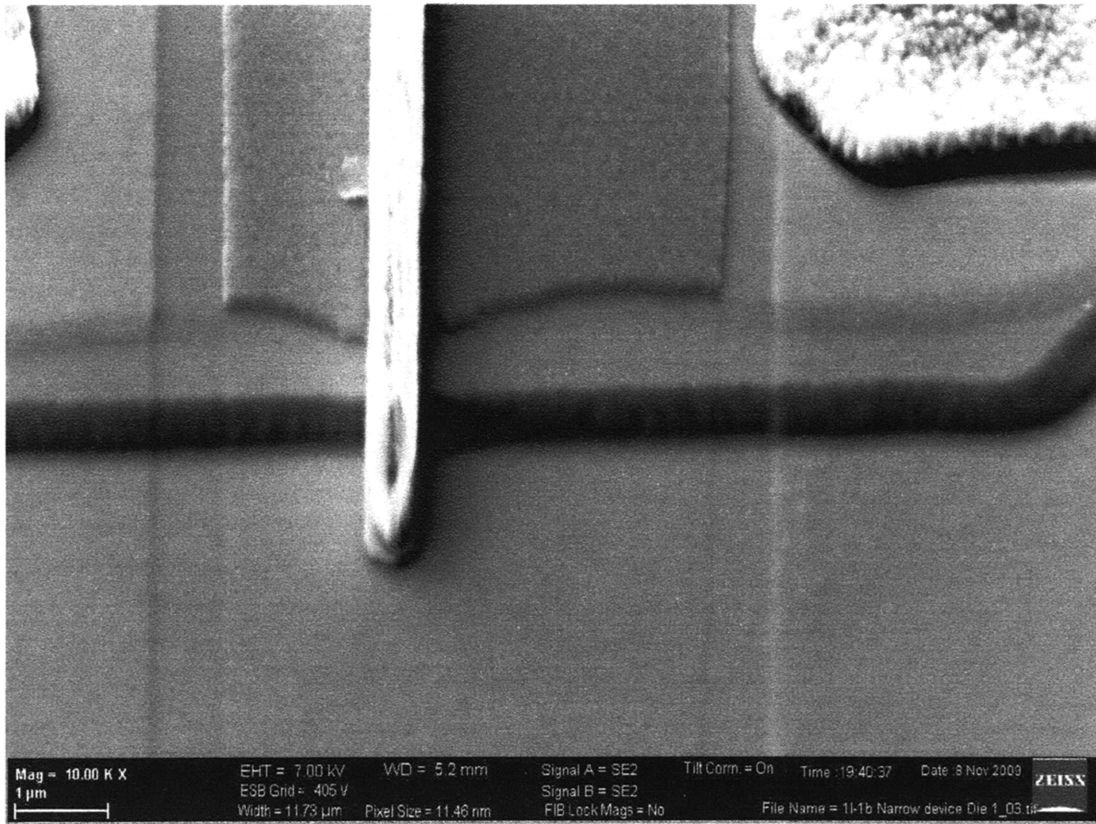


Figure 57: SEM image of Gate first self-aligned transistor fabricated with SaadatTiDopingMaskII mask. Note that there are no rings of Ti in this device design.

Chapter 7: Conclusion and Future Work

In this thesis, we have demonstrated a new gate technology with high-k dielectrics that can be used for gate-first processing where the gate is subjected to 870°C anneal temperatures. Not only did these gate stacks survive the ohmic anneal temperature, but also transistors with these gate stacks have superior performance than transistors with conventional gates for the following reason:

1. The devices with Al_2O_3 had up to 35% higher transconductance than standard devices. This was despite having lower gate capacitance, which seems to indicate an enhancement in the electron mobility.
2. The gate dielectrics allowed for positive gate voltage. The devices with Ga_2O_3 + HfO_2 gate dielectrics had 40 % higher drain current densities than standard devices.
3. Devices with dielectrics had a significant reduction in gate leakage. Devices with Ga_2O_3 + HfO_2 had a 10,000 times reduction in gate leakage in comparison to standard devices.
4. The devices with Al_2O_3 (including devices with only 15 nm of dielectric) were passivated unlike standard devices. This compares very favorably to devices that are passivated with 100 nm of SiN since thinner passivation layers are better for reducing parasitic capacitances.

Given the advantages shown for these W/high-k gate stacks, this technology is not only suitable for self-aligned high frequency devices but also for other applications like power electronics where high current densities, low gate leakage and well-passivated devices are needed.

We have also shown that Ti-based metal films can be deposited on top of the source and drain access resistance. When the AlGaN barrier was etched, we achieved a 40% reduction in sheet resistance but etching down the AlGaN barrier caused damage. When the barrier was not etched, we achieved a reduction in sheet resistance up around 30 %.

Finally, we identified a gate first and a gate last process flow for fabricating self-aligned transistors. . Transistors fabricated by using the gate last process flow were tested and showed transistor behavior. Fabrication challenges involving the gate first process, like the formation of rings on the outsides of the Ti strips that were deposited, were addressed by redesigning the mask. With these redesign masks, it is anticipated that devices with an ideal T-shaped gate can be used to fabricate gate first devices.

The high-k metal gate stack and the Ti strip deposition process can be further optimized in order to further enhance transistor performance. The gate dielectric stacks that have been developed need to be further optimized and understood by doing the following:

1. Develop thinner gate dielectrics. In this thesis, the thinnest dielectric that was used had a thickness of 15 nm. As noted in [6], it is necessary to scale down the distance between the gate and the channel in order to scale down AlGaN/GaN HEMTs. Therefore, it is necessary to fabricate transistors with thinner dielectrics for better frequency performance.
2. Understand why Al_2O_3 dielectrics are effective at passivating the surface and improving the transconductance. By understanding the physics, it would make it easier to further optimize the dielectric. Furthermore, this would allow us to

identify other dielectrics which may be as effective as Al_2O_3 at passivating the surface but with improved properties like a higher dielectric constant or lower gate leakage.

Second, we need to further improve the performance gains achieved by the silicide-like annealed Ti strip access regions. Further optimization would involve the following:

1. Deposit and anneal Ti on samples with thinner AlGaN barrier layers. Etching down the AlGaN barrier before depositing and annealing Ti improves the resulting sheet resistance by up to 40%. This is probably because the Ti/TiN was closer to the 2-DEG and because annealing Ti on top of a thinner AlGaN barrier induced a higher concentration of Nitrogen vacancies. While etching down the AlGaN barrier induces damage, starting with a thin barrier layer to begin with would help solve this problem. In addition, by using samples with thinner barriers, the gate would be closer to the channel.
2. Look at different surface treatments. In these experiments, the best results were achieved when the surface was etched by BCl_3 before the Ti deposition. Other groups have fabricated low temperature ohmic contacts by performing a $SiCl_4$ treatment [21]

Finally, we need to demonstrate self-aligned transistors that incorporate these technologies and optimize self-aligned transistors by doing the following:

1. Fabricate self-aligned transistors by using both the gate-first and gate-last processes and then compare then by DC and microwave measurements. The

processes yield different transistor structures and thus would be expected to have differing performance.

2. Further optimize the gate-last process. In this thesis, we used a dry etch to etch away the TiN. A wet etch might be more effective at etching away all the TiN

All the technologies described in this thesis show promise for improving the frequency performance for AlGaN/GaN HEMTs since they will allow for reducing access resistances and scaling down barrier thicknesses without sacrificing other aspects of transistor performance like gate leakage.

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