Heavy-ion-induced digital single event transients in a 180 nm fully depleted SOI process

Heavy-Ion-Induced Digital Single Event Transients in a 180 nm Fully Depleted SOI Process

Matthew J. Gadlage, Pascale Gouker, Bharat L. Bhuva, Balaji Narasimham, and Ronald D. Schrimpf

***Abstract*—Heavy- ion-induced single events transients (SETs) in advanced digital circuits are a significant reliability issue for space-based systems. SET pulse widths in silicon-on-insulator (SOI) technologies are often significantly shorter than those in comparable bulk technologies. In this paper, heavy-ion-induced digital single-event transient measurements are presented for a 180-nm fully depleted SOI technology. Upset cross-sections for this technology with and without body-ties are analyzed using 3-D TCAD simulations. Pulse broadening is shown to lengthen the measured SET pulse widths significantly for the circuit without body contacts.**

***Index Terms*—Heavy ions, ion radiation effects, silicon-on-insulator technology, single event transient, single event upset (SEU).**

I. Introduction

SILICON-ON-INSULATOR (SOI) technologies present inherent advantages over bulk technologies due to the lower charge collection, lower cross section per transistor, and higher operating speeds. Previous work has shown that single-event transient pulse widths are significantly shorter in SOI technologies when compared to similar bulk technologies [1]. However, one well-known issue for floating-body SOI devices is "pulse broadening" or "pulse stretching" [2]. This phenomenon may significantly increase SET pulse widths as the SET propagates through a circuit. Laser-induced SET results on test structures from a 180-nm fully-depleted SOI technology were presented by Gouker *et al.* [3]. One of the key findings was that for the target circuit without body contacts, the SET pulse broadened at a rate of nearly 3 ps/inverter as it propagated through the circuit. The authors attributed the pulse widening to the floating body of the transistors (body contacts were shown to mitigate this effect). Thus, for SOI circuits bound for radiation environments, body contacts should reduce the SET pulse widths. In this work heavy ion-induced single-event transient pulse widths are experimentally measured in a 180-nm fully depleted SOI process for devices with and without body contacts for the first time. Results clearly show a reduction in SET pulse widths and the number of measured SET pulses for the devices with body contacts. Technology computer aided design (TCAD) simulations are used to explain these experimental results. Additionally, the SET cross section of the fully depleted SOI process with and without body contacts is compared to the SET cross section of a bulk process.

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II. Test Chips

The test circuits used to characterize the SET pulses were fabricated in a 180-nm fully depleted SOI (FDSOI) CMOS technology from MIT Lincoln Laboratory. The detailed description of the circuit is given in [3], [4]. The design consists of a linear chain of 200 minimum-drive-strength inverters (the target circuit in which the SETs are generated) that terminates in a pulse-capture circuit that records the occurrence of an SET and the pulse-width of the corresponding SET. The nMOS and pMOS widths of the inverters are 0.6 μm and 2.5 μm, respectively, and the etched gate length is 0.2 μm. The pulse-capture circuit measures the SET pulsewidth in terms of latch delays [4]. The pulse-capture circuit uses 25 inverter stages along with latches to store the number of inverters affected by each SET. With the individual latch stage delay of about 70 ps (at the nominal operating voltage of 1.5 V), this circuit allows measurement of SET pulses ranging from 70 ps to over 1 ns with a 35 ps measurement resolution [3]. The test chips consisted of two measurement circuits. The first circuit consisted of transistors in the inverter chain (target circuit) with source-body contacts. The second circuit was identical but the transistors did not have body contacts. In this technology, the silicon layer thickness is 40 nm. For comparison, in IBM's 65-nm partially-depleted SOI process, the SOI thickness is 60 nm [5]. Laser-induced SET results on these test structures were presented last year by Gouker *et al.* [3].

III. Heavy Ion Test Results

Heavy ion testing on the SET test structures was performed using the 4.5 MeV/amu cocktail at Lawrence Berkeley National Labs using ions with LET's ranging from 7 to 100 MeV-cm^2/mg. Histograms of the pulsewidth distributions for the test structures with and without body contacts for four different ions are shown in Figs. 1–4. As expected, the SET pulse widths show a wide distribution, similar to what has been observed in bulk technologies [6]. The data clearly show the presence of SET pulses longer than 1 ns for particles with an LET of 40 MeV-cm^2/mg in the parts without body contacts. For the circuit with the source-body contacts, very few transients with SET widths greater than 70 ps were measured. The longer pulse widths in the circuit with a floating body may be attributed to "pulse-broadening".

One interesting item to note from Figs. 1–4 is that no SETs pulses with widths less than 280 ps were observed. The most likely explanation for this is that the test circuit is unable to accurately measure transients shorter than a few latch stages.

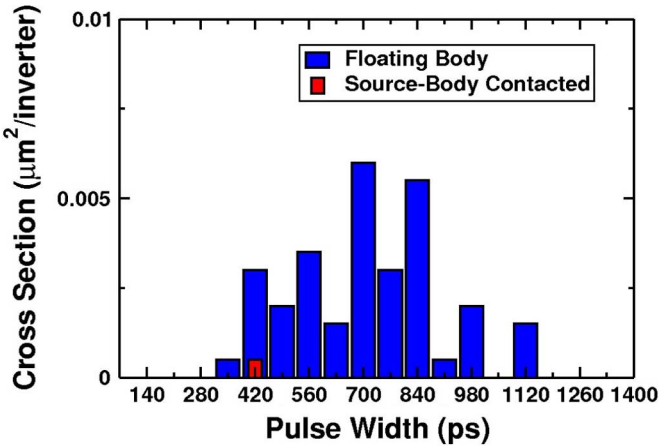

Fig. 1. SET pulsewidth distributions for Argon (LET = 14 MeV-cm^2/mg, Fluence = 1×10^9 particles/cm^2). Note that not only are the pulse widths shorter for the circuit with source-body contacts, the total the number of counts is also significantly less.

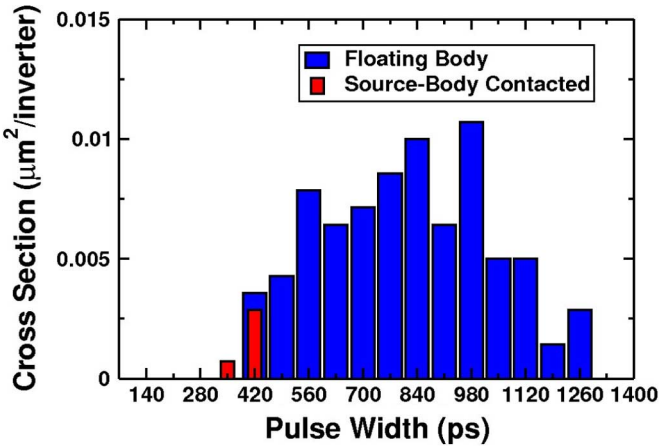

Fig. 2. SET pulsewidth distributions for Krypton (LET = 40 MeV-cm^2/mg, Fluence = 7×10^8 particles/cm^2).

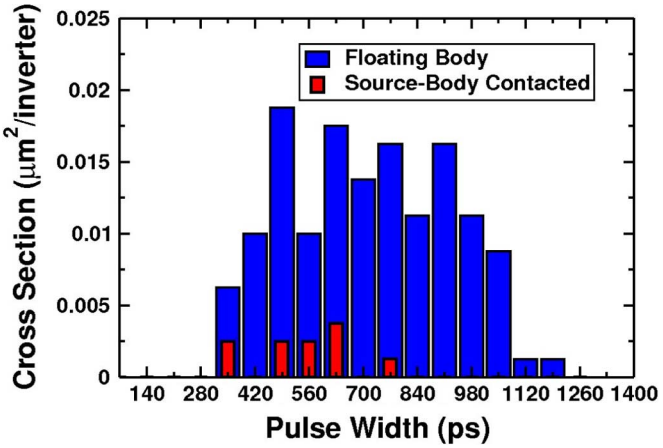

Fig. 3. SET pulsewidth distributions for Xenon (LET = 69 MeV-cm^2/mg, Fluence = 4×10^8 particles/cm^2).

This has been reported for test structures very similar to the one used in this work [7]. Narasimham has also observed this effect in a nearly identical test structure in a bulk CMOS technology [8]. Narasimham attributed it to attenuation in the pulse capture

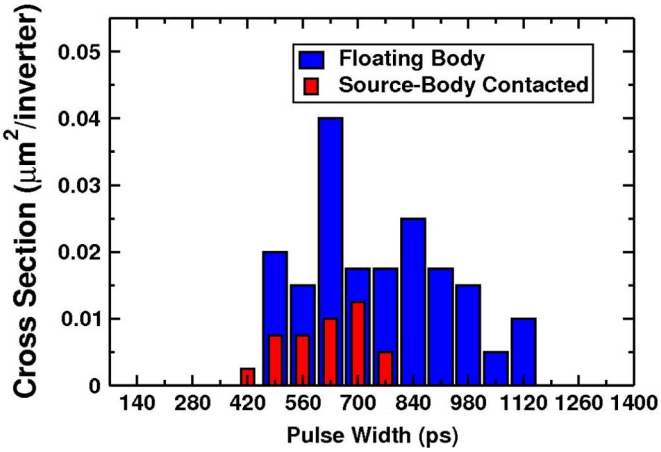

Fig. 4. SET pulsewidth distributions for Bismuth (LET = 100 MeV-cm^2/mg, Fluence = 2×10^8 particles/cm^2).

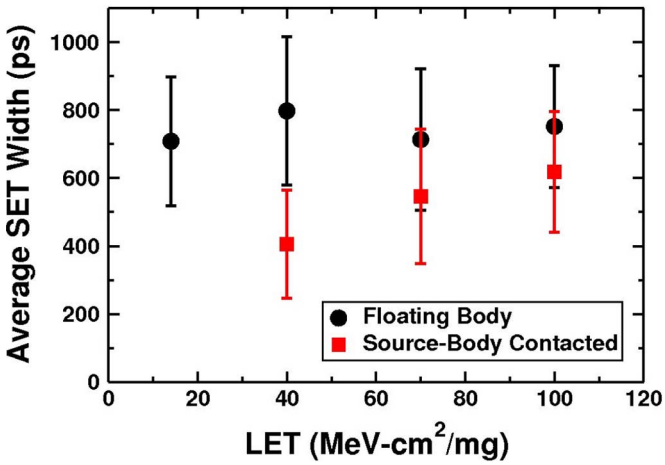

Fig. 5. Average SET pulse widths experimentally measured for the two target circuits. The error bars represent one standard deviation from the average.

latches and showed that for SETs greater than approximately three latch stages no attenuation occurred and the SET was measured correctly. The impact of this on the results presented here is that there may have been SETs generated smaller than 280 ps, but we were unable to accurately measure them with this test structure.

To clarify the data shown in Figs. 1–4, the average measured pulse widths are plotted versus LET for both circuits in Fig. 5. The average SET pulsewidth increases with LET for the source-body contacted circuit, but remains relatively constant for the floating-body circuit. This is due to the fact that for the floating-body circuit almost all of the measured SETs will have broadened from their initial width. As a result, the average measured SET width for the floating-body circuits is not an average of the generated SET width, but rather an average of the generated plus broadened SET width. In other words, the average SET width has been skewed by the broadening.

Heavy ion testing was also performed at different operating voltages to determine the effect of operating voltage on the SET pulse widths. The floating-body test structure was exposed to Xe ions (with an LET of 69 MeV-cm^2/mg). Since SET pulse widths in this test circuit are measured in terms of a latch delay,

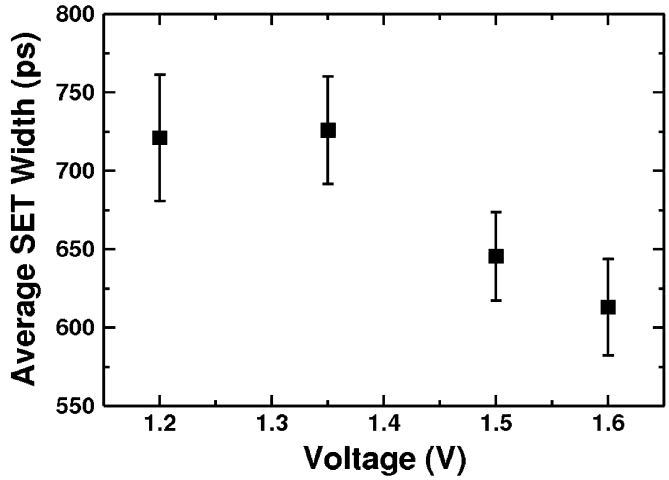

Fig. 6. Average SET pulse widths experimentally measured for several operating voltages for the floating-body circuit. The error bars represent the standard error from the average. The standard error is equal to the standard deviation divided by the square root of the number of events. Approximately 40 SET events were measured at each voltage.

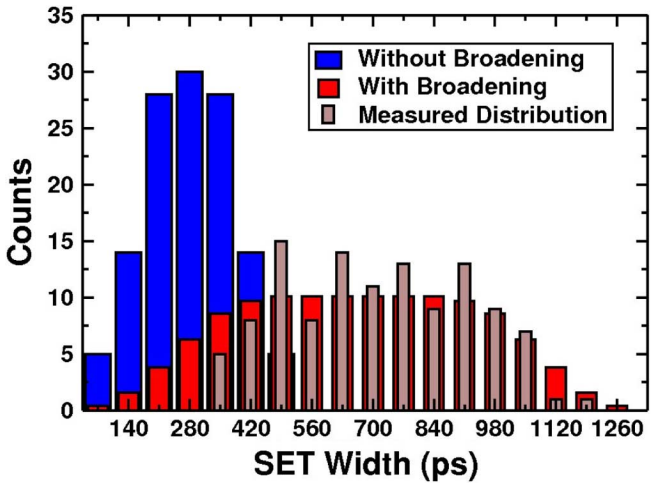

Fig. 7. Plots of a possible original distribution of SETs without pulse broadening, the distribution obtained by convolution of the broadening-caused effects, and the actual measured SET events.

TABLE I
SET DATA AS A FUNCTION OF OPERATING VOLTAGE

Voltage (V)	Average Pulse Width (latches)	Latch Delay (ps)	Average Pulse Width (ps)
1.6	9.73	63	613
1.5	9.21	70	645
1.35	9.08	80	726
1.2	7.67	94	721

knowledge of how the latch delay changed with voltage was needed. The measured latch delay (which was determined by measuring the frequency of a ring oscillator made up of the same latches used in the SET measurement circuit) for several voltages is shown in Table I. In Fig. 6, the heavy ion-induced pulsewidth is plotted as a function of operating voltage. Approximately 40 SET events were measured at each voltage. The pulse widths tend to increase with decreasing voltage. The data (i.e., increasing pulsewidth with decreasing operating voltage) are consistent with the pulsed laser probing experiments reported last year by Gouker *et al.* [3]. From 1.6 V to 1.2 V, the average measured SET pulsewidth increases by about 100 ps. The increase can be attributed to an increase in the generated (i.e., non-broadened) SET. Recent work has shown that broadening does not change significantly with operating voltage [3], [9]. An increase in generated SET widths with decreasing supply voltages has also been observed in other bulk CMOS technologies [10].

IV. EXTRACTING GENERATED SET PULSE WIDTHS FROM THE FLOATING-BODY CIRCUIT

Since the SET pulsewidth broadening rate for the non body-contacted circuit is known [3], an attempt was made to determine the SET pulsewidth distribution in the absence of pulse broadening. By doing such an analysis, an approximation of the original (non-broadened) SET distribution can be obtained. With a known broadening rate of approximately 4 ps per inverter, a generated SET of 140 ps may be measured as anywhere from 140 to 940 ps wide pulse depending on where in the 200 inverter chain it was generated. (Note: While Gouker *et al.* [3] reported an average broadening rate of 2.6 ps per inverter in this test structure, for this analysis a broadening rate of 4 ps per inverter is used. This rate corresponds to a worst case broadening reported by Gouker *et al.* The 4 ps per inverter rate can be obtained by taking the bottom and the top of the error bars from the Gouker data in [3].)

To perform this analysis, one first needs to create a reasonable distribution for the non-broadened SET pulse widths (shown as the blue curve in Fig. 7). By convolving the 4 ps increase per inverter stage with the possible non-broadened distribution, a likely measured distribution can be obtained. The likely measured distribution can then be compared to the real measured distribution. If the calculated likely distribution does not match the experimental results, new non-broadened distributions can be created until a close approximation of the measured distribution is obtained.

Fig. 7 shows plots of a possible original distribution of SETs without pulse broadening, the distribution obtained by convolution of the broadening-caused effects, and the actual measured SET events for an LET of 69 MeV-cm^2/mg. The average SET pulsewidth for the distribution without broadening is 280 ps. This average non-broadening SET width is shorter than the average of 520 ps found during heavy ion testing for the source-body contacted circuit for the same LET value. However, if one performs the same analysis using a broadening rate of only 2.6 ps per inverter, one will find that the estimated average non-broadened SET pulsewidth distribution will increase by about 140 ps ($= 200 * 1.4$ ps/2). This suggests that the generated SET pulse widths for the body-contacted and floating-body circuits are similar.

A similar analysis can be performed on any SET measurement circuit with a large number of inverters where pulse broadening may be an issue.

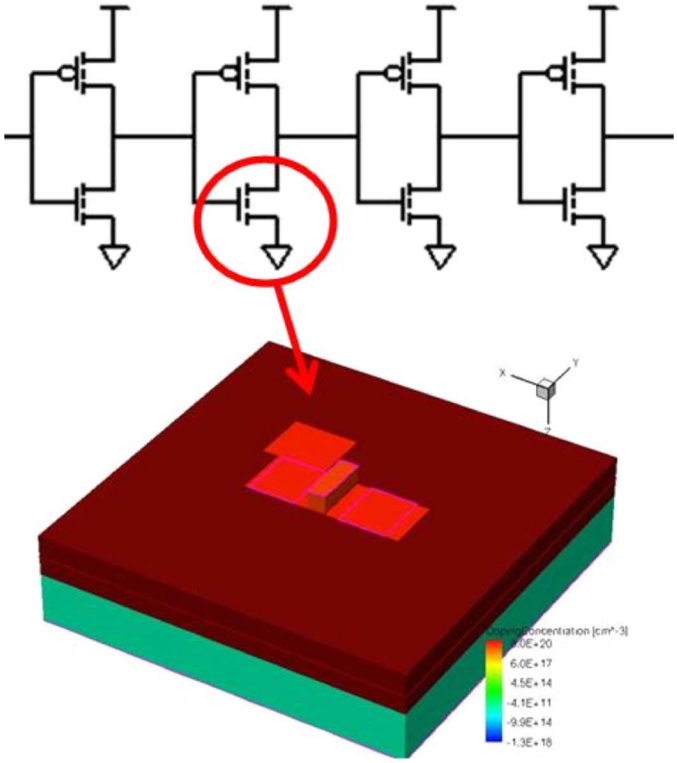

Fig. 8. Illustration of the mixed-mode model used for the simulations. The second nMOSFET in a four inverter chain was modeled in 3-D TCAD, and the remaining inverters were modeled in SPICE.

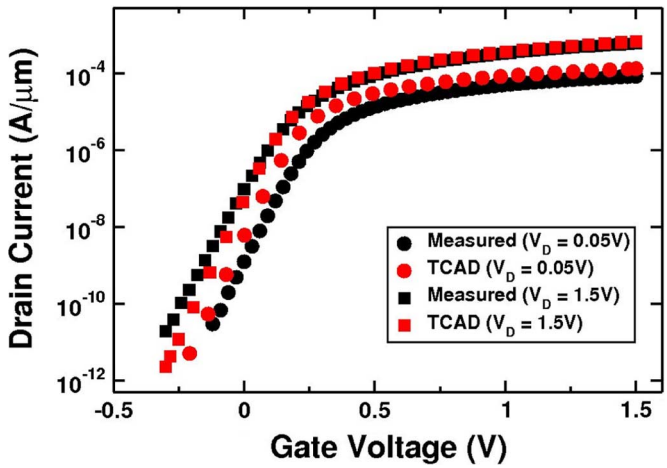

Fig. 9. Comparison of measured and simulated *I–V* curves for a device in this technology.

V. TCAD Simulations

Mixed mode simulations were performed using TCAD and SPICE models calibrated to measurements made on transistors fabricated in this 180-nm FDSOI technology. Measured *I–V* curves for the transistors are compared to the simulated *I–V* curves in Fig. 9. For these simulations, the off-state nMOS (or pMOS) transistor of the second inverter in a four inverter chain was modeled using 3D-TCAD.

For the first set of simulations, the difference in generated SET pulse widths for a body-contacted device and floating-body device was compared. The results of these

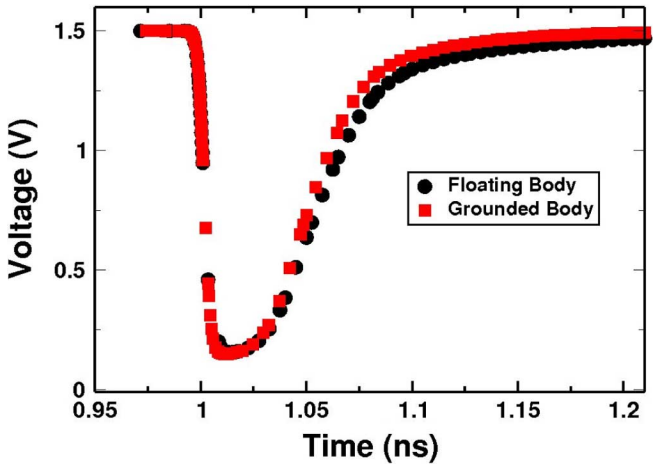

Fig. 10. Simulated SET pulse widths at the struck node for an LET of 40 MeV-cm^2/mg for the non-body contacted device and the body contacted device. The ion strike location in this simulation was the center of the gate.

simulations are shown in Fig. 10. The incident ion LET was 40 MeV-cm^2/mg and the ion strike location was the center of the gate. This is the most sensitive region for an SOI device. To simulate the body-contacted device, an ideal contact was used to tie the body potential to ground. (Note: in the actual device, the body contact consists of an oppositely doped region next to the source that overlaps the edge of the gate, and is shorted to the source by self-aligned $CoSi_2$ [3]. The importance of this is that the body contact adds extra capacitance to the node which is not taken into account in this "simple" simulation that utilizes an ideal contact.) As seen in Fig. 10, the FWHM pulse is approximately the same for both floating-body and the ideal body-contacted devices. The generated SET pulsewidth at this struck node is less than 100 ps. This simulated SET width is shorter than the measured SET widths, but the main point of the simulations presented in this section is to look more at the trends than the actual SET pulse widths, and what is observed here is that simply grounding the body does not significantly alter the SET pulse width. This simulation suggests that differences in generated SET widths between the floating-body and body-contacted devices may be due more to the extra capacitance added with the body-contact than due to the body potential being simply tied to ground.

In Fig. 11, the dependence on ion strike location for the floating-body device is shown. These simulations were also performed with an LET of 40 MeV-cm ^{2}/mg. These simulations confirm that a transient is only produced when the ion strikes the body region (i.e., the region under the gate) in these SOI devices. Identical simulations were also performed on the device with the ideal body contacts. The results were the same as those in Fig. 10 (i.e., the generated SET was approximately the same for both devices). The important difference is that in an inverter chain with body-ties, the smaller transients may attenuate as they propagate through the inverters in the target circuit. In the floating-body circuit, these transients may broaden as they propagate. The end result is that more transients that are greater than our minimum measurable width are recorded with the floating-body circuit. This leads to a larger heavy-ion cross section for the floating-body transistors.

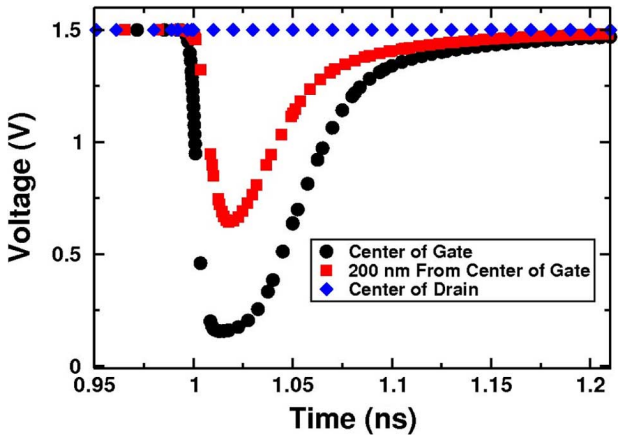

Fig. 11. Simulated SET pulse widths for the floating-body device showing the pulsewidth dependence on the ion strike location. As the strike location moves away from the center of the gate, the SET pulses become smaller. An ion strike at the center of the drain creates no SET. For "200 nm From the Center of the Gate" simulation, the ion strike location was along the length of the transistor (i.e., 200 nm from the center of the gate towards the drain area).

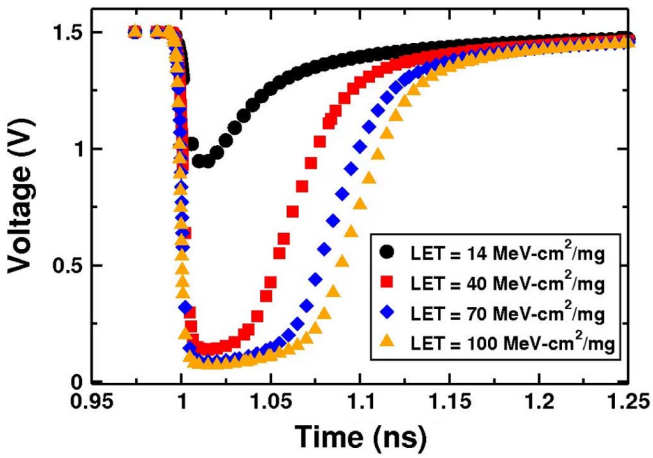

Fig. 12. Simulated SET pulsewidth distributions for strikes on the nMOS device for the ions used in testing.

The pulsewidth dependence on LET was also explored using TCAD simulations. The TCAD simulations were performed using the same LET's as were used during the heavy ion testing. A small dependence of SET pulsewidth on LET is observed in the simulated results presented in Fig. 12.

Simulations were also performed on a calibrated pMOS device. The simulated SET pulse widths were found to be significantly shorter in pMOS devices than in nMOS devices for every LET value. This correlates well with results presented by Gouker *et al.* [3] where the threshold laser energy to create a transient in the pMOS device was approximately $2.5\times$ the energy needed to create a transient in the nMOS device. A simulated SET strike (with an LET of 100 MeV-cm^2/mg) is shown in Fig. 13. The generated SET pulse is very small but is still large enough to create a transient that is able to propagate through to the next inverter. Simulations were also performed using smaller LET values, for an LET value less than 70 MeV-cm^2/mg the generated SETs were not wide enough to propagate through more than a few inverters. However, in a floating-body inverter

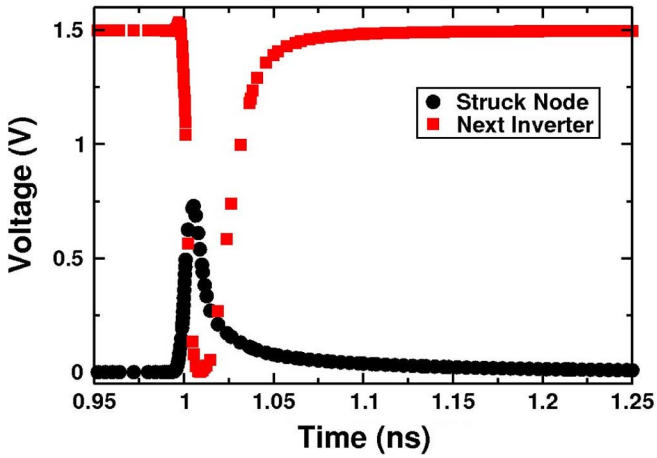

Fig. 13. Simulated SET pulsewidth for a strike on the pMOS device with an LET of 100 MeV-cm^2/mg.

chain with 200 inverters (like in our test circuit); this very small generated SET could still broaden up to 800 ps (if the broadening rate was 4 ps/inverter and it was generated near the beginning of the 200 inverter chain).

VI. Discussion

SETs widths over 280 ps have been experimentally measured in a 180-nm FDSOI process in an inverter chain with floating-body transistors and in an inverter chain with body-contacted transistors. The measured transient widths were found to be longer for the floating-body circuit. This is primarily due to pulse broadening in the inverter chain. TCAD simulations were presented that suggest that at least some of the SETs may have been smaller than 200 ps, but the test circuit was unable to accurately measure them.

In general, the TCAD simulated pulse widths were shorter than the average measured pulse widths from the heavy ion experiment. There are numerous possible explanations for this. First of all, the SET measurement circuit was not able to accurately capture the small SETs. In other words, the small SETs may have been present in the experiment, and we were just unable to measure them. Secondly, subtle differences in the TCAD model can drastically alter simulated SET pulse widths. The TCAD model was calibrated to measured *I–V* curves (Fig. 9), but it's possible certain items (such as doping, ion strike profiles, etc.) may not have been a perfect match to the actual device and/or experiment. Overall, the goal of the simulations was give insight into trends. For example, it was observed that the nMOS transistors were more sensitive to single event hits than the pMOS transistors. The dependence of SET pulsewidth on the LET of the incident ion, the ion strike location, and simply grounding the body was also discussed.

For the majority of the TCAD simulations presented in this work, only the data from the struck node was shown. The main reason for this is that pulse broadening effects are not taken into account with usual SPICE models [9]. Since it is known that pulse broadening occurs in the floating-body devices, simulations that do not take this broadening effect into account are not completely accurate for data on SET propagation. In the floating body devices, it's possible that small SETs (like some shown in

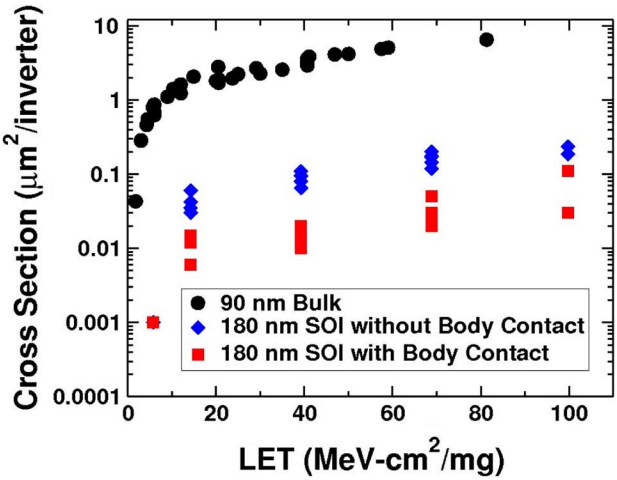

Fig. 14. Comparison of 90-nm bulk [6] and 180-nm FDSOI SET cross sections.

these TCAD simulations) may actually broaden (instead of attenuate) as they propagate. Massengill *et al.* [9] have presented a method to take into account pulse broadening in SPICE models, but it was not incorporated in this work.

To put this work into context of some previous SET measurements, the SET cross section can be compared to that of a bulk device. In Fig. 14, the cross section to produce a measurable SET in a 90-nm technology is compared to that of a 180-nm FDSOI technology. The data from the 90-nm technology is from Narasimham *et al.* [6]. The smallest measurable transient in the 90-nm technology was 100 ps. Even though the area of a transistor in the 180-nm technology is almost twice that of one in a 90-nm technology, the cross section is over an order of magnitude less. This is due to the fact that in SOI the area under the gate is the only area in which a reverse-biased junction exists to collect charge (as confirmed by the simulations shown in Fig. 11), whereas in a bulk technology reverse-biased junctions also exist between drains and substrate (or well). As seen in Fig. 14, SOI cross sections can be reduced even more by adding a body contact. However, the maximum SET pulsewidth for bulk and SOI circuits without body-ties circuits is comparable.

VII. Conclusion

In this paper, heavy ion-induced digital single-event transient pulse widths in a fully depleted SOI technology have been experimentally measured and simulated using TCAD. These are the some of the first heavy ion-induced SET pulse-width measurements for a 180-nm FDSOI technology. The long pulse widths in the floating-body circuit can be explained by pulse broadening as the transient propagates through the 200-inverter chain. TCAD simulation results show that the generated SET at the struck node is approximately the same for both a simple-grounded body and a floating-body device. However, due to pulse broadening in the floating-body circuit the transients measured in the floating-body circuit were larger than that of the body-contacted circuit.

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