45nm Direct Battery DC-DC Converter for Mobile Applications

by

Saurav Bandyopadhyay


Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2010

© Massachusetts Institute of Technology 2010. All rights reserved.
45nm Direct Battery DC-DC Converter for Mobile Applications

by

Saurav Bandyopadhyay

Submitted to the Department of Electrical Engineering and Computer Science on May 21, 2010, in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering and Computer Science

Abstract

Portable devices use Lithium-ion batteries as the energy source due to their high energy density, long cycle life and low memory effects. With the aggressive downscaling of CMOS, it is becoming increasingly difficult to efficiently interface the low voltage, low power digital baseband and DSP of the mobile phone with the battery which maybe at voltages as high as 4.2V. This is efficiently done by a DC-DC converter which is a separate IC designed on an older generation process capable of handling high voltages. However, this requires an extra IC, thereby increasing the overall system cost. Here, a buck converter is demonstrated on a standard 45nm digital CMOS process which can be integrated with the 45nm digital core on the same die. This converter is capable of handling high battery voltages (2.8V to 4.2V) and delivers a regulated low voltage (0.5V to 1.1V) to the digital core. The converter can supply 20μA to 100mA of load current. The peak efficiency of the converter is 87% for 73mW output at 4.2V supply and for the ultra low power levels, efficiency of 75% is obtained for a 20μW load at 3V. Both pulse width modulation (PWM) and pulse frequency modulation (PFM) modes of control are used. A new digital pulse width modulator (DPWM) architecture is presented which provides 75% area savings over the conventional delay line and counter based architecture with comparable power consumption. The buck converter also requires Switched Capacitor (SC) DC-DC Converters to generate stacking regulators and regulator for the control circuitry. On the whole, the complete system integrates the Power Management Unit with the core for a single chip radio in 45nm.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Joseph F. and Nancy P. Keithley Professor of Electrical Engineering
Acknowledgments

I would first like to thank my parents and my grandfather for believing in me even when I did not. No words are enough to express their selfless love, affection and support. Over the years they have helped me through all the tough times. I cannot thank them enough. I would also like to thank my advisor Prof. Anantha Chandrakasan for being more than just a mentor. He has been an ideal role model for all of us. I would also like to thank Dr. Yogesh Ramadass who has taught me everything I know about Power Converters! Every discussion with him is stimulating, even the non technical ones like cursing the Indian cricket team whenever they lost. Without his help I would not have been able to tape-out on time. Dr. Alice Wang at Texas Instruments. She always had the time and patience to answer all my questions regarding the process. It was because of her support (and DRC waivers!!) that my design went for fabrication. Margaret, our administrative assistant, for doing so much for all of us that we don’t even realize. Also to the students of ananthagroup, who have made our lab a wonderful environment to work in. Last but not the least, I am grateful to my roommates Rahul Rithe and Rishabh Singh for bearing with me for the last two years.
## Contents

1 Introduction
   1.1 Motivations for Direct Battery DC-DC Converter .......................... 14
   1.2 Background Work .................................................. 15
   1.3 Thesis Organization ............................................... 17

2 System Architecture .................................................. 19
   2.1 Power Stage of Buck Converter .................................. 19
      2.1.1 Power Transistor Sizing .................................. 20
      2.1.2 Output Filter Design ..................................... 23
      2.1.3 Level Shifters .............................................. 25
      2.1.4 Gate Drivers .............................................. 27
   2.2 Switched Capacitor Converters .................................. 29
      2.2.1 1.8V Switched Capacitor Converter ................. 29
      2.2.2 Stacking Converters .................................. 32
   2.3 Control Architecture ........................................... 40
      2.3.1 PWM control .............................................. 40
      2.3.2 PFM control .............................................. 43
      2.3.3 DPWM architecture .................................. 46
      2.3.4 Chapter Summary ...................................... 50

3 Measurement Results .................................................. 53
   3.1 Die Micrograph and Board ..................................... 53
   3.2 Efficiency Plots ................................................ 54
3.3 Transient Response .................................................. 56
3.4 Comparison of Measured Results ................................. 57

4 Conclusion and Future Work ........................................... 61
  4.1 Main Contributions .................................................. 61
  4.2 Design Summary .................................................... 62
  4.3 Further Work ....................................................... 62
List of Figures

1-1 Discharge curve of Lithium Ion battery .................................. 14
1-2 Block Diagram of DC-DC converter with digital baseband/DSP ...... 15

2-1 Block level architecture of Power Converter .............................. 20
2-2 Architecture of Power Converter ........................................... 21
2-3 Optimal Width for minimum loss .......................................... 22
2-4 Simulated losses in the power stage ...................................... 23
2-5 Conventional Level Shifter .................................................. 24
2-6 Capacitive Coupled Level Shifter ........................................... 25
2-7 Simulation result of capacitive coupled level shifter shifting the rails from 0, 1.8V to $V_{BAT}$-1.8V, $V_{BAT}$ ........................................... 26
2-8 Gate Drive for PMOS in power stage ..................................... 27
2-9 Simulation showing the gate drive circuit output with two inputs which are inverted and level shifted versions .............................. 28
2-10 1.8V SC with three gain settings ........................................ 30
2-11 PFM loop of 1.8V SC ....................................................... 31
2-12 Simulation of PFM loop of 1.8V SC ..................................... 32
2-13 Gate voltages of the power FETs ........................................ 33
2-14 $V_{BAT}$-1.8V and $V_{BAT}$-3.6V regulators ................................. 34
2-15 $V_{BAT}$-1.8V and $V_{BAT}$-3.6V regulators ................................. 35
2-16 Strong ARM comparator .................................................... 36
2-17 High Voltage tolerant Strong ARM comparator ........................ 37
2-18 High Voltage tolerant Strong ARM comparator ........................ 38
2-19 Clock Gating Circuit for Stacking Regulators .................. 39
2-20 Simulations of the clock gating circuit ............................... 40
2-21 Architecture of Control Circuitry ................................. 41
2-22 4 bit Flash ADC .............................................. 42
2-23 PFM simulation .................................................. 44
2-24 Total Loss with optimal tp ........................................ 45
2-25 Concept of Zero Current Switching ................................. 47
2-26 Delay line based DPWM architecture ............................... 48
2-27 DPWM architecture with sleep control ............................ 49
2-28 Capacitor voltage increasing linearly with time .................. 51
2-29 Simulated waveforms showing the comparator current, sleep signal and the DPWM output to PMOS power FETs ...................... 52

3-1 Die Microphotograph ................................................ 53
3-2 Board with IC and off-chip components ............................ 54
3-3 Measured Efficiency of DC-DC Converter for various battery voltages .................. 55
3-4 Breakup of Overall Power Loss ..................................... 56
3-5 Load Transient from 100uA to 5mA ................................. 57
3-6 Load Transient from 5mA to 100uA ................................. 58
3-7 Load Transient from 10mA to 50mA and vice versa ................ 59
**List of Tables**

1.1 SIA technology direction ........................................ 13
1.2 CMOS DC-DC buck converters .................................... 16
1.3 Previous Work with Design Targeted .......................... 17

2.1 DPWM techniques .................................................. 48
2.2 comparison of DPWM performance ............................... 50

3.1 Comparison of Measured Results ............................... 59

4.1 Design Summary .................................................... 62
Chapter 1

Introduction

Hand-held portable electronics have significantly advanced in the last decade. Moore’s law has enabled us to integrate more and more functionality on a chip. With each scaled generation, the number of transistors on a die has doubled, the gate oxide has scaled and the nominal voltage has reduced [1]. Table 1.1 shows the trend of scaling as predicted by the SIA road-map published in 1999. Although with scaling the gate capacitance reduced, the leakage increased due to the small channel lengths. With increased complexity, integration and functionality, the total power consumption has increased. Circuit designers have tried to alleviate the power problem by using techniques like Ultra Dynamic Voltage Scaling (U-DVS) [2], parallelism, power gating and clock gating [3]. U-DVS requires changing the supply to the digital circuit on the fly. In such cases it is essential to have a highly efficient DC-DC converter converting battery voltage to a lower voltage desired for U-DVS to be effective. Optimizations right at the power source would provide us with large energy savings and would help extend the lifetime of these devices [4].

Table 1.1: SIA technology direction

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18µm</td>
<td>0.13µm</td>
<td>0.10µm</td>
<td>70nm</td>
<td>50nm</td>
<td>35nm</td>
</tr>
<tr>
<td>Nominal Supply Voltage</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
<td>0.9V</td>
<td>0.6V</td>
<td>0.6V</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>2.5nm</td>
<td>1.9nm</td>
<td>1.5nm</td>
<td>1.2nm</td>
<td>0.8nm</td>
<td>0.6nm</td>
</tr>
<tr>
<td>Transistors/chip (million)</td>
<td>24</td>
<td>95</td>
<td>190</td>
<td>530</td>
<td>1500</td>
<td>4300</td>
</tr>
</tbody>
</table>
1.1 Motivations for Direct Battery DC-DC Converter

With advances in battery technology, it has been shown that Lithium-ion batteries provide a high energy density and long cycle time [5] making them ideal candidates for portable applications. Fig 1-1 shows the discharge curve of a 2AH Lithium-ion battery. When fully charged, the battery has a voltage of 4.2V. When discharged to moderate levels, its voltage is close to 3.7V. Beyond this, the voltage drops steeply to below 3V. For any portable application, we need to ensure that it can work for voltages ranging from about 2.8V to 4.2V.

![Discharge curve of Lithium Ion battery](image)

Typically, the power management unit (PMU) is a set of ICs capable of handling high voltages supplying power to the low voltage low power ICs. The DC-DC converters in the PMU are designed on an older generation process. Integrating the DC-DC converter with the digital baseband/DSP [6] on the same die would remove the cost
of an extra IC, the cost of integrating it on the board and would also reduce the board footprint. The nominal supply for 45nm node is 1.1V and for circuits employing U-DVS, voltages as low as 0.5V may be used. The key challenge lies in designing a converter at the 45nm node that can handle the high battery voltage.

The process used in this work provides some high voltage devices but even then stacking multiple high voltage devices is necessary. The main aim is to have a complete efficient PMU at 45nm which can handle the high battery voltage. The high voltage devices with stacking make this extremely difficult to achieve. The system block diagram is shown in Fig 1-2.

**Figure 1-2: Block Diagram of DC-DC converter with digital baseband/DSP**

### 1.2 Background Work

Integrated CMOS DC-DC converters have enabled us to have power conversion on-chip instead of the discrete component solution. It must be noted that CMOS buck converters usually have all circuits integrated except the off-chip LC filter. Table 1.2 summarizes a few of such converters with their corresponding contributions and performance.

As seen in Table 1.2, the CMOS DC-DC converters are mainly used for U-DVS systems. It is preferred that the converters be integrated with the load circuit (DSP
All the converters cited here except [9] are designed within the allowed voltage limits of the process. This makes achieving high efficiencies a lot simpler than this work. Since we are going beyond the limit of the process, additional control circuitry and stacking is required that limits the overall efficiency. A high voltage DC-DC converter design on 40nm is presented in [10] but it is not an autonomous system as the control circuit is powered not using the main battery. Also, the design can handle only up to 3.3V unlike a direct battery converter.

Table 1.2: CMOS DC-DC buck converters

<table>
<thead>
<tr>
<th>Case</th>
<th>Contributions</th>
<th>Converter Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>[4]</td>
<td>Adaptive dead time control and zero voltage switching (ZVS) to minimize capacitive switching loss in power stage</td>
<td>79% efficient at 750mW load using 1.2μm CMOS</td>
</tr>
<tr>
<td>[11]</td>
<td>Digital PID controller for buck converters first reported with DPWM using a high speed clock and multiplexer for creating pulses</td>
<td>92.9% peak efficiency for 1.38W but using off-chip switches</td>
</tr>
<tr>
<td>[12]</td>
<td>DPWM architecture with delay line and counter first reported</td>
<td>peak efficiency 89% for 20mW output on 0.6μm CMOS</td>
</tr>
<tr>
<td>[7]</td>
<td>Dynamic Voltage Scaling applied to a DSP with embedded DC-DC Converter</td>
<td>Total power savings of 30-50% with embedded DC-DC converter on 0.8μm</td>
</tr>
<tr>
<td>[8]</td>
<td>Dynamic Voltage Scaling system with microprocessor embedded DC-DC Converter</td>
<td>80% to 90% efficiency of DC-DC on 0.6μm CMOS</td>
</tr>
<tr>
<td>[9]</td>
<td>Dual Mode direct battery DC-DC converter with PWM and PFM modes of control and stacking in power stage</td>
<td>70% to 91% efficiency on 0.25μm CMOS</td>
</tr>
<tr>
<td>[10]</td>
<td>High input voltage DC-DC converter with PWM mode only</td>
<td>&gt;90% for 0.1 to 1W output at 40nm</td>
</tr>
<tr>
<td>[13]</td>
<td>Commercial direct battery design from Texas Instruments with both PWM and PFM control modes</td>
<td>49% to 65% efficiency for 90μW output and peak efficiency of 95% for 90mW output on a process that can handle high battery voltages</td>
</tr>
<tr>
<td>[14]</td>
<td>Dynamically changing the output voltage to the minimum energy point voltage of a given circuit</td>
<td>81% to 86% for 1μW to 10μW of load</td>
</tr>
</tbody>
</table>

[9] is direct battery DC-DC converter on 0.25μm CMOS having nominal supply
of 2.5V. The output power being delivered is 150μW to 0.6W. The design [13] is a commercially available IC. The process used for the design is not known but it can handle high voltages without any extra stacking in the power stage. However, no published work addresses the issues in direct battery power converters at ultra-low power levels (10's of μW) to medium power levels (0.1W) that maintain efficiency throughout this range in 45nm. Table 1.2 summarizes a comparison between the direct battery DC-DC converters cited and the targets of this design.

Table 1.3: Previous Work with Design Targeted

<table>
<thead>
<tr>
<th>Case</th>
<th>Technology</th>
<th>Nominal Supply Voltage</th>
<th>Battery Voltage</th>
<th>Output Power</th>
<th>Load Current</th>
<th>Stacking in power stage</th>
<th>Peak Efficiency for ultra-low power</th>
<th>Overall Peak Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>0.25um</td>
<td>2.5V</td>
<td>2.8V to 5.5V</td>
<td>150μW to 0.6W</td>
<td>100μA to 0.4A</td>
<td>Yes</td>
<td>70% for 150μW</td>
<td>91% for 300mW</td>
</tr>
<tr>
<td>[13]</td>
<td>process capable of handling high voltages</td>
<td>1.1V</td>
<td>2.7V to 6V</td>
<td>90μW to 0.54W</td>
<td>50μA to 0.3A</td>
<td>No as process allows high voltage</td>
<td>65% for 90μW</td>
<td>95% for 90mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.8V to 4.2V</td>
<td>10μW to 0.1W</td>
<td>10μA to 0.1A</td>
<td>Yes</td>
<td>&gt;80% for 10μW</td>
<td>&gt;90% for 100mW</td>
</tr>
</tbody>
</table>

As seen, this work targets much lower power as compared to previously published work. Also, since the latest Li-ion battery chargers have a control circuit preventing the battery from overcharging after 4.2V, there is no need for us to go up to 5.5V as in the designs in Table 1.3. Thus, the main aim of this work is to obviate the need of the extra IC like [9] and [13] and have the DC-DC conversion on the same die at the 45nm node.

1.3 Thesis Organization

This thesis presents a completely self-contained direct battery DC-DC converter at 45nm. Chapter 1 gives the main motivation behind the design and does a review of literature. As seen, a high voltage DC-DC converter is a challenging design at scaled
technologies like 45nm. With increased complexity due to stacking, in this design we also deal with a large dynamic range of load conditions. This makes achieving decent efficiencies for the whole range difficult. For light loads, leakage and conduction losses limit the efficiency. For heavy loads, the conduction losses in the power stage limits the efficiency. Chapter 2 discusses the design architecture and the circuit techniques used. Techniques like power gating and clock gating have been used in this work to achieve a highly efficient power converter. As shown, Chapter 3 presents measurement results of the design and makes comparisons with the designs cited before. This design is one of the widest output power range DC-DC converter. Chapter 4 concludes the thesis and provides future directions for this work.
Chapter 2

System Architecture

Power conversion is done by three types of DC-DC converters. The switching regulators (eg. buck, boost) provide a highly efficient solution but require an off-chip LC filter. Switched Capacitor (SC) converters on the other hand provide a completely on-chip solution but at the expense of efficiency. LDOs, which are not considered in this work, are the third type of power converters generally used. These are the least efficient among all the converters described.

Fig 2-1 shows the block level architecture of the design. The main converter used is a buck converter converting the high battery voltage to the desired low regulated voltage. The SC converters generate the intermediate stacking voltages ($V_{BAT}$-1.8V and $V_{BAT}$-3.6V) and voltages for control (1.8V and 1.2V). These are used by the main buck converter for its power stage and control circuit making the system a fully integrated DC-DC converter at 45nm. The power stage and the SC converters use high voltage transistors but the control circuit shown uses the core 45nm devices.

2.1 Power Stage of Buck Converter

The power stage of the buck converter consists of the power transistors, the gate drive circuits, level shifters and the output LC filter. From Fig 2-2, it can be seen that the power stage is asymmetric. Three high voltage PMOS transistors have been stacked and only one NMOS transistor is used. Each PMOS transistor can handle a
Figure 2-1: Block level architecture of Power Converter

certain $V_{DS}$ and $V_{GS}$ given by the process. Since we have to handle a battery voltage greater than 3.6V, three devices have been stacked. On the NMOS side, the device used is a very high voltage drain extended device that can handle very high a $V_{DS}$. Stacking on the NMOS side using the high voltage transistors (similar to the PMOS high voltage devices used) is not preferred as this would require an extra deep n-well for isolation, thus increasing the cost of processing. In this design, the bulk of all the NMOS transistors have been tied to ground obviating the need for an extra mask. The NMOS transistor in the power stage has a $V_{GS}$ of 1.8V when it is on. The power for driving the gate of this transistor is supplied by the 1.8V SC converter.

### 2.1.1 Power Transistor Sizing

In the PWM mode, the loss in the power stage is dominated by the switching loss and the conduction loss. The switching loss is given by $CV_{DD}^2f_{CLK}$, $V_{DD}$ being the higher
Figure 2-2: Architecture of Power Converter

rail for the gate drive circuit, C the total gate capacitance and \( f_{\text{CLK}} \), the switching frequency of the converter. The conduction loss is given by \( I_{\text{OUT}}R \) where \( I_{\text{OUT}} \) is the dc current being delivered and R is the on resistance of the transistor. Here, the current ripple ridding over the dc current of \( I_{\text{OUT}} \) is ignored for PWM. For a more detailed analysis, we need to consider the rms power loss, which depends also on the inductor in the output filter. As the gate capacitance is directly proportional to the transistor width, wider the transistor, more is the switching loss. On the other hand, the on resistance is inversely proportional to the transistor width. These opposing trends give an optimum width of a given load current. If we consider \( C=k_1W \) and \( R=k_2/W \), where \( k_1 \) and \( k_2 \) are two process dependent constants, the total loss is
given by the following equation,

\[ \text{loss} = k_1 W V_{DD}^2 f_{CLK} + I_{OUT}^2 k_2 / W \]  

(2.1)

For a given \( I_{OUT} \), \( V_{DD} \) and frequency, the optimum width is given by

\[ W_{optimum} = \sqrt{(I_{OUT}^2 k_2) / (k_1 V_{DD}^2 f_{CLK})} \]  

(2.2)

Fig 2-3 shows the optimal normalized width for minimum loss in the power stage. In this work, the transistor N1 has been sized optimally for 50mA load current. The sizing of the PMOS power transistors has been done to preserve the PFM efficiency at light loads which will be discussed later in this subsection.

![Optimal Width for minimum loss](image)

Figure 2-3: Optimal Width for minimum loss

The breakup of simulated power loss in the power stage is shown in Fig 2-4 for 62mW output power. As seen, a large fraction (61%) of the loss is due to the very high voltage drain extended NMOS. It must be noted that the switching loss in the NMOS is mainly dominated by the \( CV^2 f_{CLK} \) loss due to charging up the drain to
gate capacitor when PMOS power transistors are on and NMOS power transistor is off. As the drain voltage has to go up all the way up to $V_{BAT}$, it is this loss that dominates the overall switching loss rather than just the loss in the NMOS gate drive circuit to switch on the NMOS power transistor.

![Figure 2-4: Simulated losses in the power stage](image)

The PMOS transistors are intentionally not sized optimally for 50mA load in PWM, as the conduction loss is much more than switching loss. For loads less than 100μA, the leakage through the PMOS transistors starts to hurt the efficiency. To ensure that efficiency is preserved even at light loads, the transistors in the stack were sized such that the leakage was less than 80nA. This translates to <4% drop in efficiency at 10μW output load in PFM.

### 2.1.2 Output Filter Design

The inductor and capacitor values have been selected so that the current ripple and voltage ripple are within acceptable limits of design. Also, loop stability needs to be considered when the controller is designed for the PWM mode. The current ripple in the inductor current is given by the following expression.
\[ I_{\text{ripple}} = V_{\text{BAT}}(1 - D)D/(2Lf) \]  

(2.3)

L is the inductance, D is the duty cycle and f is the switching frequency of the converter. \( I_{\text{ripple}} \) is maximum when \( V_{\text{BAT}} \) is 4.2V and \( V_{\text{OUT}} \) is 1.2V. For a switching frequency of 2MHz and inductor of 10\( \mu \)H, current ripple is 23mA. This translates to 0.8mW rms conduction loss, 33\% of the total conduction loss given by Fig 2-4.

The voltage ripple is given by the following expression. For a 2\( \mu \)F capacitor, the voltage ripple is less than 1mV. As the output filter ripple is extremely small, the other sources of ripple, e.g ripple in SC effecting the switching of the transistors, dithering in PWM dominate the overall voltage ripple.

\[ V_{\text{ripple}} = I_{\text{ripple}}/(8Cf) \]  

(2.4)

![Figure 2-5: Conventional Level Shifter](image-url)
2.1.3 Level Shifters

The gate driver of the PMOS power transistor P1 as shown in Fig 2-2 needs to have \( V_{BAT} \) and \( V_{BAT} - 1.8 \)V as the two rails between which the gate voltage will be switching. For P3, the rails required are \( V_{BAT} - 1.8 \)V and \( V_{BAT} - 3.6 \)V. Level shifters are required to shift the rails so that the PMOS power FETs can be effectively switched. For a signal between 0V and 1.8V, the traditional level shifter used to shift the rails to \( V_{BAT} - 1.8 \)V and \( V_{BAT} \) is shown in Fig 2-5. Its a DCVSL type of structure but since the level shifter signal cannot go rail to rail, that is from 0V to \( V_{BAT} \), we require extra PMOS devices to prevent the voltage from going all the way down to 0V. The problem with this circuit is that it is inherently slow due to its ratioed nature and does not scale well with the battery voltage.

![Capacitive Coupled Level Shifter](image)

Figure 2-6: Capacitive Coupled Level Shifter

In this work, a capacitively coupled level shifter is designed. This is inherently low power and scales well with the battery voltage. However, we need to ensure that this circuit works even at low frequencies. Leakage might cause the level shifted output to change if the input remains constant for a long period, hence making this a dynamic
circuit. The circuit diagram is shown in Fig 2-6. Extra diodes are used to ensure that the output always remains between $V_{BAT}$ and $V_{BAT}-1.8V$. In this design, we have two such level shifters, one to shift the supply rails to $V_{BAT}-1.8V$ and $V_{BAT}$ and the other for the rails $V_{BAT}-3.6V$ and $V_{BAT}-1.8V$.

Figure 2-7: Simulation result of capacitive coupled level shifter shifting the rails from 0, 1.8V to $V_{BAT}-1.8V$, $V_{BAT}$

Fig 2-7 shows the simulation result of the capacitive coupled level shifter in the PWM mode. The bottom waveform is a 2MHz signal that goes from 0V to 1.8V. This is the input to the level shifter. The output is the top waveform swinging from 2.5V to 4.2V. It must be noted that the swing is slightly reduced at the output due to charge sharing between the coupling capacitor and the associated parasitic capacitors the the output node. The coupling capacitors used in this design were metal to metal capacitors so that the associated parasitic capacitors are minimized. This swing can be restored by a subsequent DCVSL inverter stage or a pass transistor gate drive discussed later.
2.1.4 Gate Drivers

In order to drive the power transistors, we have to design gate drivers. For the NMOS in the power stage, the driver is a string of inverters, each subsequent inverter scaled so that the final inverter has enough strength to drive the power transistor. For the PMOS, P3, we can use a string of inverters. However, for the PMOS, P1, connected directly to the battery, an inverter structure cannot be used. This is because the NMOS transistor in the inverter would be having a $V_{BAT}$ at its gate. For such a case a gate drive circuit has been proposed that uses pass transistors in manner that avoids any NMOS transistor from getting a very high voltage at the gate. The circuit is shown in Fig 2-8.

![Figure 2-8: Gate Drive for PMOS in power stage](image)

Essentially, this circuit performs an inversion operation without any NMOS with $V_{BAT}$ at its gate. P1 and P2 are the main drivers for the next stage. This requires two inputs which are level shifted and inverted versions of each other as shown in Fig
2-8. P1 is on when its gate voltage is $V_{BAT}-1.8$V. During this time, the gate voltage of P2 has to be $V_{BAT}$ to prevent any conducting path from $V_{BAT}$ to $V_{BAT}-1.8$V through P2. P3 and P4 ensure this. Meanwhile, N1 is off. Hence, the output of the circuit is $V_{BAT}$. For the case when input to P1 is $V_{BAT}$ and to N1 is $V_{BAT}-1.8$V, the gate of P2 gets $V_{BAT}-3.6$V. This ensures P2 is on and P1 is off. Hence, the output is $V_{BAT}-1.8$V. Thus, we can see that an inversion operation has been performed by just PMOS pass transistors and one NMOS which does not have to face $V_{BAT}$ at its gate. Cascading multiple such stages and scaling them helps us to have a PMOS gate driver. The simulation result of this circuit is shown in Fig 2-9.

![Gate Drive Circuit Simulation](image)

Figure 2-9: Simulation showing the gate drive circuit output with two inputs which are inverted and level shifted versions

Input_1 shows the level shifted input from the previous gate drive stage. This signal goes to the gates of P1 and P4. Input_2_leveled_down is the second input that is the level shifted and inverted version of Input_1 and goes to the gate of N1. Since, Input_2_leveled_down swings between $V_{BAT}-1.8$V and $V_{BAT}-3.6$V, it can be generated using inverters. In this implementation, the circuit generating Input_2_leveled_down and the gate driver for P3 of Fig 2-2 is shared.

Since, the operation is dependent only on PMOS transistors, a lower signal swing
will not effect the functionality. This becomes important when the input is directly from a level shifter instead from the similar predecessor stage. As it was pointed out in a previous subsection, the swing may be slightly reduced due to charge sharing at the level shifter output node. This is only going to reduce the gate overdrive of P1 and P4 in Fig 2-8. This will make the signal transitions slower. By sizing the transistors properly, this effect can be reduced.

2.2 Switched Capacitor Converters

Since the goal of this work is to have a completely integrated converter, all the internal control and regulator circuits need to be powered by the battery which has a voltage between 2.8V to 4.2V. This includes the low voltage control circuit of the buck converter, and the extra regulators for the gate drives and the stack in power stage. A 1.8V Switched Capacitor converter has been designed that gets power directly from the battery and supplies power to all the control and other regulator circuits. As shown in Fig 2-2, there are four SC regulators in this design. VBAT-1.8V and VBAT-3.6V are for the PMOS stack in the power stage. 1.8V SC is used by these stacking regulators and their control to generate the corresponding voltages. The fourth SC is for generating 1.2V for the buck control circuit from the 1.8V SC. Thus, it can be seen that the 1.8V SC is the main converter driving all the other converters in the system.

2.2.1 1.8V Switched Capacitor Converter

Fig 2-10 shows the switch implementation of the 1.8V SC [15]. It also has the simplistic picture of the capacitor orientations at each switching phase. As the battery voltage can vary between 4.2V to 2.8V, we require three gain settings (3 switch configurations) for the SC converter. Reconfigurable switches are used to switch between gain settings. The 1by2 gain setting is used when the battery is fully charged to 4.2V. Once it discharges to 4V, 2by3 gain setting is used. For voltages below 3V, 1by1 gain setting is used.
Considering 1by2 gain setting, the total output current delivered to the output is given by the following expression

\[ I_{OUT} = 4C(V_{BAT} - 2V_L)f \]  

(2.5)

where \( V_L \) is the output voltage of the SC converter, \( f \) is the switching frequency and \( 2C \) is the total charge transfer capacitance. It must be noted that this equation assumes that the load capacitor is large enough to ignore the ripple. Therefore, the output power being delivered is

\[ P_{OUT} = 4C(V_{BAT} - 2V_L)V_Lf \]  

(2.6)

In order to keep the charge transfer capacitors relatively small (within 50pF), the frequency of the SC circuits is 4MHz as compared to the system (buck converter switching) frequency of 2MHz in the PWM mode. In the PFM mode, since the current requirement of all the circuits is less, 1MHz suffices for both SC and the buck converter. The total charge transfer capacitance in the 1by2 gain setting is 45pF. Thus, by using power delivery equation from above, the SC converter can supply
a maximum output power of 300\textmu W, although the NMOS gate drive circuit when the buck converter is operating in the PWM mode consumes only 150\textmu W. This extra margin is kept to ensure that the instantaneous droops in voltage due to the switching activity in the gate drive circuit is minimized. These sudden droops lower the gate overdrive of the NMOS power transistor increasing its on resistance. For the charge transfer capacitors in the SC, metal to metal capacitors have been used. Unlike the gate oxide caps, these can withstand a higher voltage across them. Since the charge transfer capacitors have to transfer the charge from the battery to the load in phase1, they will have a voltage across them that the gate oxide capacitors cannot handle. For a completely on-chip solution, the load capacitors of the SC converters are implemented by using gate oxide capacitors. These capacitors have been sized such that both leakage (<10nA) and voltage droops are kept within acceptable limits of design.

![Figure 2-11: PFM loop of 1.8V SC](attachment:image1.png)

The voltage regulation in the SC converter is done by a PFM loop. This consists of a comparator that triggers when the voltage falls below 1.8V. This sends a signal to the switches of the SC to change phase and hence transfer the stored charge to the load. Fig.2-11 shows the PFM loop details. A clock non-overlapping circuit is used to prevent any short circuit losses when phases change.

For the 1.8V SC, signals to most of the switches have to be level shifted. The level shifters used are the same capacitive coupled level shifters discussed in the previous
section. For the 1.2V SC, the architecture remains the same but no level shifters are used. The simulation results of the 1.8V SC are shown in Fig 2-12 with the level shifted version of φ1_bar and φ2. The SC in this simulation supplies 90µW output power.

![Simulation of PFM loop of 1.8V SC](image)

Figure 2-12: Simulation of PFM loop of 1.8V SC

### 2.2.2 Stacking Converters

There are two stacking converters used in this design. These are battery voltage scalable and provide regulated $V_{BAT-1.8V}$ and $V_{BAT-3.6V}$. From Fig 2-2, the PMOS stack in the power stage requires intermediate voltages to enable proper switching. Fig 2-13 shows the timing diagram of the gate signals. For 4.2V battery voltage, the gate voltage of P1 swings from 4.2V to 2.4V ($V_{BAT-1.8V}$). The gate of P2 is held constant at 2.4V and the gate of P3 gets a signal which is the inverted version of the signal at gate of P1 but swings from 2.4V to 0.6V($V_{BAT-3.6V}$). Therefore, for proper operation of the buck converter, the voltages $V_{BAT-1.8V}$ and $V_{BAT-3.6V}$ should be
well regulated. By design, both these regulators are required to sink in current unlike the 1.8V SC which sources current. Even though the principle of operation is similar to an LDO or a 1by1 gain setting SC converter, its design is slightly different.

![Diagram of gate voltages of the power FETs](image)

Figure 2-13: Gate voltages of the power FETs

Architecture of Stacking Regulators

Fig.2-14 shows the circuits for $V_{BAT}$-1.8V and $V_{BAT}$-3.6V regulators. The main aim is to keep the voltage close to $V_{BAT}$-1.8V and $V_{BAT}$-3.6V. Since, the converter has to be scalable with battery, the references designed for this converter have been made sliding. Stacking three diodes gives us a drop of 1.8V from the battery voltage. Another 3 diodes would give us another reference which is $V_{BAT}$-3.6V. Hence, the sliding diode reference provides the scalability feature required by the stack in order to operate effectively from 4.2V to 2.8V. The converter control is PFM. When the voltage is above the reference, the comparator triggers a switch that provides a path...
to ground for the charge on the $V_{BAT-1.8V}$ load capacitor. Every time the comparator is triggered, a 4ns pulse is used to control the switch so that the voltage does not go all the way to ground. Since the NMOS transistor used in the 4ns delay is the same transistor that is used in the switch to discharge the capacitor, there is automatic process tracking in case there are variations.

![Diagram of voltage regulators](image)

Figure 2-14: $V_{BAT-1.8V}$ and $V_{BAT-3.6V}$ regulators

For battery voltage of 3.6V, the sliding reference for $V_{BAT-3.6V}$ goes to almost 0V. The regulator in this case tries to regulate the voltage to the reference, which is close to 0V. For battery voltages below 3.6V, the regulator still maintains 0V. However, now the PMOS power transistor P3 does not get an overdrive of 1.8V. Due to reduced overdrive, on resistance increases which affects the efficiency.
Fig 2-15 shows the simulation result of the $V_{BAT}$-1.8V regulator. The input current is a $10\mu$A dc current. The comparator triggers when the output goes above the reference. The comparator output is shown along with the reference and regulated voltage.

**High Voltage tolerant Strong ARM comparator**

All the comparators used in the design are similar to the Strong ARM register [16]. However, for the $V_{BAT}$-1.8V regulator, the comparator needs to be slightly modified from the conventional Strong ARM design. For the circuit shown in Fig 2-16, a PMOS transistor is used with a sense amplifier in the comparator. In this circuit, the output nodes $V_{OUT+}$ and $V_{OUT-}$ of the comparator will be swinging between 0 and $V_{BAT}$. Since, these nodes are connected to the gates of transistors NSA1, NSA2, PSA1 and PSA2, the high $V_{GS}$ of $V_{BAT}$ will cause the gate oxide in these devices to breakdown. A capacitive coupled High Voltage tolerant Strong ARM comparator is proposed that alleviates the above mentioned problem. Fig.2-17 shows the circuit for
The High Voltage tolerant Strong ARM comparator decouples the comparing PMOS transistors with the sense amplifier. When the clock is high, both the outputs are high. This is the pre-charge phase. When the clock goes low, the comparator enters the evaluate phase when the sense amplifier (with transistors PSA1,2 and NSA1,2) tries to go into the metastable state. At the same time, depending on the gate voltages of the PMOS transistors, one of them will be conducting more than the other. Current flows through the coupling capacitors and to the PMOS transistors P1 and P2. Depending on which PMOS is conducting more, the corresponding inverter in the sense amplifier goes low and the other inverter output goes high. It must be noted that the outputs are not rail to rail since the sense amplifier is decoupled from the comparing transistors. For a 'high', we get 1.8V output but for a 'low', we do not get 0V but a low value that depends on the charge sharing between the capacitor C1 or C2 and the parasitic capacitance at the source of NSA1 or NSA2. Metal to metal
capacitors are used so that the parasitic capacitors are minimized. To clean up the signal, we use a clocked DCVSL after this stage to ensure the final output is rail to rail. It must be noted that some additional switches are used so that the back to back inverters are connected only during the evaluate period of the comparator. This is done so that both the capacitors C1 and C2 are charged to the same value during the pre-charge phase. Extra switches (S3 and S6) at the bottom plate of the capacitors and P3 ensure this. Since in the pre-charge phase, the inverter (PSA1, NSA1 and PSA2, NSA2) outputs should be the same, extra switches are used to decouple them. Switches S4 and S5 play the role of transistors N1 and N2 of Fig 2-16. The timing simulation diagrams are shown in Fig 2-18.

The clock to the High Voltage tolerant Strong ARM forces both the comparator outputs to high during the pre-charge phase. During the evaluation phase, if the regulated voltage goes above the reference, the comparator triggers as shown. All this is done without any node getting a swing of 0 to $V_{BAT}$ as explained earlier.
It must be noted that this comparator is sensitive to voltage offsets. This requires changing the reference to get the desired regulated output voltage.

**Clock Gating in Stacking Regulator**

The stacking regulators have to continuously regulate the intermediate stacking voltages. When the buck converter is supplying extremely light loads, the PFM control loop power starts to limit the overall system efficiency. At these loads, the regulators can be operated at a much lower frequency as the current to sink is very small. Therefore a clock gating circuit for the stacking regulators is used for light loads.

The main advantage we have in this circuit is that we know beforehand the switching time of the PMOS transistors in the power stage. This means that the time when the stacking regulators need to operate is also known. It is during this time that the clock to these regulators is enabled. After the switching instance of the PMOS transistors in the power stage, the comparator of these regulators gets the
clock and voltage is regulated to $V_{BAT}-1.8V$ or $V_{BAT}-3.6V$. Once the voltage is below this, the clock is disabled thereby reducing the control power. The signal indicating that the voltage is below the reference, is the complimentary of the output signal from the comparator used for the PFM control loop. After this, the clock is enabled only in the next PMOS switching time where a similar operation is done. The circuit doing this clock gating is shown in Fig.2-19.

![Clock Gating Circuit for Stacking Regulators](image)

**Figure 2-19: Clock Gating Circuit for Stacking Regulators**

This circuit is actually the phase detector circuit used in PLLs. Fig 2-20 shows the simulation results of this circuit. When the ‘pmos enable’ signal goes high, the ‘clock enable’ signal goes high too. This is the time when clock is gated to the comparator. When the comparator finishes comparing, it sends back a signal ‘end of evaluation signal from comparator’. The positive edge of this signal indicates that the voltage is below the reference and hence the clock can be disabled. This causes the ‘clock enable’ signal to go low thereby, disabling the clock. Fig 2-20 shows the timing of the signals ‘pmos enable’, ‘end of evaluation signal from comparator’, gated clock and the non-gated clock.
2.3 Control Architecture

To account for the battery discharge and load transients, we need to have a robust feedback control so that the buck converter can provide a clean, regulated output voltage. Since we have to deal with a large load range both PWM and PFM modes of control are employed. Fig 2-21 shows the architecture of the control circuit. This section describes the three main parts of the control circuit, DPWM, PFM control and PWM control.

2.3.1 PWM control

For the PWM loop, a multi-bit control is used. The loop consists of a ADC, a PID controller and the DPWM as shown in Fig 2-21. In this design, a 4 bit Flash ADC was implemented. The ADC digitizes the output voltage of the buck converter. This digital output is subtracted from the reference voltage which is also in the digital
domain. The subtracted data is then processed by the PID controller. The PID controls the DPWM input such that the output of the buck converter is very close to the reference voltage. For this design, the DPWM has 5 bits, but by dithering, 1 extra bit is added to give 6 effective bits in the DPWM. To prevent limit cycles in the output [17] the number of ADC output bits have to be at least one less than the number of bits in the DPWM. The number of dithering bits can be increased however, this would require a Delta-Sigma architecture with a faster clock. This work, unlike [10] deals with extremely low power levels. Therefore, having a very fast clock for oversampling would increase the control power and would hurt the efficiency.

ADC

In this design, the ADC was designed using strong ARM latches and a resistor string to create the reference voltages. Resistors have been sized such that the total static power consumption in the resistors is less than 1μW. Higher resolution ADCs in PWM loops have earlier been demonstrated in [10] and [9]. Since, the goal of this design was to demonstrate the feasibility of the converter in 45nm, a low resolution ADC was designed. The ADC resolution can be increased at the expense of increased com-
plexity. The clock is the same as the PID control clock which is at 1MHz frequency. The ADC block diagram is shown in Fig 2-22.

**PID controller**

The PID controller implemented is a digital FIR filter with hard-coded coefficients. The FIR filter expression implemented is as follows.

\[ y(n) = y(n-1) + 1.03125 \times x(n) + 2 \times x(n-1) - x(n-2) \] (2.7)

The FIR filter was implemented by using static CMOS logic. All the computation was done on a 6 bit binary representation. The LSB was the dithering bit that
went to a dither modulator and the 5 MSBs went to the DPWM. For simplicity in implementation, the FIR filter coefficients were selected such that they can be easily implemented using shifters and adders. The measured transient for this PID is given in the next chapter under the Transient Response subsection.

2.3.2 PFM control

To cater for loads less than 10mA, the PFM mode of control is used in this design. The principle of PFM mode is to supply power on demand. The PFM loop as shown in Fig 2-21, consists of a comparator and the DPWM. When the output voltage of the buck converter falls below the reference, the comparator sends a pulse to the DPWM. The DPWM on getting this signal sends two signals, one for the PMOS power transistors and the other for the NMOS power transistor. The first signal is that of the PMOS power transistor. This pulse is of a fixed width $t_P$. An analysis in this section later will show how $t_P$ was selected in order to get optimum efficiency. Following this, another pulse of width $t_n$ is sent to the NMOS power transistor. The timing of these signals is shown in Fig 2-23. The width $t_n$ is dictated by the condition that on a per cycle basis at periodic steady state, the average voltage across the inductor has to be zero. This gives us the following condition.

$$(V_{BAT} - V_{OUT})t_P - V_{OUT}t_n = 0 \tag{2.8}$$

This simplifies as

$$t_n = (V_{BAT}/V_{OUT} - 1)t_P \tag{2.9}$$

$V_{BAT}$ is the battery voltage and $V_{OUT}$ is the regulated voltage. This is necessary for zero current switching (ZCS) to increase efficiency. The method to do ZCS is explained in a subsection later.
Determining the optimum $t_p$

Total conduction and switching loss in the PFM mode is given by the following expression

$$loss = \frac{((V_{BAT} - V_{OUT})t_p^2(R_p + R_n)f)}{(3L) + C_T V_{DD}^2 f}$$  \hspace{1em} (2.10)$$

As the frequency depends upon the output load,

$$I_{OUT} = \frac{((V_{BAT} - V_{OUT})t_p^2 V_{BAT}f)}{(2L)}$$  \hspace{1em} (2.11)$$

Therefore, the total loss can be expressed as

$$loss = 2I_{OUT}[\frac{((V_{BAT} - V_{OUT})(R_p + R_n)t_p)}{(3L) + (LCTV_{DD}^2)}]/(V_{BAT})$$  \hspace{1em} (2.12)$$

This expression can be written in the general form of
\[ \text{loss} = a \cdot tp + \frac{b}{tp^2} \]  

(2.13)

where \(a\) and \(b\) are constants depending on the battery voltage, output voltage and the load current. Here too, we notice that we have an optimum value of \(tp\) given by

\[ tp_{\text{optimal}} = \sqrt[2]{\frac{b}{2a}} \]  

(2.14)

The normalized curve for Eq 2.13 is shown in Fig 2-24. For the battery range from \(V_{BAT} 2.8\text{V}\) to \(4.2\text{V}\) and output from \(0.4\text{V}\) to \(1\text{V}\), this optimum \(tp\) varies from \(60\text{ns}\) to \(170\text{ns}\). In this design a fixed \(tp\) of \(120\text{ns}\) was used to cater for a wide range of conditions.

![Figure 2-24: Total Loss with optimal tp](image)

Since, the NMOS on time, \(tn\) depends on the battery voltage and the output voltage, it needs to be changed as the battery discharges. For this, a ZCS circuit [18] is designed to ensure that the NMOS on time is automatically set. Fig 2-23 shows
the ZCS condition, however due to ringing at the drain of N1, the key points may not be visible on this plot. Fig 2-25 illustrates the concept in a graphical format. ZCS ensures high efficiency as the loss through the parasitic diodes is minimized. In the PFM mode, the inductor current ideally should go to zero when the NMOS is switched off. However, due to limited resolution of the DPWM, the inductor current may be positive or negative when the NMOS is switched off. If NMOS is on for a period which is more than it should be for ZCS, then inductor current is negative. If NMOS is on for a shorter period than required for ZCS, inductor current is positive. If negative, then the remainder of the current goes through the diode D1 through a switch S1 with the PMOS transistors which causes the drain voltage to rise one diode drop above ground. The switch S1 is controlled by a delayed version of the NMOS gate signal ph2. On the other hand, if the inductor current is positive, the drain voltage will be one diode drop below ground as the parasitic diode $D_{parasitic2}$ of NMOS N1 will be conducting. By comparing the drain voltage at the right time, we can design a control circuit that would keep toggling between the two states, one when the inductor current is positive, the other when its negative.

### 2.3.3 DPWM architecture

The Digital Pulse Width Modulator (DPWM) is the main driving block of the control section for the buck converter. It produces pulses of a fixed time duration which are signals that drive the power stage transistors. For low power DC-DC converters, digital control is usually employed. This involves having a delay line with multiplexers [12] that select the pulse width that needs to be sent to the power stage. Fig 2-26 shows the circuit for such a DPWM architecture. The same concept of pulse width modulation is done by using a high frequency clock instead of a delay line. This approaches [11] and [10] can be power hungry due to the fast clock. Table 2.1 summarizes a comparison between the commonly used techniques. There may be other variants of these techniques but principle of operation of each of those can be mapped to one of the following techniques.

At scaled technologies like 45nm, the switching frequencies of power converters
are much higher than the design in [9] as the transistors are faster and have lower gate capacitance. However, this design uses high voltage FETs forcing us to use more traditional switching frequencies used for older generation power converters. For the DPWM architecture like [9], a lower switching frequency would require large delays which would be area consuming. When operating at 2MHz PWM, in the worst case, we require a pulse width of 215ns ($V_{OUT}=1.2V$ and $V_{BAT}=4.2V$) and for 1MHz PFM, in the worst case, we require a pulse width of $1.2\mu s$ for $tn$ as described by Eq 2.9 for the given $tp$, $V_{BAT}=4.2V$ and $V_{OUT}=0.4V$.

Using the delay-line, counter based approach is extremely area consuming which will make the design cost ineffective at 45nm. In this design, we use the compact analog technique of charging a capacitor with a constant current and comparing the
Table 2.1: DPWM techniques

<table>
<thead>
<tr>
<th>Case</th>
<th>[12]</th>
<th>[11] and [10]</th>
<th>the analog technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method</td>
<td>Delay-line and High speed clock counter based. and multiplexer</td>
<td>Select the corresponding pulse using a multiplexer</td>
<td>charging a capacitor using a current source and comparing voltage with reference</td>
</tr>
<tr>
<td>Power</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Area</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>

Figure 2-26: Delay line based DPWM architecture

Voltage with a reference. This normally requires a continuous time analog comparator that has continuous power dissipation. Instead, a sleep control mechanism is used that gives significant power savings especially when the converter is operating in the PFM mode. The DPWM circuit is shown in Fig 2-27. The capacitance to be charged is controlled digitally by switches D0 through D4 and their compliments. The analog comparator operation can be split into the comparison phase and the sleep phase. The rising edge of the system clock (at switching frequency) is used to wake up the analog comparator, thus starting the comparison phase. The reset signal forces the top plate of the effective capacitor to 0V. The current source P1 then starts to charge the capacitance. When the capacitor voltage exceeds the reference, the comparator output flips, ending the comparison phase. P2 forces the capacitor top plate to 1.2V, preventing any further current flow through P1. Since, the analog comparator second
stage is essentially a latch that stores the comparison result, using an additional SR latch, sleep and sleep_bar signals are generated that power off the comparator thus preventing any further power consumption. This is the beginning of the sleep phase. Thus, by leveraging the fact that the time instant of comparison is known, we can reduce the overall power consumption. Also, the comparator quiescent current is effectively duty cycled between the comparison and sleep phases.

Table 2.2 makes a comparison of performance between the proposed DPWM and the delay based DPWM in this technology. It must be noted that the power numbers for delay based DPWM are estimated numbers and do not include the leakage. These numbers may increase further as the number of transistors will be much more in the
Table 2.2: comparison of DPWM performance

<table>
<thead>
<tr>
<th>Case</th>
<th>delay-line based</th>
<th>proposed design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power in PWM</td>
<td>24μW (estimated)</td>
<td>15μW</td>
</tr>
<tr>
<td>Power in PFM</td>
<td>156nW (estimated)</td>
<td>159nW for 20μW output power</td>
</tr>
<tr>
<td>Area</td>
<td>0.042mm²</td>
<td>0.01mm²</td>
</tr>
</tbody>
</table>

delay based DPWM.

With proper matching of layout of capacitors, a linearity of DPWM is ensured. Mismatches do not present a very big problem in such systems due to negative feedback. Mismatches can lead to non-linearities which may cause limit cycles. However, if the number of ADC bits is atleast one less than the number of DPWM bits, chances of these limit cycles are minimized. Also, any offset in the analog comparator is compensated by the negative feedback loop. Therefore, the proposed design due to negative feedback does not suffer from the common problems in analog circuits.

Fig 2-28 shows the simulated waveforms of the capacitor voltage and the reference. When the capacitor voltage is close to 0V, the comparator is powered on. As the current source P1 of Fig 2-27 charges the capacitor, the voltage increases linearly. When this exceeds the reference, the comparator output flips as forcing the capacitor voltage to rise further due to P2 of Fig 2-27. At this time instant the comparator is powered off. The linearly rising part represents the pulse width that is to be sent to the power FETs. Fig 2-29 shows the simulated results of the comparator current (duty cycled), the sleep signal used to power off the comparator and the pmos signal going to the power FETs.

2.3.4 Chapter Summary

This chapter presents the design details of the DC-DC converter. The fact that the design has to handle high voltages at 45nm presents several circuit challenges. These have been addressed here. The architecture with stacking in the power stage, 1.8V SC converter with level shifters, stacking regulators and their clock gating and high
Figure 2-28: Capacitor voltage increasing linearly with time

Voltage handling techniques are the key features of this chapter. Towards the end, a DPWM architecture is also presented, that is compact like the high power analog technique of capacitor charging but is also low power like the digital technique of delay based circuits at the same time. Analysis showing how to size the power FETs and how to select the delays in the PFM loop was also shown.
Figure 2-29: Simulated waveforms showing the comparator current, sleep signal and the DPWM output to PMOS power FETs
Chapter 3

Measurement Results

The design was fabricated using Texas Instruments’ 45nm Digital CMOS process.

3.1 Die Micrograph and Board

![Die Microphotograph](image)

Figure 3-1: Die Microphotograph

Fig.3-1 shows the die microphotograph. The core area is about 1.5mm by 1.5mm. The power FETS occupy 0.580mm x 0.230mm. Most of the area is occupied by...
the SC load capacitors. Also, a large part of the area goes into the charge transfer capacitors in the 1.8V SC and the load capacitor in $V_{BAT}$-1.8V regulator as these have been implemented using metal to metal capacitors. Fig.3-2 shows the board for the packaged chip that was tested.

![Figure 3-2: Board with IC and off-chip components](image)

### 3.2 Efficiency Plots

Fig.3-3 shows the measured efficiency of the converter. This does not include the references. For multiple battery voltages and for the whole range from 40μA to 100mA, we can see that the efficiency is >70%. For high battery voltages like 4.2V, the leakage dominates the power loss at light loads. For 20μA to 10mA, the converter operates in PFM mode. For 10mA to 100mA, PWM mode is used. The peak efficiency in the PWM mode is 87%. For all these measurements, the output voltage was regulated to 1V.

It can be seen that the measured efficiency is slightly lower than what was obtained from simulations. In fig 2-4, the breakup of losses in the power stage was shown. For
60mW output power at 4.2V battery voltage, the measured efficiency is 87%. This is about 3% lower than simulated efficiency. Fig 3-4 shows the breakup with the overall loss. 4.3mW of power loss in power stage and 0.5mW loss in the 1.8V SC is expected from simulations. Since, the simulations were pre-layout simulations, the extra layout parasitics were absent. An estimate of 0.5Ω was made from the layout. This causes 1.5mW of conduction loss. An extra 10pF of board capacitance is also considered causing 0.4mW of switching loss. This leaves us with 1.5mW of unexpected power loss. There could be multiple reasons for this. Some are summarized as follows:

1. Core loss in the inductor at 2MHz.

2. The model of the high voltage NMOS might have been a little off. The device used is still under development.

3. The extra CV^2 losses in the control and 1.8V circuit.
3.3 Transient Response

PFM mode

The circuit was tested for load transients. Here, the load transients in the PFM mode have been presented. This is to ensure that even when the load current suddenly changes, the regulated voltage should not change too much so that the load circuit is not affected. Fig.3-5 shows the transient response when the load current changes from 100μA to 5mA and Fig.3-6 shows the transient response when load current changes from 5mA to 100μA. The ripple overriding the regulated voltage of 0.8V is less than 20mV. Hence, this is less than 2.5% of the voltage being supplied.

PWM mode

The load transient for the PWM mode is shown in Fig 3-7. The regulated voltage is 1V and the load is changed from 10mA to 50mA and vice versa. We can see the variation is less than 20mV in the final regulated voltage.
3.4 Comparison of Measured Results

This work is able to achieve comparable efficiencies in the medium power level and much higher efficiencies at the ultra low power level (10s of µW). Table 3.1 shows a comparison of the measured data with previously published work.

It can be seen from Table 3.1 that our design covers four orders of magnitude of load range. Work in [9] also covers a large range but it is a 0.25µm design. The cited design had 2 PMOS and 2 NMOS transistors in its power stage. This made the design simpler with just one stacking regulator and the same being used for control. The power transistors were also 0.25µm devices which are actually faster than the high voltage devices we used for our design (NMOS in the power stage of design is a 1.2µm device). Also, performance of the circuit with change in battery voltage is not shown. Since the stacking regulator sets the voltage to half the battery voltage, this would affect the control circuit and its performance as it has a ADC and delays which need a stable supply. In this work all these issues have been taken care of by having a dedicated supply for control (1.2V SC), separate supplies for stacking (V_{BAT}-1.8V, V_{BAT}-3.6V) and a separate supply for driving all the regulators for control, stacking and gate drivers (1.8V SC).
Figure 3-6: Load Transient from 5mA to 100uA

[13] is a commercial design that uses a process that allows us to handle high voltages without any stacking. In the table given above, our design achieves the highest efficiency in the low power regime. In the high power domain (0.1W), the stacking in the power stage affects the efficiency. However, 87% efficiency was still obtained for 0.1W. Thus for the whole range from 20μW to 0.1W, making this a competitive design in 45nm. Therefore, even after integrating the PMU with the 45nm core to lower the system cost, the DSP/baseband will be almost as energy efficient as it would have been with a PMU chipset.
Figure 3-7: Load Transient from 10mA to 50mA and vice versa

<table>
<thead>
<tr>
<th>Case</th>
<th>[9]</th>
<th>[13]</th>
<th>Target for this work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25um</td>
<td>process capable of handling high voltages</td>
<td>45nm</td>
</tr>
<tr>
<td>Nominal Supply Voltage</td>
<td>2.5V</td>
<td>-</td>
<td>1.1V</td>
</tr>
<tr>
<td>Battery Voltage</td>
<td>2.8V to 5.5V</td>
<td>2.7V to 6V</td>
<td>2.8V to 4.2V</td>
</tr>
<tr>
<td>Output Power</td>
<td>150μW to 0.6W</td>
<td>90μW to 0.54W</td>
<td>20μW to 0.1W</td>
</tr>
<tr>
<td>Stacking in power stage</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Regulators for control</td>
<td>Yes LDO but fixed to $V_{BAT}/2$</td>
<td>No</td>
<td>Completely on chip SCs and stacking voltage regulators generating 1.2V, 1.8V, $V_{BAT}$-1.8V and $V_{BAT}$-3.6V</td>
</tr>
<tr>
<td>Peak Efficiency for ultra-low power</td>
<td>70% for 150μW</td>
<td>65% for 90μW</td>
<td>75% for 20μW</td>
</tr>
<tr>
<td>Overall Peak Efficiency</td>
<td>91% for 300mW</td>
<td>95% for 90mW</td>
<td>87% for 60mW</td>
</tr>
</tbody>
</table>
Chapter 4

Conclusion and Future Work

4.1 Main Contributions

This thesis presents a high voltage direct battery DC-DC converter in 45nm. The main contributions are as follows:

1. Architecture for a completely self-contained direct battery DC-DC with stacking in power stage at the 45nm node. Challenge comes in integrating all the stacking regulators, SC converters, PWM and PFM control and the main buck converter to enable power conversion from such high battery voltages at a scaled technology like 45nm.

2. Efficiency of >70% for the wide range from 20μA to 0.1A and peak efficiency of 87%. This is the widest load range reported covering 4 orders of magnitude.

3. Novel DPWM architecture consuming 1/3rd the area of the conventional DPWM having comparable power. By using an analog technique of charging a capacitor by a current source and comparing the voltage with a reference, we are able to get a compact DPWM. Since we know the exact time when we want the comparator to start comparing, we enable the comparator at the beginning of the switching phase. The comparator is powered off when the comparison is made thus reducing the power consumption. This enables us to have a compact and low power operation which is essential when loads below 100μA are considered.
4. Novel clock gated stacking regulators for power stage.

5. Pass transistor based gate driver circuit.

### 4.2 Design Summary

Table 4.1 presents a design summary. As mentioned, this is the widest range DC-DC converter reported covering 4 orders of magnitude. Having extra devices in the power stage for high voltage protection causes the losses to increase, making design of highly efficient converters challenging for the wide load range.

<table>
<thead>
<tr>
<th>Case</th>
<th>Measured Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>45nm 1P7M Digital CMOS</td>
</tr>
<tr>
<td>Battery Voltage</td>
<td>2.8V to 4.2V</td>
</tr>
<tr>
<td>Output Power</td>
<td>20µW to 0.1W</td>
</tr>
<tr>
<td>Load Current</td>
<td>20µA to 0.1A</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>0.4V to 1.1V</td>
</tr>
<tr>
<td>PWM switching frequency</td>
<td>2MHz</td>
</tr>
<tr>
<td>SC switching frequency</td>
<td>1MHz in PFM, 4MHz in PWM</td>
</tr>
<tr>
<td>Inductor</td>
<td>10µH</td>
</tr>
<tr>
<td>Capacitor</td>
<td>2µF</td>
</tr>
<tr>
<td>Peak Efficiency</td>
<td>87% for 50mW at 3V battery</td>
</tr>
<tr>
<td>Efficiency for low power levels</td>
<td>75% for 20µW at 3V battery</td>
</tr>
</tbody>
</table>

### 4.3 Further Work

Some ideas to further improve the design are as follows:

1. The DC-DC converter may be merged with the battery recharging circuit. When the battery is being charged, the core circuits can be powered directly, from the DC supply, instead of through the battery. This would involve some extra control but would ensure that the Li-ion battery is being charged effectively minimizing the number of discharge cycles, increasing the battery lifetime.
2. In this design, the reference voltages were set by the user externally. In a more practical design, the system would be employing Dynamic Voltage Frequency Scaling (DVFS). In this case, some interaction is required between the load circuit and the DC-DC converter to set the reference voltage for low power operation.

3. A sensor circuit can be implemented to switch between PWM and PFM modes and vice versa as the load changes.

4. The PID controller in this design has coefficients hard coded. A better implementation would be a converter that can be programmed on the fly so that the transient response can be adjusted when wanted.
Bibliography


