Real-Time Analog Acquisition of Electrophysiological Signals with Soma

by

Eric Michael Jonas

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Submitted to the
Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Masters of Engineering in Electrical Engineering Computer Science

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Abstract

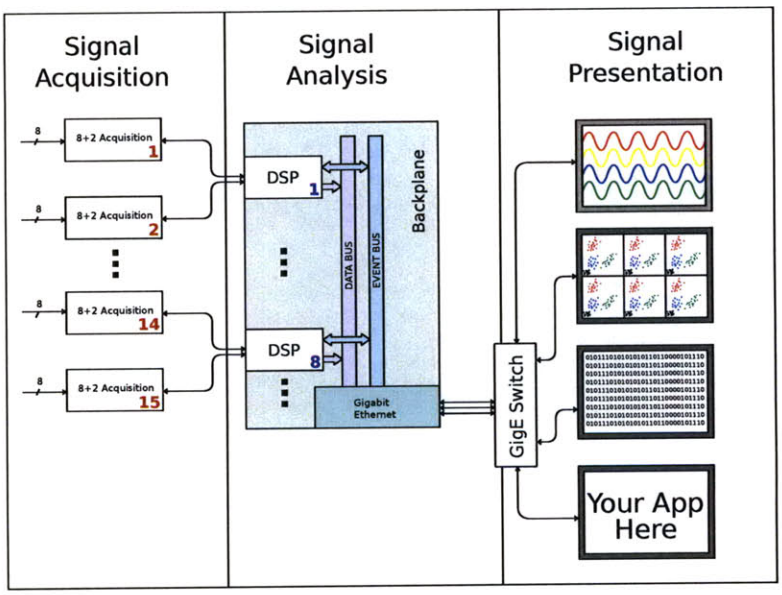
Soma is a high-density recording system for real-time acquisition and analysis of extracelluar electrophysiological signals. Here I describe the design, implementation, and evaluation of the Soma Acquisition Board, an 8-channel low-latency amplifier for amplification and digitization of these signals. Design trade-offs are discussed, and the resulting analog performance is quantified.

Thesis Supervisor: Matthew A. Wilson
Title: Professor of Brain and Cognitive Sciences

Preface

"I remember when your project was just an 8051" - Vimal Bhalodia

Soma is a high-density recording system for real-time acquisition and analysis of extracellular electrophysiological signals. Here I describe the design, implementation, and evaluation of the Soma Acquisition Board, an 8-channel low-latency amplifier for amplification and digitization of these signals. The Acquisition Board feeds into the "Analysis" subsystem consisting of the Soma DSP Modules, Backplane, and Network Interface, which in turn transmit packetized filtered data out over the network.



Soma was motivated by frustrations with the existing technical quality, design transparency, and performance of contemporary solutions for acquiring electrophysiological data. Even when this project began in 2003, it seemed inevitable that the next generation of neuroscience experiments would include a substantial real-time manipulation component.

The Acquisition Board was the first part of Soma that I designed, and in many ways is the most complex. Mixed-signal design is always a headache, and the acquisition board is no exception – the bill-of-materials lists over four hundred components, driven by six different power supply rails. Simply figuring out how to test the board was a challenge, culminating in us purchasing a $10,000 signal generator traditionally used for measuring the performance of high-end audiophile equipment.

I can't say there weren't mistakes along the way, or that knowing what I know now, I wouldn't have done things differently. But the acquisition board is versatile enough that, if I'm lucky, I

may never have to design another electrophysiology amplifier again. Thus, this document, and the associated source code (available at http://github.com/somaproject/acqboard) should be viewed as a reference design for others looking to implement similar designs.

Acknowledgments

Soma began as an M. Eng. and grew into something much larger. The extensive engineering involved would not have been possible were it not for the support and encouragement of my parents over all these years. They were willing to tolerate their seven-year-old's solder fumes and incessant requests to buy parts at Radio Shank, and encouraged me to embrace my curiosity and follow my passions (even if they couldn't help me with the specifics of the NE555 timer IC).

So thank you, Mom and Dad – I know my MIT journey has taken longer than any of us anticipated, but I hope you'll agree that it's been worthwhile.

Eric Jonas, August 20 2009

Contents

Chapter 1

Requirements

High-density extracellular electrophysiology is made possible by measuring microvolt-level signals in hostile environments meters away from the source. The exact requirements to achieve this scientific goal are enumerated below, focusing on signal amplification, common-mode rejection, bandwidth, and noise.

1.1 Differential Amplification

Most electrophysiological measurements are measurements of an electrical potential – a voltage. Like all electrical potentials, this signal is measured between two points, which we think of as an active point V_{IN} and a reference point V_{REF}.

Additional sources of voltage relative to ground are present on both of these inputs, generated by uncontrolled environmental sources. This *common-mode voltage* is common to both inputs, and can be partially removed by the differential amplification. In practice, manufacturing tolerances and input impedance differences prevent complete removal of common-mode voltage.

1.2 Input range, amplification, and resolution

The voltages encountered in neural systems can vary over orders of magnitude. Even when measuring the same phenomena, differences in electrode configuration and reference placement can result in a tenfold difference in required amplification. Thus, electrophyisology amplifiers are equipped with programmable gain amplifiers, allowing dynamic range to vary with the signal of interest.

For example, existing equipment in the Wilson lab allows for 12-bit sampling of input voltages with full-scale 20 mV (gain = 1,000) to 500 uV (gain = 40,000). This allows for LSB sizes between 4.8 mV and 122 nV, although system noise performance makes the latter number unattainable [10].

1.3 Bandwidth

Electrophysiological phenomena in the brain can be loosely divided into high-frequency, discrete events and low-frequency, continuous signals. Neural action potentials ("spikes") comprise the first category, with frequencies of interest between 1 kHz and 8 kHz. Electroencephalogram and local field potentials are believed to be the aggregate synchronous activity of large brain regions, and make up the bulk of the latter group. These slower-wave signals extend from 200 Hz down to near-DC levels.

Thus any electrophysiological system will need to be able to isolate the higher-amplitude, low-frequency LFP from the low-amplitude, high-frequency spikes, and do so using controlled filtering that prevents saturation of downstream signals. An aggregate bandwidth of 10 kHz is thus necessary.

1.4 Noise

Even in the absence of any common or differential input, all amplifiers still generate internal electrical noise, which is measured relative to the input. This noise corrupts input signals and is generally white, thwarting attempts to remove it with signal processing. Input noise can directly contribute to cluster size for multiunit recordings, making unit isolation more difficult.

Current amplifiers in use have a manufacturer-measured input noise of 20 uV peak-to-peak [10]. This can have a substantial impact on recorded peak amplitude of a common 200 uV spike.

1.5 Phase

Electrophysiological signals, in particular the local-field potential, vary in frequency over three orders of magnitude. Frequently we are interested in the precise phase relationship between different frequency signals, which necessitates a filtering scheme that exhibits a "linear phase" offset with frequency (i.e. constant group delay).

1.6 Electrical isolation

We are looking for fantastically small electrical signals in electrically hostile environments. While we can attempt to control the intra-equipment electrical environment, the presence of high-speed digital signals nearby makes this a challenge. We can not control the external environment, which is plagued by everything from noisy desktop PCs (ground noise, radiative noise) to nearby industrial centrifuges (ground noise) and 802.11 Wi-Fi access points (radiative interference). Thus we need our electrical environment to be as controlled as possible, and ideally we should isolate our analog front-end from all possible digital contamination.

1.7 Cost, size, number of channels

Tetrode-array electrophysiology uses bundles of four wires (the tetrode) to more robustly pinpoint the point sources of extracellular voltage. Arrays of tens of these tetrodes result in extremely high channel counts – 32 tetrodes might measure sources occupying less than a cubic millimeter of biological tissue, and necessitate 128 independent amplifier channels.

Chapter 2

Signal Chain

This chapter outlines the design and implementation of the primary Soma Acquisition Board signal processing chain, from low-level differential input to encoded binary data. This reflects high-level design only, with all figures reflecting simulation and design specification.

The Soma Acquisition Board signal chain can be partitioned into an analog signal acquisition section and a digital signal processing section. The signal acquisition section amplifies the differential input and scales the signal to make maximal use of the analog-to-digital converter. Digital signal processing removes aliased components, frames the data, and encodes the resulting optical output signal.

Signals are divided into two sets of four (A1-A4, B1-B4) with each set having an optional fifth channel (AC and BC, respectively) (Figure 2-1).

2.1 Input Differential Amplification

Eight input channels with high common-mode rejection accept +/- 20 mV. A constant differential input gain of 100 preamplifies weak input signals, removing common-mode contamination. To accommodate the large DC offsets inherent in most electrophysiology recording environments, the inputs are AC-coupled.

2.1.1 Optional analog high-pass filtering

Low-frequency (1-200 Hz) local field potential (LFP) oscillations can range to several millivolts. The higher-frequency extracellular action potentials (spikes) are normally sub-millivolt. When recording spikes the larger-amplitude LFP could potentially saturate our amplifier; thus we have an optional single-pole high-pass filter (f_{-3dB}=300 Hz) that can optionally remove these low-frequency oscillations and maximize spike acquisition dynamic range.

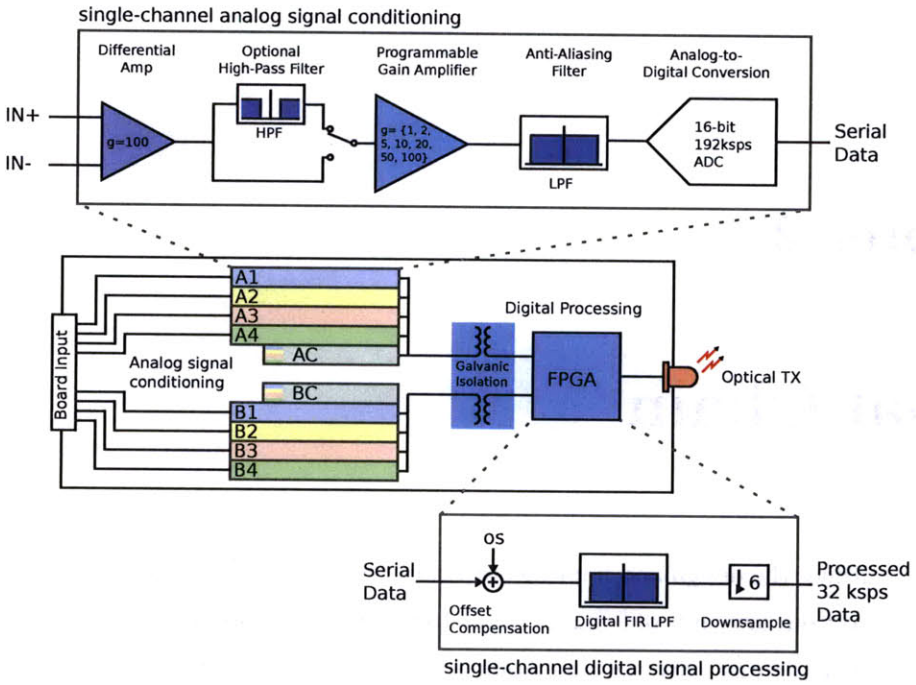


Figure 2-1: The Soma Acquisition Board signal processing chain.

Each group of four input channels feeds into an optional fifth channel (AC and BC) which can independently filter the differentially-amplified input. This allows for each bundle of four channels to record high-frequency, low-amplitude spike signals and to simultaneously record the low-frequency, higher-voltage LFP.

2.1.2 Programmable gain

The programmable gain amplification stage ranges over two orders of magnitude. The table below shows the PGA gain, total system gain, maximum input voltage, and LSB size for the possible settings.

PGA gain	Total Gain	Input Voltage Range	LSB size
1	100	+/- 20.480 mV	625 nV
2	200	+/- 10.240 mV	312 nV
5	500	+/- 4.096 mV	125 nV
10	1000	+/- 2.048 mV	62.5 nV
20	2000	+/- 1.024 mV	31.3 nV
50	5000	+/- 0.410 mV	12.5 nV
100	10000	+/- 0.205 mV	6.3 nV

2.1.3 Analog to Digital Conversion

To achieve 16-bit resolution with an input bandwidth of 10kHz, we oversample the input signal, downsample, and digitally filter. This allows us to use a more lenient analog antialiasing filter at the cost of sampling at a faster rate. The filtering process is the combination of the following factors:

- an initial antialiasing filter
- The analog-to-digital conversion step
- fixed-point FIR filtering
- downsampling

Antialiasing Filter & ADC

To achieve our desired sampling rate, an 8-pole Bessel filter achieves greater than 90 dB attenuation within the stop-band (figure 2-2) while maintaining linear phase (constant group delay) across the passband (figure 2-4). Over the desired 10 kHz bandwidth the filter droops 1.5 dB (figure 2-3)

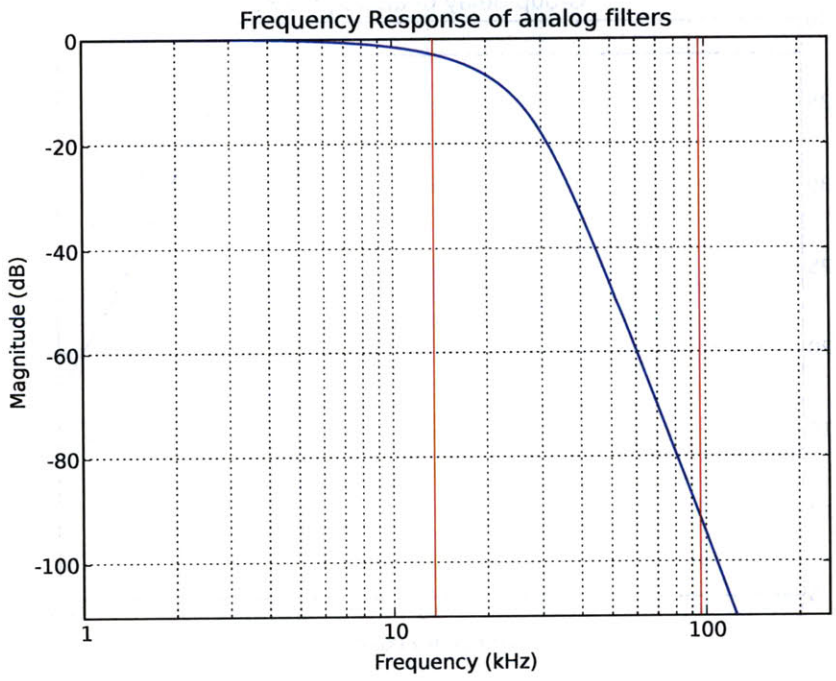


Figure 2-2: Anti-aliasing filter total frequency response.

A 16-bit ADC running at 192 kSPS samples the resulting antialiased signal.

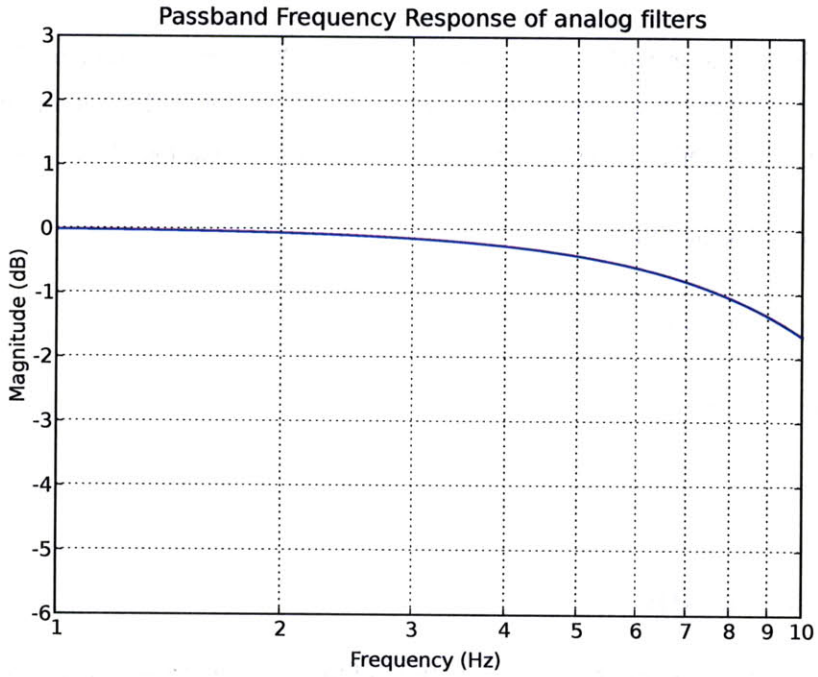


Figure 2-3: Antialiasing filter passband frequency response

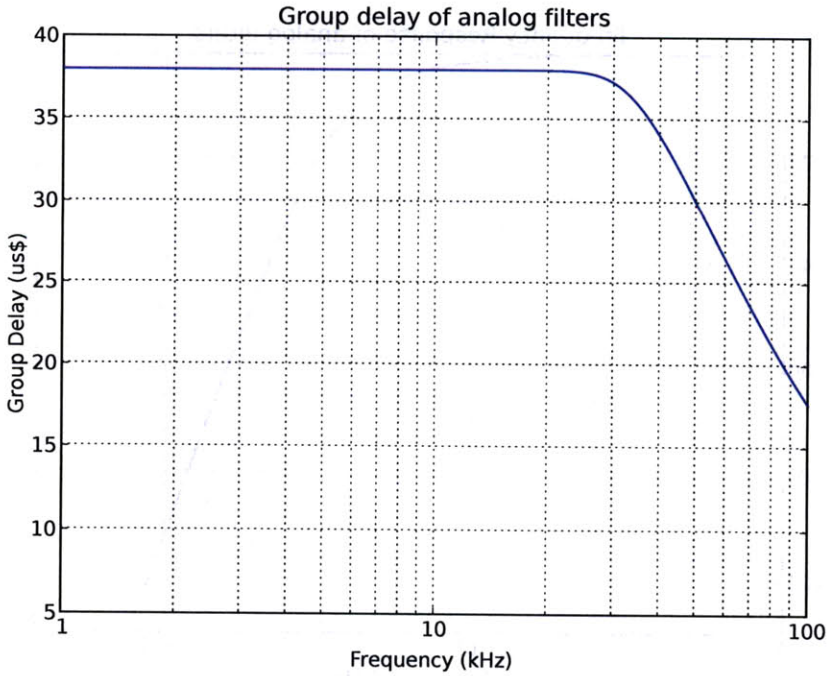


Figure 2-4: Anti-aliasing filter group delay.

Filtering

We filter the sampled data using an 143-Tap FIR filter using fixed-point convolution. We use an extended-precision multiplier, 22-bit filter coefficients, and an extended-width accumulator to reduce the quantization artifacts.

The Parks-McClellan optimum equiripple FIR filter design algorithm is used to compute the coefficients for the 143-tap filter with passband cutoff at 10 kHz. The resulting frequency response (and coefficient-quantized frequency response) are seen in the figure below (figure 2-5). The 143-tap filter gives the required stopband attenuation while keeping FIR-induced passband ripple to under 0.5 dB, while fitting in our allocated FPGA resources.

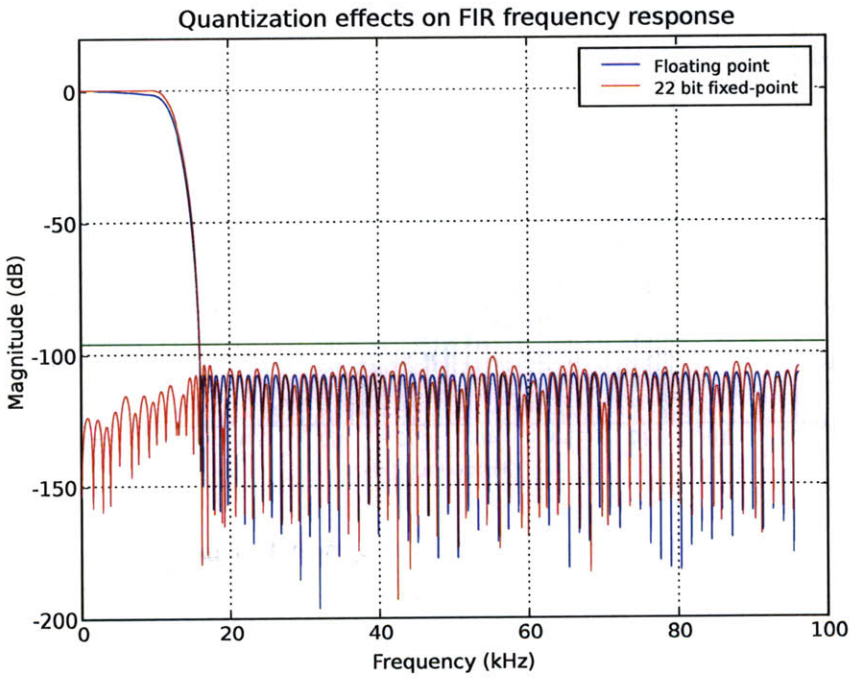


Figure 2-5: Frequency response of FIR filter, both ideal (float-point) response and the filtering performance when coefficients are quantized to 22 bits.

Downsampling

We filter and then downsample; the filtering step is actually only performed once for every M=6 input samples, as the other M-1 samples would be removed in the decimation step and thus be wasted.

2.2 Total response, designed and measured

The resulting frequency response of the combined analog and digital filters are shown in figures 2-6, including zoomed-in passband (figure 2-7) and stopband performance (figure 2-8). The frequency response following decimation is also shown, with the sum of the (imperfectly filtered) antialiased components highlighted. Note that this gives us a theoretical signal-to-alias ratio in excess of 100 dB, below that of our ADC quantization noise floor.

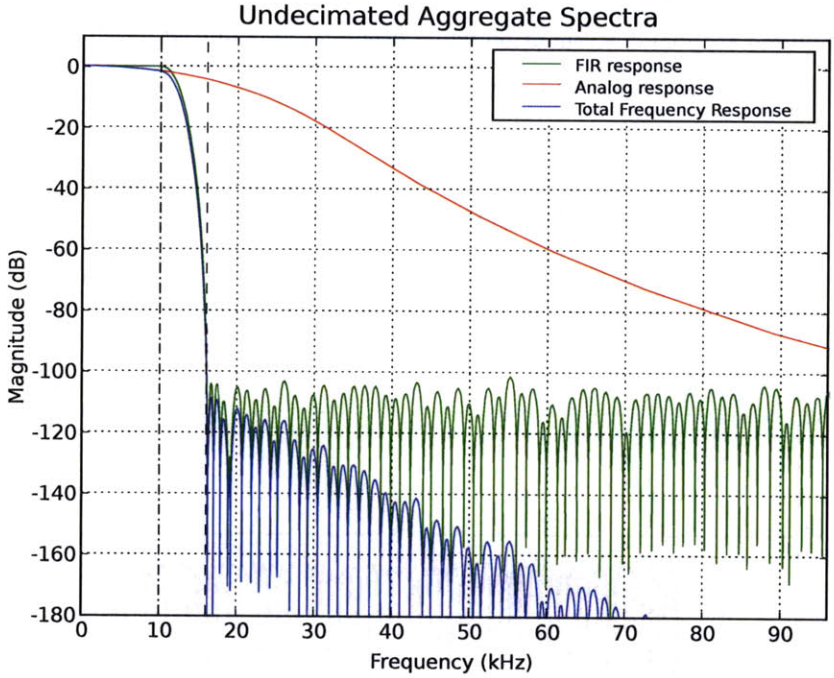


Figure 2-6: Aggregate pre-decimation signal chain filtering.

2.3 Digital Output

The resulting sampled bytes are transmitted at 32 ksps over an 8MHz 650nm 8b/10b-encoded link. A separate input 8b/10b link sends commands to control gain, filter settings, and the like. This allows complete long-haul electrical isolation between the acquisition system and the downstream noisy digital analysis.

Transmission of a serial bitstream requires the receiver to synchronize to the transmitting clock so as to determine bit boundaries. Transitions between one and zero bits can be used to infer the clocking parameters, but long strings of ones or zeros may result in a gradual precession and, eventually, a bit error. To prevent this, we use the 8b/10b encoding scheme.

8b/10b encodes 8-bit symbols in 10 bits of data [15] selecting code words to guarantee a bit

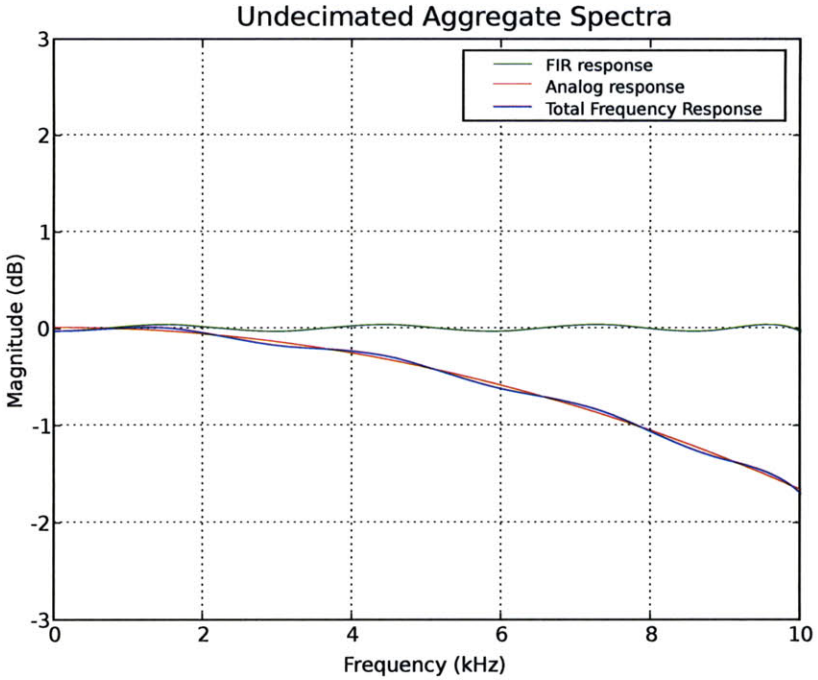


Figure 2-7: Aggregate pre-decimation signal chain passband.

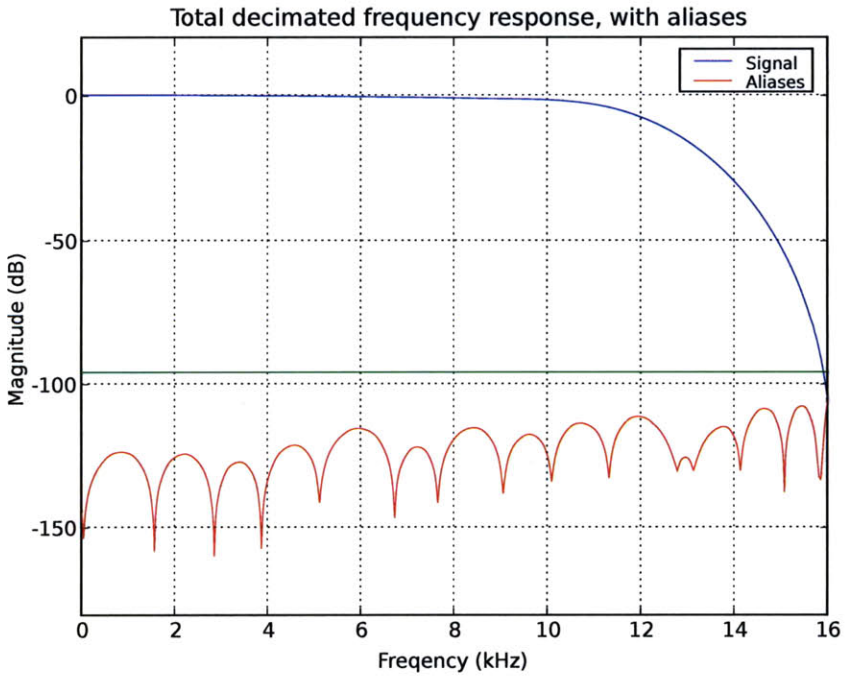


Figure 2-8: Aggregate post-decimation filtering.

transition at least every six bits. 8b/10b also defines framing ("comma") characters which simplify packet identification.

Chapter 3

Operation and interfacing

The acquisition board has four modes of operation, one normal multichannel mode, one mode for offset compensation, one mode for link testing with simulated output, and one mode for single-channel test.

Interfacing with the acquisition board is accomplished via a plastic optical fiber interface for enhanced electrical isolation even over long data transmission distances.

3.1 Modes

The acquisition board has four modes of operation, designed to set the internal state and prevent accidental configuration modification during operation.

Normal acquisition mode (Mode 0) Mode 0 is the normal acquisition mode; in this mode all 10 channels are sampled at the full normal sampling rate and the data is transmitted over the optical link using the standard encoding scheme. In this mode, gain and hardware filter settings can be changed, but nothing else.

Offset disable mode (Mode 1) Offset disable mode disables the internal offset compensation. The values transmitted are thus the actual measured ADC values. This is the only mode in which new offset values can be saved to the board's internal non-volatile memory (EEPROM).

Input disable mode (Mode 2) Input disable mode disables all reading from the ADCs; in this mode no change of input or analog settings has any effect on the board. While in this mode, the board will continuously transmit a test pattern stored in the on-board EEPROM.

In this mode, both the test pattern and the digital low-pass filter can be modified and written to. The sample pattern **is** filtered by the digital filter, and can be used as a mechanism to verify that the filter coefficients were properly written.

Raw mode (Mode 3) Raw mode simply outputs the raw, unfiltered, non-decimated data from a single selected channel. The 192 ksps data stream occupies multiple words in the transmitted data stream. This can be useful to characterize the analog properties of a given channel, and to debug signal integrity problems.

3.2 Fiber IO

The Acquisition Board's external interface is a bidirectional 8 MHz fiber-optic link over 1mm plastic optical fiber. Both the TX and RX streams are encoded using 8b/10b encoding.

The Acqboard transmits an 8b/10b-encoded frame of 24 bytes, preceded by the K28.5 comma character (figure 3-1).

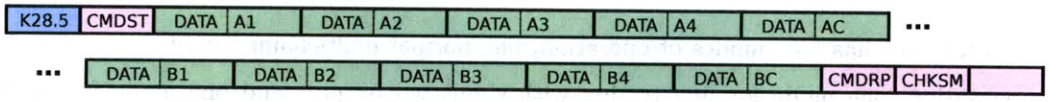


Figure 3-1: Format of 24-byte frame transmitted by the Acquisition Board.

The Command Status byte consists of three active bits. CMDST[1:0] are the mode numbers, indicating the current active mode. CMDST[0] is a "loading" bit, and is high **during transition into a new mode.** Mode switching is not instantaneous because the board needs to read values from EEPROM, a (comparatively) slow process.

Every command sent to the board contains a 4-bit Command ID (CMDID); this is a nonce which indicates command completion. The most recently-completed Command ID is transmitted with each full frame. When a command is **done executing** the output Command ID is changed to reflect this.

CMDRP is the command response field; CMDRP[4:1] are the bits of the most-recently executed CMDID; CMDRP[0] tells whether or not this command was successful.

The data fields are 1.15-bit twos-complement fixed point samples, that is they should be interpreted has having the decimal point after the first bit, with fifteen bits to the right of the point. They are transmitted MSB first.

Normally, the Acqboard receives a stream of valid 8b/10b encoded zeros; a new command is indicated by the presence of the comma character in the data stream followed by a packet (figure 3-2). A typical command packet is below, and consists of six bytes. The specific internals of the commands are explained in the following section.

3.3 Commands

The following commands are valid in any mode

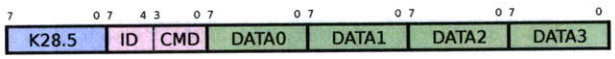


Figure 3-2: Format of six-byte command sent to the acquisition board.

3.3.1 Universal Commands

Switch Mode

Figure 3-3: Switch mode command.

Switch the current acqboard mode to **mode**. If changing to the RAW mode, the **chan** field is the 4-bit number of the raw channel to be transmitted. In all other modes, this field is ignored.

Note that some mode transitions can take up to 300 ms; during this time the transmitted packet's CMDST will reflect the new mode, but the **loading** bit will be high until the mode has been entered. Only once loading is completed will the CMDID be updated.

Set Gain

Figure 3-4: Set gain command.

Sets the gain of channel **chan** to one of the preset gain values **gain**. Valid in all modes.

Set Input

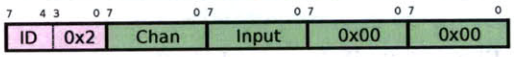


Figure 3-5: Set input command.

Select which of the four primary input channels will be used as input to the secondary input channel.

High Pass Filter Enable

Enable or disable the high pass filter on the indicated channel.

Figure 3-6: Enable HPF command.

3.3.2 Mode 1 Commands

Write offset

Figure 3-7: Write offset command.

This command writes the 16-bit twos-complement value in V as the digital offset for channel **chan** when the gain on that channel is set to **gain**. To measure the inherit DC offset (and thus compute the compensation value) you must be in offset-disable mode.

3.3.3 Mode 2 Commands

Write filter

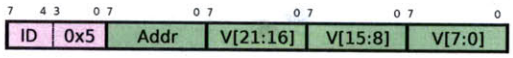


Figure 3-8: Write filter command.

This command writes the 22-bit twos-complement value in V as the addr-th coefficient for the low-pass filter.

Write Sample Buffer

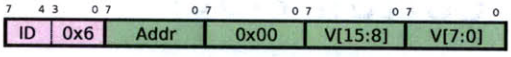


Figure 3-9: Write sample buffer command.

This command writes the 16-bit twos-complement value in V as the addr-th sample in the no-input sample buffer.

Chapter 4

Hardware IO

4.1 Front Panel

The front panel of the acquisiton module has the 20-pin input for all 8 differential channel pairs of amplifier input.

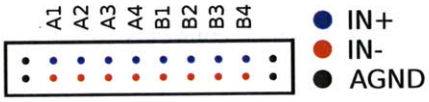


Figure 4-1: The front panel connector for the Soma Acquisition Module. AGND is connected to the amplifier analog ground.

The connector is a dual-row, twenty-pin 0.100-inch pitch IDC connector.

4.2 Back Panel

The back panel (figure 4-2) contains power, IO, and debugging information. There are four sections of interest.

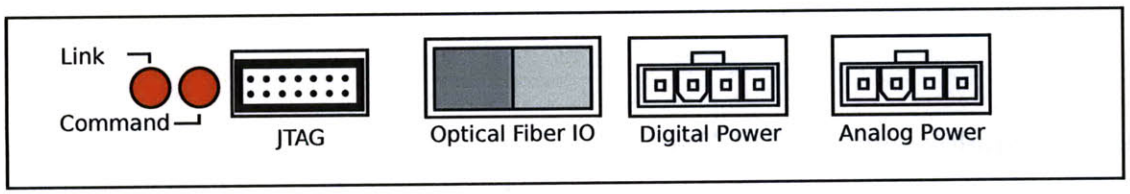


Figure 4-2: The back of the Soma Acquisition Module.

4.2.1 Status LEDs

There are two status LEDs on the back of the module:

- **Link** : indicates the link with the Soma backplane (over the optical fiber) is functioning properly.
- **Command**: Flashes briefly every time the Soma Backplane sends a command to the acqboard.

4.2.2 JTAG port

The JTAG port is the standard 14-pin 2mm-pitch JTAG connector for Xilinx FPGAs, allowing both programming of the on-board flash and debugging. This mates with any of the Xilinx programming cables, such as the Xilinx Parallel Cable IV [16].

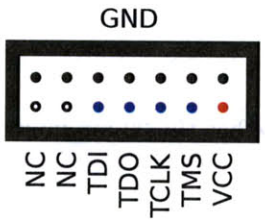


Figure 4-3: The JTAG port, which conforms to the standard Xilinx pinout.

4.2.3 Optical Fiber IO

The optical fiber interface takes two 1-mm 650nm wavelength plastic optical fibers. The receiver and transmitter colorings match up with the associated ends of the plastic optical fiber, eliminating polarity mistakes.

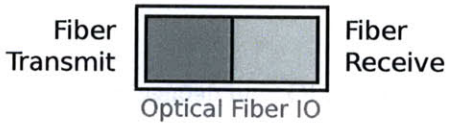


Figure 4-4: The optical fiber interface.

4.2.4 Analog and Digital Power

Powering analog and mixed signal data acquisition devices is always a challenge, as the exact nature of the power distribution scheme can substantially impact analog performance. The power connectors mate with a Molex 39-01-4041 four-pin connector (and associated female pins 44476-3112).

The Acquisition module completely isolates its internal analog and digital power supplies for maximum signal integrity. The digital power supply requires 5 volts DC. Analog requires a very clean bipolar +/- 5V DC.

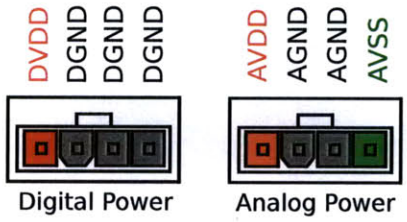


Figure 4-5: The analog and digital power ports. DVDD=+5V, AVDD=+5V, AVSS=-5V.

Chapter 5

Performance

Measuring analog performance of programmable-gain amplification with selectable filtering results in a wide range of configurations to test.

5.1 THD + N

Total harmonic distortion plus noise (THD+N) measures the ratio of a fundamental signal to the power in all other harmonics and noise over a targeted bandwidth [9] . We measure THD+N by using test signals at multiple frequencies. We follow the IEEE standard for digitizing waveform recorder [1] to fit the sine wave.

Figure 5-1 shows THD+N across frequencies, with more negative values reflecting a lower (better) THD+N. Each measurement was run ten times, with the range indicated by a partially-transparent envelope. In general, this range is very small, except at two points where the wave-finding algorithm failed to converge.

The THD+N is reduced for low frequencies when the high pass filter is on, which is not surprising – the HPF attenuates the input carrier, raising the effective noise floor. At higher gains the THD+N is worse, as expected – higher gains necessitate a lower input voltage to reach full-scale. With consistent input noise (see next section), the effective THD+N decreases.

5.2 RMS Voltage Noise

By shorting the inputs to ground we measure the RMS noise referred-to-input (RTI). In all cases the RMS noise is less than one microvolt (figure 5-2), and varies only slightly as a function of gain, indicating that the bulk of noise contribution is from the input stage of the amplifier.

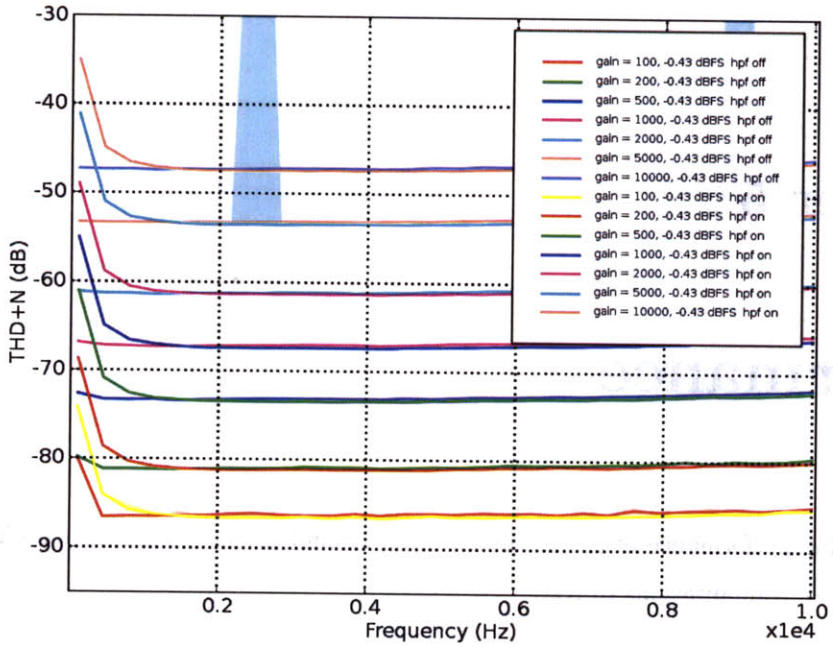


Figure 5-1: Total Harmonic distortion + noise measured across frequencies, gains, and high-pass filter settings at -0.43 dBFS. Blue shaded regions exist where the sine-fitting algorithm failed to converge on a datapoint due to numerical stability problems.

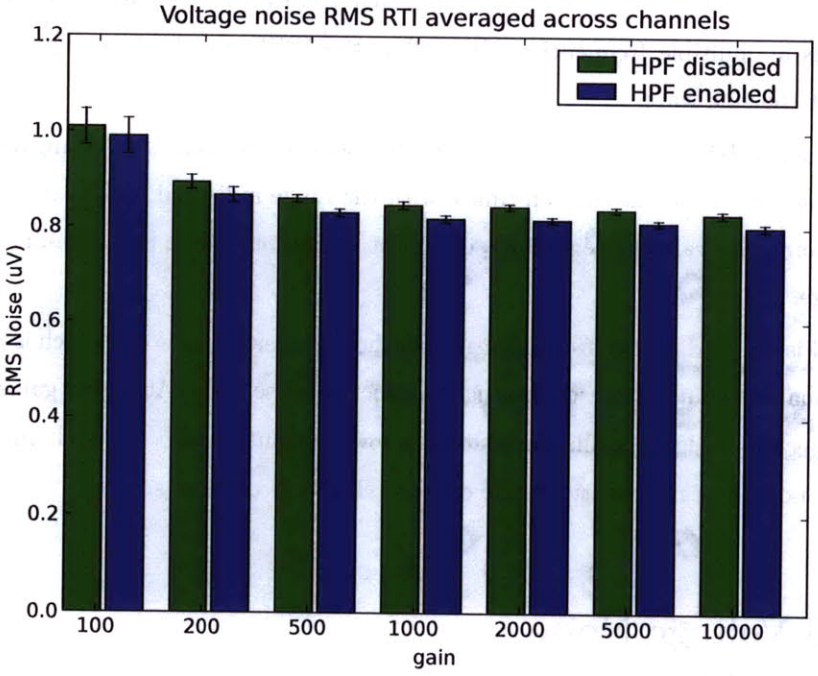


Figure 5-2: Voltage noise RMS, averaged across channels, for each gain and high-pass filter setting.

5.3 Noise Spectra

The noise spectra are relatively flat across our 10kHz bandwidth (figure 5-3), and are unsurprisingly attenuated at low frequencies when the high-pass filter is enabled.

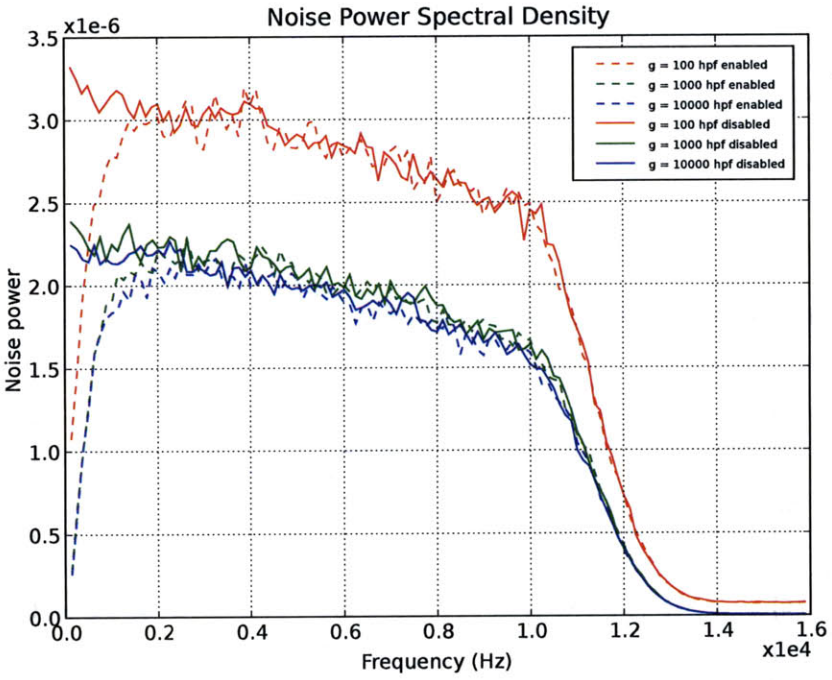


Figure 5-3: Power spectral density of noise measurements.

5.4 CMRR

Our common-mode rejection is above 75 dB across our bandwidth of interest, and 95 dB at 60 Hz.

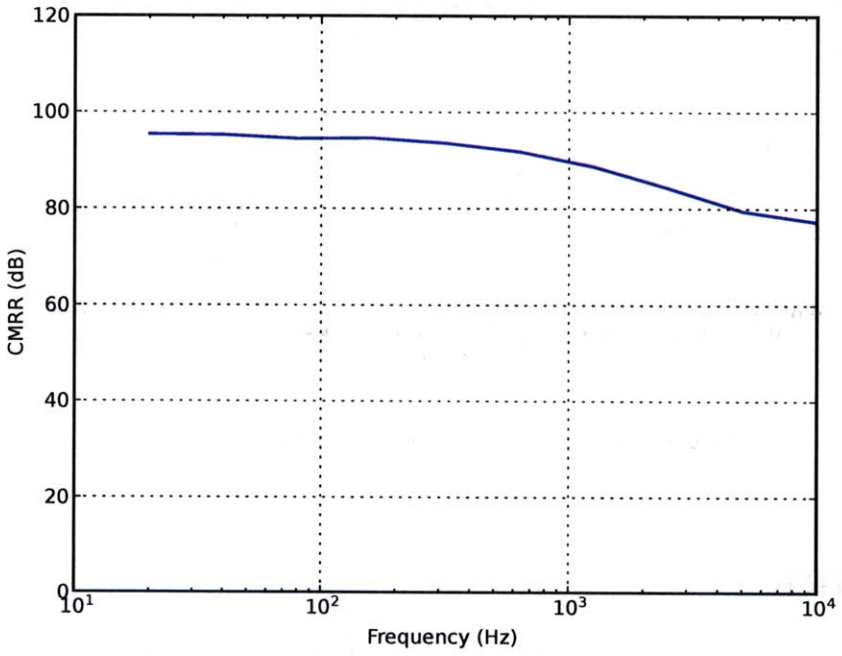


Figure 5-4: Common-mode rejection across frequency.

Chapter 6

Digital Design of FPGA

The Xilinx Spartan-3 is used for acquisition control, digital filtering, and data encoding and transmission. The modular firmware architecture (figure 6-1) implements this functionality in VHDL.

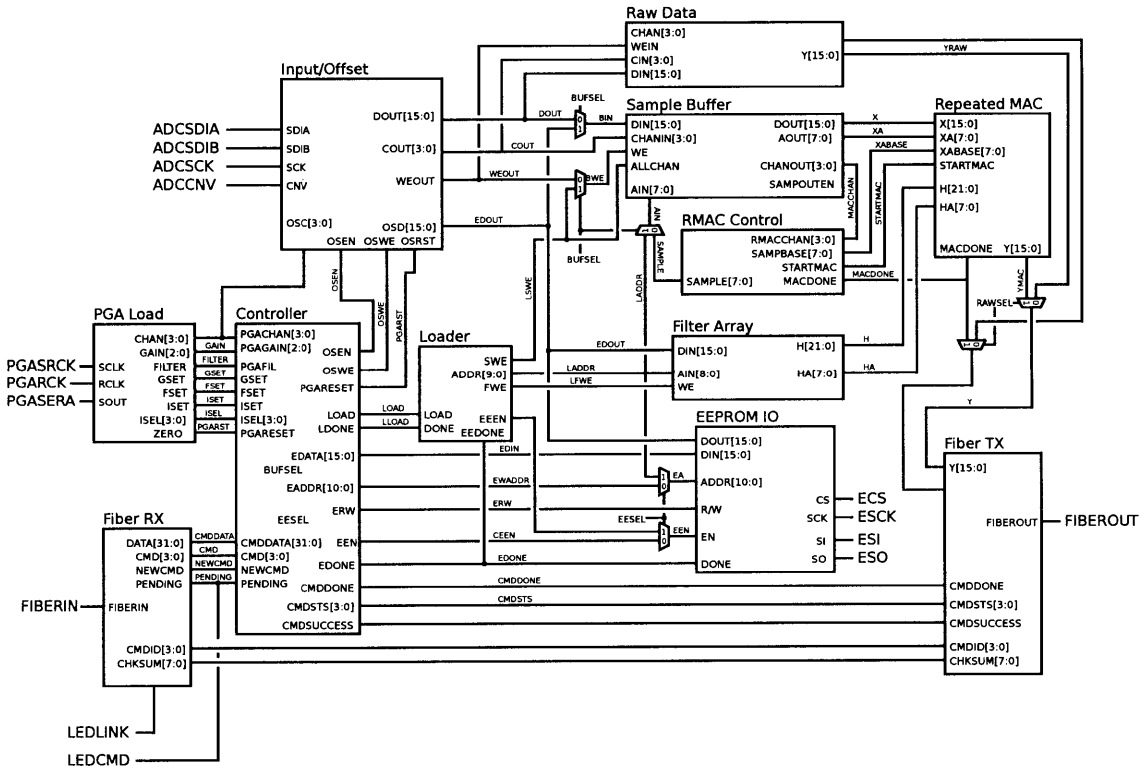


Figure 6-1: Overall architecture of the FPGA firmware for signal processing and amplifier control.

6.1 Clocks

The FPGA is clocked at 72 MHz via a DCM-doubled 36-MHz input clock signal. A series of centralized synchronized clock-enables coordinates events across the entire FPGA.

Clock name	Ticks	Frequency	Use
INSAMPLE	375	192.0 kHz	Input sample clock enable – sets the input sampling rate
OUTSAMPLE	2250	32.0 kHz	Output sample clock enable – controls the output sample rate.
OUTBYTE	90	800.0 kHz	Output byte clock enable, enables each symbol (encoded byte) on the output fiber interface.
CLK8	9	8.0 MHz	Fiber output bit clock.
SPICLK	180	400.0 kHz	SPI clock for interfacing with EEPROM.

6.2 Input

The FPGA input module controls ADC sampling, bit acquisition, offset compensation, and the eventual write-out of the sample bits.

ADC interface The ten ACDs are configured in two serial chains of five ADCs each, corresponding to input channel sets A and B, and giving rise to **SDIA** and **SDIB** (figure 6-2). The ADC FSM controls the sampling sequence (figure 6-3); CONCNT the delay between the assertion of **CNV** and the bit read-out; **BITCNT** sends the sample clock. To compesate for the ADC readout delay and the propagation delay across the galvanic isolators, we delay the **LSCK** via a shift-register into **BITEN**.We go out of our way to make sure we keep the digital signals quiet during the ADC's conversion period.

Offset arithmatic The 16-bit unipolar ACD samples are converted to bipolar samples and then added to the per-channel offset values. The resulting **SUM** is checked for overflow and then written to.

Output writing For each **INSAMPLE** assertion we cycle through all channels and then write the resulting offset-adjusted values to the downstream modules.

6.3 Sample Buffer

The sample buffer stores 256 16-bit samples for each of the 10 channels (figure 6-4). The dual-port Spartan-3 BlockRam allows for an independent interface to simultaneously read out the samples. The assertion of **ALLCHAN** writes all channels. **CHAN[3:2]** selects which internal block is used; **CHAN[1:0]** selects which range in the block is written to.

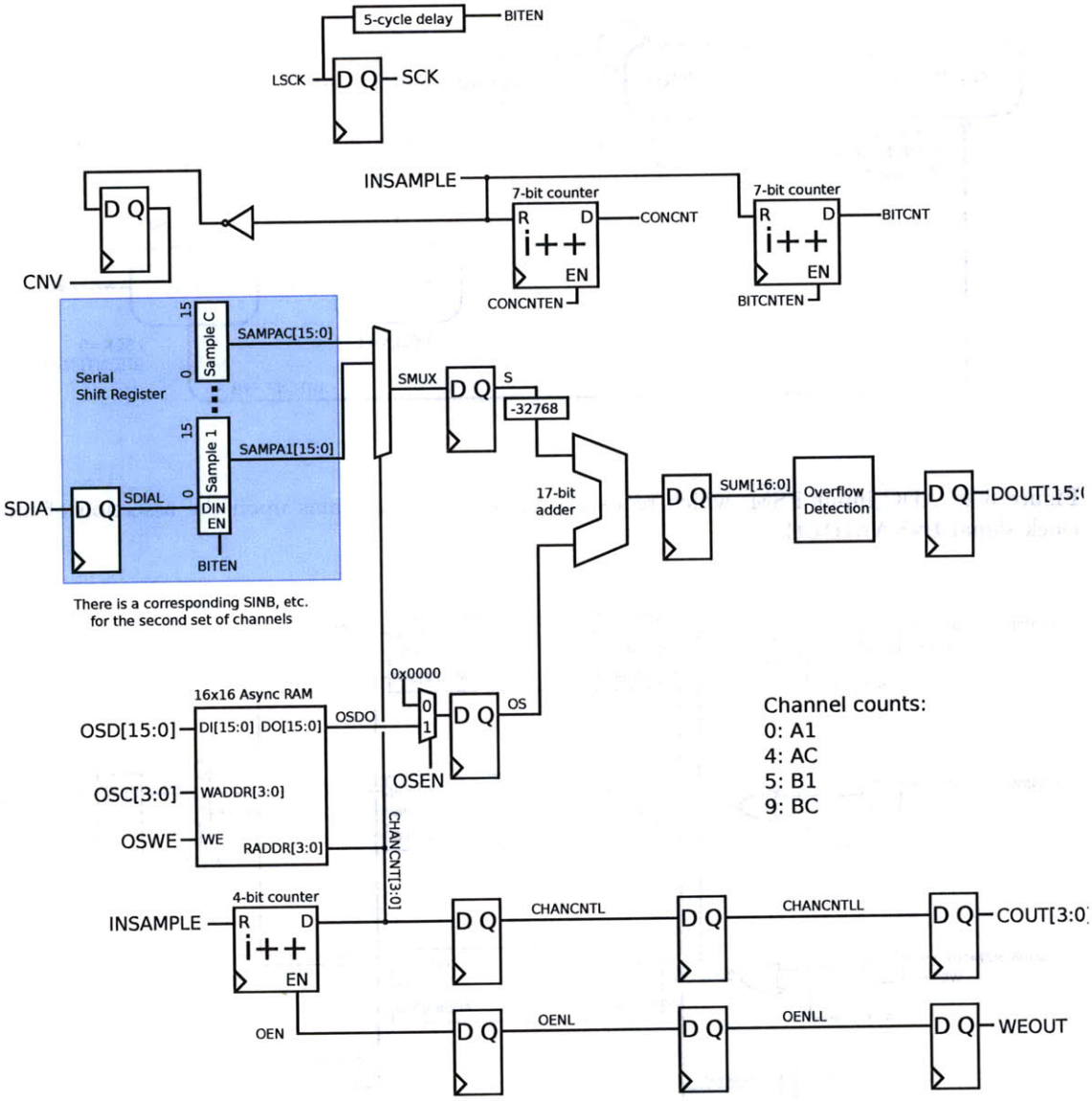


Figure 6-2: Input control which deserializes ADC samples and performs offset compensation.

6.4 Filter Array

The filter array (figure 6-5) uses BlockRAM to store the 22-bit fixed-point filter coefficients. The double-buffering allows for independent read-write ports to let the Control and EEPROM write the coefficients on mode-switch. Coefficients are written 16-bits at a time via **DIN[15:0]** and read out via **H[21:0]**.

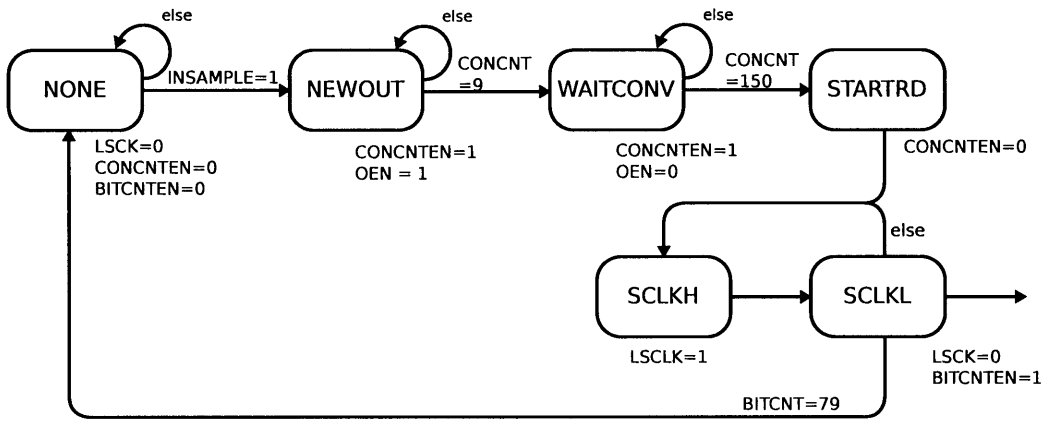


Figure 6-3: ADC input FSM, which reads all ADC serial bitstreams upon the assertion of input clock signal **INSAMPLE**.

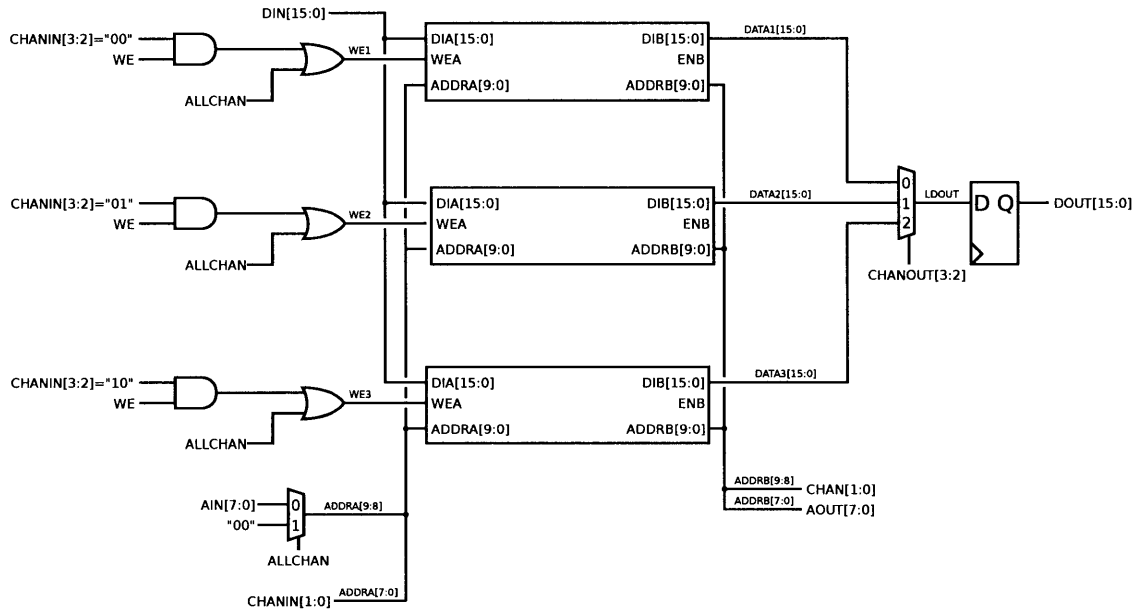


Figure 6-4: Sample buffers for 10 channels of input data.

6.5 Repeated Multiply / Accumulate

FIR filtering is performed by the repeated multiply-accumulate module; the filter used is that described earlier.

6.5.1 RMAC

The repeated multiply-accumulate unit is composed (figure 6-6) of the following subcomponents:

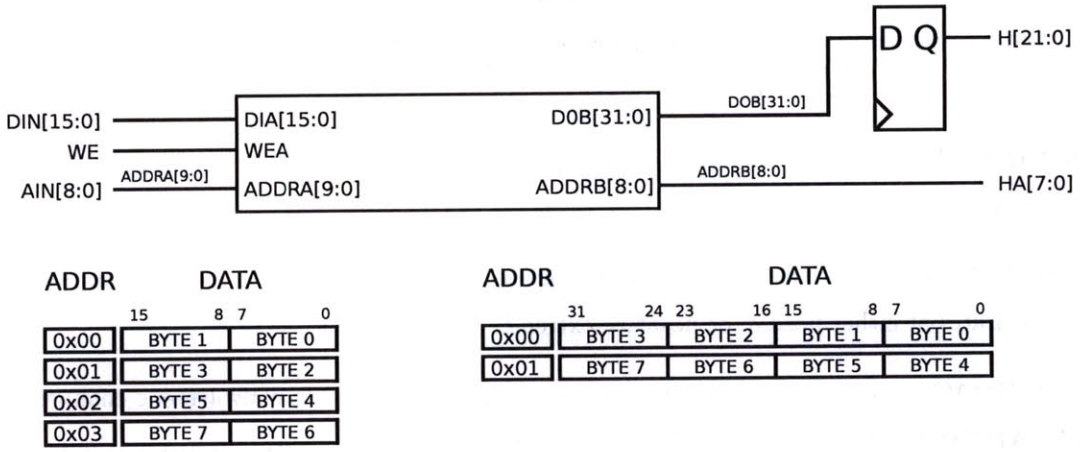


Figure 6-5: Filter coefficient buffer and write pattern.

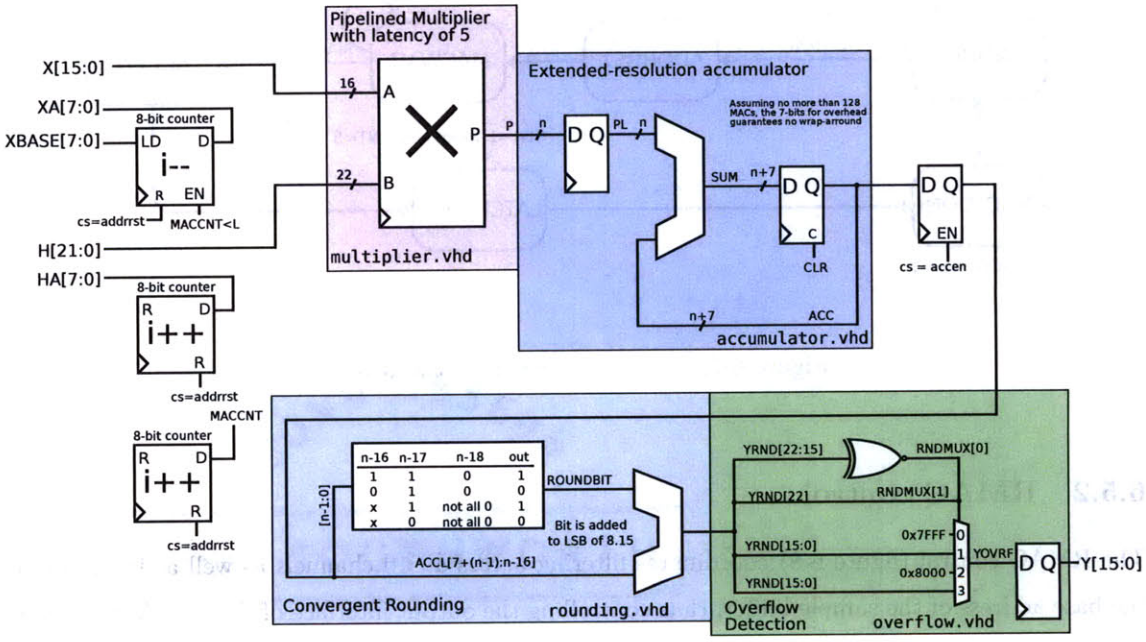


Figure 6-6: Repeated Multiply-Accumulate (RMAC) module for fixed-point convolution.

Sample Counters Under control of the RMAC FSM, the RMAC drives the sample buffer address pointer **XA[7:0]** and the filter coefficient buffer address pointer **HA[7:0]**. The sample buffer address pointer begins at location **XBASE[7:0]** and counts backwards through the buffer.

Multiplier The pipelined multiplier performs fixed-point multiplication of the input, truncating the output at 1.23 bits of data.

Extended-Resolution Accumulator For each iteration through the sample buffer, the accumu-

lator sums the resulting sample/coefficient products. The arithmetic is done with 7 extra bits of precision on the left side of the decimal, allowing for extended range and to prevent saturation mid-convolution.

Convergent Rounding Convergent rounding of the input is performed, resulting in the output being in 8.15 format.

Overflow Detection If the output is too large to be expressed in 1.15 format than the value saturates at either positve or negative extreme.

The RMAC is controlled by a FSM (figure 6-7) that is designed to convolve one channel's data per **STARTMAC**. When **STARTMAC** is asserted, the system convolves up to a maximum length L=143, and then asserts **MACDONE**.

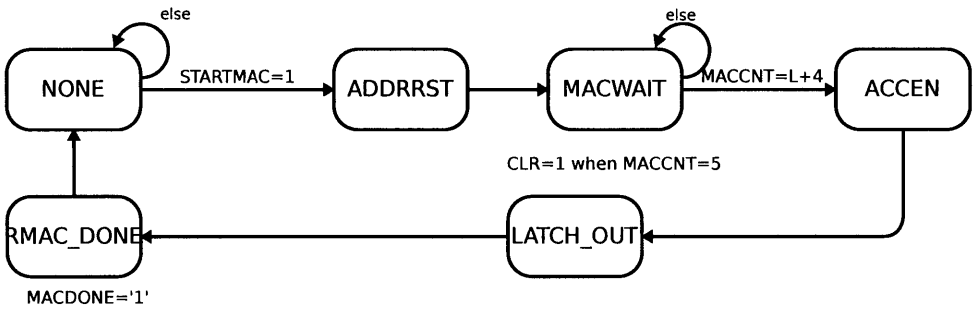


Figure 6-7: Controlling FSM for the RMAC.

6.5.2 RMAC control

The RMAC control (figure 6-8) coordinates filtering across all 10 channels as well as incrementing the base address of the sample buffer, thus controlling the output interface of the sample ring buffer. The associated FSM (figure 6-9) is equally simple, asserting **STARTMAC** to the RMAC engine and waiting for completion.

6.6 Fiber IO

The fiber IO controls the optical transmitter and receiver.

6.6.1 The Fiber TX module

The Fiber TX module (figure 6-10) formats data for transmission according to the Soma FiberIO Protocol. All inputs are latched on the **OUTSAMPLE** signal to prevent word-skew.

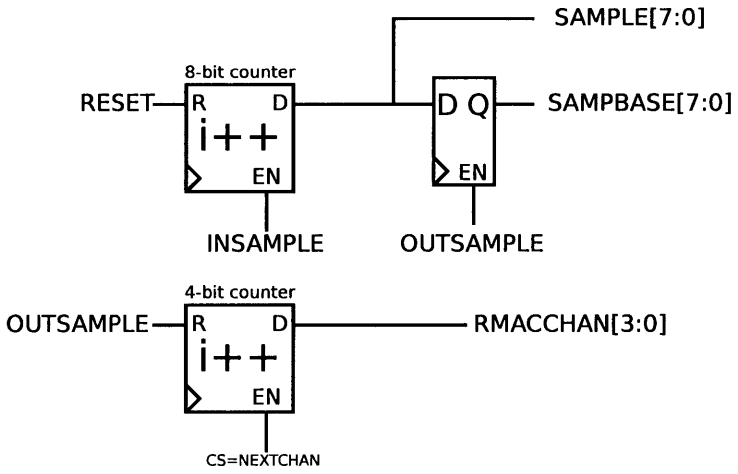


Figure 6-8: The RMAC pointer controller.

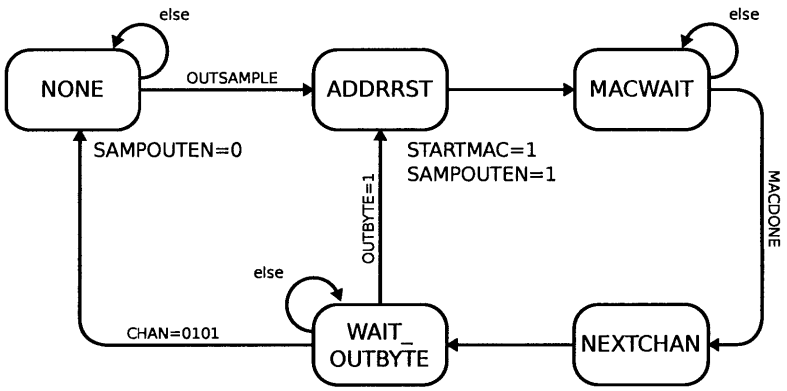


Figure 6-9: The RMAC controller FSM.

The counter **INCNT** counts the assertion of the input **YEN** to write samples from the output of the RMAC. These are stored in an appropriate array of registers **YL[n]**.

A giant mux controlled by an **OUTBYTE**-enabled counter multiplex the relevant words into the 8b/10b encoder.

A simple parallel-load LSB-out shift register takes the 10-bit encoded data **DOUT** and serializes it to the eventual output **FIBEROUT**.

6.6.2 Fiber RX

The fiber receive interface (figure 6-11) is in some ways simpler than the transmit interface. The interface's state machine waits until we receive a new packet with no errors and the appropriate K-character, and then sets about latching the relevant input words.

Any error in 8b/10b decoding or spurious (out-of-sequence) comma character causes a transition

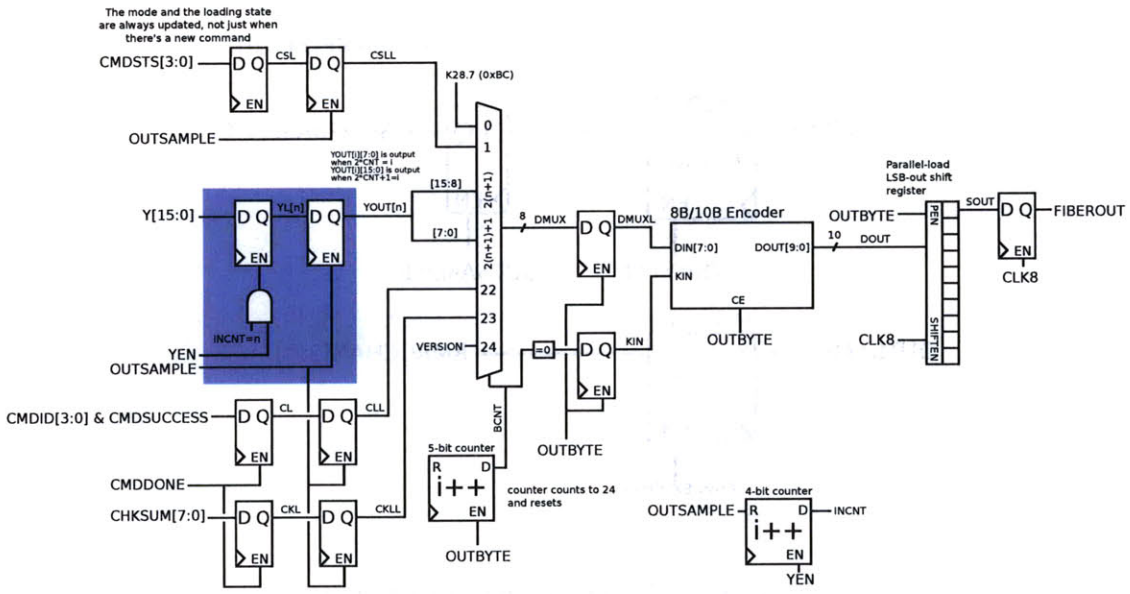


Figure 6-10: The Fiber Transmission interface

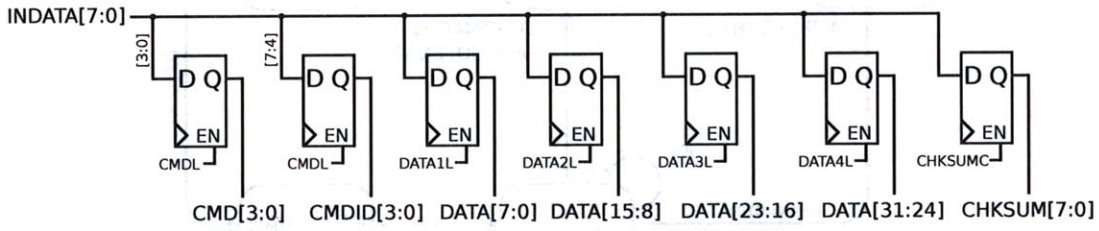


Figure 6-11: The Fiber Reception interface.

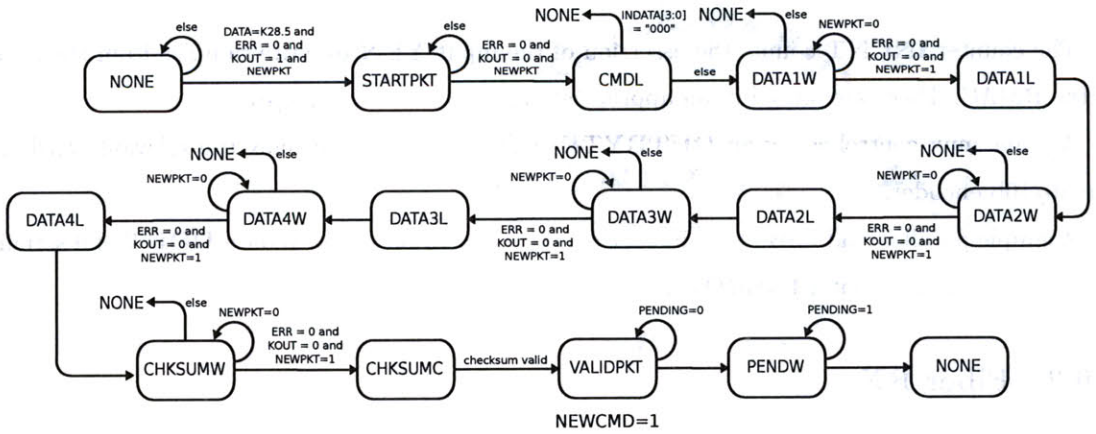


Figure 6-12: The Fiber Reception finite state machine.

back to state NONE, preventing the reception of an invalid data frame.

Decoder

The deserialization step is somewhat more difficult; as the core is running at 72 MHz, we can oversample the input bitstream by a factor of 9. The 8b/10b encoding guarantees a maximum run of five, so we simply need to maintain a lock for at most five input-bit-cycles.

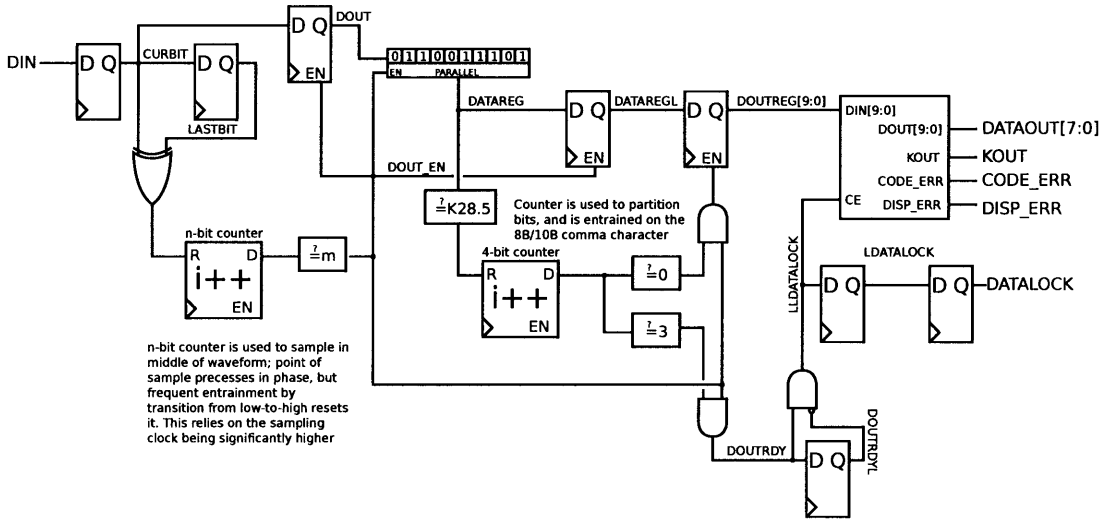


Figure 6-13: The oversampling fiber decoder

The decoder used here (figure 6-13) is generalized to work for different oversampling rates, as it was not known in the early stage of development what the final oversampling rate would be. We use a counter which is reset on each bit transition, and shift in the relevant bits; in the absence of transitions the counter loops and appropriately samples.

The detection of the unique K28.5 comma character is used to partition the bits into words via the serial-to-paralllel shift register **DATAREG**. From that point on we simply count in multiples of 10 bits in gating the output into the 8b/10b decoder.

6.7 EEPROM I/O

The EEPROM is a SPI-serial component which can store up to 32 kB of ram (figure 6-14). We store 16-bit big-endian words as in the table below.

Word Address	Data
0-511	Filter (256 2-word samples)
512 - 757	sample buffer initial values (256 words)
1024 - 1535	offset values for each gain (512 words)

On each operation we execute the EEPROM's write-enable (**WREN**) instruction, and then a full two bytes. Since we have 12 bits of address, we place the 11 input bits on the line and always

have the LSB be zero.

We use the two-byte read and two-byte write sequence capability of the eeprom for both reads and writes. We never cross page boundary since we always start with LSB = 0.

To interface to the SPI EEPROM we use a single output mux driven by **CNT**.

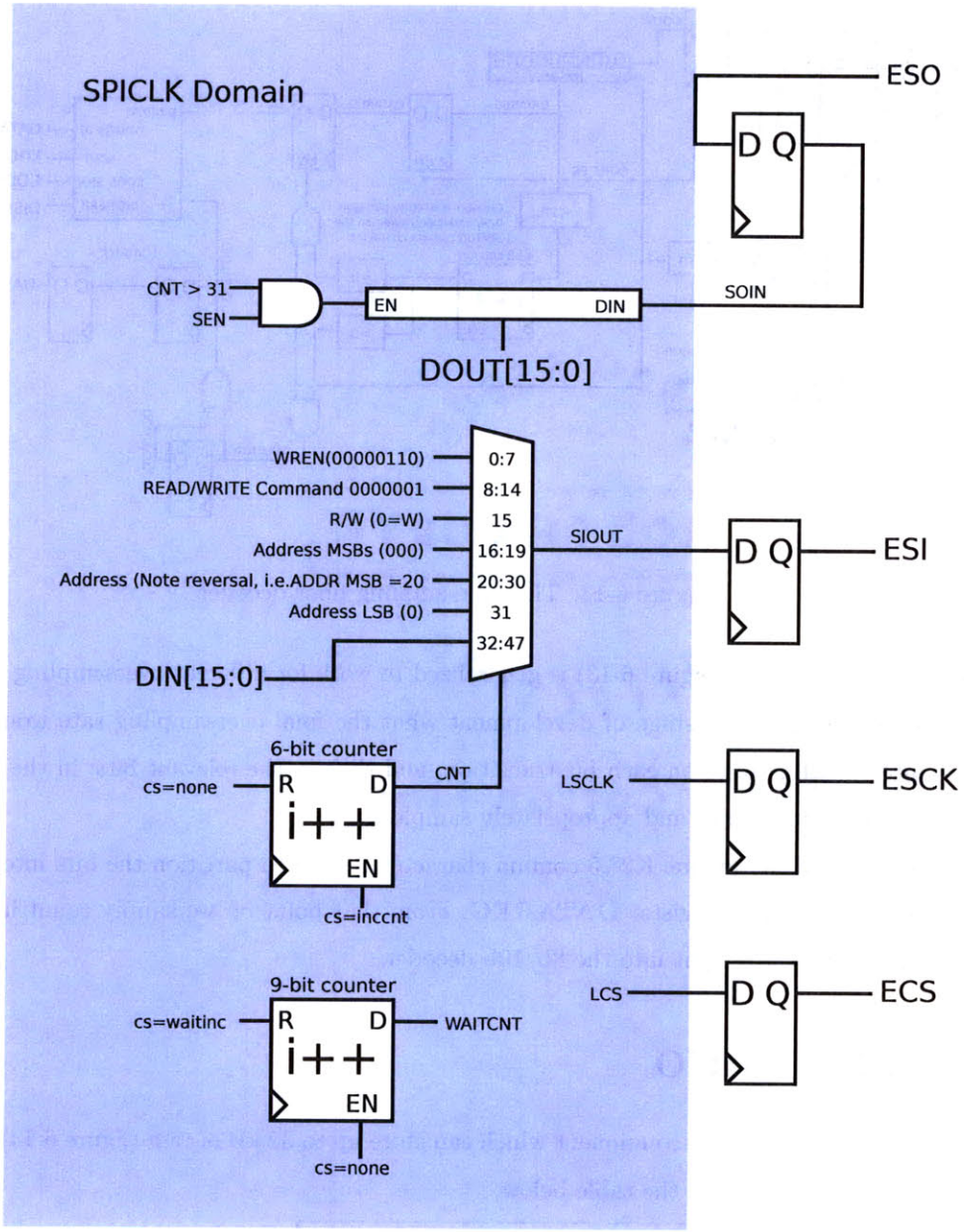


Figure 6-14: SPI interface control to the EEPROM.

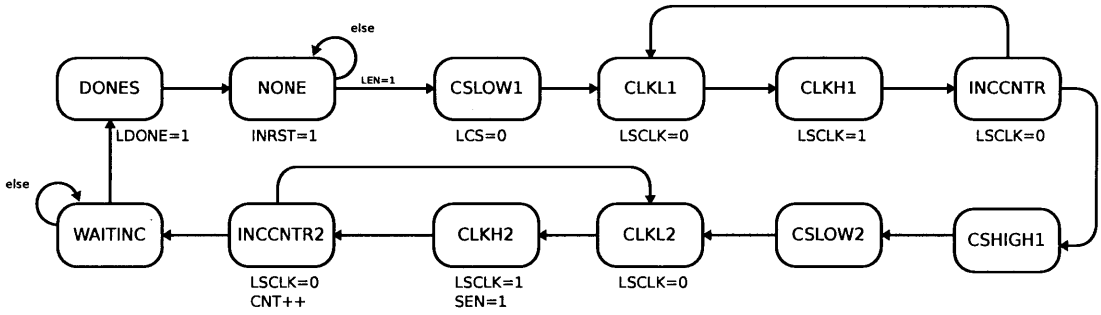


Figure 6-15: FSM for controlling the EEPROM SPI interface.

6.8 Loader

The loader (figure 6-16)simply handles the bulk transfer of data from the EEPROMIO into the filter array and the sample buffer on mode transition. The addresses of the EEPROM are decoded into the filter write-enable (**FWE**) and sample buffer write-enable (**SWE**) signals.

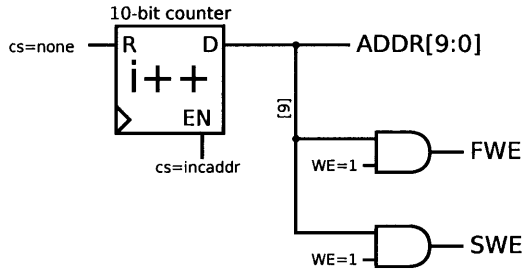


Figure 6-16: EEPROM setting loader counter and output enable.

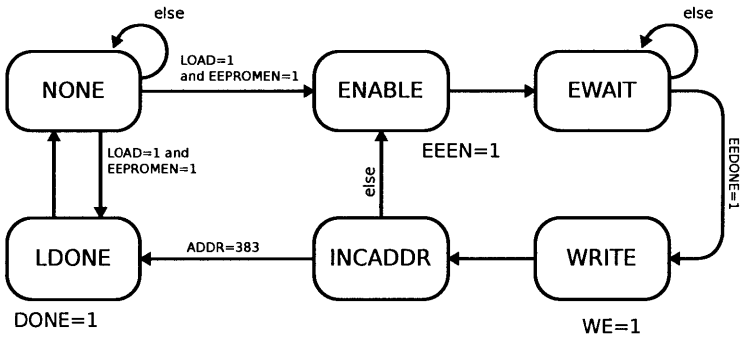


Figure 6-17: EEPROM setting loader FSM.

6.9 Control

The control module (figures 6-18 and 6-19) handles mode changes, gain and filter setting changes, and the storage and retrieval of settings and filter coefficients from the EEPROM.

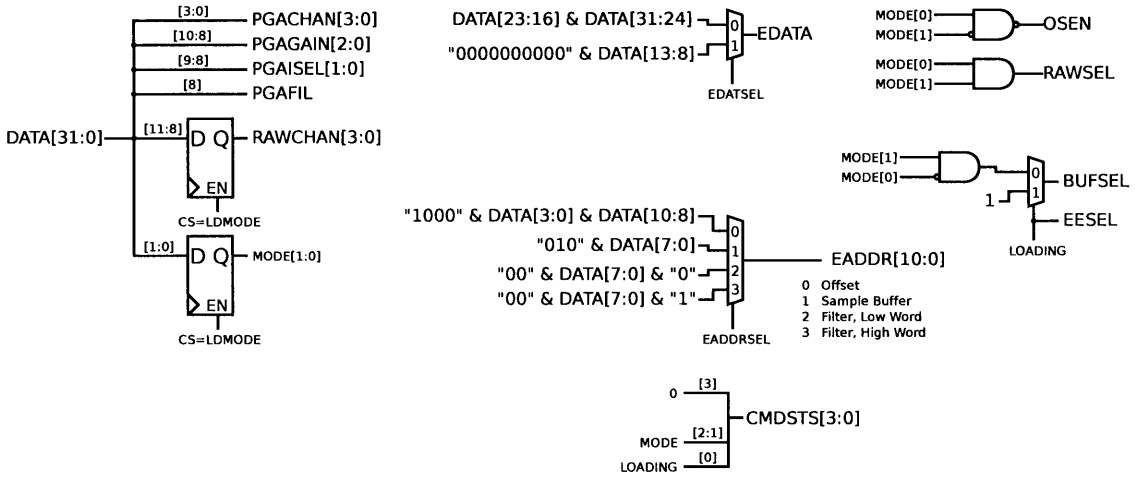


Figure 6-18: State control and decoding.

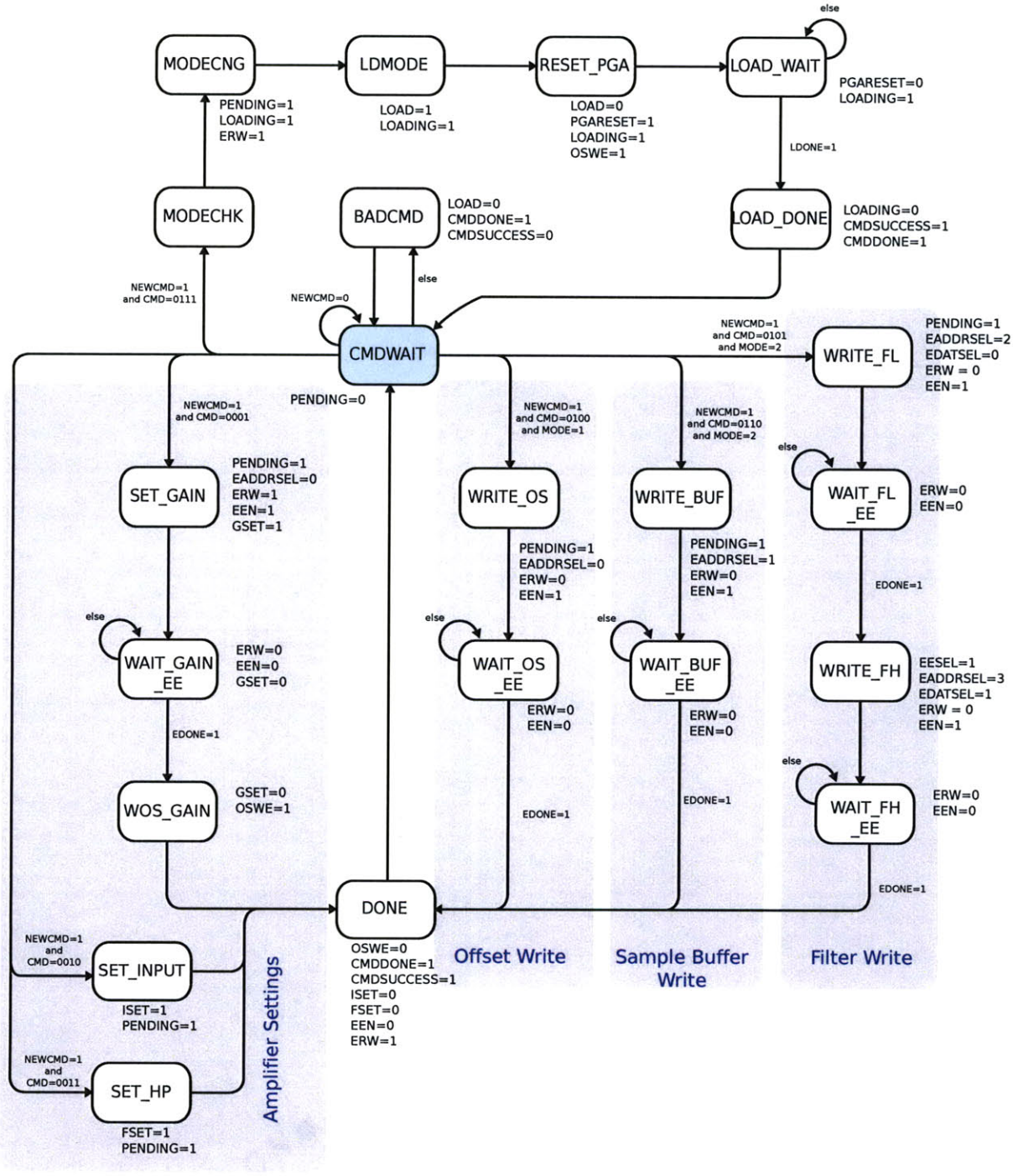


Figure 6-19: State control finite state machine.

Chapter 7

Components and Circuit Design

The design of the Soma Acquisition hardware matches the signal chain closely, but for the purpose of this discussion we will divide it into the analog and digital subsections (figure 8-1) . The analog subsection runs off bipolar 5V rails, and the digital side is powered by an independent 5V digital supply.

7.1 Analog

7.1.1 Input front-end

The AD8221AR (**U12**) (figure 8-2) was chosen as the input instrumentation amplifier due to its excellent linearity and high common-mode rejection [5]. We use a fixed gain of 100 set by **R26** – programmable gain at this stage would necessitate the introduction of an analog mux, which would unacceptably degrade performance.

The input stage is AC-coupled to deal with the issues mentioned in *Signal Chain*. We use a simple single pole RC filter with a 0.1 Hz cutoff at the input. There are other methods of AC-coupling the input of a three-op-amp instrumentation amp ([13]), but these AC couple after the input has gone through at least one stage of internal amplification. The very high DC component in our common mode voltages would overwhelm this stage.

7.1.2 Input high-pass filter and Programmable gain

To optionally high-pass filter the input, a single-pole RC filter (figure 8-3) is combined with the JFET-input **AD8510** ([7], **U7**) and an **ADG619** SPDT analog mux ([6]). The high input impedance of the AD8510 results in minimum impact to the overall signal chain.

The bipolar programmable-gain **LTC6910-1** ([14]) **U8** provides gains of 0, 1, 2, 5, 10, 20, 50, and 100, allowing us to maximize the input dynamic range of the ADC.

7.1.3 Programmable Gain Shift Register Network

For each channel we have four bits of state: the three for PGA state and one for HPF state. We use a cascaded array of shift registers (figure 8-6) to propagate these settings from the FPGA to the actual analog components.

7.1.4 Input Anti-Aliasing Filter

To achieve filtering we use an eight-pole Bessel filter in a multiple feedback configuration (figure 8-4) , implemented via low-noise JFET quad op-amp AD8513AR [8].

The last stage is biased with V_{OS} to create a single-sided signal for the unipolar ADC.

7.1.5 ADC

The differential input, single-supply ADCs **AD7685 U2** ([4]) are driven at 192 ksps from a common conversion signal (figure 8-7) . Each ADC's voltage reference input (V_{REF}) is individually buffered to limit the voltage drop on the reference with each ADC cycle.

7.1.6 Voltage Refernece

LM4140CCM-4.1 U28 is used as the voltage reference, providing V_{REF} at 4.096V with a 0.1% initial accuracy and excellent 3 ppm / C stability [12]. The output of the reference is low-pass filtered before being distributed to the ADCs, which are individually-buffered. The voltage reference is voltage-divided via precision resistors to provide the V_{OS} offset.

7.2 Digital

7.2.1 Galvanic Isolation

To isolate ground current flow, we use the **IL715-3 (U14)** and **IL716-3** high-speed galvanic isolation ICs [11] to bridge the analog-digital domain (figure 8-8).

7.2.2 FPGA

The Xilinx Spartan-3 VQ100 **XC3s200-4Q100 U4** ([17]) performs all the control, signal processing, and communication tasks on the Acquisition Board (figure 8-10) . The FPGA is driven by a single 36 MHz digital oscillator.

The primary bitstream is contained within a **XCFS01** Platform Flash EEPROM. Both the Spartan-3 and the Platform Flash EEPROM are connected to the primary JTAG chain (figure 8-

11). To power the FPGA we take the input 5V and convert it to the 3.3 V for IO, the 2.5V aux level, and the 1.2 V core.

7.2.3 Optical Interface

The 8MHz serial link is carried at 650 nm via 1 mm plastic optical fiber. We use the Avago **HFBR-1528** transmitter [2] and **HFBR-2528** receiver [3], which can transmit up to 10 MBd over 50 m of the inexpensive plastic fiber.

7.3 Mechanics, PCB, Enclosure

The resulting Acquisition Board is a four-layer FR-4 PCB measuring 7 inches by 5.5 inches. The majority of signal routing takes place on the top layer (figure 9-1) with dedicated split power and ground planes (figures 9-2 and 9-3).

Chapter 8

Schematics

The following are the schematic used in the design of the Acquisition Board, generated via Altium Designer.

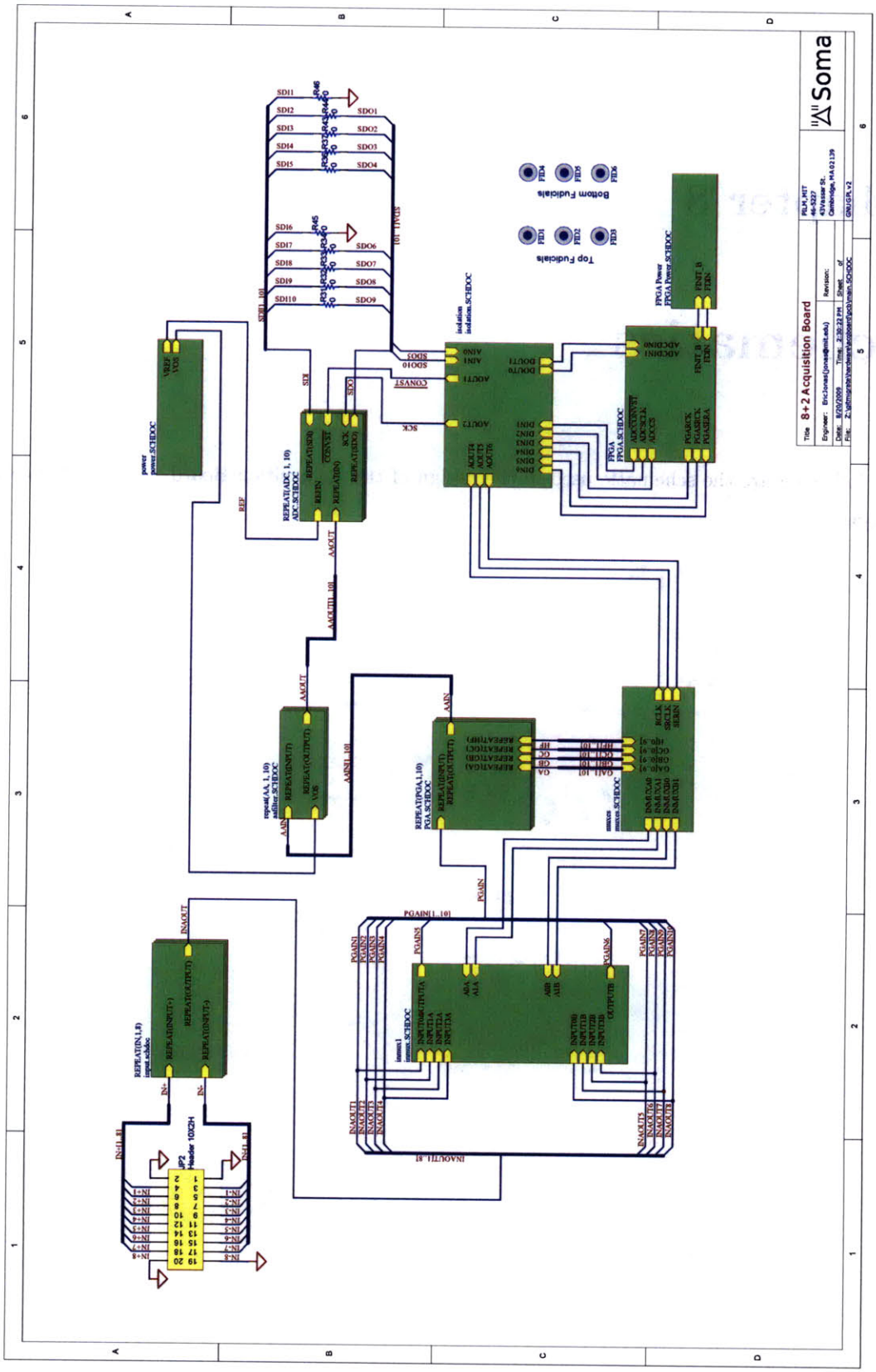


Figure 8-1: Integrated master schematic of all subsheets.

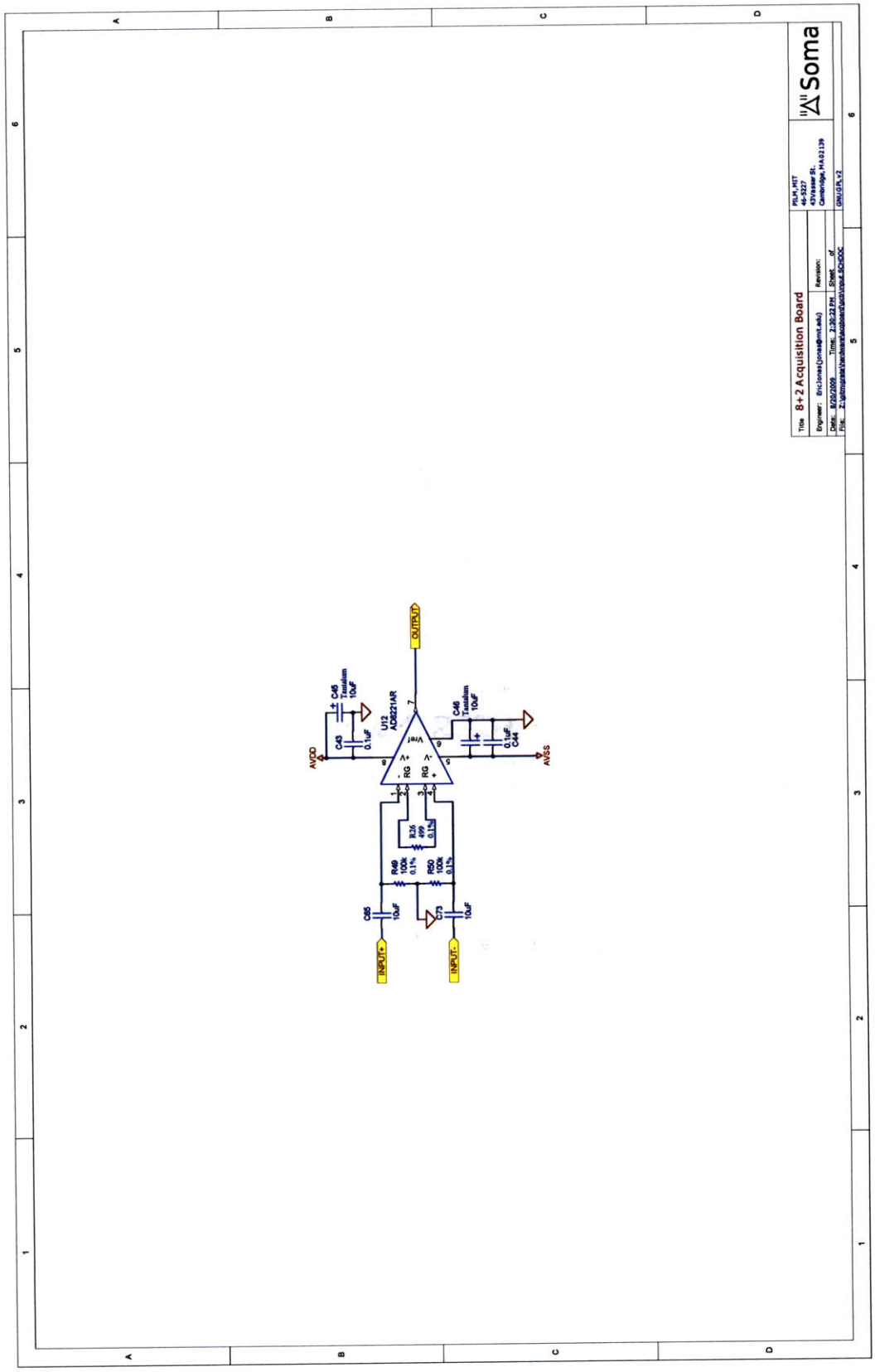


Figure 8-2: Input stage schematic.

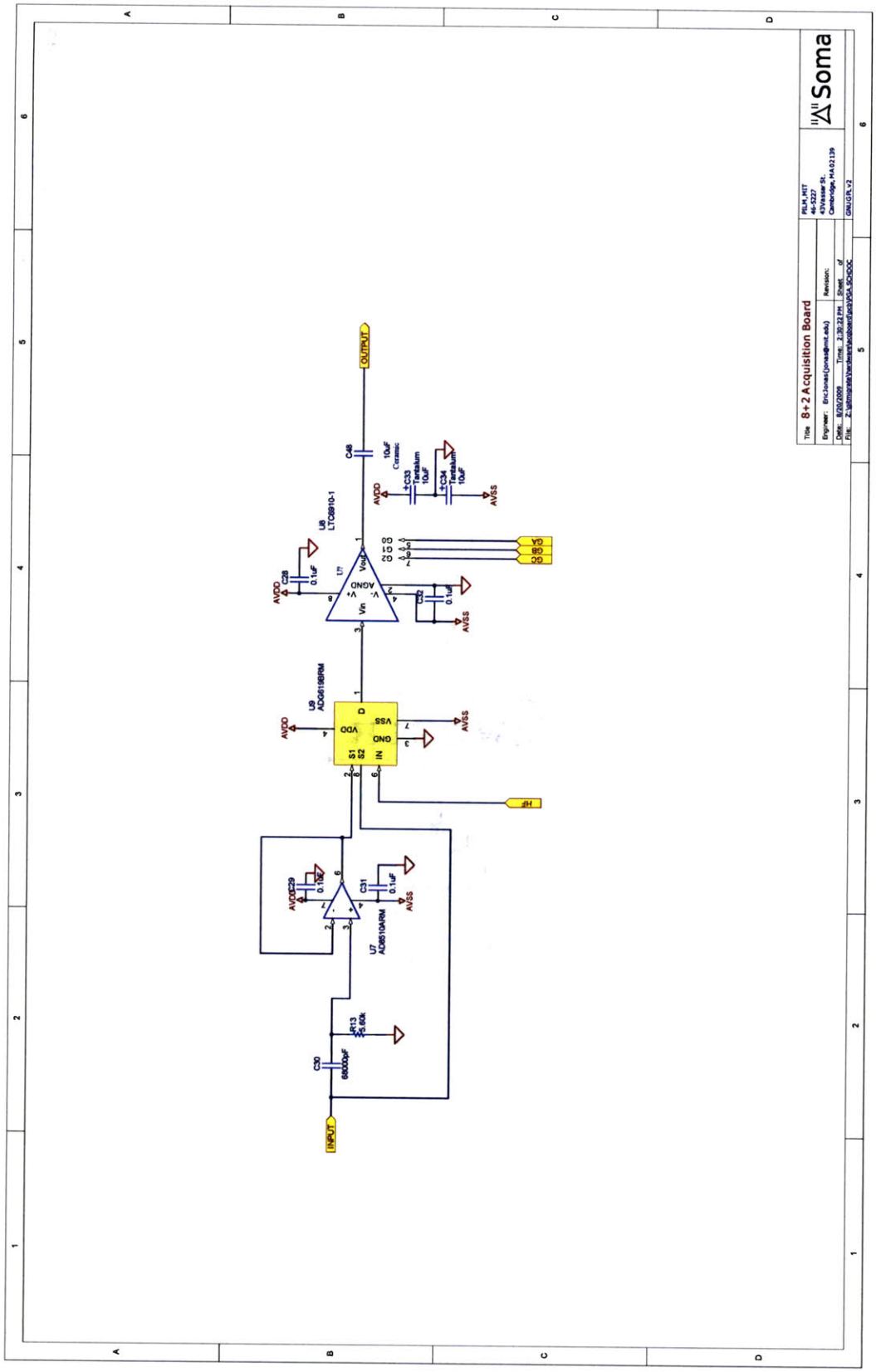


Figure 8-3: High-pass filter and programmable gain amplifier.

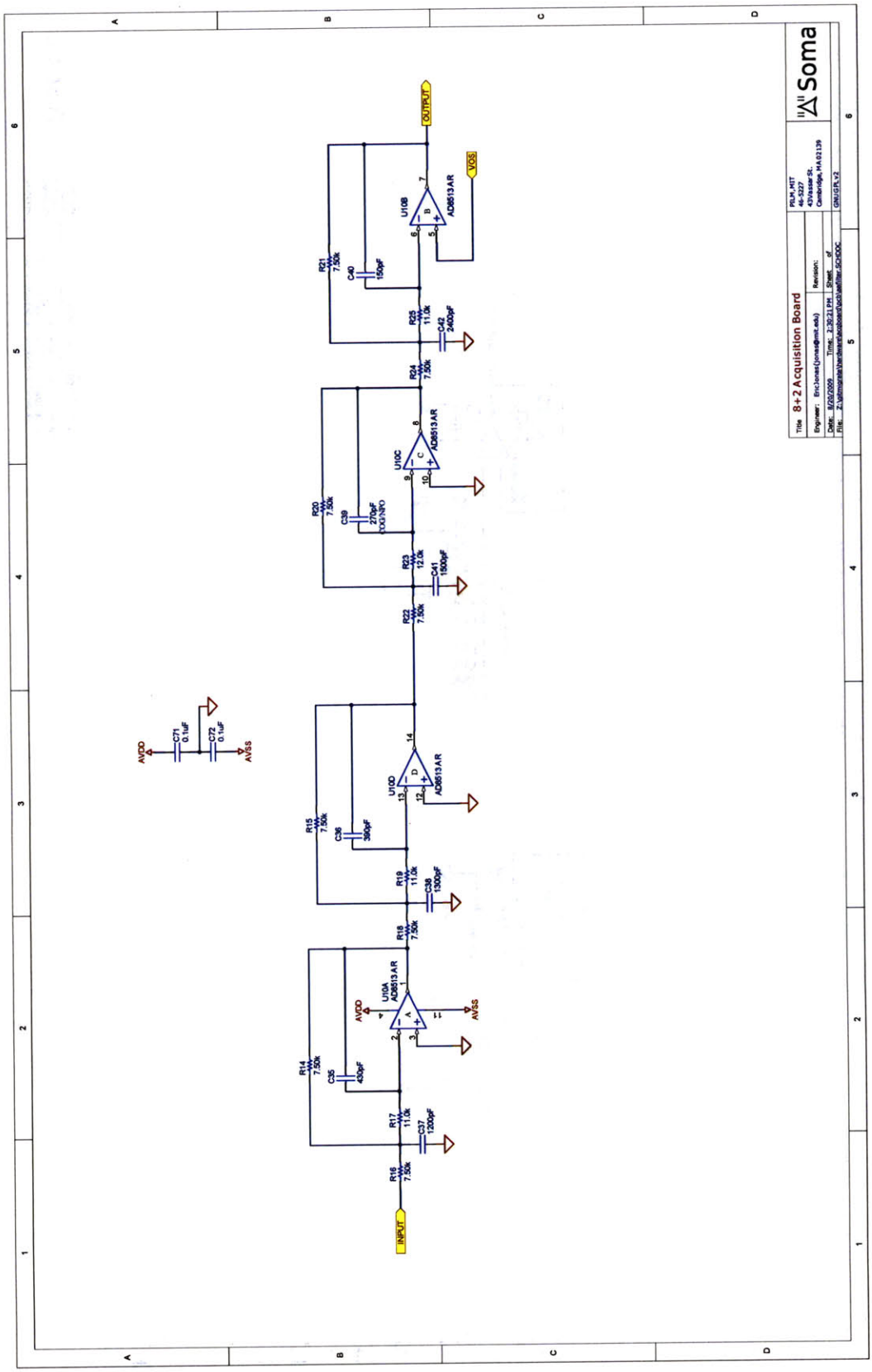


Figure 8-4: Anti-aliasing filter.

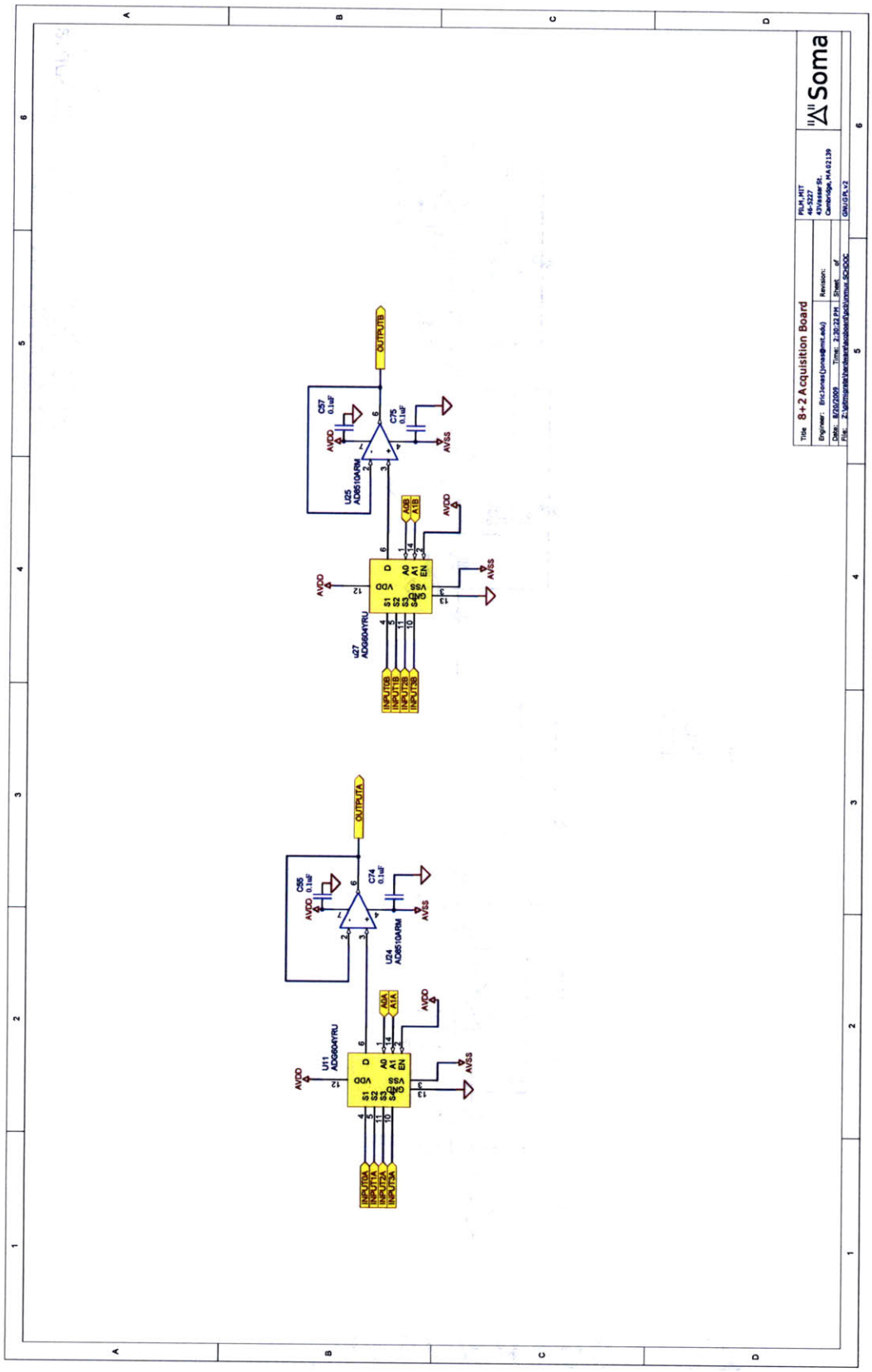


Figure 8-5: Input channel selection multiplexer.

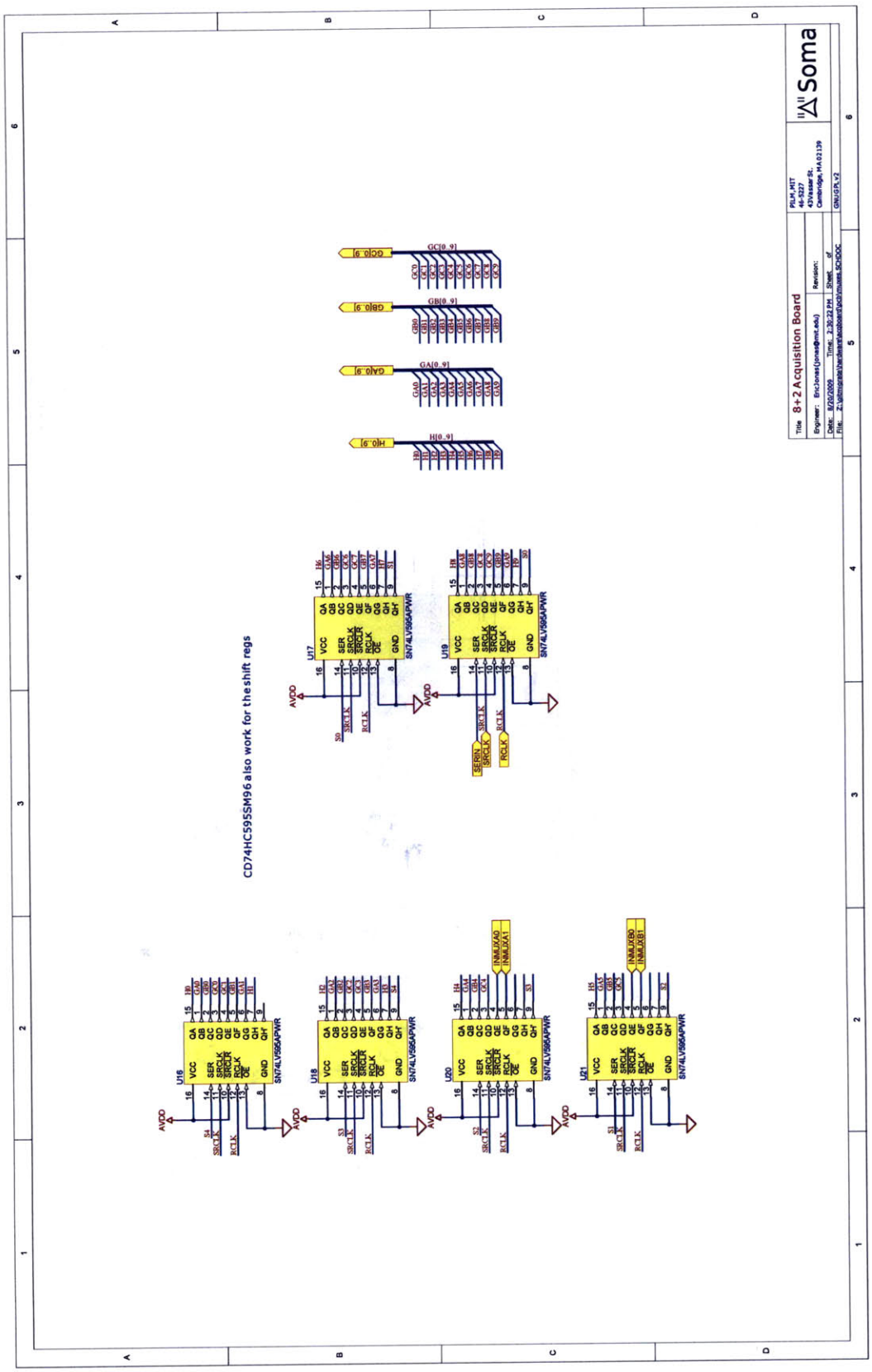


Figure 8-6: Shift register for amplifier state control.

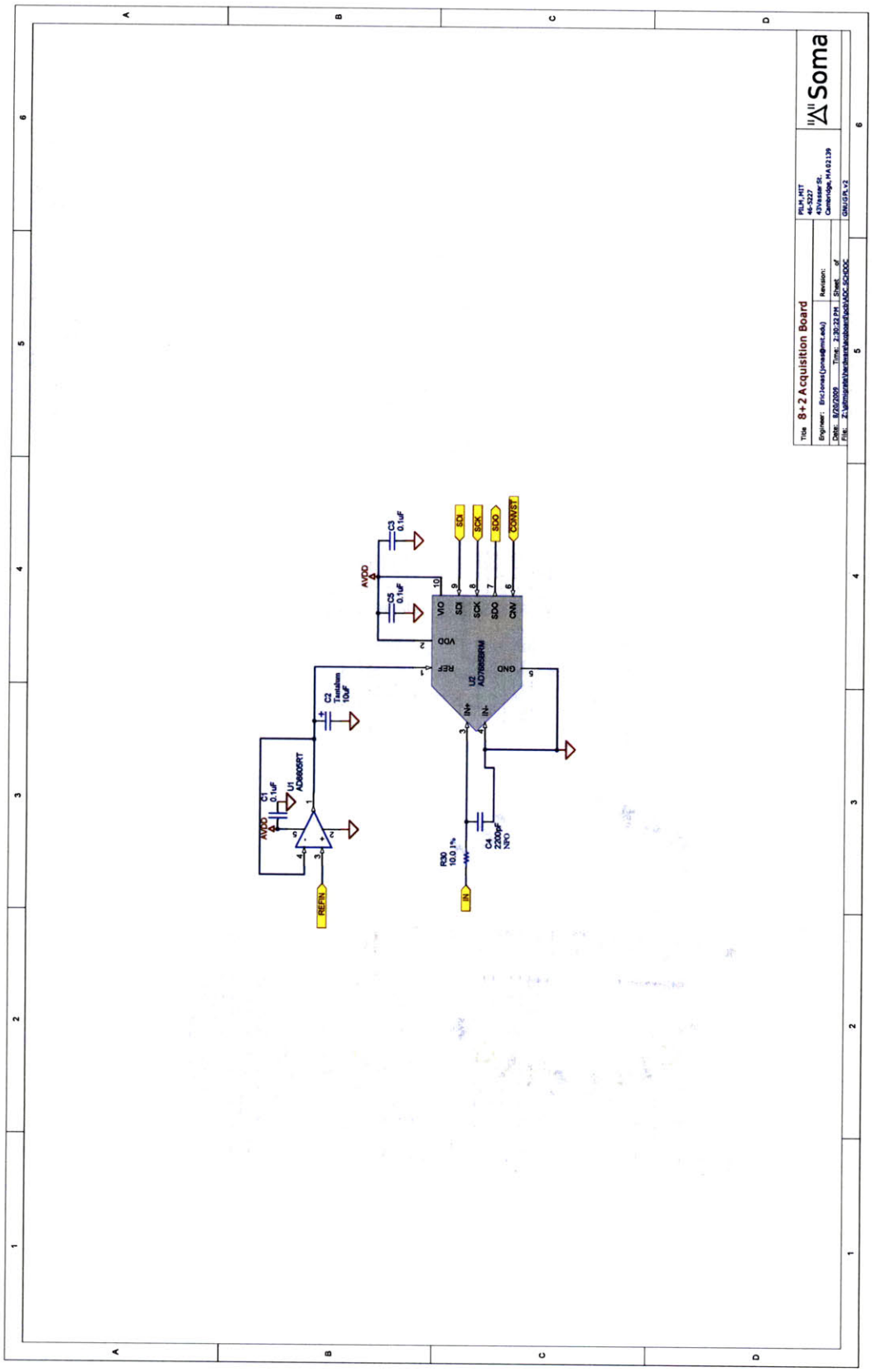


Figure 8-7: Analog-to-Digital Converter.

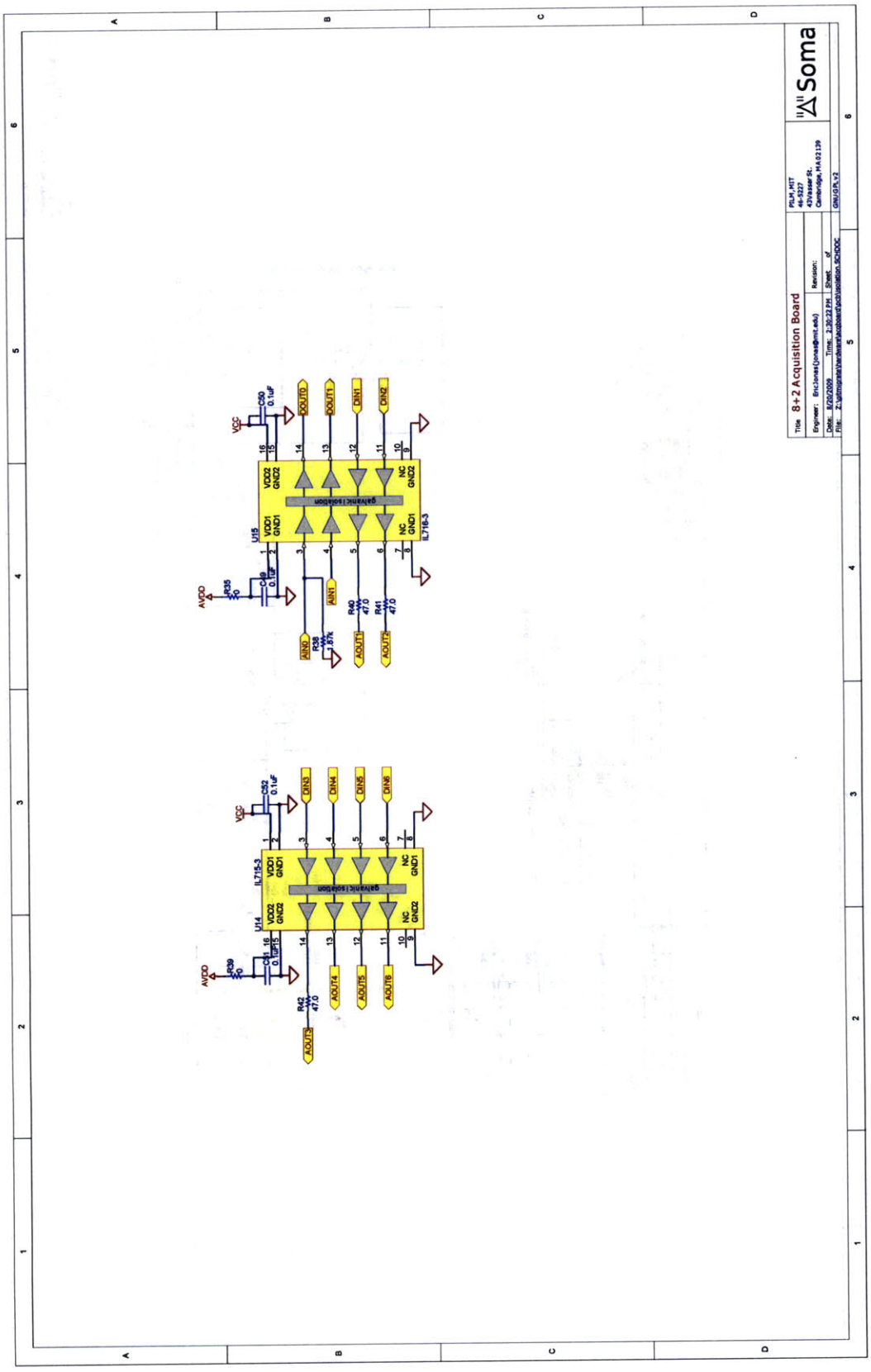


Figure 8-8: Galvanic isolation separating analog and digital subsystems.

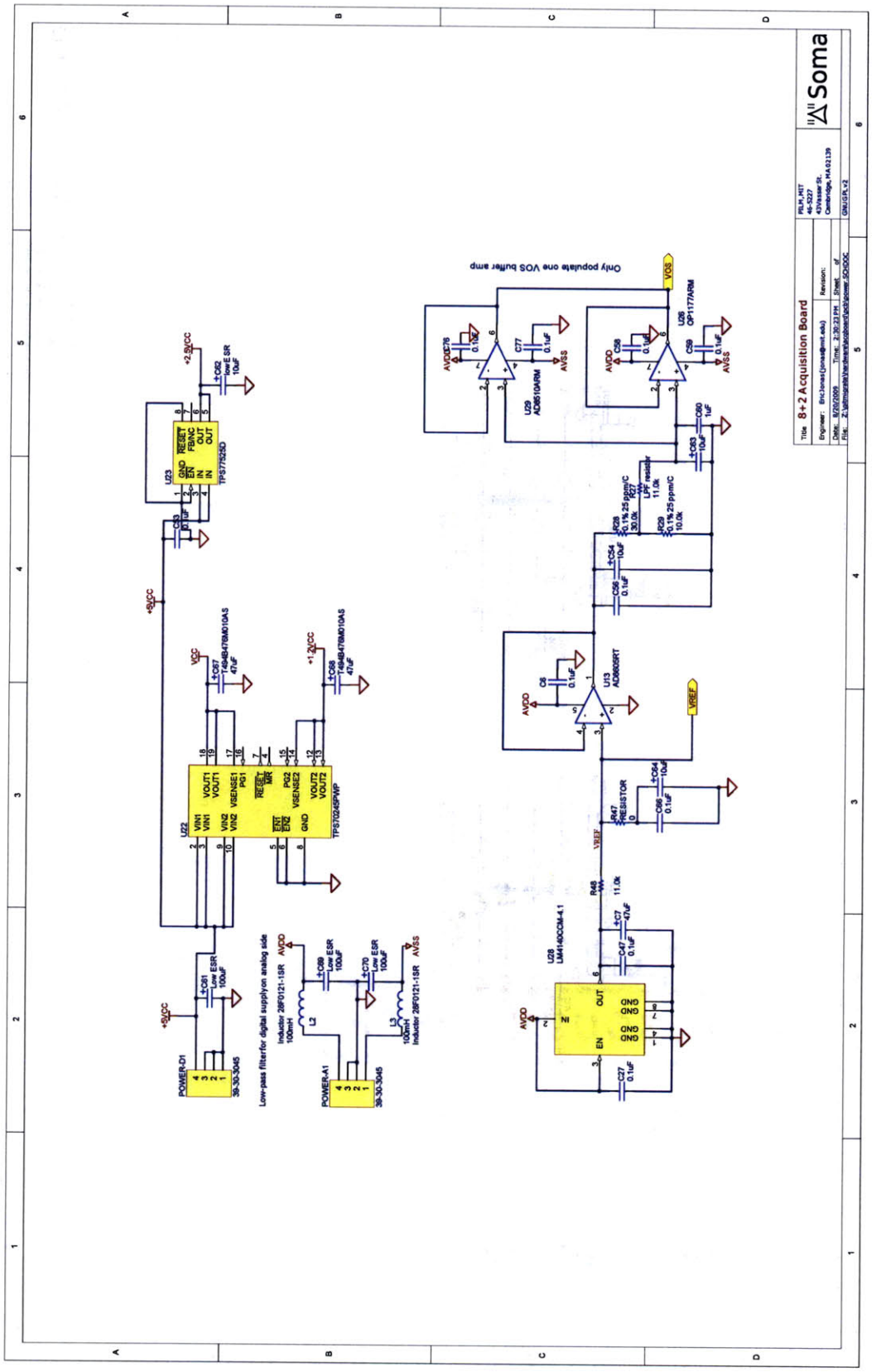


Figure 8-9: Analog power, digital power, and reference voltage generation.

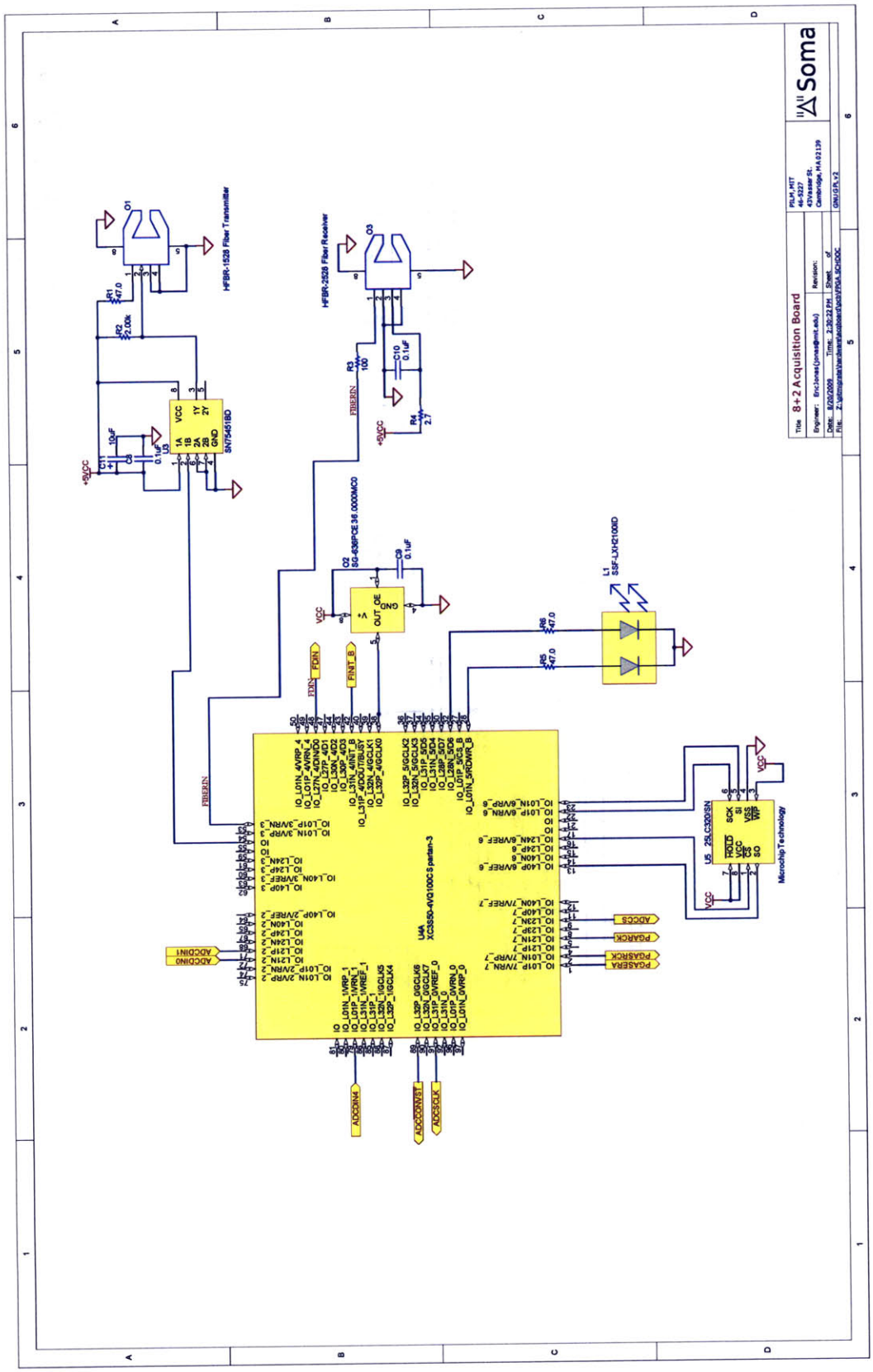


Figure 8-10: FPGA IO.

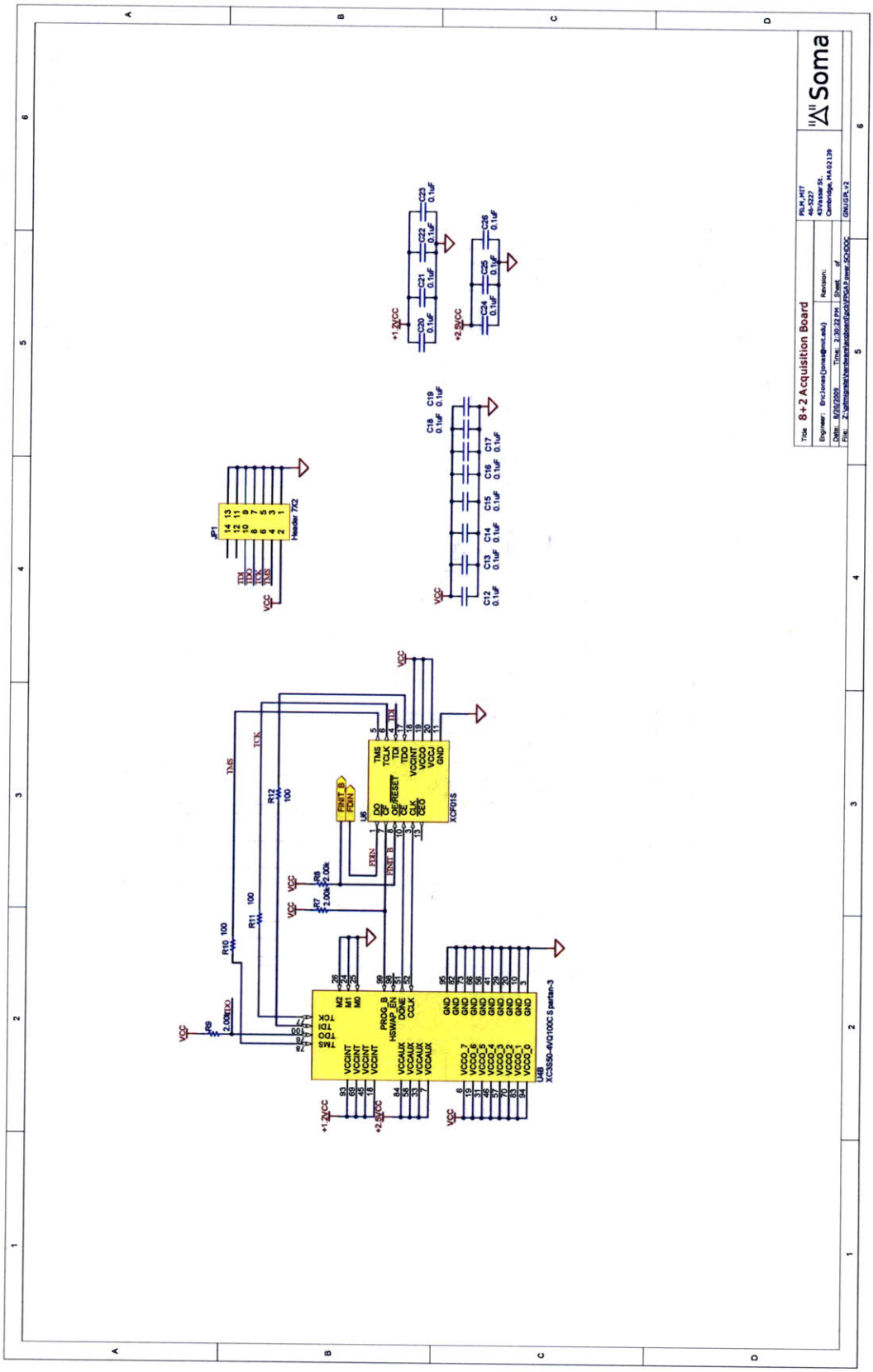


Figure 8-11: FPGA booting, JTAG.

Chapter 9

PCB Gerbers

The individual PCB mask files ("gerbers") of the Acquisition Board, generated via Altium Designer.

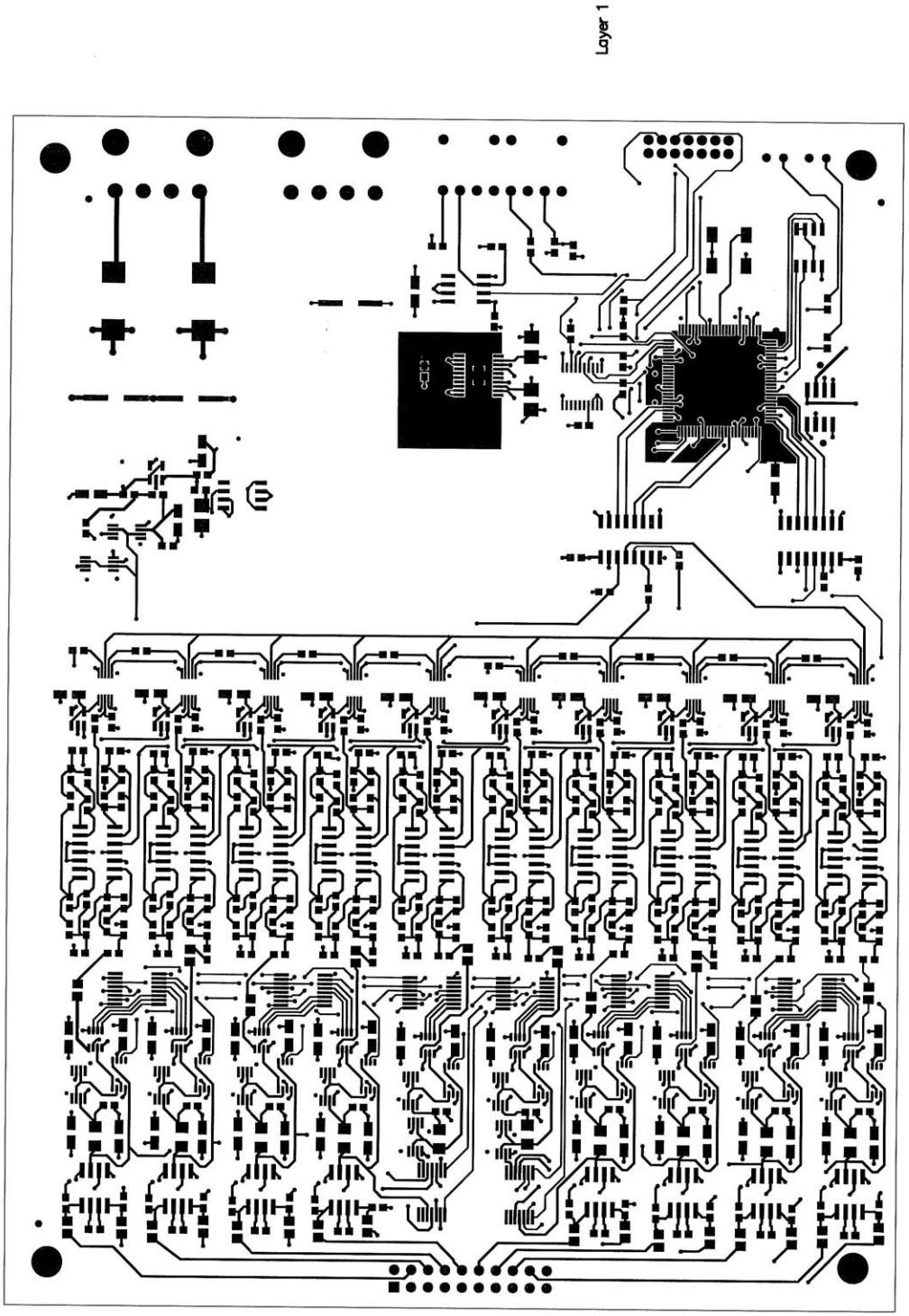


Figure 9-1: Top copper (solder) layer.

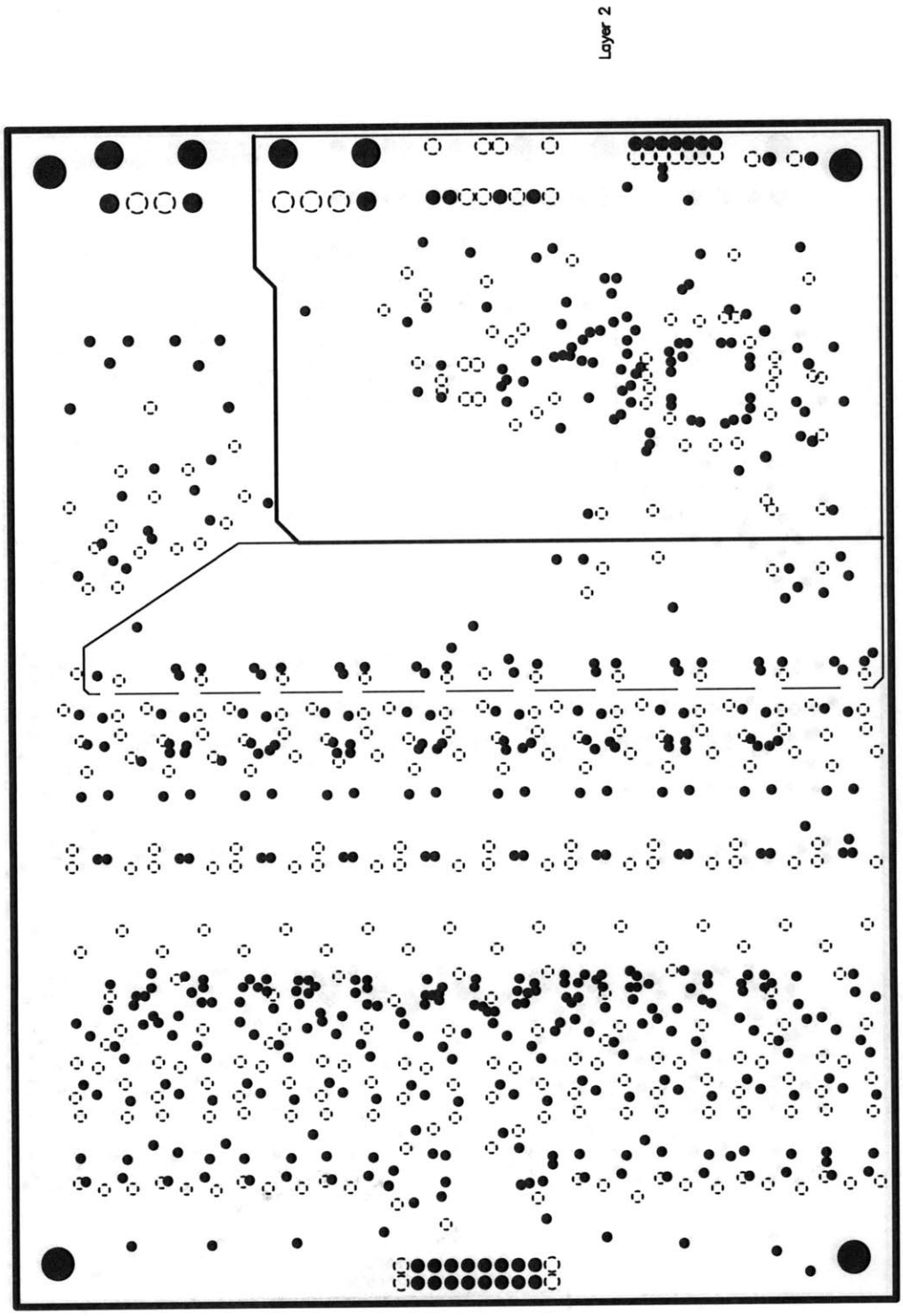


Figure 9-2: Internal ground plane 1.

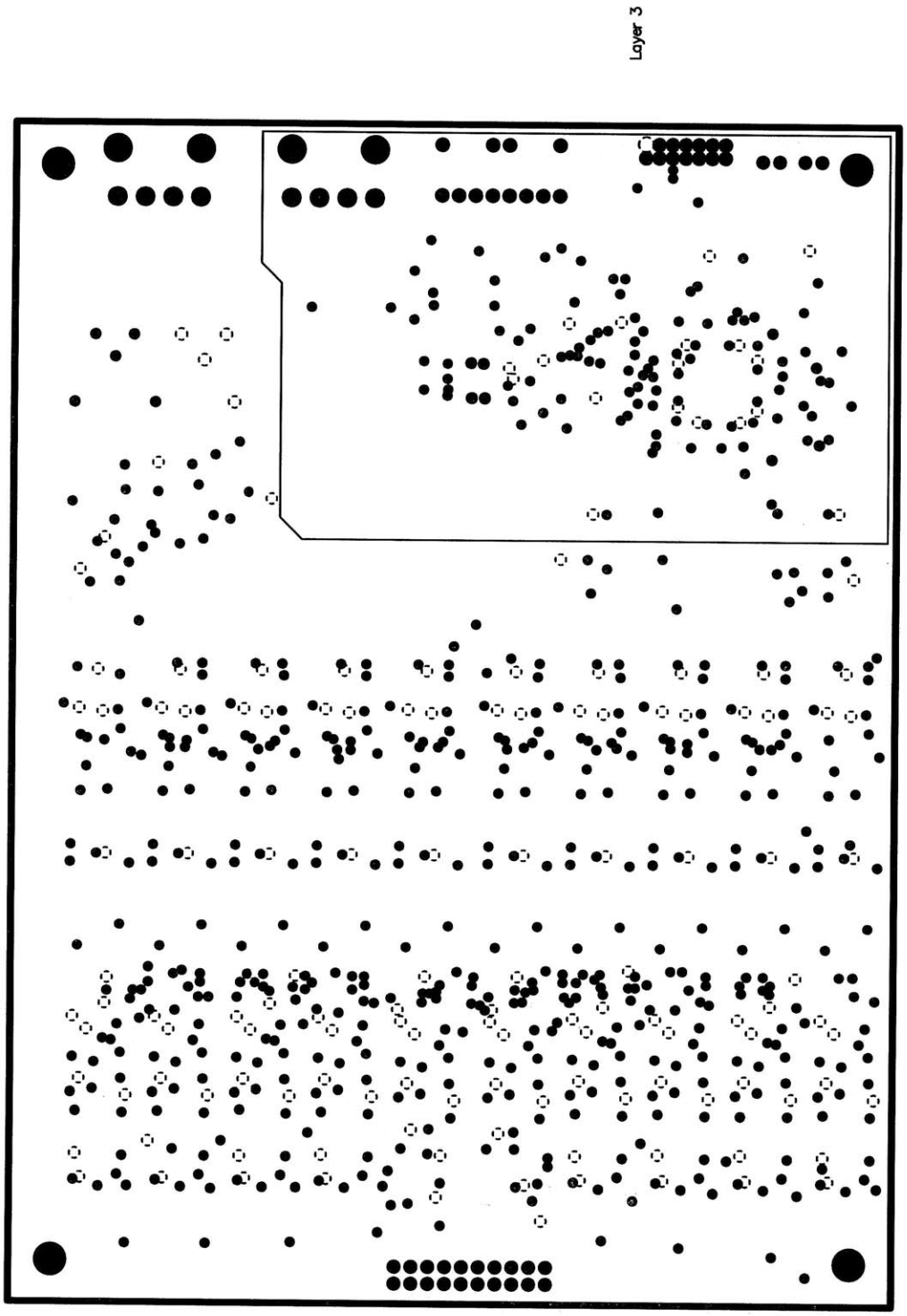


Figure 9-3: Internal ground plane 2.

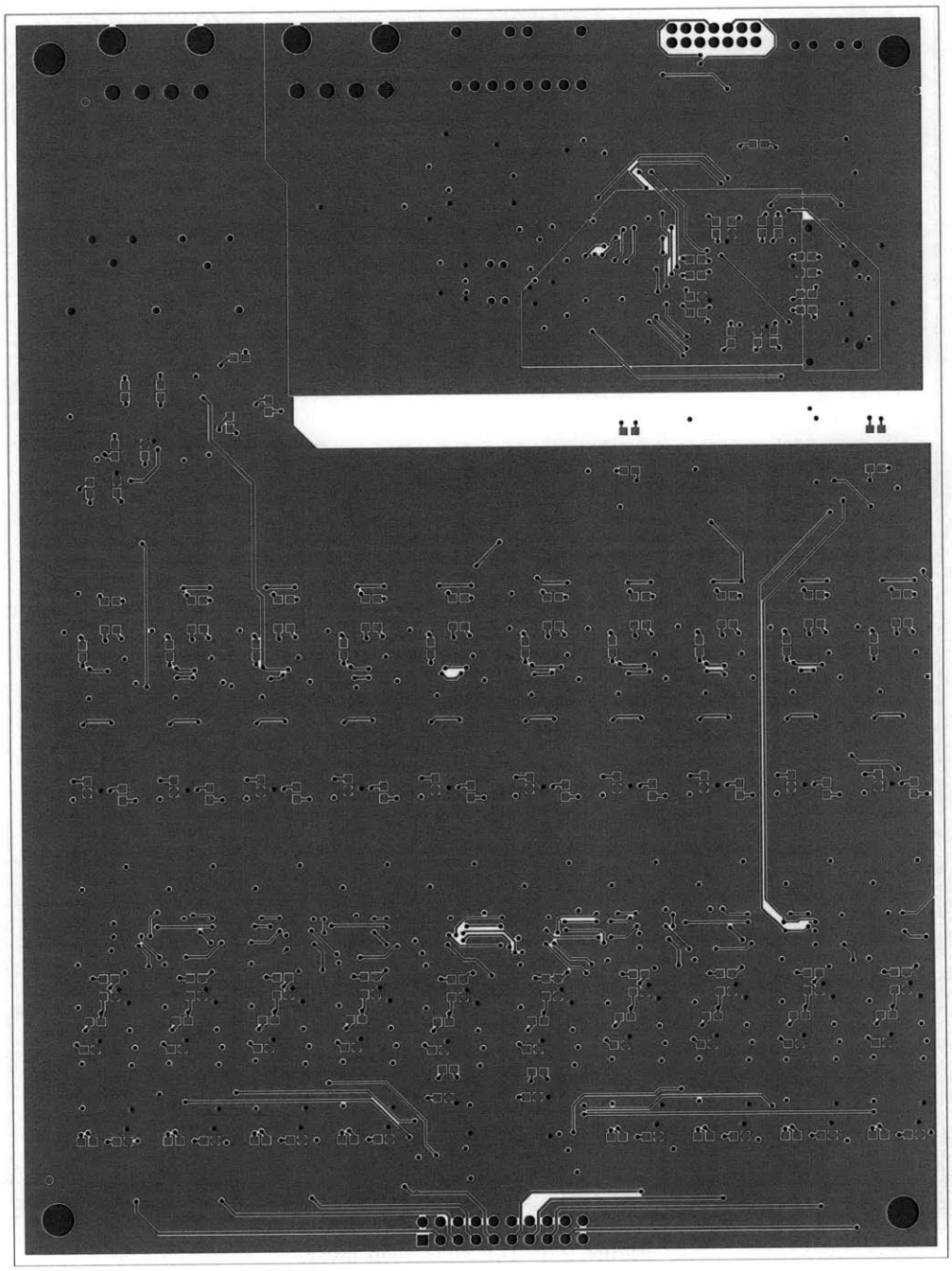


Figure 9-4: Bottom copper (solder) layer.

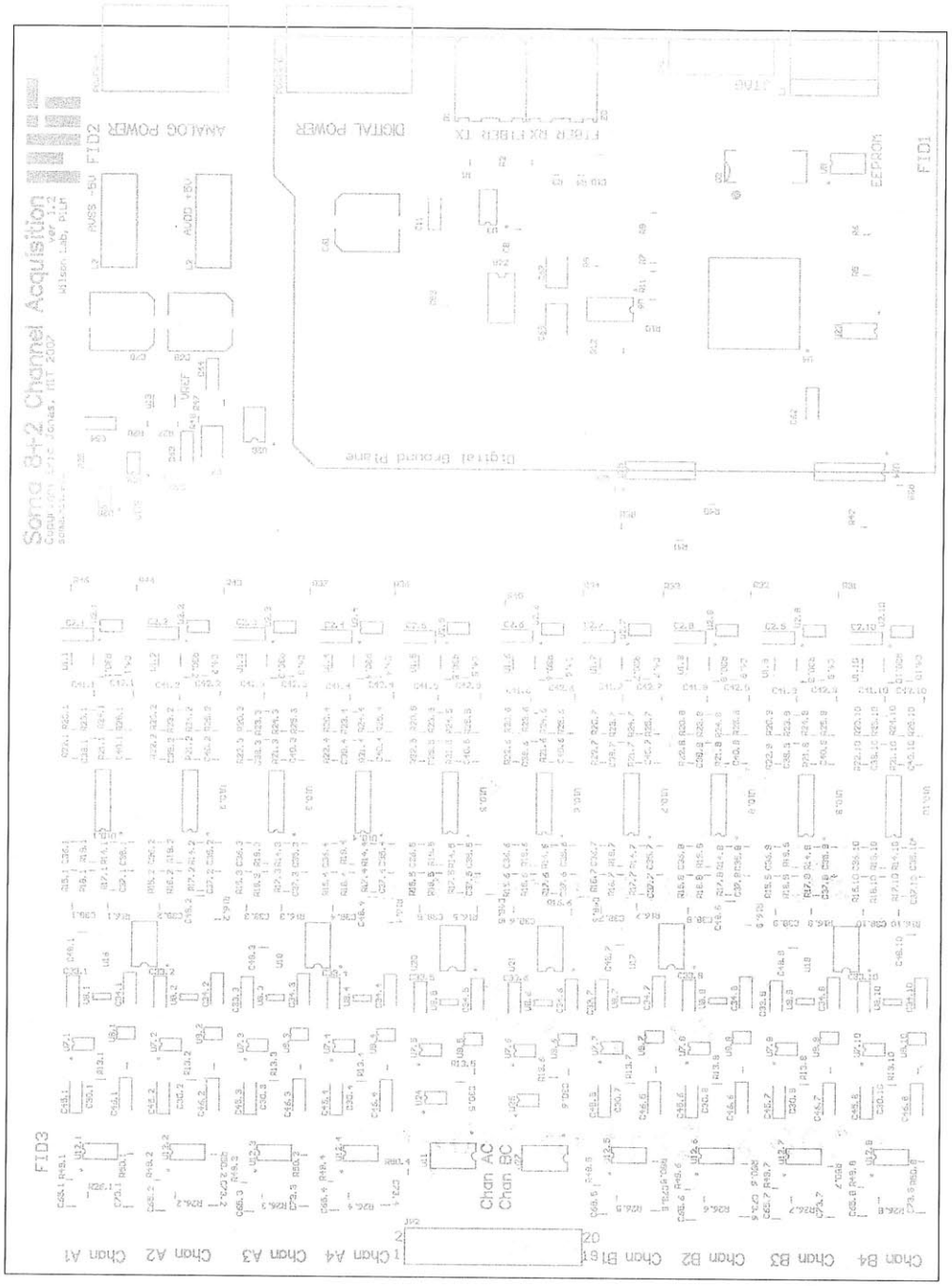


Figure 9-5: Top silkscreen layer.

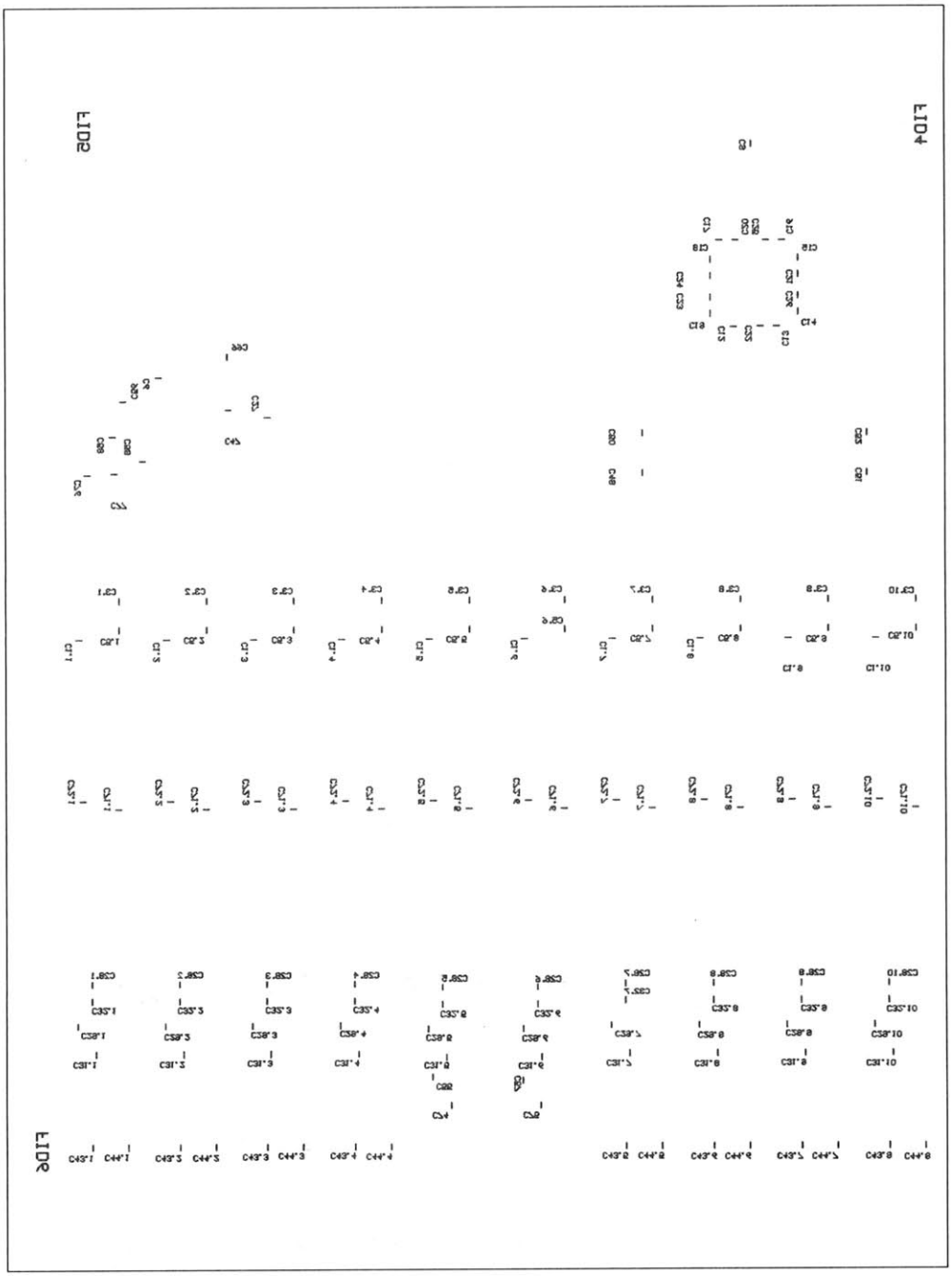


Figure 9-6: Bottom silkscreen layer.

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