Limited-Area Growth of Ge and SiGe on Si

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ABSTRACT
The goal of this thesis is to develop and understand processing conditions that
improve the surface morphology and reduce the dislocation density in limited-area
heteroepitaxy of Ge and SiGe on Si (100) substrates. Low pressure chemical vapor
deposition was investigated for two limiting cases of strain states: thin, strained, high Ge
content SiGe films for transistor applications, and thick, relaxed Ge films, for potential
optoelectronic applications.

Selective epitaxial growth of thin, high Ge-content, strained SiGe on oxide-patterned
silicon was studied, specifically the effect of growth area on the critical thickness. The
critical thickness of Si$_{0.33}$Ge$_{0.67}$ formed by selective epitaxial growth in areas of 2.3 x 2.3
µm was found to be 8.5 nm, which is an increase of 2x compared to the critical thickness
observed for growth in large areas (i.e. for non-selective epitaxy). The sources of misfit
dislocation nucleation in selective growth were analyzed, and misfit generation from the
SiGe pattern edges, due to effects such as local strain concentration, Si surface shape near
the oxide boundary, and preferential SiGe growth near the pattern edge were investigated.

Thin, smooth Ge-on-Si films were developed and the effect of growth conditions on
film morphology was examined to find an optimum temperature and pressure for smooth
film surface (365 °C and 60 torr). A period of delayed epitaxial growth, or “incubation
time” was observed, and a Si surface treatment technique, consisting of a short SiGe
pulse, with negligible SiGe thickness, was employed to realize uniform Ge films with
low surface roughness (RMS<0.3 nm) and reduced incubation time (<20 seconds).

For selective growth of relaxed, thick Ge, approximately 1 µm-thick Ge films were
grown in exposed Si regions on oxide-patterned wafers, and germanium selectivity,
faceting, surface roughness and threading dislocation density were studied as functions of
growth and processing conditions. The optimal growth condition for relaxed Ge selective
epitaxial growth was found (750 °C and 10 torr, with 100 sccms of GeH$_4$ and 10 slipm H$_2$
flow), and the effect of thermal annealing, Ge film thickness, and growth area on the
threading dislocation density was also studied.

Thesis Supervisor: Judy L. Hoyt
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Chapter 1

Introduction

1.1 Motivation

Silicon based microelectronic device technology has been well-developed for many decades, and intrinsic performance of Si devices has advanced greatly [1]. High quality SiGe and Ge epitaxially grown on Si are versatile and cost effective for high-mobility and optoelectronic device applications, as described in early references such as [2-4]. Because the Si-Ge system is compatible with existing Si technology, it can be utilized in numerous device applications, such as strained-channel metal-oxide-semiconductor field effect transistors (MOSFETs), heterojunction bipolar transistors (HBTs), mid-and far-infrared photodetectors, and resonant tunneling diodes [5, 6]. The full spectrum of heteroepitaxy is utilized for such device structures; active regions of the heterostructure-based transistors are strained layers [7-9], and photodetectors and other optoelectronic devices are usually grown as thick, relaxed layers [10, 11].

1.1.1 Strained SiGe-on-Si growth for MOSFET application

High Ge-content strained SiGe-on-Si is a potential channel material in high mobility SiGe-channel p-MOSFETS because of its extremely high hole mobility, with an enhancement of up to 10x relative to unstrained Si [12-14]. Hole mobility in strained
SiGe channel p-MOSFETs increases with increasing Ge composition. However, due to the 4% lattice mismatch between Si and Ge, growing SiGe on bulk Si is challenging due to the onset of misfit dislocation formation above the critical thickness $h_c$. It is calculated that for SiGe-on-Si heteroepitaxy, the equilibrium $h_c$ is 5 nm for $\text{Si}_{0.5}\text{Ge}_{0.5}$, 3.3 nm for $\text{Si}_{0.2}\text{Ge}_{0.8}$, and slightly above 2 nm for pure Ge [15]. Because of this, for SiGe channel p-MOSFET applications where the channel material is grown pseudomorphic to Si, it is necessary to keep the films thin to maintain the strain in the channel.

On the other hand, for the strained SiGe on bulk Si heterostructure, the mobility is shown to degrade significantly for channel thickness below 4 nm due to a combination of phonon and interface scattering [16]. It is reported that when the SiGe channel thickness is limited by critical thickness constraints, increasing Ge composition above 70% does not yield enhanced mobility, because the performance benefit from increasing Ge concentration is compensated by mobility degradation by carrier scattering [16]. Without thickness constraints, mobility enhancement of 6x can be expected for $\text{Si}_{0.2}\text{Ge}_{0.8}$ [17, 18].
Figure 1.1 Mobility enhancement vs. Ge fraction for strained SiGe channels, showing that increasing Ge composition above ~70% does not bring increased mobility, because the channel thickness is limited due to critical thickness constraints. Without thickness constraints, much higher mobility enhancements can be obtained. From C. Ni Chleirigh [16].

Increasing the critical thickness for strained SiGe heteroepitaxy will enable thicker SiGe channels and provide a pathway to avoid the mobility degradation associated with ultra-thin (< 5 nm-thick) films. One approach to solve this problem is to grow SiGe in small areas using Selective Epitaxial Growth (SEG). In this thesis, the critical thickness of SiGe films is studied for high Ge-contents (Si$_{0.33}$Ge$_{0.67}$) on exposed Si regions on oxide-patterned Si wafers with pattern size spanning sub-micron to a few tens of microns.

1.1.2 Growth of relaxed Ge-on-Si for photodiode applications
Silicon-based optoelectronic integrated devices provide a potential solution to the limitation of metal interconnect [19]. In such microphotonic systems, photodiodes and waveguides are integrated onto the Silicon CMOS platform on an electronic chip, and development of Si optoelectronic technology can greatly improve the information processing capability [20].

Germanium is a good candidate for photodiode material because it has the required responsivity and speed to serve as photodiode up to the 1.55 um wavelength range [21]. Ge photodiodes can be integrated with Si waveguides and Si based electronic devices for the distribution and detection of optical signal, and such near-infrared photodiodes can be utilized in optical interconnects, photonic integrated circuits, and optoelectronic Analog-to-Digital Converters (ADCs) [22].

![Figure 1.2](image)

**Figure 1.2** A schematic of germanium p-i-n diode with a Ge-on-Si structure

### 1.1.3 Selective epitaxial growth of SiGe and Ge on Si
For industrial applications, it is envisioned that growth in limited area will have several benefits over growth on the whole wafer [23, 24]. Selective epitaxial growth allows fabrication of advanced device structures and helps increase device density and decrease parasitic capacitances. Selective growth of SiGe has been used for p-MOSFET applications to induce compressive strain in the Si channel [25].

1.2 Outline of the thesis

This thesis studies two limiting cases of epitaxial SiGe and Ge growth on Si, both involving SEG. Chapter 2 covers fundamental concepts and past studies of SiGe and Ge heteroepitaxy, to give background information for topics that will be covered in later chapters. Chapter 3 discusses developing thin, smooth Ge-on-Si films in a non-selective ("blanket") epitaxial process. The impact of growth parameters on the film quality and growth rate is investigated. Chapter 4 focuses on selective growth of thick, relaxed Ge on Si, and the dependence of faceting and threading dislocation density on growth parameters. Chapter 5 investigates selective growth of ultrathin, high Ge content SiGe-on-Si to increase the critical thickness of the strained film. The effect of growth area and shape on the critical thickness is studied, as well as the effects of other growth conditions.
Chapter 2
Thesis Background

This chapter introduces background information to provide a foundation for the topics covered in the following chapters. For the case of heteroepitaxy of SiGe-on-Si growth, theoretical calculation of critical thickness and previous experimental results are summarized. Mechanisms for misfit dislocation formation are briefly reviewed, and the results of prior research on attempts to increase the critical thickness by small area growth are discussed.

When thick Ge is grown on Si, surface morphology and islanded growth become issues. The modes of germanium growth and past studies to improve the material quality are reviewed, including compositional grading, thermal annealing, limited area growth, and aspect ratio trapping. Material characterization by various techniques is briefly discussed, with a focus on characterizing dislocation density by methods of transmission electronic microscopy (TEM) and etch-pit density (EPD) measurement.

2.1 SiGe-on-Si heteroepitaxy

2.1.1. Critical thickness
In SiGe-on-Si heteroepitaxy, crystalline SiGe is grown on a crystalline Si substrate. Due to the 4.2% lattice mismatch between germanium and silicon, an array of interfacial misfit dislocations is formed to relieve the elastic strain in the epilayer. Misfit dislocations are observed for layers beyond a certain thickness, which is called the critical thickness $h_c$. This section reviews past efforts to calculate the equilibrium and metastable critical thickness.

For diamond cubic lattice structures the dislocations glide on the \{111\} plane, and for SiGe heteroepitaxy on Si (100), they form an interfacial misfit dislocation array along the <110> directions [26]. The critical thickness is calculated by analyzing energy or force balance and comparing the self energy of the dislocation formation to the reduced strain energy by the introduction of the misfit dislocation in the epitaxial layer. In a layer with infinite lateral dimensions, the critical thickness is given by the following semiempirical equation: [15, 27]

$$h_c = \frac{g}{x} \ln \left( \frac{4h_c}{b} \right)$$  \hspace{1cm} (2.1)

with

$$g \equiv \frac{b(1-v/4)}{4\pi(1+v)f_0}$$  \hspace{1cm} (2.2)

and

$$f_o = \frac{a_{Ge} - a_{Si}}{a_{Si}} = 0.042$$  \hspace{1cm} (2.3)
where $h_c$ is the critical thickness, $x$ is Ge fraction, and $b$ is Burgers vector. $g$ is defined by equation (2.2), where $v$ is Poisson’s ratio and $f_0$ is the misfit strain between pure Ge and Si. For the SiGe system, $b=0.388$ nm.

There is a slight discrepancy in quoted values for Poisson’s ratio $v$. Houghton’s equation for critical thickness uses $v=0.28$ [15]. However, slightly different values are found in other studies: Feldman et al. quotes $v=0.273$ in his study [28], and $v=0.26$ is also found in several reports [29, 30]. This variance in Poisson’s ratio will result in slightly different equilibrium critical thickness values. For example, at a Ge fraction of 0.5, Si$_{0.5}$Ge$_{0.5}$ will have $h_c$ of 4.07 nm if $v=0.28$, and $h_c$ of 4.2 nm if $v=0.26$ is used. This is a difference of 3.1% in critical thickness, and should be kept in mind during analysis.

For epilayer thickness below $h_c$, pseudomorphic growth without the formation of misfit dislocations is favored, and for epilayer thickness above $h_c$, the formation of a misfit dislocation array is energetically favored. However, experimental results show the empirical critical thickness is almost always larger than the calculated theoretical critical thickness. Using low growth temperature, it is possible to grow pseudomorphic layers with thickness many times greater than that predicted by equilibrium theory. This suggests that there is a metastable growth condition where misfit dislocation nucleation and propagation are kinetically limited either because the nucleation sources are inactive or the dislocation segments do not have sufficient glide velocity. The metastability limit is calculated by analyzing the availability of nucleation sites for misfit dislocations and
their glide velocity by a kinetically activated model. Figure 2.1 plots the equilibrium critical thickness and the metastable regime [15, 31-35].

![Critical thickness plot](image)

**Figure 2.1** Critical thickness for Si$_{1-x}$Ge$_x$ grown on relaxed (100) Si as a function of Ge fraction $x$. Calculated equilibrium critical thickness is shown by the solid line, and theoretical metastable limits at different temperatures are also plotted by dashed line. Experimental results are from [31-35]. Figure reproduced from [15].

### 2.1.2 Sources of misfit dislocations

Misfit dislocations form at the interface between the substrate and an epitaxial film, and typically terminate at the film surface as threading dislocations. There are several
sources of misfit dislocation formation, and general categories are reviewed below [36-39].

A. Fixed sources

Fixed sources of misfit dislocations are sources that increase linearly with an increase in growth area. Threading dislocations from the substrate, or substrate surface inhomogeneities such as particulates, impurities, precipitates, dust particles, residual oxide, or mechanical damages are examples. Matthews and Blakeslee first explained how a threading dislocation (TD) can extend into a misfit dislocation (MD). If the elastic energy released by TD glide is larger than the energy to create MD at the interface, TD segment will glide laterally, creating MD at the interface [40]. Generation of misfit dislocations from threading dislocations via the Matthews-Blakeslee mechanism is shown in Figure 2.2.

TD as a source of misfit dislocations has a very low activation energy and would be the dominant mechanism if the starting substrate had a high density of threading dislocations. However, when commercial Si (100) wafers are used as substrates, the density of threading dislocation in the substrate is extremely low and instead of existing TDs, substrate surface inhomogeneities will most likely be the cause for misfit dislocation generation. For example, oxide clusters on the Si surface can create local stress concentrations into the epilayer and create misfit dislocations [41].
B. Dislocation multiplication

Once long lengths of misfit dislocations are formed, they interact with each other, adding more misfit dislocations as a result. Hagen and Strunk [42] first proposed a multiplication mechanism from two orthogonal misfit dislocations, and other groups studied the dislocation interactions [43-45]. Figure 2.3 shows a schematic diagram of dislocation multiplication by the Hagen-Strunk mechanism. Two orthogonal misfit dislocations of 60° type along the [110] and [\bar{1}10] directions in the interface can share the same Burgers vector and repulsive interaction will occur (Figure 2.3 (a)). Under influences of interaction forces and its own line tension, the misfits form two angular dislocations, one lying in the interface and the other lying on the (111) and (\bar{1}11) glide planes above the interface plane (Figure 2.3 (b)). The dislocation segment on glide planes can reach the free surface and split into two threading dislocations (Figure 2.3 (c)). These dislocations each glide and extend to the wafer or sample edge (Figure 2.3 (d)), resulting in a dislocation network shown in Figure 2.3 (e).
Each multiplication adds new misfit dislocations at the interface, so once created and active, this dislocation interaction can produce a large number of MD segments in the heteroepitaxial interface.

Figure 2.3 Schematic diagram showing dislocation multiplication by the Hagen-Strunk mechanism. Diagram from [45]

C. Surface half-loop nucleation

When the overlayer and substrate have a large lattice mismatch, homogeneous surface nucleation can take place. High strain is needed for such event, as the activation energy to create a half-loop is very large. Mismatch strain of up to six percent is required to nucleate dislocation half-loops at surface steps with reasonable nucleation energy [46, 47]. Because of this, it is not very likely for SiGe-on-Si films to spontaneously generate a dislocation half-loop. However, heterogeneous half-loops can form by edge
imperfections or defects at the epilayer surface. Such heterogeneous half-loops have activation energy larger than fixed sources, but less than homogeneous half-loop nucleation. Figure 2.4 shows a schematic of misfit dislocation formation by surface half-loop nucleation.

Figure 2.4 A schematic diagram showing homogeneous nucleation of a dislocation half-loop at free surface. Surface half-loops could also be generated from a heterogeneous nucleation source, such as surface oxide inclusion [36].

2.2 Selective growth of SiGe on Si

In addition to the benefits described in chapter 1, selective growth of SiGe on Si can have an added benefit of reducing the misfit dislocation density in the epitaxial layer. For the SiGe-on-Si heteroepitaxy where epitaxial film thickness is kept within a few times the critical thickness, misfit dislocation generation is dominated by fixed sources because they have the lowest activation energy for the sources discussed in the previous section. When misfit dislocation nucleation is dominated by localized sources with a fixed areal density such as dust particles or precipitates, it is reported that the misfit dislocation density is lower for smaller growth areas due to the blocking effect of dislocation propagation at the edge [40, 48-51].
As a mismatched layer is grown in a large area and dislocations form, each of these dislocation can laterally glide until the edge of the substrate is reached, leaving a very long misfit dislocation segment. Long glide and long misfit dislocation length increase the probability of dislocation interactions, creating additional misfit and threading dislocations by dislocation multiplication. These additional dislocations at the SiGe/Si interface can continue gliding toward the edge of the substrate and generate even more misfit dislocation length and further dislocation interactions. As a result, many threading and interface dislocations will form in the epitaxial layer, and a dense network of misfit dislocations can be observed, as shown in Figure 2.5.

![Plan-view transmission electronic microscope (TEM) image of misfit dislocation network at Si$_{0.33}$Ge$_{0.67}$/Si(100) interface. SiGe thickness is 16.7 nm and average dislocation spacing is 86.3 nm.](image)

Figure 2.5 Plan-view transmission electronic microscope (TEM) image of misfit dislocation network at Si$_{0.33}$Ge$_{0.67}$/Si(100) interface. SiGe thickness is 16.7 nm and average dislocation spacing is 86.3 nm.

Now consider growth in small areas, as illustrated in Figure 2.6. The idea was first theorized by Matthews et al. [40], that a reduction in growth area will reduce the number
of fixed dislocation nucleation sources in that area because they have certain areal density.

In addition, an active fixed source of dislocation cannot generate long lengths of misfit dislocation in the interface if the growth area is limited – misfit dislocations will run to the edges of the small area and stop. Because the number of MD as well as the length of misfit segment is reduced, the probability of dislocation interactions is decreased and dislocations are eliminated.

Linear dislocation density can be analytically calculated with the following assumptions: only fixed sources of dislocation nucleation with density \( N \) sources/cm\(^2\) exists, one misfit dislocation segment is nucleated at each source, MD segments propagate along \(<110>\) directions away from the source, and misfit dislocations eventually terminate at the oxide sidewall. For a large growth region of area \( L^2 \), the linear dislocation density \( \rho \) is:

\[
\rho = \left( \frac{NL^2}{2} \right) = \frac{NL}{2} \quad (2.4)
\]

If the dimension of growth area is reduced by \( x \) times, the growth area is now \( L^2/x^2 \), and the small region will contain \( NL^2/x^2 \) sources/cm\(^2\). In such case, the linear dislocation density becomes:

\[
\frac{\left( \frac{NL^2}{2x^2} \right)}{L/x} = \frac{NL}{2x} \quad (2.5)
\]
So, the linear misfit dislocation density is proportional to the growth dimension, and as a result, films can be fully strained to much greater thicknesses in small areas compared to in large areas [34, 36].

![Figure 2.6](image)

**Figure 2.6** Schematic of dislocation formation and propagation for (a) larger area and (b) smaller area. Red squares indicate the boundaries of growth area. Given the same amount of fixed sources of dislocation nucleation (represented by small dots), smaller area will have lower dislocation density due to the decrease in numbers of MD generation sources and MD propagation length [34].

Reduced misfit dislocation density for growth in small areas was demonstrated by Fitzgerald, *et al.* for InGaAs material grown on circular or square mesa structures. Figure 2.7 shows cathodoluminescence (CL) images of \(\text{In}_{0.05}\text{Ga}_{0.95}\text{As}\) films of thickness 350 nm. The films are grown on GaAs substrates, in mesas of size ranging from 200 \(\mu\)m to 67 \(\mu\)m. Dislocation density is greatly decreased for smaller mesas, and dislocation spacing is increased by 6x for 67 \(\mu\)m circular mesa compared to the blanket control sample [36, 41, 52].
Figure 2.7 Cathodoluminescence images of the 35 nm-thick InGaAs layer on GaAs substrate. (a) large-area control sample, (b) 200 μm circular mesa, (c) 90 μm circular mesa, and (d) 67 μm circular mesa. Misfit dislocation is significantly reduced for growth in small areas. From [36].

For SiGe-on-Si growth, oxide patterning is used to define the growth area instead of mesa structures, as the CVD technique is preferred for Si-based fabrication. Benefits from selective growth in small area are observed in SiGe/Si heteroepitaxy as well, and Noble et al. showed that the misfit dislocation spacing of SiGe-on-Si heteroepitaxy can be greatly increased when SiGe is grown in selective areas. Comparing 200 nm-thick Si_{0.8}Ge_{0.2} films grown in large and small areas, he found the dislocation spacing was approximately 1 μm for blanket growth [53], but increased to 20 μm between oxide “fingers” spaced 10 μm apart [48]. Stoica and Vescan, Hollander, and Nishida also
reported the increase of critical thickness for small area growth. These results are summarized in Figure 2.8 [54-59].

![Graph showing critical thickness vs. Ge fraction for SiGe/Si heteroepitaxy](image)

**Figure 2.8** Reported critical thickness from selective growth of Si$_{1-x}$Ge$_x$-on-Si at different Ge composition, showing growth in small areas increases the critical thickness of SiGe/Si heteroepitaxy. Theoretical equilibrium thickness (solid line) and 550 °C metastability limit (dashed line) are also plotted. Data from [54-59]

Another approach to increasing critical thickness has recently been demonstrated; by growing SiGe on small Si pillars or fins, stress is managed and engineered by geometric effects [60, 61]. Quantitative equilibrium analysis was carried out by Plummer and coworkers to predict the equilibrium critical thickness as a function of Si pillar radius, and experimental result shows the critical thickness of SiGe is increased when deposited
on thin Si pillars. At 46% Ge content, the critical thickness of Si$_{0.54}$Ge$_{0.46}$ grown on 12 nm-wide Si pillars was 200 nm [60].

2.3 Selective growth of thick Ge on Si

2.3.1 Challenges in Ge-on-Si heteroepitaxy

Growing pure Ge on Si (100) presents additional challenges besides misfit dislocation formation, and one of them is islanded film growth. The initial stages of Ge-on-Si growth have been studied in the past, and it is understood that Ge on Si epitaxy shows a Stranski-Krastanov growth mode, or layer-plus-island growth as shown in Figure 2.9. Initially Ge adsorbates grow in a layer-by-layer fashion, but beyond a few monolayers, Ge continues to grow through the nucleation and coalescence of germanium "islands." It is reported that Ge starts nucleating islands only after a few monolayers of 2-D growth due to the large lattice mismatch [62-65], so for practical observation, Ge-on-Si films of thickness greater than 1 nm will have islanded growth. Such islanded growth results in high surface roughness of the Ge epitaxial film, and this is not desirable because high surface roughness degrades heterojunctions and causes difficulties in process integration [35].
Figure 2.9 Schematic of the three primary modes of epitaxial thin film growth.
(a) Volmer-Weber growth: island formation
(b) Frank-van der Merwe: layer-by-layer
(c) Stranski-Krastanov: layer-plus-island

Ge-on-Si heteroepitaxy shows Stranski-Krastanov growth mode; Ge film shows 2-D growth for the first few monolayers, then starts islanding into a 3-D surface.

Another challenge of thick Ge-on-Si growth is the high number of threading dislocations (TD). Because of the 4.2% mismatch, when a thick germanium film is epitaxially grown on a Si substrate, misfit dislocations will form to relieve strain in the epilayer. A dislocation must terminate at the edge or surface of the film because dislocations cannot terminate within the bulk. With a large number of misfit dislocations in Ge epitaxy, many dislocations leave the growth interface and rise up along the $\{111\}$ plane to the free surface, leaving a threading dislocation segment. These threading dislocations degrade physical and electrical properties of device material and can result in poor performance by reducing carrier lifetimes [20, 39]. For example, a high density of TD can increase the leakage current of rectifying p-n junction diodes and reduce the efficiency of photodetectors [66-68]. It is also reported that Ge diodes with less TD show
more ideal forward characteristics than diodes with a high density of threading dislocations [69]. For these reasons, the threading dislocation density in Ge-on-Si heteroepitaxy should be kept to a minimum.

### 2.3.2 Reduction of threading dislocation density

**A. Compositional Grading**

Several methods have been developed for the reduction of threading dislocation densities (TDD) in lattice mismatched epitaxial growth. One approach is to utilize a buffer layer for compositional grading. This technique is based on the idea that by preventing massive dislocation nucleation, interaction and multiplication events that can increase TDD could be reduced. Each grading layer introduces a small number of new dislocations while providing the strain to glide dislocations out to the edge of the substrate. Calculations predict a reduction of TDD with increasing buffer layer thickness, and for the Ge/Si system, a typical grading rate is 10% Ge μm⁻¹ [20, 70-72]. Figure 2.10 shows an example of the structure and growth conditions of a SiGe buffer layer grown by Ultra High Vacuum Chemical Vapor Deposition (UHVCVD). Due to the increased surface undulation with increased buffer layer thickness, and to reduce dislocation interactions and reduce threading dislocation density, a planarization step by chemical mechanical polishing (CMP) is employed after compositional grading reaches 50% Ge. This process yielded a low threading dislocation density of 2 x 10⁶ cm⁻² [70].
Figure 2.10 (a) Schematic of the structure and UHVCVD growth conditions used for a SiGe graded buffer. Ge concentrations are indicated on the left. Concentration grading is 10% Ge μm⁻¹. (b) Cross-sectional TEM images of the upper graded region and uniform Ge cap. Images from Currie et al. [70]

B. Thermal annealing and limited area growth

Another successful approach to reduce the dislocation density is postgrowth annealing. Several groups have reported that thermal annealing can reduce threading dislocation densities in GaAs-on-Si [73-76] or Ge-on-Si epitaxy [20, 77, 78]. It is suggested that the mechanism for TDD reduction is dislocation glide and annihilation. Under thermal stress, a threading dislocation will glide until it is terminated at the edge of the film or annihilated by colliding with another dislocation.

This thermal annealing can be very effective when applied in cycles of high and low anneal temperatures, and also when combined with selective area growth. By growing Ge in small areas, the propagation length for a TD to the dislocation sinks at the film edge is
shortened, and the TDD can be greatly reduced [41, 79-82]. By utilizing cyclic thermal annealing with selective area growth, very low TDD numbers for Ge-on-Si are reported by Luan (2.3 x 10^6 cm^-2) [23], Loh (3.8-9.6 x 10^6 cm^-2) [83], Hartmann (6 x 10^6 cm^-2) [84], and Olubuyide (4.3 x 10^6 cm^-2) [85].

![Graph showing Threading dislocation density by EPD measurement vs. the width of SEG squares, Figure 2.11](image)

**Figure 2.11** Threading dislocation density by EPD measurement vs. the width of SEG squares, showing the reduction of TDD with the decrease of growth feature size. After growth, Ge film is treated with cyclic thermal annealing of 10 cycles between 900 °C/10min and 100 °C/10min. Graph from Luan [20].

### C. Epitaxial necking and aspect ratio trapping

If threading dislocations rise up to the epilayer surface at a certain angle, it is possible to reduce the density of threading arms by blocking the TD using amorphous materials such as SiO₂ and Si₃N₄ [82]. In the Ge/Si (100) crystal system, misfit dislocations lie along <110> directions and the treading segments rise up on {111} planes, making a 45-
degree angle to the underlying Si (100) growth plane. Because of this, if Ge is grown in a very small area, Langdo and co-workers suggest that threading segments can be blocked by the oxide sidewall if the aspect ratio of the holes in the oxide mask is greater than 1, resulting in a defect-free top Ge surface on Si as shown in Figure 2.12 [39]. This idea is followed by several groups [86-88], and dislocation-free Ge top layers have been demonstrated by aspect ratio trapping (ART).

![Figure 2.12](image.png)

**Figure 2.12** A cross-sectional diagram showing the principles of epitaxial necking. Threading dislocations are “trapped” by the oxide sidewalls and Ge surface is free from dislocation threads. Schematic from [39].
Figure 2.13 Cross-sectional TEM images of Ge in trenches of (a) 200 nm width and (b) 400 nm width. Dislocations originating at the Ge/Si interface are trapped by the oxide sidewall and defect-free Ge is found at the top of the trenches. The dashed line in each image shows where the trench height is equal to its width. Images from [87].

2.3.3. Threading dislocation density measurement techniques

The threading dislocation density of thick Ge films is typically measured by two methods, etch-pit density (EPD) measurement or plan-view TEM analysis. TEM is more effective in observing dislocations because of its excellent resolution, but it requires extensive and skillful sample preparation, as described in Appendix A. In addition, TEM is difficult when the TDD is below \(10^7\) cm\(^{-1}\) [89]. In EPD measurement, Ge films are inspected under an optical microscope after being etched by a mixture such as CH\(_3\)COOH (65mL), HNO\(_3\) (20mL), HF(10mL), and I\(_2\) (35mg) [78, 85]. EPD has a smaller statistical error bound because the area of observation is larger than TEM.

Ishida et al. pointed out that there is a disagreement between EPD and plan-view TEM-counted TDD. Such discrepancy was first noted in TDD measurements of GaAs on Si, and with threading dislocation density in the range of \(10^6\)-\(10^7\) cm\(^{-2}\), EPD often gave measurements about a factor of two less than that by TEM [90, 91]. Shimizu and Stirland attribute this difference to the resolution limit of the optical microscope used in the EPD technique. If two etch-pits overlap each other, it becomes difficult to resolve individual pits. Considering the overlapping of etch-pits, the EPD/TEM ratio can be estimated by a statistical model proposed by Stirland and coworkers [92, 93]:

...
\[
\frac{EPD}{Nd} = \frac{[1 - \exp(-\pi Nd \cdot r^2)]}{\pi Nd \cdot r^2}
\] (2.6)

\(Nd\) is the threading dislocation density measured by TEM, \(r\) is the “etching resolution” parameter defined as the closest distance at which two similar etch-pits can be distinguished. For a germanium etch solution, typical \(r\) value is approximately 1 \(\mu\)m.

Using equation 2.6, EPD/TEM ratio based on statistical model is 0.98 for TDD < 10^6 \(cm^2\), but it drops to 0.85 for TDD ~10^7 \(cm^2\), and 0.3 if TDD is near 10^8 \(cm^2\). In the literature, experimental EPD/TEM ratio is around 0.5 for TDD in the 10^7 \(cm^2\) range [94]. It is possible to reconcile the inconsistency between EPD and TEM measurements by counting some small etch-pits that only show up under high magnification in EPD optical microscopy. Nevertheless, it is strongly recommended that when EPD counting is used for films with high threading dislocation density, TEM techniques should be utilized to verify the TDD carefully [20].

### 2.4 Chapter summary

In this chapter, a few fundamental concepts of SiGe- and Ge-on-Si heteroepitaxy are covered. In a lattice mismatched system, misfit and threading dislocations are introduced to relieve strain in the film when epilayer thickness is above the critical thickness. Theoretical equilibrium thickness is calculated by using energy balance, and experimental data indicates that there is a metastable regime where SiGe films above the critical thickness can be found without strain relaxation by misfit dislocation nucleation.
There are different sources of misfit dislocation generation, and critical thickness can be increased by selectively growing SiGe in small areas.

For thick, relaxed Ge epitaxy, islanding and threading dislocation become important growth issues. Compositional grading, thermal annealing, growth in limited areas, and aspect ratio trapping can be used to reduce the threading dislocation density. TDD is typically measured by EPD or TEM, and care should be given when analyzing threading dislocation density in a highly-defected film, as discrepancies in measurement data have been reported, and EPD can show smaller than actual TDD values due to the resolution limit of optical microscopes and the etching technique itself.
Chapter 3
Development of Thin, Smooth Ge-on-Si Films

3.1 Introduction

In this chapter, thin, flat germanium blanket film growth is experimentally investigated. Growing Ge film with high material quality and thickness less than 20 nm is desired for many applications, and Figure 3.1 shows a few structures that utilize thin Ge epitaxial layers. Such structures can be applied to Ge channel MOSFET technologies or to vertical PIN photo-detectors operating at 1.55 μm [95, 96].

![Figure 3.1 Examples of structures with thin Ge epitaxial growth.](image)

(a) Pseudomorphic Ge growth directly on bulk Si substrate
(b) Ge-on-Si growth as a seed layer before relaxed, thick (>1um) Ge growth at a higher temperature
(c) Ge growth on SiGe buffer
(d) Ge growth on strained Si.
For sections 3.2 to 3.4, Ge on a bulk Si wafer as illustrated in Figure 3.1 (a) is utilized to study the Ge growth mode and surface morphology, due to processing simplicity and high throughput of this structure. Later in section 3.5, Ge on relaxed SiGe and strained Si will also be discussed.

To fabricate thin Ge on bulk Si, p-doped six-inch CZ Si wafers are used as substrates. After pre-epi surface cleaning, which includes standard RCA clean with an additional HF dip, DI water rinse, and spin-rinse dry steps, the wafers are loaded into an Applied Materials Epi Centura™ Low Pressure Chemical Vapor Deposition (LPCVD) growth system. A hydrogen prebake temperature of 1080 °C and duration of 30 sec is used, then germanium is epitaxially grown to a thickness of 1 to 60 nm using GeH₄ gas as a precursor. For most of this chapter, focus is given to Ge samples with thickness less than 20 nm.

3.2 Growth mode of Ge on Si and incubation time

To understand Ge growth mechanism on Si, a set of samples was grown with different growth times, resulting in film thickness ranging from 1 to 60 nm. The wafers are treated with identical pre-epi cleaning and prebake step to minimize process variation. During Ge growth, the temperature is kept at 365 °C and pressure is kept at 30 T. Table 3.1 summarizes the test samples. Ge thickness is measured by a KLA Instruments
UV1280 spectroscopic ellipsometer. The numbers in parenthesis indicate wafer run numbers.

Table 3.1 List of Ge-on-Si samples

<table>
<thead>
<tr>
<th>Sample</th>
<th>Growth time (sec)</th>
<th>Ge film thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A (#4250)</td>
<td>75</td>
<td>1.3</td>
</tr>
<tr>
<td>B (#4182)</td>
<td>100</td>
<td>8.6</td>
</tr>
<tr>
<td>C (#4251)</td>
<td>130</td>
<td>13.5</td>
</tr>
<tr>
<td>D (#4128)</td>
<td>150</td>
<td>19.9</td>
</tr>
<tr>
<td>E (#4249)</td>
<td>400</td>
<td>61.6</td>
</tr>
</tbody>
</table>

Care should be given when quoting film thickness for thin, rough films by UV1280. When measured film has a rough surface, the thickness measured by UV1280 spectroscopic ellipsometer is an average value, corresponding to the best-fit value of the reflectance curve. AFM surface scans are utilized with UV1280 to fully understand the film morphology, and looking at sample A in Figure 3.2, it is noticed that the film is islanded during an initial stage of Ge epitaxy. Typical Ge nodule has a height of 2.5 nm and width of 50 nm. However, film thickness as measured by the ellipsometer is 1.3 nm, which is much smaller than the peak height of the Ge islands. This is because the UV1280 thickness is an average value, so for very thin films with high roughness, AFM or profilometer scans should be used to obtain details on the surface morphology before quoting film thickness from UV1280.
Ge shows an island growth mode at growth condition of 365 °C and 30 torr. Instead of forming flat, 2-D monolayers, Ge film starts with island formation as can be seen from sample A. Islanding becomes more severe as film thickness increases to around 10 nm. At growth time of 100 sec and thickness 8.6 nm (Sample B), average nodule height increases to 3.5 nm and width 90 nm. However, after the film thickness becomes greater than 13 to 15 nm, the islands start to coalesce into a flatter surface. Films thicker than 20 nm do not show prominent islanding, but they show more uniform surfaces, with typical undulation height less than 2 nm and width of 200 nm. Figure 3.2 (a) shows AFM images of Ge-on-Si samples that show this islands-to-smooth surface evolution. Figure 3.2 (b) compares the cross-sectional profiles of Ge-on-Si samples, taken from 1 x 1 μm AFM scans. Again, islanded growth mode is dominant for samples A through C, and the film coalesces for samples D and E.
Figure 3.2 (a) AFM Surface images and (b) sectional profile of Ge-on-Si growth at different growth stages, showing the surface evolution as film thickness is increased from 1.3 nm (sample A) to 60 nm (Sample E). Sample thickness and growth times can be found in Table 3.1. Growth temperature is 365 °C, pressure is 30T. Surface images and sectional profiles are captured from 1 x 1μm AFM scans, and the scale bar of sample E applies to all micrographs in (a). In (b) the horizontal axis corresponds to 1 μm.

Surface root mean square (RMS) value as a function of Ge film thickness is plotted in Figure 3.3. About 5 AFM scans were taken per sample for samples A through E, and the RMS roughness was averaged over the measurements. Depending on the scanning location, the RMS roughness may have a variation of up to 5%. For growth thickness of 0 nm, CZ Silicon with no Ge growth was taken as a control sample. The RMS roughness of bare Si sample is 0.23 nm, and is limited by intrinsic noise from the AFM system.
Figure 3.3 RMS roughness as a function of Ge film thickness. Values taken from 1 x 1 μm AFM scans, and may have measurement variation of up to 5%, depending on the scanning location. Growth temperature and pressure are 365 °C and 30 T.

Using the same set of data, Ge film thickness can be plotted as a function of growth time (Figure 3.4). The UV1280 ellipsometer was used for thickness measurement, and from the growth curve, one characteristic feature is noticed. For the Ge-on-Si epitaxy, there is a noticeable time during which there is no Ge growth even though GeH$_4$ gas is being supplied in the CVD chamber. This time is denoted as “incubation time,” and was also reported by Kobayashi and Halbwax [97, 98]. This is not desirable because uncontrolled period of delayed growth can cause surface contamination issues, increase the total processing time, and make growth rate calibration difficult. Incubation time is processing condition dependant, and the next section investigates how the growth parameters effect the incubation time as well as Ge surface morphology.
Figure 3.4 Ge thickness as a function of growth time. The growth curve shows a period of delayed epitaxy, or the “incubation time”. This is undesirable because it increases total processing time and also makes growth rate calibration challenging. Film thickness is measured by UV1280 spectroscopic ellipsometer. Growth condition is 365 °C and 30 T, GeH₄ gas flow is 100 sccm and H₂ carrier gas is set at 10 slpm.

3.3. Effect of temperature and pressure on Ge-on-Si growth

3.3.1 Growth temperature

To study the effect of growth temperature, Ge-on-Si samples are epitaxially grown at different temperatures while keeping the chamber pressure constant. For each temperature, a set of samples are grown with varying thicknesses, from approximately 1 nm to 40 nm. Figure 3.5 (a) shows the growth curves of four different temperatures, 335, 350, 365, and 380 °C. The graph shows two characteristics: first, the incubation time is a
strong function of temperature. When the temperature is increased from 335 °C to 385 °C, the incubation time decreases by more than 8x, from 600 sec to 70 sec. The reason for this dependency will is discussed in detail with the effect of pressure on incubation time in section 3.3.2.

Another behavior to notice from the plot is that the growth rate is temperature dependant. At temperature of 335 °C, the growth rate (given by the slope, not including the incubation time) is 2.6 nm/min., and the growth rate increases to 8.4 nm/min. at 365 °C and 19.2 nm/min. at 385 °C. This is because at these growth conditions, Ge growth is surface reaction rate limited and the growth rate is a function of a temperature with a relationship:

\[ R \approx e^{-\frac{\Delta E_a}{kT}} \]  

(3.1)

where \( R \) is the growth rate, \( \Delta E_a \) is activation energy of the reaction, \( k \) is Boltzmann’s constant of 8.617 \( \times \) 10\(^{-5}\) eV/K, and \( T \) is the temperature in Kelvin. By plotting \( \ln(R) \) vs. \( 1/T \), the activation energy of Ge epitaxy can be extracted from the slope of the curve (Figure 3.5 (b)), and the value of \( \Delta E_a \) is found to be 1.48 eV. This is slightly larger than previously published activation energy of 1.08 eV by Olubuyide [96], but it could be because the growth rate quoted by Olubuyide does not count the incubation time. Earlier studies by Bramblett and Xie reports the activation energy as 1.44 eV with GeH\(_4\) and 1.56 eV with GeH\(_6\) precursors [64, 99], and the value of 1.48 eV from this thesis agrees with their result.
Figure 3.5 The effect of temperature on (a) Ge-on-Si growth curve and (b) film growth rate. As temperature is increased, the growth rate increases and incubation time is decreased. Chamber pressure was set at 30 T, and prebake condition is 1080 °C for 30 seconds. GeH₄ gas flow is 100 sccm and H₂ carrier gas is set at 10 slpm.

3.3.2 CVD chamber pressure
In this section, the effect of reaction chamber pressure on the Ge growth curve is investigated. Ge-on-Si samples are grown after identical pre-epi treatment and at a temperature of 365 °C, and the chamber pressure is varied from 30 T to 60 T. Gas flow of 100 sccm GeH₄ and 10 slpm H₂ is selected and kept constant. At each pressure, a set of samples are epitaxially grown to have a range of Ge film thickness, from 0.5 nm to 20 nm. After growth, Ge thickness was measured by UV1280 spectroscopic ellipsometry. The growth curves are plotted in Figure 3.6.

![Figure 3.6](image)

Figure 3.6 The effect of chamber pressure on Ge-on-Si growth curve. Growth rate is 11.8 nm/min. for 30 T, 12.7 nm/min. for 45 T, and 9.7 nm/min. for 60 T. Growth rate does not depend on the pressure significantly because the deposition is limited by surface reaction rate and not by mass transfer rate. Increasing chamber pressure reduces the incubation time. Growth temperature is 365°C and prebake condition is 1080 °C for 30 seconds. GeH₄ gas flow is 100 sccm and H₂ carrier gas is set at 10 slpm.
Similar to the case of temperature, the incubation time is a strong function of growth pressure and is reduced as pressure increases; the incubation time for Ge epitaxy is 300 sec at 30 °C, 200 sec at 45 °C, and is reduced to 75 sec at chamber pressure of 60 T.

Because the growth is limited by surface reaction rate under these processing conditions, the growth rate is not dependent on the chamber pressure and only depends on the temperature. Growth temperature is kept constant at 365 °C for all samples, and growth rate is comparable for different pressures (11.8 nm/min. for 30 T, 12.7 nm/min. for 45 T, and 9.7 nm/min. for 60 T), as can be seen from the slopes of the growth curves.

From Kobayashi and Murota [100-102], who also reported similar incubation period in Ge epitaxy, the paper suggests that a source of incubation time is suppression of adsorption and/or decomposition of GeH₄ on the H-terminated Si when H₂ is used as carrier gas. At the start of Ge-on-Si growth, the exposed Si atoms from sample surface are bonded with H atoms. In order for Ge to expitaxially grown, the Si-H bonds need to be broken and hydrogen atoms desorbed from substrate surface into reaction chamber, enabling adsorbed Ge atoms to form Si-Ge bonds. The results from this temperature/pressure study support Kobayashi’s theory; increasing chamber temperature helps break Si-H bonds and reduces incubation time. Increasing chamber pressure also reduces the incubation time, because the increase in GeH₄ partial pressure makes more Ge atoms available for adsorption into exposed surface and increases the rate of Si-Ge bond formation.
3.3.3 Surface roughness

Thin Ge film could be incorporated into the channel of a MOSFET device, and in such applications, it is important to keep the surface roughness to a minimum because a rough Ge film in the channel will degrade the device performance by increasing carrier scattering [16, 95]. Growth temperature and pressure affect Ge film surface morphology, and this section investigates how the growth parameters change Ge-on-Si film roughness. Surface roughness is measured by atomic force microscopy. Five to seven 1 x 1 μm AFM scans are taken per sample, and the RMS roughness was averaged over the measurements.

![AFM scans of Ge films grown on Si at various temperatures and pressures. Images are captured from 1 x 1 μm scans, and the numbers indicate the RMS surface roughness of Ge samples. Film thickness range from 13 to 21 nm. The scale bar applies to all micrographs in the figure.](image)

Figure 3.7 AFM scans of Ge films grown on Si at various temperatures and pressures. Images are captured from 1 x 1 μm scans, and the numbers indicate the RMS surface roughness of Ge samples. Film thickness range from 13 to 21 nm. The scale bar applies to all micrographs in the figure.
Figure 3.7 shows AFM images of samples grown at various temperatures and pressures. Film thickness ranges from 13 nm to 21 nm. Increasing temperature from 335 to 365 °C reduces RMS roughness and helps keep the film flat. However, when the temperature is increased to 380 °C, the film starts roughening again. This may be explained by Ge surface diffusion. At a very low temperature, Ge atoms do not have enough surface diffusivity to find adatom incorporation sites such as terraces or ledges. Most of the Ge adatoms will be desorbed back into the reaction chamber (and thus contribute to very low growth rate), but those atoms that do attach to the substrate will form a new crystal steps and increase surface roughness. At higher (intermediate) temperatures, Ge adatoms will attach at the existing crystal steps or ledges to form more uniform monolayer. When the temperature is very high, the Ge atoms have enough thermal energy to break Ge-Ge atomic bonds, and Ge atoms from the already-formed film can move onto outer surface to reduce film strain built up by Ge/Si lattice mismatch. Such atomic movement increases surface undulation and film roughness. Figure 3.8 shows a schematic of Ge growth at different temperatures.
Figure 3.8 Schematic of Ge growth at different temperatures.
(a) at a low temperature, Ge adatoms do not have enough surface diffusivity and attach randomly on substrate, forming rough surface.
(b) at higher temperatures, Ge adatoms move across the substrate and attach onto crystal steps or ledges, making the surface smooth.
(c) when the temperature is very high, Ge atoms from inner layers can break Ge-Ge bonds and diffuse towards the outer surface. This results in film roughening.

Increasing the chamber pressure decreases RMS roughness and forms smoother Ge films. The effect is very noticeable for the case of 365 °C; when pressure is changed from 30 T to 60 T, surface roughness is reduced by more than a factor of 2, decreasing from an RMS value of 1.46 nm to 0.68 nm. It is not very clear why changing the chamber pressure changes the surface morphology, but it is speculated that reduction in the growth delay period by increasing pressure, as observed in Figure 3.6, could be the reason behind this behavior. It is well known that bare silicon surfaces are highly reactive and many undesired impurities are easily adsorbed [103]. At a lower pressure such as 30T, the incubation time is as large as 300 sec, and because there is no film growth during that
time, impurities can adsorb onto the substrate surface, causing micro-defects and rough film. By increasing the chamber pressure, reduced impurity incorporation is possible as a result of decrease in delay period, and this could lead to smoother Ge films. For pressures higher than 60 T, Ge gas phase nucleation is observed, and since it should be avoided in Ge epitaxy, the optimized growth condition for thin Ge-on-Si is chosen to be 365 °C and 60 torr.

3.4 Effect of hydrogen flow on Ge-on-Si growth

3.4.1 Hydrogen flow and Ge growth curve

In this section, the effect of hydrogen flow on the Ge growth curve is studied to better understand the relationship between gas pressure and Ge epitaxy. The reaction chamber temperature and pressure are kept at 360 °C and 60 Torr. GeH₄ gas flow is also kept constant at 100 sccm, and only the H₂ carrier gas flow was varied from 5.1 slpm to 15 slpm. Ge samples were epitaxially grown and the growth curves are plotted in Figure 3.9. The slopes of the growth curves do not change much by flowing different amounts of H₂ and are relatively constant for the entire set of Ge-on-Si growth samples, confirming that the growth is under the surface reaction rate limited region. However, it is noted that the curves are shifted and the incubation time is reduced for lower hydrogen flow. This is also consistent with the previous data in Figure 3.6, because when total chamber pressure is held constant, GeH₄ partial pressure increases with decreasing H₂ gas flow.
Figure 3.9 Hydrogen gas flow and growth curve. At 365 °C, chamber pressure was held at 60 T and hydrogen flow was varied. The bottom slit has H₂ flow of 5 slpm for all samples, but the top (main) slit flow is varied from 0.1 slpm to 10 slpm, resulting in total hydrogen flow of 5.1 slpm to 15 slpm. The slope of the growth curve does not change by flowing different amounts of H₂, but the curves are shifted and incubation time is reduced for lower hydrogen flow.

3.4.2 GeH₄ partial pressure and growth curve

Chamber pressure is the sum of H₂ and GeH₄ partial pressures, and germane partial pressure can be easily calculated by taking a ratio between GeH₄ and H₂ gas flow, and multiplying the total chamber pressure by gas ratio:

\[
P_{GeH_4} = P_{total} \times \frac{U_{GeH_4}}{U_{GeH_4} + U_{H_2}} \times 0.3
\]  

where \( P_{GeH_4} \) is germane partial pressure, \( P_{total} \) is total chamber pressure, \( U_{GeH_4} \) and \( U_{H_2} \) are germane and hydrogen gas flow, respectively. The ratio is multiplied by 0.3 because the GeH₄ gas used in the experiment is 30% diluted.
Figure 3.10 shows the incubation time as well as Ge surface roughness as a function of germane partial pressure. From Figure 3.10 (a), it can be seen that incubation time is reduced as GeH$_4$ partial pressure is increased. The same argument from the previous section can be used; the period of delayed growth results from time required to break existing Si-H bonds and replace them with Si-Ge bonds. Thus by increasing germane partial pressure, more Ge atoms are available to form Si-Ge bonds and thus reduce the incubation time. From figure 3.10 (b), it is also shown that increasing GeH$_4$ partial pressure improves Ge surface smoothness, because reduction in incubation time is directly related to reduction in RMS roughness of the epitaxial film. During the delayed growth, impurities can fall onto exposed substrate surface and become defects in the film. Such defects can act as heterogeneous nucleation source of Ge growth, increasing the number of Ge islands and thus increasing the RMS surface roughness.

![Graphs showing incubation time and Ge surface RMS roughness vs. GeH$_4$ partial pressure.](image)

**Figure 3.10** (a) Incubation time as a function of germane partial pressure. As GeH$_4$ partial pressure is increased, incubation time is reduced. (b) Ge surface RMS roughness vs. GeH$_4$ partial pressure. Because surface roughness also depends on the film thickness, samples are grouped into two sets based on the Ge thickness. For the RMS roughness value, an average over five AFM
scan measurements is taken per sample. The RMS value is location dependent, and depending on scan spot, a variation of up to 5% is found. Growth temperature is 365 °C, and pressure is 60 torr.

### 3.5 Si surface treatment with SiGe pulse

A method of Si surface treatment by flowing a short SiGe pulse before Ge growth is utilized to further improve the surface smoothness and reduce incubation time for Ge-on-Si growth. After standard pre-epi wafer cleaning and prebake step, the sample is treated by a short SiGe “pulse,” for the duration of 5 to 15 seconds. During this time, a mixture of gases containing SiH₄ and GeH₄ is introduced to the reaction chamber at an appropriate temperature. After the SiGe pulse treatment, pure Ge film is deposited as before, and it is observed that the Ge film grown after treatment has both reduced total growth time and surface roughness. This SiGe treatment can be applied to Ge-on-Si growth where Si can be a bulk CZ substrate or strained Si (Fig 3.11). This SiGe treatment study was performed in collaboration with Leonardo Gomez [95].
3.5.1 Ge on CZ Si wafers

Experiments were designed to study the growth of Ge on relaxed, bulk Si wafer with and without SiGe interfacial treatment. After prebake step, 20 sccms of SiH₄ and 22 sccms of GeH₄ with 10 slpm of H₂ carrier gas was introduced into the CVD chamber at 525 °C. This process condition would deposit Si₀.₅Ge₀.₅ film if sufficient growth time were given, but for a short pulse of 5 to 15 seconds, SiGe layer is not visible as a separate layer in the secondary ion mass spectroscopy (SIMS) profile, or by TEM, suggesting that the SiGe layer is very thin. After the treatment, GeH₄ gas is flowed to continue Ge epitaxial growth on Si. Because SiGe pulse is very thin, this treatment technique should not impact the desired properties of thin Ge films, such as carrier mobility.
Figure 3.12 shows the measured Ge thickness versus time for Ge-on-Si growth with or without SiGe interface treatment. For SiGe treatment, pulse times of 5 sec and 15 sec are used. From the plot, it is clear that the SiGe pulse reduces the Ge incubation time significantly. The incubation time of Ge growth on bare Si substrate is 75 seconds, but is reduced to approximately 15 s when SiGe pulse is applied. This is beneficial because the reduction in incubation time improves throughput and also helps growth rate calibration. Ge growth rate after incubation time is comparable for all curves, because the growth rate only depends on the growth temperature for a given growth condition.

Another benefit of SiGe pulse technique is the reduction of Ge surface roughness by decreased incubation time. Figure 3.13 compares the surface of two Ge-on-Si samples, with and without SiGe treatment. With no SiGe pulse, a 3.5 nm-thick Ge film on bulk CZ Si substrate has RMS roughness of 0.69 nm. The roughness is reduced to 0.25 nm when 15 sec SiGe pulse was used before Ge epitaxy.
Figure 3.12 Measured Ge thickness versus time for Ge-on-Si growth utilizing no SiGe surface treatment (red dotted line), a 5 second treatment (green solid line), and a 15 second treatment (blue dashed line). Ge growth on the sample with the SiGe pulse treatment shows significant reduction in incubation time. Film thickness measured by UV1280 spectroscopic ellipsometer.

Figure 3.13 1 x 1 μm AFM surface scan of two Ge-on-Si samples, showing the effectiveness of SiGe surface treatment in reducing surface roughness. (a) With no SiGe surface treatment. Film thickness is 3.5 nm, and RMS roughness is 0.69 nm. (b) With a 15 second SiGe pulse treatment. Film thickness is 3.4 nm, and RMS roughness is 0.25 nm.

Figure 3.14 shows the relationship between incubation time of Ge epitaxy and germanium surface roughness. For all data points, the growth temperature and pressure are 365 °C and 60 T, and GeH₄ flow rate is 100 sccm. For non-SiGe treated samples, H₂ flow rate was varied to change GeH₄ partial pressure without changing the chamber pressure. For SiGe treated samples, pulse treatments of 5 sec and 10 sec are used while H₂ flow was kept at 10 slpm. It is again demonstrated that the reduction of incubation time has a direct relationship in decreasing RMS roughness of Ge surface, supporting the argument that Ge surface roughness is caused by impurity incorporation on the bare Si substrate surface during the period of delayed epitaxial growth.
Figure 3.14 Ge surface roughness as a function of incubation time, showing the RMS roughness increases as incubation time is increased. RMS roughness is measured by 1 x 1 μm AFM surface scans, and incubation time is read off from Ge growth curves. For all data points, growth temperature and pressure are 365 °C and 60 T.

3.5.2 Ge on Strained Si

The SiGe pulse interface treatment can also be used in Ge on strained Si growth. Employing this technique will reduce Ge incubation time and surface roughness, and the application of this method can be utilized in fabricating strained Si/strained Ge heterostructures on insulator (HOI) to be used as a channel material in MOSFET architecture. Figure 3.15 plots the RMS roughness of Ge films versus the SiGe pulse treatment time for both Ge on relaxed bulk Si and strained Si, where strained Si can be grown on graded buffer (GBR) layer of 40% to 60% Ge. Sample structures are illustrated...
In this section, germanium on strained Si growth used a strained silicon layer on 50% graded buffer as a substrate.

The RMS value of Ge on strained Si is higher than Ge on bulk Si, because strained Si surface has intrinsic roughness from the underlying SiGe GRB layer. The reference points (RMS roughness of graded buffer) are marked in the plot. Figure 3.16 shows the AFM surface images of Ge on strained Si samples, and it is clear that the SiGe pulse method enables smooth, flat Ge epitaxy.

![Graph showing RMS roughness vs SiGe pulse treatment time]

Figure 3.15 RMS roughness is plotted for various pulse times for Ge epitaxy on relaxed Si substrate (red squares) or strained Si layer (green circles), showing that the RMS roughness decreases as the pulse time is increased. Strained Si was grown on 50% graded buffer. Surface roughness of 40% and 60% GRB are given as reference points. Ge thickness ranges from 8.2 nm to 12.0 nm. RMS roughness measured by 1 x 1 μm AFM scans. Strained Si samples were processed by L. Gomez.
Figure 3.16 AFM surface scans of Ge on strained Si layer with or without SiGe pulse treatment.
(a) Without SiGe pulse, RMS roughness is 2.83nm for 12 nm-thick Ge film. (b) With 10-sec SiGe pulse, surface roughness is significantly reduced. RMS roughness is 0.45 nm for 8.2 nm-thick Ge film. Same scale bar applies for both images. Strained Si was grown on top of 50% graded buffer. Ge-on-strained Si sample growth by L. Gomez.

The SiGe pulse method can be used to grow many device structures of interest.

Figure 3.17 shows a cross-sectional TEM image of an example structure of thin Ge film on strained Si for use in HOI structure. A 10 second SiGe pulse was utilized to growth 4.2 nm-thick, smooth Ge layer as shown in the figure.
Figure 3.17 A cross sectional transmission electron microscopy (XTEM) image of a strained Si/strained Ge heterostructure on insulator substrate. The SiGe pulse method was used to grow smooth, thin Ge layer on strained Si. Ge thickness is 4.2 nm. Sample was fabricated by L. Gomez

3.6 Summary and conclusions

In this chapter, the impact of growth parameters on thin, blanket Ge on Si is investigated. Ge films with thickness less than 60 nm were grown on Si substrates, and the growth curves were plotted to show the existence of a delayed growth time, or the “incubation time.” Incubation time as well as surface roughness is decreased with increasing temperature and pressure, to a certain point, and the optimized growth condition to yield flat Ge was chosen to be 365 °C and 60 torr.

The method of using a SiGe pulse surface treatment before Ge epitaxy can further reduce the growth delay period, and helps to realize thin, smooth Ge growth on Si surfaces. RMS surface roughness of 0.25 nm is measured for 3.4 nm-thick Ge-on-Si, and growth rate is 12 nm/min with incubation time less than 20 seconds. The reduction in incubation time improves Ge film thickness control and reproducibility as well as total growth time and thus throughput, and could be beneficial when utilized in a device process.
Chapter 4
Relaxed Ge-on-Si Selective Epitaxial Growth

This chapter discusses the study and optimization of the growth parameters for selective Ge-on-Si growth where the Ge film is thick and fully relaxed. Section 4.1 covers the Ge SEG test structure and fabrication. Section 4.2 evaluates Ge selectivity as a function of growth and processing conditions, and section 4.3 focuses on the faceting and surface morphology for Ge selective growth. Lastly, methods of improving film quality by reducing threading dislocation density are investigated in section 4.4.

4.1 Selective Ge-on-Si test structure

With applications for Ge photodiodes in mind, selective Ge-on-Si epitaxial growth experiments are designed to study germanium film quality and faceting. Figure 4.1 shows a schematic of the relaxed Ge test structure, where Ge is grown epitaxially in selective areas on oxide-patterned Si wafers. Starting with a p' doped six-inch Si wafer, a 1.0 \( \mu \)m-thick SiO\(_2\) film is deposited, and patterned using a combination of dry and wet etch processing. First, dry etching is used to ensure a vertical side-wall profile and removes all but the final 100 nm of oxide. Then wet etching by HF dipping is used to remove the remaining oxide. This eliminates issues associated with dry etch damage to the Si surface
prior to Ge epitaxial growth. This patterning step was done in collaboration with Lincoln Labs, and Nicole DeLello at MIT [104].

After patterning, the wafers were inspected under UV1280 spectroscopic ellipsometer to confirm that oxide is clear from the mask openings. Si surface was prepared with a standard RCA clean process with an additional 15 sec HF dip, DI water rinse, and spin-rinse dry step at the end, and Ge is epitaxially grown to a thickness of ~1 μm in an LPCVD growth system (Applied Materials Epi Centura™). A two-step process where deposition of a low-temperature Ge layer is followed by the deposition of a high-temperature Ge is utilized to obtain a smooth surface morphology. The low-temperature Ge deposition will suppress the tendency to form three-dimensional (3D) islands, and the high-temperature growth lowers the dislocation density and reduces overall deposition time [20, 105-108]. First, an approximately 60 nm-thick low-temperature Ge seed layer is grown, followed by a thick Ge “cap” layer deposited at higher temperature. For the material quality study, the wafers are cyclically annealed to reduce threading dislocations. In this chapter the annealing is performed in-situ immediately after epitaxial growth, but it is also possible to anneal the samples ex-situ.
Figure 4.1 Schematic of the relaxed Ge SEG test structures. SiO₂ sidewalls are 1 μm thick and patterned using a combination of dry and wet-etch process. A two-step process is used for Ge deposition; a thin Ge seed layer is grown at low temperature, followed by a thick Ge “cap” layer at higher temperature.

4.2 Germanium nucleation on the oxide field

For selective epitaxial growth, it is necessary to suppress germanium nucleation on the field oxide region of the mask pattern. The first set of Ge SEG experiments are designed to understand Ge selectivity as a function of growth parameters. Using oxide formed by low pressure chemical vapor deposition (LPCVD) as the field material, Ge films were epitaxially deposited using GeH₄ in a H₂ carrier gas with film thickness ranging from 0.8 μm to 1.3 μm. The presence of Ge nucleation on the oxide surface was verified with a Nomarski microscope at magnifications of 110-1100x, and nucleation density is visually counted. This Ge selectivity study was carried out in collaboration with Oluwamuyiwa Olubuyide [85].

Figure 4.2 (a) shows a typical Nomarski optical image of an SEG Ge sample with a high density of germanium nucleation on the field oxide. The method of counting nucleation density is illustrated in Figure 4.2 (b). Germanium nucleation is counted around square features with sizes 200 μm and 300 μm. In an optical microscope at a magnification of 440x, six to ten regions per sample are visually scanned to count field nuclei, and the nuclei number is divided by the area of observation (~0.008 cm² per region). This method gives a rough estimate as nucleation density varies by scanning
location. Depending on the location, nucleation density was observed to vary by up to a factor of 2, and with a typical observation of 8 counts per sample, the error bound is 8 to 10%. The statistics could be improved by scanning more regions per wafer.

![Nomarski optical image of SEG Ge-on-Si films with a high density of Germanium nucleation on the field oxide.](image)

**Figure 4.2** (a) Nomarski optical image of SEG Ge-on-Si films with a high density of Germanium nucleation on the field oxide. (b) Schematic of Ge field nucleation counting. The Ge nucleation was visually counted over an area of ~0.008 cm², using a Nomarski microscope. Ge-on-Si sample fabricated by O. Olubuyide.

Field nucleation density data is analyzed to understand the germanium selectivity as a function of growth conditions. Figure 4.3 (a) shows the effects of temperature and pressure on Ge nucleation. Under growth conditions with low temperature (600 °C) and pressure (15 torr), good selectivity is obtained, with Ge deposited only on the exposed Si surface and not on the oxide mask. However, when either the temperature or pressure is increased, Ge nucleates on the oxide field, possibly due to gas phase nucleation.
Growth temperature and pressure also changes the epitaxial growth rate, and Figure 4.3 (b) summarizes the experimental data. The growth rate is measured by step-height profilometer scans inside 300 μm square openings, and the average of five profilometer scans per sample is calculated and plotted in the graph. As the temperature and pressure decrease, the Ge growth rate also decrease.

Figure 4.3 (a) Nucleation density as a function of total chamber pressure and temperature. Lowering the temperature (red line) and pressure (blue line) reduces the nucleation density. (b) Ge growth rate as a function of total chamber pressure and temperature, determined by a step-height measurement. Reducing the temperature and pressure also reduces the film growth rate significantly. \( H_2 \) flow during growth was fixed at 25 slpm, and Ge film thickness is in the range of 0.8-1.3 μm. Ge-on-Si samples fabricated by O. Olubuyide.

Looking at both graphs in Figure 4.3, we can see that the reduction in the Ge nucleation density comes at the expense of lower Ge growth rate, and thus a compromise
may be needed when choosing the growth condition for Ge. If a Ge CMP step is included after growth, the Ge nucleation should not be an issue for device fabrication.

4.3 Effect of temperature and pressure on Ge faceting

The morphology of the Ge films, especially faceting, becomes an issue for selective Ge growth. Faceting is a fundamental concern in crystal growth; it depends on materials property, but it also depends on sample configurations and process conditions such as pressure, temperature, and reaction chemistry [109]. Faceting could be beneficial if controlled faceting is used to enhance device performance, but often it should be avoided as crystal facets can lead to locally non-uniform films and area loss. Thus it is important to understand and control Ge faceting, and several groups have reported that faceting behavior is influenced by growth parameters, such as temperature and pressure [100, 106, 110, 111].

For this section, because the Ge growth area is defined by oxide sidewalls, which may not be perfectly vertical, a good hole-filling behavior is desired for photodiode applications. Figure 4.4 (a) shows poor hole-filling behavior due to severe faceting. Such growth will make subsequent processing and planarization very difficult and should be avoided. For the germanium faceting study, a slightly different test structure from Figure 4.1 was developed. To fully investigate the faceting behavior of Ge, test wafers were prepared with a thin thermal SiO₂ field mask (thickness of 100 nm). This ensures “free”
growth of Ge, where the crystal is not confined by the oxide sidewalls and enables observation of the Ge facets more clearly. Figure 4 (b) shows a schematic of the test structure for faceting study.

![Figure 4.4](image_url)  
**Figure 4.4** (a) Cross-sectional SEM images of Ge Selective growth that shows severe faceting. (b) A schematic of Ge test structures to study the faceting behavior of Germanium. Thermal oxide is ~100 nm thick and patterned with a wet-etch process.

### 4.3.1 Growth temperature and Ge faceting

Previously, Talbot and Pribat reported that \{311\} facet formation in selective growth of Si is increased for higher temperature in H₂/HCl/SiH₂Cl₂ chemistry [109, 112]. This is because with the presence of Cl atoms in temperature range of 750 °C to 850 °C, the ratio of growth rates of crystal planes GR₃₁₁/GR₁₁₁ increases as the temperature increases. The \{111\} facet is dominant for lower temperature, and as the growth temperature increases, the \{311\} Si facet becomes dominant and the \{111\} facet is reduced in turn (Figure 4.5).
Figure 4.5 Cross-sectional SEM views of two Si SEG samples realized on nitride mask at high and low temperature: (a) 750 °C showing \{111\} facet and (b) 850 °C showing \{311\} facet. From Pribat et al., [109].

For the case of H₂/GeH₄ chemistry as utilized in this chapter, selective growth of Ge shows the opposite behavior from the case of Si. Keeping the chamber pressure constant at 10T, the Ge growth temperature was varied. Table 4.1 summarizes the growth conditions of test samples.

Table 4.1 List of Ge-on-Si samples for the temperature study (Figure 4.6)

<table>
<thead>
<tr>
<th>Sample</th>
<th>Temperature (°C)</th>
<th>Pressure (torr)</th>
<th>GeH₄ flow (sccm)</th>
<th>H₂ flow (slpm)</th>
<th>GeH₄ partial pressure (mT)</th>
<th>Ge growth rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A (#4854)</td>
<td>600</td>
<td>10</td>
<td>33</td>
<td>30</td>
<td>3.65</td>
<td>11</td>
</tr>
<tr>
<td>B (#4855)</td>
<td>650</td>
<td>10</td>
<td>33</td>
<td>30</td>
<td>3.65</td>
<td>14.5</td>
</tr>
<tr>
<td>C (#4870)</td>
<td>700</td>
<td>10</td>
<td>33</td>
<td>30</td>
<td>3.65</td>
<td>26.6</td>
</tr>
<tr>
<td>D (#4869)</td>
<td>750</td>
<td>10</td>
<td>33</td>
<td>30</td>
<td>3.65</td>
<td>53.2</td>
</tr>
</tbody>
</table>
Figure 4.6 shows cross-sectional SEM images of selective germanium growth, and the \{311\} facet is reduced as temperature is increased. At 600 °C the \{311\} facet is very clear, but \{111\} facet develops for growth temperature of 650 °C indicating that GR\textsubscript{111}/GR\textsubscript{311} is comparable at that temperature. For temperatures higher than 700 °C, no dominant crystal facet is found and the Ge edge shows a rounded profile.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure4.6}
\caption{Cross-sectional SEM images of Ge-on-Si growth at (a) 600 °C, (b) 650 °C, (c) 700 °C, and (d) 750 °C, showing the reduction of Ge \{311\} formation as the growth temperature is increased. The scale bar applies to all micrographs in the figure. Chamber pressure is set at 10 torr. Detailed growth conditions can be found in Table 4.1.}
\end{figure}

One explanation for the high temperature growth can be found from looking at the diffusion length of Ge adatoms during film deposition. The adatom diffusion distance, $\delta_{de}$, is given by:
\[ \delta_{de} = \sqrt{D_{SD} \tau} \]  

(4.1)

where \( D_{SD} \) is the surface diffusivity and \( \tau \) is the average time an adatom spends on the surface before it desorbs. The units of \( D_{SD} \) are length\(^2\)/time, and diffusivity is an exponential function of temperature:

\[ D_{SD} = D_0 e^{\frac{E_a}{kT}} \]  

(4.2)

where \( D_0 \) is the diffusion coefficient at infinite temperature, \( E_a \) is the activation energy, \( k \) is Boltzmann’s constant, \( 8.617 \times 10^{-5} \text{ eV/K} \), and \( T \) is temperature in Kelvin. In this Arrhenius equation, increasing the growth temperature increases \( \delta_{de} \), the diffusion distance.

As shown schematically in Figure 4.7, Ge adatoms on the SiO\(_2\) surface have a small diffusion length at a low temperature, and will be desorbed into the CVD chamber before traveling a distance sufficient to reach the adsorption site on the Ge film. When the temperature is increased, however, the Ge adatom diffusivity is also increased and more adatoms are deposited on the side of the Ge film. Once the number of germanium adatoms arriving to film edge exceeds the number of available atomic sites on the ledge of the crystalline plane, Ge atoms will be incorporated onto a non-crystalline plane and will reduce the facet.
Figure 4.7 A schematic of Ge adatom diffusion and its impact on faceting. (a) At a low temperature, Ge adatoms do not have sufficient mobility to attach to the Ge film before desorption into the CVD chamber. (b) When the temperature is increased, Ge adatom can diffuse across the SiO₂ mask and attach itself on the side of the Ge film.

4.3.2 GeH₄ partial pressure and Ge faceting

Because Ge diffusion plays an important roll in the lateral growth of Ge films, increasing the germane (GeH₄) partial pressure can further enhance the lateral growth of the Ge film and thus improve the hole-filling behavior. Figure 4.8 shows the results on the effect of germane partial pressure on the Ge lateral growth over the oxide. Keeping the chamber pressure constant at 10 T and temperature at 650 °C, the GeH₄ partial pressure was increased from 10.9 mTorr to 54.1 mTorr by keeping germane flow at 100 sccm but decreasing the H₂ carrier gas flow from 30 slpm to 6 slpm. Table 4.2 lists the growth conditions for test samples.

Table 4.2 List of Ge-on-Si samples for the GeH₄ partial pressure study (Figure 4.8)

<table>
<thead>
<tr>
<th>Sample</th>
<th>Temperature (°C)</th>
<th>Pressure (torr)</th>
<th>GeH₄ flow (sccm)</th>
<th>H₂ flow (slpm)</th>
<th>GeH₄ partial pressure (mT)</th>
<th>Ge growth rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A (#4856)</td>
<td>650</td>
<td>10</td>
<td>100</td>
<td>30</td>
<td>10.9</td>
<td>49.7</td>
</tr>
</tbody>
</table>
While the Ge growth was almost entirely confined inside of the oxide opening at the low germane partial pressure, as the partial pressure was increased, the Ge film shows increased lateral growth. This is beneficial in improving the hole-filling behavior for Ge SEG growth. Figure 4.9 shows Ge film growth rate as a function of GeH₄ partial pressure. As GeH₄ partial pressure is increased, the growth rate increases linearly because at high temperatures, the growth is limited by mass flow rate, which is proportional to source partial pressure.
Figure 4.8 Cross-sectional SEM images of Ge-on-Si SEG growth at GeH₄ partial pressures of (a) 10.9 mTorr, (b) 16.5 mTorr, (c) 21.8 mTorr, and (d) 54.1 mTorr, showing the increase in the lateral growth of Ge films as the GeH₄ partial pressure is increased. Growth temperature is 650 °C, total pressure is 10 Torr, GeH₄ flow is 100 sccm, and H₂ flow was varied to achieve different GeH₄ partial pressures.

Figure 4.9 Ge film growth rate as a function of GeH₄ partial pressure. As GeH₄ partial pressure is increased, the growth rate increase linearly. The chamber pressure was set at 10 Torr for all temperatures and GeH₄ partial pressures.

Increasing germane flow improves the hole-filling behavior, but there is a limit in increasing GeH₄ partial pressure via GeH₄ flow since the maximum flow rate was 100 sccm for the installed reactor hardware. Low hydrogen gas flow (6 slpm) is needed to achieve the highest germane partial pressure (54 mTorr), and as gas flow rate is inversely proportional to the gas residence time in the reaction chamber, very low H₂ flow will result in a large gas residence time and is not desirable in an LPCVD system [113]. At a very low H₂ flow, there can be deposits on the wall of the quarts reaction chamber
causing contamination issues with the following runs. For the relaxed Ge SEG structure, the optimized growth condition is determined to be 750 °C and 10 T, with 100 sccm of germane flow and 10 slpm H₂ carrier gas flow. This growth parameter improves the hole-filling behavior compared to the un-optimized growth conditions, as seen in Figure 4.10.

**Figure 4.10** Cross-sectional and plan-view SEM pictures of non-optimized and optimized selective Ge growth. The following growth parameters are used: (a) for the non-optimized growth, 650 °C, 10 T, 33 sccms of GeH₄ flow, and 30 slpm of H₂ flow. (b) for the optimized growth, 750 °C, 10 T, 100 sccms of GeH₄ flow, and 10 slpm of H₂ flow. Optimized growth condition for reducing faceting improves the hole-filling behavior and also the growth uniformity of thin lines.

### 4.3.3 Surface roughness and growth uniformity

In this section, the impact of growth parameters on surface morphology and germanium film quality is studied. Atomic force microscopy (AFM) is used to study the
surface roughness of Ge films after growth under varying temperature and pressure. Figure 4.11 summarizes the results.

Figure 4.11 Effect of growth temperature and germane partial pressure on RMS surface roughness of Ge films. Images are from 1 x 1 µm AFM scans of ~1 µm thick Ge films grown in 1 mm square openings. Chamber pressure was constant at 10 Torr. For the condition that yielded the best hole filling behavior, the RMS surface roughness is 1.32 nm which is believed to be acceptable for photodiode applications. The scale bar and crystallographic direction applies to all images in the figure.

In the previous section, higher growth temperature was preferred because it reduces the faceting behavior of germanium growth. However, care should be taken since as temperature increases, so does the surface roughness. Surface diffusivity is the reason for this trend as well. In epitaxial growth, the Ge adatoms are most likely incorporated when they travel to an adsorption site such as a terrace, kink, or ledge site, or when they collide
with another adatom and form a new growing surface [114, 115]. At a low temperature, germanium adatom diffusion distance, $\delta_{de}$, is short, and most of the Ge incorporation takes place at the terrace or ledge sites and smooth film forms. However, when the temperature is high, $\delta_{de}$ is increased, and new growth surface forms more readily as schematically shown in figure 4.12. From the AFM data, it can be seen that the RMS roughness increased by a factor of 2 when the growth temperature was increased from 650 °C to 750 °C.

(a) Low Temperature

(b) High Temperature

*Figure 4.12* A schematic of Ge adatom diffusion and its impact on germanium surface roughness. (a) At a low temperature, Ge-Ge collision rate is small and most adatoms attach to adsorption sites such as terraces or ledges. (b) When the temperature is increased, Ge adatoms can diffuse further before desorption into the CVD chamber. Adatoms can collide with each other to form a new atomic layer, increasing the surface roughness of epitaxial film.

Increasing GeH$_4$ partial pressure does not make the film rough, but it increases the loading effect and reduces the growth uniformity across the wafer. One 300 x 300 µm square mesa is selected in each die and germanium thickness was measured across the
wafer. Figure 4.13 shows the result; the growth is more uniform for the 650 °C, 10.9 mTorr GeH₄ growth, with a thickness variation of 5.4%. For 750 °C, 21.8 mTorr GeH₄ growth, there is more loading effect and thickness variation across the wafer is as high as 12%.

![Graph showing Ge film thickness across the wafer.](image)

**Figure 4.13** Selective Ge film thickness across a wafer. One 300 x 300 μm square mesa was selected in each die and the same feature was used to measure Ge thickness across the wafer. Step-height measurement was used to acquire the film thickness.

### 4.4 Threading dislocation density of relaxed Ge films

Another material quality of interest is the threading dislocation density (TDD) of the germanium films, because higher threading dislocation density degrades device performance. Several methods to reduce TDD in Ge-on-Si growth are examined in this section.
4.4.1 Cyclic annealing

Annealing Ge films in H\textsubscript{2} atmosphere after epitaxial growth has several benefits. First, annealing can reduce Ge surface roughness. For Ge growth at 750 °C and 10 T (run number #4900), the RMS roughness is reduced from 1.32 nm to 0.86 nm after annealing the wafer 4 times between 800 °C for 150 s and 450 °C for 90 s.

Cyclically annealing Ge films has another benefit; it is an effective way of reducing dislocation density, as discussed in Chapter 2. During cyclic annealing, the wafers undergo rapid temperature change and this thermal stress induces threading dislocations to glide and annihilate. In this section, plan-view TEM imaging was used to investigate the effect of annealing conditions on threading dislocation density. After Ge epitaxy, the wafers are annealed in-situ in the epitaxial growth reactor with a H\textsubscript{2} flow of 30 slpm and the chamber pressure at 30T. Different numbers of thermal cycles between 800 °C for 150 s and 450 °C for 90 s are used, and the sample was cleaved and prepared using standard TEM procedure. Detailed TEM sample preparation steps and imaging condition can be found in appendix A.

Figure 4.14 shows TEM images of samples from the annealing study, with ~0.7 μm of Ge grown on Si in large areas (~2 mm square) on oxide-patterned Si wafers. Figure 4.14 (a) shows an as-grown sample, (b) shows the sample that was subjected to 2 cyclic anneals with maximum temperature of 800 °C for 150 s and minimum temperature of 450 °C for 90 s, and (c) is treated with 4 cycles of anneals with maximum temperature of
800 °C for 150 s and minimum temperature of 450 °C for 90 s. Threading dislocation density is reduced from $10 \times 10^8 \text{ cm}^{-2}$ for the as grown sample to $1.2 \times 10^8 \text{ cm}^{-2}$ for x4 cyclic annealed sample. This is a reduction by a factor of $\sim 8x$, and it shows the effectiveness of cyclic annealing to reduce the TDD in relaxed Ge growth. Increased number of annealing cycles and treating time will further reduce the dislocation density, but will increase the total processing time. This result agrees with a previous report by Luan, [20], that reported a reduction of 18x after cyclic thermal annealing of 10 cycles between 900 °C/10 min and 100 °C/10 min.

Figure 4.14 Plan-view TEM images of ~0.7 μm thick Ge-on-Si, (a) as-grown, (b) x2 cyclic annealed, and (c) x4 cyclic annealed between 800 and 450°C, for 150 and 90 sec, respectively. Threading dislocation density (TDD) is (a) $10 \times 10^8 \text{ cm}^{-2}$, (b) $4 \times 10^8 \text{ cm}^{-2}$, and (c) $1.2 \times 10^8 \text{ cm}^{-2}$, with error bound of 12%. Growth parameters are: 750 °C, 10 Torr, 100 sccm of GeH₄ flow, and 10 slpm of H₂ flow. Bright-field two-beam images with $g = 2\overline{2}0$. Thickness of viewing area is 0.4~0.6 μm. The scale bar applies to all images in the figure.

4.4.2 Film thickness and threading dislocation density
Care should be taken when comparing the threading dislocation densities of Ge-on-Si samples with different thicknesses, because the Ge thickness impacts the threading dislocation in the film. Figure 4.15 demonstrates this effect. Three samples were grown at the same condition but with different growth times and thicknesses. After growth, all wafers were subjected to 4 cyclic anneals between 800°C/150s and 450°C/90s, and analyzed using plan-view TEM imaging.

As the thickness decreases, there is a significant increase in the threading dislocation density. This could be due to the high defect density at the Si/Ge interface, as well as the change in the driving force for dislocation movement. During the growth and annealing, threading arms of misfit dislocations propagate, often terminating at the edge of the sample or combining with another threading arm to reduce the overall threading dislocation density. This movement is driven by the stress in the film which is inversely proportional to the film thickness [19, 20, 84]. For a thin Ge film, there might not be enough stress to effectively move the threading arms, which would explain the observed phenomenon. Figure 4.15 and 4.16 summarize the effect of annealing and Ge film thickness on threading dislocation density. For Figure 4.15, Ge-on-Si samples are grown at varying thicknesses, and are treated with 4 cycles of 800/450°C annealing. Threading dislocation density is very high (1.68 x 10⁹ cm⁻²) when the film thickness is 0.2 μm. As the film thickness is increased, there is a significant reduction in TDD, and the dislocation density is 2.5 x 10⁸ cm⁻² at Ge thickness 0.5 μm and 1.22 x 10⁸ cm⁻² for 0.7 μm-thick layer. Figure 4.16 compares the threading dislocation density of Ge-on-Si films grown at different thickness and annealing conditions. At Ge thickness of 1.7 μm and 8x
cyclic anneal, TDD of $1.3 \times 10^7$ cm$^{-2}$ is obtained for growth in large areas. This agrees with a previous report by Olubuyide[85], with TDD of $2 \times 10^7$ cm$^{-2}$ in large areas.

**Figure 4.15** Plan-view TEM images showing the change in threading dislocation density with Ge film thickness. (a) film thickness 0.2 μm, TDD $1.68 \times 10^9$ cm$^{-2}$ (b) film thickness 0.5 μm, TDD $2.5 \times 10^8$ cm$^{-2}$, (c) film thickness 0.7 μm, TDD $1.2 \times 10^8$ cm$^{-2}$. The films are grown at 750 °C and 10T on a blanket Si substrate without any oxide on the wafer surface. After the growth, samples were treated with x4 cycles of annealing between 800/450 °C. Bright-field two-beam images with $g=220$. Thickness of viewing area is 0.4–0.6 μm. The scale bar applies to all images in the figure.
Figure 4.16 Effect of Ge film thickness and annealing on threading dislocation density (TDD) for blanket Ge epitaxial growth on silicon. Sample thickness is measured by cross-sectional SEM and TEM, and threading dislocation density is calculated from plan-view TEM images. Error bound for dislocation density is 12%.

4.4.3 Selective growth in small areas

Selective Ge-on-Si growth in limited area combined with thermal annealing can be an effective tool to reduce threading dislocation density in the film. Growth in small area is beneficial because during the growth and annealing, threading arms of misfit dislocations glide and terminate at the edge of the growth area. Selective growth in small area reduces the distance a threading arm needs to propagate before annihilating at the film edge, and it reduces the overall threading dislocation density. There is also an added benefit called aspect ratio trapping (ART), which occurs when the Ge film width is comparable to the layer thickness. Because Ge-on-Si heteroepitaxy has a diamond cubic crystal slip system, misfit dislocation half-plane lies along the <110> direction at the Si-Ge interface, and the threading arm climbs up on (111) planes, making a 45 degree angle from the Si (100) substrate. When the SEG feature has width comparable to the film height, the threading arms are “trapped” and terminate at the sidewall [86, 87].

In this thesis the reduction of threading dislocation density in selective Ge-on-Si for feature sizes less than 5µm has been investigated using cross-sectional and plan-view TEM imaging. These samples were grown in collaboration with Lincoln Labs, and Nicole DeLello at MIT [104]. The results show that TDD decreases rapidly as the width of the
grown region becomes smaller, and the trend of decreasing dislocation density with feature size applies for both as-grown and annealed Ge films (Fig. 4.17-4.19).

**Figure 4.17:** Plan-view TEM images of ~0.8 μm thick Ge structures, selectively deposited in Si openings with different widths as indicated. Ge films are as-grown, without any thermal annealing after growth. Threading dislocation density is $5.5 \times 10^8$ cm$^{-2}$ for 5 μm-wide feature, $2.6 \times 10^8$ cm$^{-2}$ for 1 μm-wide feature, and $1.7 \times 10^8$ cm$^{-2}$ for 0.65 μm-wide line. Bright-field two-beam images with $g = 220$. Thickness of viewing area is 0.4–0.6 μm Growth parameters: 750 °C, 10 torr, 100 sccm of GeH$_4$ flow, 10 slpm of H$_2$ flow.
Figure 4.18 Cross-sectional TEM images of ~0.6 \( \mu \)m thick, annealed Ge structures, selectively deposited in Si openings with different widths as indicated. Threading dislocation density is significantly reduced for smaller growth areas. For SEG width of 0.25 \( \mu \)m, no threading dislocation at the surface was found after examining 20 sites. Growth parameters: 750 °C, 10 torr, 100 sccm of GeH\(_4\) flow, and 10 slpm of H\(_2\) flow, and 4x cycles of annealing between 800/430 °C. Bright-field two-beam images with \( g = \bar{2}20 \).

![Figure 4.18 Cross-sectional TEM images](image)

Figure 4.19 Threading dislocation density as a function of SEG feature width for as-grown (blue squares) and 4-times cyclic annealed (red circles) Ge-on-Si films. Cross-sectional TEM images were used to analyze TDD values, and the error bound is ~12%. Ge thickness is 0.8 \( \mu \)m for as-grown and 0.6 \( \mu \)m for annealed samples.

4.5 Summary and conclusions

In this chapter, the impact of growth parameters on Ge SEG was investigated. Approximately 1 \( \mu \)m-thick, relaxed Ge was grown on oxide-patterned Si substrates, and the selectivity of Ge was studied as a function of the temperature, pressure, and growth rate. Reduction of \{311\} facets was achieved by increasing the growth temperature and
germane partial pressure, and at the growth condition which minimized faceting (750°C and 10T), an RMS surface roughness of 1.3 nm was obtained for as-grown samples, measured by 10 x 10 μm AFM scans.

Threading dislocation density of relaxed Ge film depends on post-growth annealing conditions and Ge film thickness. Aspect ratio trapping (ART) was observed and TDD was reduced for structures smaller than 5 μm, and for features less than 0.5 μm, no treading arm was observed to reach the Ge surface under cross-sectional TEM examination.

Further improvements in Ge-on-Si material quality are expected to be obtained by optimizing the post-Ge-growth annealing conditions as well as pre-epi Si surface preparation.
Chapter 5
Selective Growth of Thin, Strained, High Ge-content SiGe-on-Si

5.1 Introduction

This chapter investigates an approach to increase the SiGe critical thickness without having to grow a graded buffer layer to reduce the lattice mismatch. SiGe film is grown in small areas using Selective Epitaxial Growth (SEG), and the critical thickness of SiGe on exposed Si regions on oxide-patterned Si wafers was studied. The goal is to provide a way to grow thicker SiGe-on-Si films without strain relaxation, and make it possible to realize a high-quality SiGe channel material in MOSFET applications.

Thin, strained SiGe-on-Si growth is investigated with a focus on SiGe films with high Ge concentration (>65%) grown in limited areas, where pattern sizes span sub-micron to a few tens of microns. Section 5.2 reviews the process flow used to fabricate the SiGe-on-Si SEG structures. The loading effect in selective growth is studied in section 5.3, and section 5.4 analyzes the misfit dislocation (MD) spacing as a function of film thickness using plan-view transmission electron microscopy. The sources of misfit dislocation generation are discussed, and heterogeneous MD nucleation near SEG pattern edges is investigated in section 5.5.
5.2 Test structures and fabrication process

5.2.1 Wafer structure and SEG mask

In order to grow the epitaxial SiGe films in selective areas on oxide-patterned Si wafers, the following steps were taken. Starting with a p+ doped six-inch (100) Si wafer, a SiO$_2$ film with thickness ranging from 40 nm to 70 nm was grown using thermal oxidation, followed by patterning using standard lithography and wet etching in BOE/HF solution. After patterning, a KLA Instruments UV1280 spectroscopic ellipsometer was used to ensure the Si openings are clear from field oxide, and samples were examined under scanning electron microscopy (SEM) to check for any patterning abnormality. After the pre-epitaxial Si surface preparation, which includes standard RCA clean with an additional HF dip, DI water rinse, and spin-rinse dry steps, the wafers are loaded into an Applied Materials Epi Centura™ Low Pressure Chemical Vapor Deposition (LPCVD) growth system. A hydrogen prebake temperature of 900 °C and duration of 5 minutes is used, and SiGe with a nominal concentration of 70% Ge was epitaxially grown to varying thicknesses up to 25 nm. Using SiH$_4$ and GeH$_4$ as precursors, the SiGe growth temperature was kept at 450°C and chamber pressure at 100 torr during growth. SiH$_4$ gas flow was set at 10 sccm, and GeH$_4$ gas flow was kept at 28 sccm. Blanket SiGe films of comparable thicknesses were also grown under the same conditions to be used as control.
samples for comparison. Figure 5.1 shows a schematic and cross-sectional TEM image of the SiGe-on-Si SEG test structure.

(a) (b)

Figure 5.1 (a) A schematic of SiGe-on-Si SEG test structure. (b) A typical cross-sectional transmission electron microscope image of SEG samples. Oxide thickness is 40 nm, and the SiGe film is around 10 nm-thick. The growth temperature is 450 °C and pressure is 100 torr. Hydrogen prebake of 900 °C for 5 min is used.

A mask was designed to systematically study the changes in critical thickness of SiGe in small areas. Figure 5.2 shows the mask layout used in the SEG study. The mask is grouped into 3 x 3 mm grids, and each grid contains densely packed, same-sized features suitable for TEM study. The size of oxide openings ranges from 0.8 µm to 50 µm, and this work focused on features with size less than 10 µm. Various shapes are also included, such as squares, rectangles, diamonds, circles, and star-burst patterns.

From the previous study of selective growth of Ge-on-Si, it was noticed that the germanium growth rate is dependent on the ratio between growth area and surrounding mask field area. The less dense the exposed silicon areas are, the faster is the Ge growth,
because more Ge atoms are available for growth from the gas associated with the surrounding field oxide regions. Because of this, the density of oxide openings was kept roughly the same for all shapes and sizes on the mask, to minimize the loading effects during epitaxial growth. Approximately 20% of the wafer surface is exposed silicon, and the remaining 80% is covered by the oxide field.

Figure 5.2 Mask layout for the SEG study. The mask is grouped into 3 x 3 mm grids, and each grid contains densely packed, same-sized features suitable for TEM study. The size of oxide openings ranges from 0.8 μm to 50 μm.

5.2.2 Prebake condition

During sample preparation, special care should be taken at two stages. First is the hydrogen prebake, which is a high-temperature, in-situ hydrogen anneal that is required to remove oxide from the exposed Si surface. Prebake utilizes a reaction that is the opposite of thermal oxidation:
The prebake step is necessary because any bare silicon surface exposed to air will form a layer of 1 to 2 nm-thick native oxide. Chemical oxide of similar thickness can also form as a part of pre-epi cleaning process such as in RCA [103]. To remove this any oxide on Si surface, a prebake is needed to ensure high quality epitaxial growth. Conventional hydrogen prebake used for epitaxial growth on unpatterned wafers generally benefits from a temperature above 1000 °C [116], and for blanket epitaxy, standard prebake step of 1080 °C for 30 seconds is often used.

Selective epitaxial growth introduces a problem of undercut forming along the substrate interface to the mask oxide during the H₂ bake. An example of SiGe SEG structure with severe oxide undercut by high-temperature prebake is shown in Figure 5.3. Due to the oxide undercut, SiGe growth occurs underneath the oxide mask, and this is very undesirable because the stress at the SiGe film edge is not controlled and can affect the misfit dislocation formation.
Using a lower temperature during the prebake process decreases the undercut, but with the reduction in temperature, the oxide removal process becomes more sensitive to background impurities on the wafer surface and inside the reactor, such as O₂ and H₂O. Previous studies report that gaseous H₂O can both oxidize and etch silicon, and the maximum background H₂O pressure allowed inside a reactor to maintain oxide-free silicon surface is highly temperature dependent [103, 116]. Because of this, incomplete removal of oxide can become an issue if the temperature is kept too low during the hydrogen prebake.
To determine the necessary prebake temperature, SiGe-on-Si samples with different prebake temperatures were compared, and it was found that the film quality and surface roughness were deteriorated for prebake temperatures lower than 850 °C. For the remainder of this chapter, the prebake condition for SEG samples was set to 900 °C and 5 minutes. This condition minimizes oxide undercutting while allowing native oxide to be removed from the Si surface.

5.2.3 Oxide patterning by wet etching

Another processing step to pay attention to is the etching of the oxide field. Etching in buffered oxide etch (BOE) solution should be avoided because BOE oxidizes and etches the Si substrate, causing the Si surface to “dish-in” as illustrated in Figure 5.4. BOE (5 parts NH4F + 1 part HF) etching of SiO2 is also very fast with an etch rate of 100 nm/min. [117], and because the thermal oxide mask of SEG samples is only 40 nm to 70 nm-thick, such fast etching makes it difficult to control the process. Substantial over-etching is very likely when extra time is allocated to ensure that all the oxide is removed from the mask openings. Figure 5.4 (a) shows a cross-sectional TEM image of a SiGe SEG sample, patterned in BOE. The Si surface shows a severe “dished-in” profile, and the Si surface is recessed in the open windows. This is not desired because the Si surface curvature is uncontrolled, and misfit dislocations can be generated from the curved SiGe film edge, as will be discussed in section 5.5.
A solution of 50:1 diluted HF is gentler on the Si surface, but the long etching time due to a slow etching rate (5 nm/min.) can cause the photoresist mask to peel off during the etching process. As a result, a two-step etching was utilized where most of the oxide was etched with BOE first, than the remaining oxide was removed in diluted HF solution. Visual check of wafer surface changing from hydrophilic into hydrophobic is used to tell when all SiO₂ has been etched in the open areas. After rinsing in DI and spin-drying, the wafers were examined under UV1280 ellipsometer to make sure all oxide is removed from the mask openings. Figure 5.4 (b) shows a TEM image of the SiGe-on-Si SEG sample fabricated by a combination of BOE/HF etching. The profile shows a flatter Si surface without significant overetching.

Figure 5.4 Cross-sectional TEM images of Si₉₃Ge₆₇ SEG samples patterned using different wet etch chemistry. (a) When the oxide is patterned in BOE, the solution etches Si and causes the exposed Si surface to “dish-in.” (b) Si surface is much flatter when BOE is used to etch most of the oxide, followed by 50:1 HF etch to remove the remaining oxide. SiGe thickness is 12.1 nm for sample (a) and 10.6 nm for sample (b). Prebake condition at 900 °C for 5 minutes, and SiGe growth is at 450 °C and 100 torr.
5.3 Auger study: Ge compositional analysis and loading effect

To measure the critical thickness of SiGe films and compare the value to the equilibrium thickness, it is necessary to know the Ge concentration in the film. First, germanium composition in large growth area was calibrated, followed by determination of the Ge concentration in smaller SEG areas and comparison to that in the larger area.

After SiGe growth, germanium concentration in the SiGe film was primarily measured by the UV1280 spectroscopic ellipsometer. This method gives a quick but rough estimate, yielding a Ge composition in the range of 62 % to 69 % based on the best-fit approximation of the spectral curve. To obtain a more accurate measurement of Ge content, a blanket SiGe-on-Si sample was analyzed by Secondary Ion Mass Spectrometry (SIMS). The result shows that the SiGe film contains 67 % germanium and 33 % silicon, excluding the signal from the top 5 nm of the SiGe film which is subject to artifacts from the measurement and to surface contaminants.

Loading effect, or a difference in the growth rate of selective epitaxy from blanket growth, is another concern for selective epitaxy. There are two aspects to the loading effect: SiGe layers on patterned substrates may have different growth rate, or different Ge contents than for blanket growth [118-121]. Either behavior is undesirable, because the variation in SiGe film thickness or germanium composition will make a comparison of
critical thickness very hard, if not impossible. In this section, it is verified that for the growth conditions employed, no significant loading effect took place for SEG features with sizes spanning 1 μm to 10 μm.

In order to determine whether the Ge composition in the SiGe film depends on the size of the SiGe growth area, Auger electron spectroscopy was used to compare the Ge contents in SiGe features of different sizes. 11 nm-thick SiGe films grown in 1.3 and 10.3 μm square-shaped oxide openings were analyzed and compared to the data for blanket films. The Ge concentration in all samples fell within a few atomic percent of that measured for blanket SiGe growth. As the accuracy of the Auger technique is also a few atomic percent, it can be suggested that the Ge concentration for the SEG SiGe films in this study does not vary with the size of the features. Figure 5.5 shows the atomic concentration of Ge across selective features with different sizes. Ge concentration of 67 % as measured by SIMS is also plotted. Si concentration is plotted as well, and the composition does not vary significantly as SEG size changes. Because this Auger analysis was performed at the sample surface, oxygen and carbon atoms from the atmosphere and surface oxidation are also detected, and the sum of germanium and silicon atomic percentage is less than 100 at. %.
Figure 5.5 Atomic concentration of Ge (blue squares) and Si (open triangles) as measured by Auger electron spectroscopy conducted at the surface of SiGe-on-Si SEG samples. There is no significant variation of Ge composition over different SEG feature size. SIMS measurement is also taken for a blanket sample, and Ge concentration was verified to be 67%. For the Auger measurement at the surface, the sum of Ge and Si composition is less than 100% because oxygen and carbon atoms are also detected due to the surface oxidation and carbon from the atmosphere.

To check the SiGe film thickness variation for different SEG feature sizes, a sample with SiGe-on-Si selective epitaxy (SiGe film thickness around 11 nm) was used for compositional profiling by Auger spectroscopy combined with sputtering by an ion source. The operating condition for electron beam was the following: acceleration voltage 10 kV, current 10 nA, and a beam size 0.5 x 0.5 μm. In between Auger measurements, a 30 second exposure to the ion beam was used for sample sputtering. Assuming the sputtering rate is the same for SiGe film and Si substrate, sputter rate was 1.4 nm/min. and sputter time can be converted into depth from the surface.
Figure 5.6 shows the Auger peak intensity as a function of sputter time for the SiGe films selectively grown in square-shaped oxide openings with sizes 1.3, 3.3, and 10.3 μm. The profile is almost identical for all three sizes, and this shows the thickness and Ge composition of SiGe SEG films are comparable for features less than 10 μm. The profile is not abrupt at the SiGe/Si interface because the sputtering by ion beam does not leave a flat surface. Rather, ion beam results in a "crater," and the curvature of sputtered surface may be a reason for the gradual drop in Ge concentration at the SiGe/Si interface.

![Graph showing Auger peak intensity as a function of sputter time for different SEG feature sizes.](image)

**Figure 5.6** Auger peak intensity as a function of sputter time for different SEG feature sizes. The plots are almost identical for SEG sizes less than 10 μm, showing that there is no significant loading effect in the SEG wafers.

### 5.4 Increased critical thickness by selective growth

#### 5.4.1 Measurement of SiGe thickness and misfit dislocation spacing
The thickness and dislocation spacing of Si$_{0.33}$Ge$_{0.67}$ films was measured by transmission-electron-microscopy (TEM) techniques, using both plan-view and cross-sectional analysis. A standard sample preparation method by grinding and ion milling was utilized as described in Appendix A. Cross-sectional TEM is used to measure the sample thickness, and from the TEM images, it is observed that the SiGe film is slightly thicker within 100 nm of the oxide boundary compared to the thickness in the rest of the open area (See Figure 5.1 (b)). SiGe film thickness quoted in this chapter refers to that in the bulk of the film.

Plan-view TEM images are used to determine the misfit dislocation spacing. For blanket samples, typically 5 to 7 TEM images with observation window of approximately 4 x 6 μm per image was taken. Misfit dislocations were manually counted across randomly-placed lines along <110> directions on the image. The dislocation count is divided by the line length to give dislocation density (#dislocation/μm), or the number is inverted to give dislocation spacing (μm/dislocation). Detailed methodology is found in Appendix B. It should be noted that the dislocation spacing and density are inversely proportional; for a sample with few misfits, the dislocation spacing is large, and dislocation density is small. For a heavily-dislocated sample, dislocation spacing is small, and density is large.

For SEG samples of feature size smaller than 10 μm, the area of observation is limited by the SiGe growth area. Greater numbers of TEM images are needed to obtain a statistically meaningful result, and for SEG features of size 1.3 μm, a minimum of 20 to
25 sites are analyzed. Table 5.1 summarizes the number of observation sites and total area of observation for the SEG and blanket samples.

Table 5.1: typical number of observation sites and total area of observation by SEG feature size (for uniformly distributed and densely spaced misfit dislocation network)

<table>
<thead>
<tr>
<th>Feature size (square width)</th>
<th>number of observation sites</th>
<th>SiGe film area per site (at ×5k magnification)</th>
<th>total area of observation</th>
</tr>
</thead>
<tbody>
<tr>
<td>blanket</td>
<td>5 – 7</td>
<td>6 × 4 μm²</td>
<td>120 – 160 μm²</td>
</tr>
<tr>
<td>10.3 μm</td>
<td>5 – 7</td>
<td>6 × 4 μm²</td>
<td>120 – 160 μm²</td>
</tr>
<tr>
<td>5.3 μm</td>
<td>7 – 10</td>
<td>5.3 × 4 μm²</td>
<td>148 – 200 μm²</td>
</tr>
<tr>
<td>3.3 μm</td>
<td>10 – 12</td>
<td>3.3 × 3.3 μm²</td>
<td>100 – 120 μm²</td>
</tr>
<tr>
<td>2.3 μm</td>
<td>15 – 20</td>
<td>2.3 × 2.3 μm²</td>
<td>80 – 100 μm²</td>
</tr>
<tr>
<td>1.3 μm</td>
<td>20 – 25</td>
<td>1.3 × 1.3 μm²</td>
<td>33 – 42 μm²</td>
</tr>
</tbody>
</table>

The above number of observation sites is used when the density of misfit dislocations is fairly high and uniformly distributed across the sample. When dislocation density is high (dislocation spacing is small), observation areas taken at random will have similar number of dislocation counts. In such case, sampling error in dislocation measurement is 10 to 13%, depending on the sample size and data distribution. Detailed analysis can be found in Appendix B.

However, when dislocations are sparsely scattered or when SEG feature size is comparable to dislocation spacing, sampling error is much bigger because there will be a
large variation of dislocation counts depending on the observation location. A larger
number of observation sites is necessary for samples with low dislocation density, and in
such cases, approximately 30 sites were observed to obtain statistically meaningful data.
Appendix B has an example of a SiGe SEG sample, where the average dislocation
spacing is larger than the SEG feature size. When 30 features are analyzed, sampling
error is as high as 24.6%, and care should be taken when interpreting such data.

5.4.2 Misfit dislocation spacing of blanket and selective growth

From TEM analysis, it is clear that selective epitaxy in small areas reduces
dislocation density in SiGe films compared to the growth in a large areas. Figure 5.7
compares TEM images for the SEG and blanket films with comparable thickness. Figure
5.7 (a) shows plan-view TEM images of 10.6 nm-thick SiGe films grown in 1.3 μm and
2.3 μm square openings. Very few dislocations are observed in SiGe films with this
thickness, and when an area of ~126 μm² was observed, the dislocation spacing was
measured to be 2.7 ± 0.54 μm. Figure 5.7 (b) shows plan-view TEM images of a blanket
SiGe film of comparable thickness (11 nm). Misfit dislocations are easily seen, and
dislocation spacing is found to be 0.25 ± 0.03 μm for an area of observation of ~144 μm².
Figure 5.7 Plan-view TEM images of Si$_{0.33}$Ge$_{0.67}$-on-Si films illustrating the increase in critical thickness in small areas. (a) Few misfit dislocations are detected for a 10.6 nm-thick SEG film (average dislocation spacing is 2.7 μm). (b) 11-nm thick blanket Si$_{0.33}$Ge$_{0.67}$ film shows increased misfit dislocation density (dislocation spacing is 0.25 μm). Bright-field two-beam images with g=220. The same scale and crystallographic directions applies for all images in the figure.

It was found that the critical thickness is increased for SiGe films selectively grown in small areas. For wafers with a blanket SiGe deposition, no misfit dislocations are detected when the film thickness is 4.1 nm, but misfits are found for SiGe films with thickness greater than 5 nm. In this thesis, critical thickness is defined as a mid-point between film thickness where no dislocations are observed and misfits are first found. Using this definition, the critical thickness of Si$_{0.33}$Ge$_{0.67}$ in large areas is around 4.5 nm and is close to the calculated equilibrium thickness of 3.8 nm [15]. For SEG SiGe grown in 2.3 μm square openings, misfit dislocations are not found for 8 nm films but are
detected for films thicker than 8.9 nm, indicating that the critical thickness is around 8.5 nm and is increased by roughly 2x compared to that of the large area growth.

5.4.3 Effect of feature size on misfit dislocation spacing

When the dislocation spacing of SEG films of different sizes are compared, and impact of the growth area on the dislocation spacing is apparent for growth areas smaller than 10 x 10 μm. Figure 5.8 (a) shows plan-view TEM images of 24 nm-thick Si_{0.33}Ge_{0.67} films selectively grown in square openings of sizes 1.3, 2.3, and 10.3 μm. Misfit dislocations are very dense (small dislocation spacing) for 10.3 μm feature, but the density is significantly reduced for small growth area (large dislocation spacing). Figure 5.8 (b) plots misfit dislocation spacing as a function of SEG feature size, and shows as SEG feature becomes smaller, the misfit dislocation spacing becomes larger.
Figure 5.8 (a) Plan-view TEM images of 24 nm-thick Si$_{0.33}$Ge$_{0.67}$-on-Si films. Two-beam bright-field images $g$=220. (b) Misfit dislocation spacing as a function of SEG feature size. As SEG feature becomes smaller, the density of misfit dislocation is reduced, and misfit dislocation spacing becomes larger. Error bound is approximately 20%.

Misfit dislocation spacing is measured for SiGe films of thickness ranging from 4 nm to 24 nm, and the results are summarized and compared to the blanket data in Figure 5.9. While the blanket film shows a critical thickness (asymptote where dislocation spacing increases to infinity) only slightly higher than the calculated equilibrium thickness, SEG SiGe shows a larger dislocation spacing for a given thickness, which translates into fewer
misfit dislocations per unit area. The critical thickness is estimated to be 4.5 nm for blanket film, 6 nm for SiGe film grown in 50 x 50 μm square openings, and 8.5 nm for SiGe grown in 2.3 x 2.3 μm square openings. This represents a 1.5x and 2x increase for 50 μm and 2.3 μm openings respectively, compared to the equilibrium critical thickness of Si$_{0.33}$Ge$_{0.67}$.

**Figure 5.9** Dislocation spacing versus film thickness for SEG and blanket growth for Si$_{0.33}$Ge$_{0.67}$-on-Si. $h_c$ is 8.5 nm for SEG with feature size 2.3 μm, 6.0 nm for SEG feature size 50 μm and 4.5 nm for blanket growth. Calculated equilibrium thickness for Si$_{0.33}$Ge$_{0.67}$ is 3.8 nm.

### 5.5 Sources of misfit dislocation nucleation

For SiGe on Si heteroepitaxy where the SiGe film is grown above the critical thickness, several sources of misfit dislocation generation exist such as fixed sources, surface half-loop, or dislocation multiplication, as discussed in Chapter 2. To understand
the sources of dislocation nucleation for the SEG of SiGe on Si, an analysis introduced by Fitzgerald [36] has been utilized and the linear interface dislocation density is plotted against the SEG feature size, as shown in Figure 5.10. Error bound is estimated to be approximately 20% for SEG features of size 1.3 μm to 5.3 μm, and 13% for a feature size 10.3 μm.

![Graph showing the linear interface dislocation density against SEG feature size](image)

**Figure 5.10** Misfit dislocation density versus SEG feature size for Si$_{0.33}$Ge$_{0.67}$-on-Si film with different thickness. The linear slope indicates the existence of areal-dependent source of dislocation nucleation, and nonzero y-intercept suggests an additional active source for dislocation nucleation, possibly dislocation nucleation from SiGe film edges.

Three things are noticed from the above plot. First, the linear MD density is decreased for smaller features, which shows the effect of small area growth in reducing the misfit dislocation density. Second, for SEG features less than 10 μm, the linear interface-dislocation density is found to increase linearly with feature size. This indicates the source of dislocation nucleation is area dependent, and this source will be discussed further in section 5.5.1. Because the number of the samples is small, different fit were
tried to test the linearity of the data, and it was confirmed that a linear fit has the highest
coefficient of determination, $R^2$, value of 0.932, while polynomial and exponential fit
showed lower $R^2$ values of 0.829 and 0.865, respectively. Lastly, the plot shows the linear
fit does not extrapolate to zero density when feature size is reduced to 0. This suggests
that there is an additional source of misfit dislocations which does not scale with area,
such as SiGe film edges. Section 5.5.2 investigates the generation of misfit dislocations
from pattern edges.

### 5.5.1 Misfit dislocation nucleation by fixed sources

The linear slope in figure 5.10 suggests that only nucleation sources that scale with
the area have an impact in dislocation formation, because if dislocation multiplication
was active, the MD density would have superlinear dependence on feature size.

When dislocation interaction and multiplication are absent, the linear dislocation
density is given by the following equation [36].

\[
\rho = j \cdot N \cdot l
\]  

(5.2)

$\rho$ is the linear dislocation density, $N$ is the density of active source of dislocation
nucleation, $j$ is the fraction of MD along one $<110>$ direction, and $l$ is the average length
of MD segment. For selective growth of SiGe in small areas, $j=0.5$ and $l=L$, the SEG
feature size. Combining the variables,
\[ \rho = \frac{NL}{2} \quad (5.3) \]

and the density of fixed sources of misfit generation, \( N \) can be obtained from the slope of the linear MD density plot.

The \( N \) values are \( 0.098 \ \mu m^{-2} \) for film thickness 8.9 nm, \( 0.129 \ \mu m^{-2} \) for 10.6 nm, and \( 0.107 \ \mu m^{-2} \) for 11.2 nm. Previous study by A. Nishida [59] for \( Si_{0.8}Ge_{0.2} \) and \( Si_{0.7}Ge_{0.3} \) reports similar values; \( N=0.107 \ \mu m^{-2} \) for 150 nm-thick \( Si_{0.8}Ge_{0.2} \), and \( N=0.143 \ \mu m^{-2} \) for 75 nm-thick \( Si_{0.7}Ge_{0.3} \).

### 5.5.2 Misfit nucleation from the edge of SEG films

The linear dislocation density from Figure 5.10 extrapolates to a non-zero value when SEG features size is traced to 0 \( \mu m \). This indicates there is another active source of dislocation nucleation that is independent of area and cannot be eliminated by reducing the feature size. Nucleation from the pattern edges is proposed as the source of misfit dislocation generation.

**A. Strain concentration at the edge of a SiGe film**

The edge of the SEG films could generate misfit dislocations for several reasons. First, stress modeling of a SEG structure shows a point of high strain at the film edge. Stress simulation was performed by Jamie Teherani using the Sentaurus software, and at the film edge, the level of strain was approximately 3x higher than the neighboring area.
Such strain concentration point can act as a dislocation nucleation source, and introduce misfits in the SiGe film.

![High strain point](image)

**Figure 5.11** Stress simulation of a Si$_{0.3}$Ge$_{0.7}$ SEG structure showing a high strain point at the SiGe film edge. Stress modeling using Sentaurus software by J. Teherani.

**B. Non-planar Si substrate**

Cross-sectional TEM images reveal a slight curvature in the Si substrate near the pattern edge. The curvature originates from the oxide mask etching and prebake steps (section 5.2.3), and is never fully eliminated even after careful wet etching and low-temperature prebake. Such curvature can result in stress concentration and generate misfit dislocations near the edge. Figure 5.12 shows the worst-case example, where the Si substrate shows a severe "dishing" profile. The SiGe film grown on this sample shows a very high density of misfit dislocations in the layer, and TEM analysis shows that the defects are concentrated near the film edge, where the Si curvature is high. Typical SEG structures show much flatter film (Figure 5.1 (b)), but the curvature still exists. This
implies the Si substrate preparation is very important in controlling misfit dislocation density, and Si surface curvature can contribute to dislocation generation from the edge of SEG films.

Figure 5.12 XTEM image of the “worst case example,” showing SiGe grown on Si substrate with severe overetching. High density of defects at the film edge is found, and since misfit dislocation can be generated from a non-planar Si surface, care should be taken during the pre-epi processing steps to ensure planar Si profile. SiGe thickness is 12.1 nm.

C. Increased thickness near the film edge

TEM images show there is a film thickness variation near the pattern edge. The film thickness near approximately 100 nm from the pattern edge is slightly thicker (as much as 15% and with an average of 7.5%) than the bulk of the SEG film, as shown in Figure
5.13. This rim of greater thickness introduces more elastic stress, and can assist in generating misfit dislocations in the SiGe film.

![Graph](image)

**Figure 5.13** SiGe film thickness at the edge, plotted against the film thickness at the bulk of the SEG features of size less than 10.3 μm. The thickness at the edge is greater than the center thickness, by an average of 7.5%. Thickness is measured by cross-sectional TEM imaging.

5.5.3 EDS analysis: Ge composition at the SiGe film edge

One question that came up is whether the SiGe composition is affected by the preferential growth at the pattern edge, since an increase in the growth rate at the pattern edge could result in a change in germanium composition. Previous Auger study confirmed there is no significant loading effect for SEG samples with feature size less than 10 μm, however, an analysis has not been done to compare the Ge composition near
the edge to the bulk of the film. An experiment was designed to use energy-dispersive X-ray spectroscopy (EDS) with a TEM setup to measure the atomic composition at the film edge. A cross-sectional TEM sample was prepared using a SiGe film selectively grown in 2.3 x 2.3 μm opening. XTEM image shows the film thickness is 11.2 nm at the center and 12.3 nm near the pattern edge, which is 9.8% thicker than the bulk of the film. Using an electron beam of size around 5 x 7 nm, EDS spectra were collected and are plotted in Figure 5.14. The two spectra from the center and edge of the SiGe film are nearly identical, and indicate there is no significant compositional variance between the center and the edge of the SiGe film.

Figure 5.14 (a) Cross-sectional TEM image of a SiGe film used in the EDS analysis. SiGe film is grown in a 2.3 μm square opening. Thickness is 11.2 nm at the center of the film and 12.3 nm near the pattern edge. (b) EDS measurement performed at the center and near the edge of the
SiGe sample. The EDS spectrum show almost identical graphs for both areas. EDS measurement courtesy of Dr. Y. Zhang, MIT Center for Materials Science and Engineering.

5.6 The orientation of SEG features

The SEG mask includes various shapes such as squares, circles, diamonds, and long rectangular openings to study the influence of feature orientation on the critical thickness. It is observed that the misfit dislocation density for SEG growth is strongly influenced by the shape and orientation of the growth area. Figure 5.15 shows 10.6 nm-thick Si$_{0.33}$Ge$_{0.67}$ films, where the SiGe in Figure 5.10 (a) is grown in square oxide openings with edges parallel to the $<110>$ direction, Figure 5.10 (b) in 45° rotated squares with edges parallel to $<100>$, and Figure 5.10 (c) in circular openings. All squares in (a) and (b) are 3.3 x 3.3 μm, and circles in 5.10 (c) have diameter of 3.3 μm. The misfit dislocation density is much higher in Figure 5.10 (b) and (c), compared to (a).
Figure 5.15 Plan-view TEM of Si$_{0.33}$Ge$_{0.67}$ that was grown in (a) $<110>$ square oxide openings, (b) 45° rotated features (sidewall along $<100>$), and (c) circular features. (b) and (c) show higher misfit dislocation density. All SiGe films are 10.6 nm thick. Bright-field two-beam images with g=220. The same scale and crystallographic directions applies for all images in the figure.

Further analysis was carried out to compare the dislocation spacing of 3.3 x 3.3 μm features oriented along $<110>$ and $<100>$ sidewalls. TEM analysis was used to measure the dislocation spacing of SiGe films with thickness of 8.9 nm, 10.4 nm, and 10.6 nm, and it can be shown from Figure 5.16 (a) that for all cases, SEG features with $<100>$ sidewall have smaller dislocation spacing (more misfit dislocations), by a factor of approximately 4x. Figure 5.16 (b) compares the 3.3 x 3.3 μm data to a blanket SiGe growth and also SiGe SEG in large area (50 x 50 μm, sidewall oriented along $<110>$ directions). Even though 3.3 μm SEG with $<100>$ sidewalls have more dislocations than
<110> sidewalls, there still is a benefit from small area growth for 3.3 μm SEG samples, compared to a growth in large areas.

![Graphs showing misfit dislocation spacing versus Si$_{0.33}$Ge$_{0.67}$-on-Si film thickness for 3.3 μm-wide squares oriented along <110> direction (blue squares) and along <100> direction (red diamonds). Features with <100> sidewalls show much lower dislocation spacing, indicating a higher density of dislocations. 8.9 nm-thick SiGe sample was grown on p$^+$ Si substrate with a rotated major flat along the <100> direction. p' substrates are used for the rest of samples.](image)

**Figure 5.16** Misfit dislocation spacing versus Si$_{0.33}$Ge$_{0.67}$-on-Si film thickness for 3.3 μm-wide squares oriented along <110> direction (blue squares) and along <100> direction (red diamonds). Features with <100> sidewalls show much lower dislocation spacing, indicating a higher density of dislocations. 8.9 nm-thick SiGe sample was grown on p$^+$ Si substrate with a rotated major flat along the <100> direction. p' substrates are used for the rest of samples.

MD density is increased when SEG sidewalls are not aligned along the <110> directions. This could be due to microfaceting of the Si$_{0.33}$Ge$_{0.67}$ film. Figure 5.17 shows AFM topographical images from a study by L. Vescan et al. [122, 123]. Si$_{0.95}$Ge$_{0.05}$ films were selectively grown on Si in 3 x 3μm oxide openings, and AFM scans show the SiGe faceting behavior when the growth area has sidewalls along <110> or <100> directions. When the growth is aligned along the <110> direction, {311} facets are dominant. However, when the SiGe film is aligned along the <100> direction, multiple facets such as {110} and {311} are formed. Figure 5.18 shows a sample grown as part of this thesis,
consisting of thick Ge-on-Si selective epitaxy along \( <110> \) and \( <100> \) sidewalls, and similar behavior to that reported by Vescan is observed. For growth with \( <110> \) sidewalls, the \( \{311\} \) facets are much better defined, but the growth with \( <100> \) sidewalls shows jagged facets along the film edge. These microfacets introduce stress variation near the edge, and also could act as gettering sites for impurities and precipitates. Because of this, dislocation density might be increased for SEG features with non-\( <110> \) sidewalls.

![Figure 5.17](image)

**Figure 5.17** AFM topographical images of Si\(_{0.05}\)Ge\(_{0.05}\) films selectively grown on Si with sidewalls (a) along the \( <110> \) directions and (b) along the \( <100> \) directions. \( \{113\} \) faceting is dominant for (a), but multiple facets are shown for (b). These microfacets might act as nucleation sites for misfit dislocations, increasing the dislocation density for feature with non-\( <110> \) sidewalls. From L. Vescan [123]
Figure 5.18 SEM images of Ge films selectively grown on Si with sidewalls (a) along the <110> directions and (b) along the <100> directions. (113) faceting is dominant for (a), but multiple, jagged facets are shown for (b). Film thickness is approximately 500 nm. The scale bar and crystallographic direction applies to both images in the figure.

5.7 Summary and conclusions

Figure 5.19 shows the critical thickness for SEG and blanket SiGe growth from this work, and compares the data to previously reported experimental values and to the calculated equilibrium limit [15, 35, 54-59, 122, 124]. It is noted that for all Ge ranges, \( h_e \) for SEG is larger than that of the blanket growth. However, while a factor of 3 to 5-fold increase in \( h_e \) is found for SEG of SiGe with low Ge composition, for high Ge content, the increase in \( h_e \) in small areas is a factor of two. This may be related to the higher mismatch and driving force for dislocation formation.
In summary, the selective epitaxial growth of thin, high Ge-content strained SiGe-on-Si has been studied. Germanium percentage is found to be independent of the SEG feature size, and for Si$_{0.35}$Ge$_{0.65}$, the critical thickness was increased by a factor of two (from 4.5 nm to 8.5 nm) using limited area growth with a feature size 2.3 μm. For SEG samples, misfit dislocations are generated by fixed sources such as surface impurities or mechanical damage, instead of dislocation multiplication events. SiGe film edge also introduces misfit dislocations, and because the MD generation from pattern edge is very process sensitive, care should be given during fabrication process to control such sources. SEG feature orientation has a strong influence on the critical thickness of SiGe films, and features with edges along <110> yield the lowest misfit dislocation density.
Chapter 6

Thesis Summary and Future Work

In this chapter, the main topics and contributions of this thesis are reviewed, and suggestions for future studies are discussed.

6.1 Thesis summary

The goal of this thesis was to study the selective growth of two limiting cases of SiGe-on-Si heteroepitaxy for device applications: thin, strained SiGe films for active regions of the heterostructure-based transistors, and thick, relaxed Ge films for optoelectronic devices.

In developing thin, smooth Ge-on-Si films, growth conditions have a large effect on film morphology. When the effect of growth temperature and reaction chamber pressure on Ge-on-Si growth was studied, an optimum temperature and pressure for smooth film surface was found. At 365 °C and 60 torr, it took 100 sec to grow 20 nm of Ge, with an RMS roughness less than 1 nm. From Ge growth data, a period of delayed epitaxial growth, or the “incubation time,” was noticed, and growth conditions for minimizing Ge surface roughness generally corresponded to the conditions to minimize the incubation time. Si surface treatment by flowing a short SiGe pulse was developed to improve the
Ge surface roughness (RMS roughness around 0.3 nm), and it also reduced the incubation time for growth of thin Ge on Si substrates.

For photodiode applications, relaxed, thick Ge was grown in selective areas on oxide-patterned Si wafers. Growth temperature and germane partial pressure affect the faceting and hole-filling behavior of Ge film, and optimal growth condition for relaxed Ge SEG was found to be 750 °C and 10 torr, with 100 sccms of GeH₄ and 10 slpm H₂ flow. To reduce the threading dislocation density, thermal cyclic annealing at 800/450 °C was utilized, and the effect of Ge film thickness and growth area on the TD density was also studied. After cyclic annealing, Ge surface had a RMS roughness of less than 1 nm and threading dislocation density of ~3x10⁷ cm⁻² in large areas. The TD density can be further reduced for small area growth.

SEG of high Ge-content, strained SiGe-on-Si was studied for applications in SiGe-channel structures. The sources of misfit dislocation nucleation in selective growth were analyzed, and the MD generation from SiGe pattern edges was investigated. Strain concentration, Si surface curvature, and preferential SiGe growth near the SEG pattern edge all contribute to the generation of misfit dislocations. Using limited area growth, the critical thickness of SEG Si₀.₃₃Ge₀.₆₇ film was found to be 8.5 nm, which is an increase by a factor of two compared to the growth in large areas (h_c=4.5 nm for blanket SiGe growth).
6.2 Contributions

The major contributions from this thesis are listed below.

1. Development of thin, smooth Ge-on-Si films
   - Development of the optimum growth conditions for smooth Ge-on-Si growth
   - Investigation of the effect of growth temperature and pressure to the Ge-on-Si growth rate, incubation time, and film morphology
   - Development of (with Leonardo Gomez) a pre-epi Si substrate treatment technique to reduce the Ge incubation time and improve film smoothness

2. Selective epitaxial growth of relaxed Ge-on-Si
   - Experimental analysis of the effect of growth condition to Ge nucleation on the oxide field.
   - Development of the optimum growth temperature and gas pressure for uniform Ge film with reduced faceting and improved hole-filling behavior
   - Analysis of the threading dislocation density and how it is influenced by thermal annealing and small area growth.

3. Selective growth of ultrathin, high Ge-content SiGe-on-Si
   - Development of a mask pattern suitable for TEM study of misfit dislocation analysis
   - Increase in the critical thickness of Si$_{0.33}$Ge$_{0.67}$ films in SEG growth
   - Analysis of the sources of MD generation for SiGe SEG
6.3 Suggestions for future work

- For thin Ge-on-Si study, further investigation of pre-epi Si substrate treatment will help in understanding the role of SiGe pulse technique. A theoretical model can be developed to explain the relationship between incubation time and Ge surface morphology.

- For thick, relaxed Ge-on-Si, studying doped Ge film growth would be necessary for photodiode device fabrication. In selective growth, the effect of sidewall material and further study of growth conditions to further reduce the threading dislocation density in the Ge film.

- For selective growth of SiGe-on-Si, obtaining more experimental data for SEG features with less than 10 μm will help understanding and analyzing the sources of misfit dislocations. The effect of thermal annealing in the metastable film should be investigated, and SEG of even higher Ge-content SiGe film can be beneficial for heterostructure MOSFET applications.
Appendix A
TEM sample preparation and imaging

Standard TEM specimen preparation methods were employed to prepare the samples for TEM imaging. Both cross-sectional and plan-view analysis were utilized in this thesis.

A.1 Cross-sectional TEM (XTEM)

A.1.1 Sample preparation

Figure A.1 shows the sample preparation steps used for XTEM samples. After cleaving the sample to small pieces of size 3 x 3 mm, two pieces of Ge- or SiGe-on-Si samples are bonded such that the films of interest mirror each other (Figure A.1 (d)). This stack is mounted on the Gatan™ Disc Grinder, and is mechanically grinded and polished on one side first. The sample is then flipped over to grind the other side until the sample thickness is less than 10 μm, and the polished surfaces are optically smooth (Figure A.1 (e)). The sample is carefully transferred to a Cu TEM grid which has a circular or oval opening in the center, and is thinned by Fischione 1010 Ion mill to create an electron transparent region. Ideally, the ablation by ion bombardment occurs in the center of the sample, and a symmetric hole will open up.
Figure A.1 Steps for XTEM sample preparation. (a) Starting sample. (b) The sample is cleaved to 3 x 3 mm pieces. (c) Two pieces are stacked and (d) bonded using the M-Bond™. (e) The stack is mechanically ground and polished. (f, g) Sample is mounted on a Cu TEM grid. (h) Fischione ion mill is used to thin the sample, until a small hole opens up in the center.

A.1.2 XTEM imaging

Cross-sectional TEM analysis was used to either measure the film thickness or to image crystalline defects such as threading dislocations in thick Ge-on-Si growth. Because Si and Ge have a diamond cubic structure, they cleave along the <110> directions and the [110] zone axis can easily be found looking at the electron diffraction pattern in the TEM. Figure A.2 shows the diffraction pattern for a diamond cubic structure with the [110] axis aligned to the electron beam [20, 125]. The 002 reflection is forbidden, but is present because the allowed 111 diffracted beam acts like a new incident beam and is rediffracted by the (1 1 1) plane. The sum of the two allowed
reflections, \((\bar{1}11) + (1\bar{1}1)\), results in a 002 reflection, but it is much weaker than other reflections [126].

Figure A.2 (a) Electron diffraction pattern for a diamond cubic structure when the [110] axis is aligned to the electron beam, from Luan [20]. (b) Diffraction pattern of crystalline Si obtained in TEM using a parallel beam, 100kV in a [110] zone axis, from De Wolf et al. [125].

For the film thickness measurement, high-resolution TEM on-axis images are taken, using JEOL 2011 High Contrast Digital TEM and double-tilt holder available in the MIT Center for Materials Science & Engineering (CMSE). For defect imaging, bright-field two-beam conditions were used. In chapter 4, the defect of interest was threading dislocations in Ge-on-Si structure. It is well known that in the Ge/Si system, the 60° “mixed” dislocations have Burgers vector of the form \(\pm \frac{a}{2}[101], \pm \frac{a}{2}[10\bar{1}], \pm \frac{a}{2}[01\bar{1}], \) or \(\pm \frac{a}{2}[011]\), and reflecting condition of \(g=2\overline{2}0\) or \(g=\overline{2}20\) was used for TEM analysis to ensure \(g \cdot b \neq 0\) and the dislocations are visible [20].
A.2 Plan-view TEM (PTEM)

A.2.1 Sample preparation

Figure A.3 shows the sample preparation steps for plan-view sample. Sample is cleaved to a size of 3 x 3 mm piece, and is mechanically grinded and polished from the backside of the wafer (Figure A.3 (b)). The sample is transferred to a Cu TEM grid which has a circular or oval opening in the center, and Fischione 1010 ion mill is used to thin the sample until a small hole opens up in the center of the sample.

Figure A.3 Steps for PTEM sample preparation. (a) The sample is cleaved to a 3 x 3 mm piece. (b) The sample is mechanically grinded and polished from the backside. (c, d) Sample is mounted on a Cu TEM grid. (e) Fischione ion mill is used to thin the sample, until a small hole opens up in the center.

A.2.2 PTEM imaging
In chapter 4, thick Ge-on-Si structures were studied and the threading dislocation density was analyzed using plan-view TEM images. In chapter 5, thin SiGe-on-Si samples and the misfit dislocation spacing were investigated using TEM. In both studies, beam direction was along the [001] direction, and bright-field two-beam condition was utilized with \( g = \{220\} \). In most cases, the imaging area of the sample was tiled in two directions 90° apart, i.e. in \( g = 220 \) and \( g = \overline{2} 20 \) reflections, to ensure all dislocations are imaged.

Ion milling angle was set at 13°, and after milling, the sample thickness approaches 0 near the center hole and increases in thickness away from the opening. For threading dislocation analysis, viewing areas close from the hole were imaged because it was desired to only image dislocations that threaded all the way to the free surface. Typical images would show electron-transparent viewing area of thickness 0.4 to 0.7 microns. For strained SiGe-on-Si study, sample thickness is not as important as long as the viewing area is transparent to electrons. To avoid severe bend contours, viewing area of 5 to 20 \( \mu \text{m} \) away from the hole was chosen, and the thickness of observed area would range from 1 to 4 microns.

![Figure A.4](image)

**Figure A.4** A schematic diagram of a typical plan-view TEM sample used in the analysis of threading dislocations and misfit dislocations.
Appendix B

The error bound in analysis of MD spacing

To measure the misfit dislocation density and spacing of SiGe-on-Si sample, the following steps and statistical analysis are performed.

CASE 1:

Uniform distribution of misfit dislocations with spacing < 1 μm.

Figure B.1 shows TEM images a blanket Si_{0.33}Ge_{0.67} film with thickness around 13 nm. Plan-view TEM images are taken with magnification of x5000. For blanket samples, five to seven images are taken at random observation sites. For each image, six lines of counting dislocations of length 4 μms are randomly placed along the <110> directions and misfit dislocations across the line are counted. The counting lines are numbered as below, and the measurement data is tabulated in Table B.1.
Figure B.1 Plane-view TEM images of SiGe-on-Si sample, growth in large area. Lines of counting misfit dislocations are indicated in red. Crystallographic directions and scale bar applies to all micrographs in the figure.

Table B.1: dislocation counts for blanket SiGe film

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<td>22</td>
<td>23</td>
<td>13</td>
<td>9</td>
<td>8</td>
<td>8</td>
<td>16</td>
<td>17</td>
<td>13</td>
</tr>
</tbody>
</table>

The average, or mean value of dislocation count is:

\[ m = \frac{1}{n} \sum x_i \] (B.1)

where \( m \) is the average value over \( n \) cut lines, \( n \) is the number of cuts, and \( x_i \) is the individual dislocation counts for each cut line. In above case, \( n=30 \) and \( m = 15.73 \)
Sample variance $\sigma$ of the data is given by:

$$\sigma = \sqrt{\frac{1}{n} \sum (m-x_i)^2}$$  \hspace{1cm} (B.2)

and standard error of the mean from sampling distribution is:

$$\sigma_M = \frac{\sigma}{\sqrt{n}}$$  \hspace{1cm} (B.3)

From the values in Table B.1, straight forward calculation can be carried out using equations B.2 and B.3 [127, 128]. Sample variance is 5.12, and standard error of the mean for this set of data is 0.93. Assuming a normal distribution of sampling data, 95% confidence interval will give an error bound at 11.8%. More rigorous analysis can be performed using t-distribution method [129-131]. However, with 30 data points the difference in error bound is not significant and simpler analysis is used for the rest of the thesis to avoid extra difficulty.

Because this number is based on a cross section of 4 $\mu$m length, the misfit dislocation density and dislocation spacing is

$$\text{average dilocation density} = \frac{\text{average count per cut line}}{4 \ \mu\text{m}} = 3.93 \mu\text{m}^{-1}$$  \hspace{1cm} (B.4)

$$\text{average dilocation spacing} = \frac{4 \ \mu\text{m}}{\text{average count per cut line}} = 0.254 \mu\text{m}$$  \hspace{1cm} (B.5)

with error bound of 11.8%, the dislocation density from above example will be $3.93 \pm 0.46 \mu\text{m}^{-1}$, or dislocation spacing of $0.254 \pm 0.03 \mu\text{m}$. 

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CASE 2:

Sparse misfit dislocations distribution with dislocation spacing > 2 μm.

When there is a small number of misfit dislocations, the sampling error is increased with same statistical analysis. Careful analysis should be performed especially for SEG wafers, because when there are few misfit dislocations, there could be a large sample variance depending on the observed location.

Figure B.2 shows plan-view TEM images of Si$_{0.33}$Ge$_{0.67}$ film with thickness around 10 nm, grown in selective area of 3.3 x 3.3 μm squares. When 30 SiGe patches are analyzed, the films either contained 0, 1, or 2 misfit dislocations per SEG area, as shown below.

(a) (b) (c)

Figure B.2 Plane-view TEM images of SiGe-on-Si SEG sample, containing (a) 2 misfit dislocations, (b) 1 misfit dislocation, or (c) no dislocations. Bright-field two-beam images with g=220. Crystallographic directions and scale bar applies to all micrographs in the figure.

<table>
<thead>
<tr>
<th>feature #</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>dislocation count</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>
Using equation B.1 to take an average, 0.93 dislocation/feature is calculated. However, because the dislocation count can vary up to 100% depending on the feature, sample variance is 0.628 and standard error is 0.115. Sampling error with 95% confidence interval is 24.6%, which is much higher than the case of blanket sample of 11.8% error. Lowering the confidence interval to 90% will still give a sampling error of 21%, and care should be given when analyzing and interpreting samples with very low misfit dislocation density.

Because the average count and sampling error is based on SEG features of size 3.3 μm,

\[
\text{average dilocation density} = \frac{\text{average count per feature}}{3.3 \ \mu m} = 0.283 \ \mu m^{-1} \quad (B.6)
\]

\[
\text{average dilocation spacing} = \frac{3.3 \ \mu m}{\text{average count per cut line}} = 3.53 \ \mu m \quad (B.7)
\]

with error bound of 24.6%, the dislocation density from above sample will be 0.283 ± 0.069 μm⁻¹, or dislocation spacing of 3.53 ± 0.87 μm.

<table>
<thead>
<tr>
<th>feature #</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
<th>17</th>
<th>18</th>
<th>19</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>dislocation count</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>feature #</th>
<th>21</th>
<th>22</th>
<th>23</th>
<th>24</th>
<th>25</th>
<th>26</th>
<th>27</th>
<th>28</th>
<th>29</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>dislocation count</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Appendix C
Sample list from chapter 5

1. For SEG samples with square feature size < 10 μm

<table>
<thead>
<tr>
<th>Epi number</th>
<th>SiGe thickness</th>
<th>MD spacing for SiGe films grown in square openings of size:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1.3 μm</td>
</tr>
<tr>
<td>6586</td>
<td>8.6 nm</td>
<td></td>
</tr>
<tr>
<td>5268</td>
<td>8.9 nm</td>
<td></td>
</tr>
<tr>
<td>6358</td>
<td>8.9 nm</td>
<td></td>
</tr>
<tr>
<td>5764</td>
<td>9.0 nm</td>
<td>3.9 μm</td>
</tr>
<tr>
<td>6587</td>
<td>10.4 nm</td>
<td></td>
</tr>
<tr>
<td>5765</td>
<td>10.6 nm</td>
<td>3.53 μm</td>
</tr>
<tr>
<td>5766</td>
<td>11.2 nm</td>
<td>1.52 μm</td>
</tr>
<tr>
<td>6643</td>
<td>24 nm</td>
<td>0.47 μm</td>
</tr>
</tbody>
</table>

2. For SEG samples with square feature size = 50 μm

<table>
<thead>
<tr>
<th>Epi number</th>
<th>SiGe thickness</th>
<th>MD spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>6363</td>
<td>6.2 nm</td>
<td>11.4 μm</td>
</tr>
<tr>
<td>6364</td>
<td>7.8 nm</td>
<td>2.56 μm</td>
</tr>
<tr>
<td>6365</td>
<td>10.5 nm</td>
<td>0.75 μm</td>
</tr>
<tr>
<td>6366</td>
<td>14.4 nm</td>
<td>0.66 μm</td>
</tr>
</tbody>
</table>

3. For blanket SiGe samples

<table>
<thead>
<tr>
<th>Epi number</th>
<th>SiGe thickness</th>
<th>MD spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>5767</td>
<td>4.9 nm</td>
<td>9.2 μm</td>
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<tr>
<td>5877</td>
<td>5.5 nm</td>
<td>5.5 μm</td>
</tr>
<tr>
<td>5878</td>
<td>6.63 nm</td>
<td>1.7 μm</td>
</tr>
<tr>
<td>6369</td>
<td>8.9 nm</td>
<td>1.16 μm</td>
</tr>
<tr>
<td>5879</td>
<td>11.0 nm</td>
<td>0.25 μm</td>
</tr>
<tr>
<td>5880</td>
<td>22 nm</td>
<td>0.074 μm</td>
</tr>
<tr>
<td>5882</td>
<td>45 nm</td>
<td>0.033 μm</td>
</tr>
</tbody>
</table>
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