

# Designing and Implementing a Readout Strategy for Superconducting Single Photon Detectors

by

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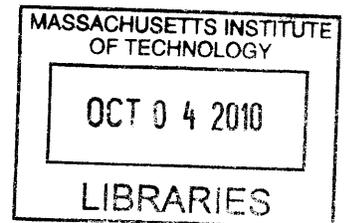
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# Contents

<b>1</b>	<b>Introduction</b>	<b>17</b>
1.1	SNSPD Physics . . . . .	19
1.1.1	Hotspot Theory . . . . .	19
1.2	Current Readout Status . . . . .	20
1.3	Project Scope . . . . .	21
1.3.1	Rapid Single-Flux-Quantum (RSFQ) On-chip Readout . . . . .	21
1.3.2	Cryogenic RF Electronics . . . . .	22
1.3.3	Detectors in Parallel . . . . .	22
<b>2</b>	<b>Cryogenic Amplifier</b>	<b>23</b>
2.1	Cryogenic Electronics Considerations . . . . .	23
2.2	Amplifier Topology . . . . .	25
2.3	Simulations . . . . .	28
2.4	Results . . . . .	32
2.5	Possible Improvements . . . . .	33
2.6	Cryogenic Bias Tee . . . . .	35
<b>3</b>	<b>RSFQ Theory</b>	<b>39</b>
3.1	Josephson Junction Physics . . . . .	40
3.2	Resistively Shunted Junction Model . . . . .	43
3.3	RSFQ Definition . . . . .	45
<b>4</b>	<b>RSFQ Cell Design</b>	<b>47</b>

4.1	Josephson Transmission Line (JTL)	47
4.2	SQUID Comparator	48
4.3	D Flip Flop	49
4.4	DC to SFQ converter	51
4.5	SFQ to DC converter	52
4.6	Experimental Configurations	54
<b>5</b>	<b>RSFQ Simulations</b>	<b>57</b>
5.1	Front-End Simulations	57
5.1.1	Simulink Implementation of RSJ Model	58
5.1.2	Combined SNSPD-RSJ Model	59
5.2	Logic Simulations	63
<b>6</b>	<b>Parallel SNSPDs</b>	<b>69</b>
6.1	Advantages of Parallel Detectors	69
6.2	Simulations	70
<b>7</b>	<b>RSFQ Layout</b>	<b>75</b>
7.1	WRSpice Design Package for Superconducting Circuits	75
7.2	RSFQ Specific Layout Practices	76
7.3	Layout of Readout Experiments	80
7.4	Additional Considerations	82
<b>8</b>	<b>RSFQ Experimental Setup</b>	<b>83</b>
8.1	Physical Construction	83
8.2	Electrical Connection Strategy	84
8.3	Optical Setup	86
<b>9</b>	<b>Conclusion</b>	<b>89</b>
<b>A</b>	<b>Appendix</b>	<b>91</b>
A.1	Integrated Circuit Layout	91
A.1.1	General Practices	91

A.1.2	Hypres Foundry . . . . .	96
A.1.3	Superconducting IC Layout . . . . .	97
A.2	Simulink Thermoelectric Model for SNSPD . . . . .	99
A.2.1	Thermal Model Implementation . . . . .	99
A.2.2	Simulink Setup . . . . .	99
A.2.3	Simulation Results . . . . .	100
A.2.4	Matlab Code Listing . . . . .	101
A.3	Experimental Drawings . . . . .	106



# List of Figures

1-1	An electron micrograph of an example Superconducting Nanowire Single-Photon Detector (SNSPD). Current flows through the meanders in the middle from pads on either side. The wires in the meander are approximately 100 nm wide. Note that the additional formations exist to balance the dose between the edges and the middle of the detector.	19
1-2	This is a schematic of how an incident photon produces a voltage pulse at the output. At (a), an incident photon is absorbed to produce an initial hot-spot shown in (b). The diverted supercurrent exceeds the critical current in the now-constricted wire in (c). Finally, a small section of the wire becomes fully resistive in (d), producing a voltage pulse.[23]	20
1-3	Schematic of current RF/DC setup. Each of these electronic components lies outside of the cryostat. As a result, the system must be very well shielded and 50Ω matched to prevent noise from overcoming our signal.	21
1-4	Schematic of the scope of this project. Digital logic is constructed utilizing RSFQ technology. Additional (unshown) analog interface circuits will be discussed.	22
2-1	Schematic of a HEMT band diagram. Note that the carrier channel is displaced from the doping sites, thereby preventing retrapping at low temperatures.[3].	25

2-2	Schematic of the cryogenic amplifier design. The active element is an Avago ATF-55143 enhancement pHEMT. . . . .	26
2-3	Figure of gain versus frequency. Note that there is a small amount of peaking around 2GHz. This is due to the small value of the gate resistor.	29
2-4	Stability factor K of the amplifier for varying frequencies. Note that this is simulated at room temperature for 50Ω input and output impedances. Therefore, we can assume a reasonable amount of error associated with this simulation. . . . .	30
2-5	Noise factor of our amplifier. Note that this is an overestimate because we have simulated our amplifier at 300K, so the Johnson noise of our resistors will be much larger than at 4.2K where the amplifier will operate. . . . .	31
2-6	S parameters for the cryogenic amplifier. Note that S11 and S22 are larger than is usually acceptable. This mismatch is a design choice specific to our application which enables us to get additional gain. . .	31
2-7	Measured S21 parameter at room temperature. These results follow exactly what we expect. Note that we have a slightly decreased bandwidth and no peaking between 1 and 2 GHz due to the loss in the FR4. The additional peaking above 5GHz is disconcerting, but will not be observed, as the loss in the probe is much greater than 5dB at 5GHz.	32
2-8	Measured S21 of the amplifier when attached to the probe. Note that now we have less gain and a very sharp cutoff just below 800MHz. This is due to the loss of the probe. . . . .	33
2-9	Reverse-engineered schematic of the currently used bias tee (Mini-Circuits ZFBT-4R2G+).[1] This tee is 50Ω matched at all inputs. The analog inductor/capacitor values are far too large to fabricate on-chip.	35
2-10	Schematic of the new bias tee design. Note that it consists only of an on-chip inductor utilizing kinetic inductance to achieve the large value. Note that we include a 50 Ω termination on the current source to simulate a low-impedance cable. . . . .	36

2-11	Results for simulations of the bias tee with a SNSPD detector pulse. The blue line shows the current through the $50 \Omega$ amplifier, and the red line shows the current lost into the current source. The original signal amplitude is $10\mu\text{A}$ . . . . .	37
3-1	Basic Josephson junction potential. Energy of the superconducting wavefunction is given as $E_0$ , which is less than the barrier height. Image courtesy of [21] . . . . .	41
3-2	Schematic of RSJ model. Note that the element in the middle is the ideal Josephson junction with relations given by 3.10 and 3.11. The R and C elements represent unavoidable aspects of the Josephson junction.	43
3-3	Figure of information token for RSFQ circuits. First, we define our clock as a train of SFQ pulses with period $T_{CLK}$ . We then define ‘0’ and ‘1’ as either the presence or absence of a pulse in between two clock pulses. . . . .	46
4-1	Schematic of the JTL stage. Input and output is labeled, but the stage is symmetric; an SFQ pulse can propagate in either direction. . . . .	48
4-2	Design schematic of input SQUID comparator. Note that there is a resistive divider at the input which provides a $50 \Omega$ termination. This termination is not completely necessary, as it will be located close to the detector. However, it does serve to remove any potential ringing due to parasitic capacitance causing an underdamped LC circuit. . . . .	49
4-3	Schematic of the D Flip Flop Stage. This stage functions by trapping a fluxon in L1 when a pulse inputs from the input and releasing it with a clock pulse. . . . .	50
4-4	A design schematic for the DC to SFQ converter. J1-J3, L1-L3 are effectively a hysteretic comparator, while L5, L6, and J4 are an output JTL buffer. . . . .	51

4-5	Schematic of SFQ/DC converter. Effectively, we have an input JTL (J1) which goes to a T Flip Flop (J2-J7). In the 1 state, the output exceeds the critical current of J9, which produces a series of SFQ pulses at the output. This yields a small DC voltage when low-passed. . . .	53
4-6	Block diagram for the ‘Brahman’ experiment. This is the most basic RSFQ circuit that we will design. We will utilize this circuit as a baseline and testbench for manipulating bias and environment parameters.	54
4-7	Block diagram for the ‘Brangus’ experiment. This circuit implements a memory element, the D flip flop. We will utilize this circuit to test the memory lifetime capabilities of RSFQ circuits. . . . .	55
4-8	Block diagram for the ‘Hereford’ experiment. This circuit implements our SQUID comparator at the input. We will utilize this circuit along with some standalone SQUIDS to characterize this input stage. . . .	55
4-9	Block diagram for the ‘Texas Longhorn’ experiment. This circuit can act as a fully functional readout for a single SNSPD. We will test this circuit first to ensure functionality. Next, if all is functional, this circuit will be interfaced to the SNSPD. . . . .	56
5-1	Simulink model for a Josephson junction. We use the RSJ approximation and include the presence of an external shunt resistance in the model. Each of our junctions is shunted with approximately $1\Omega$ . . . .	58
5-2	Simulink construction of a DC/SFQ converter. We will perform most of our digital simulation in WRSpice, as it uses more accurate models and is designed for layout. However, our RSJ model suffices to describe basic RSFQ circuits. . . . .	59
5-3	Simulation results for the DC/SFQ converter. This Matlab simulation accurately reflects the results given in WRSpice, demonstrating the robustness and capability of our model. . . . .	60

5-4	Simulink model of the complete SNSPD and input stage to RSFQ. Note that we have included the newly designed bias tee as the splitter. Finally, the input stage consists of the magnetically coupled SQUID that we read out. . . . .	61
5-5	Top: detector current; Middle: SQUID output voltage; Bottom: Detector Resistance. Note that as the detector fires, we observe multiple SFQ pulses being produced by the SQUID comparator. This occurs because we have biased the SQUID very close to its critical current, so we exceed the critical current by a larger amount, creating a rapid train of SFQ pulses. . . . .	62
5-6	Simulation results for the ‘Brahman’ test circuit. If this circuit functions properly, an input current square wave will result in SFQ pulses causing the DC/SFQ converter to produce a DC output. Note that because the DC/SFQ converter is effectively a T flip flop, the output frequency will be 1/2 of the input frequency. . . . .	64
5-7	Simulation results for the ‘Brangus’ test circuit. The top four traces reflect the input signals and their respective SFQ pulse trains. ‘D SFQ’ goes to the D port of the flip flop, and when the next clock pulse arrives, we observe an SFQ pulse at the flip flop output. This then toggles the SFQ/DC converter. . . . .	65
5-8	Simulation results for the ‘Hereford’ test circuit. Note that we have tried to mimic the detector current input by having a $20\mu\text{A}$ peak pulse input with decay time on the order of 10nS. This current profile roughly matches that of the detector. We observe the predicted pulse train from the SQUID, and these toggle the SFQ/DC converter. . . . .	66
5-9	Simulation results for the ‘Texas Longhorn’ test circuit. The top four traces are input stage signals and their respective SFQ pulses incident on the flip flop. Flip flop and SFQ/DC output pulses are given. Note that the D flip flop gates multiple pulses from the SQUID comparator stage. . . . .	67

6-1	Simulink setup for the parallel nanowire simulation. Individual detector currents and resistances are shown in dashed/solid, respectively. Note that each 4-port box contains a full thermoelectric model for the SNSPD. We also tie an inductor to ground in series with the detector. This is a deliberately fabricated part that aims to maintain constant current in the detectors. . . . .	71
6-2	Results for the parallel nanowire simulation at $9\mu\text{A}$ total bias. Note that the system oscillates due to the fact that one detector does not fire immediately after another. This results in a type of ‘flux trapping’ which causes the second detector to switch at a later time, causing oscillations. . . . .	72
6-3	Simulation results for a properly functioning detector cascade. Individual detector currents and resistances are shown in dashed/solid, respectively. Conditions are the same as the oscillating case except bias current has been increased to $10\mu\text{A}$ . Note that after the switching event, the current does not redistribute between the two detectors evenly.	74
7-1	Standard design flow for integrated circuit fabrication. This flow is mimicked exactly by WRSpice, which provides integrated software for each of these steps. . . . .	76
7-2	A schematic of the Hypres stack with each layer designated.[33] . . .	77
7-3	Schematic of how a large series inductance leads to flux trapping. Note that the persistent current will have current such that $LI = \Phi_0$ . Since we have a large inductance, $I$ can be small enough not to exceed $I_c$ of the Josephson junctions. Avoiding large series inductances prevents this problem. . . . .	78

7-4	Schematic of the anodization stack[9]. This corresponds to the Hypres stack as follows: upper and lower Nb contacts are M2 and M1 respectively. Junction area is defined by I1A or I1C depending on the process (1kA/cm <sup>2</sup> /4.5kA/cm <sup>2</sup> respectively). The insulator is patterned with I1B. Finally, the anodization area is patterned by its own layer, ‘A’.	79
7-5	Example of the abstraction breakage between the DC/SFQ converter cell and its containing cell. (a) is a figure of the DC/SFQ converter, (b) is the containing cell, and (c) is a figure of both cells flattened. Note that certain layers overlap from the outer layer to the DC/SFQ such that the layers have to ‘interlock’. This is not desirable because if this dependence changes, it requires the designer to change all of the containing cells at each DC/SFQ instance.	81
8-1	Measurement of $S_{21}$ of the probe. This transmission coefficient indicates loss in our system. This measurement is over twice the length of the probe, and as such indicates twice the loss that we will observe from a signal transmitting from the probe head to the instrumentation outside the cryostat.	86
A-1	A schematic of the Hypres stack with each layer designated.[33]	96
A-2	Simulink model of a SNSPD. Note that the electrical model is simply a constant kinetic inductanc with a series resistance. The thermal model controls the value of this resistor in time by measuring detector current and whether or not a photon is incident.	100
A-3	Example circuit for simulating a single SNSPD with readout circuitry. Note that the readout amplifier is simulated as a single 50 $\Omega$ resistor.	101
A-4	Simulation results from the Simulink thermoelectric model. Note that the simulation properly reproduces previous simulation results for resistance versus time and output voltage versus time.	102

A-5	Model of the probe head. There are three primary flanges connected by posts. Flange ‘A’ connects the probe head to the 0.5” O.D. tube. Flange ‘B’ is the mount for the PCB adapters and shielding can. Flange ‘C’ is the mount for the incoming fiber line. . . . .	106
A-6	Schematics of the boards for the adapter stack. (a) RSFQ Sample mount (b) RSFQ adapter board (c) Base board (d) SNSPD mount board. . . . .	107

# List of Tables

4.1	Values of electrical components for the D flip flop . . . . .	50
4.2	Values for electrical components in the DC/SFQ converter. . . . .	52
4.3	Values for electrical components in the SFQ/DC converter. . . . .	54



# Chapter 1

## Introduction

Photon detection is an integral part of experimental physics, high-speed communication, as well as many other high-tech disciplines. In the realm of communication, unmanned spacecraft are travelling extreme distances, and ground stations need more and more sensitive and selective detectors to maintain a reasonable data rate.[10] In the realm of computing, some of the most promising new forms of quantum computing require consistent and efficient optical detection of single entangled photons.[27] Due to projects like these, demands are increasing for ever more efficient detectors with higher count rates.

The Superconducting Nanowire Single-Photon Detector (SNSPD) is one of the most promising new technologies in this field, being capable of counting photons as faster than 100MHz and with efficiencies around 50%.[22] Currently, the leading competition is from the geiger-mode avalanche photodiode, which is capable of  $\sim$ 20-70% efficiency at a  $\sim$ 5MHz count rate depending on photon energy.[18]

In spite of these advantages, the SNSPD is still a brand-new technology and as a result they do not have the same support hardware support as other detectors. As such, SNSPD's are much more difficult to integrate into an existing an experiment. Because of this difficulty, SNSPD's have not been deployed extensively for research or industrial applications. The signal analysis chain that is connected to this detector is one of the key choke points.

Each detector count produces a 0.1 mV, 10 nS wide pulse with a maximum count

frequency on the order of 100MHz. Currently, this signal is processed outside of the cryostat with a series of RF amplifiers and a high-speed counter. This design works for detector prototyping, but poses a series of problems with actual design implementation. Most importantly, it prevents our design from being scalable. Even though we can fabricate thousands of detectors on a single wafer, it would be extremely difficult to place that many RF lines without crosstalk or other interference.

The purpose of this thesis is to build a more robust and scalable readout technology for SNSPDs. First, we will develop intermediate technologies that improve upon current readout technology and will be necessary to develop the final goal. Ultimately, we plan to build circuitry on-chip that will first convert each detector's analog signal to a digital signal and then condense the data from each detector into an externally clocked, single-bit output indicating the presence or absence of a photon at any detector. This will allow simultaneous readout of a large number of detectors on a single wafer. Additionally, our cryogenic will decrease the noise observed by the detector, as the amplifier is no longer operating at room temperature. Finally, our readout will provide a simple hardware API to be interfaced to a computer or embedded processing unit.

The catch to this development process is that the entire system must operate at 4.2K or below. As such, one must either use HEMT CMOS or Rapid Single-Flux-Quantum (RSFQ) logic. HEMT CMOS is better suited to analog amplification of the output signal, while RSFQ circuitry is better suited to the construction of the SNSPD interface and digital logic.

RSFQ circuitry is better suited as an input stage because input amplification with CMOS is difficult, as one must operate in the linear regime of a HEMT. This requires on the order of 1 mA at 1.8 V minimum, which results in approximately 2 mW per stage. This is to be compared against RSFQ comparators which utilize approximately 0.5 mA at almost no voltage, resulting in  $\mu$ W of dissipation per stage. Given that we are hoping to produce a large number of SNSPD input stages, RSFQ is clearly a better choice. However, we only have a small number of output signals from the cryostat, so it is much more reasonable to use CMOS, as we can attain larger signal

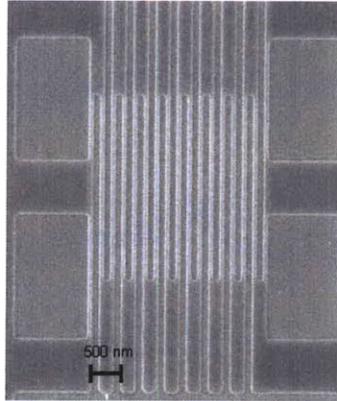


Figure 1-1: An electron micrograph of an example Superconducting Nanowire Single-Photon Detector (SNSPD). Current flows through the meanders in the middle from pads on either side. The wires in the meander are approximately 100 nm wide. Note that the additional formations exist to balance the dose between the edges and the middle of the detector.

amplitudes.

## 1.1 SNSPD Physics

This photon detector consists of a meandering superconducting nanowire biased close to its critical current. In this regime, a single incident photon can cause a section of the detector to switch to normal conduction, producing a voltage pulse due to its now-finite resistance. An electron micrograph is given in figure 1-1.

### 1.1.1 Hotspot Theory

When a section of the detector goes normal due to an incoming photon, the effective resistance of the detector increases dramatically, and therefore the current through the detector drops temporarily.

Now, two things happen simultaneously. First, the heat localized in the hotspot must diffuse to other parts of the detector or substrate. Second, the detector is inductive, so there is an  $L/R$  relaxation time of current returning to the detector.

However, these are competing processes. Any current through the detector will

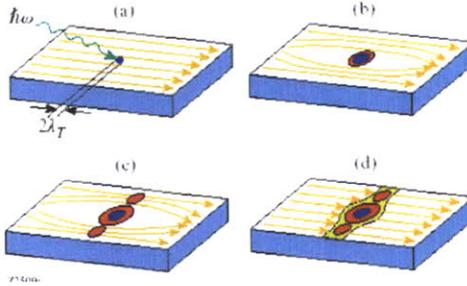


Figure 1-2: This is a schematic of how an incident photon produces a voltage pulse at the output. At (a), an incident photon is absorbed to produce an initial hot-spot shown in (b). The diverted supercurrent exceeds the critical current in the now-constricted wire in (c). Finally, a small section of the wire becomes fully resistive in (d), producing a voltage pulse.[23]

end up in joule heating of the resistive section of the detector, extending the amount of time it takes to cool the hotspot back down. There are two stable states to this system. The system can either relax to the superconducting state, or it can ‘latch’ into the normal state. When a photon is incident on the detector, the  $L/R$  reset time determines which of these states the system resets to. Generally, longer  $L/R$  time constants result in resetting to the superconducting state, while shorter  $L/R$  results in latching.[32][15]

These two time constants determine the output pulse size and therefore the maximum count rate of the detector.

## 1.2 Current Readout Status

Currently, all SNSPD readout technology takes place outside of the cryostat. A schematic of the RF setup required is shown in figure 1-3. This system is not scalable to multiple SNSPDs, as each SNSPD would require an individual bias line, which is not feasible.

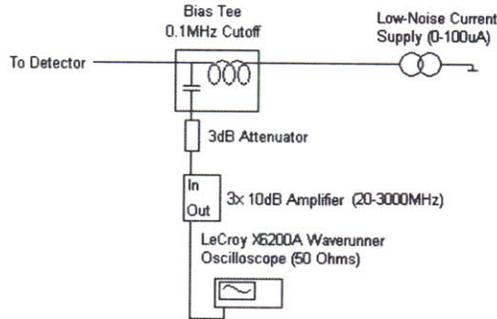


Figure 1-3: Schematic of current RF/DC setup. Each of these electronic components lies outside of the cryostat. As a result, the system must be very well shielded and  $50\Omega$  matched to prevent noise from overcoming our signal.

## 1.3 Project Scope

The goal of this project is to develop a fully integrated readout system. A schematic is given in 1-4. We will be replacing all of the RF circuitry discussed in the previous section, and replacing this with processing technology that exists on-chip.

This project consists of several facets which will ultimately come together for a full readout. First, we have the RSFQ circuitry which will serve as the dominant amplification and processing technology. However, we will also design some analog interfaces which will enable RSFQ to be used. In addition, I will quickly discuss some adaptations of the detector itself which can make readout easier.

### 1.3.1 Rapid Single-Flux-Quantum (RSFQ) On-chip Readout

RSFQ circuitry will provide most of the functionality as an on-chip readout. This circuitry is comprised of an input SQUID comparator, basic digital processing, and DC/SFQ converter units. Our initial circuit design is very simple, as we wish to characterize the fabrication process, our experimental setup, and SNSPD/RSFQ interactions. However, in principle, this digital design is highly scalable, allowing for complex digital analysis of incoming SNSPD signals.

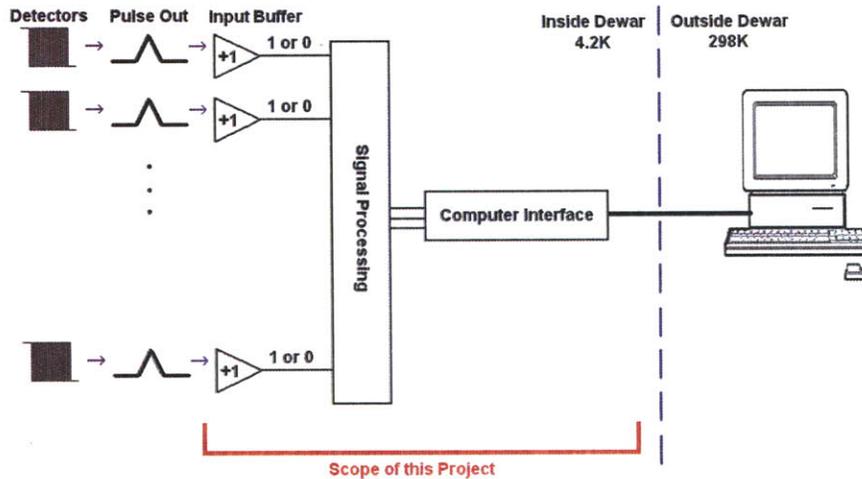


Figure 1-4: Schematic of the scope of this project. Digital logic is constructed utilizing RSFQ technology. Additional (unshown) analog interface circuits will be discussed.

### 1.3.2 Cryogenic RF Electronics

In order to use RSFQ circuitry, we must first adapt the detector output to properly channel its signal into the RSFQ comparator. This cryogenic bias tee has been designed and fabricated. In addition, we must provide a proper interface between the RSFQ outputs and traditional CMOS logic. Since RSFQ utilizes much smaller signal amplitudes than traditional CMOS, it will be necessary to design a cryogenic amplifier to boost these signals.

### 1.3.3 Detectors in Parallel

We will quickly discuss one way to modify the detector itself to aid in the readout process. If one utilizes multiple SNSPDs in parallel, the signals from each photon detected causes an avalanche which is substantially easier to read out.

However, this topology is significantly more complicated than a single nanowire, and therefore contains complex dynamics. Analysis and models constructed for SNSPD/RSFQ interaction analysis are also used to better understand these dynamics and their effect how we read out these parallel detectors.

# Chapter 2

## Cryogenic Amplifier

For our scalable cryogenic readout, we require an RSFQ input stage which converts each detector pulse to a digital SFQ signal. However, we ultimately must convert this signal to a DC voltage to be read by traditional room-temperature CMOS logic. This is difficult, as RSFQ circuits can only output fractions of a mV. Therefore, we need additional amplification on the back-end.[31]

Although we could not use a cryogenic amplifier for each of the detectors due to power considerations, there are far fewer output signals from the RSFQ circuitry that must be amplified. Therefore, we can now use a cryoCMOS amplifier without fear of dissipating too much energy inside of the cryostat. In addition, the bandwidth of this detector is broad enough to amplify single detector pulses as well. Although it is still difficult to read out multiple detectors, there are a number of advantages to amplifying the detector signal close to the detector: we decrease noise seen by the detector, which increases our SNR of the pulses coming out of the cryostat.

### 2.1 Cryogenic Electronics Considerations

Most electrical devices are rated for around  $300\pm 40\text{K}$ . This rating is mostly package-driven for high-temperatures. For cryogenic considerations, there are a different set of considerations that must be taken into account. These problems vary depending on the component in question.

First, many resistors are highly temperature dependant. High-value carbon resistors use stacked Metal-Insulator-Metal tunnelling junctions to achieve this high resistance. However, the behavior of this physical phenomena changes dramatically at low temperatures.[16] Therefore, one must use lower-value metal film resistors which have much better behavior at low T. These resistors depend only on the resistivity of a given metal and therefore behave well at low temperature. The most common materials for thin film resistors are NiCr, TaN, and PbO. None of these become superconducting at 4.2K. Given a linear 25-50ppm/°C temperature dependence (as specified in the data sheet), we can expect between 10-15% value change maximum between room temperature and cryogenic temperatures. This extrapolation is supported by experimental findings[24]. This change in resistivity is acceptable for our purposes, as our resistor values are not tightly specified.

Next, electrolytic capacitors require mobile ions in a solvent in the capacitor itself to achieve its rating. However, once the solvent freezes, the capacitor value drops dramatically. Therefore, it is only prudent to use chip capacitors with solid dielectrics. In this case, the dielectric constant is much less sensitive to temperature change and does not 'freeze out' like electrolytic dielectrics. The best options are polymer and low-K ceramic capacitors. High-K ceramics tend to use complicated materials as dielectric. The physics of these materials is not guaranteed to function at low temperatures.[16]

Finally, MOSFET's and BJT's also do not function at low temperatures. Basic semiconductor technology utilizes doping to provide free carriers. However, these dopants have a specific ionization energy (which is usually less than  $KT$ ). However, as one cools the transistor, the number of free carriers drops dramatically as the dopant sites retrap their carriers. HEMT and p-HEMT transistors address this problem by using a heterojunction which uses differences in bandgap to displace carriers away from the doped material.[8] Specifically, one uses N doped AlGaAs (relatively large bandgap material) sandwiching a thin layer of InGaAs (lower bandgap material with a lower energy conduction band).

The excess electrons flow to the InGaAs conduction band, as it is of lower energy.

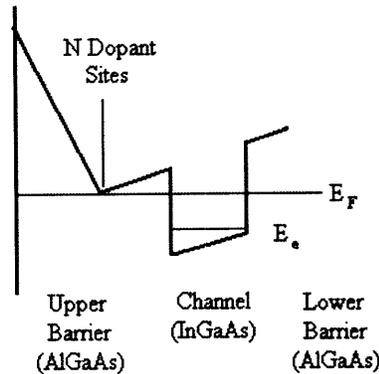


Figure 2-1: Schematic of a HEMT band diagram. Note that the carrier channel is displaced from the doping sites, thereby preventing retrapping at low temperatures.[3].

Now, with an applied voltage at the gate, we can decrease the energy of this conduction band below the Fermi energy of the contacts, and conduction is allowed. This interests us, however, because the carriers are now displaced from the dopant sites, so there is no retrapping. Therefore, freeze-out cannot occur, and these devices behave well even at cryogenic temperatures.

## 2.2 Amplifier Topology

Despite the difference in microphysics, a HEMT has the same basic behavioral characteristics as a standard MOSFET. Therefore, we can use the standard topologies for amplification that have been developed for MOSFET technology.

Our first amplifier design used a common-source topology. This topology allowed us to derive the most gain from our devices, but also had the side-effect of having a high input impedance to the transistor (a small capacitive load,  $C_{gs}$ ). A high impedance input is traditionally desirable, but it can potentially become a liability at UHF frequencies, as it may cause a  $50\ \Omega$  matched system to become unstable.

At this point, it must be mentioned that we are mounting our amplifier geometrically close to the detector, and as such the amplifier will not see  $50\ \Omega$  at its input. Rather, we can treat the SNSPD as a freewheeling inductor. However, if we stabilize

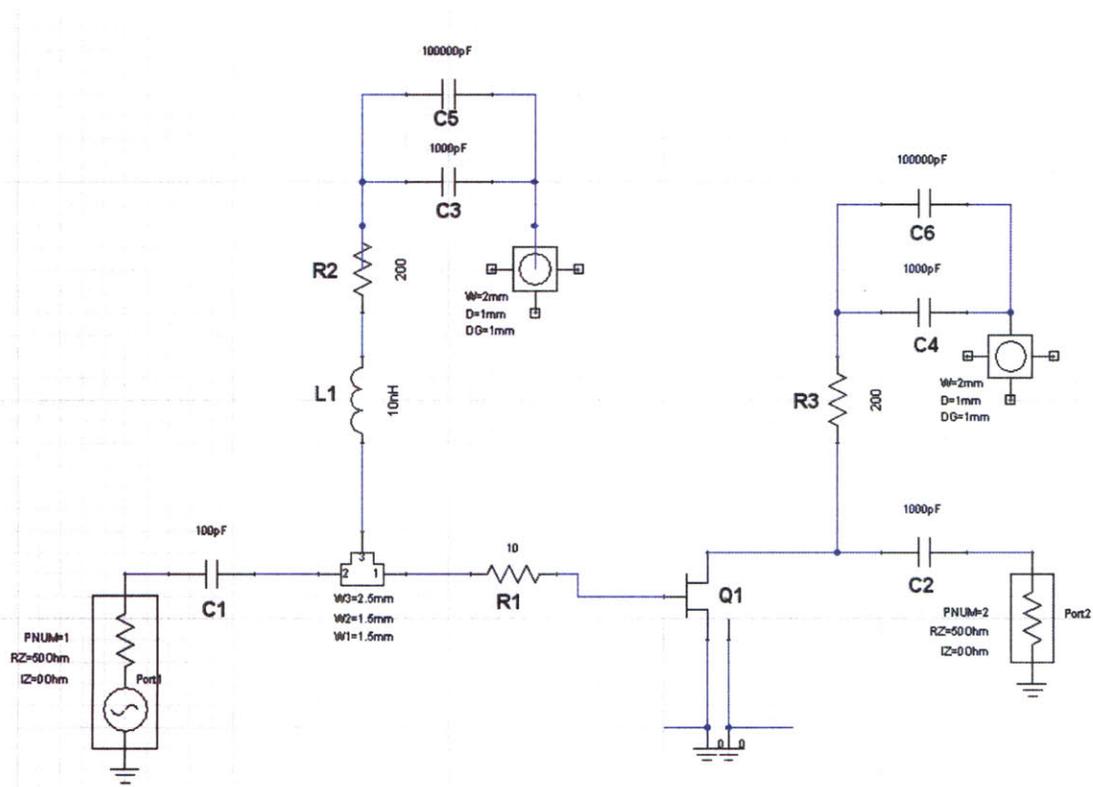


Figure 2-2: Schematic of the cryogenic amplifier design. The active element is an Avago ATF-55143 enhancement pHEMT.

our system properly, we should not observe oscillations in either of these cases.

Note also that in our single-stage implementation above, we do not match the output to  $50 \Omega$  either. We have made this choice because we need more gain than is available if we match the output to  $50 \Omega$ . The impedance mismatch is not a huge problem for us, as we are not terribly concerned about reflections off of this node, but should it become an issue, it is easily resolved by either using multiple stages or using a source-follower impedance matching circuit. Such an addition will not remove bandwidth from the system. The only downside will be increased power draw.

Traditionally when designing RF circuits, one aims for a specific (narrow band) region of amplification. We are looking for much more broadband amplification, so I used a different strategy than most RF amplifiers. We are operating at such a low frequency (0.01-2GHz), that instead of utilizing the HEMT S-Parameters, we can roughly approximate our HEMT (Q1) as having infinite input impedance in this region of input frequency with a small capacitance from gate to source. In order to maintain a relatively constant input impedance, I added a small inductance (L1) to the input termination to compensate. However, the most important element is the gate resistor (R1). This resistor decreased the transconductance of the stage as less voltage was seen between the gate and source of the HEMT at high frequencies. This reduction in input signal was necessary, as the HEMT had significant transconductance even at very high frequencies. If we had not compensated for this, the system would have become unstable at high frequencies (1-2GHz). We could see this by observing the  $K$  stability factor. If this factor is less than 1, our system is conditionally stable:[2]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (2.1)$$

where  $\Delta = S_{11}S_{22} - S_{12}S_{21}$ . This factor becomes small when  $|S_{12}S_{21}|$  becomes of order unity. At low frequencies, the reverse transmission  $S_{12}$  is very low, so the system is stable. However, past 1GHz,  $S_{12}$  begins to approach unity. In order to keep  $K > 1$ , our system has to be very well matched ( $S_{11}$  and  $S_{22}$  small) to remain stable.

However, we have chosen to not match our system perfectly to achieve better gain characteristics. Therefore, we decrease  $S_{21}$  at high frequencies with the gate resistor R1.

The downside to this approach is that it increases our noise substantially since Johnson-Nyquist noise is directly amplified by the high-impedance node of the common source amplifier. Therefore, we make R1 as small as possible without destabilizing the circuit.

## 2.3 Simulations

After simulating this circuit, there are several interesting features to note. However, we must keep in mind the limitations of our simulation. First, we have simulated our system with a  $50 \Omega$  source and load. While the latter is accurate, our detector is far from  $50 \Omega$ . In reality, it can be only really be understood as a constant inductance with some varying resistance in time (corresponding to an incident photon and heat dissipation). This system is *highly* nonlinear and as such cannot be simulated as a small signal model. We have addressed this problem by building an appropriate detector model in Simulink, and then reconstructing the input stage of our amplifier as a load for the photon detector and performing a transient simulation. These simulations have shown that the input stage does not oscillate, so the impedance mismatch does not create problems.

Simultaneously, if this amplifier will be used for RSFQ circuitry it will see a low impedance output from the RSFQ circuitry. The SFQ to DC converter has an output impedance equal to the normal resistance of the Josephson junction in parallel with its shunt resistor. The shunt resistor is much smaller than the Junction resistance at  $1 \Omega$ , so the amplifier will see a  $1 \Omega$  voltage source. This also is not problematic, because in both of these cases the amplifier will be exceedingly close to the operating device with respect to the wavelength of the incoming signal. Therefore, we do not need to view the input as coming from a transmission line.

However, for the purpose of our analysis it is useful to characterize scattering

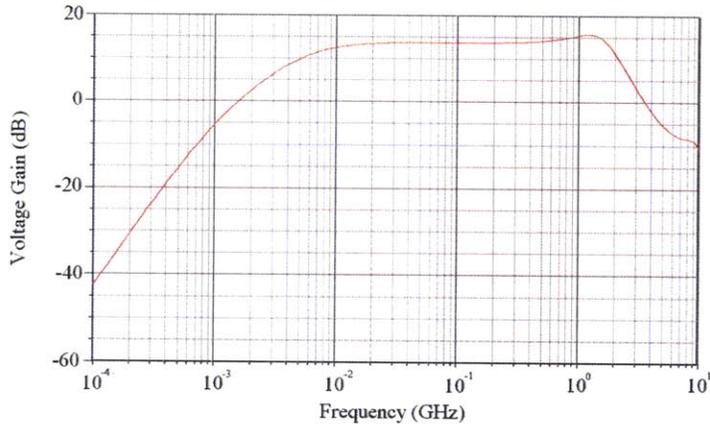


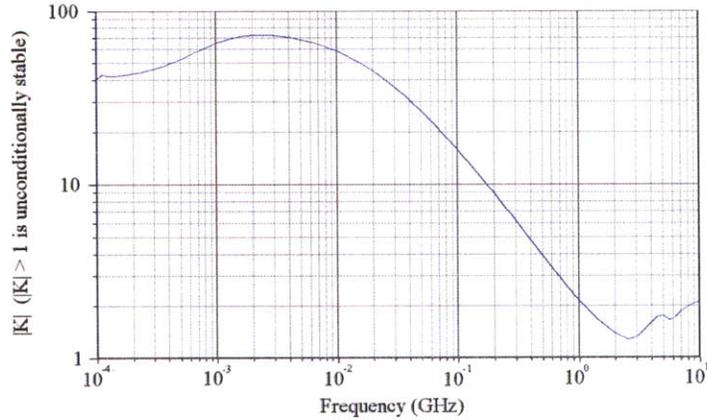
Figure 2-3: Figure of gain versus frequency. Note that there is a small amount of peaking around 2GHz. This is due to the small value of the gate resistor.

parameters, so we will assume a  $50 \Omega$  input and keep in mind that this impedance is not the impedance of the detector. Therefore, the simulation is not numerically accurate, but provides insight as to the behavior and stability of the amplifier.

A second shortcoming is that we must simulate at room temperature (300K). This is due to the fact that there is very little real data as to the temperature dependence of passive parts on that extreme of a temperature range. As a result, dramatically changing the temperature in simulation does not accurately reflect device performance. However, we have taken proper precautions to use passive parts that will not deviate from their nominal values much at cryogenic temperatures. The HEMT may potentially cause instability at low temperatures, as its gain increases slightly as temperature decreases. This problem will be discussed further later.

The maximum available gain of the device (calculated from S parameters on datasheet) is approximately 15dB over the range of interest. We have achieved slightly less than 15dB gain between 20MHz and 2GHz. (See figure 2-3)

Note that our stability factor (K) becomes very close to 1 (below 1 indicates instability) slightly above 1GHz. This dip in the stability factor is due to the inductively coupled terminations having a slightly underdamped resonant system with  $C_{gs}$  of the transistor. This behavior of this resonance also explains why we stabilize our system when we increase the resistance of the gate resistor. This resistor is effectively a



Instead of utilizing the HEMT S-Parameters,

Figure 2-4: Stability factor  $K$  of the amplifier for varying frequencies. Note that this is simulated at room temperature for  $50\Omega$  input and output impedances. Therefore, we can assume a reasonable amount of error associated with this simulation.

damping resistor. However, we have minimized this value to achieve minimal noise figure, therefore our system is slightly underdamped, leading to some peaking in the gain curve and resultant decrease in the stability of the circuit. This peaking behavior is worsened by the fact that our HEMT has increased gain at low temperatures.

However, there is one additional unsimulated factor that will prevent our system from oscillating. We are building our circuit on an FR4 substrate. FR4 is the standard PCB material and behaves well below 1-2GHz. At and above these values, FR4 becomes lossy. Therefore, we will not observe significant gain peaking in this frequency range, as our substrate will be the ultimate limiting factor. If it becomes necessary to understand this loss further, one can gain additional understanding of this loss through lossy transmission line theory with transmission line capacitor shunted by a resistor simulating the loss.

Our noise figure simulation is probably the least accurate of the simulation data we have collected for two reasons: (1) we simulated at room temperature, so all of our resistors are contributing full 300K Johnson noise; and (2) the HEMT noise figure is not well defined over the frequencies of interest, but is claimed to be approximately between 0.3-0.6dB at room temperature and decrease as temperature decreases. In summary, the simulated values are an overestimate of noise figure.

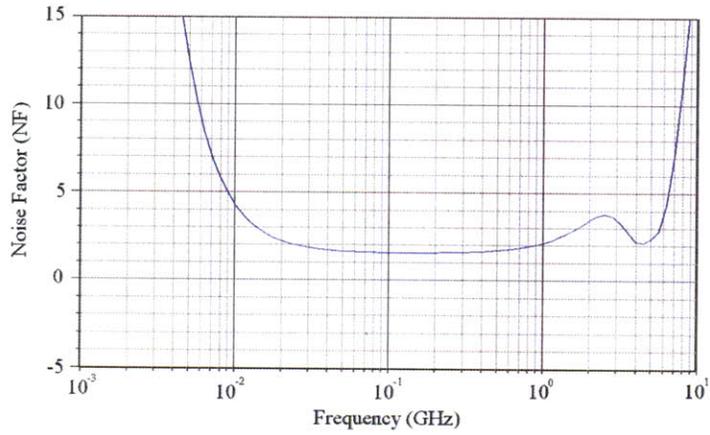


Figure 2-5: Noise factor of our amplifier. Note that this is an overestimate because we have simulated our amplifier at 300K, so the Johnson noise of our resistors will be much larger than at 4.2K where the amplifier will operate.

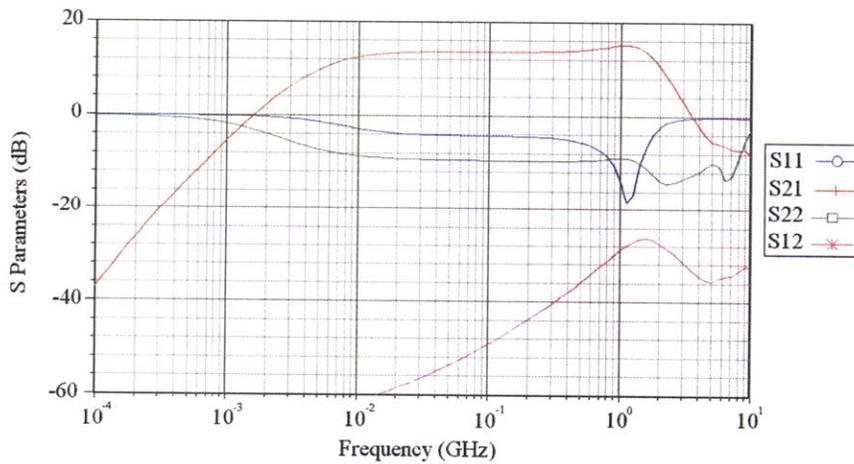


Figure 2-6: S parameters for the cryogenic amplifier. Note that S11 and S22 are larger than is usually acceptable. This mismatch is a design choice specific to our application which enables us to get additional gain.

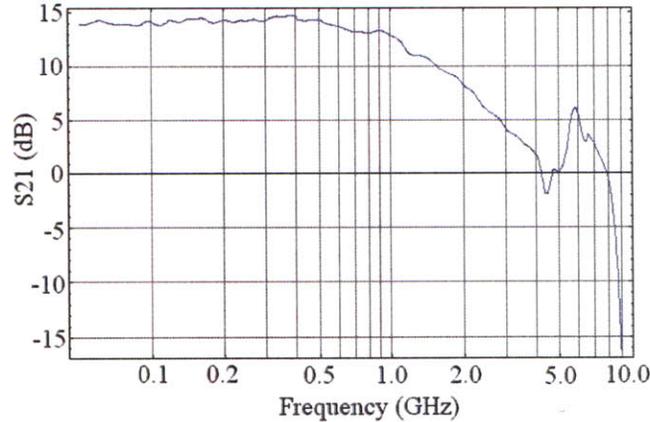


Figure 2-7: Measured S21 parameter at room temperature. These results follow exactly what we expect. Note that we have a slightly decreased bandwidth and no peaking between 1 and 2 GHz due to the loss in the FR4. The additional peaking above 5GHz is disconcerting, but will not be observed, as the loss in the probe is much greater than 5dB at 5GHz.

Finally, we have simulated scattering parameters for the amplifier. This plot is revealing as to the limitations of this amplifier. Since we have not matched input or output very well to  $50 \Omega$ , our S11 and S22 parameters are relatively large. However, I argue that this is acceptable for our applications. Our input will not be  $50 \Omega$  matched, and some reflections off the output are acceptable as the other end of our system will be properly terminated.

## 2.4 Results

We constructed an amplifier and it worked as designed. We first characterized gain as a function of frequency directly, as shown in figure 2-7. Note that we observed a roll-off in gain at about 1-2GHz as expected, but we did not observe any gain peaking or indications of instability at this frequency. On the other hand, we observed a gain peak between 5 and 10GHz. This peaking is most likely due to self-resonance of the passive components (the inductor (L1) in particular). While this is bothersome, it turned out to have little importance due to additional losses from the cryogenic probe on which the amplifier is mounted.

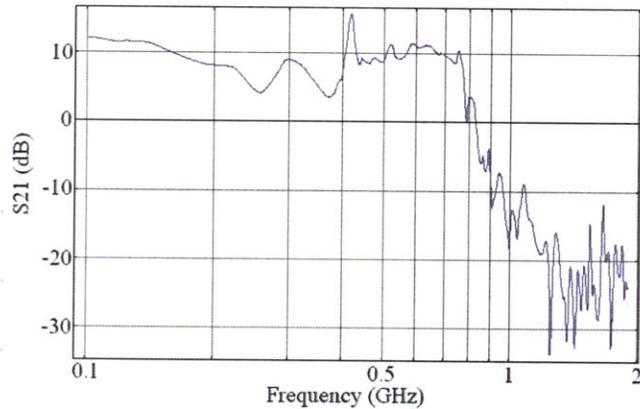


Figure 2-8: Measured S21 of the amplifier when attached to the probe. Note that now we have less gain and a very sharp cutoff just below 800MHz. This is due to the loss of the probe.

We have also characterized the transfer function of the amplifier when mounted on the cryogenic probe. This curve is shown in figure 2-8. Note that we observed a dramatic cutoff in gain at 800MHz. This was due to the fact that the probe head had significant parasitic capacitance. As a result, high frequency signals were lost. This capacitance removed the peaking behavior of the amplifier but also limits our bandwidth.

In the above plots, note that we have characterized the S parameters from 50MHz to 2GHz due to the lower frequency limit on our network analyzer. Below this frequency we used a spectrum analyzer to verify the  $s^2$  roll-off at 20MHz (not shown). However, the higher frequency characteristics are more critical to our application, therefore we focus our analysis here.

## 2.5 Possible Improvements

This first cryogenic amplifier is a single-stage common source amplifier. There are several simple methods of improving this topology should additional specifications need to be met. For example, if the gain is not high enough or we need to match output impedance, we can add an additional source follower onto the output of the

common source amplifier. This will provide a low-impedance output which we can match to  $50\Omega$ . In addition, the intermediate impedance between the common source amplifier and source follower can take any reasonably low value, so we can choose to have a larger amount of amplification than is possible with a single stage.

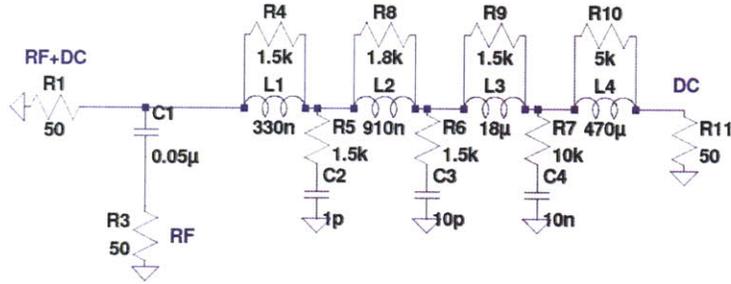


Figure 2-9: Reverse-engineered schematic of the currently used bias tee (Mini-Circuits ZFBT-4R2G+).[1] This tee is  $50\Omega$  matched at all inputs. The analog inductor/capacitor values are far too large to fabricate on-chip.

## 2.6 Cryogenic Bias Tee

One of the most crucial technologies enabling our single photon detector is the bias tee, which allows a DC bias current and RF signal pulse to travel along a single RF-coax line and subsequently be separated. Typically, a bias tee is implemented in figure 2-9.[12]

Note that this is basically just an LC circuit with stacked inductors to successively remove incrementally lower frequencies. The use of incremental stages is necessary because the larger inductors have self-resonances at frequencies of interest. Also, the entire system is  $50\Omega$  matched on the RF-DC and RF ports.

Ultimately, we are trying to achieve scalability of design. We need to bias and read-out multiple detectors on a single chip. The problem then arises that the our detectors are of the order  $10\text{-}100\mu\text{m}^2$ , the RSFQ circuitry for each element is on the same order of area, but the bias tee connecting them must be large due to its large passive elements. Therefore, we must find a technology that has the same order space requirements as the detector/RSFQ circuitry.

The solution lies in the fact that our system is not  $50\Omega$  matched, and our cutoff frequency can be much higher than standard bias tees (most of our frequency components lie between 1MHz and 1GHz). Taking this into consideration, we consider the passive elements available to us with each of our fabrication processes. With Hypres's tri-layer Nb process for RSFQ circuits and the current space requirements,

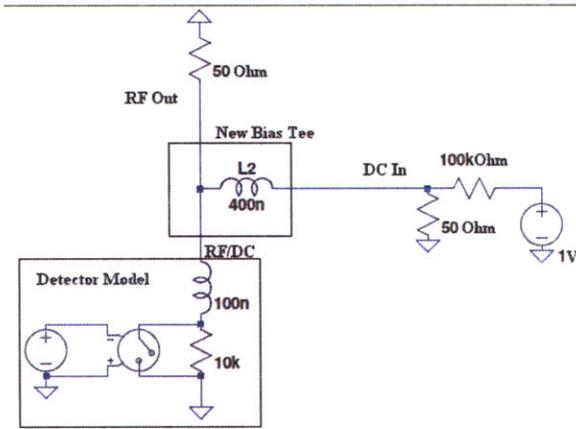


Figure 2-10: Schematic of the new bias tee design. Note that it consists only of an on-chip inductor utilizing kinetic inductance to achieve the large value. Note that we include a  $50 \Omega$  termination on the current source to simulate a low-impedance cable.

we can fabricate capacitors with values on the order of  $1\text{pF}$  or below, inductors with values on the order of  $100$ 's of  $\text{pH}$  or below, and resistors with values on the order of  $100 \Omega$  or below.[20] None of these values is large enough to create a cutoff below our required frequency of  $1\text{-}10\text{MHz}$ .

Next, if we consider the process we use to actually fabricate detectors, we observe that we cannot fabricate resistors. We cannot fabricate capacitors with significant values. However, due to the fact that the film is  $4\text{nm}$ , we measure a kinetic inductance of approximately  $80\text{pH}/\text{sq}$ . This allows us to construct  $400\text{nH}$  inductors with an area comparable to the size of the detector. Now, this will be an on-chip construction, so consider the circuit in figure 2-10.

Note that this works properly as a bias tee. Since the SNSPD has no resistance to ground, the DC current will pass entirely through the SNSPD. Also note that AC signals above the first order cutoff of  $L/R$  will pass through the amplifier. This roll-off frequency can be calculated to be  $20\text{MHz}$ .

There are several important notes to this implementation. First, since we have no capacitance in this system, we have only a first order roll-off, so the cutoff is not precise. In reality, we have nonideal behavior below  $200\text{MHz}$ .

Probably the most important to note is how we view the current source. Ide-

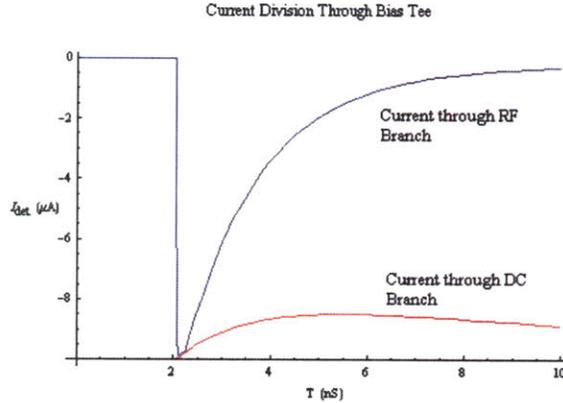


Figure 2-11: Results for simulations of the bias tee with a SNSPD detector pulse. The blue line shows the current through the  $50\ \Omega$  amplifier, and the red line shows the current lost into the current source. The original signal amplitude is  $10\ \mu\text{A}$ .

ally, this current source would be high impedance, but since we are looking at UHF frequencies and the current source is removed from the system, we cannot use this approximation. Instead, we must recognize that our probe station (where we test this circuit) utilizes a  $50\ \Omega$  probe to apply the DC bias current. Therefore, at the frequencies of interest, we will see the impedance of the cable. In addition, to practically prevent coupling too much electromagnetic noise to the system one must terminate the current source with  $50\ \Omega$ , so the above model is accurate.

This implementation immediately lends itself to multiple potential improvements. First, in the final implementation, we do not need a  $50\ \Omega$  RF coaxial line to bias the detector at DC. In reality, we only need an unshielded bias line with a ferrite bead RF choke near the detector. The RF choke will dramatically increase source resistance and decrease our cutoff frequency. This improvement is a part of the final experimental setup.



# Chapter 3

## RSFQ Theory

Rapid Single Flux Quantum (RSFQ) logic uses Josephson junctions as the switching element much like CMOS logic uses MOSFETS as the switching element. However, beyond having active elements, RSFQ and CMOS logic are dramatically different.

RSFQ circuitry is faster and uses less energy than traditional CMOS logic. This logic has been used to create frequency downconverters that operate up to 750GHz.[6] Also, basic 4/8 bit processors have been implemented that operate at frequencies of 10s of GHz.[4] However, given the cryogenic and shielding requirements for such circuitry to operate, RSFQ has never become mainstream, remaining a niche technology for specific applications. In addition, silicon CMOS technology has advanced so quickly that most speed advantages of using RSFQ have been marginalized. Currently, RSFQ only offers a factor of 3-5 speedup over mainstream CMOS technology. Therefore, it is extremely unlikely that RSFQ will ever compete with CMOS for mainstream usage. However, as it turns out, RSFQ is very well suited for developing a cryogenic readout for SNSPDs. RSFQ lends itself to this application for two primary reasons. First, our system is already cryogenic, so standard CMOS technology is not an option. Second, we can only sustain a minimal heat load, so the energy advantage of RSFQ logic makes it an excellent engineering choice.

To understand how RSFQ circuitry works, one must first understand the basics of how the Josephson junction works.

### 3.1 Josephson Junction Physics

This fundamental superconducting element is typically comprised of a superconductor-insulator-superconductor (S-I-S) stack where the insulator is extremely thin and allows quantum tunneling of Cooper pairs through the barrier. In reality, this can be any form of weak link, but we will be using oxide tunnelling to achieve this effect. Possibly the least intuitive process of Josephson junction physics is that Cooper pairs do not break before tunneling. Instead, the macroscopic phase parameter is correlated from one side of the junction to the other just as if the entire superconducting wavefunction were treated as the tunneling particle, rather than the individual wavefunctions for each electron. [21][28]

The superconducting wavefunction can be approximated as:

$$\Psi(\vec{x}) = \frac{1}{\sqrt{n^*}} e^{i\theta(\vec{x})} \quad (3.1)$$

where  $n^*$  is the density of superconducting charge carriers, and  $\theta(\vec{x})$  is the local phase of the wavefunction. Now, utilizing Ginzburg-Landau theory, we can derive the current of the macroscopic quantum wavefunction to be:

$$J_s = \frac{2q^*}{m^*} \text{Re} \left\{ \Psi^* \frac{\hbar}{i} \nabla \Psi \right\} \quad (3.2)$$

where  $m^*$  and  $q^*$  are the effective mass and charge of the carriers. For the case of a Cooper pair,  $m^* = 2m_e$  and  $q^* = 2q_e$ . Now, if we derive the wavefunction across a barrier, we can observe the current across a junction. Consider a potential shown in figure 3-1.

Now, let us consider the solution in all three sections of the potential. The solution on either side of the barrier is simply the solution given in equation 3.1.

In the barrier however, the solution becomes exponentially decaying in  $x$ :

$$\Psi(x) = C_1 \cosh\left(\frac{x}{\zeta}\right) + C_2 \sinh\left(\frac{x}{\zeta}\right) \quad (3.3)$$

where  $\zeta = \sqrt{\frac{\hbar^2}{2m^*(V_0 - E_0)}}$ . We allow different charge carrier densities  $n_1^*$  and  $n_2^*$  and

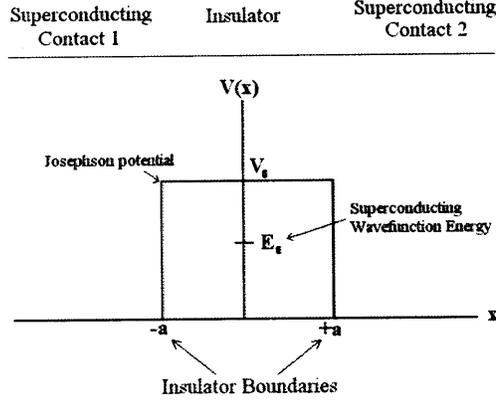


Figure 3-1: Basic Josephson junction potential. Energy of the superconducting wavefunction is given as  $E_0$ , which is less than the barrier height. Image courtesy of [21]

phases  $\theta_1$  and  $\theta_2$  on the left and right hand side of the potential, respectively. Now, we match boundary conditions and derive  $C_1$  and  $C_2$ .

$$C_1 = \frac{\sqrt{n_1^*}e^{i\theta_1} + \sqrt{n_2^*}e^{i\theta_2}}{2 \cosh(a/\zeta)} \quad (3.4)$$

$$C_2 = \frac{\sqrt{n_1^*}e^{i\theta_1} - \sqrt{n_2^*}e^{i\theta_2}}{2 \sinh(a/\zeta)} \quad (3.5)$$

Finally, we use our equation for  $J_s$  and derive the DC Josephson effect:

$$J_s = J_c \sin(\theta_1 - \theta_2) \quad (3.6)$$

where the Josephson critical current density  $J_c = \frac{e\hbar\sqrt{n_1 n_2}}{m\zeta \sinh(2a/\zeta)}$ . In real applications, we do not have exact control over the potential barrier, we generally consider  $J_c$  to be a fundamental parameter of a specific process, rather than a derived property as it is shown above.

Now, to consider a voltage across a junction, let us work backward from the answer. We will derive that a voltage creates a linear increase in phase in time, so let us consider the rate of change of the gauge-invariant phase across the Josephson junction. Let  $\Theta(t)$  be this gauge-invariant phase difference. We must subtract off a

line integral of the magnetic field to maintain gauge invariance.

$$\frac{\partial \Theta}{\partial t} = \frac{\partial \theta_1}{\partial t} - \frac{\partial \theta_2}{\partial t} - \frac{2\pi}{\Phi_0} \frac{\partial}{\partial t} \int_1^2 \vec{B}(\vec{r}, t) \cdot d\vec{l} \quad (3.7)$$

where the integral is a path integral of the vector potential from one node of the Josephson junction to the other. Now, we note the supercurrent equation at the boundaries:

$$\frac{\delta}{\delta t} \theta(\vec{r}, t) = -\frac{1}{\hbar} \left( \frac{\Lambda J_s^2}{2n^*} + q^* \phi(\vec{r}, t) \right) \quad (3.8)$$

We plug this in and cancel terms to show that:

$$\frac{\delta \Theta}{\delta t} = \frac{2\pi}{\Phi_0} \int_1^2 \left( -\nabla \phi - \frac{\delta \vec{A}}{\delta t} \right) \cdot d\vec{l} = \frac{2\pi}{\Phi_0} (V_1 - V_0) \quad (3.9)$$

Note that the above integral is an integral of the gauge invariant electric field across the Josephson junction which yields the voltage across the junction. Therefore, we have related the voltage across the Josephson junction to the time rate of change of the phase across the same junction.

In conclusion, we have derived constitutive relations for the Josephson junction:

$$I(t) = I_c \sin(\Theta(t)) \quad (3.10)$$

$$V(t) = \frac{\Phi_0}{2\pi} \frac{\delta}{\delta t} \Theta(t) \quad (3.11)$$

where  $\Theta(t)$  is the phase across the Josephson junction. If  $\Theta(t)$  is constant in time and arbitrary in value, this means that the current can take any value between 0 and  $I_c$  without developing any voltage across the Josephson junction. Note that these equations are *highly* nonlinear and not linearizable for any nonzero voltage. This is the source of the difficulty with analyzing Josephson junction circuits. This difficulty will become apparent when we try to establish a rigorous design methodology for digital circuits using this technology.

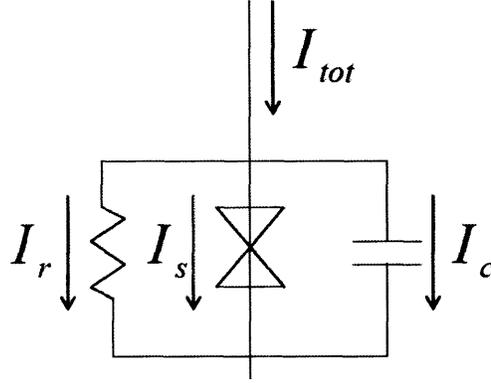


Figure 3-2: Schematic of RSJ model. Note that the element in the middle is the ideal Josephson junction with relations given by 3.10 and 3.11. The R and C elements represent unavoidable aspects of the Josephson junction.

## 3.2 Resistively Shunted Junction Model

The Resistively Shunted Junction (RSJ) model attempts to model the nonideal elements of Josephson junctions by using a shunt capacitor and resistor. The capacitor takes into account the capacitive effect that occurs with two parallel plates of superconductor with an oxide layer between. The resistive shunt tries to approximate the single-electron tunneling through the oxide barrier. The capacitive approximation is very accurate, as a junction really is just a parallel plate capacitor. However, the resistive approximation fails to approximate the subgap resistance, which will be discussed later.

Note that in the RSJ model, we can break down the overall differential equation governing behavior into the following:

$$I_{tot} = I_c \sin(\theta) + \frac{1}{R} \frac{\Phi_0}{2\pi} \frac{\partial}{\partial t} \theta + C \frac{\Phi_0}{2\pi} \frac{\partial^2}{\partial t^2} \theta \quad (3.12)$$

which looks exactly like the differential equation for the full nonlinear dynamics of a pendulum.

$$\Gamma = mgl \sin(\theta) + b \frac{\partial}{\partial t} \theta + ml^2 \frac{\partial^2}{\partial t^2} \theta \quad (3.13)$$

Note that in this analogy, the capacitance becomes a ‘mass’ term, resistance becomes the ‘damping’ term, and  $I_{tot}$  becomes equivalent to a ‘torque.’ With this analogy, we can understand the dynamics of how a current affects the phase. Now, consider with the pendulum analogy what happens if we have a heavily overdamped system. Mechanically, the damping term corresponds to frictional resistance at the pivot, while for Josephson junctions, it corresponds to a small shunt resistor.

If we give the pendulum a ‘torque’ that is small enough, the system will reach some steady state angle  $\theta$ . This angle must be less than  $\pi/2$ , as gravity provides the strongest force at this angle. If any more torque is added to this ‘critical torque’, it will cause the system to oscillate. This ‘critical torque’ is the same as the critical current of a Josephson junction. A bias current in excess of the critical current will cause the phase of the junction to oscillate in the same way as the pendulum.

Now, if we bias the junction close to its critical current, this picture is analogous to providing torque slightly less than that which is required to make a pendulum oscillate. Now, in the mechanical picture, if one gives the pendulum a small kick, the pendulum rotates by  $2\pi$  and returns to its original position without rotating further (assuming overdamping).

With the Josephson junction, an analogous event occurs. We bias the junction very close to its critical current, apply a small voltage pulse, and observe an output voltage pulse resulting from the phase changing by  $2\pi$ . Note that this pulse has an area of  $\Phi_0$  and also corresponds to a single magnetic flux quantum passing through the Josephson junction. These pulses will be the basis of RSFQ logic.[13][17]

One important note that has been alluded to is that the RSJ model is far from perfect. This error manifests itself in the shunt resistance. We are approximating this shunt resistance as a pure ohmic resistor. This models a single-electron tunnel junction with a constant density of charge carriers, and is far from completely accurate. In reality, with  $V > 0$ , there is a strong nonlinear current dependence below  $V_g = I_C R_n$ , where  $R_n$  is the normal (Ohmic) resistance at higher currents. This nonlinear resistance is called the subgap resistance ( $R_{sg}$ ), and is usually very large.[17]

However, this nonlinear dependence does not affect analysis for RSFQ circuits. Since we only want each junction to rotate by a single  $2\pi$  increment for each input voltage pulse, all of our junctions must be critically damped. A Josephson junction with no external shunt resistor has a large  $R_n$ , and is generally underdamped. Therefore, we must explicitly add a much smaller shunt resistor in parallel with the junction. When we do this, any nonlinearities, and especially the large  $R_{sg}$  are completely irrelevant for any analysis since the shunt resistor is so much smaller.

Also, note that in our constitutive relations we consider a current density. As a result, the Josephson junction area will be directly proportional to the critical current of the junction. Since we have no control over the process itself, we must rely on scaling the area of the junction to effectively fabricate junctions with different critical currents. The area of a junction is a function of the layout parameters. Therefore, the quality of area definition becomes the primary limiting factor on the sizes of junctions and their matching characteristics.[29]

### 3.3 RSFQ Definition

The interesting characteristic of the above physical processes is that they take place on a very short timescale. Generally, it takes on the order of 10 ps for the  $2\pi$  flip of a single Josephson junction. Therefore, it seems intriguing to build logic that utilizes this phase flipping mechanism due to the speed with which it occurs. However, one must note that there are no constant voltage/currents to represent ‘1’ or ‘0’. Instead, we define a new information token:[13]

A clock signal is a train of SFQ pulses. If a SFQ pulse is received at an input port between two clock signals, that is interpreted as a ‘1’. No pulse is interpreted as a ‘0’.

Immediately, one notices that since we have no constant voltage/current, the design methodology for RSFQ circuits is dramatically different than standard CMOS circuits. For CMOS, it seems clear that two or more FETs in parallel will produce an AND gate, etc. However, logic design turns out not to be this simple for RSFQ.

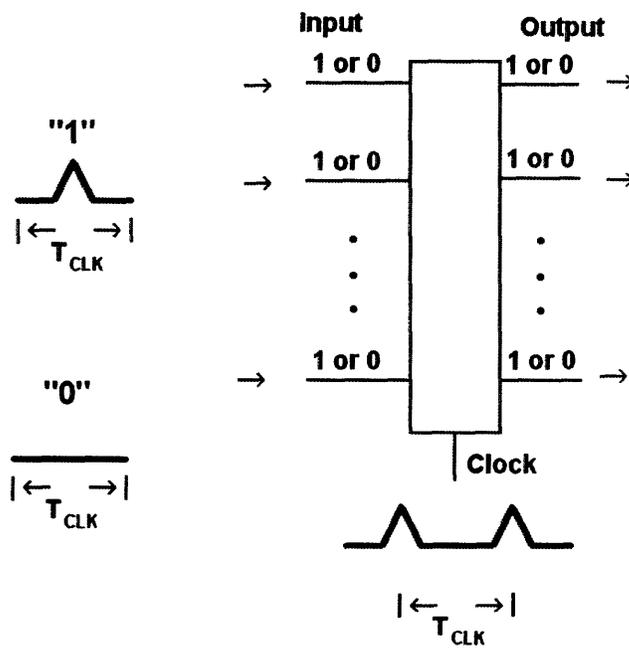


Figure 3-3: Figure of information token for RSFQ circuits. First, we define our clock as a train of SFQ pulses with period  $T_{CLK}$ . We then define '0' and '1' as either the presence or absence of a pulse in between two clock pulses.

# Chapter 4

## RSFQ Cell Design

With an understanding of Josephson junction physics and the information token of RSFQ logic, we can now develop the circuits necessary for building a complex digital circuit. We first discuss the design of each of these cells individually. We then combine these cells into full experiments to test specific cell functionality and device parameters.

RSFQ design is unlike standard MOSFET digital design in that it does not have a well-established design process to follow. Since the Josephson junction is very nonlinear, and we are exploiting these nonlinearities to perform digital logic, the best approach is to build basic cells that are easily understandable with a knowledge of Josephson junction physics and subsequently tie these cells together.

Most of these cells are based on the cells provided by SUNY RSFQ website with modifications in bias conditions, topology and Josephson Junction size.[5] All resistors are of resistance  $1 \Omega$  unless otherwise noted.

### 4.1 Josephson Transmission Line (JTL)

The JTL is the simplest SFQ circuit element. It simply acts as a buffer that transfers SFQ pulses from one side to the other. We bias both of the junctions to an identical bias current close to their critical current. Then an incoming SFQ pulse will cause one junction to switch, which propagates the pulse the second junction, which outputs it

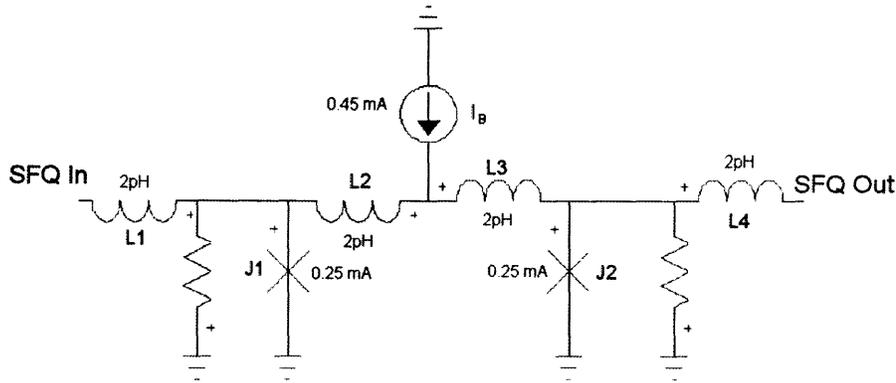


Figure 4-1: Schematic of the JTL stage. Input and output is labeled, but the stage is symmetric; an SFQ pulse can propagate in either direction.

at the other end. Note that due to symmetry, SFQ pulses can move in either direction along the transmission line. This circuit element, although simple is extremely important in SFQ circuits. One of the primary problems in SFQ circuit design is flux trapping. Flux trapping is caused by parasitic inductance between stages which in turn allows flux to be trapped between the stages without causing current greater than  $I_c$  of the Josephson Junctions of either stage. The JTL first allows one to break up this series inductance. Also, the JTL acts as a digital buffer. It will sharpen and amplify incident SFQ peaks to be exactly  $\Phi_0$  in area and filter noise that is below this threshold.

## 4.2 SQUID Comparator

This cell is simply a critically damped SQUID (Superconducting Quantum Interference Device) used to measure the current in the incoming line. I chose a lambda parameter of 1 (one flux quantum capable of being stored in the inductor before  $I_c$  of the junctions are exceeded). Note that the input stage has a  $50 \Omega$  termination. Note that we typically avoid inductive loads on the SNSPD because it tends to increase the  $L/R$  reset time of the detector. However, in this case the inductance is acceptable, as the input transformer inductance is on the order of pH, while the kinetic inductance

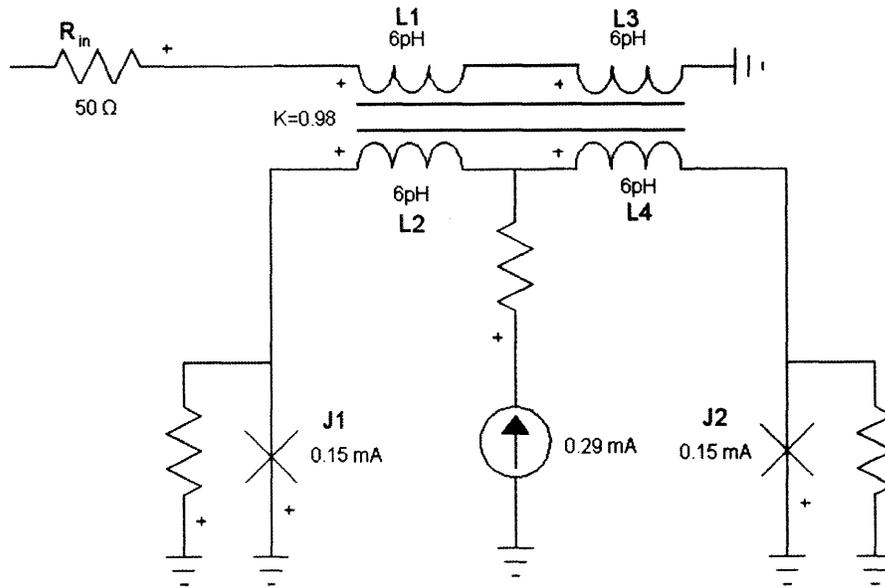


Figure 4-2: Design schematic of input SQUID comparator. Note that there is a resistive divider at the input which provides a  $50\ \Omega$  termination. This termination is not completely necessary, as it will be located close to the detector. However, it does serve to remove any potential ringing due to parasitic capacitance causing an underdamped LC circuit.

of the SNSPD itself is on the order of 100's of nH. Therefore, this inductor will have no real effect on the reset time of the SNSPD.

This stage effectively acts as a current comparator. Any increase in current from the input will induce a circulating current in the SQUID loop. This circulating current will result in the critical current being exceeded for one of the junctions. This produces SFQ pulses at the output. Note that the rate and number of SFQ pulses depends sensitively on the magnitude and duration of the current pulse. Therefore, we will have to make sure that these multiple pulses are not interpreted as multiple photons by using a D flip flop gate.

### 4.3 D Flip Flop

This stage is first comprised of an input Josephson buffer (I1, J1). Initially all of the bias current from I1 passes through J1. An incident SFQ signal pulse will result in a

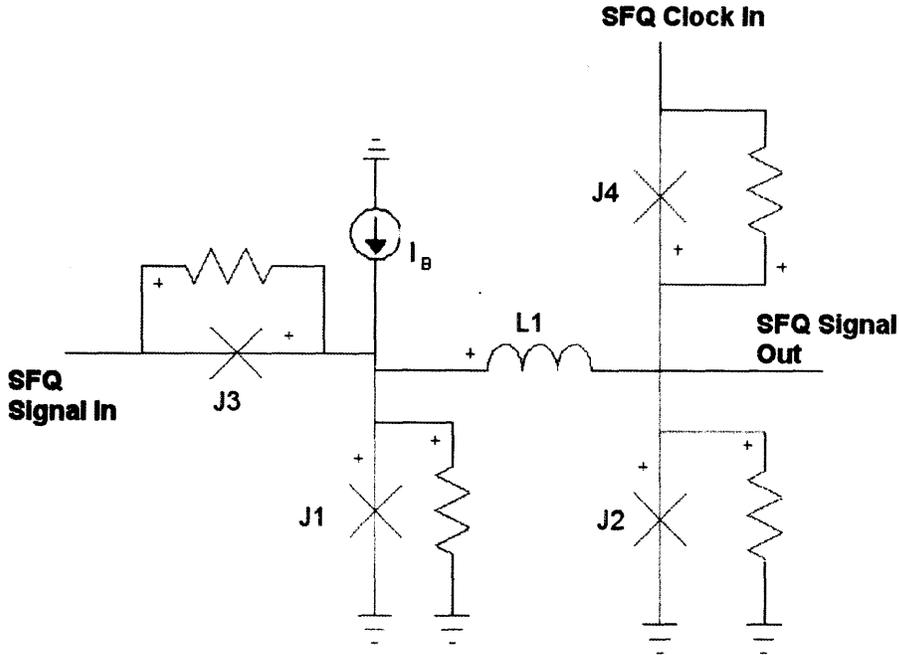


Figure 4-3: Schematic of the D Flip Flop Stage. This stage functions by trapping a fluxon in L1 when a pulse inputs from the input and releasing it with a clock pulse.

flux quantum being trapped in the J1,L1,J2 loop. Any additional input SFQ pulses simply pass through J1 to ground. A clock pulse occurring after a flux quantum is trapped in the above loop will exceed the critical current of J2, resulting in a SFQ pulse at the output. SFQ pulse. However, if there is no trapped fluxon, the clock pulse simply passes through J2, and nothing is observed at the output. J3 and J4 serve as directional buffers that prevent SFQ pulses from propagating backwards through the circuit.

Table 4.1: Values of electrical components for the D flip flop

Inductor	Value (pH)	Junction	$I_c$ (mA)	Current	Value (mA)
L1	10	J1, J2	0.25	I1	0.24
		J3, J4	0.27		

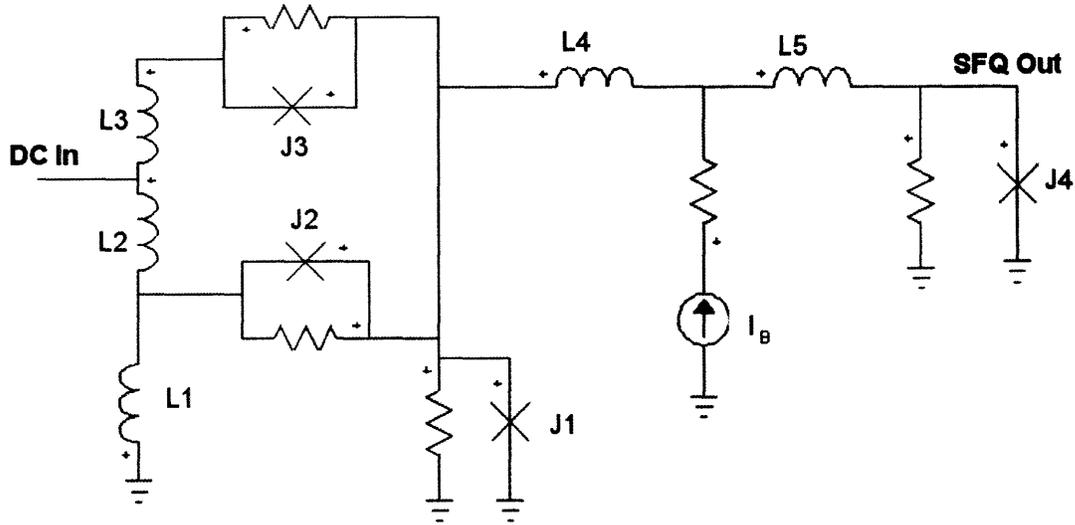


Figure 4-4: A design schematic for the DC to SFQ converter. J1-J3, L1-L3 are effectively a hysteretic comparator, while L5, L6, and J4 are an output JTL buffer.

## 4.4 DC to SFQ converter

This converter is effectively a SQUID comparator formed by J1-L1- (J2,J3). J2, J3, L2, L3 act as a single junction initially, splitting the input current and passing it through J1. The bias current also splits to J4 (which is basically an extra JTL) and J1. When the input current is large enough, the critical current of J1 is reached, causing a flux-antiflux pair to be produced. One is passed up to the output Josephson transmission line (JTL) stage. The other is maintained in L1. Note that before this switch, *all* of the current (both input and bias) passes through J1. After the switch, note that when the input current is switched, the current through L2 simply passes down L1. The current through L3 must pass through J3, J2 and then L1. The bias current passes through J2 and then L1. Therefore, as long as the input current stays constant, the bias current and one half of the input current flow through J2. When the input current decreases, the current through L1 stays constant, and more current must be drawn through the L1-J2-J1 loop. If one decreases the input current far enough, the critical current of J2 is reached, and the system resets, also pumping a single fluxon through the JTL.

Table 4.2: Values for electrical components in the DC/SFQ converter.

Inductor	Value (pH)	Junction	$I_c$ (mA)	Current	Value (mA)
L1	3.6	J1, J3	0.17	$I_B$	0.35
L2, L3	1.0	J2	0.13		
L4	1.1	J4	0.22		
L5	1.6				

## 4.5 SFQ to DC converter

This converter is based off of a ‘T’ Flip Flop. All bias currents are at 0.2 mA. This configuration has two stable states (0 and 1): with and without a flux quantum trapped in the J7-L4-L6-L7-L5-J6 loop. In the 0 state, some current from I2 flows through J3-J2-L1-J4-GND. The circulating current causes J2 to switch, blocking the SFQ from propagating upwards. The SFQ then switches J5 and J7, trapping a fluxon in the above mentioned loop (approx 0.4 mA through L9).

In the 1 state, some current flows through J8. This exceeds the critical current of J9, which continuously pumps SFQ pulses the output. Also, in the 1 state, the current through the J2-J3 column is reversed, so an incoming SFQ pulse now switches J3 and propagates upward, switching J4 and J6, returning the cell to the 0 state.

In the toggled state, the SFQ pulses are then passed through through the output. In reality, the output will resemble a low-pass filter, which simulates the loss of the exterior electronics. Roll-off characteristics for the probe are close to 1GHz. These output capacitances will only affect the maximum clock speed at which we can read the output and have no effect on the actual functionality of the circuit.

Also, it is important to note that the output of this stage is on the order of 0.1-1 mV. This signal needs to be amplified similarly to the original SNSPD signal. However, we now have control over the output waveform. Also, the digital system is resistant to any amplifier noise. Finally, we can combine multiple SSPD outputs into a single serial line.

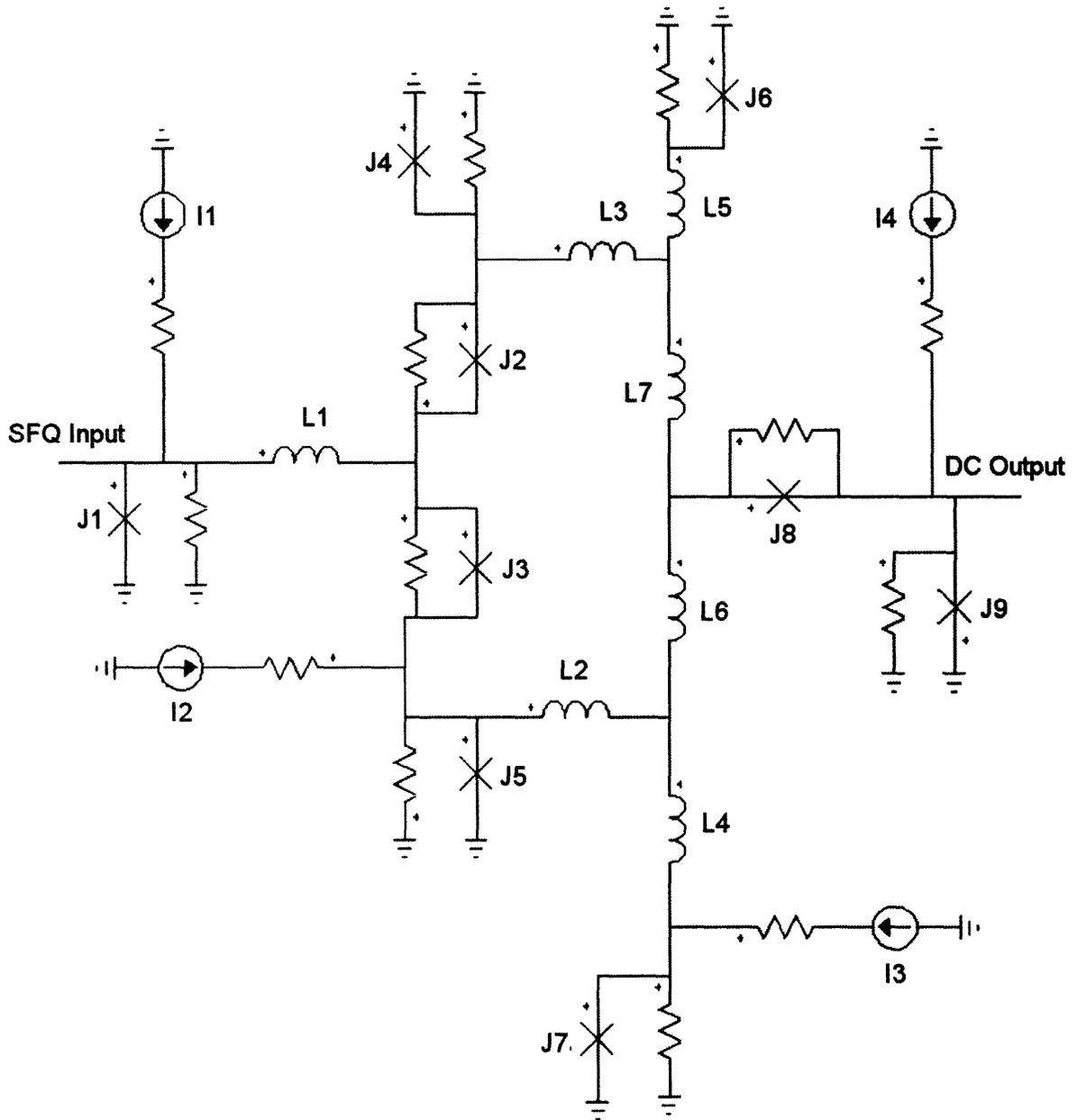


Figure 4-5: Schematic of SFQ/DC converter. Effectively, we have an input JTL (J1) which goes to a T Flip Flop (J2-J7). In the 1 state, the output exceeds the critical current of J9, which produces a series of SFQ pulses at the output. This yields a small DC voltage when low-passed.

Table 4.3: Values for electrical components in the SFQ/DC converter.

Inductor	Value (pH)	Junction	$I_c$ (mA)	Current	Value (mA)
L1	1.2	J1	0.30	I1	0.20
L2	1.3	J2, J3	0.22	I2	0.20
L3	0.85	J4, J5	0.17	I3	0.20
L4	1.1	J6, J7	0.34	I4	0.23
L5	1.9	J8	0.13		
L6	2.0	J9	0.22		
L7	1.9				

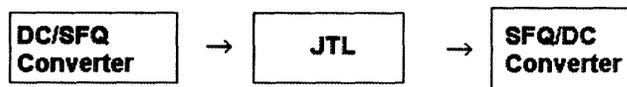


Figure 4-6: Block diagram for the ‘Brahman’ experiment. This is the most basic RSFQ circuit that we will design. We will utilize this circuit as a baseline and testbench for manipulating bias and environment parameters.

## 4.6 Experimental Configurations

Now that we have some basic RSFQ cell designs, we can design test circuits and the final readout circuitry. We have chosen to take an incremental approach to this design, breaking our design into four smaller incremental experiments.

A diagram for our first experiment, Brahman, is given in figure 4-6. This circuit is the simplest SFQ circuit possible. It converts a DC signal to SFQ pulses, buffers these pulses with a JTL, and converts this back to DC to be measured.

This circuit, although basic, will act as a baseline for the remainder of our SFQ circuits. We will utilize this circuit to measure baseline tolerance parameters in the bias currents. We will utilize this circuit to characterize failure modes, such as failure due to flux trapping or our-of-design range input current.

Our second experiment, Brangus, is shown in figure 4-7. This circuit contains each of the elements in Brahman plus a single D flip flop. This flip flop acts as a memory element, storing the presence or absence of an incident flux quantum. We will utilize this circuit to characterize the stability of this memory. If we have significant flux

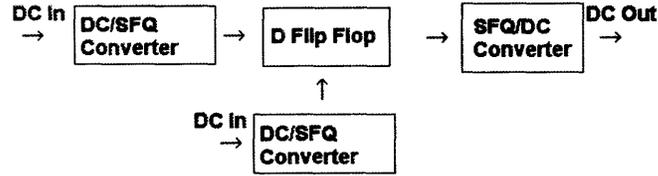


Figure 4-7: Block diagram for the ‘Brangus’ experiment. This circuit implements a memory element, the D flip flop. We will utilize this circuit to test the memory lifetime capabilities of RSFQ circuits.



Figure 4-8: Block diagram for the ‘Hereford’ experiment. This circuit implements our SQUID comparator at the input. We will utilize this circuit along with some standalone SQUIDS to characterize this input stage.

noise due to some design failure, our memory lifetime might be unacceptably short. In addition, we will be able to characterize failure modes of the D flip flop, just as is possible with Brahman.

Our third experiment, Hereford, is shown in figure 4-8. This circuit is designed to test the SQUID comparator input stage designed to interface to the SNSPD. Using this circuit and standalone SQUID devices, we will be able to characterize the necessary bias conditions and their tolerances for photon detection.

Our final experiment, Texas Longhorn, is shown in figure 4-9. This circuit can work as a full synchronizing readout for a single SNSPD. We will first verify that this circuit functions as expected utilizing room temperature electronics. We will then connect this circuit to an SNSPD to complete the readout.

Each of our circuits is designed to test a specific part of the RSFQ functionality. Given that we have little recent RSFQ experience, we must build up our technology rigorously. Once we have verified the above circuits, we can utilize the cells described above on any future RSFQ design with confidence.

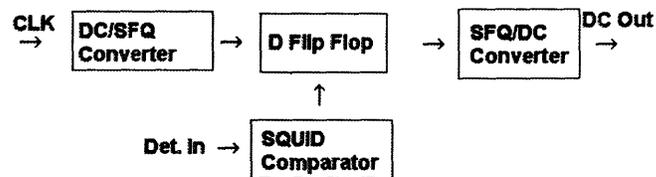


Figure 4-9: Block diagram for the ‘Texas Longhorn’ experiment. This circuit can act as a fully functional readout for a single SNSPD. We will test this circuit first to ensure functionality. Next, if all is functional, this circuit will be interfaced to the SNSPD.

# Chapter 5

## RSFQ Simulations

One of the most fundamental and necessary parts of the modern integrated circuit design process is the ability to simulate circuits. Modern circuit topologies are far too complicated to realistically expect hand calculations to be feasible. In addition, non-linear elements such as the MOSFET or Josephson junction are exceedingly difficult to handle analytically.

Therefore, we used the WRSpice software package to simulate RSFQ logic and ensure that our design parameters result in a functional circuit.[30] However, it is much more difficult to consider the interaction between Josephson junctions and SNSPD's. The Josephson junction model is fairly well established, but the SNSPD model is a full thermoelectric model not accurately described by any reasonable constitutive relationships between voltage and current.

### 5.1 Front-End Simulations

To accurately simulate the interaction between SNSPDs and Josephson junctions such as is the case in our analog front-end circuit, we must take a much more general and powerful approach by utilizing Matlab's Simulink software, which numerically solves general ODE's and algebraic systems.

Simulink comes equipped with circuit solving capability, so we utilized this functionality as a base on which we built custom electrical components.

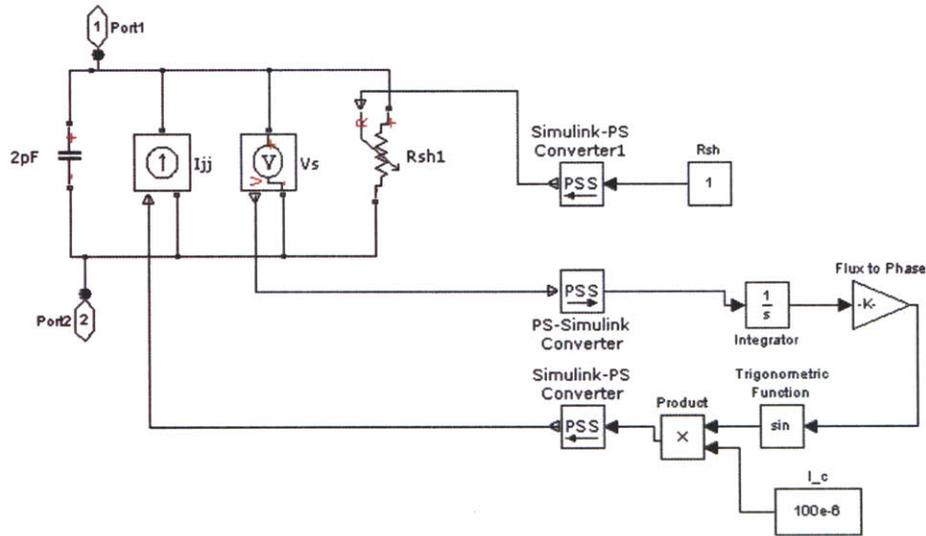


Figure 5-1: Simulink model for a Josephson junction. We use the RSJ approximation and include the presence of an external shunt resistance in the model. Each of our junctions is shunted with approximately  $1\Omega$ .

### 5.1.1 Simulink Implementation of RSJ Model

The first task was to construct an effective Josephson junction model. As explained in the section on RSFQ theory, we are simulating digital RSFQ circuits, so we can use the RSJ model without too much concern as to the inaccuracies of the model.[28]

We have chosen to source current and measure voltage only due to ease of implementation. It is also possible to reverse the source/measurement, but one has to be more careful with the terms, as one must use  $\arcsin(I/I_c)$ .  $I/I_c$  can fall outside the domain of  $[-1, 1]$  due to numerical errors or improper initial conditions.

In addition, this Josephson junction model unlike the SNSPD model does not require any specific timing. Even though we have a feedback loop between the electrical circuit and the Simulink processor, this process will work (to some accuracy) independent of the timing choices made in the ODE solver.

To demonstrate the robustness of this model, we have implemented a DC/SFQ solver to match functionality with simulation results from WRSpice. This complicated circuit goes beyond simple AC/DC Josephson effects and demonstrates that we can

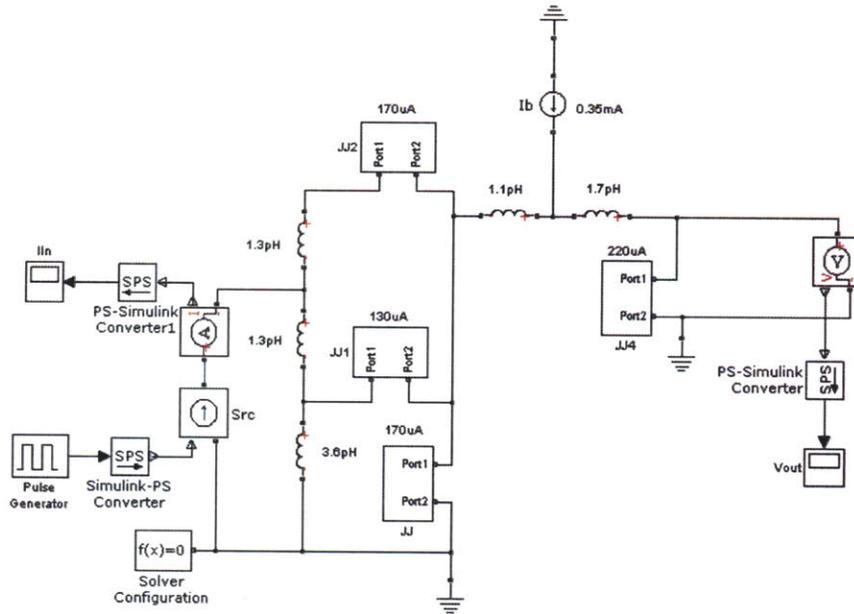


Figure 5-2: Simulink construction of a DC/SFQ converter. We will perform most of our digital simulation in WRSpice, as it uses more accurate models and is designed for layout. However, our RSJ model suffices to describe basic RSFQ circuits.

make accurate predictions with our Simulink model as to the behavior of our RSFQ circuits.

### 5.1.2 Combined SNSPD-RSJ Model

The primary advantage to the Simulink software is generality of the platform. By using this platform, we can combine multiple types of models, such as our SNSPD and Josephson junction model. In figure 5-4, we have fully designed the SNSPD, bias circuitry, and input stage of the RSFQ readout.

We use the full thermoelectric model for the SNSPD, the updated bias circuitry, and the SQUID input stage for the RSFQ readout. Note that the input bias circuitry is a  $100\text{ k}\Omega$  terminated source, but there is an additional  $50\Omega$  termination to ground. This shunt resistance simulates a worst-case approximation that is due to the fact that at high-frequencies, detector pulses will see cable impedance, rather than the impedance of the current source. Such a termination ensures that the bias tee alone

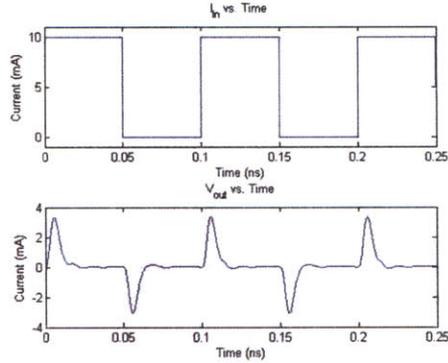


Figure 5-3: Simulation results for the DC/SFQ converter. This Matlab simulation accurately reflects the results given in WRSpice, demonstrating the robustness and capability of our model.

routes the high-frequency signal to the RSFQ detector, rather than relying on the impedance of the current source.

One can also worry about an impedance mismatch here, but our bias tee is designed such that all frequencies high enough such that mismatch is becomes a serious problem are filtered to the on-chip RSFQ circuitry.

Note that the magnetic coupling to the SQUID utilizes two 6pH inductors. This small size is excellent both for enabling proper impedance matching at the source, and for preventing digital switching noise from propagating back to the detector.

We have simulated the above system, and results are plotted in figure 5-5. The photon arrives at  $t = 0.1$  ns, and one observes a dramatic increase in  $R_{\text{det}}$  and the corresponding drop in  $I_{\text{det}}$ . The center plot demonstrates the output voltage from the SQUID. Note that as soon as the detector fires, we begin to observe a train of SFQ pulses.

This comparator will generate this train of pulses as long as current is being rerouted through the transformer. Also, the rate of pulses is proportional to how much current is rerouted. This pulse-train behavior can be observed in figure 5-5 as the pulses space out as current returns to the detector.

It is very important to mention that we are biasing the SQUID as  $198\mu\text{A}$  precisely, where  $I_c = 200\mu\text{A}$ . We use this level of precision primarily for demonstration to show

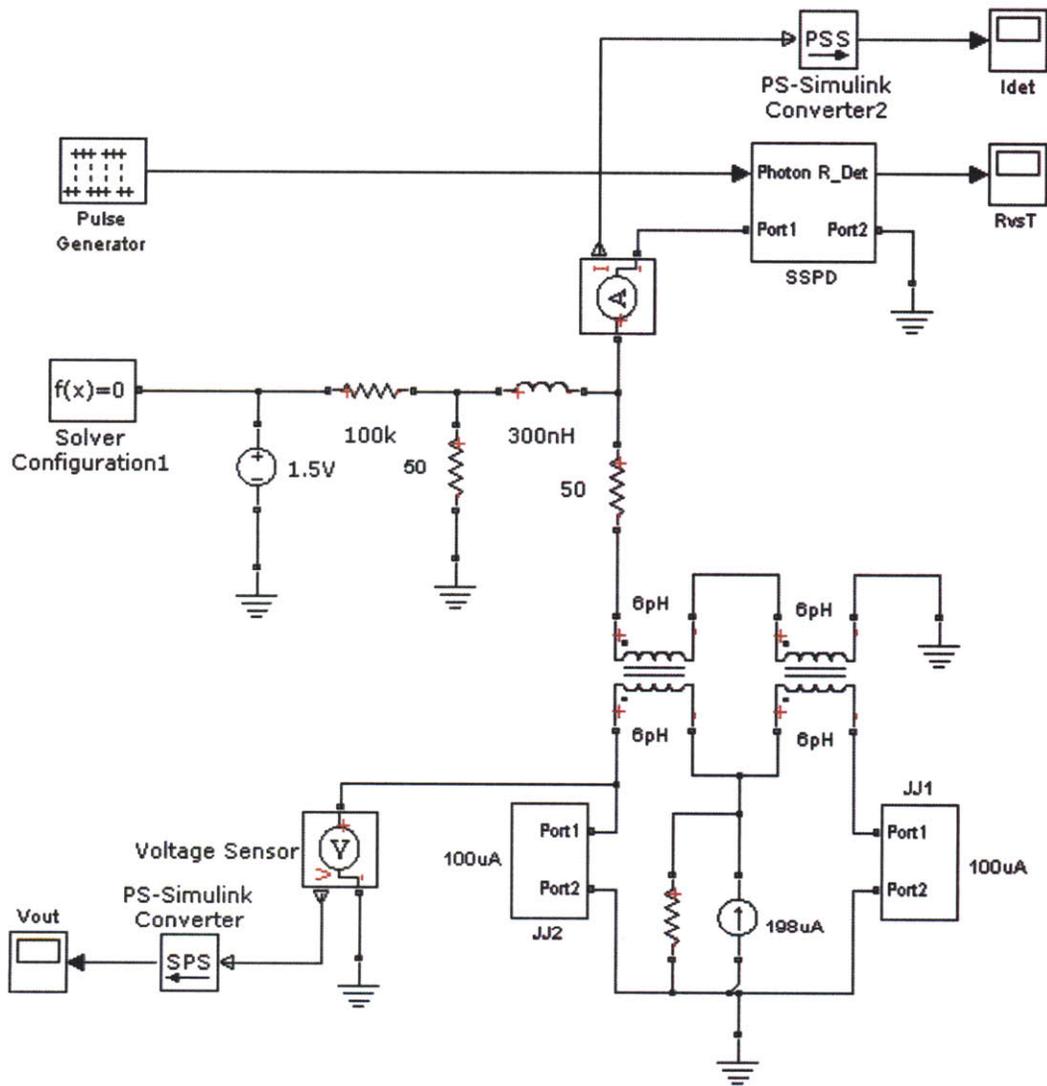


Figure 5-4: Simulink model of the complete SNSPD and input stage to RSFQ. Note that we have included the newly designed bias tee as the splitter. Finally, the input stage consists of the magnetically coupled SQUID that we read out.

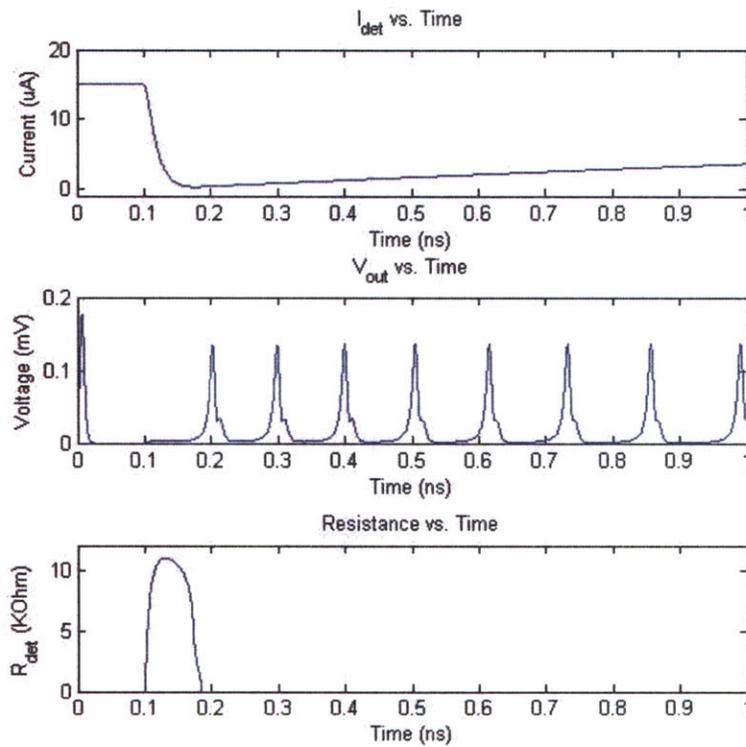


Figure 5-5: Top: detector current; Middle: SQUID output voltage; Bottom: Detector Resistance. Note that as the detector fires, we observe multiple SFQ pulses being produced by the SQUID comparator. This occurs because we have biased the SQUID very close to its critical current, so we exceed the critical current by a larger amount, creating a rapid train of SFQ pulses.

a rapid pulse train. It is not practically a good design choice to bias this close to the critical current, as current noise as well as layout mismatching may become important. A decrease in bias current results in a slower pulse train, which is perfectly acceptable, and desirable in many cases (so that one does not accidentally count one photon twice).

Also, although we are producing a rapid pulse train, the final design has this pulse train gated by a D flip flop. This circuit measures the presence/absence of a SFQ pulse. If more than one SFQ pulse arrives at the input between clock cycles, this is still treated as a '1'. Therefore, a rapid pulse train will not cause the circuit to miscount unless the photon is incident within a few nanoseconds of a clock cycle, causing the pulse train to overlap with the clock pulse. The probability of this overlap is very low for the count rates we are interested in.

## 5.2 Logic Simulations

Since we need to both design and layout circuits, we have used WRSpice to perform the remainder of our circuit simulations. WRSpice uses an extended RSJ model which accounts for subgap resistance and nonlinearities near the transition.[30][17] More importantly, however, WRSpice allows us to forward and reverse check our layout with the design schematic. After physically laying out an inductor, Josephson junction, or resistor, we can extract an estimated value from the layout and update our design schematic.

We have done this for all four of our circuits and re-simulated each with the updated schematic information that more accurately reflects layout parasitics. Each of these simulations is summarized in figures 5-6 5-7 5-8 5-9.

In addition to verifying functionality, we can also utilize WRSpice to set tolerances on specific components or bias settings. In most of these cases, design parameters are  $\pm 10\%$ . However, there are a few notable exceptions. First, the SQUID comparator will be the most sensitive part. This sensitivity will be primarily localized to the stability of the bias current. The bias current must be within the SNSPD detector

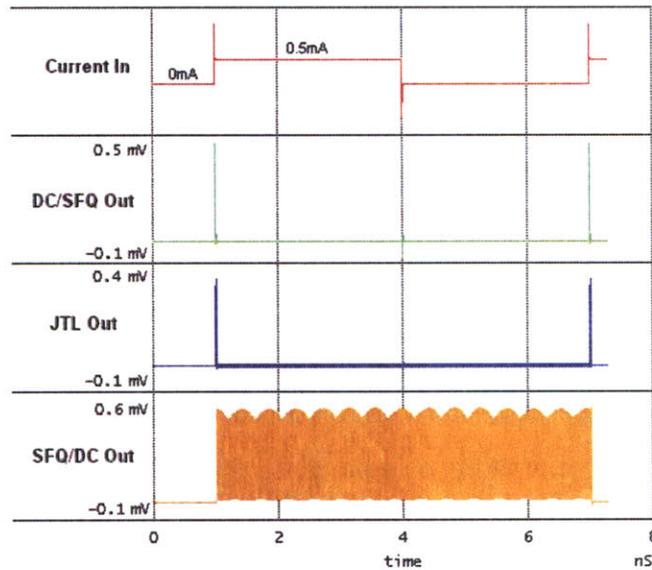


Figure 5-6: Simulation results for the ‘Brahman’ test circuit. If this circuit functions properly, an input current square wave will result in SFQ pulses causing the DC/SFQ converter to produce a DC output. Note that because the DC/SFQ converter is effectively a T flip flop, the output frequency will be 1/2 of the input frequency.

critical current of the SQUID critical current. For example, if the detector critical current is  $10\mu\text{A}$ , and the SQUID critical current is  $200\mu\text{A}$ , the bias current must be between  $190\mu\text{A}$  and  $200\mu\text{A}$ . The closer one is to the SNSPD critical current, the more sensitive the comparator is to detector pulses. The level of bias current is therefore a tunable parameter, but must be controlled precisely to be effective. Currently we are biased  $5\mu\text{A}$  off of the critical current.

This bias current is most likely a parameter that will have to be tweaked due to differences between fabrication and simulation. Therefore, we have fabricated multiple SQUID input stages to observe how each behaves and how significant the variation is between each.

In addition, this simulation has been used to verify that the series inductance between stages is not too high. This inductance leads to flux trapping between stages. In initial designs, the SQUID output and flip flop input had a tendency to trap flux. Redesign and simulation rectified these problems.

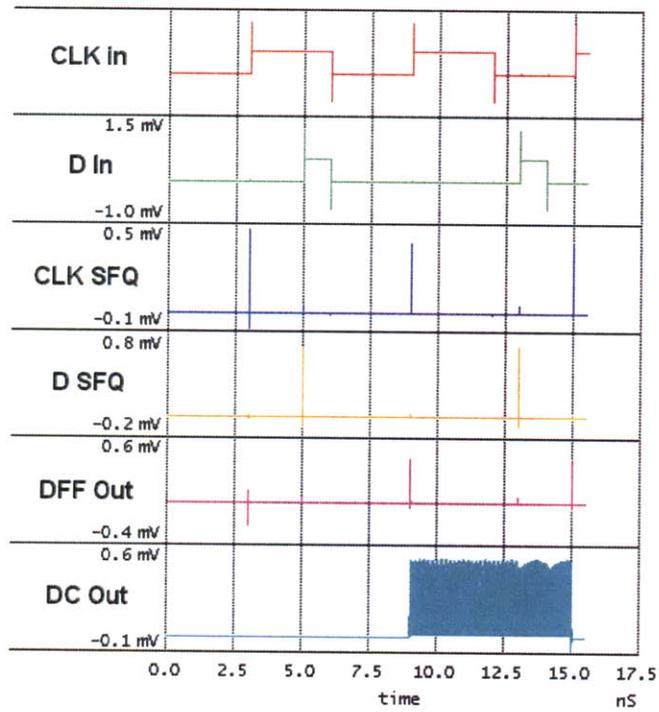


Figure 5-7: Simulation results for the ‘Brangus’ test circuit. The top four traces reflect the input signals and their respective SFQ pulse trains. ‘D SFQ’ goes to the D port of the flip flop, and when the next clock pulse arrives, we observe an SFQ pulse at the flip flop output. This then toggles the SFQ/DC converter.

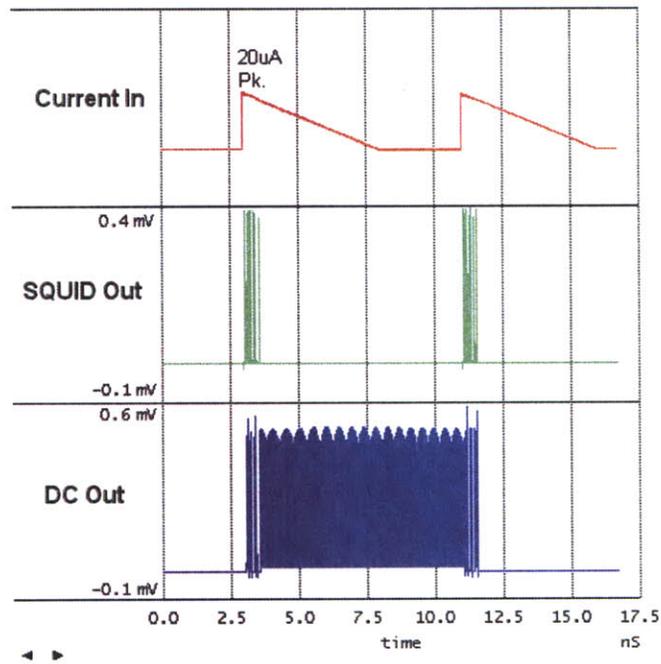


Figure 5-8: Simulation results for the 'Hereford' test circuit. Note that we have tried to mimic the detector current input by having a  $20\mu\text{A}$  peak pulse input with decay time on the order of 10nS. This current profile roughly matches that of the detector. We observe the predicted pulse train from the SQUID, and these toggle the SFQ/DC converter.

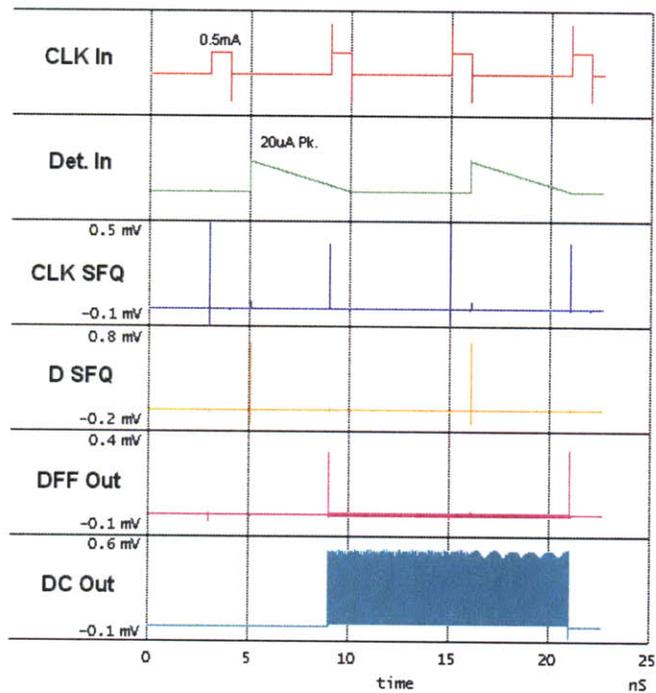


Figure 5-9: Simulation results for the ‘Texas Longhorn’ test circuit. The top four traces are input stage signals and their respective SFQ pulses incident on the flip flop. Flip flop and SFQ/DC output pulses are given. Note that the D flip flop gates multiple pulses from the SQUID comparator stage.



# Chapter 6

## Parallel SNSPDs

Recently, our group has begun to explore more complex topologies than a single SNSPD wire. One such alternative has been the parallel nanowire detector. Instead of a single nanowire, one fabricates a larger number of nanowires in parallel. When one nanowire detects a photon, current is rerouted through the other detectors, causing an avalanche switching mechanism.

### 6.1 Advantages of Parallel Detectors

The advantages of a parallel detector stem from the advantages of smaller detectors. Traditionally, we desire fast switching speed, which is governed by the kinetic inductance ( $L/R$ ) reset time of the detector. Smaller detectors have smaller kinetic inductances, leading to faster reset times and therefore faster possible count rates.[14][32]

However, the demand for fast count rates must be balanced by the demand for large detector active area. With a larger active area, more photons can be absorbed, and applications such as imaging become more feasible. Size and speed are traditionally engineering tradeoffs for single detectors.

However, it seems possible to achieve the same count rates with larger active areas by having multiple detectors in parallel. In this case, one can utilize multiple smaller detectors to cover a larger area.

Another potential advantage of such a system is that traditionally, smaller (nar-

rower) wires are more difficult to read out because they have lower  $I_c$ , resulting in a smaller voltage pulse when they are activated. If one uses multiple narrow-nanowire detectors in parallel, this problem is mitigated, because the avalanche signal is the sum of all the signals of each detector. This combined signal is substantially easier to read out since the voltage amplitude and SNR is higher.

## 6.2 Simulations

The catch to such a system is that as the topology increases in complexity, so does the analysis. Although we are utilizing multiple separate SNSPD elements, their interaction is nontrivial. However, in an effort to understand readout of SNSPD devices, we have developed a Simulink model for SNSPD devices that is robust enough to be incorporated in an arbitrary electrical network (See Appendix B). Therefore, we can actually simulate these complex interactions directly utilizing Matlab’s Simulink software.

There are two specific properties that are of direct importance to the implementation of parallel SNSPD detectors. First, we need to characterize the ‘avalanche current’ ( $I_{av}$ ).  $I_{av}$  is the current at which a photon-induced hotspot on a single wire will cause the other detectors to switch as well. This value of this current is relatively easy to understand, but we will verify these results.

In addition, we have simulated and now understand a transition ‘oscillating’ regime which exists just above the theoretical avalanche current. To simulate this, we constructed the circuit in figure 6-1

For this setup, we have two detectors with equal inductances (160nH), and slightly varying critical currents ( $6.7\mu\text{A}$ , and  $7.3\mu\text{A}$ ). We bias the system at  $9\mu\text{A}$  total. Note that we expect the system to avalanche if the current rerouted from one detector will cause the other detector to switch. That is clearly the case here.

We trigger a photon detection event at the start of the simulation, and we measure the following results shown in figure 6-2. Note that the system oscillates due to the fact that the current from the SSPD1 does not cause SSPD2 to switch immediately.

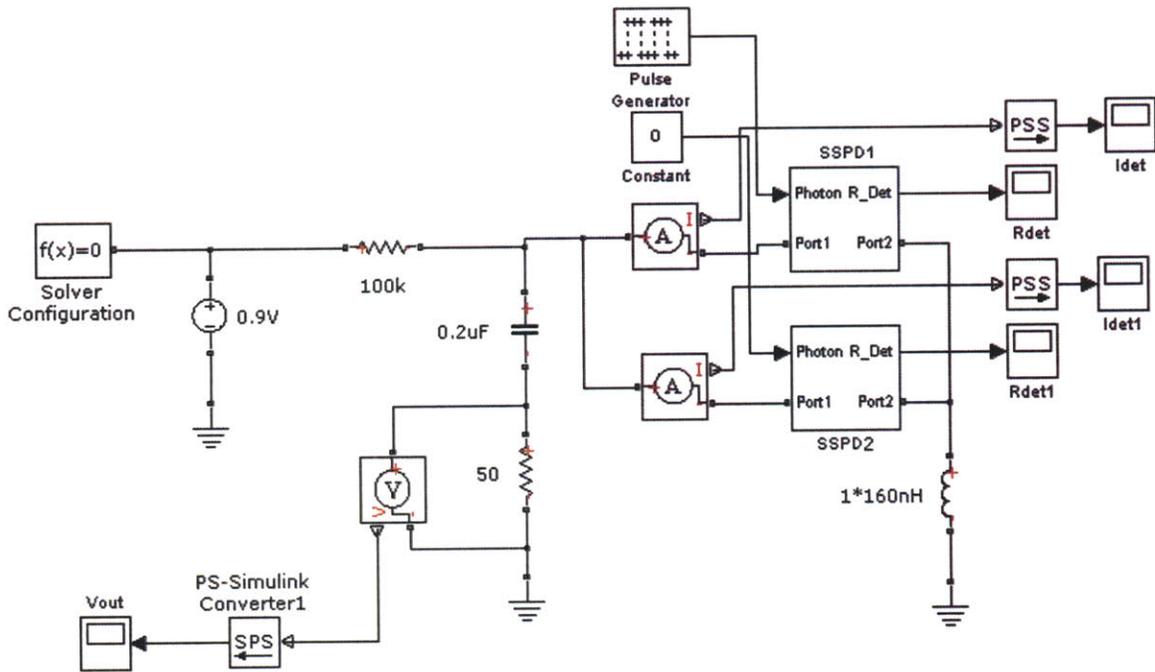


Figure 6-1: Simulink setup for the parallel nanowire simulation. Individual detector currents and resistances are shown in dashed/solid, respectively. Note that each 4-port box contains a full thermoelectric model for the SNSPD. We also tie an inductor to ground in series with the detector. This is a deliberately fabricated part that aims to maintain constant current in the detectors.

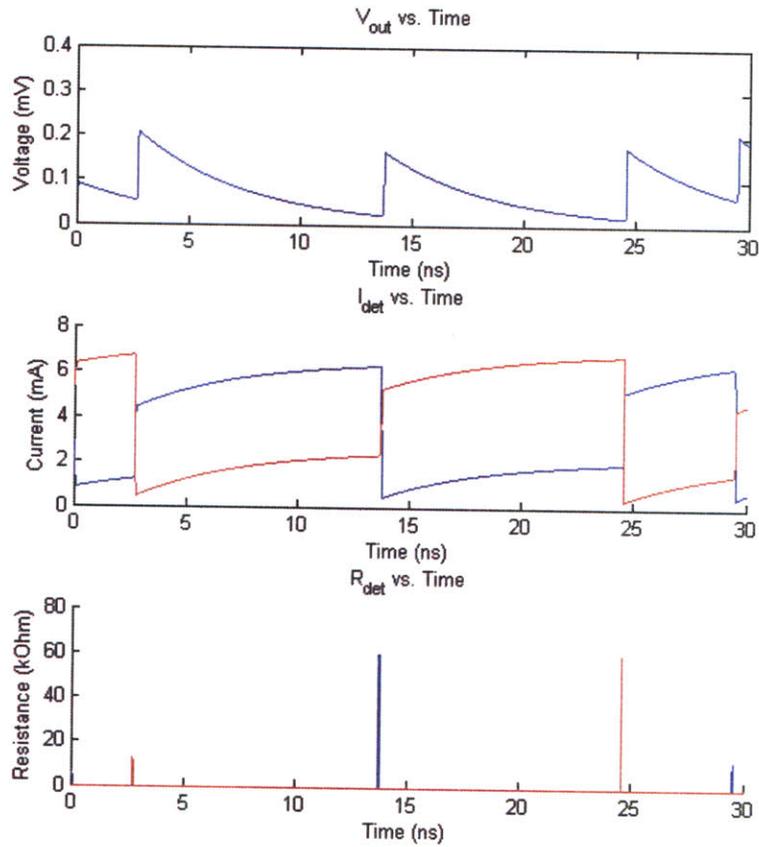


Figure 6-2: Results for the parallel nanowire simulation at  $9\mu\text{A}$  total bias. Note that the system oscillates due to the fact that one detector does not fire immediately after another. This results in a type of ‘flux trapping’ which causes the second detector to switch at a later time, causing oscillations.

What happens is, some overall current is rerouted from the detector to the output. When this current returns to the detector array, the additional current must divide equally between inductors. This results in SSPD2 switching during the ‘reset’ time of SSPD1.

This secondary switching event produces the same results as the first, only in reverse. Now SSPD1 has dramatically more current, but initially not in excess of its critical current. Current redistributing to the detector exceeds the critical current, causing another switching event.

This oscillation theoretically should not occur because we are above the avalanche current. However, there are two non-ideal elements included in this simulation that result in the experimentally observed oscillations. First, when a detector switches, its current does not drop completely to 0 due to the fact that the detector relaxes thermally before all of its current is lost. In addition, the second detector's current does not increase by the amount that the first detector loses. The ratio results from the fact that this current is divided between the output impedance (determined primarily by  $L_{series}$ : the series inductance to the detector) and the secondary detector's impedance ( $L_{det}$ : the kinetic inductance of the second detector). As a result, even though we are above the theoretical avalanche current, we do not trigger the second detector immediately, and oscillations occur.

Note that we can mitigate this problem by increasing the value of the series inductor, as the inductor will cause additional current to route through the secondary detector. In addition, if we increase bias current, the detector can function properly. A proper avalanche detection is shown in figure 6-3.

When the detector functions properly, the secondary detector avalanches while the first detector is still resistive. This prevents any problems resulting from current redistribution. However, also note that this system still does not function flawlessly in that it does not return to exactly its original state after the detector fires.

In observing the detector currents closely, one observes that the detectors relax to different bias currents. Therefore, after the detector fires, the current redistributes in a seemingly unpredictable manner. Also, this difference in current is not insignificant, being at approximately  $1\mu\text{A}$ . This difference in bias could dramatically affect detector efficiencies or relative dark count rates.

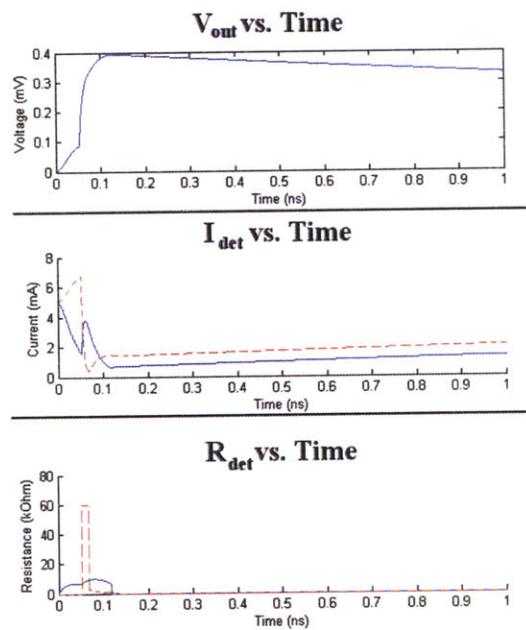


Figure 6-3: Simulation results for a properly functioning detector cascade. Individual detector currents and resistances are shown in dashed/solid, respectively. Conditions are the same as the oscillating case except bias current has been increased to  $10\mu A$ . Note that after the switching event, the current does not redistribute between the two detectors evenly.

# Chapter 7

## RSFQ Layout

Now that we have our designed and simulated RSFQ circuits, we must now actually construct them physically. Given the component sizes, it is readily apparent that this circuitry must be constructed as an integrated circuit. Design of such electronics is usually performed in Cadence, but Cadence does not intrinsically support our fabrication stack or the Josephson junction circuit element. Therefore, we are better served using a solution more specifically tailored to superconducting electronics.

### 7.1 WRSpice Design Package for Superconducting Circuits

WRSpice is a software package written by Whiteley Research for exactly this purpose.<sup>[30]</sup> This software is similar to Cadence both in functionality and operation. However, this software package is specifically designed to fabricate superconducting circuits, intrinsically supporting Josephson junctions as fundamental circuit elements.

The design flow is also identical to Cadence. WRSpice is designed to simulate and layout cell-based designs from previously designed schematics.

Probably the most important aspect of the WRSpice environment is the technology file. This file is very similar to the Cadence counterpart. It defines editing layers for both schematic capture and layout. It controls the fabrication stack definitions for

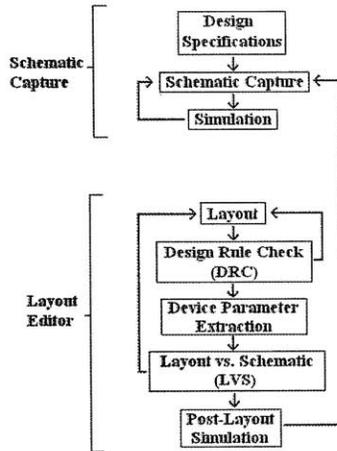


Figure 7-1: Standard design flow for integrated circuit fabrication. This flow is mimicked exactly by WRSpice, which provides integrated software for each of these steps.

the layout as well as their electrical parameters. It defines how the program performs circuit extraction from layouts. Finally, it gives design rules to be used by the DRC.

For this design, we are using Hypres' 3-layer fabrication process standard.[29] We carefully translated the stack properties and design rules into WRSpice and subsequently checked our properties with other research groups who design RSFQ circuits. As a result, we are confident in all of our designs constructed with this technology file.

## 7.2 RSFQ Specific Layout Practices

Although there are significant similarities in the design and fabrication processes for superconducting circuits and traditional silicon circuits, there are also a number of design and layout practices that vary dramatically. Since we are using Hypres' process, we will consider this process as a model. More general design practices are given in Appendix A.

There are a series of design considerations for superconducting electronics that differ significantly from normal electronics. First, biasing techniques differ. Since we are using superconducting traces, we have to make sure that we do not exceed the

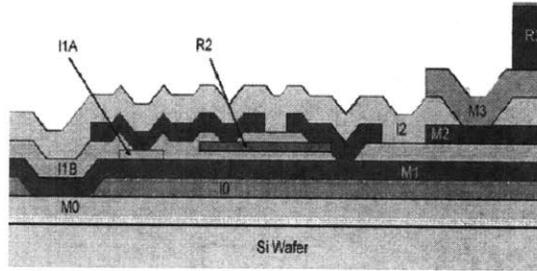


Figure 7-2: A schematic of the Hypres stack with each layer designated.[33]

critical current for each trace. General recommended practice for Hypres' process is for bias lines to be on the order of  $10\ \mu\text{m}$  wide, especially for the thinner layers in the stack (M0, and M1).[29]

For our application, we do not use as much power as most RSFQ circuits, so we have chosen to use  $5\ \mu\text{m}$  traces. This smaller width is acceptable because we are also using multiple bias lines for each experiment. Also, we do not have the power transmission lines run over steps in the lower layers. Since the Hypres process is not planarized, steps under a trace can potentially reduce the critical current of the trace. This decrease is not well characterized, so we simply avoid the situation entirely.

In addition, the digital signal in RSFQ circuits is very small, so noise coupling between the power trace and the signal trace must be minimized. One shields the power traces by providing a grounded shield between the power trace and all signal traces.

Additional measures can be taken to prevent coupling by ensuring that all power traces that must cross signal traces do so in a perpendicular manner. Such an intersection minimizes the mutual inductance between the two traces and therefore minimizes the coupling.[5]

Another more subtle difference between silicon and superconducting processes reveals itself in the use of the ground plane. Whereas in silicon processes, current follows the minimum-resistance path, in superconducting process, current instead follows the minimum-inductance path. To minimize inductance, return current will follow the

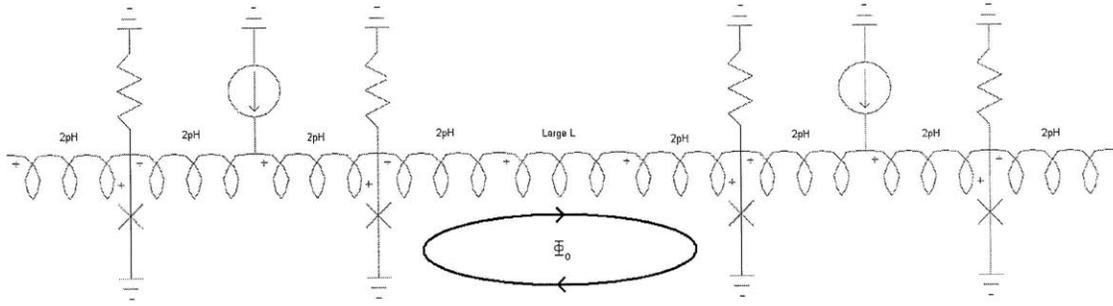


Figure 7-3: Schematic of how a large series inductance leads to flux trapping. Note that the persistent current will have current such that  $LI = \Phi_0$ . Since we have a large inductance,  $I$  can be small enough not to exceed  $I_c$  of the Josephson junctions. Avoiding large series inductances prevents this problem.

ground plane directly underneath the power trace. This current distribution on the ground plane is fine for most applications, but one must be careful not to break the ground plane below power traces, as this could potentially create pockets of high ground plane current in sensitive areas of the circuit.

For our purposes, we only ever break the ground plane to create a superconducting moat, so this has not been a problem for us. In addition, we have created a large enough ground plane around the power traces such that some additional return current will not affect circuit performance.

One of the most significant problems that arises in superconducting electronics that is nonexistent in a normal silicon process is flux trapping. If one traps a persistent current in a circuit loop, the additional current can prevent the circuit from functioning as designed.

The minimum amount of flux that can be trapped is one magnetic fluxon ( $\Phi_0 = 2.07 \times 10^{-15}$  Weber). Generally, the circuit we have to consider is an RF SQUID or equivalent, with a Josephson junction and inductor in series.

If we wish to avoid flux trapping in the inductor, we can make  $LI_c < \Phi_0$ , where  $I_c$  is the critical current of the junction. Since  $I_c$  is generally determined by the circuit design, generally one minimizes the series inductance.

The majority of inductance in a superconducting circuit occurs simply through

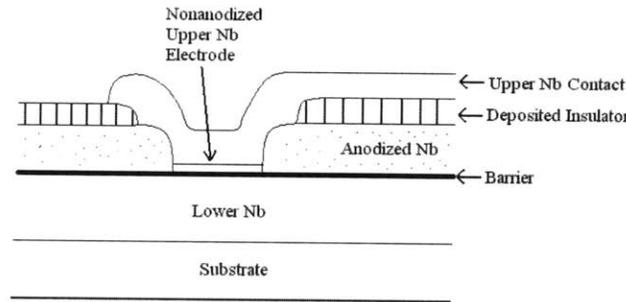


Figure 7-4: Schematic of the anodization stack[9]. This corresponds to the Hypres stack as follows: upper and lower Nb contacts are M2 and M1 respectively. Junction area is defined by I1A or I1C depending on the process ( $1\text{kA}/\text{cm}^2/4.5\text{kA}/\text{cm}^2$  respectively). The insulator is patterned with I1B. Finally, the anodization area is patterned by its own layer, 'A'.

parasitics arising from finite-length traces over a ground plane. Therefore, we must minimize the length of these transmission lines. The proper way to do this is to break up this series inductance by placing a Josephson transmission line between two elements that must be physically separated by more than a few microns.

Finally, there are a few Hypres-specific application notes that merit discussion. First is the fabrication of resistors. Hypres uses a Mo layer with resistivity of  $2\ \Omega/\square$ . [29] The Mo layer is much thinner than the layers below it, so one must be extremely careful not to locate a resistor over a step in a lower layer (M0, I0, M1). Otherwise, the Mo layer will not be continuous, and resistor will become open.

Next, Hypres uses a self-aligned anodization process that allows more accurate definition of Josephson junction area. This stack is given in figure 7-4.

Note that we have an additional layer that defines an insulating layer above M1. As a result, one can define the Josephson junction area with I1A/I1C. Next, one can connect to the top of this node to M2 by defining I1B around the connection. The advantage of using the anodization process is that one can define I1B to much larger than the area of I1A and the two layers do not have to be very well aligned. This significantly relaxes the requirements on the I1B mask and has been shown to produce better yields and junctions. [19]

Finally, there is one simple practice that is worth noting simply because of its

importance to circuit yield and durability. One connects to the circuit by wirebonding to pads patterned on the R3 mask. This conductive layer effectively acts as an interface. However, one must be careful not to short this layer to ground in the process of wirebonding. The heat required to wirebond to this layer will degrade the oxide insulating layers below it. Therefore, if there are any conductive layers below wiring pads (including the ground plane), one runs the risk of shorting these to the pad after wirebonding.[29]

### 7.3 Layout of Readout Experiments

For this experiment, we designed four separate circuits to test individual components as discussed previously. Each of these experiments simply uses the basic cells connected in some simple fashion, so the actual experimental layout was relatively simple. However, there are additional design elements that merit some discussion.

Our design for each cell was very robust and scalable. However, after layout of the fundamental circuit, we tried to go back and add superconducting moats. As it turned out, this was a relatively inefficient approach that can be rectified in the next design iteration.

In order to maximize moat area, we tried to design moats that contained blocks in multiple cells.[11][25][26] Although this was possible and we succeeded in implementing a successful design, the design time was far too long and resulted in complex interaction between parent and child cells. In our next revision moats will be included in each of the basic RSFQ cells, or the cell containing the whole circuit. No moats will cross this abstraction layer.

On the other hand, a very good design choice we have made is to independently bias each point on the circuit. Each of the basic cells requires bias current at different points in the topology. Traditionally, one provides a single bias line which is broken into multiple currents on chip. However, we wish to be able to characterize the process and the RSFQ elements, so we have chosen to bring each of these bias points out individually.

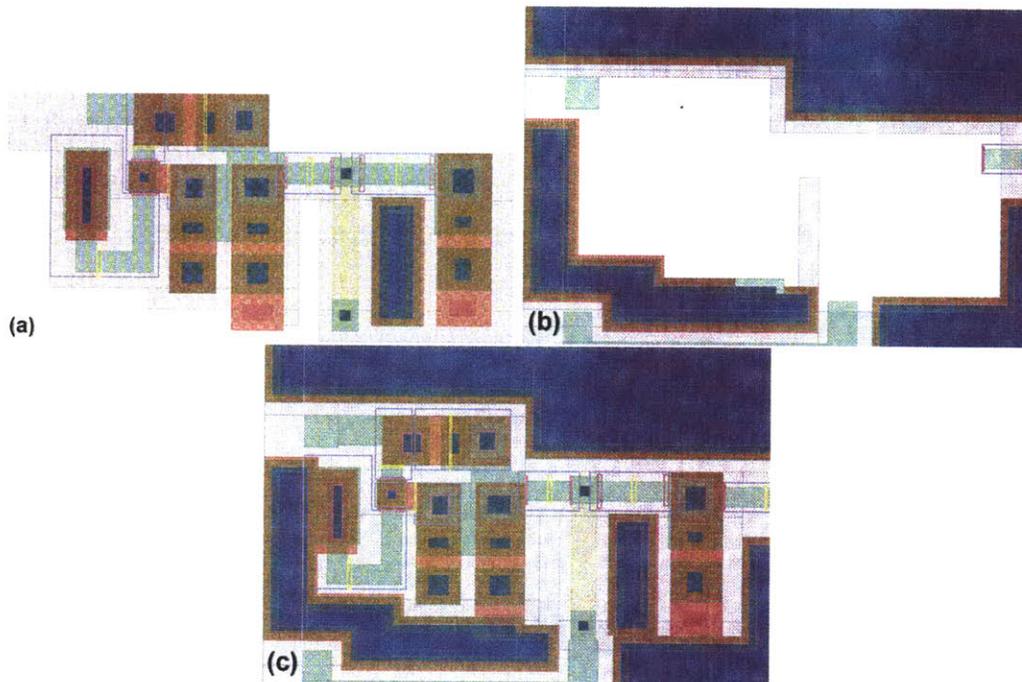


Figure 7-5: Example of the abstraction breakage between the DC/SFQ converter cell and its containing cell. (a) is a figure of the DC/SFQ converter, (b) is the containing cell, and (c) is a figure of both cells flattened. Note that certain layers overlap from the outer layer to the DC/SFQ such that the layers have to ‘interlock’. This is not desirable because if this dependence changes, it requires the designer to change all of the containing cells at each DC/SFQ instance.

The ability to tweak individual bias currents will allow us to verify the simulation bias point as well as explicitly measure tolerances. The only downside to having so many power traces is the area requirement. For our prototype, this loss of area is acceptable, but in the final implementation, it will be far more efficient to use a single bias line.

One final note on the point of multiple bias lines is that this design choice has allowed us to relax the tolerances on our resistances for each bias point. Normally these resistances set the current bias point for each individual element, but in our case we can individually manipulate the input current outside the cryostat. As a result, we can effectively allow these resistors to take whatever value is geometrically most convenient. Once we measure the operating point we wish to use, we will redesign these resistors to properly split the bias current.

## 7.4 Additional Considerations

Since we are just beginning to explore the experimental implementations of Josephson junctions and RSFQ circuits in our group, it is necessary to perform extensive baseline measurements. Therefore, in addition to testing the basic RSFQ circuits, we also wish to characterize the Hypres process. To do this, we have fabricated individual overdamped Josephson junctions outside of the experimental area for individual testing.

As a note, we have chosen a 2-point measurement of each Josephson junction. Although this is less accurate than a 4-point measurement, we chose to do this because wirebonding pads require large amounts of area on chip, and it was more important to us to measure the full range of Josephson junction areas with acceptable granularity, rather than measuring each junction with maximum precision.

In addition, we have layouts of the SQUID input stage for the SNSPD. Since this is a purely analog stage, we can actually test this stage without supporting RSFQ circuitry. We can characterize exactly what bias current we need and with what tolerance to ensure that all pulses are properly processed.

# Chapter 8

## RSFQ Experimental Setup

In addition to designing just the readout circuit, we also have to construct the experimental platform on which it will function. Because we are just beginning to build RSFQ circuitry, it is prudent for us to build a maximally general experimental setup capable of delivering a large number of RF and DC lines.

### 8.1 Physical Construction

The driving parameter of the physical experimental manifold is the inner neck diameter of our cryogenic storage device. We wish to perform experiments over longer periods of time, requiring our probe to mount into a 100L storage tank of liquid helium. The standard inner neck diameter of this mount is 1.45", so our entire experiment must fit into this diameter.

Simultaneously, we wish our probe head to be accessible and robust enough to modify on-the-fly without having to completely reconstruct the probe head.

The probe head mounts onto a standard 0.5" O.D. vacuum stainless tube, which will act as mechanical support and the connection to the feedthroughs at the top of the dewar.

As shown in figure A-5, the probe has three primary flanges. Flange 'A' serves as the base mount onto the connecting vacuum tube. Flange 'B' serves multiple functions. First, it is threaded on the outside to match the shielding can. All elements

between flange ‘B’ and flange ‘C’ will be mounted inside the shielding can. In addition to this threading, the electrical mounting stack will be placed on the backside of this flange (between flange ‘B’ and ‘C’). Finally, flange ‘C’ serves as the optical mount. It mounts onto the posts to mechanically stabilize the fiber with respect to the electrical/sample mounts.

The shielding can is the most critical component of this setup. Because RSFQ is so sensitive to trapped flux within the circuit, we must reduce the ambient field around the chip to below approximately 20mG.[11]

To achieve this, we have utilized a dual-layer 0.010”  $\mu$ -metal magnetic shield mechanically wrapped around a stainless can. If the  $\mu$ -metal shield were perfectly continuous around the entire cylinder, we would observe a reduction of the ambient field around the chip by a factor of 1000-10000.[7] However, the endcaps of our shielding are not physically connected, so some flux leaks into the can.

We have measured the ambient field *normal* to the RSFQ chip’s surface to be approximately 5-15mG depending on the degaussing performed. Note that although we have not measured all three axes of magnetic field, the other two axes are not as important as the effective area that the flux be trapped in is much smaller. We are concerned about flux through the superconductor of the RSFQ chip, which is necessarily normal to its surface. The chip is always mounted in the same orientation, so we only need to characterize the total magnetic field perpendicular to its surface.

## 8.2 Electrical Connection Strategy

Our experimental setup has 4 RF and 10 DC lines which we wish to route to arbitrary wirebond connections to an RSFQ or SNSPD sample. These numbers were determined by the number of electrical connections that any one RSFQ experiment requires. We have two extra RF and DC lines than is necessary to perform each experiment.

We wish to route these electrical connections in such a manner as to preserve as much high-frequency content as possible. Because of this, we cannot use any physical

switches. Instead we opted to fabricate a board that is customizable to multiplex signals that can be swapped out if necessary. These boards are shown in figure A-6.

There are three primary branches of experimental setup that we need to consider. Our experimental setup is designed to test RSFQ circuits, SNSPDs, or both. Our RSFQ mount needs a large number of wirebonds which can be multiplexed down to the base board. To test SNSPD's, we need only a few RF lines at a time. Therefore, I use different adapter boards for each application.

Board 'c', above is the base board. This board is always connected to the probe, and all electrical connections feed through this PCB. Next, for SNSPD applications, we attach board 'd' directly to board 'c'. This board provides multiple RF lines for SNSPD testing. In addition, it routes a few DC lines so that we can attach a temperature sensor to the sample mount.

If we wish to test RSFQ circuits, we mount the sample on board 'a'. This board has 64 wirebonding points, each of which are routed to the DF-12 connector on the reverse side. This connector then attaches to board 'b', the multiplexer board. Board 'b' brings each of these connections out to a solderable pad. The user then connects these pads to the respective via's near the edges. Each of these vias is connected to a different RF/DC signal on the base board. One can swap out adapter boards for different experimental tests without wirebonding the sample mount. Finally, if wants to test both RSFQ and SNSPD circuits, the setup described for RSFQ testing with boards 'a' and 'b' will suffice.

The primary downside to this approach is bandwidth. although we are utilizing physical connections at all points (as opposed to switches), none of our traces are shielded from each other, and our connectors have a very small (0.5mm) pitch. As such, there is significant parasitic capacitance.

This loss is shown in figure 8-1. Note that this parameter is measured transmission from the electrical connections down to the probe head and back up to another electrical connection. As such, it is measured over twice the length of the probe, and therefore reflects twice the loss of a signal transmitted from the probe head and measured by instrumentation outside the cryostat.

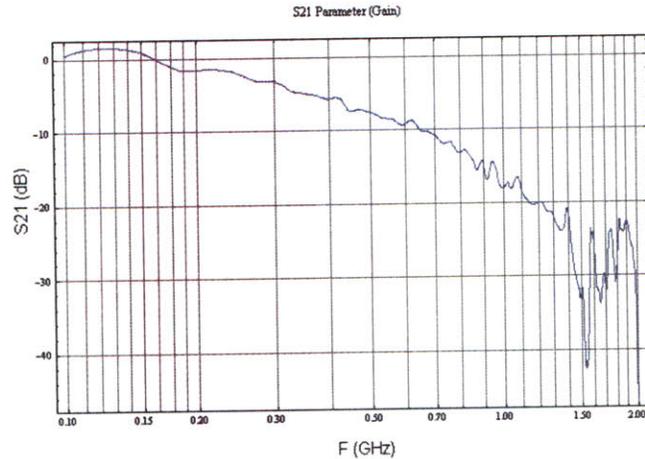


Figure 8-1: Measurement of  $S_{21}$  of the probe. This transmission coefficient indicates loss in our system. This measurement is over twice the length of the probe, and as such indicates twice the loss that we will observe from a signal transmitting from the probe head to the instrumentation outside the cryostat.

Finally, we ground each of our RF lines to the probe manifold at the feedthrough at the top of the dewar. One DC line also serves as a ground connection. This ground is then shared at the probe head. This connection scheme produces a small ground loop around the shields of the RF, but given the number and strength of connections, this effects of this loop should be minimal.

### 8.3 Optical Setup

In order to test SNSPD efficiencies, we wish to couple light to the chip mount. To do this, we bring a fiber optic line down to the probe head and mount it on flange ‘c’ (see figure A-5). Note that the fiber mount attaches to the same posts that the sample mount attaches to. As a result, the fiber will be very stable with respect to the sample.

We do not collimate or focus light coming out of the fiber. Instead we utilize a large numerical aperture fiber to spread the light as much as possible over the area of the chip.

Therefore, we mount the fiber directly into flange ‘c’ directly. This setup has

yet to be tested, and there exist a few concerns stemming from the fact that the system must exist in a 1.5" diameter. This will require a relatively tight bend in the fiber line which may hinder functionality. This needs to be tested empirically, as we cannot predict how such a bend will interact with cryogenic temperatures to affect the performance of the fiber.



# Chapter 9

## Conclusion

We have made a number of advancements in SNSPD readout technology. First, we have completely designed an RSFQ circuit capable of digitizing, clocking, and outputting the presence or absence of an incident photon. We have explored from the ground up exactly how this circuit works.

To ensure that our design will work properly, we have simulated both the RSFQ circuitry alone, and we have simulated the interface between RSFQ and SNSPD. To achieve this, we have designed our own custom models and simulation setup using Matlab Simulink.

In addition, we have designed a complete experimental apparatus capable of testing this circuit. Once again, we have had to build this apparatus from the ground up. We have discussed the engineering tradeoffs made in this apparatus to achieve the properties that we need.

Next, we have designed and fabricated all of the analog interfaces necessary to properly realize an RSFQ readout. We have designed an on-chip bias tee capable of routing the SNSPD signal to the RSFQ circuitry while allowing an external DC bias. In addition, we have designed and constructed a broadband cryogenic amplifier capable of delivering over 10dB gain from 2MHz to 700MHz within the manifold of the probe.

Each of these pieces has been researched, designed, and fabricated. Over the next six months, we will begin to implement and test the readout and its capabilities.

Once this testing has been completed, this readout will serve as a major advancement allowing general research and commercial usage of the SNSPD.

# Appendix A

## Appendix

### A.1 Integrated Circuit Layout

After designing and simulating a circuit with spice, one then has to CAD the physical implementation of the desired circuit. Now, there are a huge number of additional degrees of freedom for design choices regarding placement, part geometry, and many more variables. The foundry to be used will supply a basic design rule document that generate the best yields, but do not provide information as to the best practices to have an efficient and reproducible design flow.

#### A.1.1 General Practices

There are several rules that generalize across all forms of electrical layout, ranging from PCB to Silicon to Niobium. These practices include general rules that decrease parasitics, cross-talk, and time-consuming debugging.

#### CAD Usage

Computer Aided Design (CAD) has long since been the industry standard for all forms of layout. Most tools are very similar in function with only a few design-specific functions to distinguish individual pieces of software. Therefore, good practices for a specific CAD program generalize to most if not all other CAD applications.

The primary advantage of CAD is that the computer can draw very precise shapes. This is enabled by the use of a grid on the layout surface. Therefore, at all times, one must use this grid to take advantage of the layout software. Although this seems trivial, it becomes difficult to keep in order when one is editing both large and small features simultaneously. Consider the case of a superconducting circuit with multiple micron-size Josephson junctions. Each of these junctions must be patterned with a micron sized grid. Now, on this same chip, one will have millimeter-sized landing pads. These must be patterned with a *much* larger grid.

This is achieved by editing specific sections of a chip with a single grid. This is not a feature in any CAD program, rather it must be maintained by the user. Next, one must adapt between grid sizes on the boundaries where one section meets another.

This process is made easier by the fact that a design is broken up into cells. Cell design is the process of designing a chip on a hierarchy. Specifically, one has basic cells that implement gates, Josephson junctions, or simple circuit elements. One then can insert these files as links into more complicated designs, etc. This allows for a very modular design in which a change in one of the leaf designs is easy to enact.

Note that there are several advantages to using a hierarchical implementation of a complex circuit. First, if there is a process change that changes the geometry of a fundamental device, such as a FET or Josephson junction, one does not need to change all  $10^6$  or so elements individually. Rather one needs only to change the affected leaf nodes (should be 10 nodes) to propagate this change to the entire design.

Second, as mentioned above, it becomes dramatically easier to manage the grid. Specific cells will be edited only with a single grid setting, ensuring that no grid-related errors occur (large rectangles separated by very small distances, very small misalignments, etc).

However, there are several potential pitfalls to this approach that must be avoided. As with any hierarchy-based design, the boundaries between leaves and parents or adjacent cells is extremely important to manage properly. Each cell should be completely self-contained and provide specific connections at specific ports. An example of a mistake that the author made on this front was in superconducting circuits. In

the process of trying to design moats around individual cells, the author tried to have half-of a moat contained within a leaf cell and the other half within the parent cell. As the leaf was contained within multiple parents, it became extremely difficult to maintain a consistent moat geometry across all of the parents as the leaf note changed.

In summary, utilize the cell and grid functionality of the CAD software, but make sure that they are utilized properly. For grids, make sure that your grid of choice is always consistent for a given element, and ensure that you adapt properly between sections of the chip with different grid spacings. For cell and hierarchical design, make *sure* that each cell is self-contained.

Next, some layout editors contain advanced features such as Layout vs. Schematic (LVS) comparison, and Design Rule Checking (DRC). These features are very useful in producing a consistent design.

Utilizing LVS properly is an exercise in proper design flow. LVS software only works within a specific layout design package, such as Eagle, Cadence, or WRSpice. Therefore, make sure to edit your schematic in the same software that you layout in.

Second, LVS requires that the schematic be present *first*. It is possible to produce a schematic from a layout, but this process is ugly and time-consuming. Always draw the schematic first before laying out.

Third, utilize the hierarchical nature of your circuit. Don't count on the LVS to give you error notes that are helpful in determining the nature of your error. In many cases, a layout error will completely change the topology of the circuit (such as shorting V+ and GND nodes), and the LVS program will give you completely nonsensical errors. In this case, it becomes crucial to break your design up into small parts, so you can check small parts of your circuit individually.

Utilizing DRC properly is an exercise in being thorough. Design rules vary from foundry to foundry, so one cannot count on the proper design rules already being implemented on your software. If this is the case, one must implement these design rules manually. This process is very time consuming, but absolutely necessary. A foundry design document will give you up to several hundred individual rules to

check, depending on the process. In addition, some foundries (such as Hypres) do not DRC submitted designs with their own rules, so one cannot count on the foundry to catch any mistakes.

For this process, one must manually enter and check specific rules to ensure proper functionality. Create individual circuits that validate each DRC rule you implement. All of this must be done *before* one begins the layout process. Good layout practices keep elements as close together as possible, so one design rule error due to improper spacing can result in a cascade effect that is very time-consuming to fix.

Although DRC is a very powerful tool, it cannot and will not check all of the rules put forth by the foundry. For example, Hypres's optical lithography process results in certain layers being systematically larger or smaller than what is drawn in CAD. This is not compensated for in DRC, rather one must read the design document carefully and recognize which rules are checked by the DRC and which rules must be kept track of by the designer.

## **General Electrical Practices**

When laying out electrical circuits, there are several practices that have been proven to produce consistently good results. The first and most general rule about good circuit design is to keep traces short.

This practice minimizes parasitic capacitance and inductance. These additional unintentional devices will decrease circuit speed, distort signals, and potentially completely hinder circuit functionality depending on the frequency of operation. In addition to removing parasitics, shorter traces help to prevent physically close traces from having significant cross-talk.

For particularly sensitive signals, one can provide a physical ground shield around the trace. In this case, we shield any potential fields from interacting with the trace by placing a ground plane below and above the signal trace. We then connect these two ground layers together with vias on either side of the signal trace. This process is intensive in both design time and chip area, so it should only be used for specific applications where shielding is absolutely necessary.

Probably the most troublesome traces other than those with very sensitive signals are the power traces. These traces must have a number of characteristics. First, power traces inevitably carry large amounts of current and as such absolutely *must* be wide. Guidance for this varies between applications. For normal silicon, one must ensure that the resistance of the wire is not large, and that energy dissipated in the wire will not be excessive. For superconducting applications, one must make sure that the current through the wire does not exceed the critical current of that wire.

Also, since the trace is carrying a considerable current density, the magnetic field around the wire is considerable. Therefore, one must ensure that crosstalk is minimal. In the case of power traces, physical proximity to sensitive parts must be avoided wherever possible. If a power trace must come near a trace with a sensitive signal, make sure that the current paths are orthogonal to minimize cross-talk.

In addition, power traces should be shielded from the remainder of the circuit if possible. By encasing power traces in a ground shield, one can prevent most supply noise and extraneous fields from coupling from the power trace to the circuit in question.

Along these same lines, one must be careful of ground usage. Note that the ground plane has a finite inductance and/or resistance. Therefore, fast digital signals will cause a ripple on the ground plane. If this is not handled properly, it can significantly affect the performance of other circuits.

First, one can ameliorate this problem by physically removing digital and switching elements to areas that are far away from sensitive analog circuitry. Second, if analog circuitry is extremely sensitive, all measurements and signals must be differential or referenced to a separate, quieter analog ground. For integrated circuits, the base layer of metal is ground for the whole chip, so it may be difficult to separate grounds. Therefore, one must use the other techniques mentioned above to try to reduce ground noise.

Finally, one must always be cognizant of the fact that the physical process is not perfectly aligned. Therefore, it is good practice to make sure no two layers have edges that are on top of each other for the following reasons. First, a slight misalignment

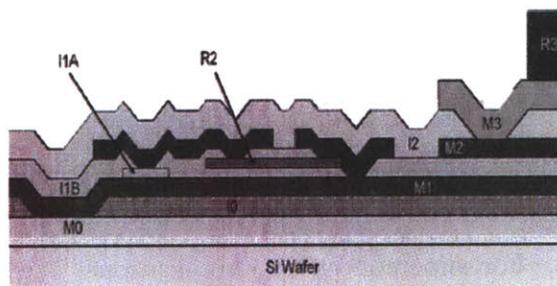


Figure A-1: A schematic of the Hypres stack with each layer designated.[33]

between the two might cause a section of the top layer to spill over the step created by the bottom layer. Since the section in question will necessarily be very narrow, it may or may not be well connected to the rest of the layer. This might result in a narrower wire or other electrical element than anticipated.

Another problem that aligning layer edges can create is due to the fact that this will increase the step size seen by higher layers. For example consider the stack shown in figure A-1. If there is a simultaneous step of M0 and I0, this would create a much larger step for M1. If one were trying to have a trace over this step, the trace would most likely dissociate, since the deposited metal M1 is not thick enough to completely cover the step.

### A.1.2 Hypres Foundry

Hypres, Inc. is a commercial foundry for superconducting integrated circuits. They use a 3-metal layer Niobium process that utilizes Nb-Al/ $\text{AlO}_x$ -Nb Josephson junctions.[29] The full stack is given below in figure A-1. M0,M1,M2,M3 are Nb layers (M0 is ground). I0,I1B, and I2 are insulating layers. I1A is the  $\text{AlO}_x$  layer for Josephson junctions. Finally, R2 and R3 are Mo layers that are resistive at cryogenic temperatures. R2 is used for resistors, while R3 is used for contact pads.

One important note about Hypres' process is that it is non-planarized. Therefore, we must worry about steps from all lower layers, M0, I0, etc. when we design the upper layers. This will result in several design rules which will be discussed later.

### A.1.3 Superconducting IC Layout

One of the most important considerations in designing RSFQ circuits is how to remove flux from the circuit. This is done by removing all superconductor from certain areas away from the actual circuit. By removing superconductor, one can trap a ‘vortex’ inside of this area. This is a lower energy state because there is no normal core anymore. There exists only the circulating current around the moat.[11][25][26]

Note that this is a very difficult process to calculate analytically or numerically. Therefore, the process of adding moats to a circuit is not precise. There is no exact definition of what is ‘enough’. Rather, this is akin to adding bypass capacitance to a CMOS circuit. One does not simulate the full geometry of the circuit. Instead, one estimates about how much capacitance is necessary. With superconducting moats, the definition is even less precise, as relative location and geometry of the moats and circuits come into play.

Good general moat rules are as follows: Keep moats as large as possible. Try to intersperse moats with your superconducting circuitry. Do not have large ( $1000\mu\text{m}^2$ ) areas of circuitry without moats. Finally, do not place moats very close to sensitive traces.

Another important aspect of superconducting layout are the power traces. There are several additional considerations for a superconducting process. First, since we have a non-planarized process, if a power trace runs over a step (created by the edge of a trace in a layer below it), the critical current will decrease. Therefore, one must overspecify the width of the trace significantly to compensate for this.

Also, it is important to note that the ground return mechanism is dramatically different than in normal silicon electronics. Where current will return along the minimum resistance path for silicon, it will return along the minimum *inductance* path for superconducting electronics. This path is the path that will minimize magnetic field. Therefore, it makes sense that the path will flow back along the ground plane directly under the power trace.

This can potentially cause two primary problems. First, if there are electrically

sensitive connections that are grounded close to a power trace, they will potentially see noise due to the current return. Second, if the ground plane is interrupted under the power trace, the current must find a new path, and could potentially reroute itself through sensitive circuitry. The above two considerations are small at best, but can potentially cause problems for very sensitive applications.

## A.2 Simulink Thermoelectric Model for SNSPD

The original electrothermal model for the SNSPD was developed by Dr. Joel Yang et. al.[32] They broke the SNSPD into a 1-D mesh and solved the heat equation along the wire. An incoming photon is considered as a small region of resistive material. Then, they propagated the competing processes of Joule heating and thermal loss to the substrate.

### A.2.1 Thermal Model Implementation

Our thermoelectric model utilized a simple fixed-step discretization scheme for time evolution (typical step size: 0.1pS). As mentioned above, the SNSPD was broken down into a 1-D mesh. For each step, we used a Crank Nicholson finite difference method to evolve the heat equation forward in time, with  $I^2R$  for each element as a heat source and loss to a 2K substrate as a constant sink.

Next, we recalculate which sections of the wire are superconducting and which are normal by measuring  $T$  relative to  $T_c$  and  $I$  relative to  $I_c(T)$  for each element of the mesh. We then output the total resistance and wire state to be used in the next step.

### A.2.2 Simulink Setup

In order to achieve maximum generality of our model, we must allow it to interface with other facets of Simulink. Simulink utilizes different types of ODE solvers to iterate the entire system forward one step at a time. Therefore, we must first ensure that our model properly reflects a single step forward in time. Therefore, we made several design choices. Instead of trying to explicitly model the thermal processes in simulink, we wrote a Matlab script which evolved the state forward by a given amount of time. These variables were implemented in a discrete system which Simulink solves algebraically.

The output of this discrete system then controls the resistor value in the electrical circuit which is simulated in ‘continuous time’ by an ODE solver. There are several subtleties in meshing these systems together in an accurate manner. First, we must

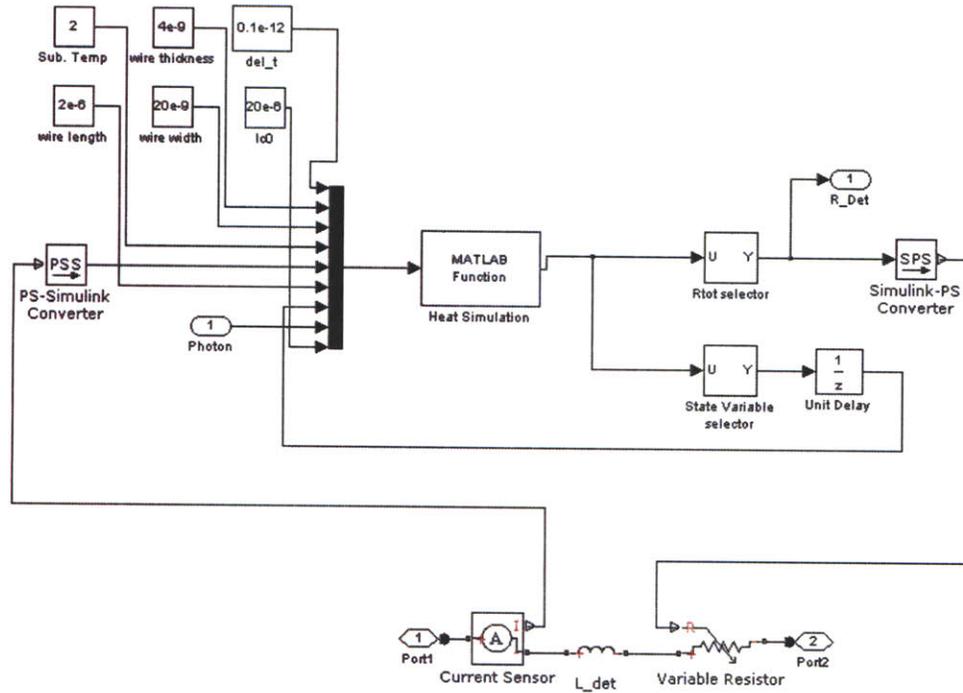
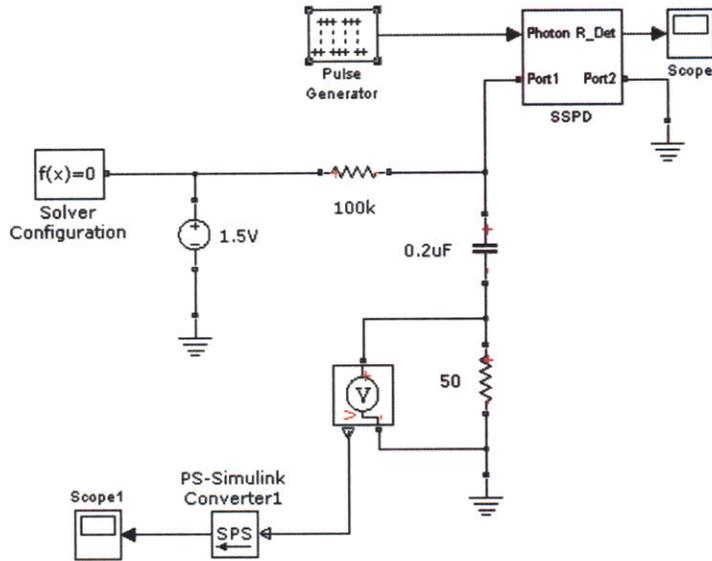


Figure A-2: Simulink model of a SNSPD. Note that the electrical model is simply a constant kinetic inductance with a series resistance. The thermal model controls the value of this resistor in time by measuring detector current and whether or not a photon is incident.

make sure that the timescales match up. Most ODE solvers use a variable step. However, this is incompatible with our thermal model, so we must choose the 'ode14x' fixed step solver for electrical circuits. This is a medium-accuracy solver among the Matlab ODE solver family, but given our incredibly short step size (0.1pS) with relation to the relevant time constants of our system (about 10nS), we can trust that the solver yields accurate results.

### A.2.3 Simulation Results

The next step is to abstract our model as a 2-port electrical model to be simulated in a larger circuit. An example circuit is given in figure A-3. Note that the additional input provides a photon triggering mechanism, and the output provides the status of the resistance of the wire for measurement purposes.



4

Figure A-3: Example circuit for simulating a single SNSPD with readout circuitry. Note that the readout amplifier is simulated as a single  $50\Omega$  resistor.

We measured the outputs of this circuit, the resistance value of the wire and the output voltage at the  $50\Omega$  amplifier termination. These are shown in figure A-4.

The simulation functions properly, yielding the proper resistance versus time and output voltage. However, these results are more significant than this single simulation. We can now simulate the SNSPD as a simple 2-port device in a much larger circuit. This will be crucial when simulating the SNSPD with the RSFQ readout, or simulating SNSPD's in parallel.

## A.2.4 Matlab Code Listing

```

1 function funcout = heatsim(pinput)
2 %Constant parameters
3 del_t = pinput(1);
4 d = pinput(2);
5 W = pinput(3);
6 T_sub = pinput(4);
7 wire_length = pinput(6);
8 del_x = wire_length/1000;
9
10 %Previous state variables
11 I = pinput(5);
12 T = pinput(7:1006);

```

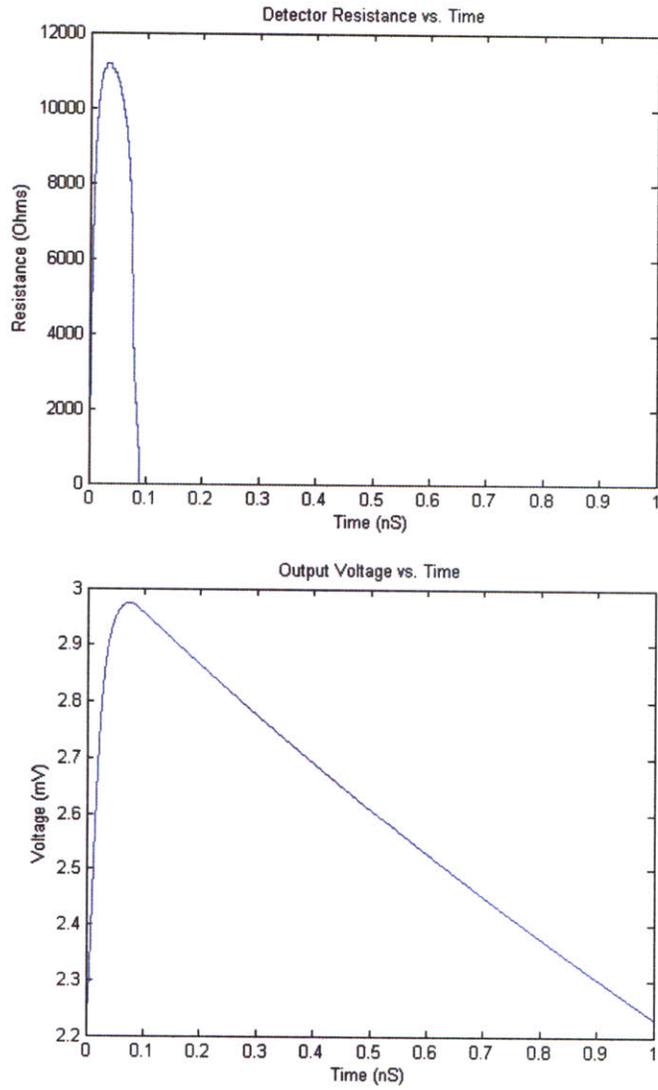


Figure A-4: Simulation results from the Simulink thermoelectric model. Note that the simulation properly reproduces previous simulation results for resistance versus time and output voltage versus time.

```

13 rho_R = pininput(1007:2006);
14 c = pininput(2007:3006);
15 K = pininput(3007:4006);
16 trig = pininput(4007);
17 Ico = pininput(4008);
18
19 %thermal conductivity of NbN
20 %use wiedemann franz law  $K = L_o \cdot T / \text{resistivity}$ 
21 %Lorenz number units of Watts Ohms /  $K^2$ 
22  $L_o = 2.45e-8;$ 
23
24 %heat transfer coefficient per unit area to sapphire substrates from
25 %Tinkham 2W/cm2 K
26  $\alpha = 800;$  %from calculations
27
28 %critical temperature of NbN
29  $T_c = 10;$ 
30 %bandgap energy
31  $kb = 1.3807e-023;$ 
32  $E_{bg} = 3.5 \cdot kb \cdot T_c / 2;$ 
33
34 %specific heat of NbN rough estimate
35 % $\gamma = 1.85e-4 \text{ J/cm}^3 \text{K}^2$  from J. Appl. Phys. V 75, 3695 (1993)
36  $\gamma = 2.4e3/10;$ 
37  $1.85e-4 \cdot 1e6;$ 
38  $\text{specific\_heat\_constant} = 2.43 \cdot \gamma \cdot T_c / \exp(-E_{bg}/kb/T_c);$ 
39
40  $I_{bias} = I;$ 
41
42  $N = \text{round}(\text{wire\_length}/\text{del}_x);$ 
43
44  $jj = 0;$ 
45
46 %assume a length of  $l_{init}$  is resistive when a photon is incident
47  $l_{init} = 15e-9;$ 
48  $\text{resistivity} = 600 \cdot d;$ 
49
50  $\text{unstable} = 0;$ 
51
52
53 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
54 %initialize T rho_R, c, K if nothing previous:
55 if  $T(1) == 0$  %This is the first step, perform initialization routines
56      $T = T_{sub} \cdot \text{ones}(1, N);$ 
57      $\text{rho}_R = 0 \cdot T(1, :);$ 
58      $c = \text{specific\_heat\_constant} \cdot \exp(-E_{bg}/kb./T(1, :));$ 
59      $K = (L_o/\text{resistivity}) \cdot T(1, :).^2/T_{sub};$ 
60
61 else %simulink passes ROW vectors, but we need COL
62      $T = T';$ 
63      $\text{rho}_R = \text{rho}_R';$ 
64      $c = c';$ 
65      $K = K';$ 
66 end

```

```

67
68 if max(rho_R) == 0
69     %wire is superconducting, assume instantaneous reset of temperature
70     T = T_sub*ones(1,N);
71     c = specific_heat_constant*exp(-Ebg./kb./T(1,:));
72     K = (Lo/resistivity).*T(1,:).^2/T_sub;
73
74     Ic = (Ico*(1-(T(1)/Tc).^2).^2);
75     if I - Ic > 0 || trig == 1
76         trig = 1;
77     else
78         funcout = [0,T,rho_R,c,K];
79         return; %don't run the heat model, save some CPU time
80     end
81 end
82
83 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
84
85 %add phonon specific heat
86 c = c + 9.8e3*(T(1,+)/10).^3;
87 %constants that keep changing for every time step
88 At = K/(2*(del_x)^2);
89 Et = c/del_t;
90 Dt = alpha*(T(1,).^3)/(2*d);
91 Bt = (-2*At - Dt - Et);
92 Ct = (-Et + 2*At + Dt);
93
94 %crank nicolson finite difference method calculation
95 RHS = Ct(2:N-1).*T(1,2:N-1) - At(2:N-1).*(T(1,1:N-2) + T(1,3:N)) - (2*Dt(2:N-1))*T_sub
96 RHS(1) = RHS(1) - At(1)*T(1,1);
97 RHS(N-2) = RHS(N-2) - At(N)*T(1,N);
98
99 %prepare a banded matrix for gaussian elimination
100 LHS = [At(2:N-1)' Bt(2:N-1)' At(2:N-1)'];
101 T(1,2:N-1) = gaussElim(LHS,RHS,(N-2));
102 T(1,1) = T(1,2);
103 T(1,N) = T(1,N-1);
104 %stability check
105 if min(T(1,)) < 0
106     unstable = 1
107     return;
108 end
109
110 %begining of electrical model
111 %critical currents at different positions along the wire
112 TIc = T(1,);
113 TIc(find(TIc>=Tc))=Tc;
114 Ic = (Ico*(1-(TIc/Tc).^2).^2);
115
116 %actual flowing current
117 I_flow = I;
118
119 test = I_flow - Ic;
120

```

```

121 %trigger is 1, so simulate an incident photon
122 if trig == 1 %create hotspot midway along the wire
123     resistive_elements = round(l_init/del_x);
124     rho_R(round((N-resistive_elements)/2)+1:round((N+resistive_elements)/2))= resistivity;
125 else %otherwise, figure out what element is normal/superconducting
126     resistive_elements = find(test > 0);
127     rho_R(1:length(rho_R))=0;
128     rho_R(resistive_elements)= resistivity;
129
130     %update specific heat for every wire element
131     c(resistive_elements) = gamma*T(1,resistive_elements);
132
133     non_resistive_elements = find(test<=0);
134     c(non_resistive_elements) = specific_heat_constant*exp(-Ebg./kb./T(1,non_resistive_elements));
135     K(resistive_elements) = (Lo*T(1,resistive_elements)/resistivity);
136     K(non_resistive_elements) = (Lo*T(1,non_resistive_elements)/resistivity).*T(1,non_resistive_elements);
137
138 end
139
140 %overall resistance
141 Rtot = length(resistive_elements)*del_x*resistivity/W/d;
142
143 %format output to be used by Simulink
144 funcout = [Rtot,T,rho_R,c,K];

```

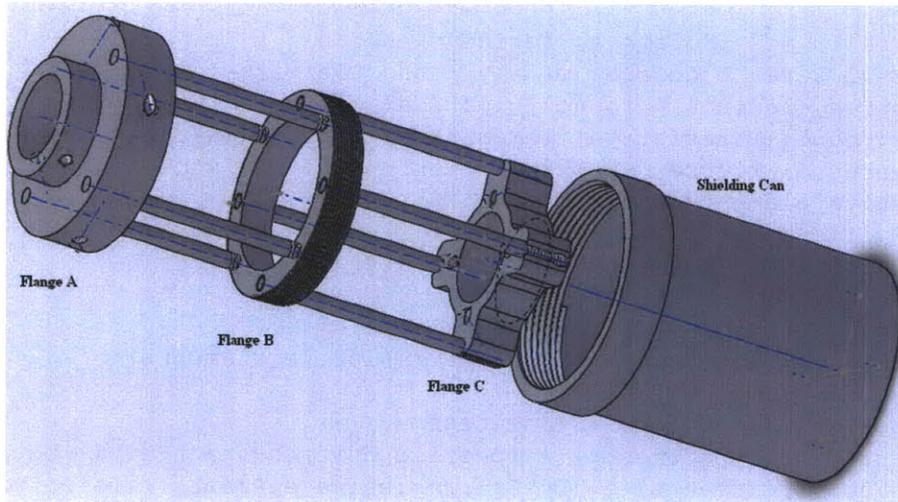


Figure A-5: Model of the probe head. There are three primary flanges connected by posts. Flange 'A' connects the probe head to the 0.5" O.D. tube. Flange 'B' is the mount for the PCB adapters and shielding can. Flange 'C' is the mount for the incoming fiber line.

### A.3 Experimental Drawings

For reference, I include machine drawings of the probe head and the adapter circuit boards to be mounted inside. (A-5, A-6)

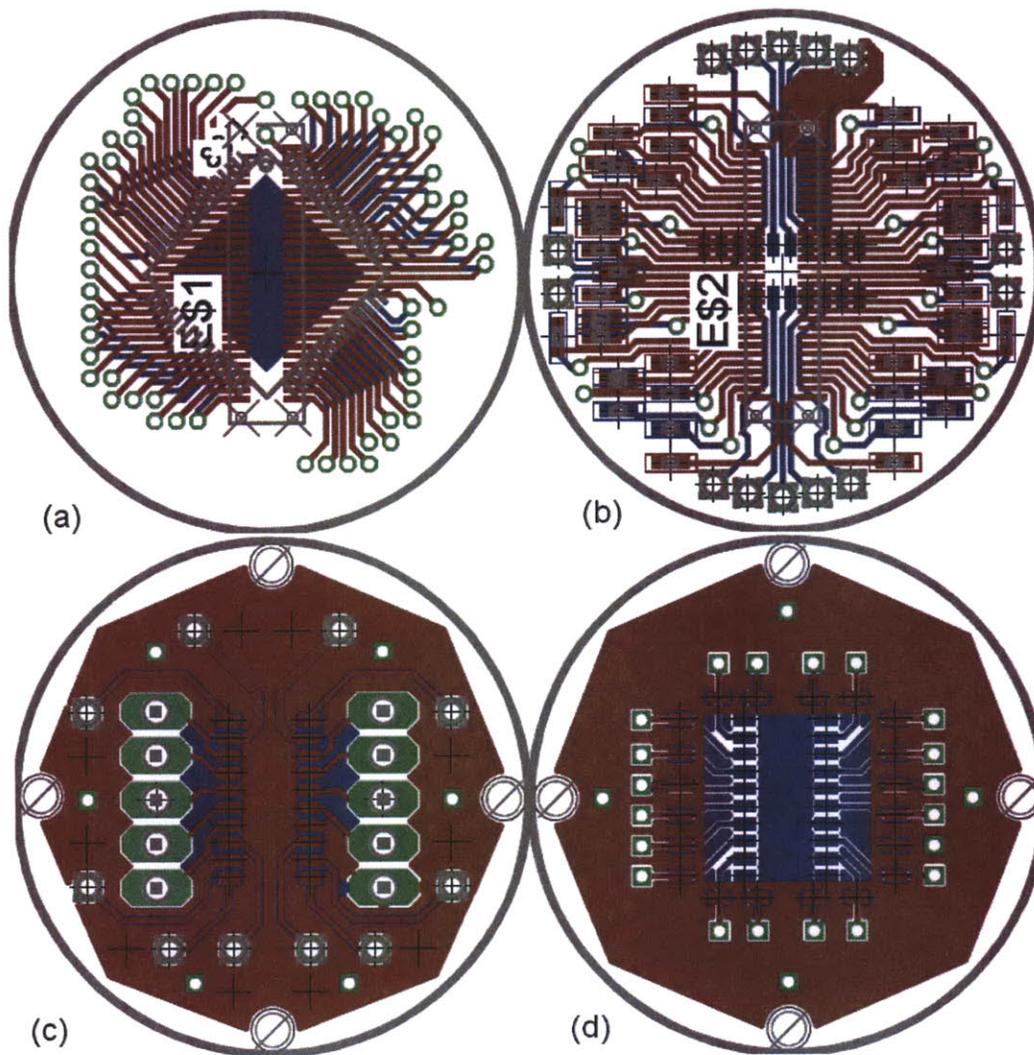


Figure A-6: Schematics of the boards for the adapter stack. (a) RSFQ Sample mount (b) RSFQ adapter board (c) Base board (d) SNSPD mount board.



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