Hole Mobility in Strained Ge/Relaxed SiGe with a High-k/Metal Gate Stack

by

Evelina Aleksandrova Polyzoeva

B.Sc., Electrical Engineering
Technical University of Sofia (2004)
M.Sc., Electrical Engineering
Technical University of Sofia (2006)

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Signature of Author

Certified by

Department of Electrical Engineering and Computer Science
Dimitri A. Antoniadis
Professor of Electrical Engineering
Thesis Supervisor

Accepted by

Chairman, Department Committee on Graduate Students

Terry P. Orlando
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ABSTRACT

The need for high speed and density in the modern semiconductor industry requires new channel
materials and techniques for improved carrier transport and continuous scaling of the device dimensions.
As a material for enhanced hole transport strained-Ge is implemented in this work. High-k dielectric and
metal gate stack is used for improved electrostatic control, as an alternative to the unstable native oxides.
The hole mobility of strained-Ge ring-FETs with and without Si cap and with Al2O3/WN gate stack is
investigated. The dependence of the mobility on the strained-Ge layer thickness and the silicon cap
thickness is explored. Decrease of 13 % in the hole mobility is observed in the devices with thicker Ge
channel suggesting partial relaxation of the strained-Ge. Removal of the Si cap results in almost 40 %
decrease in hole mobility suggesting that the presence Si cap is required in realizing high mobility
devices.

Thesis Supervisor: Dimitri A. Antoniadis
Title: Ray and Maria Stata Professor of Electrical Engineering
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Contents

List of figures............................................................................................................ iv
List of tables........................................................................................................ vi

Chapter 1
Introduction and Motivation................................................................................... 1
1.1. Thesis Goals ......................................................................................... 4
1.2. Thesis Outline..................................................................................... 4

Chapter 2
Theory............................................................................................................. 5
2.1. Properties of Si and Ge................................................................. 5
  2.1.1. SiGe Virtual Substrates......................................................... 5
  2.1.2. Review of Si, Ge and SiGe Bandstructures............................. 7
  2.1.3. Biaxial Strain........................................................................... 7
2.2. Hole Mobility..................................................................................... 9
  2.2.1. Effective Mass........................................................................ 9
  2.2.2. Scattering Mechanisms......................................................... 11
2.3. Critical Thickness............................................................................ 12
2.4. Chapter Summary............................................................................. 13

Chapter 3
Experimental Process....................................................................................... 15
3.1. Device Fabrication............................................................................. 15
3.2. Device Layout........................................................................................................... 18
3.3. Processing Problems................................................................................................. 18
3.4. Chapter Summary.................................................................................................... 19

Chapter 4

Electrical Measurements.............................................................................................. 20
4.1. I-V measurements.................................................................................................... 20
4.2. Output characteristics.............................................................................................. 23
4.3. Split C-V measurement............................................................................................ 23
   4.3.1. Measurement setup.......................................................................................... 23
   4.3.2. C-V characteristics......................................................................................... 24
4.4. Chapter Summary.................................................................................................... 26

Chapter 5

Mobility extraction and analysis.................................................................................... 27
5.1. Threshold voltage extraction.................................................................................. 27
5.2. Doping concentration extraction............................................................................ 28
5.3. Series resistance extraction.................................................................................... 29
5.4. Fixed and interface trapped charge........................................................................ 30
5.5. Mobility extraction................................................................................................. 31
   5.5.1. Calculating Qenv............................................................................................. 31
   5.5.2. Series resistance correction............................................................................. 33
   5.5.3. Hole mobility dependence on the strained-Ge thickness................................. 33
   5.5.4. Hole mobility dependence on the annealing temperature................................. 34
   5.5.5. Hole mobility dependence on the Si cap thickness........................................... 35
      5.5.5.1. Hole mobility as a function of electric field............................................... 35
List of Figures

1.1. Hole mobility in relaxed-Ge with different high-k/metal gate stack structures reported in the literature. The highest hole mobility enhancement over the universal curve (~40%) is obtained for Si as an interfacial layer. Zimmerman et al. – 1.2nm EOT, Saraswat et al. - 0.6-1nm EOT, Shang et al. – 8nm EOT, Hennessy – 1.1nm EOT ................................................................. 2

1.2. Hole mobility of strained-Si/strained-Ge dual-channel heterostructures grown on relaxed Si_{1-x}Ge_x substrates. Decreasing the atomic fraction of Ge in the Si_{1-x}Ge_x substrates increases the strain in the Ge layer and therefore the hole mobility ................................................................................. 3

2.1. Schematic representation of Si, Ge and Si_{1-x}Ge_x lattice structures. The lattice constants of Si and Ge are 5.466\AA{} and 5.431 \AA{}, respectively. The SiGe lattice constant can be calculated according to Vegard’s rule .................................................................................................. 6

2.2. Introducing tensile/compressive strain in Si/Ge layers by growing them on a, presumed thick, SiGe “virtual” substrate .............................................................................................................. 6

2.3. Conduction and valence bands as a function of substrate composition x for Si/Si_{1-x}Ge_x structure (a) and Ge/Si_{1-x}Ge_x structure (b) .............................................................................................................. 7

2.4. Band alignment for the strained Si/strained Ge/relaxed Si_{1-x}Ge_x structure ............................................................................................................................. 8

2.5. Hole effective mass dependence on the hole density for different strain level (a) and hole effective mass dependence on the strain for hole density of 2\times 10^{12} \text{ cm}^{-2} (b) .................................................................................. 10

2.6. Different scattering mechanism contributions to the overall mobility of strained-Ge MOSFET. Ionized impurity scattering dominates at low N_{inv}, and the interface impurity scattering becomes more important at high N_{inv} ............................................................................................................. 12

2.7. (a) Critical thickness for Si_{1-y}Ge_y grown on Si substrate as a function of Ge fraction, y. Increasing of the strain and the processing temperature decreases the critical thickness. (b) Mobility enhancement over the Si control as a function of channel thickness for strained-Ge channel. The notation Ge/X describes Ge layer on X \% SiGe substrate .............................................................................................................. 13

3.1. Schematic cross-sections of the device structures investigated in this work: (a) 3.5/5, (b) 3.5/9.5, (c) 0/8.5 and (d) Si control. The graded buffer and the relaxed buffer layer are doped with Phosphorus to concentration of 5\times 10^{16} \text{ cm}^{-3} .............................................................................................................. 16

3.2. Process flow of p-ringFETs with the different splits. Due to contact and contamination problems with the 600 °C-annealed samples, only the 3.5/5 structure (see text for definition) was investigated at that temperature .............................................................................................................. 17
3.3. Ring-FET mask and relevant device dimensions, used in the mobility extraction

4.1. Comparison of measured transfer characteristics in linear (a) and semi-log (b) scales for 3.5/9.5, 3.5/5, 0/8.5 and Si control p- ring-FETs (L 20 μm, Al₂O₃ dielectric, EOT ~4 nm, WN gate). Very large threshold voltage shift is observed for the capped devices. The current in strong inversion in the silicon control is about 10x lower than in the germanium devices, primarily because of higher S/D resistance in Si due to poorer dopant activation, and also in part due to inherently lower hole mobility in Si. The off-state leakage of the Si/Ge and Ge devices is considerable and is possibly related to the cause of the large threshold voltage shift.

4.2. Comparison of measured hysteresis for 3.5/9.5, 3.5/5, 0/8.5 p- ring-FETs (L 20 μm, Al₂O₃ dielectric, EOT ~4 nm, WN gate). The hysteresis for the capped structures is considerable even at low currents and reaches 2V for Iᵦ ~0.5 mA.

4.3. DC gate leakage current in 0/8.5, 3.5/5, 3.5/9.5 device structures. All devices show similar DC gate leakage, implying that the Si-cap presence is related to the “memory effect” seen in devices 3.5/5 and 3.5/9.5.

4.4. Measured Typical Output Characteristics of 3.5/5 ring-FET with 30 nm WN/6 nm Al₂O₃ gate stack, annealed at three different temperatures. The 600 °C sample shows poorer output characteristics which might be due to existing contact problems.

4.5. Forward and reverse sweep C-V characteristics of (a) 3.5/5 and (b) 3.5/9.5 device with 500 °C SD activation. The hysteresis was calculated at capacitance C = (Cₘₐₓ - Cₘᵢₙ)/2. There is a notable frequency dispersion leading to 7% decrease in Cₘₐₓ value for frequency of 50 kHz, compared to the capacitance value at 10 kHz (a). The anomalous C-V curves, with very high leakage current in accumulation, were observed in all devices with thick germanium layer (b), suggesting partial relaxation of the strain.

4.6. Effect of the anneal temperature on the C-V characteristics for 3.5/5 device. Hysteresis is not changed by annealing at the higher temperature of 600 °C compared to 500 °C.

5.1. Two approaches to calculate the charge illustrated for 3.5/5 device with series resistance correction. For low inversion charges the Cₘₐₓ approximation fails to provide a good estimation of the actual mobility due to underestimation of the charge density for Vₛₜ close to Vₜ. The hole mobility for Nₐ = 5.1x10¹⁶ cm⁻³ is shown for comparison.

5.2. Hole mobility curves before and after series resistance correction for 3.5/5 device with the corresponding enhancement factors over the hole mobility curve for Nₐ = 5.1x10¹⁶ cm⁻³.

5.3. The effect of strained Ge layer thickness on the hole mobility was investigated for 3.5/5 and 3.5/9.5 devices. Both curves were obtained using Cₘₐₓ(Vₛₜ-Vₜ) approximation for the inversion
charge and were corrected for series resistance. Increasing the strained-Ge layer thickness from 5 to 9.5 nm leads to 13% decrease in hole mobility at $N_{inv}=1 \times 10^{13} \text{cm}^{-2}$.

5.4. Effect of the S/D activation temperature on the hole mobility for 3.5/5 device without series resistance correction. The mobility enhancement over the universal curve at inversion charge $10^{13}$ cm$^{-2}$ is 3.5x for activation temperature of 450 °C and increases to 3.6x for 500 °C. Mobility enhancement calculated for 600 °C S/D activation is 2.8x.

5.5. The effect of the Si-cap thickness on the mobility was investigated based on the results extracted from the 3.5/5 and 0/8.5 devices. The enhancement factor compared to universal hole mobility curve is shown in the figure. The mobility of a previously reported device with a structure 3nm Si/7nm Ge and HfO$_2$/TiN gate stack is also plotted.

List of Tables

2.1. Effective masses for relaxed and compressively strained Ge

5.1. Extracted values of $V_T$ and $R_{ext}$
Chapter 1
Introduction and Motivation

The need for high speed and density in the modern semiconductor industry requires continuous scaling of the device dimensions. Silicon has been the material of choice for its highly developed processing technology and relative ease of scaling using traditional methods. Unfortunately, scaling through these methods alone is reaching fundamental limits imposed by effects such as saturation of the source injection velocity with increasing strain in the Si, drain-induced barrier lowering (DIBL) and quantum mechanical tunneling through the gate oxide. New materials that improve carrier transport in the channel and methods to increase scalability (improve electrostatic control) need to be introduced.

As a channel material for enhanced hole transport, Germanium has become the subject of renewed interest. One critical challenge for the Germanium MOSFET fabrication is the difficulty to obtain a stable gate dielectric with high quality of the Ge/dielectric interface. The thermally grown Ge oxides are not suitable candidates due to their high solubility in water and their inferior thermal stability [1, 2]. As a viable alternative, high-k dielectrics and metal gate stacks are increasingly used in high-mobility research devices including those with relaxed Ge channels. The high dielectric constant allows for a thicker layer and thus acceptable gate leakage, while maintaining low Equivalent Oxide Thickness (EOT). The successful use of a ZrO$_2$ high-k gate dielectric directly on bulk Ge has been demonstrated [3]. The reported peak hole mobility of the Ge/ZrO$_2$ devices was about 2x that of the universal Si/SiO$_2$
devices. However, it has also been noted that the direct deposition of a high-\(k\) dielectric on Ge resulted in interfacial reactions and Ge diffusion into the dielectric [4]. At present, incorporating an interfacial layer between the high-\(k\) dielectric and Germanium is the most promising approach for achieving a high quality germanium-dielectric interface. Shang et al. [5] demonstrated p-MOSFETs with 40% increase in mobility over the so-called universal hole mobility curve, i.e. mobility vs. effective transverse electric field, when using germanium oxynitride (GeON) as an interfacial layer. Deposited nitrides such as AlN and Hf\(_3\)N\(_4\) have also been investigated [6, 7]. They offer certain advantages over the GeON such as smaller dielectric constant and better temperature stability. However, due to bulk traps and interface states the hole mobility is degraded [8, 9]. Silicon can also be incorporated as an interfacial layer. One drawback of using a silicon layer is the decreased gate to channel capacitance, i.e. the increased Capacitance Equivalent Thickness (CET) of the structure. Another disadvantage is that this layer is a parasitic path for hole transport at increased gate voltage which deteriorates the effective hole mobility in the device. Nevertheless, the highest reported hole mobility in unstrained-Ge p-MOFETs was achieved in structures with a silicon interfacial layer [10, 11]. Figure 1.1 summarizes the reported hole mobility in Ge for different interfacial layers and high-\(k\)/metal stacks.

![Figure 1.1](image-url)

Figure 1.1. Hole mobility in relaxed-Ge with different high-\(k\)/metal gate stack structures reported in the literature. The highest hole mobility enhancement over the universal curve (~40%) is obtained for Si as an interfacial layer. Experimental data from [10], [3], [5], [12], [13].
Increased hole mobility in Si and SiGe or Ge channels has been achieved through lattice-mismatch induced and process-induced compressive strain. Mobility enhancement of up to 10x over bulk Si channels has been demonstrated in strained-Ge pMOSFETs [14]. Biaxial strain is introduced in the Ge by pseudomorphically growing it on relaxed Si$_{1-x}$Ge$_x$ substrates. The in-plane lattice parameter of the epitaxially grown Ge is reduced to match the lattice parameter of the underlying Si$_{1-x}$Ge$_x$ layer. The level of the compressive strain is determined by the atomic fraction $x$ of the Ge in Si$_{1-x}$Ge$_x$ layer. In general, increasing the strain ($x$) leads to higher hole mobility as demonstrated by Lee et al. [15] and reproduced in Figure 1.2.

![Figure 1.2](image_url)

Figure 1.2. Hole mobility of strained-Si/strained-Ge dual-channel heterostructures grown on relaxed Si$_{1-x}$Ge$_x$ substrates [15]. Decreasing the atomic fraction of Ge in the Si$_{1-x}$Ge$_x$ substrates increases the strain in the Ge layer and therefore the hole mobility.

Currently, most of published work on strained Ge has been obtained on structures with a silicon cap to provide a better interface with the dielectric [14, 16, 17]. The work of Lee used a thick gate insulator (300 nm SiO$_2$), while Ni Chléirigh used 10 nm SiO$_2$ and Weber employed HfO$_2$ with a CET of 2.2 nm. As already mentioned, one drawback of structures with a Si cap above the Ge layer is the increased CET, defined as the equivalent SiO$_2$ thickness corresponding to the maximum measured capacitance $C_{\text{max}}$. 
Removing the Si cap entirely would mean smaller CET with the tradeoff of inferior electrical quality of the interface. This work explores the effect on the hole mobility of reducing the CET by removing the Si cap.

1.1. Thesis Goals

The hole mobility of strained-Ge ring-FETs with and without Si cap and with Al₂O₃/WN gate stack will be investigated in this work. The dependence of the mobility on the strained-Ge layer thickness and the silicon cap thickness will be explored. A quantitative assessment of mobility degradation after removing the cap will also be conducted.

1.2. Thesis Outline

In Chapter 2 some of the relevant parameters of the investigated structures such as bandstructure, effect of introducing strain, hole mobility and critical thickness are reviewed. In Chapter 3 the process flow for fabricating the device structures is covered. The results from the electrical measurements (I-V, Output, C-V characteristics) are analyzed in Chapter 4. The mobility extraction and its dependence on the Ge and Si layer thicknesses are covered in Chapter 5. Finally, summary of the experimental results and the suggestions for future work are included in Chapter 6.
Chapter 2

Theory

2.1. Properties of Si and Ge

In this section some of the properties of Si and Ge such as lattice structure, dependence of the energy band diagram on the level of strain and alignment of the bands in the Si/Ge/Si\textsubscript{1-x}Ge\textsubscript{x} structure will be discussed. It is important to note that all these properties determine the confinement of carriers in the channel and the level of mobility enhancement.

2.1.1 SiGe virtual substrates

One of the most important qualities of Si and Ge, that may lead to success in implementing Ge into CMOS fabrication, is that they can form fully miscible Si\textsubscript{1-x}Ge\textsubscript{x} alloys, with gradually varying properties over the composition range from x=0 to x=1. Both elements crystallize in a random cubic diamond lattice (as shown schematically in Figure 2.1) with a lattice constant determined by Vegard’s rule which is a linear interpolation between the Si and the Ge lattice constants.

\[ a_{SiGe} = a_{Si}(1-x) + a_{Ge}(x) \]  

Eq. 2.1

Here \( a_{Si} \) (5.646 Å) is the lattice constant of Si, \( a_{Ge} \) (5.431 Å) is the lattice constant of Ge and \( x \) is the Ge fraction in SiGe alloy.
Figure 2.1. Schematic representation of Si, Ge and Si$_{1-x}$Ge$_x$ lattice structures. The lattice constants of Si and Ge are 5.646Å and 5.431 Å, respectively. The SiGe lattice constant can be calculated according to Vegard's rule.

Once grown on Si, Si$_{1-x}$Ge$_x$ layers can serve as “virtual” substrates, with various lattice constants, for subsequent layer growth. There are a few reasons for implementing epitaxial growth for fabrication of such substrates. The relative ease of controlling the concentrations of the different reactants in a Chemical Vapor Deposition system, (e.g. LPCVD system) allows for access to a wide range of SiGe compositions. The difficulty in creating single crystal SiGe substrates and the need for compatibility with existent Si processing equipment also necessitate the use of “virtual” substrates. The mismatch between Si/Ge and SiGe lattice constants can be used for introducing biaxial tensile/compressive strain into the layers. When growing epitaxially a thin layer on another, thicker, layer with different lattice constant, the top layer expands or shrinks to accommodate the difference in the lattice constants and as a result strain is induced in it. Figure 2.2 depicts the process of introducing strain in Ge and Si by epitaxially growing them on a Si$_{1-x}$Ge$_x$ substrate.

Figure 2.2. Introducing tensile/compressive strain in Si/Ge layers by growing them on a, presumed thick, SiGe “virtual” substrate.
2.1.2. Review of Si, Ge and SiGe bandstructures

The conduction band edge is comprised of a sixfold degenerate $\Delta$ valley in Si and an eightfold degenerate $L$ valley in Ge. The valence band is comprised of degenerate heavy hole (HH) and light hole (LH) bands at the $\Gamma$ point for both Si and Ge. The SiGe alloy has Si-like structure for Ge fractions up to $x = 0.85$ and becomes Ge-like for higher Ge fractions. The conduction band edge changing from $\Delta$ to $L$ valley results in a rapid decrease in the bandgap for SiGe alloys with Ge fraction above 0.85 [17]. The change in the bandgap of SiGe is mainly attributed to the valence band shifting upwards with increasing Ge fraction. The shift in conduction band is relatively small.

2.1.3. Biaxial strain

The introduction of biaxial tensile strain in the Si lattice results in net downwards energy shift in the valence and conduction band edges [18]. Introducing strain causes the 6-fold degenerate $\Delta$ valley in the conduction band to split, with the $\Delta_2$ conduction band shifting downwards. Degenerate light-hole (LH) and heavy-hole (HH) valence bands also split, with a shift downwards of the LH band. The shift in the LH band edge as seen from Figure 2.3 (a) is less than 50 meV with respect to the unstrained case ($x = 0$). It can also be noted that the Si/Si$_{1-x}$Ge$_x$ structure is of type-II configuration (staggered gap).

![Diagram](image)

Figure 2.3. Conduction and valence bands as a function of substrate composition $x$, for Si/Si$_{1-x}$Ge$_x$ structure (a) and Ge/Si$_{1-x}$Ge$_x$ structure (b) [18].
For Ge, the introduction of biaxial compressive strain causes the degenerate LH and HH bands to split with the HH band shifting upwards (Figure 2.3 (b)). The Ge/Si$_{1-x}$Ge$_x$ structure has for most compositions a flat conduction band, but it switches to a type-I configuration (straddling gap) for $x > 0.5$. The conduction band offset occurs for $0.5 < x < 0.85$ between the L band in the strained Ge layer and the Δ band in the substrate, for higher $x$ between the L band in both layers. The HH valence band in the active Ge layer defines the valence band maximum independently of the substrate composition.

An example of a typical band alignment for Si/Ge/Si$_{1-x}$Ge$_x$ is shown in Figure 2.4 (adapted from Ni Chléirigh [17]).

It can be seen that the alignment of the bands for Si/Ge/Si$_{1-x}$Ge$_x$ structure form a quantum well for hole confinement in the Ge layer. Better confinement can be expected for higher levels of strain in the Si layer, resulting in LH band shifting further down. However, for sufficiently large vertical fields, i.e. upwards bend of the bands, holes can be pulled into the Si layer and the beneficial effect of utilizing the higher mobility Ge for hole transport can be lost.
Although the conduction and valence band offsets ($\Delta E_c$ and $\Delta E_v$) between the different layers can be estimated with experimental and theoretical work, this study is not carried out in this thesis.

2.2. Hole mobility

The hole mobility is a material parameter and for low fields is given by

$$\mu_h = \frac{q \tau}{m^*} \quad Eq. 2.2$$

where $q$ is the elemental charge, $\tau$ is the mean time between scattering events and $m^*$ is the effective mass. It can be seen from Equation 2.2 that reducing the effective mass and the frequency of scattering events is expected to result in higher mobility.

2.2.1 Effective mass

As already shown in Figure 2.3, introduction of compressive strain in Ge leads to splitting of HH and LH bands with the HH band moving up in energy. Even though the effective mass for holes is difficult to quantify, due to the non-parabolic and anisotropic valence bands, it was shown by Ni Chléirigh [17] that the HH effective mass decreases with initial introduction of strain. Further increase of the strain did not lead to effective mass reduction. Table 2.1 summarizes the simulated values for HH effective mass for relaxed and strained-Ge layers [17].

| Table 2.1. Effective masses for relaxed and compressively strained Ge |
|-------------------------|-------------------------|-------------------------|
|                         | Relaxed-Ge              | Ge/Si$_{0.3}$Ge$_{0.7}$ | Ge/Si$_{0.5}$Ge$_{0.5}$ |
| HH <100>                | 0.33$m_e$               | 0.21$m_e$               | 0.15$m_e$               |
| HH <001>                | 0.33$m_e$               | 0.20$m_e$               | 0.20$m_e$               |
Another study by Sawano et al.[19] showed that the induced strain additionally causes strong nonparabolicity of the hole band, making the effective mass highly dependent on the hole density. Roessner et al also demonstrated that the effective mass drastically increased with increase of hole density [20]. Figure 2.5 (a) shows the hole effective mass as a function of hole density for two different strain levels corresponding to virtual substrate Ge compositions of 76% and 52%. As mentioned, increasing the strain allows for low effective mass even for high hole densities. Figure 2.5 (b) shows the effective mobility dependence on the strain level for fixed hole density of $2\times10^{12}$ cm$^{-2}$.

![Figure 2.5](image)

**Figure 2.5.** Hole effective mass dependence on the hole density for different strain level (a) and hole effective mass dependence on the strain for hole density of $2\times10^{12}$ cm$^{-2}$ (b) [19].

Even though the high hole density required for high conductivity can lead to increase of the effective mass and therefore decrease in the mobility, higher level of strain has proven beneficial in reducing this dependence. For a given hole density, increasing the strain from 0.8% to 2.8% reduces the effective mass from $0.195m_0$ down to $0.15m_0$. This demonstrates that $m^*$ can be effectively reduced by increasing the strain in the Ge channel.
2.2.2. Scattering mechanisms

The scattering time \( \tau \) depends on the different scattering mechanisms and can be calculated according to

\[
\frac{1}{\tau} = \frac{1}{\tau_{ii}} + \frac{1}{\tau_{ph}} + \frac{1}{\tau_{is}} \quad Eq.\ 2.3
\]

where \( \tau_{ii} \) refers to ionized impurity scattering, \( \tau_{ph} \) to phonon scattering and \( \tau_{is} \) to interface impurity scattering.

The ionized impurity scattering (also coulombic scattering), as the name suggests, is due to the presence of ionized impurities in the device. The effect of this scattering mechanism on the mobility can be highly reduced when implementing channels with low dopant concentration.

Phonon scattering is caused by quantized lattice vibrations, both optical and acoustic. The interband optical phonon scattering can be significantly reduced by introducing strain into the channel due to the splitting of the HH and LH bands. The acoustic phonon scattering is given by

\[
\frac{1}{\tau_{pha}} = \frac{\pi D_{a} k_{B} T_{L}}{\hbar c_{i} W_{fi}} g_{2D}(E) \quad Eq.\ 2.4
\]

Here \( D_{a} \) is the deformation potential for acoustic phonon scattering, \( k_{B} \) is Boltzmann's constant, \( T_{L} \) is the lattice temperature, \( c_{i} \) is the elastic constant of the material, \( W_{fi} \) is the inversion layer thickness and \( g_{2D}(E) = m^{*}/\hbar^{2} \) is the density of states in 2D quantum well [17]. According to Eq.2.4 and the 2D density of states expression, introducing strain is expected to reduce \( g_{2D} \) by reducing the effective hole mass and therefore to result in lower scattering rate. On the other hand, increasing the confinement (decreasing \( W_{fi} \)) increases the scattering rate and reduction in mobility is expected for thinner Ge channels.

The third scattering mechanism from Equation 2.3 is the interface impurity scattering. Gamiz et al [21] showed that the scattering is higher for carriers closer to the interface. Increasing the surface potential leads to increased band bending at the surface and closer confinement of the carriers to the scattering potential and therefore, a very strong dependence of the interface scattering on the inversion charge density ensues.
Two separate studies in scattering mechanisms in strained-Ge MOSFETs [19, 20] confirmed that the main scattering mechanisms in those structures were ionized impurities scattering (for low inversion charge) and surface impurity scattering (for high inversion charge). Figure 2.6 shows the contribution of each scattering mechanism to the overall effective mobility as a function of the inversion charge density [20].

![Graph showing scattering mechanisms contribution to mobility]

**Figure 2.6.** Different scattering mechanism contributions to the overall mobility of strained-Ge MOSFET [20]. Ionized impurity scattering dominates at low $N_{inv}$, and the interface impurity scattering becomes more important at high $N_{inv}$.

**2.3. Critical thickness**

Strained layers can be pseudomorphically grown up to a certain thickness that depends on the lattice mismatch between the layers and the substrate and the processing temperatures. Above that thickness the strained layers start to relax through dislocation formation [22]. The critical thickness can be increased by decreasing the strain in the layers, i.e. using virtual substrates with lower mismatch in Ge content. High layer deposition and subsequent processing temperatures also favor the formation of dislocations and relaxation. Figure 2.7 (a) shows the effect of strain and temperature on the critical thickness for
strained-SiGe. The experimental data are from [23-27]. Figure 2.7 (b) shows the strained-Ge hole mobility enhancement over the so-called universal mobility of holes in relaxed Si, for different strain levels and strained-Ge layer thickness. The highest mobility is obtained for strain level corresponding to 40-50 % Ge content in the SiGe virtual substrate and Ge layer thickness between 6 nm and 10 nm. Increasing the Ge layer thickness from 4 nm to 8 nm leads to ~4.5x increase in mobility enhancement for the same strain level (sample Ge/50, which denotes strained-Ge on 50 % SiGe substrate) suggesting better hole confinement in thicker layers. The monotonic decrease in the mobility for thickness above 10 nm is possibly due to relaxation of the layer (Figures taken from [17]).

![Graph](image)

Figure 2.7. (a) Critical thickness for Si$_{1-y}$Ge$_y$ grown on Si substrate as a function of Ge fraction, y. Increasing of the strain and the processing temperature decreases the critical thickness. (b) Mobility enhancement over the Si control as a function of channel thickness for strained-Ge channel. The notation Ge/X describes Ge layer on X % SiGe substrate.

2.4. Chapter Summary

Introduction of strain in the channel was proven beneficial in increasing hole mobility by reducing the effective hole mass and the rate of phonon scattering events. The increase of channel layer thickness leads to hole mobility increase up to a certain critical thickness. On the other hand, a very thin Ge layer can result in mobility degradation due increased phonon scattering and worse confinement in the channel.
Keeping the dopant concentration in the channel low and improving the interface quality are also necessary conditions for reducing scattering and improving the mobility of the devices.
Chapter 3

Experimental process

3.1. Device fabrication

The wafers used in this experiment were grown in an Applied Materials low pressure chemical vapor deposition (LPCVD) "Epi-Centura" system. A 4-μm-thick graded buffer was first grown with starting concentration of 2% Ge and the percentage was linearly increased to a final composition of 40% Ge. This well known technique has been shown to minimize the dislocations at the surface of the graded buffer [28, 29]. A 750-nm-thick relaxed Si$_{0.6}$Ge$_{0.4}$ layer was grown on the graded buffer to form the virtual substrate for the device structures. To ensure good substrate contact, the graded buffer and the relaxed layer were in-situ doped with phosphorus to a nominal doping level of $10^{17}$ cm$^{-3}$ during epitaxial growth.

Unintentionally-doped SiGe of 15-nm thickness was grown on top of the relaxed buffer to reduce the impact of P autodoping on channel mobility and sensitivity to doping variations. Nevertheless, the strained Ge and strained Si layers are expected to be unintentionally doped by P autodoping, likely to a level of $\sim5 \times 10^{16}$ cm$^{-3}$. Three different wafers were grown with varying thickness of these layers to investigate the effect of the germanium and silicon layer thickness. The notation used in this work to describe the different structures is x/y, where x is strained-Silicon cap thickness (nm) and y is strained-Germanium layer thickness (nm). An epitaxially grown silicon control wafer was processed along with
the device wafers. Schematic cross sections of the device structures are shown in Figure 3.1 and additional information about the structures and the growth conditions can be found in Appendix A.

After epitaxial growth all of the wafers were directly transferred to the atomic layer deposition (ALD) chamber without an intervening cleaning step. This was done to preserve the initially designed thickness of the Si cap layer. In-situ ozone treatment for 10 min (10 cycles) was conducted before dielectric deposition. This step has been shown to enhance the mobility of the relaxed Ge MOSFETs by forming an interfacial passivation layer, very likely composed of GeO₂ [12].

![Figure 3.1. Schematic cross-sections of the device structures investigated in this work: (a) 3.5/5, (b) 3.5/9.5, (c) 0/8.5 and (d) Si control. The graded buffer and the relaxed buffer layer are doped with Phosphorus to concentration of 5x10¹⁶ cm⁻³.](image)

Aluminum oxide (Al₂O₃) was chosen as gate dielectric for its superior C-V behavior and lower interface state density compared to Zr- and Hf- based layers deposited on Ge in this same ALD system [12]. The aluminum oxide was deposited at temperature of 250 °C using tri-methyl-aluminum (TMA) and water sources. To ensure low leakage, 6 nm (60 cycles) of dielectric thickness was chosen. As a gate metal, 40
nm of WN was deposited in situ in 800 ALD cycles at 340 °C. The ring transistor gates were then patterned on the wafers and the WN was etched in the LAM Rainbow metal etch system using a Cl₂ plasma. The source and drain regions were implanted with Boron at energy of 10 keV and dose of 4x10¹⁵ cm⁻² with the photoresist-WN gate stack acting as a mask. After stripping the photoresist, a 200-nm-thick PECVD SiO₂ was deposited to later serve as an interlayer dielectric (ILD). The dopants were activated by 30 min forming gas anneal (FGA) at three different temperatures: 450 °C, 500 °C and 600 °C. These temperatures were chosen for consistency with the preliminary experiments done on similar device structures. The preliminary experiments had shown considerable decrease of the series resistance for the 500 °C annealed samples compared to the 450 °C ones, presumably because of increased S/D dopant activation at the higher temperature. The 600 °C anneal was added to the current experiment in an attempt to further decrease the series resistance. After the photo steps for via and metal etch, Ti/Al (50 nm/500 nm) was deposited on the front side of the wafers. A backside contact was formed via deposition of 1 μm Al. A 30 min final sinter anneal was performed at 420 °C in FG ambient. A schematic process flow with the corresponding splits is shown in Figure 3.2. The detailed process flow can be found in Appendix B.

Figure 3.2. Process flow of p-ringFETs with the different splits. Due to contact and contamination problems with the 600 °C-annealed samples, only the 3.5/5 structure (see text for definition) was investigated at that temperature.
3.2. Device layout

The devices were fabricated using three-mask process (gate, via, metal) and the layout of the ring-FETs and the relevant parameters are shown in Figure 3.3. Devices with three different lengths of 5, 10 and 20 μm were used to extract the parameters of interest. The total width of the devices was approximated as the average perimeter of the channel ring between the drain and source sides of the gate. This approach was chosen over the commonly used geometry factor (G) approximation for the relatively long channel devices used in this experiment [30].

![](image)

Figure 3.3. Ring-FET mask and relevant device dimensions, used in the mobility extraction.

<table>
<thead>
<tr>
<th>L, μm</th>
<th>W₁, μm</th>
<th>W₂, μm</th>
<th>W = (4 \frac{(W₁ + W₂)}{2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>90</td>
<td>100</td>
<td>380</td>
</tr>
<tr>
<td>10</td>
<td>180</td>
<td>200</td>
<td>760</td>
</tr>
<tr>
<td>20</td>
<td>160</td>
<td>200</td>
<td>720</td>
</tr>
</tbody>
</table>

3.3. Processing Problems

In general, the process used to fabricate the ring-FETs was successful. However, formation of bubbles was observed on the wafer surface after implant annealing and presence of particles after implantation was noted while examining the wafers in different stages of fabrication. Both types of defects were relatively large with a size on the order of a few microns. The randomness of occurrence of these defects made it difficult to draw conclusions about their nature. It can be speculated that the formation of bubbles
is due to the high ramp rate of the anneal temperature, preventing trapped gas from the ALD layer from escaping the interface. This, however, does not explain the lack of bubbles on some of the wafers of the same lot. To examine the particles, the samples were characterized with Energy-dispersive X-ray spectroscopy (EDS). The species found to constitute the particles were Al and O. However, the particles were noticeable only on the wafers with a Si cap, suggesting a possible epitaxial growth problem or problem with adhesion of the high stress WN layer to the Si cap layer. Particles were not observed immediately after epitaxial growth. These issues need to be further investigated in the future.

3.4. Chapter Summary

Ring-FETs with varying Ge and Si thicknesses were successfully fabricated using a three-mask process. A high-k/metal gate stack (Al₂O₃/WN) was ALD deposited on all samples at the same conditions. The samples were post-implantation annealed at a number of temperatures to investigate the effect of the anneal temperature on hole mobility. Some defects were observed on the wafer surface at different stages of fabrication and their formation needs to be addressed in the future.
Chapter 4

Electrical Measurements

4.1. I-V measurements

The current–voltage (I-V) characteristics were measured for all of the devices annealed at 450 °C and 500 °C. Out of devices annealed at 600 °C, only the 3.5/5 devices showed adequate characteristics and only these were used in the analysis. The transfer characteristics on linear and semi-log scales are shown in Figure 4.1 (a) and (b), respectively. A major concern is the threshold voltage shift, noticeable for the structures with a silicon cap. Drain leakage current is also considerable which is in part expected due to the low bandgap in the strained Ge channel, and the low effective bandgap of the strained Si/strained Ge structure. Though definitive identification of the leakage mechanism could not be carried out, most likely the leakage is due to poor quality of the drain junctions, which have particularly large area in these ring-FET devices.

The Si control showed 10x lower current in strong inversion compared to the Ge. This is in part due to the inherently lower hole mobility in Si. Another reason for the low current is the inadequate dopant activation. Typically, boron in silicon is activated at temperatures above 800°C [31, 32]. The relatively low temperature used in this experiment (450 °C – 600 °C) resulted in poor activation of the dopants and therefore very low current. As these samples could not be used as adequate references, most of the...
measured and extracted parameters of the strained-Ge ring-FETs were compared to the universal mobility for SiO₂/Si [13].

Figure 4.1. Comparison of measured transfer characteristics in linear (a) and semi-log (b) scales for 3.5/9.5, 3.5/5, 0/8.5 and Si control p- ring-FETs (L = 20 μm, Al₂O₃ dielectric, EOT ~4 nm, WN gate). Very large threshold voltage shift is observed for the capped devices. The current in strong inversion in the silicon control is about 10x lower than in the germanium devices, primarily because of higher S/D resistance in Si due to poorer dopant activation, and also in part due to inherently lower hole mobility in Si. The off-state leakage of the Si/Ge and Ge devices is considerable and is possibly related to the cause of the large threshold voltage shift.

Figure 4.2 shows the transfer characteristics obtained for forward and reverse sweep of the gate voltage. A hysteresis of about 85 mV is observed for 0/8.5 device and up to 2 V at high current drive for the Si-capped devices. There is a notable “dent” in the I-V characteristics for the Si-capped devices in reversed sweep which seems to be independent of the number of sweeps and the initial sweep direction.

To ensure that this “memory effect” is not due on the high voltage the structures were subject to, the capless sample was also stressed up to V_G=5.5 V. It can be seen from Figure 4.3 that the gate leakage is similar to the Si-capped structures suggesting similar gate dielectric thickness and charge trapping behavior. However, there is no visible “dent” in the I-V characteristics even after stressing the device, suggesting that the presence of a Si-cap is somehow related to its occurrence. This effect has not been
reported on previously investigated structures with high-k on Si and LTO on s-Si/s-Ge and it may be due to a combination of trapping mechanisms at both the high-k dielectric/Si and Si/Ge interfaces.

Figure 4.2. Comparison of measured hysteresis for 3.5/9.5, 3.5/5, 0/8.5 p- ring-FETs (L 20 μm, Al2O3 dielectric, EOT ~4 nm, WN gate). The hysteresis for the capped structures is considerable even at low currents and reaches 2V for I_D ~0.5 mA.

Figure 4.3. DC gate leakage current in 0/8.5, 3.5/5, 3.5/9.5 device structures. All devices show similar DC gate leakage, implying that the Si-cap presence is related to the "memory effect" seen in devices 3.5/5 and 3.5/9.5.
4.2. Output characteristics

The output characteristics were measured at $V_{DS}$ from 0 to -5 V and are shown in Figure 4.4. Increase of the current was observed for the 500 °C compared to 450 °C anneal for most of the structures. Further increasing the anneal temperature to 600 °C led to poorer output characteristics and smaller current than for the devices that received 450 °C anneal which is more likely due to the non-optimized process, resulting in contact problems, rather than the higher temperature alone.

![Figure 4.4. Measured Typical Output Characteristics of 3.5/5 ring-FET with 30 nm WN/6 nm Al₂O₃ gate stack, annealed at three different temperatures. The 600 °C sample shows poorer output characteristics which might be due to existing contact problems.](image)

4.3. Split C-V measurement

4.3.1. Measurement setup

For mobility calculation we are mostly interested in measuring the gate-to-channel capacitance ($C_{GC}$) and therefore the “Split C-V” technique [33] was used in characterizing the mobility behavior. The
measurement setup requires grounding the substrate terminal and connecting S and D terminals together. Since the source and drain are isolated from the bulk with pn-junctions, only holes from the channel can flow into and out of the S/D regions. Therefore, the measured current corresponds to the inversion charge $Q_{inv}$. The measurement frequency need to be optimized because if too low the oxide interface states could also respond to the signal and if it is too high parasitic RC effects may lead to erroneously small value for $C_{GC}$. Even though the behavior of the devices was investigated for a wide range of frequency from 10kHz-1MHz, only the 50kHz curve was used for mobility extraction.

### 4.3.2. C-V characteristics

Split capacitance-voltage (C-V) characteristics were measured in the 10 kHz-1 MHz frequency range. There was notable frequency dispersion and hysteresis in all samples. The 3.5/5 and the silicon control samples showed ~7% decrease in $C_{max}$ between 10 kHz and 50 kHz capacitance curves. High density of interface states in the upper half of the bandgap is most likely responsible for the large frequency dispersion of the measured devices. The frequency dispersion could also be due in part to the high contact resistance in these devices. The lowest frequency dispersion was observed in sample 0/8.5, resulting in less than 1% difference in $C_{max}$ at 10 and 50 kHz. Sample 3.5/5 showed hysteresis of 90 mV, compared to 230 mV for sample 0/8.5. The hysteresis of all samples was found to be dependent on the voltage/capacitance value as well as on the number of sweeps and therefore a fair comparison between I-V and C-V hysteresis could not be made. Figure 4.5 shows the C-V characteristics of the two Si-capped samples – 3.5/5 (figure 4.5a) and 3.5/9 (figure 4.5b). Anomalous CV curves are observed for device 3.5/9.5 with very high capacitance in accumulation. It was already shown in Figure 4.3 that the DC gate leakage current in the two capped devices is very high but still comparable, suggesting that the gate DC leakage is not the reason for the anomalous C-V curves. It is reasonable to believe that the excessive junction leakage due to the possible strain relaxation (associated with the thicker Ge layer) and resulting
dislocation formation in the channel is the more probable reason for the trapping and the high capacitance in accumulation. In fact, when "split CV" is performed with the S/D contacts shorted to the body, the capacitance always increases to $C_{\text{max}}$ in accumulation.

Figure 4.5. Forward and reverse sweep C-V characteristics of (a) 3.5/5 and (b) 3.5/9.5 device with 500 °C SD activation. The hysteresis was calculated at capacitance $C = (C_{\text{max}} - C_{\text{min}})/2$. There is a notable frequency dispersion leading to 7% decrease in $C_{\text{max}}$ value for frequency of 50kHz, compared to the capacitance value at 10 kHz (a). The anomalous C-V curves, with very high leakage current in accumulation, were observed in all devices with thick germanium layer (b), suggesting partial relaxation of the strain.

Figure 4.6. Effect of the anneal temperature on the C-V characteristics for 3.5/5 device. Hysteresis is not changed by annealing at the higher temperature of 600 °C compared to 500 °C.
Figure 4.6 shows the effect of different annealing temperatures on the CVs for the 3.5/5 sample. Annealing at higher temperature resulted in less frequency dispersion with no effect on hysteresis which supports the possibility that dispersion may be due to RC effects. Using a different MOSFET structure and optimizing the process for better dopant activation could be some of the possible steps to help reduce this effect.

4.4. Chapter Summary

In this chapter the electrical behavior of the strained-Ge ring-FETs was investigated. Very high threshold voltage shift and a “dent” in the I-V characteristics were observed in the devices with a Si-cap suggesting that the presence of the cap may be related to these effects. The gate leakage, being similar in all of the investigated structures, was overruled as a possible cause. Anomalous C-V curves with very high current in accumulation were measured for the device with thick-Ge channel. A combination of strain relaxation and the lack of isolation are considered primary reasons for the high leakage. The effect of the S/D activation temperature was also investigated. The reduced frequency dispersion for increased annealing temperature suggests RC effects playing a role in the device operation.
Chapter 5

Mobility extraction and analysis

Extracting the mobility of the ring-FETs required calculation of a number of parameters, such as channel dopant concentration, threshold voltage and series resistance. Most of the calculations and parameter extractions were performed on the devices that received 500 °C anneal. This temperature was chosen after the preliminary results showed lower series resistance of the samples annealed at 500 °C, compared to those annealed at 450 °C. The series resistance was notably degraded after the annealing temperature was increased to 550 °C.

5.1. Threshold voltage extraction

The threshold voltage was determined using the linear extrapolation technique. For this technique the drain current was measured as a function of gate voltage at a low drain voltage of 50 mV to ensure operation in the linear MOSFET region. The point of maximum slope (maximum transconductance) on the $I_D - V_{GS}$ curve was then identified. Fitting a straight line to the $I_D - V_{GS}$ curve at that point and extrapolating it to $I_D = 0$ gave the value of the threshold voltage. This technique can be analytically expressed by:

$$V_T = V_{GS1} - \frac{I_{D1}}{g_{m1}}$$  \hspace{1cm} (Eq. 4.1)
Where $V_{GS1}$, $I_{D1}$ are the gate voltage and drain current, corresponding to the maximum transconductance $g_{m1}$.

### 5.2. Doping concentration extraction

The effective doping concentration, $N_D$, was extracted from the threshold voltage shift for different body biases. The relevant doping for $V_T$ shift with applied $V_{BS}$ in these structures is the doping of the SiGe layer since this is where most of the depletion region resides. Four different devices on each wafer were measured at five different values of the body bias.

The dependence of $V_T$ on the body bias is given by:

$$V_T(V_{SB}) = V_{T0} + \gamma \left( \sqrt{\varphi_{sth} + V_{SB}} - \sqrt{\varphi_{sth}} \right)$$

(Eq 4.2)

where $V_{T0}$ is the threshold voltage at $V_{SB}=0$ V, $\varphi_{sth}$ is the surface potential at threshold, and $\gamma$ is the body effect factor given by:

$$\gamma = \frac{\sqrt{2q\varepsilon_{SiGe}N_D}}{C_{ox}}$$

(Eq. 4.3)

Here $q$ is the charge of the electron, $\varepsilon_{SiGe}$ is the dielectric constant for the 40% SiGe and $C_{ox}$ is the capacitance, associated with the gate dielectric.

The surface potential can be calculated approximately from:

$$\varphi_{sth} = \frac{2kT}{q} \ln \frac{N_D}{n_i}$$

(Eq. 4.4)

where $k$ is Boltzmann’s constant ($8.617 \times 10^{-5}$ eV/K), $T$ is the temperature (K) and $n_i$ is the intrinsic carrier concentration of the substrate. The intrinsic carrier concentration in the 40% SiGe substrate was found as a linear interpolation from published data [34]. The value extracted and used in the current work is $n_i = 0.96 \times 10^{13}$ cm$^{-3}$. This corresponds to $E_g = 0.986$ eV [35].

Since $N_D$ appears in both Eqs 5.3 and 5.4, best fit of Eq. 5.2 to experimental $V_T$ data requires an iterative process. The initial value of $N_D$ was assumed to be the designed level of $10^{17}$ cm$^{-3}$ in the SiGe layer and
the surface potential was then iteratively calculated, consistently with the body factor coefficient until best match of Eq. 5.2 to experimental $V_T$ vs. $V_{SB}$ data was achieved. The body factor was calculated to be in the range of 0.12 - 0.3 $V^{1/2}$ for the different structures.

The doping was then calculated from the body factor expression, Eq. 5.3:

$$N_D = \frac{(\gamma C_{ox})^2}{2 \varepsilon_{SiGe} q}$$  \hspace{1cm} (Eq. 5.5)

The dielectric constant for the 40% SiGe substrate was calculated as linear interpolation between the values for pure Si and pure Ge, according to Vegard’s law:

$$\varepsilon_{Si_{1-x}Ge_x} = (1-x)\varepsilon_{Si} + x\varepsilon_{Ge}$$  \hspace{1cm} (Eq. 5.6)

Substituting the values for the dielectric constants of Si and Ge (11.7 and 16), the dielectric constant of 40% germanium was found to be 13.42. The extracted doping concentration was in the range of 1x10$^{16}$-2x10$^{17}$ cm$^{-3}$ which is reasonably close to the target doping of 10$^{17}$ cm$^{-3}$. The average value of $N_D=5x10^{16}$ cm$^{-3}$ was used for all subsequent calculations.

### 5.3. Series resistance extraction

One problem with all the MOSFETs in this experiment is the large series resistance of the S/D regions. This is due to the limited stability of high-k dielectric, which limits the thermal budget in the fabrication process. The high series resistance affects the threshold voltage and mobility extraction and should therefore be accounted for when calculating these parameters. The total resistance of a MOSFET can be expressed by

$$R_{tot} = R_{ch} + R_{ext} = \frac{L - \Delta L}{W \mu_C C_{ox}(V_{SC} + V_T)} + R_{ext}$$  \hspace{1cm} (Eq. 5.7)

where $R_{tot}$, $R_{ch}$ and $R_{ext}$ are the total resistance, channel (intrinsic) resistance and extrinsic resistance, respectively. A plot of $R_{tot}W$ versus $L$ for devices with different gate length $L$ and varying overdrive ($V_{SC}+V_T$) voltages has lines intersecting at one point giving both $R_{ext}W$ and $\Delta L$. 

The extracted values for $V_T$ and $R_{ext}$ are shown in Table 5.1. Due to contact problems the series resistance of the 3.5/9.5 sample at 500 °C could not be extracted. To facilitate comparison the series resistance was assumed to be the same as 3.5/5 structure.

Table 5.1. Extracted values of $V_T$ and $R_{ext}$

<table>
<thead>
<tr>
<th>T (°C)</th>
<th>450</th>
<th>500</th>
<th>600</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample</td>
<td>3.5/5</td>
<td>3.5/9</td>
<td>0/8.5</td>
</tr>
<tr>
<td>$V_T$ (V)</td>
<td>4.52</td>
<td>-</td>
<td>0.62</td>
</tr>
<tr>
<td>$R_{ext}$*W (kΩ·μm)</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

5.4. Fixed and interface trapped charge

The devices with silicon cap showed large threshold voltage shift. The fixed and interface trapped charge density associated with the threshold voltage shift was estimated using Eq. 5.8.

$$V_T = V_{FB} - \varphi_{sth} - \frac{\sqrt{2q\varepsilon SiGeN_D\varphi_{sth}}}{C_{OX}} - \frac{Q_f + Q_i}{C_{OX}} \quad (Eq. \ 5.8)$$

Here $Q_f$ is the fixed charge, $Q_i$ is the interface trapped charge and $V_{FB}$ is the flatband voltage given by:

$$V_{FB} = -\frac{1}{q}(W_S - W_M), \quad (Eq. \ 5.9)$$

where $W_S$ and $W_M$ are the semiconductor and ALD WN work functions, respectively. The value of $W_M$ found in literature [35] is 5.3eV and $W_S$ was calculated assuming Si$_{0.6}$Ge$_{0.4}$ substrate, according to:

$$W_S = \chi_S + kT \ln \frac{N_C}{N_D}, \quad (Eq. \ 5.9)$$

where $\chi_S$ is the electron affinity of the substrate, $N_C$ is the effective density of states in the conduction band.

30
The ideal threshold voltage (i.e. assuming zero fixed and interface charge) for these devices was calculated to be 0.55 V. Then, the threshold voltage shift of 3.9 V (for 3.5/5 structure) corresponds to charge density of \(-1.7 \times 10^{13} \text{ cm}^{-2}\). Even though the source of the increased interface and fixed charges could not be determined it can be speculated that they may have been introduced during compromised device layer growth and deposition and perhaps may be related to the presence of the particles mentioned above. Regardless of the existence of the large fixed charge the mobility of all devices was extracted.

### 5.5. Mobility extraction

The expression for the mobility was obtained from the equation of the drain current for a long channel pMOSFET with width \(W\) and length \(L\):

\[
I_D = \frac{W \mu_p Q_{inv} V_{DS}}{L} \quad \text{(Eq. 5.10)}
\]

where \(W\) is the width of the MOSFET, \(\mu_p\) is the hole mobility, \(Q_{inv}\) is the inversion charge density, \(V_{DS}\) is the drain to source voltage.

The mobility was then calculated as

\[
\mu_p = \frac{L}{W V_{DS} Q_{inv}} \quad \text{(Eq. 5.11)}
\]

#### 5.5.1 Calculating \(Q_{inv}\)

Two approaches were used in this work for calculating the charge density. The approach giving better results is based on a direct measure of \(Q_{inv}\) from the split-CV measurements, with the mobile channel charge density determined from the gate-to-channel capacitance per unit area, \(C_{GC}(V_{GS})\), according to

\[
Q_{inv} = \int_{-\infty}^{V_{GS}} C_{GC}(V_{GS}) dV_{GS} \quad \text{(Eq. 5.12)}
\]
The second approach approximates the charge by the oxide capacitance per unit area

\[ Q_{\text{inv}} = C_{\text{max}}(V_{\text{SG}} + V_T) \]  \hspace{1cm} (Eq. 5.13)

The second approach was used to calculate the charge density for the samples with anomalous CV characteristics, where integration of the C-V characteristics to obtain the inversion charge was not possible.

The two approaches for calculating mobility are illustrated in Figure 5.1 for device 3.5/5 with series resistance correction. It can be noted that the approximation with \( C_{\text{max}} \) leads to overestimation of the mobility, which is due to significant underestimation of the charge density at low inversion charge densities, i.e. for \( V_{\text{GS}} \) close to \( V_T \). Good agreement between the two approaches is observed for inversion charge densities larger than \( 8 \times 10^{12} \text{ cm}^{-2} \). Therefore, to achieve a reasonably good estimate of the mobility enhancement between the different samples and the universal curve, the enhancement factor was calculated for \( N_{\text{inv}} \) in that range.

![Figure 5.1](image)

Figure 5.1. Two approaches to calculate the charge illustrated for 3.5/5 device with series resistance correction. For low inversion charges the \( C_{\text{max}} \) approximation fails to provide a good estimation of the actual mobility due to underestimation of the charge density for \( V_{\text{GS}} \) close to \( V_T \). The hole mobility for \( N_D = 5.1 \times 10^{14} \text{ cm}^{-3} \) is shown for comparison (from Takagi et al [13]).
5.5.2. Series resistance correction

The mobility was corrected for series resistance according to:

\[ \mu_p = \frac{L}{W} \frac{I_D}{(V_{DS} - I_D R_{ext}) Q_{inv}} \]  

(Eq. 5.14)

Series resistance correction resulted in 16.5% increase in the mobility at \( N_{inv} = 10^{13} \text{cm}^{-2} \) for 3.5/5 device at 500 °C and 6.7% increase at 600 °C suggesting better dopant activation for the higher temperature. The mobility of the 0/8.5 device at the same inversion charge density showed less dependence on the series resistance - 5.3%. The hole mobility with and without series resistance correction is given in Figure 5.2 for 3.5/5 device.

![Hole Mobility Curves](image)

Figure 5.2. Hole mobility curves before and after series resistance correction for 3.5/5 device with the corresponding enhancement factors over the hole mobility curve for \( N_D = 5.1 \times 10^{16} \text{cm}^{-3} \) (from Takagi et al. [13]).

5.5.3. Hole mobility dependence on the strained-Ge thickness

To study the effect of strained-Ge thickness on hole mobility while keeping silicon cap thickness constant, the mobility of devices 3.5/5 and 3.5/9.5 was compared and the results are plotted in Figure 5.3. Due to the lack of sufficient data to extract the series resistance of 3.5/9.5 device, the correction was done
assuming equal $R_{ex}W$ for the two structures. Both mobility curves were calculated using $C_{max}$ approximation to ensure consistency. The mobility was compared at $N_{inv}=1 \times 10^{13}$ cm$^{-2}$ to eliminate the dependence of the hole mobility on the method of extraction. The decrease of 13% for the 3.5/9.5 sample clearly indicates that in this case the deleterious effect of partial strain relaxation in the thicker Ge layer and misfit dislocation scattering is the primary factor in determining hole mobility, overwhelming the beneficial effect of better hole confinement in the thicker Ge layers that was observed by Ni Chleirigh [17].

![Figure 5.3](image.png)

Figure 5.3. The effect of strained Ge layer thickness on the hole mobility was investigated for 3.5/5 and 3.5/9.5 devices. Both curves were obtained using $C_{max}(V_{GS}-V_T)$ approximation for the inversion charge and were corrected for series resistance. Increasing the strained-Ge layer thickness from 5 to 9.5 nm leads to 13% decrease in hole mobility at $N_{inv}=1 \times 10^{13}$ cm$^{-2}$.

5.5.4. Hole mobility dependence on the annealing temperature

Figure 5.4 shows the implant annealing temperature dependence of the mobility for the 3.5/5 device. The series resistance of the 600 °C-annealed sample could not be extracted and therefore the curves without series resistance correction are plotted. The devices activated at 450 °C show mobility enhancement of
3.5x compared to the hole mobility for the Si/SiO2 device at inversion charge density of $1 \times 10^{13}$ cm$^2$. The enhancement factor increases slightly to 3.6x for samples with anneal temperature of 500 °C and it decreases to 2.8x for the devices annealed at 600 °C. The mobility degradation at 600 °C cannot be solely attributed to the higher temperature since the effect of the cause for the particles and bubbles on the device performance cannot be ruled out. It is possible that higher mobility could be achieved when optimized fabrication process is accomplished.

![Graph showing hole mobility vs. inversion charge density](image)

**Figure 5.4.** Effect of the SD activation temperature on the hole mobility for 3.5/5 device without series resistance correction. The mobility enhancement over the universal curve at inversion charge $10^{13}$ cm$^2$ is 3.5x for activation temperature of 450 °C and increases to 3.6x for 500 °C. Mobility enhancement calculated for 600 °C SD activation is 2.8x.

### 5.5.5. Hole mobility dependence on the Si cap thickness

#### 5.5.5.1. Hole mobility as a function of electric field

In the preceding calculations, mobility was studied as a function of inversion charge density which in turn depends on channel doping level. To facilitate comparison with published data and to eliminate doping level dependence, mobility was calculated as a function of the vertical (transverse) electric field $E_{eff}$. 

35
\[ E_{\text{eff}} = \frac{Q_b + \eta Q_{\text{inv}}}{\varepsilon_{\text{SiGe}}} \]  \hspace{1cm} (Eq. 5.15)

where \( Q_b \) is the bulk depletion charge, \( Q_{\text{inv}} \) is the inversion charge, \( \varepsilon_{\text{SiGe}} \) is the permittivity of the substrate and \( \eta \) is a fitting parameter. The fitting parameter \( \eta \) is defined as 1/2 for electrons and 1/3 for holes. Using this expression is not strictly justified, since it assumed bulk substrate and uniform doping. For the purpose of the current work though, it gives a reasonable estimate for the expected values of the vertical effective field. The values for doping concentration and permittivity of the 40% Ge substrate were used since the depletion charge is mostly located in the relaxed SiGe layer.

The bulk charge \( Q_b \) was calculated using the expression:

\[ Q_b = N_D \cdot x_{\text{dmax}} \cdot q \]  \hspace{1cm} (Eq. 5.16)

Where \( N_D \) was the extracted average substrate doping concentration (5x10^{16} \text{ cm}^{-3} ), and \( x_{\text{dmax}} \) was found from:

\[ x_{\text{dmax}} = \sqrt{\frac{2 \varepsilon_{\text{SiGe}} \varphi_{\text{sth}}}{q N_D}} \]  \hspace{1cm} (Eq. 5.17)

### 5.5.5.2. Hole mobility dependence on the Si cap thickness

The effect of the Si-cap thickness on the mobility was investigated based on the results extracted from the 3.5/5 and 0/8.5 devices and plotted vs \( E_{\text{eff}} \) in Figure 5.5. The enhancement factor compared to universal hole mobility curve is 4.7x for the 3.5/5 device and 2.2x for the 0/8.5 device at low effective field of 0.4 MV/cm. As expected, removing the silicon cap entirely moves the channel to close proximity of the dielectric interface, making the holes subject to surface-roughness scattering and therefore decreasing the mobility.
5.5. Chapter Summary

In this chapter a number of parameters such as series resistance, doping concentration, threshold voltage and effective field were calculated. High series resistance was extracted for all of the samples resulting in up to 16.5% decrease in the mobility at $N_{inv} = 10^{13}$ cm$^{-2}$ for 3.5/5 device. It was estimated that a negative
fixed charge of $1.7 \times 10^{13}$ cm$^{-2}$ corresponded to the large shift in the threshold voltage for the Si-capped devices. The hole mobility of the ring-FETs was extracted and compared for the different devices. The dependence of the hole mobility on the Ge channel thickness, the Si cap thickness, the S/D activation temperature was also shown. The results are summarized in Chapter 6.
Chapter 6

Summary

The goal of this work was to evaluate the hole mobility of strained-Ge p-type ring-FETs with high-k/metal gate stack. This was motivated by the need for improved transport and scalability in future CMOS technologies for which high mobility channel material and high permittivity gate dielectric are required.

Mobility was studied in strained-Ge channels with and without a Si cap and the degradation of the mobility after the silicon layer removal was assessed. The hole mobility dependence on the strained-Ge layer thickness was also explored.

The results suggest that there is a critical thickness of the strained-Ge layer thickness above which the effect of strain relaxation overwhelms the beneficial effect of hole confinement in thicker Ge-layers. The samples with 9.5-nm-thick Ge layer showed 13 % degradation in mobility at \( N_{inv}=10^{13} \text{ cm}^2 \) compared to those with 5-nm-thick Ge-layer. The samples without silicon cap showed almost 40 % lower hole mobility at \( E_{eff}=0.7 \text{ MV/cm} \) than the the Si-capped devices. While removing the cap did not lead to the highest hole mobilities, the samples maintained mobility enhancement of 2.2x to 2.7x over the relaxed-Si universal hole mobility curve across most of the range of \( E_{eff} \). The capless devices also showed some superior characteristics compared to Si-capped devices such as steeper sub-threshold slope and higher \( I_{on}/I_{off} \) ratio, a promising result in favor of future scaled CMOS devices based entirely on strained-Ge channels.
Suggestions for future work

1. **Active area mask.** In this work only a three step photolithography process was used. As a result, devices lacked the proper isolation and considerable junction leakage current was observed. As an initial step toward decreasing of the leakage current an active area mask should be used as a first step of the fabrication process after epitaxial growth of the device layers.

2. **Si cap thickness.** The silicon cap seems necessary for obtaining high mobility devices. Several references in the literature reported increased mobility with decreasing the Si-cap thickness. In this work, only devices with a fixed, relatively thick, Si-cap thickness were investigated. More Si-cap thicknesses need to be examined and the effect of varying the thickness on the mobility should be studied.

4. **Increased strained-Ge thickness.** In order to further understand the dependence of the hole mobility on strained-Ge layer thickness, devices must be grown with varying thickness of the Ge layer. It was demonstrated in Section 4.3.2 that 9.5-nm-thick Ge layer shows signs of relaxation which was not evident in the 8.5-nm-thick layer. Work is required to determine if this behavior is solely due to the thickness of the Ge-layer, or to a combination of factors such as the presence of a Si-cap, the processing conditions, and the lack of proper isolation.

3. **Increased anneal temperature.** It was shown that increasing the annealing temperature from 450 °C to 500 °C led to better activation of the dopants, lower series resistance and higher mobility. The decrease of the mobility for 600 °C could be due to the defects that were observed on the wafer surface. Therefore, this mobility decrease may not be intrinsically due to the increased temperature, and it is recommended that this experiment be repeated for 600 °C and higher temperatures.
5. Other gate dielectric materials. In an attempt to further decrease EOT/CET, materials with higher permittivity, such as HfO$_2$, should be investigated as gate dielectrics and their effect on mobility enhancement should be observed.
## Appendix A

### Wafer Structures

<table>
<thead>
<tr>
<th>Structure</th>
<th>Recipe Details</th>
</tr>
</thead>
</table>
| **3.5/5** | 6568 (like 6501)  
Recipe: CAIT GE 40-6 | 36 Å Si @ 600 °C, 160 s  
5 min Si@ 525 °C  
5 min Si@ 450 °C  
65 Å Ge@365 °C, 30T, 85 sec, 0+5  
~150 Å 40% SiGe @900 °C, undoped, 12 sec  
0.75 μm 40%SiGe @ 900 °C, 1E17 Phos, 462s  
4.0 μm 2-40%SiGe @ 900 °C, 1E17 Phos  
N+ substrate |
| **3.5/9.5** | 6572 (like 6501)  
Recipe: CAIT GE 40-6 | 36 Å Si @ 600 °C, 170 s  
5 min Si@ 525 °C  
5 min Si@ 450 °C  
100 Å Ge@365 °C, 30T, 110 sec, 0+5  
~150 Å 40% SiGe @900 °C, undoped, 12 sec  
0.75 μm 40%SiGe @ 900 °C, 1E17 Phos, 462s  
4.0 μm 2-40%SiGe @ 900 °C, 1E17 Phos  
N+ Substrate |
| **0/8.5** | 6574 (identical to 6500)  
Recipe: CAIT 40-6 NO SI | ---  
100 Å Ge@365 °C, 30T, 110 sec, 0+5  
~150 Å 40% SiGe @900 °C, undoped, 12 sec  
0.75 μm 40%SiGe @ 900 °C, 1E17 Phos, 462s  
4.0 μm 2-40%SiGe @ 900 °C, 1E17 Phos  
N+ substrate |
| **Si control** | 6585 (like 4586)  
Recipe: TFET CONTROL | 250 Å Si @936 °C, 10 sec, undoped  
2μm Si, 600 sec, 936 °C, 1E17 Phos, 10% ratio, 75 sccm DOP2, 75 sccm SiH4  
N+ substrate |
# Film Thickness Summary:

The UV-1280 Recipes: “Si on Ge on SiGe”; “Ge on 40% GRB”

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Native Oxide Thk (Å)</th>
<th>Si Cap Thk (Å)</th>
<th>Ge Layer Thk (Å)</th>
<th>SiGe Thk (Å)</th>
<th>%Ge</th>
<th>Fit</th>
<th>Peak Correlation</th>
<th>Goodness of Fit</th>
</tr>
</thead>
<tbody>
<tr>
<td>6568</td>
<td>4.7</td>
<td>32.1</td>
<td>51.4</td>
<td>7500-</td>
<td>40% fixed</td>
<td>excellent</td>
<td>0.9976</td>
<td>0.9926</td>
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<tr>
<td>6572</td>
<td>0</td>
<td>37.5</td>
<td>92.1</td>
<td>7500-</td>
<td>40% fixed</td>
<td>excellent</td>
<td>0.9974</td>
<td>0.9924</td>
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<td>6574</td>
<td>--</td>
<td>--</td>
<td>84.9</td>
<td>7500-</td>
<td>40% fixed</td>
<td>excellent</td>
<td>0.9944</td>
<td>0.9894</td>
</tr>
<tr>
<td>6585</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No metrology possible. No film interfaces, only Silicon.</td>
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</tbody>
</table>


# Appendix B

## Device Fabrication Process Flow

<table>
<thead>
<tr>
<th>Gate Stack</th>
<th>ALD</th>
<th>10 cycles ozone (~16%) @N2=0.05 sccm Recipe: OZONE_CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ozone treatment</td>
<td>ALD</td>
</tr>
<tr>
<td>2</td>
<td>High-k Deposition (Al2O3)</td>
<td>ALD</td>
</tr>
<tr>
<td>3</td>
<td>Metal gate Deposition (WN)</td>
<td>ALD</td>
</tr>
<tr>
<td>4</td>
<td>HMDS</td>
<td>HMDS/TRL</td>
</tr>
<tr>
<td>5</td>
<td>Coater PR</td>
<td>Coater/TRL</td>
</tr>
<tr>
<td>6</td>
<td>Pattern Gate</td>
<td>EV1/TRL</td>
</tr>
<tr>
<td>7</td>
<td>Develop PR</td>
<td>Photo/TRL</td>
</tr>
<tr>
<td>8</td>
<td>Etch WN gate</td>
<td>Rainbow</td>
</tr>
<tr>
<td>9</td>
<td>Send wafers for SD implant</td>
<td>Innovion</td>
</tr>
<tr>
<td>10</td>
<td>IPA</td>
<td>Photo/TRL</td>
</tr>
<tr>
<td>11</td>
<td>Ashing PR</td>
<td>Asher/TRL</td>
</tr>
</tbody>
</table>

### ILD deposition and Via pattern

<table>
<thead>
<tr>
<th>ILD deposition and Via pattern</th>
<th>concept-I</th>
<th>200 nm SiO2</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>S/D activation</td>
<td>Tube A3</td>
</tr>
<tr>
<td>13</td>
<td>HMDS</td>
<td>HMDS/TRL</td>
</tr>
<tr>
<td>14</td>
<td>Coat PR</td>
<td>Coater/TRL</td>
</tr>
<tr>
<td>15</td>
<td>Pattern Via</td>
<td>EV1/TRL</td>
</tr>
<tr>
<td>16</td>
<td>Develop PR</td>
<td>Photo/TRL</td>
</tr>
<tr>
<td>17</td>
<td>BOE etch</td>
<td>acidhood 2/TRL</td>
</tr>
<tr>
<td>18</td>
<td>Ashing PR</td>
<td>Asher/TRL</td>
</tr>
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</table>

### Metal pattern and Sinter

<table>
<thead>
<tr>
<th>Metal pattern and Sinter</th>
<th>acidhood 2/TRL</th>
<th>30 sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>HF dip</td>
<td>500 Å Ti, 5000Å Al</td>
</tr>
<tr>
<td>21</td>
<td>Frontside Metalization</td>
<td>Endura</td>
</tr>
<tr>
<td>22</td>
<td>Backside Metalization</td>
<td>Endura</td>
</tr>
<tr>
<td>23</td>
<td>HMDS</td>
<td>HMDS/TRL</td>
</tr>
<tr>
<td>24</td>
<td>Coat PR</td>
<td>Coater/TRL</td>
</tr>
<tr>
<td>25</td>
<td>Pattern Metal</td>
<td>EV1/TRL</td>
</tr>
<tr>
<td></td>
<td>Process</td>
<td>Duration/Method</td>
</tr>
<tr>
<td>---</td>
<td>-----------</td>
<td>----------------------------------------</td>
</tr>
<tr>
<td>26</td>
<td>Develop PR</td>
<td>Photo/TRL, 1 min in OCG developer</td>
</tr>
<tr>
<td>27</td>
<td>Metal etch</td>
<td>Rainbow, Recipe: Ti_AL_500nm_eva_nospin Manual endpoint ~40 sec</td>
</tr>
<tr>
<td>28</td>
<td>Ashing PR</td>
<td>asher/TRL, 1 h 15 min</td>
</tr>
<tr>
<td>29</td>
<td>Sinter</td>
<td>tube A3, 430 °C, 30 min, FG</td>
</tr>
</tbody>
</table>
Bibliography


