Analysis, Modeling and Design of Energy Management and Multisource Power Systems

by

John Jacob Cooley

B.S., E.E., Massachusetts Institute of Technology (2005)
B.S., Physics, Massachusetts Institute of Technology (2005)
M.Eng, Massachusetts Institute of Technology (2007)
Electrical Engineer, Massachusetts Institute of Technology (2009)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2011

Author .....
Department of Electrical Engineering and Computer Science
May 20, 2011

Certified by .....
Steven B. Leeb
Professor, EECS & ME, MacVicar Faculty Fellow
Thesis Supervisor

Accepted by .....
Leslie A. Kolodziejski
Chair, Committee on Graduate Students

Analysis, Modeling and Design of Energy Management and Multisource Power Systems

by

John Jacob Cooley

Submitted to the Department of Electrical Engineering and Computer Science
on May 20, 2011, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy in Electrical Engineering

Abstract

Transformative impacts on our energy security rely on creative approaches for consumption and generation of electricity. Technological contributions can impact both areas if they focus on problems of scale. For example, occupancy-based electrical loads (HVAC and lighting) accounted for roughly 50% of the total consumed electricity in the U.S. in 2008. Meanwhile, roughly 50% of consumed oil in the U.S. is imported. The U.S. Department of Energy has appropriately identified "sensing and measurement" as one of the "five fundamental technologies" essential for achieving energy security. Complementing reductions in consumption with increases in deployment of fossil-fuel-independent generation (solar and wind) and energy storage (batteries, capacitors and fuel cells) will yield a two-fold impact. Lofty energy security goals can be made realizable by aggressive application of inexpensive technologies for minimizing waste and by maximizing energy availability from desirable sources.

Long-standing problems in energy consumption and generation can be addressed by adding degrees of freedom to sensing and power conversion systems using multiple electrical sources. This principal drove the invention of the hybrid electric vehicle, which achieves efficiency increases by combining the energy capacity of gasoline with the flexible storage capability of batteries. Similarly, fresh strategies for electrical circuit design, control, and estimation in systems with multiple electrical sources can minimize consumption, extend the useful life of storage, and improve the efficiency of generation.

A solar array constitutes a grid or network of panels or cells that may best be modeled and treated as independent sources needing careful control to maximize overall power generation. A fuel cell stack, an array of sources in its own right, is best used in a hybrid arrangement with batteries or capacitors to mitigate the impact of electrical transients. Meanwhile, room lighting constitutes a network of multiple electrostatic field sources that can be particularly useful for occupancy detection.

Exploiting performance benefits of multi-source electrical networks requires an increased flexibility in the analysis required to make informed design choices. This thesis addresses the added complexity with linear analytical and modeling approaches

that reveal the salient features of complicated multisource systems. Examples and prototypes are presented in capacitive sensing occupancy detectors, hybrid power systems and multi-panel solar arrays.

Thesis Supervisor: Steven B. Leeb
Title: Professor, EECS & ME, MacVicar Faculty Fellow

Acknowledgments

I thank my fiance, Clarissa, for her patience, love and support. I have relied on her countless times and I am elated to share the rest of my life with her.

I thank my advisor, Steve. I have been constantly amazed by his innate ability to guide me toward both exciting technical contributions and critical life lessons. I am certain that I will never adequately express my gratitude toward him.

I thank my committee, Prof. Perreault and Prof. Shaw. Their guidance, insight and encouragement over the years has been precious on many levels.

I would like to thank my colleagues who contributed to my personal and technical development and also, in some cases, directly to this thesis: Al Avestruz, Rob Cox, Chris Laughman, Jim Paris, Warit Wichakool, Uzoma Orji, Chris Schantz, Riccardo Signorelli, Robert Pilawa, Brandon Pierquet, Dan Vickery, Sabrina Neuman, Zach Clifford, Zack Remscrim, Alex Crumlin, BJ Thompson, and Shahriar Khushrushahi. I would like to thank the faculty members from whom I have received valuable insight and support over the years: Prof. Dawson, Prof. Roberge, Prof. Ram, Prof. Braida, and Prof. Lee.

I would also like to thank my friends and family, my mom, my brother, and my sister. Finally, this thesis is dedicated to the memory of my dad.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Multisource electrical networks pervade systems that consume and generate electrical power. Understanding, modeling, and designing multisource networks is increasingly a key step in implementing technological solutions for energy management, conservation and generation. A lighting array, for example, constitutes a network of multiple electrostatic field sources particularly useful for occupancy detection. A solar array constitutes a grid or network of panels serving as sources, and a fuel cell stack is typically used in a hybrid arrangement with other electrical storage devices like batteries or capacitors to control the impact of electrical transients. The benefits of multisource electrical networks come with increased complexity in the analysis required to make informed design choices.

This thesis addresses the added complexity with linear analytical and modeling approaches that reveal the salient features of complicated multisource systems. Examples from capacitive sensing occupancy detectors, hybrid power systems and multipanel solar arrays demonstrate the utility of the analytical approaches.

1.1 Thesis Overview

The advantages of multisource networks are explored first in the context of capacitive sensing occupancy detectors. Multiple signal sources can be configured to yield a natural carrier suppression enabling surprising resolution of fine perturbations in

the lumped capacitive network comprising the occupancy detection field. The carrier suppression is exploited with a fully-differential measurement technique which necessitated analytical modeling not previously found in the literature. The resulting circuit and mathematical model of the fully-differential amplifier is employed to validate our understanding of the operating principles in a first capacitive sensor that uses multiple sources of stray electric fields from fluorescent lamps to detect occupants. Extensions of this application are demonstrated for solid-state lighting and for a capacitive sensor based on multiple artificially generated electric field sources.

In a second example, multisource networks are explored in the context of fuel cell power processing. The need to maintain a fuel cell output current at a fixed and safe operating point to contend with the well-known inherent reliability issues therein is addressed by deploying a multisource multi-converter system. The multisource system fundamentally provides the needed degrees of freedom to support both safe fuel cell operation and the practical variability in the load. As an added benefit, that system is designed to achieve integral diagnostics of the fuel cell based on impedance spectroscopy using a control approach that could only be developed with a firm understanding of the linearized behavioral aspects of that power converter system. The analyses and examination of the behavior and design of multi-converter systems presented in this thesis has far-reaching implications in the area of control paradigms for paralleled converter systems, hybrid power systems, and distributed source power systems.

A distinct example of multisource power conversion addressed in this thesis focuses on distributed solar power processing. With the growing need for per panel maximum power point tracking of solar arrays to contend with varying light levels, panel ages, etc. across a physically widespread array there are interesting challenges defined by simultaneous constraints in cost, performance and longevity. The development of a linearized circuit model for such a system has revealed a solar power harvesting approach exhibiting a combination of benefits regarding all of the fundamental constraints.

The common analytical style in this thesis blends linear superposition and decom-

position techniques to establish linearized circuit models and design-oriented mathematical results. The analysis prioritizes intermediate circuit models often useful in their own right, but that also serve as abstractions useful in completing the analysis of the full system. Similarities are evident in the design-oriented analytical process discussed by Middlebrook in [31].

1.2 Thesis Contributions

The principle contributions of this thesis are summarized here.

1.2.1 Capacitive Sensing Occupancy Detectors

An approach based on carrier suppression techniques in amplitude-modulated sensing systems is presented in the context of capacitive sensing occupancy detectors. The carrier suppression techniques largely rely on balanced systems derived from multisource excitation networks. A differential measurement technique is employed to sense small imbalances in the resulting capacitive bridge-like networks. An analytical model of the fully-differential closed-loop op-amp circuit and a detailed analytical approach is presented. The analytical model captures the distinct common-mode and differential-mode current paths through the fully-differential transimpedance amplifier. The circuit model of the transimpedance amplifier, useful in its own right, is used to continue the analysis for fully-differential voltage amplifiers leading to mathematical results that hold for arbitrary external impedance values - a characteristic that is superior to the mathematical results from classical analyses of the same circuit. Lumped element models for capacitive sensors are developed and validated. System design and modeling considerations are presented for example capacitive sensing occupancy sensors based on the circuit model of the fully-differential amplifier. A signal processing approach and circuit is presented with frequency-domain and noise analysis. The performance of several implemented capacitive sensor systems is presented.

1.2.2 Multi-converter Systems

An analytical and modeling framework is presented that addresses three key areas in the implementation of practical multisource, multi-converter power systems: open-loop transfer function analysis, closed-loop transfer function analysis, and the effect of multiple input filters on both. The analysis is applied to two design examples constituting two different feedback control techniques in the context of fuel cell power processing. Design considerations enabling integral diagnostics based on impedance spectroscopy using small-signal power converter control techniques are presented in the context of the example systems. The performance of two implemented systems and fuel cell impedance results indicative of run-time integral diagnostics are presented. The health of an electrically-simulated fuel cell stack is determined based on run-time impedance measurements showing distinct differences between healthy and damaged states.

1.2.3 Per-panel Photovoltaic Power Processing

A linearized circuit model of an N-converter-N-panel solar power array is developed leading to a maximum power point tracking approach enabling the use of circuit topologies with benefits in efficiency, cost, and complexity. The maximum power point tracking approach overcomes the limitations of multilevel output switched-capacitor converters and obviates the need for interpanel communication. The underlying motivation is to deploy switched-capacitor converters because they achieve power conversion without magnetic energy storage – a key cost element in inductor-based power converters. A statistical performance evaluation method is presented revealing the predicted average performance of the proposed system. Competitive tracking efficiencies are supported by the statistical performance predictions despite a relatively small number of discrete conversion ratios accessible to each of the panel converters. A switched-capacitor experimental prototype is presented to demonstrate power processing and design concepts. Predicted and measured conversion efficiencies agree well and indicate good performance.

1.3 Thesis Organization

Chapter 2 presents a detailed analysis of the first multisource electrical network considered in this thesis. The analysis develops circuit models and mathematical expressions to describe the behavior of fully-differential closed-loop op-amp circuits. The results of that analysis are used in the design and configuation of the multisource capacitive sensing occupancy detectors detailed in Chapters 3 - 5.

Chapters 6 - 9 present work on multiconverter power systems with examples for fuel cell power processing. Chapter 6 investigates a linearized model of the multiconverter system and the analysis of its behavior in the context of feedback control. Chapter 7 addresses the effect of multiple input filters in multisource, multiconverter systems using an application of the two extra element theorem (2EET). Chapter 8 presents a design example using dual voltage regulated power converters for impedance spectroscopy in a grid-tied fuel cell application. Chapter 9 presents a design example using a master-slave control technique for impedance spectroscopy in a fuel cell application intended for unmanned aerial vehicles (UAV's).

Chapter 10 describes a method for deploying magneticless per panel solar power converters.

Chapter 2

Analysis and Modeling of Fully-differential Closed-loop Op-amp Circuits

2.1 Introduction

Fully-differential (FD) amplifiers afford notable benefits in dynamic range and rejection of unwanted signals. The dynamic range benefit is significant when contending with low supply voltages in fully-integrated and system on-chip design [32–38], general purpose and audio frequency instrumentation [35, 39–41], and in discrete op-amp applications particularly for accommodating differential-mode (DM) input ADC's [40–44]. Integrated switched-capacitor amplifiers have exploited this benefit as well [45–48]. Power supply disturbances and common-mode (CM) pickup are typical unwanted signals that are better rejected by FD electronics when compared to their single-ended (SE) counterparts [39, 45, 49–52]. Both voltage-mode and current-mode (transimpedance) FD amplifiers are useful as front-end amplifiers for suppressing unwanted carrier content in balanced or "bridge-like" systems [1, 53–55]. Additionally, DM signal processing rejects the effects of even-order nonlinearities [42, 51]. Both balanced and intentionally asymmetric FD amplifiers play important roles [41, 44].

The benefits of FD signal processing come at the expense of added complexity in analysis. Powerful simplifications are possible upon assuming perfect or almost perfect symmetry, e.g. equality between homologous elements, Z_{f1} and Z_{f2}, in Figure 2-1. References [51, 56–58] exploit those simplifications to develop half-circuit decomposition methods. In reference [41] the author analyzes FD amplifiers directly, but relies on perfect symmetry assumptions late in the analysis to arrive at expressions in terms of DM or CM input signals.

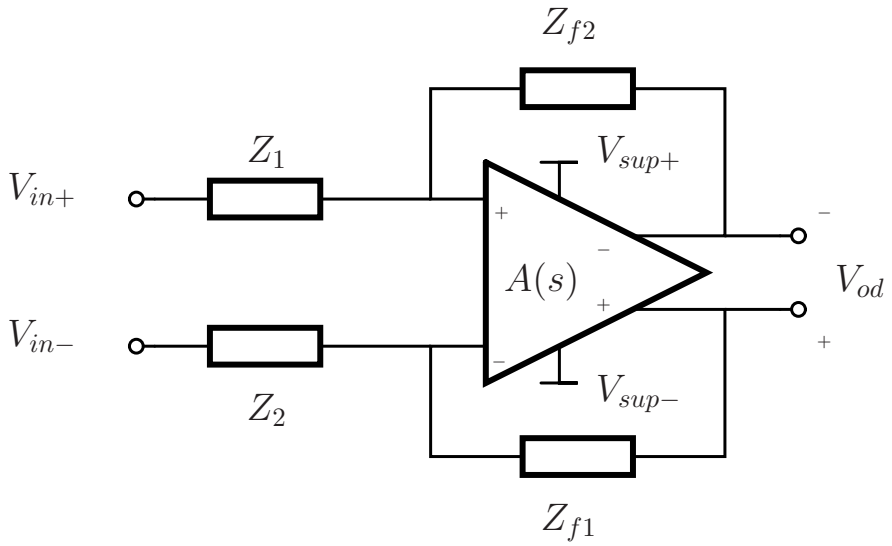


Figure 2-1: A FD closed-loop op-amp circuit

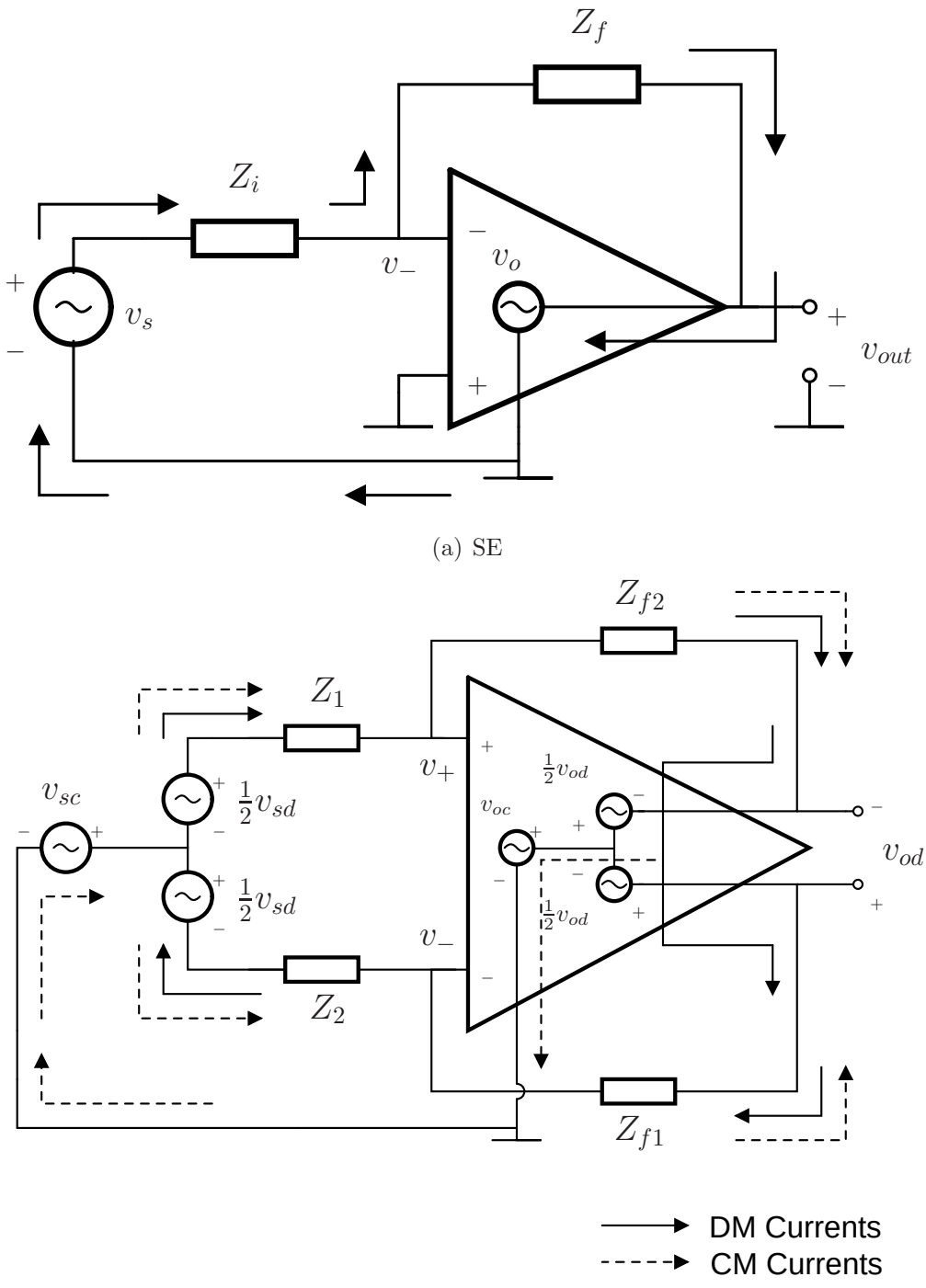
This work takes an alternative approach to the analysis of FD amplifiers. The analysis is separated into two steps corresponding to the inner transimpedance amplifier and the outer voltage-mode amplifier. Linear superposition of CM and DM signals assures the results are written directly in terms of those quantities. Separation of the analysis and the use of linear superposition leads to concise or "low-entropy" mathematical expressions [31]. An added benefit of the approach is that the usual symmetry assumptions are not needed and so the results hold for arbitrary element values.

The development of the FD transimpedance amplifier circuit model in Section 2.2 is perhaps the core contribution of this work. The versatility of that circuit model is demonstrated in three key contexts. First, the transimpedance amplifier model

is used to derive the performance of a voltage amplifier with arbitrary impedance elements, Z_1 and Z_2 in Figure 2-1. The results hold for arbitrary impedance values and agree well with the simulated behavior of a commercial FD op-amp. Second, the extension of that analysis to include finite op-amp input impedance, using the same transimpedance amplifier circuit model is described. Finally, the transimpedance amplifier model is used to predict the behavior of a capacitive bridge sensor system. In the capacitive bridge sensor system, the external impedance elements Z_1 and Z_2 are further generalized to an arbitrary impedance network. Finite op-amp input impedance is captured by including shunt impedances at the transimpedance amplifier circuit model inputs. In the capacitive bridge sensor system, the front-end amplifier is loaded by the subsequent synchronous demodulation circuitry. Model validation comparing experimental data to data simulated using the transimpedance amplifier circuit model shows excellent agreement.

2.1.1 Current Paths in FD Amplifiers

The ensuing analysis will be better appreciated having an understanding of the CM and DM current paths through a FD amplifier. The current paths in the FD amplifier (Figure 2-2(b)), are in some sense a generalization of those in the SE amplifier (Figure 2-2(a)); current return paths are supported by the output structure of the op-amp itself, but in the FD amplifier purely DM and purely CM currents take two distinct paths. The circuit models developed through the analysis in Sections 2.2 and 2.3 will mirror the current paths shown in Figure 2-2(b). Note that the incremental grounds in Figure 2-2 are physically supported by the op-amp power supply connections.



(a) SE

(b) FD

Figure 2-2: Small-signal current paths in closed-loop op-amp amplifiers.

2.1.2 Definitions

Definitions of CM and DM signal decompositions vary among the literature. We define them in this work as follows. Differential-mode (DM) voltage is defined as the difference between two voltages,

$$v_{dm} \equiv v_+ - v_-, \tag{2.1}$$

and common-mode (CM) voltage is defined as the geometric mean of the two,

$$v_{cm} \equiv \frac{v_+ + v_-}{2}. \tag{2.2}$$

Differential-mode current is defined as half the difference between two currents,

$$i_{dm} \equiv \frac{i_+ - i_-}{2}, \tag{2.3}$$

while common-mode (CM) current is defined as the sum of the two,

$$i_{cm} \equiv i_+ + i_-. \tag{2.4}$$

2.1.3 Scope

The analysis in Sections 2.2 and 2.3 focuses on the DM output voltage while the CM output voltage is assumed to be held fixed by the CM feedback circuit included in all commercial FD op-amps. The scope of this chapter is intended to address op-amp circuits that process signals having frequency content well below the op-amp cross-over frequency, e.g. 1 kHz in the simulations of the LTC6404. These cases are ubiquitous as they correspond to good design practices guaranteeing that the op-amp will exhibit large DM-DM gain, a_d, and relatively small CM-DM gain, a_c. Loading effects on the closed-loop op-amp circuit are negligible under these conditions because the feedback control significantly reduces the effect of finite op-amp (open-loop) output impedance. The assumptions described above will be validated in both

simulation and in a practical setting in Section 2.4.

2.1.4 Dynamics

The results in this chapter are derived in terms of op-amp gain parameters, a_d and a_c, and generalized external impedance elements. The behavior of an arbitrary system having dynamic effects may be described by inserting the frequency dependencies of those parameters into the mathematical results or circuit models.

2.1.5 Model Validation

Comparison of the mathematical results with simulated and experimental data validates the assumptions taken in the analysis, the practical relevance of this work and the correctness of the mathematical manipulations.

Simulated model validation was carried out by comparing numerical results from the mathematical results to SPICE simulations of ideal circuit models and of a commercial FD op-amp, the LTC6404. The model validations plot the quantities of interest against percentage mismatch between homologous elements, e.g. ΔZ is the mismatch between Z_1 and Z_2 in Figure 2-1. A 0% mismatch corresponds to perfect symmetry while a 200% mismatch means that one element is zero-valued while the other is twice the average value.

Experimental model validation was carried out by comparing simulated data to experimental data in a practical setting involving macroscopic capacitive occupancy sensing and a synchronous detection signal processing system.

2.2 Analysis Step One: Transimpedance Amplifier

In this section, we analyze a FD transimpedance amplifier using the small-signal model shown in Figure 2-3. According to the CM and DM signal definitions from Section 2.1, in the small-signal model, the DM input voltage is

$$v_{id} = v_+ - v_-, \tag{2.5}$$

and the CM input voltage is

$$v_{ic} = \frac{1}{2}(v_+ + v_-), \tag{2.6}$$

while the DM output voltage is

$$v_{od} = v_{o+} - v_{o-}. \tag{2.7}$$

Similarly, the DM input current is

$$i_{id} = \frac{1}{2}(i_+ - i_-), \tag{2.8}$$

while the CM input current is

$$i_{ic} = i_+ + i_-. \tag{2.9}$$

Finally, the amplifier has the effect according to its DM-DM voltage gain, a_d, and its CM-DM voltage gain, a_c:

$$v_{od} = a_d v_{id} + a_c v_{ic}. \tag{2.10}$$

The output terminal voltages are symmetrical about the incremental CM output voltage, a CM voltage that is assumed fixed for the analyses in this chapter, i.e.

$$v_{o+} = -v_{o-}. \tag{2.11}$$

Normally, a_d, the DM-DM op-amp gain, is large by design while a_c, the CM-DM op-amp gain, is relatively small, also by design. The small-signal CM output voltage is an incremental ground having assumed a purely DC CM output voltage.

2.2.1 Transimpedance Amplifier Output Behavior

A CM-DM superposition approach for determining the transimpedance amplifier's DM output voltage is summarized by the equation:

$$v_{od} = i_{id}\left(\frac{v_{od}}{i_{id}}\right)_{i_{ic}=0} + i_{ic}\left(\frac{v_{od}}{i_{ic}}\right)_{i_{id}=0}, \tag{2.12}$$

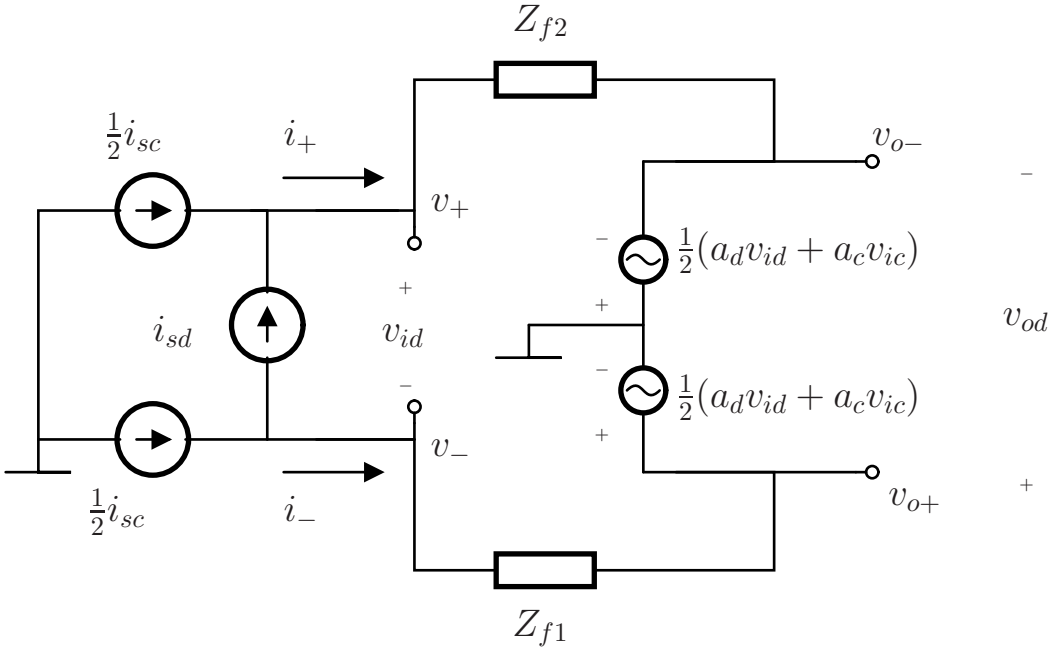


Figure 2-3: A FD transimpedance amplifier small-signal model.

in which the terms in parentheses are the transimpedance and cross-transimpedance. To find $(v_{od}/i_{id})_{i_{ic}=0}$, the CM input current sources are deactivated. Note that in this case,

$$i_{id} = i_{sd} = i_+ = -i_-. \tag{2.13}$$

From Figure 2-3, the resulting input terminal voltages are

$$v_+ = v_{o-} + i_{id} Z_{f2} \tag{2.14}$$

and

$$v_- = v_{o+} - i_{id} Z_{f1}, \tag{2.15}$$

so that, from (2.5) and (2.6), the CM and DM input voltages become

$$v_{ic} = \frac{1}{2}(v_+ + v_-) = \frac{i_{id}}{2}(Z_{f2} - Z_{f1}) \tag{2.16}$$

and

$$v_{id} = v_+ - v_- = -v_{od} + i_{id} Z_{f2} + i_{id} Z_{f1}, \tag{2.17}$$

respectively. Substituting the CM and DM input voltages into the output voltage from (2.10) yields

$$v_{od} = a_d(i_{id}(Z_{f1} + Z_{f2}) - v_{od}) + a_c\frac{i_{id}}{2}(Z_{f2} - Z_{f1}), \tag{2.18}$$

so that,

$$\left(\frac{v_{od}}{i_{id}}\right)_{i_{ic}=0} = 2\frac{a_d}{1+a_d}\overline{Z_f} - \frac{a_c}{2(1+a_d)}\Delta Z_f, \tag{2.19}$$

where the following terms are defined:

$$\overline{Z_f} \equiv \frac{(Z_{f1} + Z_{f2})}{2} \tag{2.20}$$

and

$$\Delta Z_f \equiv Z_{f1} - Z_{f2}. \tag{2.21}$$

To calculate $(v_{od}/i_{ic})_{i_{id}=0}$, the DM input current source is deactivated. A similar analysis yields

$$\left(\frac{v_{od}}{i_{ic}}\right)_{i_{id}=0} = \frac{1}{2}\frac{(-a_d\Delta Z_f + a_c\overline{Z_f})}{(1+a_d)}. \tag{2.22}$$

Superposing the two responses in (2.19) and (2.22) yields the complete expression for the DM output voltage in response to generalized input currents:

$$\boxed{v_{od} = i_{id}\left(\frac{2\overline{Z_f}a_d - \frac{1}{2}a_c\Delta Z_f}{(1+a_d)}\right) + i_{ic}\left(\frac{a_c\overline{Z_f} - a_d\Delta Z_f}{2(1+a_d)}\right)}. \tag{2.23}$$

2.2.2 Transimpedance Amplifier Input Behavior

Having derived the DM *output* voltage, a similar analysis leads to the DM and CM *input* voltages. These results will be grouped according to the superposition expressions below. The DM input voltage will be grouped as follows:

$$v_{id} = i_{id}\left(\frac{v_{id}}{i_{id}}\right)_{i_{ic}=0} + i_{ic}\left(\frac{v_{id}}{i_{ic}}\right)_{i_{id}=0} \tag{2.24}$$

and the CM input voltage will be grouped as follows:

$$v_{ic} = i_{id}\left(\frac{v_{ic}}{i_{id}}\right)_{i_{ic}=0} + i_{ic}\left(\frac{v_{ic}}{i_{ic}}\right)_{i_{id}=0}. \tag{2.25}$$

Analyzing the small-signal model in Figure 2-3, leads to

$$\boxed{v_{ic} = -i_{id}\frac{\Delta Z_f}{2} + i_{ic}\frac{\overline{Z_f}}{2}} \tag{2.26}$$

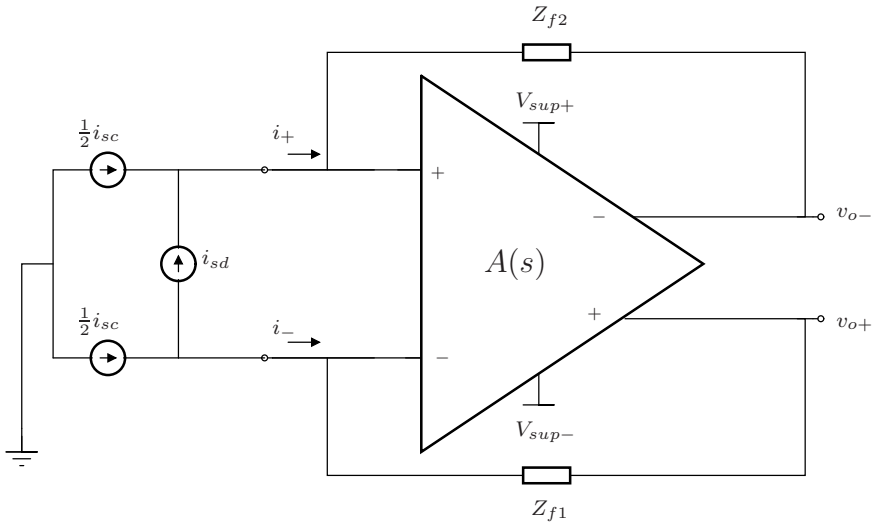
and

$$\boxed{v_{id} = i_{id}\left(\frac{2\overline{Z_f} + \frac{1}{2}\Delta Z_f a_c}{(1+a_d)}\right) - i_{ic}\left(\frac{\Delta Z_f + \overline{Z_f} a_c}{2(1+a_d)}\right)}. \tag{2.27}$$

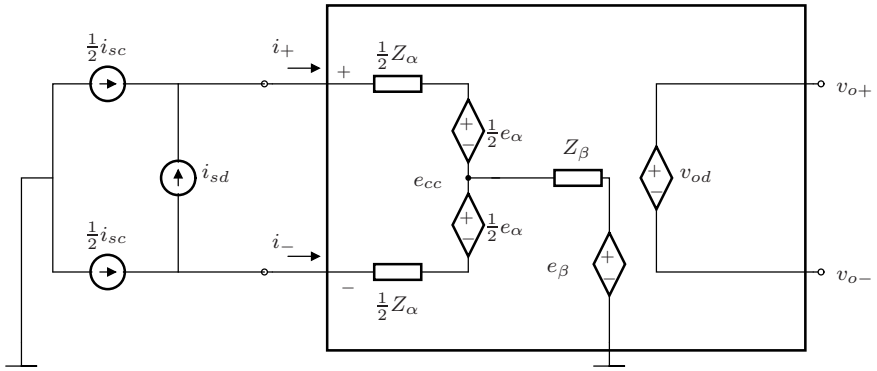
Comparing these results to (2.24) and (2.25) reveals the distinct terms resulting from the superposition of the CM and DM input sources. An interesting pattern arises in the results above. Terms with one of a_c or ΔZ_f influence *cross-coupling* from CM to DM signals. On the other hand, terms with a product of a_c and ΔZ_f appear as non-ideal terms in the relation between two DM signals. This pattern is intuitive and ubiquitous in this chapter.

2.2.3 Circuit Models of the Transimpedance Amplifier

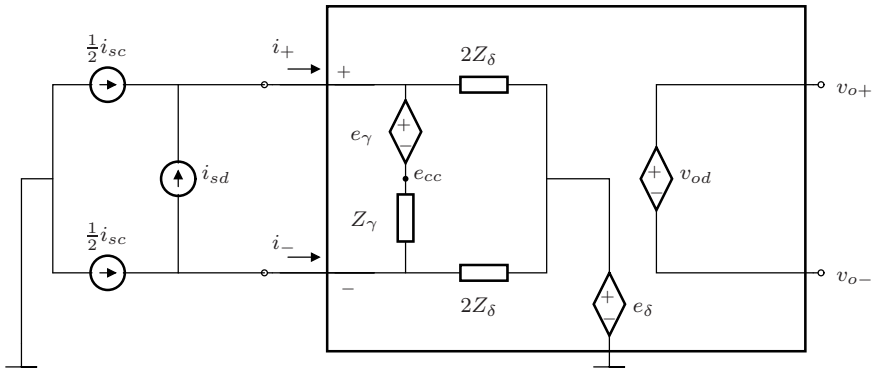
For the second step of the analysis, it will be useful to form circuit models of the transimpedance amplifier. Figures 2-4(b) and 2-4(c) show 'T' and 'Π' topologies that are helpful for representing the CM and DM input voltages in (2.26) and (2.27). Both models include a dependent voltage source at the output, which captures the function of the transimpedance and the cross-transimpedance from equation (2.23). The two models differ in their input structures. The T-network and the Π-network are each intended to approximate the behavior of the CM and DM input voltages in equations (2.26) and (2.27).



(a) A FD Transimpedance Amplifier



(b) A Small-signal T-model



(c) A Small-signal Π-model

Figure 2-4: A FD transimpedance amplifier and two approximate small-signal models. The T-model and the Π-model differ in the structure of their input network. Each contain an internal node labeled e_{cc}.

To simplify the following discussion, it is convenient to rename the terms in equations (2.26) and (2.27) as follows. The impedance elements in the CM current path will be assigned values according to,

$$Z_c \equiv \left(\frac{v_{ic}}{i_{ic}}\right)_{i_{id}=0} = \left(\frac{\overline{Z_f}}{2}\right) \tag{2.28}$$

while the impedance elements appearing in the DM current path will be assigned values according to,

$$Z_d \equiv \left(\frac{v_{id}}{i_{id}}\right)_{i_{ic}=0} = \left(\frac{2\overline{Z_f} + \frac{1}{2}\Delta Z_f a_c}{(1+a_d)}\right). \tag{2.29}$$

The dependent voltage source in the CM current path will be assigned a value according to,

$$e_c(i_{id}) \equiv i_{id}\left(\frac{v_{ic}}{i_{id}}\right)_{i_{ic}=0} = -i_{id}\left(\frac{\Delta Z_f}{2}\right) \tag{2.30}$$

while the dependent voltage sources in the DM current path will be assigned values according to,

$$e_d(i_{ic}) \equiv i_{ic}\left(\frac{v_{id}}{i_{ic}}\right)_{i_{id}=0} = -i_{ic}\left(\frac{\Delta Z_f + \overline{Z_f} a_c}{2(1+a_d)}\right). \tag{2.31}$$

The terms Z_c and Z_d are the diagonal-terms from equations (2.26)-(2.27) and they are the CM and DM input impedances of the transimpedance amplifier. The terms $e_c(i_{id})$ and $e_d(i_{ic})$ represent dependent voltage sources that capture the effects of the "cross-terms" in equations (2.26) and (2.27).

Using the definitions in (2.28)-(2.31), the following model parameters achieve an exact match between the terminal behaviors of the circuits in Figures 2-4(b) and 2-4(c) and the input voltages represented by (2.26) and (2.27). For the T-model, the impedance elements are

$$Z_\alpha = Z_d \tag{2.32}$$

$$Z_\beta = Z_c \tag{2.33}$$

and the dependent sources are

$$e_\alpha = e_d(i_{ic}) \tag{2.34}$$

$$e_\beta = e_c(i_{id}) - \frac{i_{ic}Z_d}{4}. \tag{2.35}$$

For the Π-model, the impedance elements are

$$Z_\gamma = Z_d \frac{Z_d}{Z_d||4Z_c} \tag{2.36}$$

$$Z_\delta = Z_c, \tag{2.37}$$

and the dependent sources are

$$e_\gamma = e_d(i_{ic}) \frac{Z_d}{Z_d||4Z_c} \tag{2.38}$$

$$e_\delta = e_c(i_{id}). \tag{2.39}$$

The model parameters in (2.32)-(2.39) can be simplified under practical approximations to make the circuit models more intuitive. For sufficiently small Z_d, the additive term, $(i_{ic}Z_d/4)$, will approach zero and the multiplicative term, $(Z_d/Z_d||4Z_c)$, will approach unity. From (2.28)-(2.31), Z_d is guaranteed to be small if both a_d and the ratio a_d/a_c are large. Under these assumptions, the model parameters in (2.32)-(2.39) reduce to the following. For the T-model, the impedance elements are

$$Z_\alpha = Z_d \tag{2.40}$$

$$Z_\beta = Z_c \tag{2.41}$$

and the dependent sources are

$$e_\alpha = e_d(i_{ic}) \tag{2.42}$$

$$e_\beta = e_c(i_{id}). \tag{2.43}$$

For the Π-model, the impedance elements are

$$Z_\gamma = Z_d \tag{2.44}$$

$$Z_\delta = Z_c, \tag{2.45}$$

and the dependent sources are

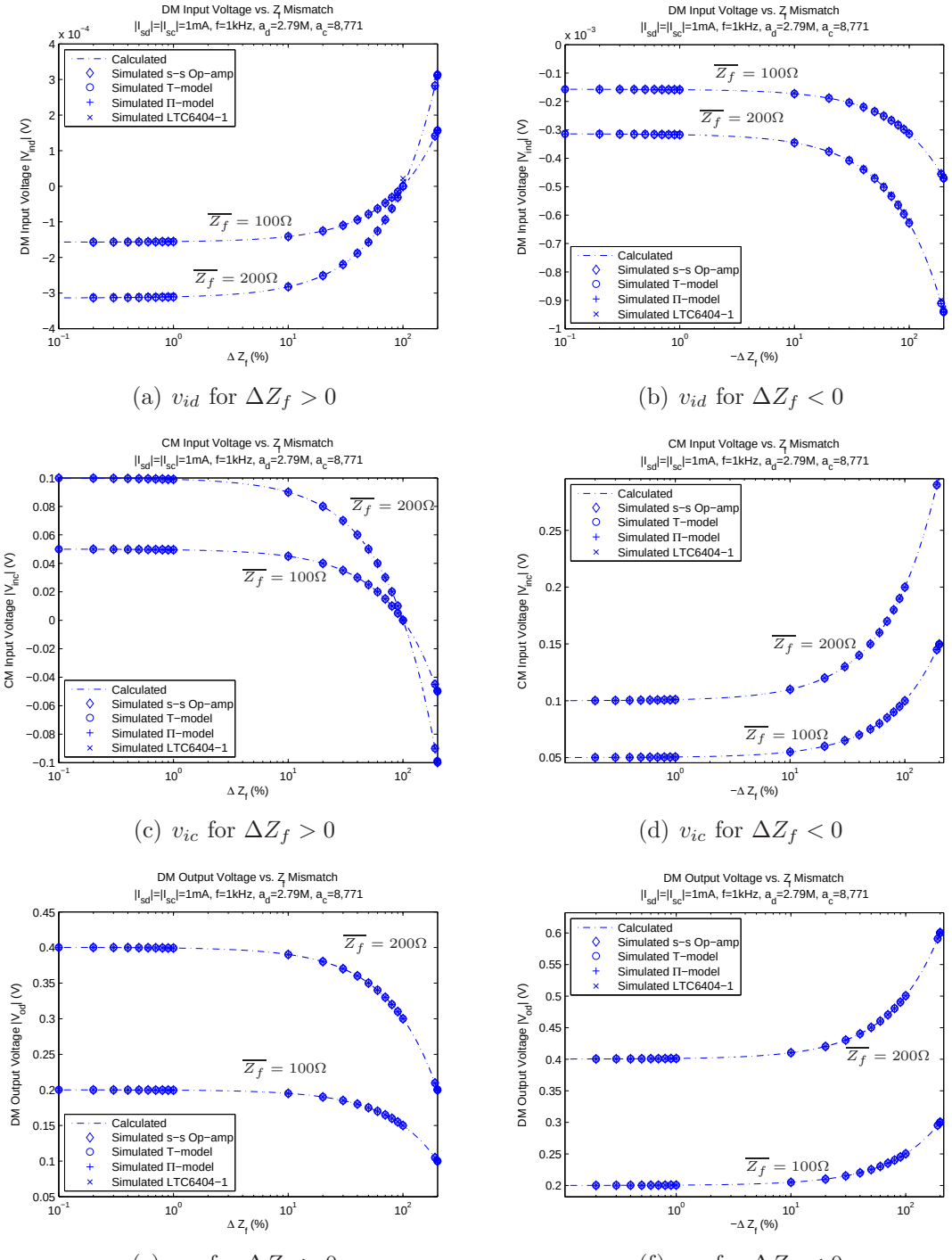
$$e_\gamma = e_d(i_{ic}) \tag{2.46}$$

$$e_\delta = e_c(i_{id}). \tag{2.47}$$

For simplicity, the rest of this analysis assumes that the gain criteria above have been met, and proceeds with the approximate model parameters in (2.40)-(2.47).

2.2.4 Transimpedance Amplifier Model Validation

Figure 2-5 shows model validation plots for the transimpedance amplifier. In the model validations, the amplifier was driven with a 1 kHz sinusoidal current source with equal CM and DM components each having an amplitude of 1 mA. The calculated results for v_{id}, v_{ic}, and v_{od} were overlayed on the simulated results for the T and Π circuit models, a small-signal ("s-s") op-amp model, and a simulated commercial op-amp. The left column in Figure 2-5 shows results for positive-valued mismatches, ΔZ_f. The right column shows results for negative-valued mismatches. The results in Figure 2-5 show good agreement among the calculated and simulated results.



(a) v_{id} for $\Delta Z_f > 0$

(b) v_{id} for $\Delta Z_f < 0$

(c) v_{ic} for $\Delta Z_f > 0$

(d) v_{ic} for $\Delta Z_f < 0$

(e) v_{od} for $\Delta Z_f > 0$

(f) v_{od} for $\Delta Z_f < 0$

Figure 2-5: Validating the transimpedance amplifier model.

2.2.5 The Virtual Short-Circuit Approximation

From (2.29), the impedance of the DM virtual short-circuit is predominantly $2\overline{Z_f}/(1+a_d)$. The DM gain, a_d, is large by design, so this impedance is small and hence the virtual short circuit approximation. On the other hand, the CM input impedance in (2.28) is half the average feedback impedance – approximately equal to $Z_{f1}||Z_{f2}$ for small mismatch values. These results become intuitive when following the respective current paths (Figure 2-2(b)) through the amplifier.

The circuit model intuition, and in particular, the virtual short-circuit approximation will be useful in the chapters that follow. System configurations, modeling and design of the capacitive occupancy sensor systems in Chapters 3-5 will rely heavily on the analytical model of the FD transimpedance amplifier developed here and on these intuitive approximations.

2.3 Analysis Step Two: Voltage Amplifier

In Figure 2-6, input elements Z_1 and Z_2 are added onto the Π-model of the transimpedance amplifier circuit model to form a voltage amplifier model. The goal of this section is to find the DM output voltage, v_{od}, that results from the CM and DM input voltages, v_{sc} and v_{sd}. The transimpedances derived in Section 2.2 reveal the relationships between the input currents, i_{ic} and i_{id}, and the DM output voltage, v_{od}, from (2.23). The voltage amplifier analysis reduces to finding the relationships between the input voltage sources, v_{sc} and v_{sd}, and the input currents, i_{ic} and i_{id}. This analysis results in four transconductances. Detailed algebraic manipulations for these derivations can be found in Appendix A.7.

A superposition approach to find the overall DM output voltage yields the following expression:

$$v_{od} = i_{id}\left(\frac{v_{od}}{i_{id}}\right)_{i_{ic}=0} + i_{ic}\left(\frac{v_{od}}{i_{ic}}\right)_{i_{id}=0}, \tag{2.48}$$

where the terms in parentheses are the two transimpedances from Section 2.2. The currents, i_{id} and i_{ic} in (2.48), may be found using linear superposition of the DM and

CM input voltage sources as follows

$$v_{od} = \underbrace{\left(v_{sd} \left(\frac{i_{id}}{v_{sd}} \right)_{v_{sc}=0} + v_{sc} \left(\frac{i_{id}}{v_{sc}} \right)_{v_{sd}=0} \right)}_{i_{id}} \underbrace{\left(\frac{v_{od}}{i_{id}} \right)_{i_{ic}=0}}_{\text{transimpedance}} + \underbrace{\left(v_{sd} \left(\frac{i_{ic}}{v_{sd}} \right)_{v_{sc}=0} + v_{sc} \left(\frac{i_{ic}}{v_{sc}} \right)_{v_{sd}=0} \right)}_{i_{ic}} \underbrace{\left(\frac{v_{od}}{i_{ic}} \right)_{i_{id}=0}}_{\text{cross-transimpedance}}, \tag{2.49}$$

where the added terms in parentheses are the four transconductances. The *two* transimpedances and *four* transconductances can be renamed for brevity as follows. The transimpedance from DM input current to DM output voltage is

$$Z_{dd} \equiv \left(\frac{v_{od}}{i_{id}} \right)_{i_{ic}=0}, \tag{2.50}$$

and the transimpedance from CM input current to DM output voltage is

$$Z_{cd} \equiv \left(\frac{v_{od}}{i_{ic}} \right)_{i_{id}=0}. \tag{2.51}$$

The transconductance from DM input voltage to DM input current is

$$Y_{dd} \equiv \left(\frac{i_{id}}{v_{sd}} \right)_{v_{sc}=0}, \tag{2.52}$$

and the transconductance from CM input voltage to DM input current is

$$Y_{cd} \equiv \left(\frac{i_{id}}{v_{sc}} \right)_{v_{sd}=0}. \tag{2.53}$$

The transconductance from DM input voltage to CM input current is

$$Y_{dc} \equiv \left(\frac{i_{ic}}{v_{sd}} \right)_{v_{sc=0}}, \tag{2.54}$$

and the transconductance from CM input voltage to CM input current is

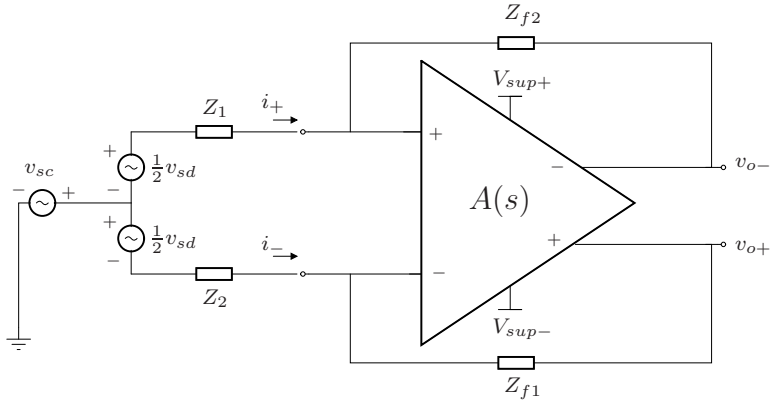
$$Y_{cc} \equiv \left(\frac{i_{ic}}{v_{sc}} \right)_{v_{sd}=0}. \tag{2.55}$$

With the definitions above, the expression in (2.49) can be re-written

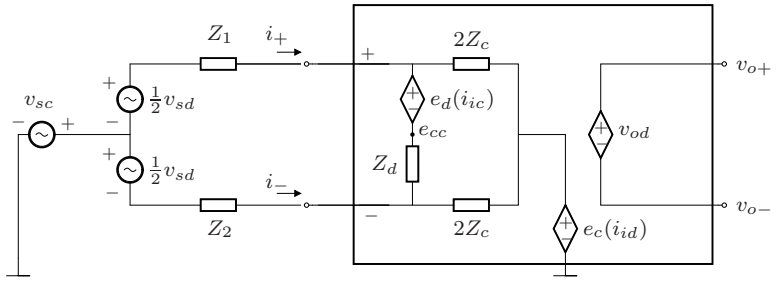
$$v_{od} = (v_{sd}Y_{dd} + v_{sc}Y_{cd})Z_{dd} + (v_{sd}Y_{dc} + v_{sc}Y_{cc})Z_{cd} \tag{2.56}$$

and then regrouped with the source terms:

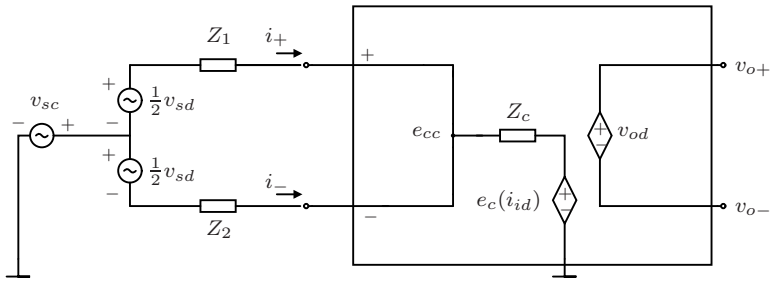
$$v_{od} = v_{sd}(Y_{dd}Z_{dd} + Y_{dc}Z_{cd}) + v_{sc}(Y_{cd}Z_{dd} + Y_{cc}Z_{cd}). \tag{2.57}$$



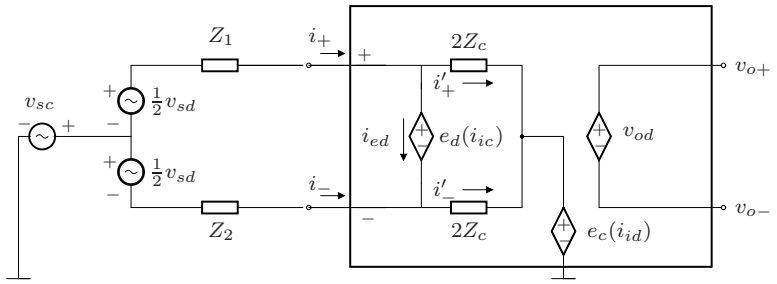
(a) A FD voltage-mode amplifier



(b) A voltage-mode amplifier model built from the Π-model of the transimpedance amplifier



(c) A voltage-mode amplifier model using the "virtual short-circuit approximation"



(d) The model used for deriving the correction in Section 2.3.1

Figure 2-6: Adding the input elements onto the transimpedance amplifier model yields a voltage-mode amplifier model.

The analysis may be simplified using the virtual short-circuit approximation quantified in Section 2.2.5. Analysis of the resulting circuit in Figure 2-6(c) may be divided into four distinct pieces for the four unknown transconductances needed in the expression for v_{od} (2.57). Shorting the DM input source results in the set of constraints on the input currents,

$$i_+ = \frac{(v_{sc} - e_{cc})}{Z_1} \tag{2.58}$$

$$i_- = \frac{(v_{sc} - e_{cc})}{Z_2}, \tag{2.59}$$

while shorting the CM input source results in the set of constraints on the input currents,

$$i_+ = \frac{(\frac{1}{2}v_{sd} - e_{cc})}{Z_1} \tag{2.60}$$

$$i_- = \frac{(-\frac{1}{2}v_{sd} - e_{cc})}{Z_2}. \tag{2.61}$$

In either case, the node voltage e_{cc} in Figure 2-6(c) is constrained to be

$$e_{cc} = e_c + (i_+ + i_-)Z_c. \tag{2.62}$$

Solving for $i_{id} = (i_+ - i_-)/2$ and $i_{ic} = (i_+ + i_-)$ leads to four permutations of constraints corresponding to the four transconductances. For instance, to find Y_{dd}, the CM input voltage is deactivated according to the definition in (2.52), and the DM input current is found from

$$i_{id} = \frac{i_+ - i_-}{2}, \tag{2.63}$$

with the three constraints from KVL above, (2.60), (2.61), and (2.62). Solving for i_{id}/v_{sd} and simplifying leads to:

$$Y_{dd} = \frac{2\overline{Z_f} + Z_1 + Z_2}{4(Z_1||Z_2 + \frac{1}{2}\overline{Z_f})(Z_1 + Z_2) + \Delta Z \Delta Z_f}. \tag{2.64}$$

The denominator in Y_{dd} above appears in all four transconductances. The quantities

in that denominator can be identified with respect to physical current paths in the voltage amplifier as follows:

$$Z_{dm} = Z_1 + Z_2 \tag{2.65}$$

$$Z_{cm} = Z_1||Z_2 + \frac{\overline{Z_f}}{2}. \tag{2.66}$$

For the simplified model of Figure 2-6(c), Z_{dm} is the impedance seen by a purely DM input voltage source driving a purely DM input current and Z_{cm} is the impedance seen by a purely CM input voltage source driving a purely CM input current. That is,

$$Z_{dm} = \left(\frac{v_{sd}}{i_{id}}\right)_{\substack{v_{sc}=0 \\ i_{ic}=0}} \tag{2.67}$$

$$Z_{cm} = \left(\frac{v_{sc}}{i_{ic}}\right)_{\substack{v_{sd}=0 \\ i_{id}=0}}. \tag{2.68}$$

Applying the constraints in the four permutations, simplifying and identifying the impedance terms Z_{dm} and Z_{cm} leads to the DM-DM transconductance,

$$Y_{dd} = 2\frac{\overline{Z_f} + \overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}, \tag{2.69}$$

the CM-DM transconductance,

$$Y_{cd} = 2\frac{-\Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}, \tag{2.70}$$

the DM-CM transconductance,

$$Y_{dc} = 2\frac{\Delta Z_f - \Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}, \tag{2.71}$$

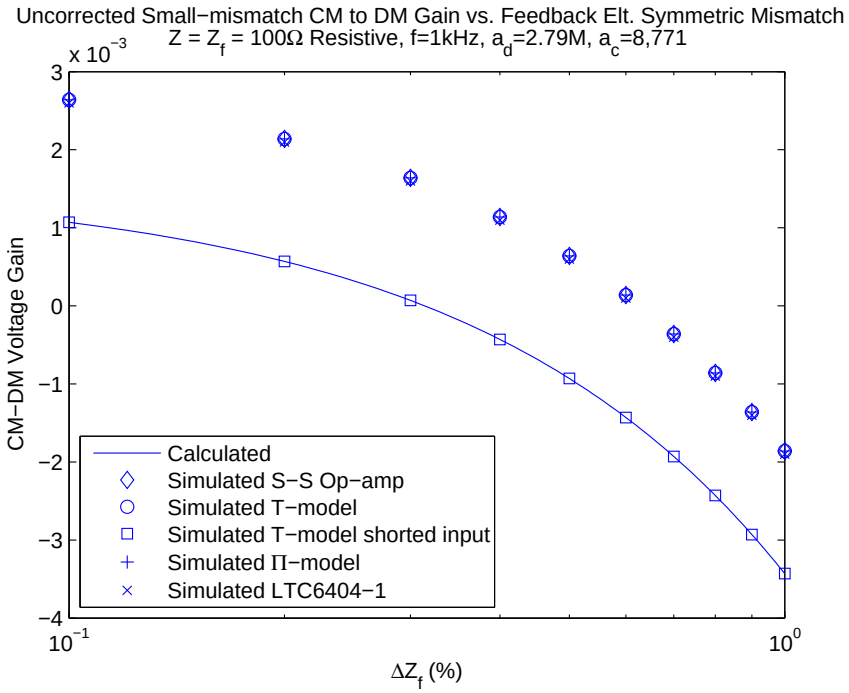
and the CM-CM transconductance,

$$Y_{cc} = 8\frac{\overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}. \tag{2.72}$$

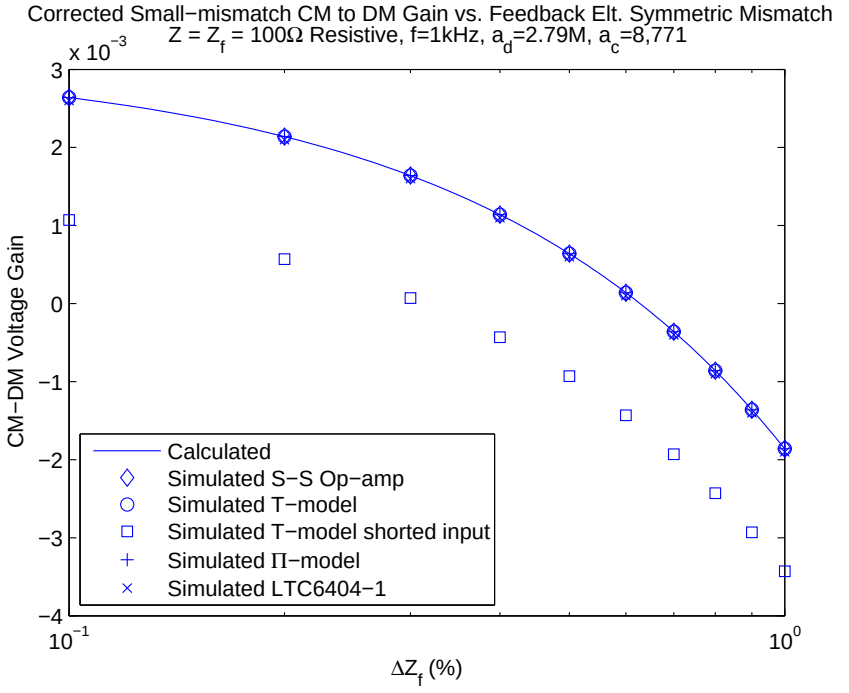
The common denominator in these transconductances aids further analysis when we form linear combinations of these terms (see Section 2.3.3).

2.3.1 Model Correction

The virtual short-circuit approximation led to some inaccuracy in the results for CM-DM gain, A_{vc}, in the small-mismatch region, Figure 2-7(a). The modularity of the results allows for rapid correction of this inaccuracy. Adding the effect of $e_d(i_{ic})$ is most critical for correcting A_{vc} because it accounts for a DM input voltage in response to a CM input current. Among the two transconductaces that affect CM-DM gain, Y_{cd} quantifies the DM input current, which is most directly affected by the addition of $e_d(i_{ic})$ to the model. This correction rederives Y_{cd} from the circuit in Figure 2-6(d), while Y_{cc} is assumed sufficiently accurate.



(a) Small-mismatch "zoom-in" of A_{vc} for $\Delta Z_f > 0$ (uncorrected). Plotting A_{vc} for $\Delta Z > 0$ results in a very similar plot. The calculated line falls on the shorted-input model data instead of the more accurate simulated data.



(b) Small-mismatch "zoom-in" of A_{vc} for $\Delta Z_f > 0$ (corrected). A plot of A_{vc} for $\Delta Z > 0$ is very similar. Small-mismatch CM-DM gain agrees well with simulated circuits after the correction is added.

Figure 2-7: Accuracy improvement for small-mismatch A_{vc}.

The circuit in Figure 2-6(d) leads to the following constraints. The DM input current is,

$$\begin{aligned} i_{id} &= i_{ed} + \frac{e_d}{4Z_c} \\ &= i_{ed} + i'_{id}, \end{aligned} \tag{2.73}$$

while the CM input current is,

$$i_{ic} = i_+ + i_- = i'_{ic}, \tag{2.74}$$

where we have made the following definitions:

$$i'_{id} \equiv \frac{1}{2}(i'_+ - i'_-) \tag{2.75}$$

$$i'_{ic} \equiv i'_+ + i'_- = i_{ic} \tag{2.76}$$

and the current through the added DM voltage element is

$$\begin{aligned} i_{ed} &= i_+ - i'_+ \\ &= i'_- - i_-. \end{aligned} \tag{2.77}$$

Finally, applying KVL results in two equations:

$$v_{sc} - i_+ Z_1 - e_d - i'_- 2Z_c - e_c = 0 \tag{2.78}$$

$$v_{sc} - i_- Z_2 + e_d - i'_+ 2Z_c - e_c = 0. \tag{2.79}$$

Solving these constraints for the "corrected transconductance," $Y'_{cd} = (i_{id}/v_{sc})_{v_{sd}=0}$, leads to

$$Y'_{cd} = \frac{Y_{cc}(\overline{Z_f}\Delta Z + \overline{Z}\frac{\Delta Z_f + a_c\overline{Z_f}}{1+a_d}) - \Delta Z}{4Z_1Z_2 + \frac{1}{2}\Delta Z_f \Delta Z}, \tag{2.80}$$

which is more complicated than the expressions in (2.69)-(2.72). Because the small-

mismatch region is of interest here, Y'_{cd} can be simplified with the small-mismatch approximations,

$$\Delta Z_f << Z_{f1}, Z_{f2}, \overline{Z_f} \tag{2.81}$$

$$\Delta Z << Z_1, Z_2, \overline{Z}, \tag{2.82}$$

which imply that $Z_{f1} \approx Z_{f2} \approx \overline{Z_f}$ and $Z_1 \approx Z_2 \approx \overline{Z}$. The "small-mismatch corrected transconductance" becomes

$$Y'_{cds} \approx \frac{\frac{\overline{Z_f} a_c}{1+a_d} - \Delta Z}{2 Z_{dm} Z_{cm}}. \tag{2.83}$$

The denominator in (2.83) can be forced to match the common denominator from the other three transconductances by multiplying the numerator and denominator by 2 and adding the small quantity, $\Delta Z \Delta Z_f$, back in:

$$Y'_{cds} \approx 2\frac{\overbrace{\overline{Z_f}\frac{a_c}{1+a_d}}^{\text{correction term}} - \Delta Z}{4 Z_{dm} Z_{cm} + \Delta Z_f \Delta Z}. \tag{2.84}$$

Comparing Y'_{cds} from (2.84) to Y_{cd} from (2.70), reveals that they differ only in the "correction term" $\left(\overline{Z_f}\frac{a_c}{1+a_d}\right)$.

Model validation (Figure 2-7(b)) with this corrected Y'_{cds} shows good agreement for small mismatch values. Although Y'_{cds} was calculated while assuming small mismatches, model valdiatons will show that the full model, including the corrected Y'_{cds}, agrees for the range $0\% - 200\%$ of resistive element mismatch values. Therefore, the following results, including Y'_{cds}, are proposed as the full transconductance-transimpedance descriptive abstraction of the FD voltage amplifier. The DM-DM and CM-DM transconductances are

$$Y_{dd} = 2\frac{\overline{Z_f} + \overline{Z}}{4 Z_{cm} Z_{dm} + \Delta Z \Delta Z_f} \tag{2.85}$$

$$Y'_{cds} = 2\frac{\overline{Z_f}\left(\frac{a_c}{1+a_d}\right) - \Delta Z}{4 Z_{cm} Z_{dm} + \Delta Z \Delta Z_f}, \tag{2.86}$$

while the DM-CM and CM-CM transconductances are

$$Y_{dc} = 2\frac{\Delta Z_f - \Delta Z}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \tag{2.87}$$

$$Y_{cc} = 8\frac{\overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f} \tag{2.88}$$

and the transimpedance amplifier results are repeated here for convenience:

$$Z_{dd} = 2\frac{a_d\overline{Z_f} - a_c\Delta Z_f/2}{(1+a_d)} \tag{2.89}$$

$$Z_{cd} = \frac{1}{2}\frac{a_c\overline{Z_f} - a_d\Delta Z_f}{(1+a_d)}. \tag{2.90}$$

The results in (2.85)-(2.90) yield the full expression for the DM output voltage when substituted into the following expression:

$$\boxed{v_{od} = v_{sd}(Y_{dd}Z_{dd} + Y_{dc}Z_{cd}) + v_{sc}(Y'_{cds}Z_{dd} + Y_{cc}Z_{cd})}. \tag{2.91}$$

2.3.2 Voltage Amplifier Input Impedance

Input impedances for the voltage-mode amplifier may be taken directly from the transconductances as follows. The DM input impedance is

$$Z_{ind} \equiv \left(\frac{v_{sd}}{i_{id}}\right)_{v_{sc}=0} = Y_{dd}^{-1} \tag{2.92}$$

and the CM input impedance is

$$Z_{inc} \equiv \left(\frac{v_{sc}}{i_{ic}}\right)_{v_{sd}=0} = Y_{cc}^{-1}, . \tag{2.93}$$

The results above can be written as follows. The DM input impedance is

$$Z_{ind} = \frac{1}{2}\frac{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}{\overline{Z_f} + \overline{Z}} \tag{2.94}$$

and the CM input impedance is

$$Z_{inc} = \frac{1}{8}\frac{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}{\overline{Z}}. \tag{2.95}$$

Simplifying the expressions for DM and CM input impedance with the small-mismatch approximations in (2.81)-(2.82) leads to the "small-mismatch DM input impedance,"

$$\boxed{Z_{inds} = Z_{dm} = Z_1 + Z_2}, \tag{2.96}$$

and the "small-mismatch CM input impedance,"

$$\boxed{Z_{incs} = Z_{cm} = Z_1 || Z_2 + \frac{\overline{Z_f}}{2}}, \tag{2.97}$$

which can be approximated for intuition as

$$Z_{incs} \approx Z_1 || Z_2 + Z_{f1} || Z_{f2}. \tag{2.98}$$

The DM and CM input impedance expressions, especially (2.96) and (2.98), are intuitive when following the respective current paths (Figure 2-2(b)) through the amplifier. As one might expect, the special-case impedances, Z_{dm} and Z_{cm} from (2.65) and (2.66), are related to the input impedances, Z_{ind} and Z_{inc} in (2.94)-(2.97). In fact, Z_{dm} and Z_{cm} are, by definition, special cases of Z_{ind} and Z_{inc}. Mathematically, the special-case impedance, Z_{dm} is related to the DM input impedance:

$$Z_{dm} = Z_{ind}|_{i_{ic}=0} \tag{2.99}$$

and the special-case impedance, Z_{cm} is related to the CM input impedance:

$$Z_{cm} = Z_{inc}|_{i_{id}=0}\,. \tag{2.100}$$

Moreover, the results in equations (2.96) and (2.97) suggest that those special cases are coincident with small mismatches in the external homologous elements.

2.3.3 Discussion and Model Validation

Familiar quantities such as DM-DM gain, A_{vd}, and common-mode rejection ratio, CMRR, are readily extracted and simplified from the modularized result. For instance, DM-DM gain in the result from (2.91) is

$$A_{vd} \equiv \left(\frac{v_{od}}{v_{sd}}\right)_{v_{sc}=0} = Y_{dd}Z_{dd} + Y_{dc}Z_{cd}, \tag{2.101}$$

and expanding this leads to the full DM voltage gain expression,

$$A_{vd} = \frac{4(\overline{Z_f}+\overline{Z})(a_d\overline{Z_f} - \frac{a_c\Delta Z_f}{2}) + (\Delta Z_f - \Delta Z)(a_c\overline{Z_f} - a_d\Delta Z_f)}{(4Z_{cm}Z_{dm} + \Delta Z\Delta Z_f)(1+a_d)}. \tag{2.102}$$

This full gain expression can be simplified to suit the particular non-idealities of interest. For instance, if mismatches are small, the difference between them is smaller ($\Delta Z_f - \Delta Z \approx 0$), and the second term in the numerator of (2.102) can be disregarded leaving only $A_{vd} \approx Y_{dd}Z_{dd}$. In the small-mismatch approximation this becomes

$$A_{vd} \approx \frac{4(\overline{Z_f}+\overline{Z})(a_d\overline{Z_f} - \frac{1}{2}a_c\Delta Z_f)}{(4Z_{cm}Z_{dm})(1+a_d)}, \tag{2.103}$$

where the small second-order mismatch term in the denominator has been left out. Expanding the impedances, Z_{dm} and Z_{cm}, the DM voltage gain above reduces to

$$\boxed{A_{vds} = \frac{(a_d\overline{Z_f} - \frac{1}{2}a_c\Delta Z_f)}{\overline{Z}(1+a_d)}}, \tag{2.104}$$

where we define A_{vds} as the "small-mismatch DM voltage gain." In the fully-ideal limit, $a_d \to \infty$ and $a_c \to 0$

$$\boxed{A_{vdo} = \frac{\overline{Z_f}}{\overline{Z}}}, \tag{2.105}$$

where we define A_{vdo} as the "fully-ideal voltage gain." The form of A_{vdo} is consistent with intuition that we bring from SE amplifier cases.

Also from (2.91), the CM-DM cross-coupling gain is

$$A_{vc} \equiv \left(\frac{v_{od}}{v_{sc}}\right)_{v_{sd}=0} = Y'_{cds}Z_{dd} + Y_{cc}Z_{cd}. \tag{2.106}$$

Model validation plots for the voltage amplifier results are shown in Figures 2-8 and 2-9. The calculated results for A_{vd} and A_{vc} were overlayed on the simulated results for the circuit models, a small-signal ("s-s") op-amp model, and a simulated commercial op-amp. The top rows in Figures 2-8 and 2-9 show A_{vd} and A_{vc} across mismatches in the feedback elements, ΔZ_f, while the bottom rows show the same for mismatches in the input elements, ΔZ. The model validation results show good agreement among the calculated and simulated results.

The plots in Figures 2-8 and 2-9 include comparisons to the results from a half-circuit analytical example found in reference [58] demonstrating the break down of the half-circuit analytical approach for large mismatches and, in some cases, for relatively small mismatches. Reference [58] did not consider mismatches in the feedback elements so the plots showing the quantities across feedback element mismatch are somewhat trivial. However, reference [58] did include the effect of the CM-CM gain of the op-amp. That value was measured for the LTC6404-1 part as $a_{cm} = -0.043$ and was used for plotting the results.

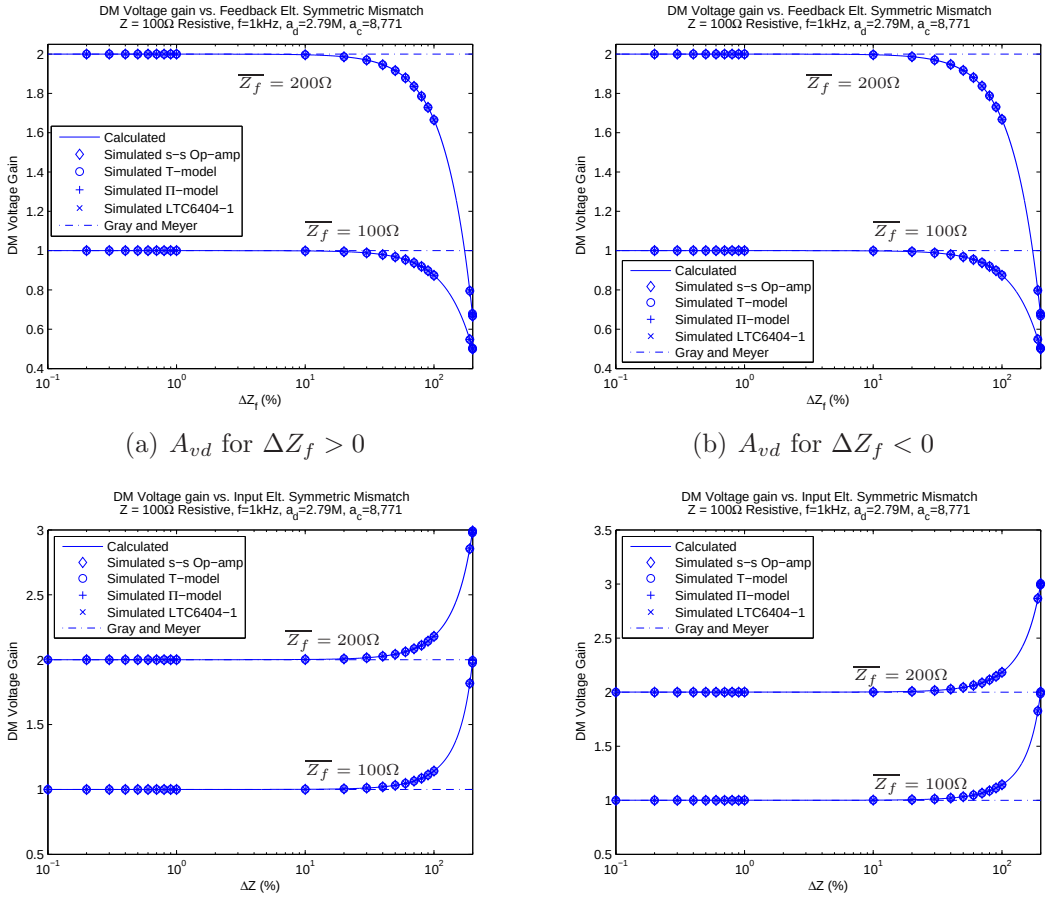
Dividing the CM-DM voltage gain by the DM-DM voltage gain yields the common-mode rejection,

$$\text{CMR} \equiv \left(\frac{A_{vc}}{A_{vd}}\right) = \frac{Y'_{cds}Z_{dd} + Y_{cc}Z_{cd}}{Y_{dd}Z_{dd} + Y_{dc}Z_{cd}}, \tag{2.107}$$

which can be simplified by neglecting small terms to get the approximate CMR:

$$\text{CMR} \approx \frac{4(\overline{Z_f}\left(\frac{a_c}{1+a_d}\right) - \Delta Z)a_d\overline{Z_f} + 4\overline{Z}(a_c\overline{Z_f} - a_d\Delta Z_f)}{4(\overline{Z_f} + \overline{Z})a_d\overline{Z_f} + (\Delta Z_f - \Delta Z)(a_c\overline{Z_f} - a_d\Delta Z_f)} \tag{2.108}$$

The common denominator in the transconductances (2.85)-(2.88) divides out, simplifying the calculation above. Collecting terms, approximating $(1 + a_d) \approx a_d$, and



(a) A_{vd} for $\Delta Z_f > 0$

(b) A_{vd} for $\Delta Z_f < 0$

(c) A_{vd} for $\Delta Z > 0$

(d) A_{vd} for $\Delta Z < 0$

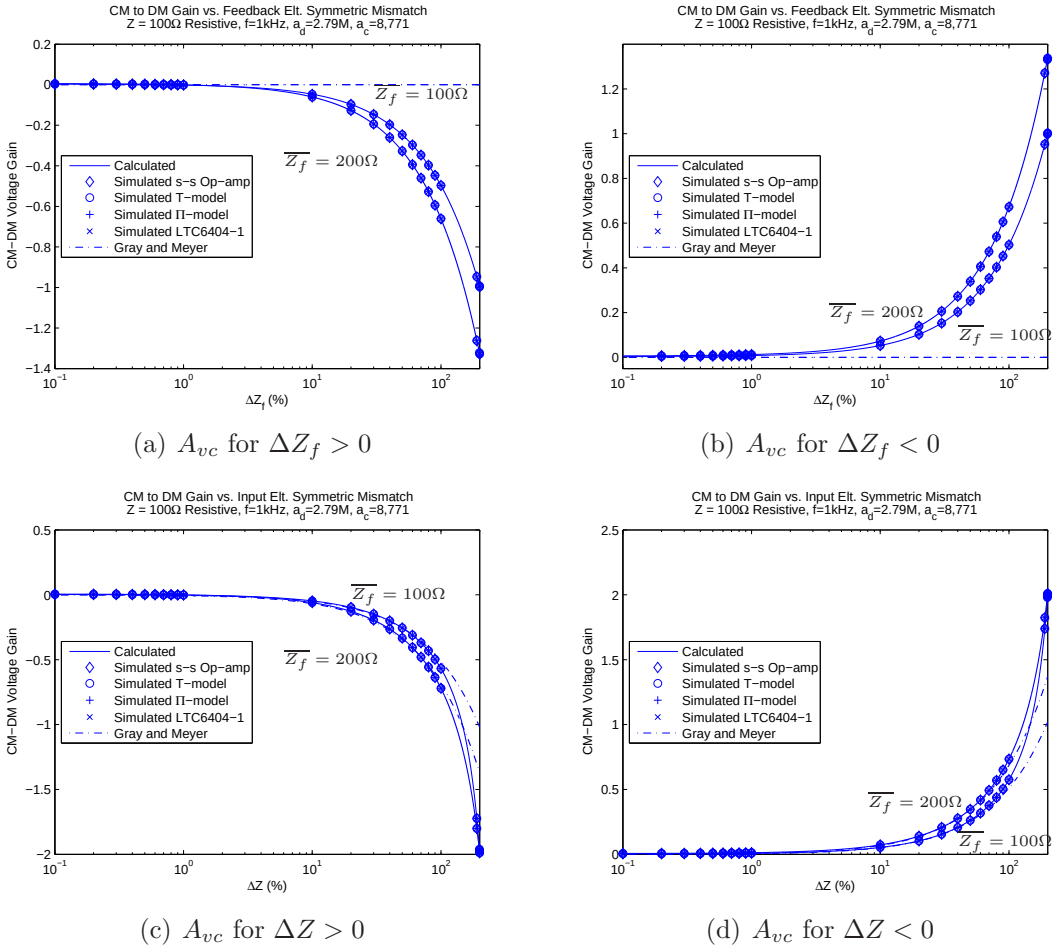
Figure 2-8: Validating the voltage amplifier model: A_{vd}. Impedances are purely real (resistive).

rewriting (2.108):

$$\boxed{\mathrm{CMR} \approx \frac{\frac{a_c}{a_d} - \frac{\frac{\overline{Z}}{\overline{Z_f}}\Delta Z_f + \Delta Z}{\overline{Z_f}+\overline{Z}}}{1 + \frac{(\Delta Z_f - \Delta Z)(\frac{a_c}{a_d} - \frac{\Delta Z_f}{\overline{Z_f}})}{4(\overline{Z}+\overline{Z_f})}}}. \tag{2.109}$$

Reducing (2.109) further with the small-mismatch approximations in (2.81) and (2.82), the denominator approaches 1, leaving the numerator and we arrive at the "small-mismatch common-mode rejection:"

$$\boxed{\mathrm{CMR}_s = \underbrace{\frac{a_c}{a_d}}_{\text{"op-amp gains"}} - \underbrace{\frac{\frac{\overline{Z}}{\overline{Z_f}}\Delta Z_f + \Delta Z}{\overline{Z_f}+\overline{Z}}}_{\text{"external elements"}}}, \tag{2.110}$$



(a) A_{vc} for $\Delta Z_f > 0$

(b) A_{vc} for $\Delta Z_f < 0$

(c) A_{vc} for $\Delta Z > 0$

(d) A_{vc} for $\Delta Z < 0$

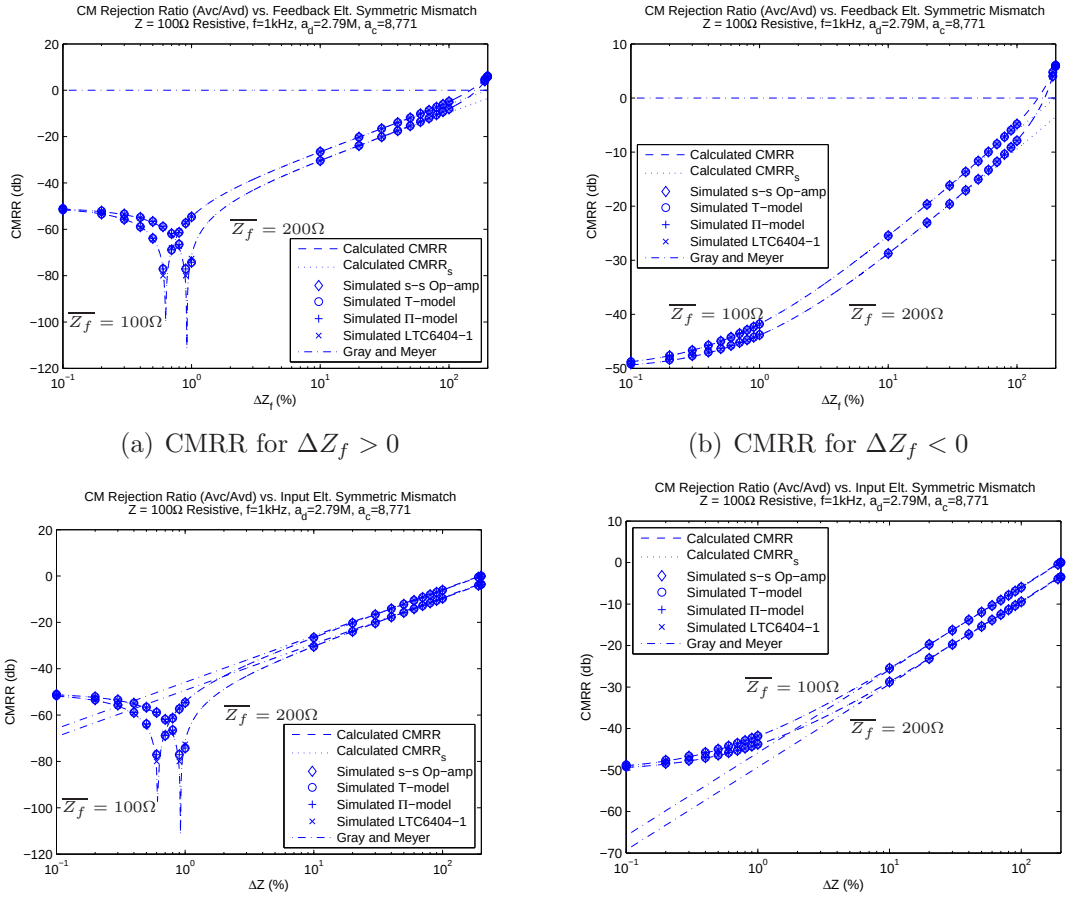
Figure 2-9: Validating the voltage amplifier model: A_{vc}. Impedances are purely real (resistive).

which is neatly separable into an "op-amp gain term" and an "external element term."

Model validation plots for CMR_s in Figure 2-10 show good agreement for symmetric mismatches up to about 100% in the feedback and input elements.[1] For calculating CMR with larger mismatches, the expression in (2.109) can be used for better accuracy as it is shows good agreement for large percentage mismatch (200%). Numerical results from the half-circuit decomposition analysis in reference [58] are overlaid on the lower plots. In Figures 2-10(a) and 2-10(b), the results from reference [58] are trivial because that analysis does not consider mismatches in feedback elements. In Figures 2-10(c) and 2-10(d), the results from reference [58] fail to predict the key

[1]CMRR is defined here as the logarithmic version of CMR measured in decibels, $\text{CMRR} \equiv 20\log_{10}|\text{CMR}|$.

feature, the null in the CMRR for nonzero-valued mismatches because that analysis does not consider the finite op-amp gain, a_c.



(a) CMRR for $\Delta Z_f > 0$

(b) CMRR for $\Delta Z_f < 0$

(c) CMRR for $\Delta Z > 0$

(d) CMRR for $\Delta Z < 0$

Figure 2-10: Finite op-amp CM gains, a_d and a_c, lead to a null in the CMRR at nonzero mismatch values.

The cancelation effect at nonzero-valued mismatch results from the finite DM and CM gains of the op-amp, a_d and a_c, as is clear from the CMR expression in (2.110). For example, with $\overline{Z_f} = 100\Omega$, the optimal mismatch for the LTC6404-1 for either the feedback or input element mismatch alone is about 0.61% as shown in Figure 2-10. In theory, arbitrarily small CMR values could be obtained by adjusting the mismatches to achieve zero-valued CM-DM gain. In practice, such control over the mismatch is perhaps difficult. The zero-crossing of the CM-DM gain, which leads to the null in the CMRR, is also evident in the plot of Figure 2-7(b) from Section 2.3.1. Note that the plots for CMRR in Figure 2-10 approach the CMRR of the op-amp, -50 db, for

zero-valued mismatches also in agreement with (2.110).

2.3.4 Sensitivity

The results in Sections 2.2 and 2.3 indicate good model accuracy having considered op-amp gain parameters, a_d and a_c. Examining the sensitivity of the mathematical model to those parameters may reveal the amount of modeling error caused by uncertainties in our knowledge of the op-amp gain parameters. It may also reveal the amount that particular performance metrics change as op-amp gain parameters vary in time due temperature effects, etc. In either case, the simple derivative may be employed to examine the effect of changes in the op-amp gain parameters.

For example, starting from (2.110), the value of feedback impedance mismatch, ΔZ_f, corresponding to the null in the CMRR varies with op-amp gain parameters as follows. The sensitivity to changes in DM-DM op-amp gain of the feedback impedance mismatch value corresponding to the null is

$$a_d \left.\frac{\partial \Delta Z_f}{\partial a_d}\right|_{\substack{\mathrm{CMRR}\to-\infty \\ \Delta Z=0}} = -\frac{a_c}{a_d}\frac{\overline{Z_f}}{\overline{Z}}\left(\overline{Z_f}+\overline{Z}\right), \tag{2.111}$$

while the sensitivity to changes in CM-DM op-amp gain is

$$a_c \left.\frac{\partial \Delta Z_f}{\partial a_c}\right|_{\substack{\mathrm{CMRR}\to-\infty \\ \Delta Z=0}} = \frac{a_c}{a_d}\frac{\overline{Z_f}}{\overline{Z}}\left(\overline{Z_f}+\overline{Z}\right). \tag{2.112}$$

Analysis regarding the value of input element mismatch leads to similar results. Note that the error due to changes in a_d is simply the negative of the error due to changes in a_c.

As a numerical example, consider the nominal impedances $\overline{Z_f} = \overline{Z} = 100\ \Omega$ and op-amp gain parameters from the simulations above. Using (2.111), a fractional change in DM op-amp gain, $\partial a_d/a_d = -0.15$, corresponding to a multiplicative error of 0.85, leads to an error in the location of the null of approximately +0.09% in agreement with the results plotted in Figure 2-11. Figure 2-11 also illustrates the effect of larger changes in a_d. Naturally, the zero-mismatch CMRR should increase

as a_d decreases, also in agreement with Figure 2-11.

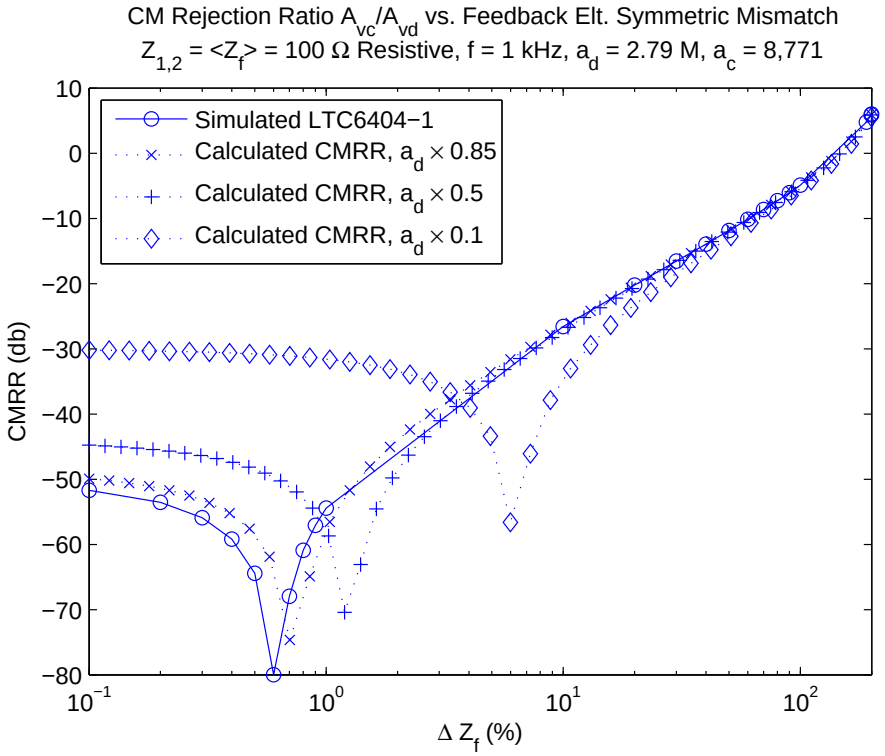


Figure 2-11: Plots of CMRR for various multiplicative errors in op-amp gain a_d compared to the actual CMRR for the Linear Technology part LT6404-1.

2.3.5 Finite Op-amp Input Impedance

The results above were calculated based on the op-amp model in Figure 2-3 and the assumptions described in Section 2.1.3. Model validation showed excellent agreement among the calculated results and the behavior of a commercial FD op-amp. In general, there may be a need to include other aspects in the op-amp model. The versatility of the transimpedance amplifier abstraction developed in Section 2.2 was demonstrated in a first example, by adding to it the input elements, Z_1 and Z_2, yielding a voltage amplifier. Here, we consider the addition of finite op-amp input impedance to the idealized op-amp model of Figure 2-3.

The op-amp input impedance elements can be modeled as shunt impedances at the op-amp input nodes to incremental ground. The addition of those impedances can be viewed as a modification of the voltage amplifier analysis in Section 2.3 leading to

the four transconductances, $Y_{dd} - Y_{cc}$. Because the transimpedance amplifier model responses were derived in terms of the input currents i_+ and i_-, only the voltage amplifier analysis needs to be iterated.

Using the Thevenin equivalent circuits comprised of the input voltage sources and impedances Z_1, Z_2 and the additional op-amp input impedance elements, equations (2.58)-(2.61) become

$$i_+|_{v_{sd}=0} = \frac{(v_{sc}\frac{Z_{in1}}{Z_{in1}+Z_1} - e_{cc})}{Z_1||Z_{in1}} \tag{2.113}$$

$$i_-|_{v_{sd}=0} = \frac{(v_{sc}\frac{Z_{in2}}{Z_{in2}+Z_2} - e_{cc})}{Z_2||Z_{in2}} \tag{2.114}$$

$$i_+|_{v_{sc}=0} = \frac{(\frac{1}{2}v_{sd}\frac{Z_{in1}}{Z_{in1}+Z_1} - e_{cc})}{Z_1||Z_{in1}} \tag{2.115}$$

$$i_-|_{v_{sc}=0} = \frac{(-\frac{1}{2}v_{sd}\frac{Z_{in2}}{Z_{in2}+Z_2} - e_{cc})}{Z_2||Z_{in2}}. \tag{2.116}$$

Starting from these modified constraints, one can re-derive the four tranconductances in terms of op-amp input impedances, Z_{in1} and Z_{in2}, while keeping the same results for the two transimpedances found in Section 2.2.

2.4 Experimental Validation

This treatment of FD amplifiers was motivated by an investigation of a particular capacitive sensing occupancy detector. The sensor, presented in [1], employs a FD amplifier connected between two electrodes, to measure changes in a physically balanced bridge network comprised of the lumped capacitances between conducting bodies in the detection field. A half-circuit representation of the FD amplifier was not suitable for capturing the effect of the arbitrarily varying capacitive impedances in the bridge network nor was it sufficient to account for the effects of the amplifier's separate DM and CM current paths. Only a generalized model with an unbroken structure could accurately represent these effects.

Figure 2-13 shows a schematic of the signal conditioning electronics for this ca-

pacitive sensor including the FD front-end amplifier. Also shown in the Figure is a simplified depiction of the lumped element capacitive bridge network. The capacitive impedances in the bridge network correspond to the input impedance elements Z_1 and Z_2 in Figure 2-1. The FD front-end amplifier is loaded by a FD multiplier circuit used to synchronously detect modulations of the high frequency carrier signal caused by the presence of the occupant. More details can be found in [1].

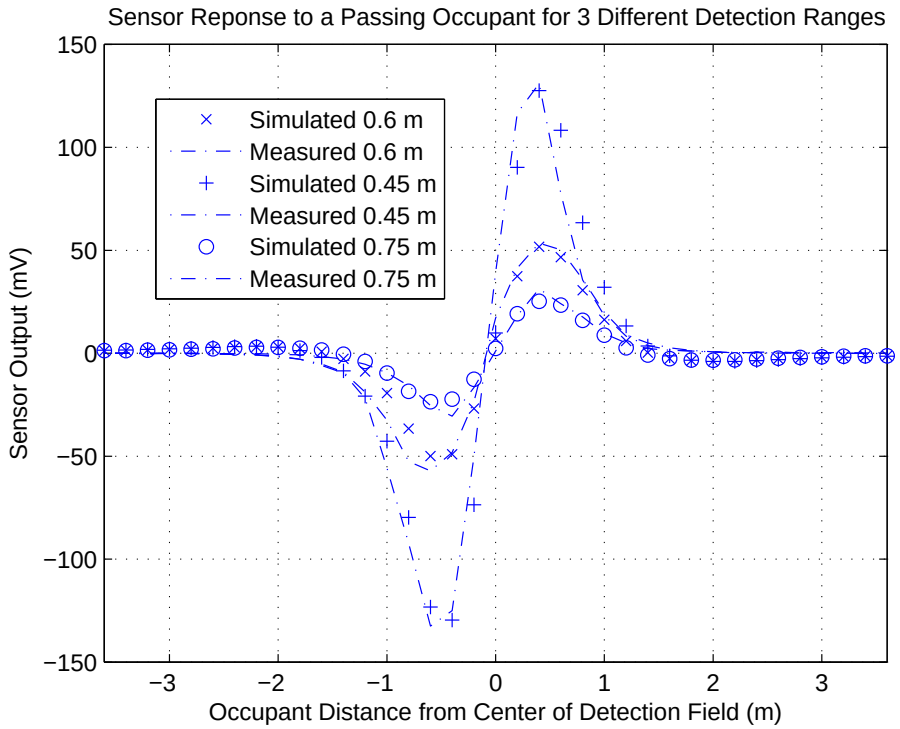


Figure 2-12: Plot of simulated and measured occupancy sensor output data from reference [1].

A comparison of experimental and simulated data further validated the analytical modeling in this work. Experimental data was taken from an implemented capacitive sensor using the electronics shown in Figure 2-13. Simulated data was taken from a SPICE simulation of the experimental setup having replaced the front-end amplifier with the circuit model of the FD amplifier in Figure 2-4(b). Finite op-amp input impedances as well as coaxial shield stray capacitances were included in the simulated model as shunt impedances at the input terminals to the transimpedance amplifier circuit model. Model parameters, a_d and a_c, for the FD front-end circuit model were

taken from the datasheet for the THS4140 FD op-amp at the signal frequency, 50 kHz in this example.

Finite element modeling software, FastCap®, was used to determine the values of the lumped element capacitances needed for the SPICE simulation. To simulate a passing occupant, the FastCap® simulation was re-run for several different configurations of the system corresponding to different time steps as the occupant passed through the detection field. Details can be found in reference [1].

Model validation results showing excellent agreement are plotted in Figure 2-12 for three different detection ranges as the occupant passes through the detection field.

2.5 Conclusion

A new approach for small-signal analysis of fully-differential (FD) closed-loop op-amp circuits is presented. The approach is built upon the development a circuit model for a FD transimpedance amplifier. The circuit model of the FD transimpedance amplifier enables analysis and simulation of practical FD circuits and captures the distinct CM and DM paths through the amplifier. Simulated model validation showed excellent agreement between the calculated results and the performance of a commercial FD op-amp. Experimental model validation showed excellent agreement between the behavior of the simulated FD transimpedance amplifier circuit model and an implemented capacitive sensor employing a FD front-end amplifier.

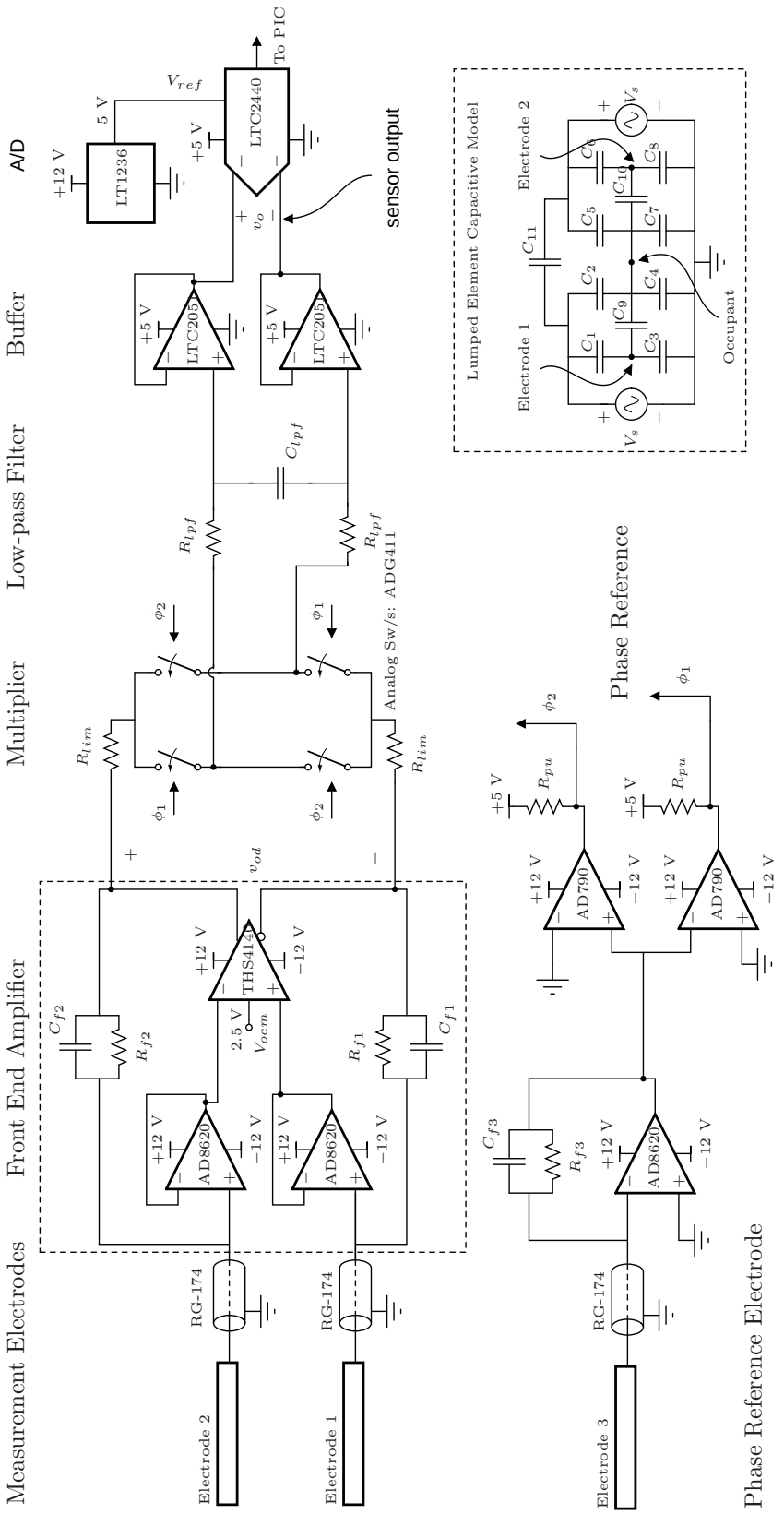


Figure 2-13: A simplified schematic of the fully-differential signal conditioning electronics

Chapter 3

Capacitive Sensing Fluorescent Lamps

3.1 Introduction

The U.S. Department of Energy has identified "sensing and measurement" as one of the "five fundamental technologies" essential for driving the creation of a "Smart Grid" [59]. In 2008, occupant-oriented loads such as lighting, and heating, ventilation and air conditioning (HVAC) accounted for 50% and 47% of the total consumed electricity in the U.S. for the residential and commercial sectors, respectively [60]. The integration of smart grid-enabled control into industrial power electronic systems and occupant-based control of lighting have been shown to provide substantial benefits in this regard [61–63].

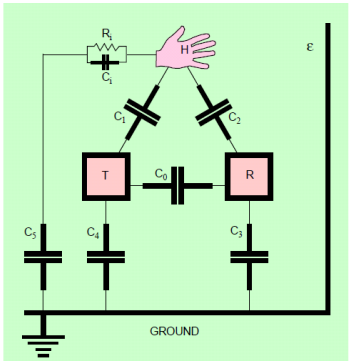
This chapter presents an occupancy detector that exploits a fluorescent lamp's own stray electric fields as an excitation source for capacitive sensing (the lamp sensor). Reuse of in-place fluorescent lamp infrastructure should support low-cost, widespread deployment. Additionally, the sensor measures electric fields rather than IR, so the usual limitations associated with PIR sensors are eliminated and true presence detection is feasible. Finally, by incorporating the sensor electronics in fluorescent lamps, control of lighting based on occupancy detection can be particularly straightforward. Reference [64] details an application example in which the lamp sensor directly con-

trols the lamp's power consumption using a custom dimming fluorescent lamp ballast [65–67]. Significantly, [64] demonstrates good detection sensitivity even at very low bulb power (1%). The "autodimming" lamp obviates the need for frequent lamp ignition which has been shown to impact bulb life [67, 68].

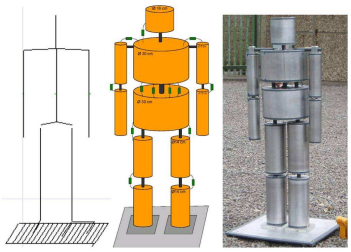
Pyroelectric Infrared (PIR) sensors have been used extensively for low-cost occupancy detection [69–71]. Typically, the ability of a PIR sensor to function as a presence detector is limited by low-frequency noise or drift from changes in background infrared radiation (IR). The measured signals can be bandlimited (high-pass filtered), but the sensor effectively becomes a motion sensor, not a presence sensor [69, 70]. As an alternative to PIR sensors, reference [4] presents a retrofit capacitive sensor for detecting occupants using in-place utility wiring and demonstrates detection ranges of about 1 m from the wire to the occupant. The sensor presented here demonstrates detection ranges approximately three times as long as those in [4].

Reference [4] is one of many references that set a precedent for modeling a human as a conducting body. Other such precedents can be found in references [3, 5–9]. Figure 3-1 shows some human conductor models from those references. Reference [6] demonstrates capacitive sensors for occupancy sensing in automobiles and [7] demonstrates a human capacitive sensor for robotics applications. Other applications of capacitive sensors include fingerprint sensing [72–75], MEMS accelerometers and position sensors [76–80], pressure [81], humidity [82], and angular speed sensors [83], an underground power cable sensor [84], and a sensor for micro-fluids [85]. Capacitive sensors are also found in Medical applications [9, 86, 87]. Reference [88] uses daylight MEMS sensors to inform a lighting energy management system.

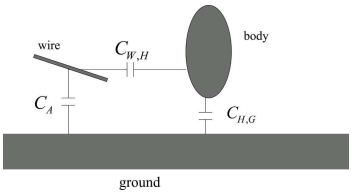
Section 3.2 reviews and develops the basic operating principles and modeling of the lamp sensor system. Section 3.3 presents the implementation of a lamp sensor including a discussion of key design principles and experimental data from a cart-mounted lamp sensor. Section 3.4 presents the results of a range test for the cart-mounted lamp sensor. Section 3.5 presents a new full system model and validates it against experimental data from a hanging lamp sensor.



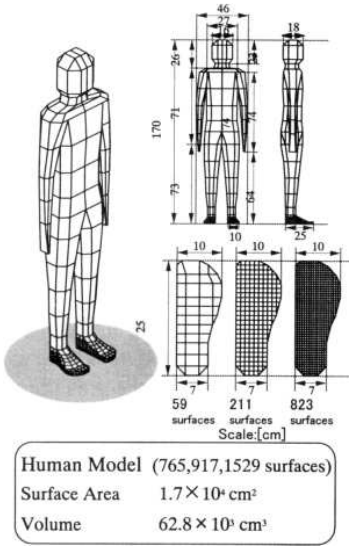
(a) 3D touchless computer mouse: [2]



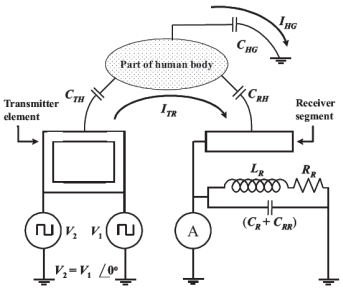
(b) Modeling utility linesman potentials: [3]



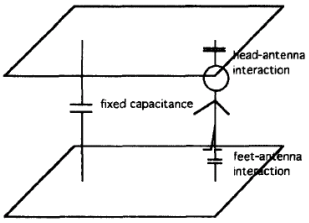
(c) Utility wiring occupancy sensing: [4]



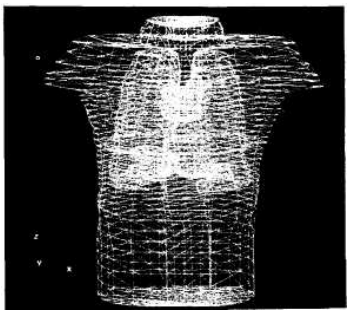
(d) Human body capacitance modeling for ESD studies: [5]



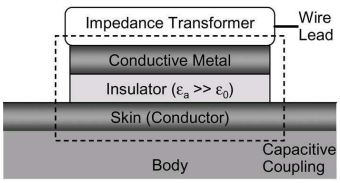
(e) Passenger vehicle seat occupancy sensing: [6]



(f) Human occupancy sensor for robotics: [7]



(g) Conductor model of the human thorax for medical applications: [8]



(h) Capacitive sensing of the heart for medical applications: [9]

Figure 3-1: Examples of systems with human conductor models taken from references [2–9].

3.2 Modeling

The operation of the lampsensor system can be understood with a capacitive abstraction which models the behavior of the electrostatic fields coupling the conducting objects below the lamp. Implicit in this abstraction is the assumption that the electric fields vary slowly enough that the system is quasistatic – an assumption that holds for any reasonable lamp ballast operating frequency (10-100 kHz). In this section, the link between electrostatic field modeling and the capacitive abstraction is briefly reviewed starting from Maxwell's equations. Then, the development of a capacitive model is discussed by considering models of the key system elements.

The boundary conditions that arise from Maxwell's equations are useful for studying these interactions. For instance, from one of Maxwell's equations, the electric Gauss' Law, the gradient (spatial derivative) of the electric flux density, $\vec{D}$, is equal to the volumetric charge density, ρ_v, with units C/m^3, i.e.

$$\nabla \cdot \vec{D} = \nabla \cdot \epsilon \vec{E} = \rho_v. \tag{3.1}$$

Taking a fixed volume of charge with charge density ρ_v, and shrinking its thickness to zero yields a charged planar boundary with "surface charge density" ρ_s having units C/m^2. For instance, for $\rho_s = 1$ C/m^2, a plane with area 1 m^2 contains 1 C of charge. Gauss' electric law (3.1) then leads directly to a constraint on the electric flux density on sides "1" and "2" of an arbitrary planar boundary (boundary condition):

$$\boxed{\hat{n} \cdot \left(\vec{D_1} - \vec{D_2}\right) = \rho_s}, \tag{3.2}$$

where $\hat{n}$, is a unit vector normal to the boundary surface, i.e. the discontinuity in the electric flux normal to a boundary aries from the surface charge on that boundary.

From another of Maxwell's equations, Faraday's law: $\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$, the curl of the electric field strength is proportional to the time derivative of the proximal

magnetic flux density. In integral form, Faraday's law is

$$\oint_S \vec{E} \cdot dl = -\frac{\partial \Phi_B(t)}{\partial t}, \tag{3.3}$$

where $\Phi_B(t)$ is the magnetic flux impinging the surface, S, enclosed by the line integral $\oint_S$. Holding one dimension of the surface, S, fixed and pinching the other dimension until it shrinks to zero, the magnetic flux and its time derivative through that surface (the right side of (3.3)) also shrinks to zero. To make the closed integral of $\vec{E}$ (the left side of (3.3)) equal to zero, adjacent components of the electric field strength must be equal in magnitude and direction. Therefore, the boundary condition on $\vec{E}$ is:

$$\boxed{\hat{n} \times \left(\vec{E_1} - \vec{E_2}\right) = 0}, \tag{3.4}$$

i.e. tangential components of electric field strength are continuous. Combining the boundary condition in (3.4) with the fact that the electric field strength inside a conductor is forced to zero reveals that the tangential component of $\vec{E}$ at the surface of the conductor is zero. Therefore, the electric field must terminate normal to the surface. Adding to this, the boundary condition on the electric flux density (3.2), reveals that the electric field at the surface is both normal to the (conducting) surface *and* equal to the surface charge density divided by the permittivity of the medium around the conductor, i.e. $\vec{E} = \vec{E_n} = \frac{\rho_s}{\epsilon}$. The total charge in an area, A, on the surface of a conductor is therefore,

$$\begin{aligned} Q(t) &= \iint_A \rho_s(t) dA \\ &= \epsilon \iint_A \vec{E_n}(t) \cdot d\vec{A}, \end{aligned} \tag{3.5}$$

so the charge is equal to the permittivity times the electric flux,

$$Q(t) = \epsilon \Phi_e(t), \tag{3.6}$$

where $\Phi_e(t)$ is the total electric flux impinging normal to the surface with area A. If

the electric field impinging on the surface of the conductor is the result of the potential on a second conductor, then the potential difference between any two points on those two conductors is

$$v_c(t) = \int_s \vec{E}(t) \cdot d\vec{s}, \tag{3.7}$$

where (little) s is an arbitrary path between the two conductors. The voltage, $v_c(t)$, must be the potential difference between any points on those two conductors since they are both equipotential surfaces. Dividing the total charge on either conductor by this potential difference, by definition, yields the capacitance, i.e.

$$C \equiv \frac{\epsilon \iint_A \vec{E_n}(t) \cdot d\vec{A}}{\int_s \vec{E}(t) \cdot d\vec{s}} = \epsilon \frac{\Phi_e(t)}{v_c(t)}. \tag{3.8}$$

The current drawn onto a surface of area A, by an impinging electric field, $\vec{E_n}$, must be the time derivative of the total charge in that area. From (3.6), the current is then

$$\boxed{I(t) = \frac{\partial Q(t)}{\partial t} = \epsilon \frac{\partial \Phi_e(t)}{\partial t}}. \tag{3.9}$$

Examining the expression in (3.9) reveals two key insights. First, the time-derivative of the electric flux must be nonzero to support a current on the conductor (electrode). Therefore, the electrical signal source must be time-varying and in most practical situations will be ac. Second, the time-derivative between the electric field and the current indicates a 90° phase shift for each sinusoidal component of excitation. A measurement electrode can therefore be thought of as a transducer between electric field and current. The transducer has a gain term proportional to the electrode area, A, the permittivity of the space containing the electric field, ϵ, and the frequency of the sinusoidal component of interest, ω. It also has a phase term equal to 90°. Since the electric potential is always related to the electric field through a *spatial* not a time-derivative, that 90° phase shift occurs between the capacitor voltage and current as expected. Equation (3.8) implies that

$$\epsilon \Phi_e(t) = C v_c(t) \tag{3.10}$$

so that taking the time-derivative of both sides yields

$$\epsilon \frac{\partial \Phi_e(t)}{\partial t} = C \frac{\partial v_c(t)}{\partial t} \tag{3.11}$$

and comparing (3.11) to (3.9) reveals that

$$\boxed{I(t) = C \frac{\partial v_c(t)}{\partial t}} \tag{3.12}$$

as expected.

The capacitive abstraction approach in this work generally attempts to lump conducting objects in the lamp sensor system as nodes in a circuit model. For instance, the backplane of the lamp, the measurement electrodes, and other large unmovable conducting objects in the detection field are taken as conducting nodes in the system. References [2–9] set precedents for treating a human as a conducting shell. Therefore, the human "target" is also taken as a conducting (and moving) node in the system.

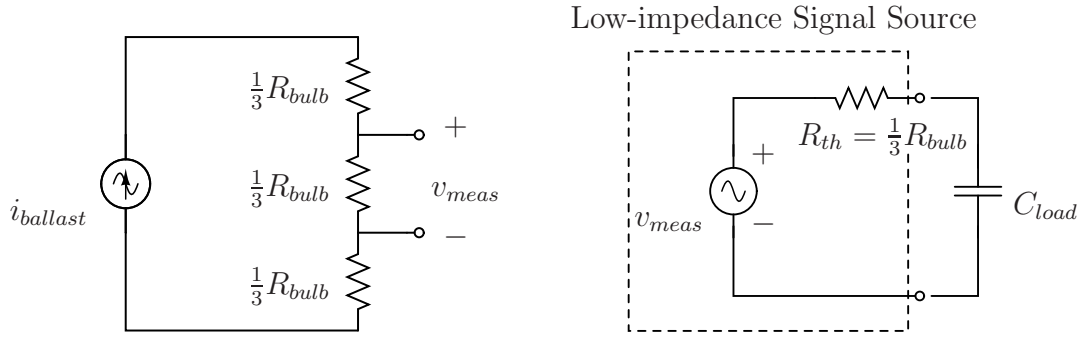
3.2.1 Modeling the Floor

It is difficult to generalize the floor below the lamp as a conducting or a nonconducting plane. The correct treatment is perhaps dependent on the particular construction of any given floor. Moreover, if the floor is taken as a conducting plane, it must then be determined if it is sufficiently well-connected to any reference potentials in the system, e.g. earth ground. Section 3.5 describes a method for controlling these ambiguities by iteratively comparing simulated results to experimental data. For now, the floor may simply be taken as another conducting node in the system.

3.2.2 Modeling the Source

Identifying a reasonable and useful model of the signal source is a key challenge in forming the lumped-element abstraction of the lamp sensor system. The signal source is derived from stray electric fields that couple from the ends and surfaces of the bulbs to the other conducting objects in the system.

First, the signal source should be qualified as either a voltage source (low impedance) or as a current source (high impedance). Consider the circuit model of a driven fluorescent bulb in Figure 3-2(a). Typically, a fluorescent bulb will be driven by a high-impedance (current) source as shown in Figure 3-2(a). Reference [89] argues a resistor model of a fluorescent lamp bulb excited at high frequency. Data taken from the fluorescent bulbs used in the experimental setup of Section 3.5 will confirm a bulb model with a resistance of approximately 1 kΩ (see Figure 3-22).



(a) A high-impedance source drives the bulb

(b) Loading impedances are small compared to the effective source impedance.

Figure 3-2: Capacitive loading impedances on the signal source are very large compared to the Thevenin resistance of the source.

With the resistor model of the bulb, the current source supports a potential difference between any two points along its length. In Figure 3-2(a), we take those points to divide the bulb equally into three pieces. The circuit in Figure 3-2(a) is re-drawn as its Thevenin equivalent in Figure 3-2(b). Typical operating bulb resistances vary between 100 and 10 kΩ [89] and the Thevenin resistance in Figure 3-2(b) is upper-bound by that value. Capacitances coupling directly to the source will be shown in simulation (Section 3.5) to have values ranging between 20 fF and 30 pF. At the ballast operating frequency, $f_c = 50$ kHz, those capacitances correspond to impedances ranging between 160 MΩ and 106 kΩ. The simplified picture depicted in Figure 3-2(b) therefore indicates loading impedances that are large compared to the effective source impedance. Therefore, the signal source is taken here as a voltage (low-impedance) source.

To develop a voltage-source element representation of the signal source, each bulb

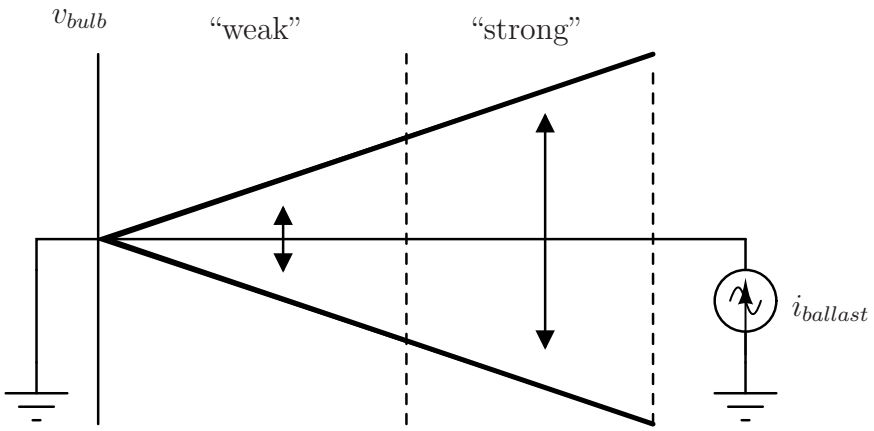


Figure 3-3: Alternating linear voltage profile of a resistive bulb.

must be lumped into at least two pieces and those pieces must be assigned corresponding (alternating) potentials. Figure 3-3 depicts the alternating linear voltage profile along the length of a driven resistive bulb. If the bulb is lumped into two halves, the half closer to the driven end may be called the "strong" half because the potentials in that piece vary a lot with respect to the undriven end (the ballast common). Then, the half closer to the undriven end may be called the "weak" half for obvious reasons. A corresponding lumped element model of a single driven fluorescent bulb is depicted in Figure 3-4. In Section 3.5, a capacitive model is evaluated in which the

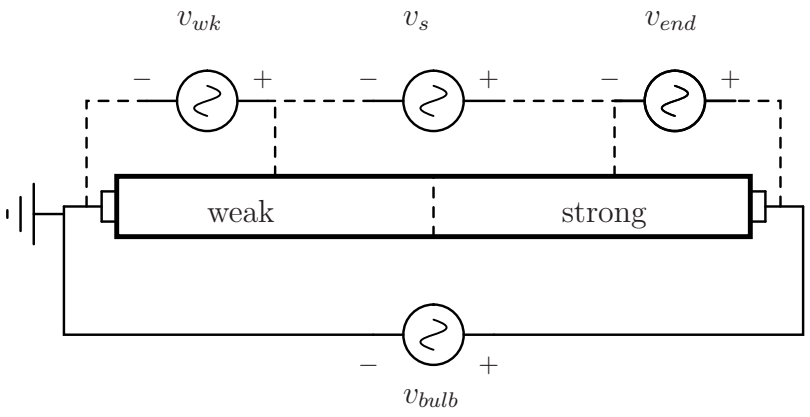


Figure 3-4: Two bulb halves comprise the lumped element model of a single bulb.

signal source derived from a two-bulb lamp is represented using two lumped-element models like the one shown in Figure 3-4.

3.2.3 Signal Source Reference

In this electrostatic system, it is important to establish conceptions of the reference potentials and surfaces that support current return paths as we develop lumped-element models of the system. Because the signal source itself is a conceived electrostatic model of driven fluorescent bulbs, the signal source reference potential and its physical location in the system is perhaps ambiguous. In the signal source model in Figure 3-4, the high potential end of the bulb (the strong node), may be taken as the conducting surface from which currents leave the source and the low potential end of the bulb (the weak node) may be taken as the surface which sinks those currents. Following this reasoning, we might choose to call the weak end of the bulb the "signal source reference." However, in practical configurations of the lamp, there may be more than one bulb so the location and potential of the signal source reference becomes muddied. Moreover there is no convenient way to electrically (ohmically) connect to the conceived model of the weak end of the bulb.

A more convenient choice for the signal source reference is the ballast common shown as a ground symbol in Figure 3-4 because a) it is separated from the weak node in the bulb model by a relatively small (alternating) potential difference and b) it is a physical node in a the ballast circuit that allows for explicit ohmic connections. Therefore, in this work, the ballast common is called the "signal source reference" and those two node names are used interchangeably. For example, when the signal source reference is said to be explicitly connected to the lamp sensor power supply ground, this means that the ballast common is connected (with a wire) to the ground on the power supply for the lamp sensor electronics.

3.2.4 Capacitive Models and Limitations

Having lumped all of the key elements in the system as conducting nodes that may or may not be driven to a particular potential, the electric field behavior may be captured by considering the capacitive coupling between those nodes. Proceeding along these lines, a circuit model of the relatively complicated system can be drawn.

The signal conditioning electronics can be taken to connect to that circuit at the electrode nodes and the system response can be determined by various means. An example of such a full system model is presented and evaluated in Section 3.5 using capacitance extraction software and a SPICE simulation.

Perhaps the primary limitation of the lumped element capacitive model originates in the modeling of the signal source. The electric field is related to the spatial derivative (gradient) of the corresponding scalar potential field, i.e. $\vec{E} = -\nabla\varphi$. When the bulb is lumped into two distinct halves and each half assigned a single potential, the variation of the actual potential along the length of those sections is neglected. Furthermore, abrupt changes are implicitly introduced in the potential at the ends of the bulb halves. The electric field corresponding to the lumped element model is inevitably an approximation of the actual electric field. Section 3.5 will show that the approximations inherent to the lumped-element model allow for acceptable prediction of the system behavior.

3.3 Implementation

Section 3.2 conceived a circuit model of the lamp sensor system. This section considers the design (and analysis) of a lamp sensor and appropriate signal conditioning circuitry informed by the conceptual developments in Section 3.2.

The lamp sensor design combines two key operating principles, carrier suppression and synchronous detection. Carrier suppression is achieved with a balanced or symmetrical excitation source and a differential measurement technique. Synchronous detection is achieved through multiplication of the measured signal with an in-phase reference signal. Figure 3-9 shows a simplified schematic of the implemented electronics. For a detailed schematic see Appendix A.1. Typical passive component values are shown in Table 3.1.

Table 3.1: Typical system parameters and passive components.

Parameter	Value
$R_{f1,2}$	10 MΩ
$C_{f1,2}$	7.5 pF
R_{f3}	200 kΩ
C_{f3}	660 pF
R_{lim}	20 Ω
R_{pu}	500 Ω
R_{lpf}	10 kΩ
C_{lpf}	150 pF
f_c	50 kHz

3.3.1 Carrier Suppression

The physical configuration of the lamp shown in Figure 3-5 includes two measurement electrodes spaced symmetrically about the center of the lamp. The electrical configuration shown in Figure 3-6 reverses the ballast connections to one of the two bulbs. The result is a symmetrical electric field source. Coupling this lamp and electrode configuration with a differential measurement yields a natural suppression of unneeded carrier content. This carrier suppression is important for detecting very small perturbations of the capacitive system caused by the occupant below the lamp.

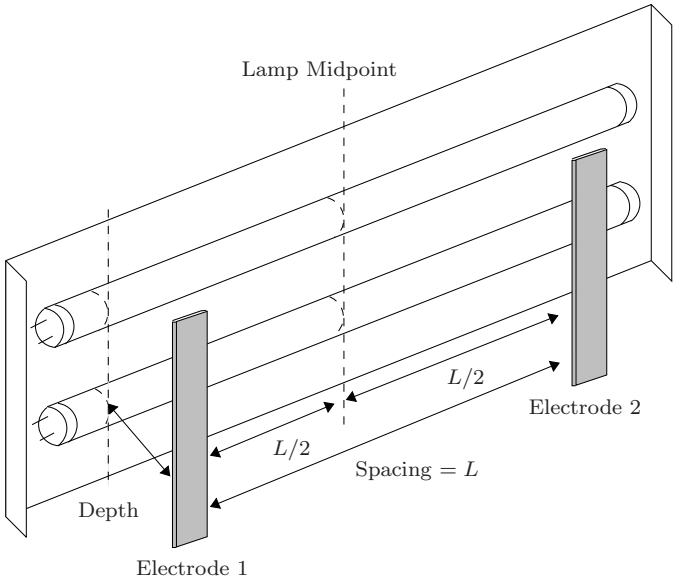


Figure 3-5: A diagram of the two-bulb fluorescent lamp and electrodes. The electrodes are spaced symmetrically about the center of the lamp.

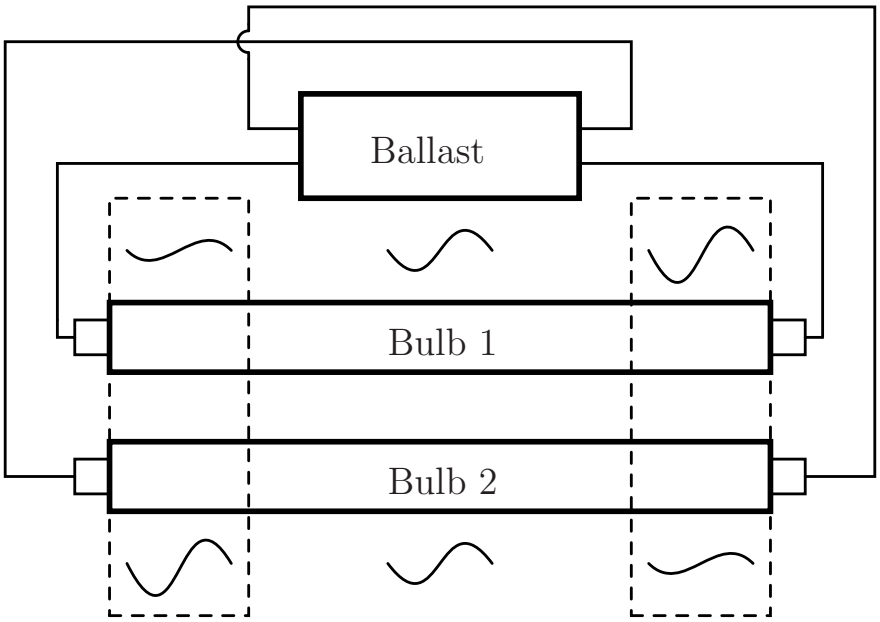


Figure 3-6: Reversing the connections to one bulb in a two-bulb lamp yields the desired symmetry in the electric field source.

A fully-differential transimpedance amplifier was used to achieve the needed carrier suppression. The analytical modeling effort in Chapter 2 supports the circuit model in Figure 3-7(b). Based on the analytical results in Chapter 2, the approximate circuit model parameters are as follows. The impedance elements are

$$Z_c = \left(\frac{\overline{Z_f}}{2}\right) \tag{3.13}$$

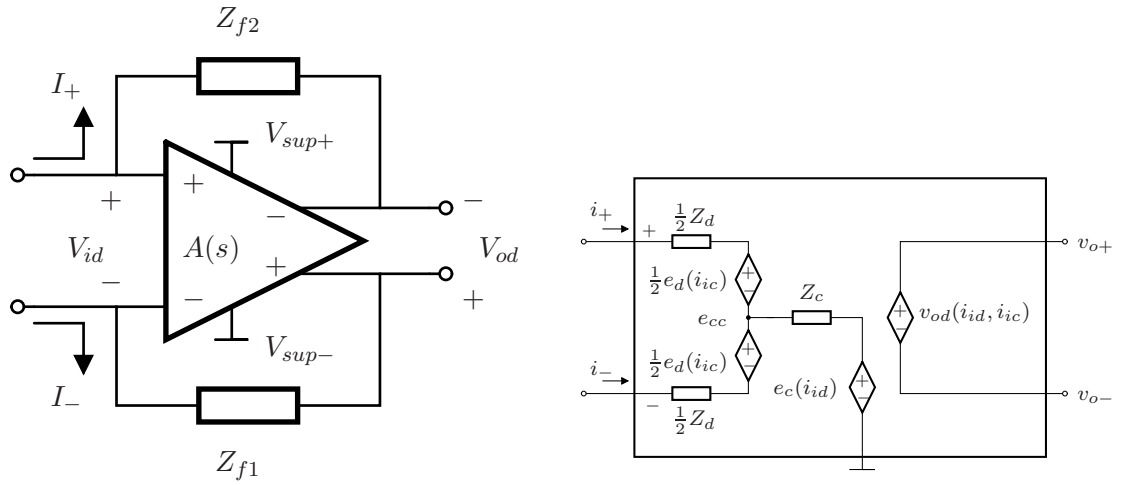
$$Z_d = \left(\frac{2\overline{Z_f} + \frac{1}{2}\Delta Z_f a_c}{(1+a_d)}\right) \tag{3.14}$$

and the dependent voltage sources as

$$e_c(i_{id}) = -i_{id}\left(\frac{\Delta Z_f}{2}\right) \tag{3.15}$$

$$e_d(i_{ic}) = i_{ic}\left(-\frac{\Delta Z_f}{2(1+a_d)} - \frac{\overline{Z_f}a_c}{2(1+a_d)}\right). \tag{3.16}$$

Notably, the model indicates a low impedance path for purely differential-mode input currents, i.e. a differential-mode virtual short-circuit between the input nodes of the amplifier. Accordingly, the fully-differential transimpedance amplifier may be



(a) A fully-differential transimpedance amplifier. (b) A small-signal T-model approximation.

Figure 3-7: A fully-differential transimpedance amplifier and its approximate small-signal model.

approximated as a short circuit between the measurement electrodes. Its output voltage is proportional to the current that flows through that short circuit according to (2.23). The circuit model in Figure 3-7(b) is validated as part of the full system model in Section 3.5.

3.3.2 Synchronous Detection

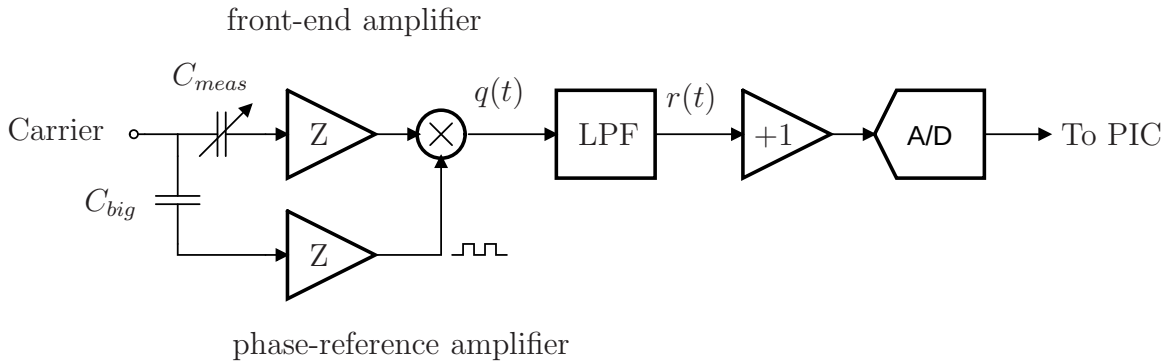


Figure 3-8: A block diagram of the signal conditioning system. Transimpedance amplifiers are marked with a 'Z'.

The block diagram in Figure 3-26 illustrates the synchronous detection scheme. The carrier signal is the high-frequency alternating signal source originating in the fluorescent lamp. Presence of the occupant in the detection field changes the amount

of capacitive coupling from the lamp to the electrodes and thus the amount of current input to the front-end. This modulation effect is represented in Figure 3-26 with a variable capacitor, C_{meas}. A copy of the (unmodulated) carrier signal is fed forward and multiplied with the output of the front-end amplifier. Multiplication by this phase reference achieves specificity in phase and frequency leading to a significant rejection of unwanted signals. A low-pass filter (LPF) attenuates the high-frequency residue after demodulation to yield the low-frequency modulations caused by the occupant below the lamp.

The synchronous detector primarily functions by multiplying the modulated signal with a phase reference signal as described above. In the implemented synchronous detector, a FD multiplier is controlled by the phase reference signal so that it inverts the incoming DM signal every half-cycle. A reasonable model for this effect is a multiplication of the modulated signal by a square wave with zero offset and unity amplitude. The demodulated signal can thus be written as a multiplication between the Fourier series decomposition of a square wave, and the incoming signal. The incoming signal may be comprised of a wanted portion with time-varying amplitude $A(t)$ at the carrier frequency, ω_c, and an unwanted portion with time-varying amplitude $E(t)$ at a different frequency, ω_e. The result is

$$q(t) = \frac{4}{\pi} \sum_{n,\ \text{odd}}^{\infty} \left(\frac{1}{n} \sin(\omega_{c,n} t + \phi_{c,n}) \times \left(A_n(t) \sin\left(\omega_{c,n} t\right) + E_n(t) \sin\left(\omega_{e,n} t\right) \right) \right), \quad (3.17)$$

for the n^{th} harmonic of the carrier frequency, $\omega_{c,n}$, where $\phi_{c,n}$ is the phase error between the front-end output and the reference signal at the carrier frequency. Using a trigonometric identity leads to a demodulated signal with a zero-frequency component whose magnitude decreases with $\phi_{c,n}$:

$$\begin{aligned} q(t) = & \\ & \frac{4}{\pi} \sum_{n,\ \text{odd}}^{\infty} \frac{1}{n} \frac{1}{2} A_n(t) \left(\cos \phi_{c,n} - \cos\left(2\omega_{c,n} t + \phi_{c,n}\right) \right) \\ & + \frac{1}{n} \frac{1}{2} E_n(t) \left(\cos\left(\omega_{c,n} t + \phi_{c,n} - \omega_{e,n} t\right) - \cos\left(\omega_{c,n} t + \phi_{c,n} + \omega_{e,n} t\right) \right). \end{aligned} \quad (3.18)$$

After low-pass filtering, the high-frequency content is stripped leaving,

$$r(t) = \frac{2}{\pi} \sum_{n=1,3,5...}^{\infty} \left(\frac{1}{n} A_n(t) \cos \phi_{c,n} + \frac{1}{n} E_n(t) \cos \left(\omega_{c,n} t + \phi_{c,n} - \omega_{e,n} t \right) \right). \tag{3.19}$$

Further, if the LPF bandwidth is narrower than the difference between the carrier frequency and the frequency of the unwanted signal, $(\omega_{c,n} - \omega_{e,n})$, then the unwanted signal $(E(t))$ is also stripped and the output becomes

$$r(t) = \frac{2}{\pi} \sum_{n=1,3,5...}^{\infty} \frac{1}{n} A_n(t) \cos \phi_n. \tag{3.20}$$

In our system, $A(t)$ is the amplitude of the DM output voltage from the front-end amplifier, $v_{od}(t)$. From Chapter 2, the DM output voltage might be approximated as $v_{od}(t) \approx 2\overline{Z}_f i_{id}(t)$, which has an amplitude, $A(t) = 2\overline{Z}_f I_{id}(t)$. Equation (3.20) can then be re-written in terms of the DM input current to the front-end amplifier:

$$r(t) = \frac{2}{\pi} \sum_{n=1,3,5...}^{\infty} \frac{1}{n} 2\overline{Z}_f I_{id,n}(t) \cos \phi_n. \tag{3.21}$$

Further, assuming a single frequency component, the output reduces to

$$\boxed{r(t) = \frac{4}{\pi} \overline{Z_f} I_{id}(t) \cos \phi}. \tag{3.22}$$

The phase specificity of the synchronous detector is evident in equation (3.22) and the frequency specificity was explicit in the analysis above.

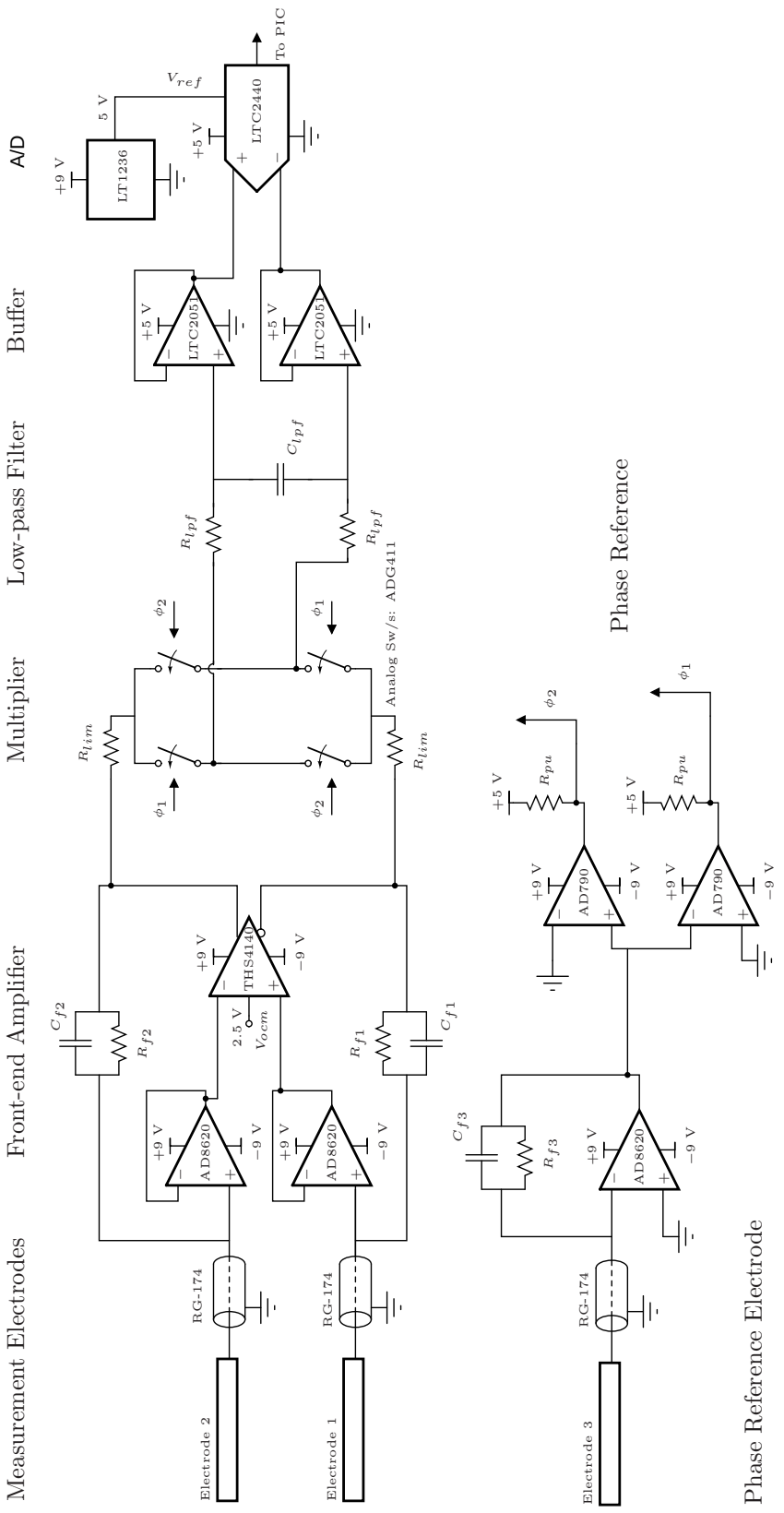


Figure 3-9: A simplified schematic of the fully-differential signal conditioning electronics

3.3.3 Front-end Amplifier

The front-end amplifier was implemented with a fully-differential op-amp in a closed-loop transimpedance configuration. The feedback components for the front-end were chosen to satisfy constraints in noise performance and closed-loop stability. The AD8620 op-amps shown in Figure 3-9 were chosen for their JFET input devices, which draw very little input bias current and input-referred current noise.

The developments regarding circuit models and analysis of the fully-differential transimpedance front-end amplifier from Chapter 2 are useful for modeling the system response to capacitive coupling changes in the detection field below the lamp and for understanding and assigning values to the distinct current paths supported by the amplifier. The virtual short-circuit approximation quantified in Chapter 2 has already been utilized as a basic operating principle concept in the current chapter (see Section 3.2). The circuit model of the front-end amplifier will be even more critical in the full system simulation later in this chapter (see Section 3.5) and also in the chapters that follow as it will inform the configuration of those systems. However, for the present task of gaining an understanding around the nominal amplifier stability and noise performance, a simplified analytical approach is used instead. Specifically, noise performance and stability are evaluated having assumed perfect symmetry among external homologous elements. Those assumptions will be apparent in the design-oriented analyses throughout this section.

Three main considerations led to the choice of feedback impedance components for the front-end amplifier including,

- Noise performance
- Closed-loop stability
- Phase-matching.

The transimpedance value should be large enough that the noise produced by the amplifier itself does not overwhelm amplified signals of interest. The value of the total impedance in the feedback network is equal to (half) of the nominal tran-

simpedance for the FD front-end based on equation (2.23). Therefore, either increasing $R_{f1,2}$ or decreasing $C_{f1,2}$ increases the transimpedance value. The values of the feedback impedance components themselves also influence the total amount of noise contributed by the front-end. Section 3.3.9 will show that noise embedded in the incoming signal currents dominates the total noise at the output of the sensor electronics implying that the implemented front-end is suitable in this regard. Because the JFET-input buffers (AD8620) require very little input bias current, a very large feedback resistor can be used. The transimpedance value at ballast operating frequencies is then typically upper-bound by practical values for $C_{f1,2}$ and in that case, the transimpedance becomes capacitive.

The components that make up the transimpedance, $R_{f1,2}$ and $C_{f1,2}$, should also result in a stable closed-loop configuration. Section 3.3.7 derives the loop transfer function and evaluates the stability of an implemented sensor front-end. Finally, the transimpedance should be chosen so that the phase of the front-end output, with respect to the ac signal source, is well-matched to that of the phase reference amplifier. Section 3.3.4 shows that the implemented front-end amplifier achieves a calculated phase error of about 1° and a corresponding multiplicative error factor of about 0.99. Refer to Table 3.1 for typical front-end feedback component values.

3.3.4 Phase-Reference Amplifier

The phase reference is measured with a SE transimpedance amplifier that is capacitively-coupled to the bulbs similar to the front-end amplifier. The phase reference electrode can be taped to the bulb or to the ballast wire. It can also be built into the ballast as a trace adjacent to the drive signal for the bulb or as an explicit capacitor coupling to the ballast drive signal. The output of the phase reference amplifier drives opposite inputs of two comparitors in order to generate two (barred and unbarred) control signals for the FD multiplier.

It is important to realize the implications of using a SE amplifier to measure the phase reference. Because the lamp sensor is a quasistatic system, every measured current must have a return path. If the power supply ground of the lamp sensor is

not explicitly connected to the signal source reference, the SE capacitively coupled measurement will rely on stray return paths. In practice, we have observed little or no measurable change in the behavior of the lamp sensor with or without an explicit connection (short-circuit) between the power supply ground and the signal source reference. This suggests that the stray coupling, although uncontrolled, is both significant and unavoidable.

Three main considerations led to the choice of feedback impedance components for the phase-reference amplifier including,

- Output Signal level
- Closed-loop stability
- Phase-matching.

The transimpedance value for the phase reference amplifier should be chosen so that, given the configuration of the phase reference electrode, the amplifier's output signal is well-behaved. That is, the output signal should be large enough to support good transitions in the comparators, but it should not saturate the output of the phase reference amplifier. Depending on the particular implementation of the phase reference electrode, the transimpedance value that satisfies this criterion is most easily found by experimentation. Stability considerations for choosing the transimpedance for the phase reference amplifier are addressed in Section 3.3.7.

The phase-reference amplifier's output should be well-matched in phase to the output of the front-end amplifier. From equation (2.23), the closed-loop frequency response of the FD transimpedance amplifier can be approximated with the transimpedance, $2\overline{Z_f}$. Similarly, the closed-loop response of the SE amplifier can be approximated by its feedback impedance value. Given the typical passive component values from Table 3.1 the magnitude and phase of the closed-loop response for the phase-reference amplifier is

$$|Z_{f3}| = 4.82 \text{ k}\Omega \tag{3.23}$$

$$\angle Z_{f3} = -88.6^\circ \tag{3.24}$$

and for the front-end amplifier,

$$|2\overline{Z_f}| = 424 \text{ k}\Omega \tag{3.25}$$

$$\angle 2\overline{Z_f} = -87.6^\circ. \tag{3.26}$$

Equations (3.24) and (3.26) show a phase error of $\phi = 1^\circ$ between the front-end and phase-reference amplifiers' closed-loop response at f_c. From equation (3.22), the multiplicative error factor corresponding to this phase error is

$$\eta = \cos\phi = \cos 1^\circ \approx 0.99985. \tag{3.27}$$

Because both the front-end and the phase-reference amplifiers are capacitively coupled to the signal source and because η is close to unity, the outputs of the two amplifiers should be well-matched in phase. Equations (3.24) and (3.26) also reveal that both transimpedances are largely capacitive at the signal frequency, f_c. Therefore, the phase between the *signal source voltage* originating in the lamp and the outputs of the two amplifiers should be nearly 0°.[1] Refer to Table 3.1 for typical phase-reference feedback component values.

3.3.5 Electrode Cable Shields

In this implementation of the lamp sensor, the electrodes are connected to the input nodes of the amplifiers with shielded coaxial cables connected to the lamp sensor power supply ground as shown in Figure 3-9. Those shields reduce coupling to the wires between the electrodes and the electronics. However, they also present a significant capacitance between the input nodes and power supply ground. That shield capacitance has different implications depending on the configuration of the lamp sensor system. For instance, if the power supply ground is well-connected or even coupled to the signal source reference, those shields may actually shunt some of the desired signal currents away from the amplifier. On the other hand, if the power

[1] or 180° depending on the implementation, e.g. inverting or non-inverting amplification.

supply ground and signal source reference are not well-connected, the shield capacitances should have a lesser impact on desired signal currents. In either case, the shield capacitances should be taken into account when enumerating the stray input capacitances at the input nodes of the amplifiers.

3.3.6 Stray Input Capacitances

There are some significant capacitances between the amplifier input nodes and power supply or incremental ground in the implementation of the lamp sensor presented here. These "stray input capacitances" largely consist of the coaxial shield capacitance from the electrode cables, the stray capacitance between PCB traces and the input capacitance of the AD8620 op-amps in the front-end amplifier. The total stray input capacitance was measured, using an LCR meter operating at 50 kHz, between the input node on the lamp sensor PCB connected to electrode 1 in Figure 3-9 and the lamp sensor's power supply ground.[2] For this measurement, the lamp sensor was powered off and the feedback passive components, R_{f1} and C_{f1}, were removed from the PCB. An electrode with a 48-inch `RG-174` electrode cable was attached to the input node of interest. Typical measured stray input capacitances depended on the particular PCB tested and they fell in the range:

$$120 \text{ pF} < C_{stray} < 165 \text{ pF}. \tag{3.28}$$

For the analysis and modeling in the rest of this work, the total stray capacitance is taken to be that measured for one particular PCB:

$$\boxed{C_{stray} = 159 \text{ pF}}. \tag{3.29}$$

For convenience, the stray input capacitances were assumed to be the same for both input nodes of the front-end amplifier and for the input node of the phase-reference amplifier.

[2]Either input node yielded about the same capacitance.

3.3.7 Transimpedance Amplifier Stability

The feedback impedances for the front-end and the phase-reference amplifiers are chosen with several considerations in mind. One key consideration is the closed-loop stability of those amplifiers. Therefore, the choice of feedback impedances comprises feedback compensation for both amplifiers.

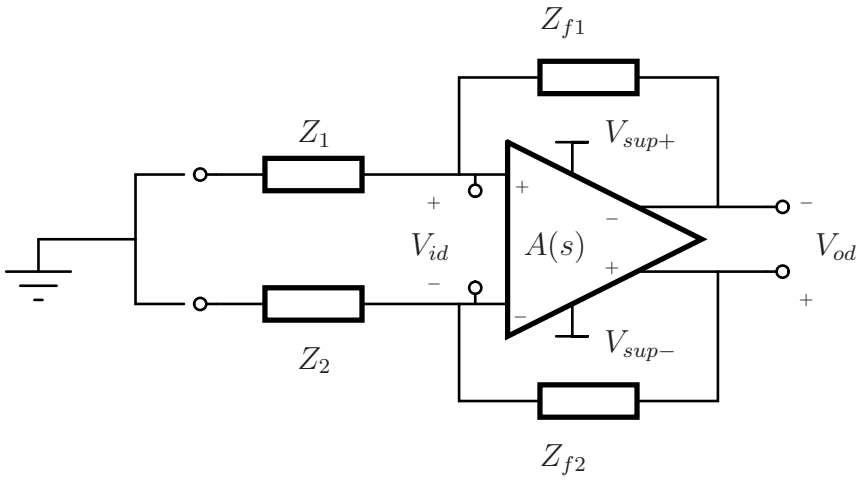


Figure 3-10: A circuit for calculating the loop transfer function in a FD amplifier.

Closed-loop stability is readily evaluated by analyzing the open-loop transfer functions ("loop transfer functions"). The loop transfer function for the front-end can be examined by analyzing the circuit of Figure 3-10. The analysis is simplified by assuming symmetry between homologous elements (e.g. $Z_{f1} = Z_{f2} = Z_f$ and $Z_1 = Z_2 = Z$). Assuming, that the CM feedback loop within the amplifier is stable, the output CM voltage is fixed. In that case, only the DM output voltage, v_{od}, varies. The DM output voltage is

$$v_{od} = a_d(s)v_{id} + a_c(s)v_{ic}, \tag{3.30}$$

for DM-DM op-amp gain, $a_d(s)$ and CM-DM op-amp gain, $a_c(s)$. If the amplifier in Figure 3-10 is symmetrical and the CM output voltage is fixed, the CM input voltage variation, v_{ic}, is zero volts. The DM output voltage reduces to

$$v_{od} = a_d(s)v_{id}. \tag{3.31}$$

Using a voltage divider relation, the amplifier's input voltages are

$$v_+ = v_{o-}\frac{Z_1}{Z_1 + Z_{f2}} \tag{3.32}$$

$$v_- = v_{o+}\frac{Z_2}{Z_2 + Z_{f1}}. \tag{3.33}$$

Symmetry yields,

$$\frac{Z_1}{Z_1 + Z_{f2}} = \frac{Z_2}{Z_2 + Z_{f1}} = \frac{Z}{Z + Z_f}, \tag{3.34}$$

Combining equations (3.32),(3.33) and (3.34) leads to

$$v_{id} = v_+ - v_- = -v_{od}\frac{Z}{Z + Z_f}. \tag{3.35}$$

Equations (3.31) and (3.35) describe the negative feedback between v_{od} and v_{id} in which the loop transfer function is

$$\boxed{L(s) = a_d(s)\frac{Z}{Z + Z_f}}. \tag{3.36}$$

The same result could be obtained using half-circuit analysis [56]. In fact, a half-circuit analytical approach highlights the manner in which the JFET-input buffers (AD8620) can be accounted for in the front-end implementation of Figure 3-9. Since there is one JFET-input buffer for each side of the circuit, the overall DM-DM op-amp gain for the front-end amplifier can be taken to be $a_d(s) \times H_j(s)$, where $H_j(s)$ is the closed-loop transfer function of one JFET-input buffer. This again assumes that the circuit is symmetrical, so that the two buffers are identical. More explicitly, if the DM-DM gain, of the op-amp is defined so that

$$v_{od} = v_{o+} - v_{o-} = a_d(s)(v_+ - v_-), \tag{3.37}$$

and $H_j(s)$ multiplies each of v_+ and v_- in the front-end of Figure 3-9, the argument

above follows directly from the commutative property in (3.37), i.e.

$$v_{od} = a_d(s)(H_J(s)v_+ - H_J(s)v_-) = a_d(s)H_J(s)(v_+ - v_-) \tag{3.38}$$

so that the effective DM-DM gain of open-loop front-end amplifier is simply

$$a_{d,eff}(s) = a_d(s)H_J(s). \tag{3.39}$$

The loop transfer function for the implemented front-end amplifier is therefore

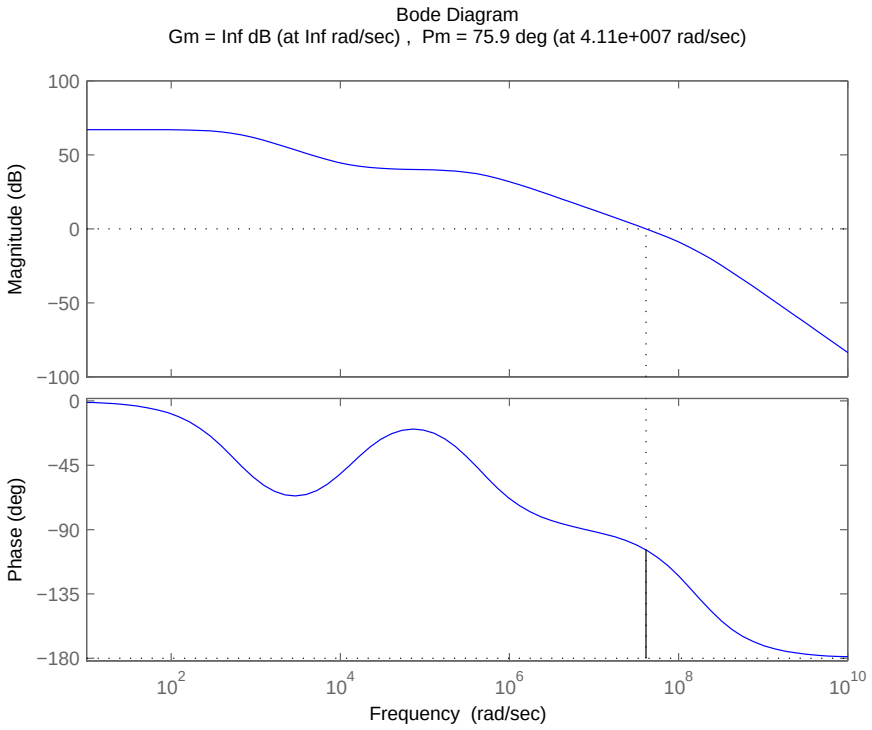
$$\boxed{L(s) = a_d(s)H_J(s)\frac{Z}{Z + Z_f}}. \tag{3.40}$$

A similar analysis leads to the loop transfer function for the (single-ended) phase-reference amplifier:

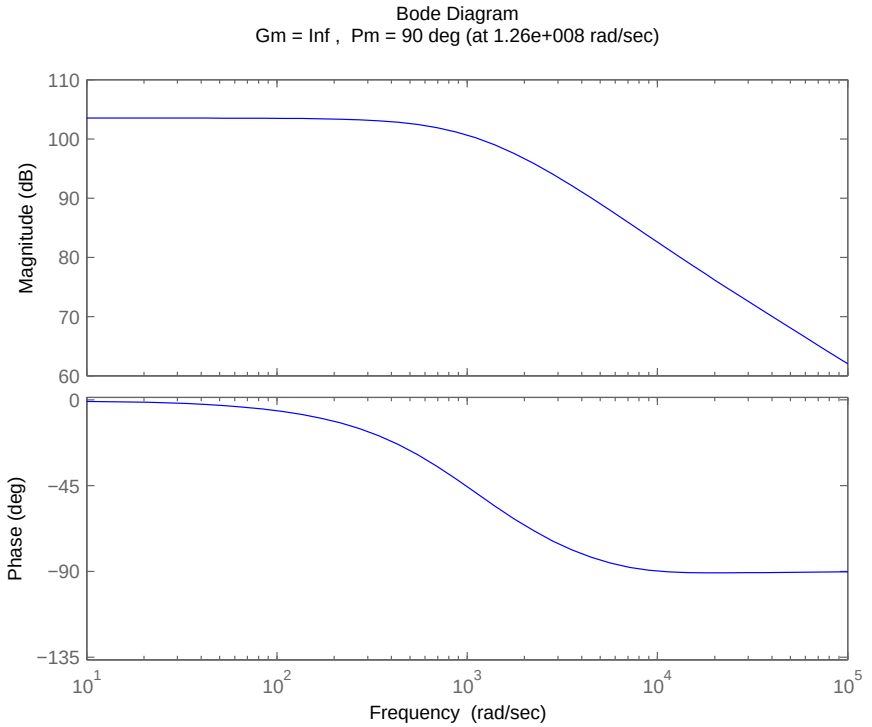
$$\boxed{L_p(s) = a_J(s)\frac{Z}{Z + Z_{f3}}}, \tag{3.41}$$

in which $a_J(s)$ is the DM voltage gain of the AD8620 op-amp, Z is the impedance between the op-amp inverting input and incremental ground and Z_{f3} is the value of the amplifier's feedback impedance, e.g. the parallel combination of R_{f3} and C_{f3} shown in Table 3.1.

Stray capacitances from the input nodes to ground enter into (3.40) and (3.41) because they appear in parallel with the input elements, e.g. Z_1 and Z_2 in Figure 3-10. Therefore, Z in (3.40) was taken to consist of the stray capacitance shown in equation (3.29). Increasing the stray capacitance at the input nodes decreases $|Z|$ and attenuates the loop-transfer function magnitude. In many cases, this effect will actually increase the stability of the closed-loop system.



(a) Front-end, P.M. = 75.9°



(b) Phase-reference, P.M. = 90°

Figure 3-11: Open-loop frequency responses showing suitable phase margin.

To evaluate the stability of both amplifiers, dominant pole models of the op-amp dynamics were extracted from the datasheets [90, 91]. Those model parameters are shown in Table 3.2. Finally, feedback impedances in this implementation were those

Table 3.2: Dominant Pole Models

Part	Parameter	Value
THS4140	GBW	2,238.7 Hz
[91]	Dominant Pole	67 kHz
AD8620	GBW	150 kHz
[90]	Dominant Pole	166 Hz

shown in Table 3.1. Bode plots of the corresponding loop transfer functions are shown in Figure 3-11. Both plots show good phase margin indicating suitable stability.

Closer examination of the loop-transfer functions reveals the manner in which the feedback compensation achieves closed-loop stability. The loop-transfer, $L(s)$, for the front-end can be re-written as

$$L(s) = a_d(s)H_J(s)\left(\frac{1 + R_f s C_f}{1 + R_f s(C_{in} + C_f)}\right), \tag{3.42}$$

where C_{in} is the total capacitance from the either input node to ground. With the dominant pole models, the gain terms $a_d(s)$ and $H_J(s)$ each contribute one pole but no zeros. The addition of R_f contributes one additional pole and the addition of C_f contributes one additional zero (consider equation (3.42) for $C_f = 0$). Therefore, $L(s)$ contains three poles and one zero. The uncompensated loop transfer function ($C_f = 0$ pF) would have been

$$L'(s) = a_d(s)H_J(s)\left(\frac{1}{1 + R_f s C_{in}}\right). \tag{3.43}$$

The uncompensated loop transfer function, $L'(s)$, contains three poles and no zeros. The bode plot corresponding to $L'(s)$ is shown in Figure 3-12. The uncompensated system shows a significantly reduced phase margin compared to Figure 3-11(a) and a non-infinite gain margin. The non-infinite gain margin reflects the fact that the number of poles exceeds the number of zeros by three or more, so the phase exceeds

-180° for some frequencies. Increasing the loop gain by the gain margin would result in instability. The instability in the uncompensated front-end amplifier arises from

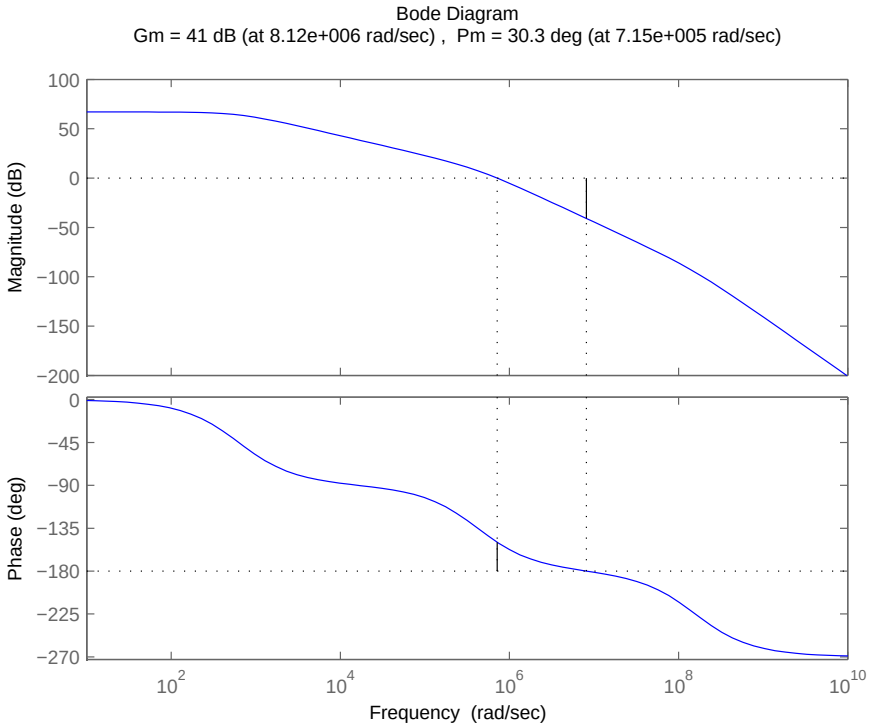


Figure 3-12: Bode plot of the loop transfer function for the uncompensated system ($C_f = 0$) showing poor phase margin.

the two-pole roll-off near the cross-over ($|L'(s)| = 0$ db) frequency. With the lack of a zero in the vicinity, the phase is allowed to approach -180° at cross-over, hence a poor phase margin. From (3.42) the feedback capacitance, C_f, adds a zero in the loop-transfer function in the vicinity of at least one of the poles. This significantly reduces the phase of the loop transfer function near cross-over thereby increasing the phase margin of the system. The addition of the parallel capacitance, C_f, in the feedback network is a form of lead compensation because it adds leading phase shift or positive phase to the output signal relative to the input signal at all frequencies [92].

3.3.8 Fully-differential Synchronous Detector

The electronics between the front-end and the ADC are fully-differential (FD) primarily because this eliminates the need for a differential-to-single-ended converter.

The FD signal chain also rejects CM pickup and power-supply disturbances.

The FD multiplier is implemented with a full-bridge of analog switches controlled according to the measured phase reference signal. The FD low-pass filter is implemented as an RC ladder and serves to attenuate the high-frequency residue left after demodulation. Because band-limiting effects in the final ADC are significant, the LPF may be viewed as an anti-aliasing filter while the majority of interpolation occurs in the ADC itself. A typical sampling rate for the ADC is 14 sps. Taking the corresponding Nyquist rate (7 Hz) as the low-pass bandwidth, the synchronous detector will largely reject unwanted signals whose frequency differs from that of the desired signal by more than 7 Hz. Given typical carrier frequencies near 50 kHz, the synchronous detector effectively achieves extremely aggressive bandlimiting of the incoming modulated signal.

Two chopper-stabilized op-amps buffer the output of the LPF. Those buffers present a high input impedance to the preceding LPF and a low-output impedance to the ensuing ADC. Therefore, inserting those buffers de-couples the frequency response design constraints of the LPF from the maximum source impedance constraints specified for the ADC [93].

3.3.9 Noise

The signal conditioning circuitry was designed to contribute less noise than the noise inherent in the measured signal. To evaluate the implemented design in this regard, the effects of individual noise sources originating in the electronics may be enumerated as follows.

A noise model of the front-end amplifier is shown in Figure 3-13(a) [41]. A small-signal noise model is shown in Figure 3-13(b).[3] The following analyses are simplified by assuming symmetry between homologous elements (e.g. $Z_{f1} = Z_{f2} = Z_f$ and $Z_1 = Z_2 = Z$).

[3]The notation here uses e to represent a noise voltage density with units $\mathrm{V}/\sqrt{\mathrm{Hz}}$ and v to represent voltages in the conventional sense.

3.3.10 Op-amp Input-referred Noise

The effect of each noise source on the DM output, e_{od}, can be evaluated separately with a superposition approach. For instance, to determine the effect of the THS4140 part's input-referred voltage noise, e_{nT}, the other voltage noise sources may be shorted and the current noise sources open-circuited. Defining e_{id} as the DM input noise voltage, e_{ic} as the CM input noise voltage, and e_{od} as the DM output noise voltage, a KVL loop around the amplifier dictates that

$$0 = e_{id} + e_{nT} + e_{od}, \tag{3.44}$$

which can be re-written based on the op-amp DM gain, a_d, and CM gain, a_c,

$$0 = e_{id} + e_{nT} + a_d e_{id} + a_c e_{ic}, \tag{3.45}$$

according to the equation $e_{od} = a_d e_{id} + a_c e_{ic}$. Collecting terms,

$$e_{id}(1 + a_d) + e_{ic} a_c + e_n = -e_{od}, \tag{3.46}$$

where e_{id} and e_{ic} can be found from their definitions as follows. Identifying terminal voltages, e_+ and e_-, the DM input noise voltage is

$$e_{id} \equiv e_+ - e_-, \tag{3.47}$$

which, under the assumption of perfect symmetry reduces as follows

$$e_{id} = -\frac{1}{2} e_{od} + e_{nT} - \frac{1}{2} e_{od} = e_{nT} - e_{od}. \tag{3.48}$$

Similarly, the CM input noise voltage is

$$e_{ic} \equiv \frac{e_+ + e_-}{2}, \tag{3.49}$$

which, reduces as follows

$$e_{ic} = \frac{-\frac{1}{2}e_{od} + e_{nT} + \frac{1}{2}e_{od}}{2} = \frac{e_{nT}}{2}. \tag{3.50}$$

Substituting the results for e_{id} and e_{ic} into (3.46) yields

$$(e_{nT} - e_{od})(1 + a_d) + \frac{e_{nT}}{2}a_c + e_{nT} = -e_{od}, \tag{3.51}$$

and simplifying leads to

$$e_{od} = e_{nT}\frac{1 + a_d}{a_d} + e_{nT}\frac{1 + \frac{a_c}{2}}{a_d}. \tag{3.52}$$

For most practical cases, a_d/a_c is large and e_{od} can be approximated as follows

$$e_{od} \approx e_{nT}\frac{1 + a_d}{a_d}, \tag{3.53}$$

which can be further approximated under the practical assumption that $a_d >> 1$ as follows

$$\boxed{e_{od,T}^2 \approx e_{nT}^2 \ \frac{\mathrm{V}^2}{\mathrm{Hz}}}. \tag{3.54}$$

The analysis of the e_{nJ} sources on e_{od} is equivalent except that there are two noise sources corresponding to the two AD8620 parts, so

$$\boxed{e_{od,eJ}^2 \approx 2e_{nJ}^2 \ \frac{\mathrm{V}^2}{\mathrm{Hz}}}. \tag{3.55}$$

The input-referred current noise sources are drawn only for the AD8620 parts. The input current noise from the THS4140 part multiplies the low output impedance of the JFET-input buffers and should contribute no significant noise voltage. A KVL loop can be written to account for each current noise from the AD8620 parts as follows:

$$0 = e_{id} - i_{nJ}Z_{f1} + e_{od}. \tag{3.56}$$

Equation (3.56) is similar to the expression in (3.45) except that the noise voltage, e_{nT}, has been replaced with the term $-i_{nJ}Z_{f1}$. Therefore, the same practical assumptions made in the analysis for e_{nT} apply here and the effect on e_{od} can be approximated as follows:

$$\boxed{e_{od,iJ}^2 \approx 2i_{nJ}^2 Z_f^2 \ \frac{\mathrm{V}^2}{\mathrm{Hz}}}, \tag{3.57}$$

where the factor of two accounts for the two separate current noise sources from the two AD8620 parts.

3.3.11 Feedback Resistor Noise

The feedback resistors can be modeled as noiseless resistors in parallel with current noise sources having a flat spectral density:

$$i_{nR_f}^2 = \frac{4kT}{R_f} \ \frac{\mathrm{A}^2}{\mathrm{Hz}}. \tag{3.58}$$

Multiplying the current noise from (3.58) with the feedback impedance, Z_f, yields a noise voltage across those feedback impedances

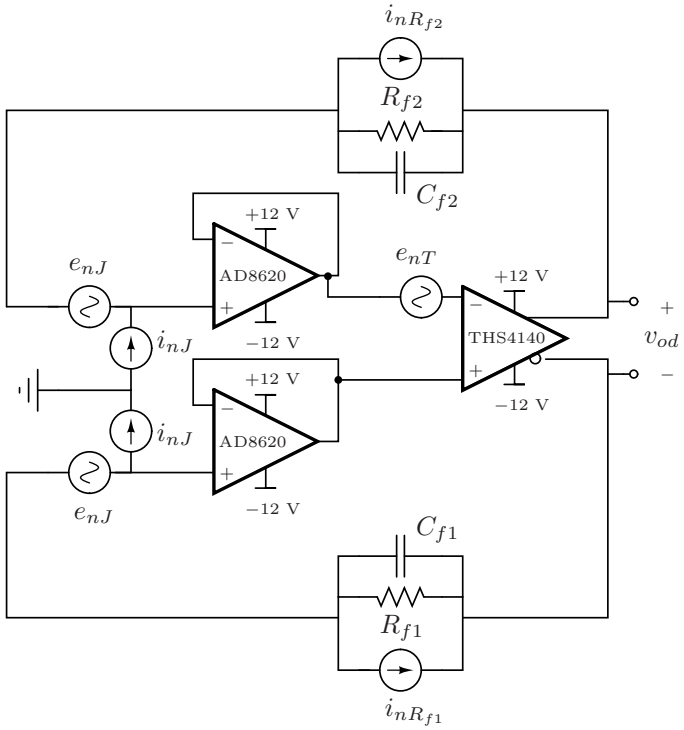
$$e_{nR_f}^2 = \frac{4kT}{R_f} Z_f^2 \ \frac{\mathrm{V}^2}{\mathrm{Hz}}. \tag{3.59}$$

An analysis similar to those for the op-amp input-referred noise sources above reveals that the contribution of the feedback resistor noise to the output of the front-end is

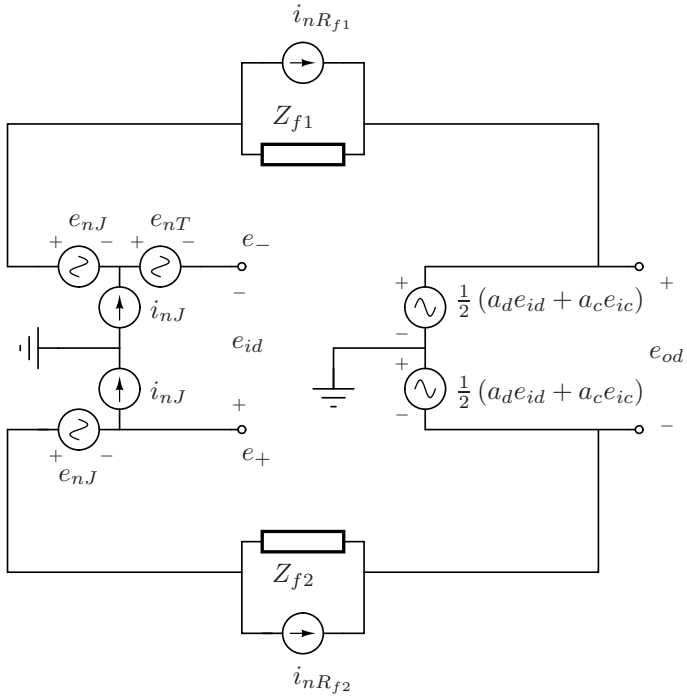
$$e_{od,R_f}^2 \approx 2e_{nR_f}^2, \tag{3.60}$$

which can be re-written

$$\boxed{e_{od,R_f}^2 \approx 2\frac{4kT}{R_f} Z_f^2 \ \frac{\mathrm{V}^2}{\mathrm{Hz}}}. \tag{3.61}$$



(a) Noise model of the front-end amplifier [41].



(b) Small-signal noise model of the front-end amplifier.

Figure 3-13: Noise in the front-end amplifier.

3.3.12 Total Narrowband Front-end Output Noise

The noise density at the output of the front-end amplifier is generally frequency-dependent. In particular equations (3.57), and (3.61) show that the noise density is a function of the complex feedback impedance value. For instance the power spectral density described by equation (3.61) is depicted in Figure 3-14. The synchronous

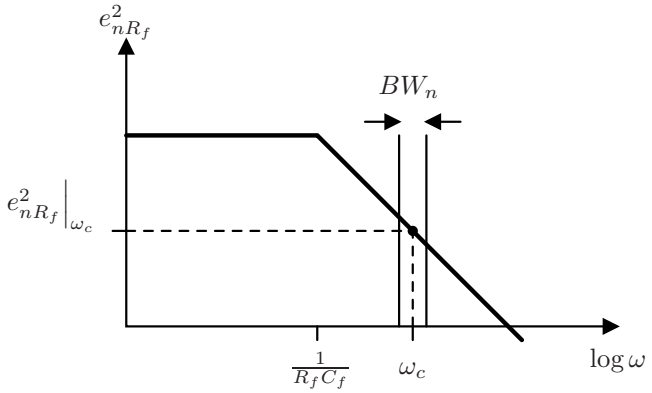


Figure 3-14: Power spectral density of noise voltage due to feedback resistors.

detector will isolate a narrow band of frequencies around the carrier frequency as suggested by Figure 3-14. In other words, the spectral density of the output noise voltage will be approximately flat over the frequency range $\omega_c \pm \frac{1}{2}BW_n$. This narrowband feature means that the value of the frequency-dependent noise contributions can be well-approximated by evaluating those quantities at a single frequency, ω_c. Therefore, in (3.57), and (3.61), Z_f may be approximated as $Z_f|_{\omega_c}$ so that those noise contributions become

$$e^2_{od,iJ} \approx 2i^2_{nJ}Z_f|^2_{\omega_c} \ \frac{\mathrm{V}^2}{\mathrm{Hz}} \tag{3.62}$$

$$e^2_{od,R_f} \approx 2\frac{4kT}{R_f}Z_f|^2_{\omega_c} \ \frac{\mathrm{V}^2}{\mathrm{Hz}}. \tag{3.63}$$

Finally, summing the power spectral densities for the various noise source contributions at the output of the front-end yields the front-end output noise density:

$$e^2_{n,amp} = e^2_{od,T} + e^2_{od,eJ} + e^2_{od,iJ} + e^2_{od,R_f} \ \frac{\mathrm{V}^2}{\mathrm{Hz}}. \tag{3.64}$$

Taking the square root in (3.64) and using equations (3.54), (3.55) and (3.63), the front-end output voltage noise density becomes

$$\boxed{e_{n,amp} = \sqrt{e_{nT}^2 + 2e_{nJ}^2 + 2i_{nJ}^2 Z_f|_{\omega_c}^2 + 2\frac{4kT}{R_f} Z_f|_{\omega_c}^2} \ \frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}}. \tag{3.65}$$

3.3.13 Noise in the Synchronous Detector

To see how the synchronous detector processes the noise from the front-end, it is necessary to consider the effect of the multiplier and the filtering that follows (Figure 3-26). To that end, we consider an in-phase and quadrature decomposition of a hypothetical noisy signal. According to [10], a noisy voltage signal, n, with spectral density N_o V^2/Hz in a frequency band centered on ω_i can be divided into two orthogonal components as follows:

$$n = n_x + n_y, \tag{3.66}$$

where the in-phase component is

$$n_x = x \sin \omega_i t \tag{3.67}$$

and the quadrature component is

$$n_y = y \cos \omega_i t. \tag{3.68}$$

The amplitudes, x and y, are random time functions each with flat spectral density N_o V^2/Hz. In analyzing the synchronous detector it is helpful to consider the noiseless signal of interest as well [10]. For instance, taking

$$v_i(t) = \sum_{j=1}^{\infty} V_{ij} \sin(\omega_{ij} t) \tag{3.69}$$

as the input signal of interest to the multiplier and adding it to the noise signal yields a phasor diagram like that in Figure 3-15 for j^{th} frequency component. The phasor diagram shows that n_x contributes amplitude noise while n_y contributes phase noise to the input signal [10]. The situation depicted in Figure 3-15 is described by the following equation:

$$v_{ij} + n_j = V_{ij} \sin(\omega_{ij} t) + x_j \sin(\omega_{ij} t) + y_j \cos(\omega_{ij} t). \tag{3.70}$$

The synchronous detector isolates the in-phase part of this noisy signal, $V_{ij} \sin(\omega_{ij} t) + x_j \sin(\omega_{ij} t)$, leaving out the phase-noise contribution in $y_j \cos(\omega_{ij} t)$. After low-pass filtering, the output of the synchronous detector including both noise and the signal of interest is

$$r(t) = \frac{2}{\pi} \sum_{j,\text{odd}}^{\infty} \frac{1}{j} V_{ij} + \frac{2}{\pi} \sqrt{\sum_{j,\text{odd}}^{\infty} (\frac{1}{j} x_j)^2} \sqrt{BW_n}. \tag{3.71}$$

For simplicity, it is assumed that only the noise surrounding the fundamental frequency is significant after demodulation. The contributions from the higher harmonic terms are attenuated as $1/j$ for $j = 1, 3, 5...$ in addition to the natural band-limiting in the system. In an rms-sum, the noise contributions from the higher harmonic terms quickly become insignificant. From (3.71), the total rms noise voltage from the front-end amplifier at the output of the synchronous detector is approximately,

$$v_{n,amp} \approx \frac{2}{\pi} e_{n,amp} \sqrt{BW_n}. \tag{3.72}$$

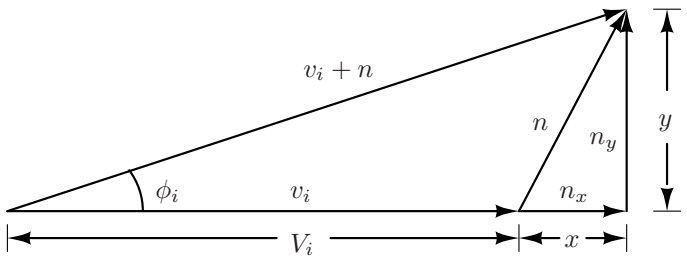


Figure 3-15: Phasor diagram for additive noise [10].

3.3.14 Total Noise at the ADC Input

Combining (3.72) with (3.65) yields the total noise voltage contribution of the front-end amplifier at the ADC input (the output of the synchronous detector):

$$\boxed{v_{n,amp} \approx \frac{2}{\pi}\sqrt{\left(e_{nT}^2 + 2e_{nJ}^2 + 2i_{nJ}^2 Z_f|_{\omega_c}^2 + 2\frac{4kT}{R_f}Z_f|_{\omega_c}^2\right) BW_n}\ \mathrm{V}_{rms}}. \tag{3.73}$$

The noise bandwidth, BW_n, is ultimately determined by the ADC, assuming the LPF is a suitable anti-aliasing filter. For a typical sampling rate of 13.75 Hz, BW_n, for the LTC2440 part is 12.4 Hz [93]. Using the datasheets for the THS4140 and AD8620, the individual noise densities are as follows [90,91]. The THS4140 part input-referred voltage noise density is

$$e_{nT} = 6.5\ \frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}} \tag{3.74}$$

The AD8620 input-referred voltage and current noise densities are, respectively,

$$e_{nJ} = 6\ \frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}} \tag{3.75}$$

$$i_{nJ} = 5\ \frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}}. \tag{3.76}$$

Using these values along with the passive component values from Table 3.1 and a nominal room temperature of $T = 300$ K in equation (3.73) yields the total noise voltage from the front-end at the output of the synchronous detector:

$$\boxed{v_{n,amp} = 60\ \mathrm{nV}_{rms}}. \tag{3.77}$$

in a frequency band from 0.1 to 12.4 Hz. Note that if the inputs to the THS4140 part were left unbuffered, its much more significant input current noise of 1.25 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ would develop a noise voltage contribution of 2.8×10^{-13} V^2/Hz, several orders of magnitude larger than the current noise term contributed by the JFET-input buffers. In addition to the front-end, significant noise sources originate in the buffers that follow the LPF and in the ADC. The noise sources at the ADC input for the entire

signal conditioning chain are enumerated as follows [93, 94]. The noise contribution from the front-end amplifier is

$$v_{n,amp} = 60 \text{ nV}_{rms} \tag{3.78}$$

in a frequency band from 0.1 to 12.4 Hz. The noise contribution from the buffer op-amps is

$$v_{n,buff} = 1.5 \ \mu\text{V}_{p-p}, \text{ typical in } 0.1 - 10 \text{ Hz} \tag{3.79}$$

and the noise contribution from the ADC is

$$v_{n,AD} = 250 \text{ nV}_{rms}, \tag{3.80}$$

also in a frequency band from 0.1 to 12.4 Hz. From (3.78)-(3.80), the dominant noise source originates in the buffers that precede the ADC inputs. Therefore, the front-end is suitably low-noise in the sense that it is *not* the dominant noise source.

3.3.15 The Effect of Stray Input Capacitance on Noise

Section 3.3.6 discussed significant stray capacitances at the input nodes to the front-end amplifier in a practical implementation. This section considers the effect of the those stray capacitances on the noise contribution of the front-end amplifier. Figure 3-16 shows a noise model of the front-end amplifier having added the stray input capacitances to power supply or incremental ground. In analyzing the circuit of Figure 3-16(b), it is convenient to use the following approximations

$$Z_1 = Z_2 = Z \tag{3.81}$$

$$Z_{f1} = Z_{f2} = Z_f, \tag{3.82}$$

as in the analyses above. It is helpful to take the following additional approximations

$$v_{od} \approx a_d v_{id} \tag{3.83}$$

$$v_{od} \approx 2 Z_f i_{id} \tag{3.84}$$

where (3.83) approximates the CM-DM gain, a_c, of the fully-differential amplifier to be zero and (3.84) is the fully-ideal DM output voltage from the analysis of the FD transimpedance amplifier in Chapter 2. Analyzing the circuit in Figure 3-16(b) leads to the following front-end output noise densities. The noise density contribution from the THS4140 part itself is

$$e_{od,T}^2 \approx e_{nT}^2 \left(\frac{Z_f}{Z} \right)^2. \tag{3.85}$$

The noise density contribution from the AD8620 input-referred voltage noise is

$$e_{od,eJ}^2 \approx 2 e_{nJ}^2 \left(\frac{Z_f}{Z} \right)^2 \tag{3.86}$$

and the noise density contribution from the AD8620 input-referred current noise is

$$e_{od,iJ}^2 \approx 2 i_{nJ}^2 Z_f^2. \tag{3.87}$$

Finally, the noise contribution from the feedback resistors is

$$e_{od,R_f}^2 \approx 2 \frac{4kT}{R_f} Z_f^2, \tag{3.88}$$

so that the total noise voltage contribution of the front-end amplifier at the ADC input (the output of the synchronous detector) becomes:

$$\boxed{v_{n,amp} \approx \frac{2}{\pi} \sqrt{\left(e_{nT}^2 \left(\frac{Z_f}{Z} \right)_{\omega_c}^2 + 2 e_{nJ}^2 \left(\frac{Z_f}{Z} \right)_{\omega_c}^2 + 2 i_{nJ}^2 |Z_f|_{\omega_c}^2 + 2 \frac{4kT}{R_f} |Z_f|_{\omega_c}^2 \right) BW_n} \ \mathrm{V}_{rms}}. \tag{3.89}$$

where we have taken the values of Z_f and Z at the carrier frequency, ω_c, e.g. $Z_f \approx Z_f|_{\omega_c}$ because the synchronous detector output is narrowband. Equations (3.85)-

(3.88) reveal that the contributions of the current noise sources to the output of the front-end are approximately unchanged. On the other hand, the input-referred voltage noise sources from the op-amps are gained by a factor $\frac{Z_f}{Z}$. For the typical stray capacitance from Section 3.3.6 and the passive component values in Table 3.1, the magnitude of the factor $\frac{Z_f}{Z}$ at ω_c is approximately

$$\sqrt{\frac{Z_f^2}{Z^2}}\bigg|_{\omega_c} \approx 21. \tag{3.90}$$

With this gain factor, the total noise voltage from the front-end at the output of the synchronous detector (compare to equation (3.77)) becomes

$$\boxed{v_{n,amp} \approx 500 \text{ nV}_{rms}}. \tag{3.91}$$

The addition of stray capacitances at the input nodes caused the noise voltage sources to be gained to the output while the effect of the current noise sources remained approximately the same. The result was a significant degradation of the front-end amplifier noise performance. The significant noise contributions at the ADC input upon addition of the stray input capacitances are enumerated as follows. The noise contribution from the front-end amplifier is

$$v_{n,amp} = 500 \text{ nV}_{rms} \tag{3.92}$$

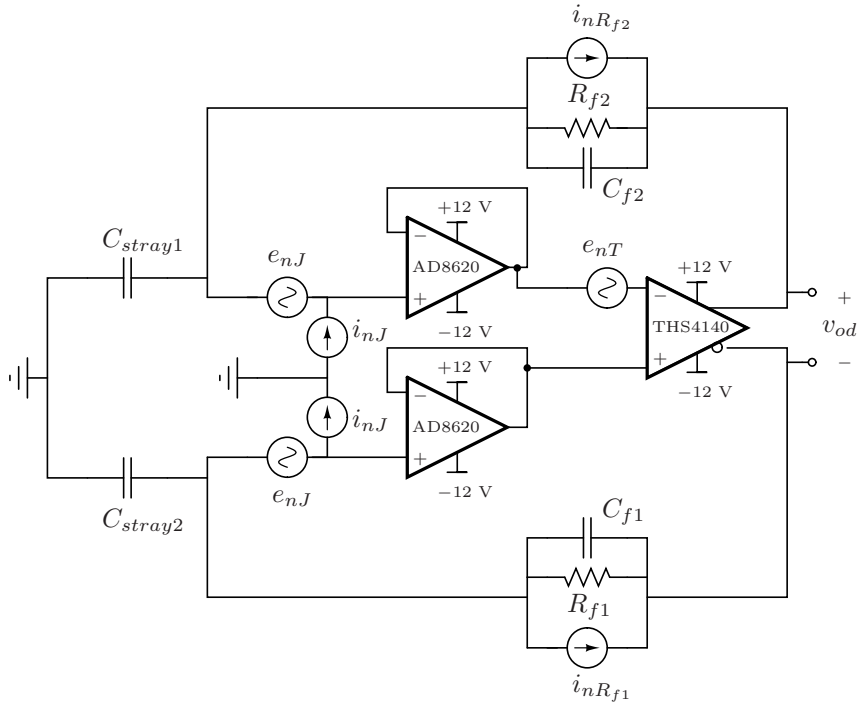
in a frequency band from 0.1 to 12.4 Hz. The noise contribution from the buffer op-amps is

$$v_{n,buff} = 1.5 \ \mu\text{V}_{p-p}, \text{ typical in } 0.1 - 10 \text{ Hz} \tag{3.93}$$

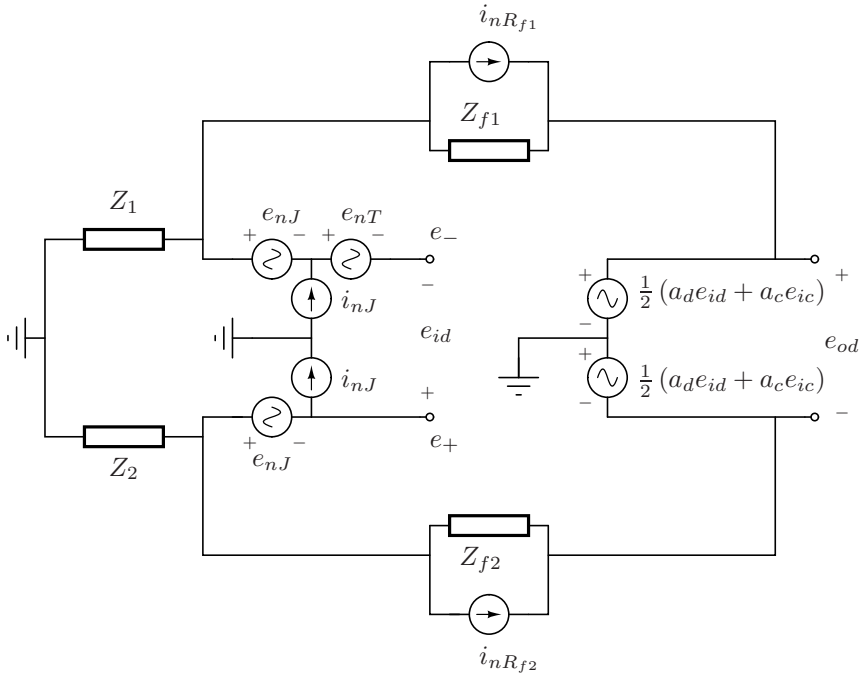
and the noise contribution from the ADC is

$$v_{n,AD} = 250 \text{ nV}_{rms}. \tag{3.94}$$

also in a frequency band from 0.1 to 12.4 Hz. From (3.92)-(3.94), the front-end is suitably low-noise in the sense that it is still *not* the dominant noise source.



(a) Noise model of the front-end amplifier [41].

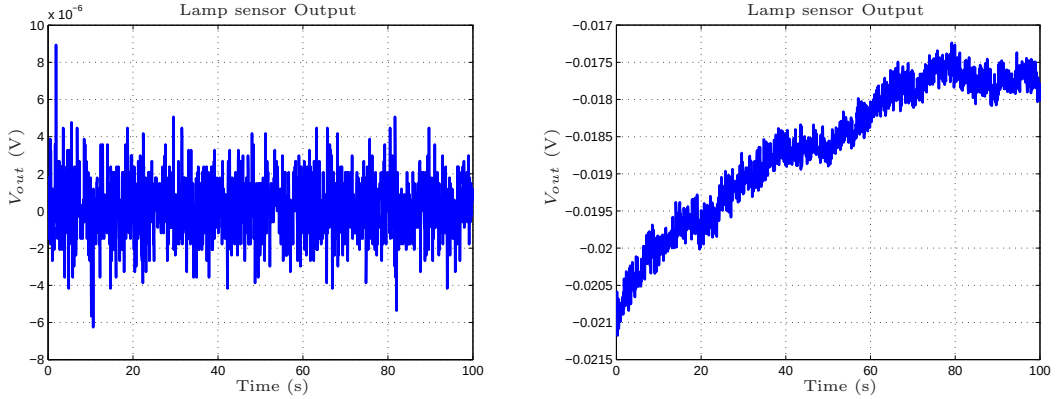


(b) Small-signal noise model of the front-end amplifier.

Figure 3-16: Noise in the front-end amplifier with stray input capacitances.

3.3.16 Time-domain Noise Data

Whether or not the electronics as a whole are suitably low-noise depends on the noise content inherent in the measured signals. Time-domain plots of typical noise at the lamp sensor output are shown in Figure 3-17. Figure 3-17(a) shows data taken with electrode cables attached and with the lamp turned off but with an artificial phase reference signal driving the demodulator at 50 kHz. The typical (windowed) noise level depicted in Figure 3-17(a) is 2.5 μV_{rms} and is reasonably consistent with the noise contributions listed in (3.92)-(3.88). Figure 3-17(b) shows time-domain noise data from the lamp sensor once the lamp has been turned on. Typical (windowed) noise levels for this case are 186 μV_{rms}. Comparing the noise in Figure 3-17(a) to that in Figure 3-17(b) reveals that the signal conditioning electronics contribute negligibly to the overall noise content. Therefore, the signal conditioning electronics are suitably low-noise. MATLAB® scripts for computing the time-domain windowed noise values can be found in Appendix A.3.



(a) Without Lamp: Avg. noise voltage in 10-sec window = 2.51 μV_{rms}

(b) With Lamp: Avg. noise voltage in 10-sec window = 186 μV_{rms}

Figure 3-17: Time-domain noise data taken from an experimental prototype lamp sensor.

3.4 Range Test

A cart-mounted system, shown in Figure 3-18, was constructed to collect data and to perform a range test using the lamp sensor. Examples of the output voltage

data collected from the cart-mounted lamp sensor during the range test are shown in Figure 3-19. Experimental setup parameters including passive component values for the sensor are shown in Table 3.3.

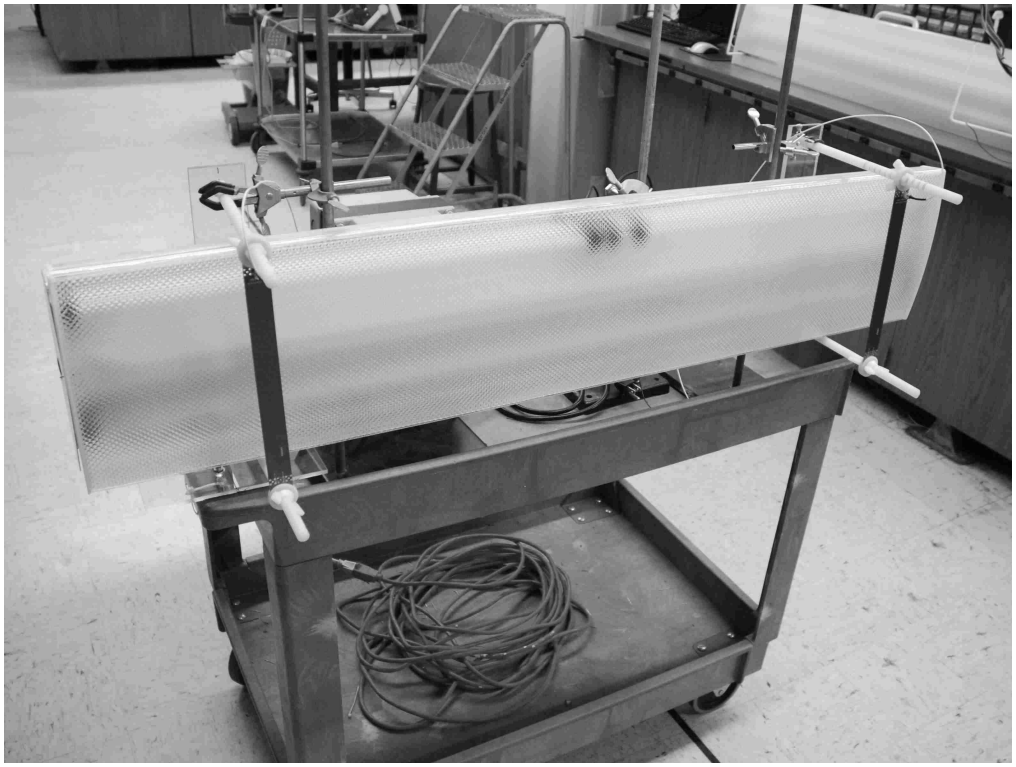


Figure 3-18: A photograph of the cart-mounted lamp experimental setup

Data was taken for 20 different electrode configurations. Each configuration consisted of an electrode spacing and depth as defined in Figure 3-5. Each sample consisted of one pass of a human target walking in front of the horizontally mounted lamp. The metric for each sample was the ac rms output voltage, $V_{ac,rms}$. For each configuration, 10 control samples (noise floor measurements) were taken with no target. Then, for each range in each electrode configuration, 5 samples were taken with a target person passing in front of the lamp. A Z-test in MATLAB® was performed on the data comparing each 5-sample data set for each range to the control data set for the corresponding electrode configuration. In our detection rule, the sample data sets had to demonstrate a mean $V_{ac,rms}$ larger than that of the control data sets with a confidence level of 99% or better. The resulting statistical data are shown in Table 3.4 at the boundary of the detection range. The range between the lamp and the

target varies along the columns. The electrode configuration varies along the rows.

Table 3.3: Range Test Experimental Setup Parameters.

Parameter	Note / Value
$R_{f1,2}$	1 MΩ
$C_{f1,2}$	1 pF
R_{f3}	80 kΩ
C_{f3}	30 pF
f_c	42 kHz
Phase Ref Elect.	Taped to bulb center
Earth, gnd, Common	Not explicitly connected

The Z-test measures the statistical likelihood that the means of two gaussian-distributed random variables are different based on the mean and variance calculated from sample sets of the two variables. The p-value quantifies the confidence level of detection where, p is the probability that the means of the two sample sets are equal. Thus a higher p-value indicates a higher probability that there is no detection. Therefore, the confidence level, α, that there has been a detection is defined as:

$$\alpha = 1 - p. \tag{3.95}$$

For example the percent confidence for the 10 foot range in the configuration with the electrodes two inches from the lamp and 28 inches apart (2x28) is

$$PC = 100(1 - p) = 100\%(1 - 0.027) = 97.3\% \tag{3.96}$$

and it is rejected as a detection based on the 99% confidence level rule.

For each configuration in Table 3.4, the p-values for the data straddling the detection range are highlighted. The highlighted data therefore indicate the detection range for each configuration. From Table 3.4, it appears that the detection range varies with the electrode configuration. Considering the differential measurement between the two electrodes, it is intuitive that the sensitivity to the target should increase as the spacing between the electrodes increases. It is also intuitive that the sensitivity to the target should increase as the depth of the electrodes increases (as the

Table 3.4: Detection Data $p-values$ for Various Electrode Configurations at the Limit of the Detection Range.

Spacing(in.)	Depth(in.)	p-values 7ft.	8ft.	9ft.	10ft.	11ft.	Noise Floor ($\mu V_{ac,rms}$)
44	5	0	0	0	2.53×10^{-4}	0.328	54.5
	4	0	0	4.63×10^{-7}	0.0165	N/A	65.1
	3	0	0	0	4.85×10^{-6}	0.661	98.9
	2	0	$< 10^{-7}$	0.0426	N/A	N/A	168.5
38	5	0	0	3.05×10^{-5}	0.0240	N/A	61.8
	4	0	0	4.93×10^{-5}	0.865	N/A	67.3
	3	0	0	$< 10^{-7}$	0.133	N/A	62.7
	2	0	0	0.00200	0.0160	N/A	74.0
28	5	0	0	0	$< 10^{-7}$	0.306	45.2
	4	0	0	1.19×10^{-4}	0.676	N/A	70.7
	3	0	0	$< 10^{-7}$	0.884	N/A	52.3
	2	0	2.62×10^{-5}	0.00100	0.0270	N/A	65.3
19	5	0	$< 10^{-7}$	0.382	N/A	N/A	55.4
	4	0	0	$< 10^{-7}$	0.126	N/A	41.6
	3	0	$< 10^{-7}$	0.0120	N/A	N/A	45.4
	2	0	0	1.01×10^{-5}	0.0340	N/A	42.2
15	5	0	$< 10^{-7}$	0.0360	N/A	N/A	40.9
	4	$< 10^{-7}$	0.0210	N/A	N/A	N/A	51.5
	3	0	$< 10^{-7}$	0.0640	N/A	N/A	49.9
	2	$< 10^{-7}$	0.0120	N/A	N/A	N/A	57.2

electrodes are moved closer to the target). The trend of the detection range evident in Table 3.4, matches our intuition about how the detection range should be affected by the electrode configuration.

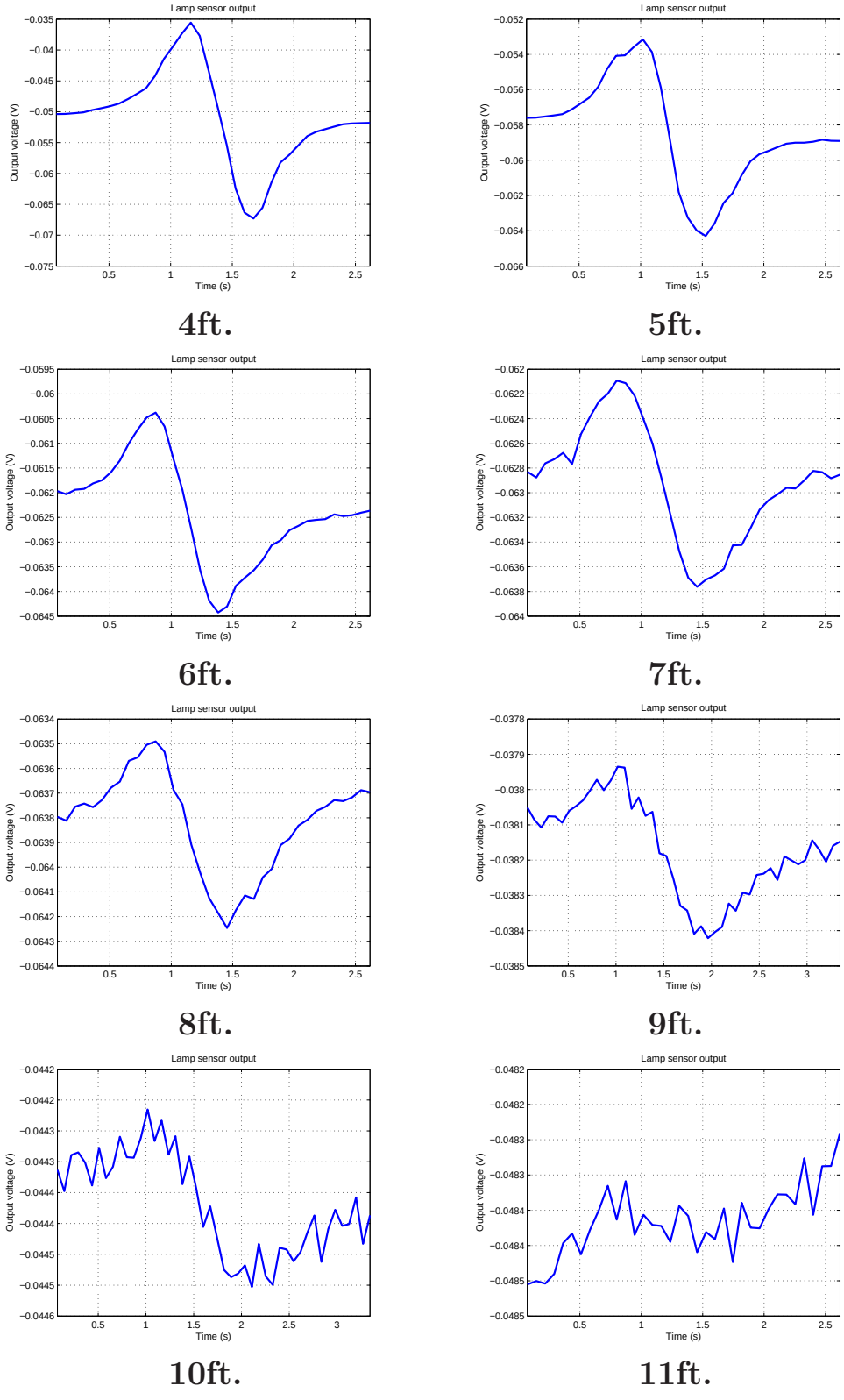


Figure 3-19: Examples of plots of sample detections from the range test. (Configuration 44x5)

3.5 Full System Model

This section presents and evaluates a SPICE model of the lamp sensor system including a lumped element capacitive model. A depiction of the model implemented in LTSPICE® is shown in Figure 3-25.

3.5.1 SPICE Model

The SPICE simulation (Figure 3-25) includes a lumped element capacitive model like the one described in Section 3.2, a circuit model of the front-end amplifier taken from Chapter 2, and a model of the entire signal processing chain described in Section 3.3. The netlist for the front-end amplifier can be found in Appendix A.4.2. The remaining SPICE parameters can be found in Appendix A.4.3 and example capacitance values can be found in Appendix A.4.4. With these components, the output voltage of the synchronous detector, corresponding to equation (3.22), can be read directly from the simulated results. The SPICE model can be used to validate the capacitive model and the model of the electronics including the front-end amplifier model developed in Chapter 2.

Phase Accounting

By accounting for the phase contributions in SPICE, the simulation is expected to yield the correct polarity of the output voltage. The phase reference in the SPICE simulation includes an additional 270° phase lag to account for the inversion in the phase reference amplifier and the 90° phase contribution from the front-end amplifier, not accounted for by the front-end SPICE circuit model.[4] The ADG411 analog switches shown in Figure 3-9 are active-low. This was accounted for in the SPICE simulation by controlling the simulated switches with logically-inverted ("barred") versions of the control signals from the comparators.

[4]The 90° phase contribution is due to the capacitive feedback elements in the real sensor front-end. For simplicity, in the SPICE model, we take the entire feedback network to be purely real with a resistance equal to the magnitude of the impedance of the actual feedback network.

3.5.2 Capacitive Model

The intent of the capacitive modeling approach in this section is to build the model by considering all of the capacitances between all of the conducting nodes in the system. Each conducting node is initially taken to be floating. Depending on the configuration of the system or on measurements taken from the experimental setup, some of those nodes may then be modeled as driven to a particular potential.

FastCap® - Capacitance Extraction

A capacitance extraction software, FastCap®, was used to determine the lumped element capacitance values to insert into the SPICE simulation [95]. A screenshot of the 3D model built for this purpose is shown in Figure 3-20. In the 3D model, one can see the floor at the bottom, the human target on the left and the fluorsecent lamp and electrodes (lamp sensor) above the center of the floor. Also included in the model are other unmovable conducting objects such as a large cabinet on the left, as well as overhead pipes, other lamps, a large duct and a power strip case that appears at waist level. The 3D model in Figure 3-20 corresponds to the photograph of the experimental setup in Figure 3-23(b).

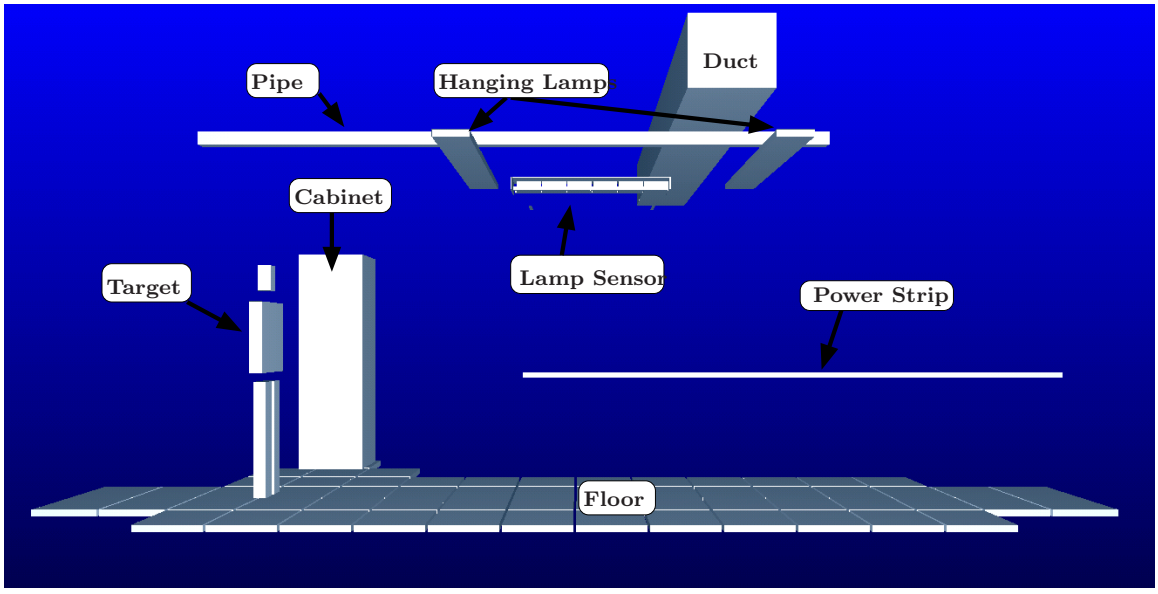


Figure 3-20: A screenshot of the FastCap® 3D model

For each simulation, FastCap® generated an output matrix like the one shown in Figure 3-21. The output matrices contained the values of the capacitances between each conductor in the system. For instance, the matrix element at row 5, column 8, corresponded to the net capacitance between conductor 5 (the left electrode) and conductor 8 (the target).[5]

CAPACITANCE MATRIX, femtofarads

		1	2	3	4	5	6	7	8	9	10
1%GROUP1	1	3.295e+004	-39.1	-122.9	-1623	-470.8	-25.47	-2.993e+004	-299.7	-39.45	-221.7
1%GROUP2	2	-39.1	3.304e+004	-1617	-126.5	-25.68	-455.5	-3.021e+004	-167.4	-56.4	-209.2
1%GROUP3	3	-122.9	-1617	3.296e+004	-39.19	-469.7	-24.75	-3.002e+004	-291.4	-65.85	-179
1%GROUP4	4	-1623	-126.5	-39.19	3.302e+004	-26.19	-456.3	-3.011e+004	-175.5	-47.29	-252.8
1%GROUP5	5	-470.8	-25.68	-469.7	-26.19	4860	-15.86	-2861	-536.9	-74.87	-224
1%GROUP6	6	-25.47	-455.5	-24.75	-456.3	-15.86	4843	-3127	-187.2	-43.94	-328.7
1%GROUP7	7	-2.993e+004	-3.021e+004	-3.002e+004	-3.011e+004	-2861	-3127	3.479e+005	-1.43e+004	-1.906e+004	-7.6e+004
1%GROUP8	8	-299.7	-167.4	-291.4	-175.5	-536.9	-187.2	-1.43e+004	6.776e+004	-2511	-4.538e+004
1%GROUP9	9	-39.45	-56.4	-65.85	-47.29	-74.87	-43.94	-1.906e+004	-2511	1.656e+005	-1.227e+005
1%GROUP10	10	-221.7	-209.2	-179	-252.8	-224	-328.7	-7.6e+004	-4.538e+004	-1.227e+005	3.633e+005

Figure 3-21: An example FastCap® output matrix

Typical simulated capacitances are shown in Table 3.5. Those capacitances represent the simulation of the target under the left edge of the lamp in Figure 3-20 with the lamp at a height of 2.43 m. Several capacitances in simulation are taken to be fixed as the target moves under the lamp ("Assumed Fixed") while only a few are taken to vary while the target moves ("Vary with Target"). When the target passes directly below the center of the lamp, many capacitances can also be assumed from symmetry.

Simulating the Floor

Section 3.2, discussed the ambiguity concerning the correct model of the floor below the lamp. The floor in the experimental setup was a tile floor on top of a concrete slab of unknown construction. Two key questions arise: 1) is the floor is well-represented by a conducting plane? and 2) if it is well-represented by a conducting plane, is it well-connected to reference potentials in the system, e.g. earth ground? To control these ambiguities, data from simulation was compared to data from the experimental system with and without an artificial conducting floor made of aluminum foil. The

[5]According to the Maxwell capacitance matrix format, mutual capacitances (off-diagonal elements) are reported as the negative of their actual value while diagonal elements are reported as positive values. If the capacitance matrix has non-negative off diagonals, we expect that there has been a problem with the extraction of the capacitance values [95].

Table 3.5: Typical Simulated Capacitances (shown for a target positioned under the left end of the lamp sensor depicted in Figures 3-20 and 3-23(b)).

Capacitance	Value	Notes
		Vary with Target
L. strong-Target	300 fF	
R. strong-Target	167 fF	
L. Electrode-Target	534 fF	
R. Electrode-Target	187 fF	
Backplane-Target	14.3 pF	
Cabinet-Target	2.5 pF	
		Assumed Fixed
L. strong-L. Electrode	477 fF	
L. strong-L. weak	126 fF	
L. strong-R. strong	41 fF	
L. strong-Cabinet	56 fF	
R. strong-Cabinet	62 fF	
L. weak-Cabinet	81 fF	
R. weak-Cabinet	53 fF	
L. Electrode-Cabinet	102 fF	
R. Electrode-Cabinet	52 fF	
Backplane-Cabinet	19 pF	
L. strong-R. Electrode	27 fF	
L. strong-Backplane	3 pF	
L. Electrode-Backplane	3.1 pF	
L. strong-R. weak	1.6 pF	
Floor-Backplane	79.7 pF	
Floor-Cabinet	121 pF	
Floor-L. strong	321 fF	
Floor-L. Electrode	401 fF	
Floor-Target	42.4 pF	"Shoe Capacitance"

artificial conducting floor was also connected and disconnected to or from the earth ground reference. Because little change was observed in the measured output from the experimental system among the three cases, it was speculated that the actual floor below the lamp was well-represented by an earthed conducting plane. In the SPICE model of Figure 3-25, this was implemented as a short circuit between the "earth" and "floor" nodes. In the FastCap® 3D model of Figure 3-20, this is manifested as a conducting plane below the lamp and the target.[6]

Having a conducting plane model of the floor, the effective depth of that con-

[6]Segmenting the floor plane into smaller panels, as shown in Figure 3-20, aided the FastCap simulator. In general, this method of breaking the conductors into pieces aided the simulation and was a practical necessity for getting the simulator to work properly. Common results yielded by a model without enough of this kind of granularity included "non-negative off-diagonals" and "failure to converge" errors as well as prohibitively long computation times.

ducting floor ("effective conducting floor depth") was also adjusted by comparing simulated and experimental data. To that end, a conducting plane was positioned in the FastCap® simulation some distance below the surface of the actual floor. That distance was determined empirically, by closely matching the peak deviation of simulated data taken from the SPICE simulation to the peak deviation of corresponding experimental data. The effective conducting floor depth was set using data with the lamp set at a height of 2.43 m and then held fixed for the other experiments. The final value of the effective conducting floor depth is shown in Table 3.6.

Simulating the Source

The capacitive model in Figure 3-25 includes a model of the signal source consistent with the developments in Section 3.2. That is, in the signal source model, each bulb consists of two nodes - "strong" and "weak". Because the model in Section 3.2 divides the bulb into two distinct pieces, it is necessary to assign each piece an alternating potential with respect to the signal source reference. Based on the alternating linear voltage profile of a single (resistive) bulb shown in Figure 3-3, it is convenient to assign the model parameters for the signal source model in Figure 3-4 as follows:

$$v_{wk} = \frac{1}{4}v_{bulb},\ v_s = \frac{1}{2}v_{bulb},\ v_{end} = \frac{1}{4}v_{bulb}, \tag{3.97}$$

where the total bulb voltage is comprised of the three voltages, i.e.

$$v_{bulb} = v_{wk} + v_s + v_{end}. \tag{3.98}$$

Figure 3-22 shows an oscilloscope shot of the bulb voltage and current under the experimental conditions. It shows a bulb voltage amplitude of 200 V and an operating frequency of about 50 kHz. With $v_{bulb} = 200$ V, the pieces of the signal source model become, $v_{wk} = 50$ V, $v_s = 100$ V, and $v_{end} = 50$ V. The signal source model parameters are summarized in Table 3.6.

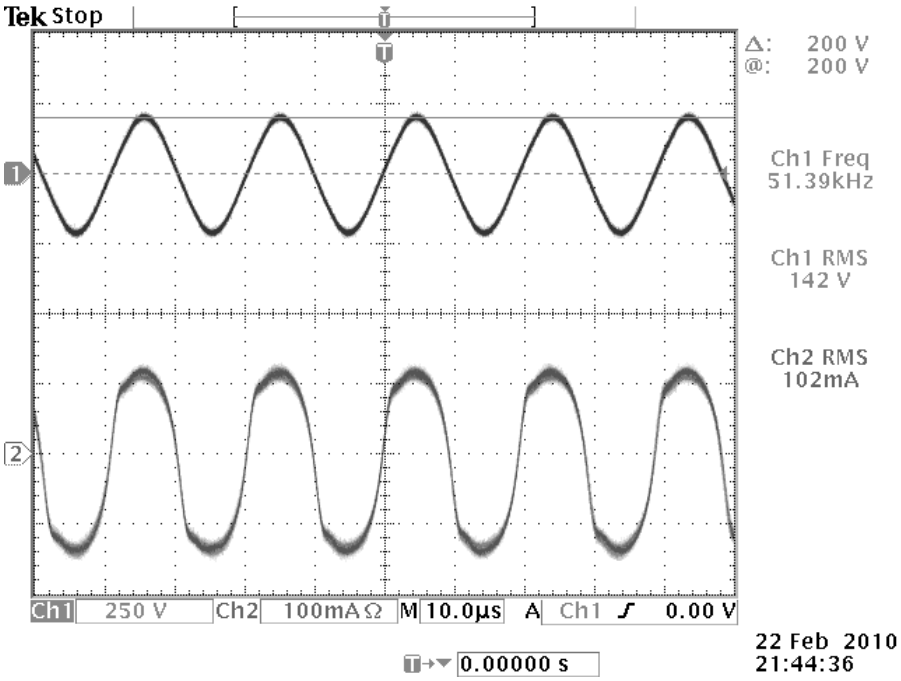


Figure 3-22: Fluorescent bulb voltage (top) and current (bottom).

Note that the polarity and lack of phase shift between the measured bulb voltage and current validates the assumption that the bulb is well-modeled at high-frequency as a resistor. The bulb voltage and current in Figure 3-22 indicate a bulb resistance of approximately 1 kΩ.

3.5.3 Connecting "Earth," "GND," and "Common"

In the lamp sensor system, there are several "reference potentials" including the lamp sensor power supply ground ("gnd"), the ballast common ("common"), and earth ground ("earth").[7] To simplify the simulation, all of those reference potentials were explicitly shorted together in both the experimental setup and in simulation (see the bottom left of Figure 3-25).[8]

Certain conductors were found to be connected to the reference potentials. It was verified with an ohm meter (and a piece of sandpaper) that the pipes, fluorescent lamp backplanes, duct and power strip case were earthed. Those corresponding nodes in

[7] In the LTSPICE simulation, the triangular ground symbol is equivalent to any node labeled "gnd."

[8] Shorting the ballast common to earth required that the L/N utility feed to the ballast be isolated.

Figure 3-25 were shorted to earth. On the other hand, the cabinet was not connected to earth and was therefore modeled in Figure 3-25 as a floating node.

Some of the capacitances in Table 3.5 do not effect the simulated results depending on the connections between reference potentials. For instance, the capacitance between the backplane and the floor is irrelevant when both the backplane and the floor are taken to be connected to earth.

3.5.4 Simulation Procedure

The simulation was conducted using the FastCap® model in Figure 3-20. The simulated capacitances were inserted into the SPICE model shown in Figure 3-25 and the simulated lamp sensor output voltage was read directly from SPICE.

First, the fixed capacitances listed as "assumed fixed" in Table 3.5 were taken from a FastCap® simulation with the target below the left end of the lamp. Then, the simulated offset was measured by inserting all of the capacitances from that FastCap® simulation into the SPICE model of Figure 3-25 and reducing the "vary with target" capacitances by 10 orders of magnitude. The resulting output voltage was saved so that it could be subtracted from the rest of the simulated output values.

Finally, thirty-seven separate simulations like the one depicted in Figure 3-20 were used to model a passing occupant. For each simulation, the target was moved, in 20 cm increments, along the path that the real target in the experimental setup would take. In the simulation, the left end of the lamp was positioned at the x-origin (x = 0 m). The target started 3 m to the left of the origin in simulation (x = -3.0 m) and was stopped 3 m beyond the right end of the lamp (x = 4.2 m). Simulation parameters are summarized in Table 3.6. An example list (.lst) file for creating the model in Figure 3-20 and the dimensions of the individual conductors can be found in Appendix A.4.

Table 3.6: Simulation Parameters.

Simulation Parameter	Note / Value	Source
$v_{bulb1,2}$	200 V	Oscilloscope (Figure 3-22)
$v_{s1,2}$	100 V	Model (Section 3.2)
$v_{wk1,2}$	50 V	Model (Section 3.2)
f_c	50 kHz	Oscilloscope (Figure 3-22)
$Z_{f1,2}$	423 kΩ	Calculated as $\|Z_f\|$ @ $\omega = 2\pi f_c$
Earth, gnd, Common	Explicitly connected	N/A
Electrode Depth	14.5 cm	Meas'd electrodes to bulb surface
Electrode Spacing	98 cm	Measured between electrodes
Lamp Height	2.28, 2.43, 2.58 m	Measured from bulb surface to floor
Target Height	1.83 m	Measured height of human occupant
Effective Conducting Floor Depth	-2.5 cm	Empirical (Section 3.5.2)

3.5.5 Experimental Procedure

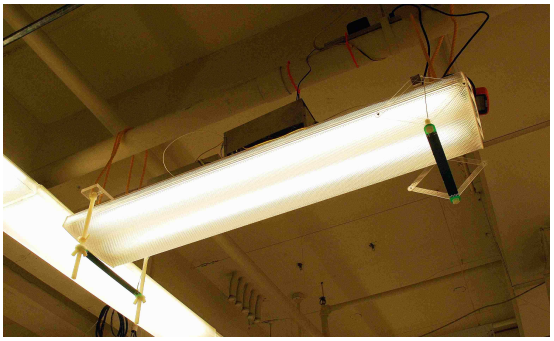
Experimental data was taken from the experimental setup shown in Figure 3-23(b). The photograph in Figure 3-23(b) is labeled so that it is obvious how the experimental setup corresponds to the 3D model shown in Figure 3-20. Figure 3-23(a), shows a close-up of the hanging lamp sensor and its adjustable electrodes.

Data was taken for the target passing through a detection field 7.2 m long positioned symmetrically about the center of the lamp (along the black line on the floor in Figure 3-23(b)). This path was chosen to correspond to the simulated path described in Section 3.5.4.

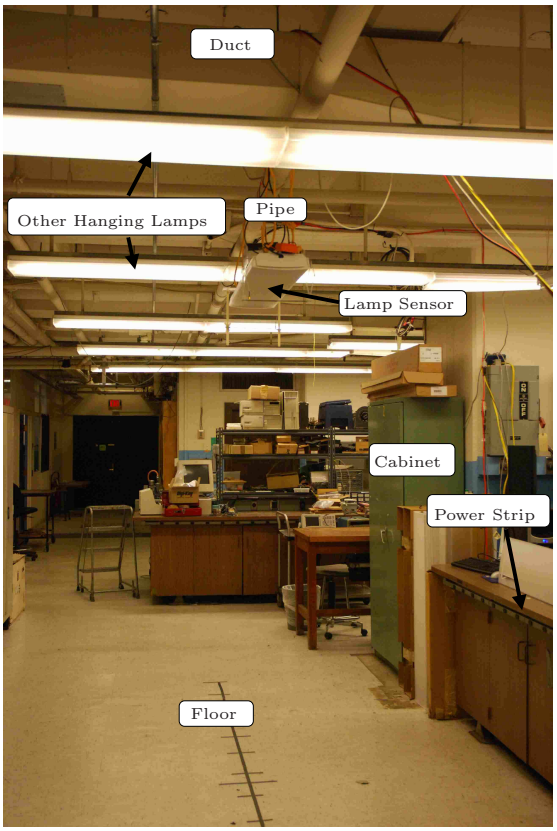
Table 3.7: Experimental Setup Parameters.

Experimental Parameter	Note / Value
$R_{f1,2}$	10 MΩ
$C_{f1,2}$	7.5 pF
R_{f3}	200 kΩ
C_{f3}	660 pF
f_c	50 kHz
Phase Ref Elect.	Integrated as Trace in Ballast
Earth, gnd, Common	Explicitly connected
Electrode Depth	14.5 cm
Electrode Spacing	98 cm
Lamp Height	2.28, 2.43, 2.58 m
Target Height	1.83 m

Exactly 37 data points were taken from each pass in the experimental setup in order to ease the comparison to the simulated data. At the sampling rate of 13.75 sps, 37 data samples took approximately 2 seconds. Some trial and error was necessary



(a) A close-up photograph of the hanging lamp sensor.



(b) A photograph of the experimental setup.

Figure 3-23: Photographs of the hanging lamp experimental setup.

to acquire data that was situated symmetrically about the time axis in the resulting output plot. The experimental offset was measured as the value of the first data point taken from the sensor (corresponding to the case when the target is not well within the detection field). That offset was subtracted from all of the experimental data. Experimental setup parameters including passive component values for the sensor are summarized in Table 3.7.

3.5.6 Model Evaluation

Figure 3-24 shows three comparisons between measured data taken from the lamp sensor and simulated data taken from the circuit in Figure 3-25. The three plots in Figure 3-24 correspond to three different lamp heights, 2.28 m, 2.43 m and 2.58 m measured between the floor and the bottom of the bulb surfaces in the experimental

setup. They show good agreement among the simulated and experimental data. Scripts for extracting data from the SPICE .log files and generating the plots in Figure 3-24 can be found in Appendix A.4.1.

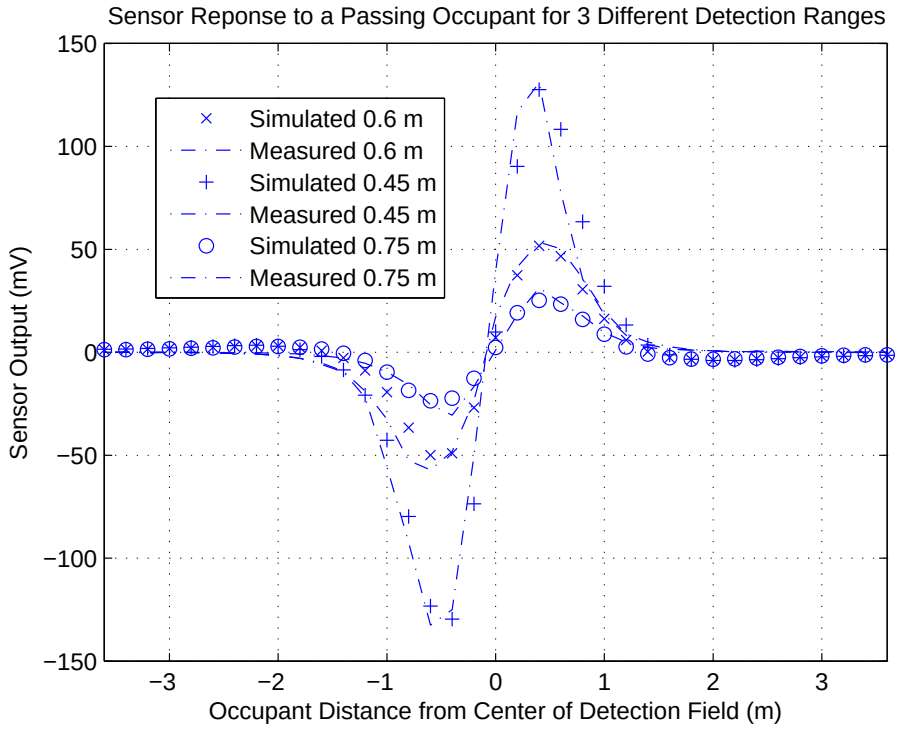


Figure 3-24: Comparison between simulated and measured occupancy sensor output data.

The system model in this section was presented "as-is" with little or no simplification. That is, the intent was to include all of the capacitances between all of the conducting nodes in the system as a starting point for a working model. Undoubtedly, accurate prediction is possible without considering all of those capacitances. Moreover, the simulation likely discounts some capacitances that may influence the sensor response. Finally, the limitations of the lumped-element capacitive model described in Section 3.2.4 should be considered when evaluating the model presented here.

3.5.7 Effective Capacitive Sensitivity

From the lamp sensor response in Figure 3-24, and the simulated capacitances taken from FastCap®, the sensitivity of the lamp sensor to changes in capacitances (effective

capacitive sensitivity) can be inferred. Table 3.8, shows the capacitances that vary with the target for two different simulations. The first column shows capacitances for the target positioned 40 cm to the left of the left end of the lamp ($x = -100$ cm). The second column shows capacitances for the target positioned 20 cm to the left of the left end of the lamp ($x = -80$ cm). The third column shows the change in those capacitances. In the lampsensor output plot of Figure 3-24, this corresponds to a change of at least 10 mV. Compared to typical noise levels of about 200 μV, like those in Figure 3-17, a deviation of 10 mV is quite significant. Therefore, based on simulation and experiment, the lamp sensor appears to easily measure changes in the capacitances below the lamp on the order of 10's and 100's of fF.

Table 3.8: Simulated Capacitance Change: $x = -100$ cm to $x = -80$ cm.

Capacitance	$x = -100$ cm	$x = -80$ cm	Change
L. Source-Target	214 fF	266 fF	52 fF
R. Source-Target	100 fF	133 fF	33 fF
L. Electrode-Target	394 fF	475 fF	81 fF
R. Electrode-Target	116 fF	144 fF	28 fF
Backplane-Target	13.2 pF	13.8 pF	600 fF
Cabinet-Target	3.6 pF	3.0 pF	600 fF

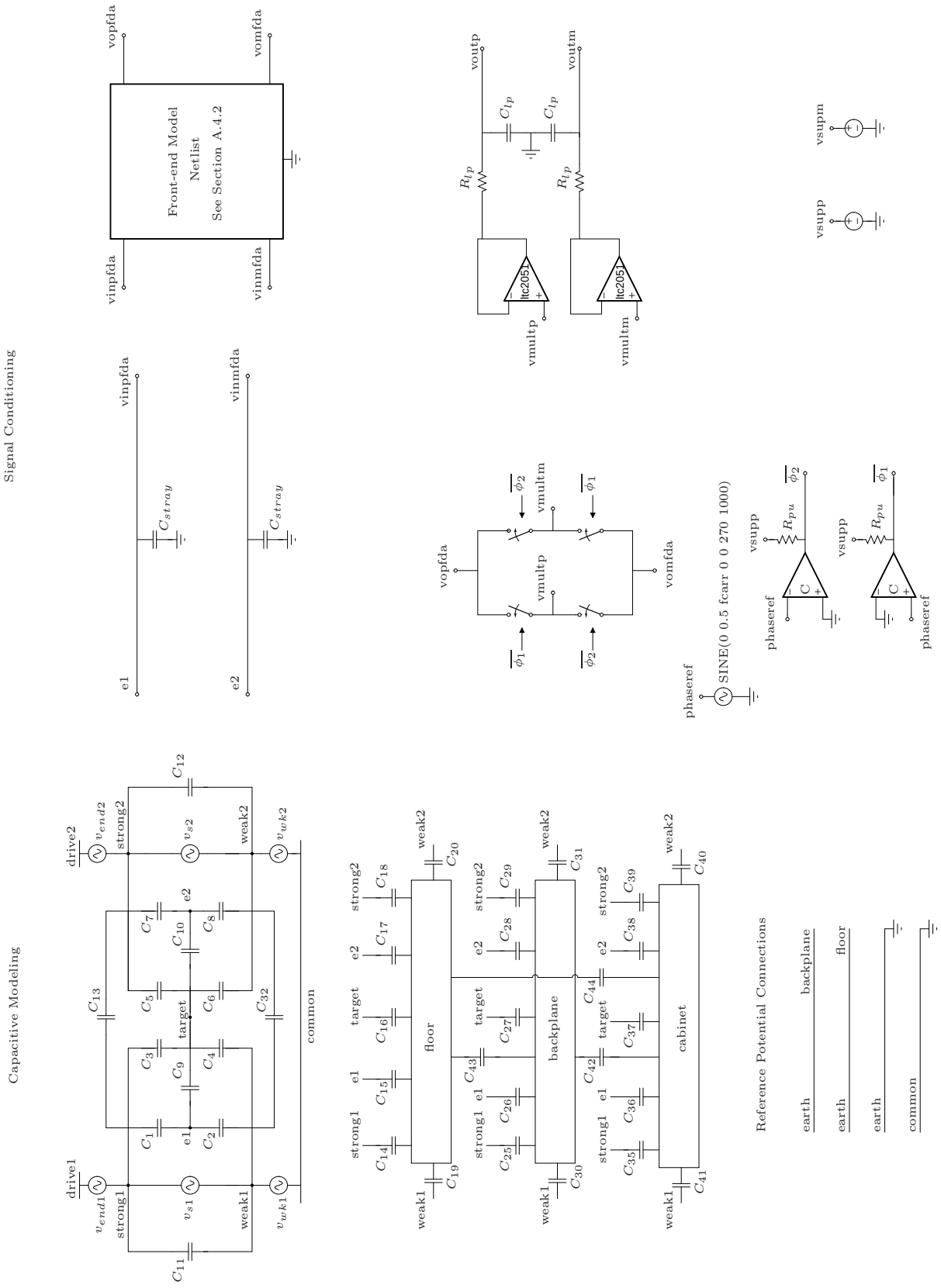


Figure 3-25: A SPICE simulation of the capacitive model, F-D Transimpedance Amplifier Front end and the signal conditioning electronics.

3.6 Auto-dimming

This section presents the building blocks of a new autonomous and self-expanding demand-side energy management system for lighting control. It is a demand-side energy management system because the control of energy consumption is confined to the demand or end-user portion of the power system. References [96–99] detail the design of the "lamp sensor" which measures the lamp's own electric fields to detect human targets. Interfacing the lamp sensor with a dimming ballast creates a smart auto-dimming lamp which uses the lamp sensor's occupancy detections to appropriately dim or brighten. These fine-grain occupancy detections may also be used to adjust power consumption of other systems such as Heating, Ventilation and Air Conditioning (HVAC). All of the electronics are made to fit inside a ballast box with the intent to create a drop-in replacement for standard ballasts. We have also demonstrated a quasistatic frequency-modulated (FM) wireless link to enable communication between adjacent lamps. By communicating with adjacent lamps, one lamp can command a cluster or an entire room of lamps to turn on above an occupant according to desired lighting schemes. The wireless link reuses the lamp sensor electric field measurement and the action of the frequency-controlled dimming ballast.

Because the performance of the lamp sensor system depends on many factors such as ceiling height, electrode configuration, separation of lamps, the physical geometry of the particular lamp case, etc., the auto-dimming lamp in this work is presented as an example. From this example, we detail critical system characterizations that must be understood by the system designer to implement a network of auto-dimming lamps.

Section 3.6.2 presents system characterizations necessary to implement the auto-dimming lamps including the lamp as a signal source and the lamp sensor signal-to-noise ratio (SNR) across dimming levels. It also presents example characterizations of three critical non-idealities in the lamp sensor system: drift, offsets and offset settling after switching between dimming levels. It then presents a strategy for using this

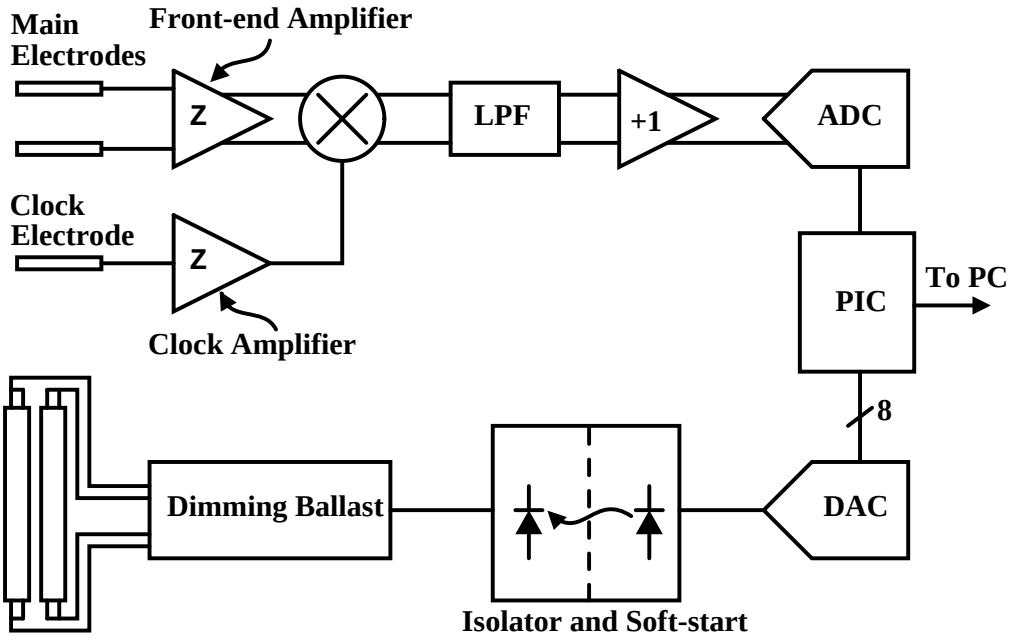


Figure 3-26: The block diagram of the auto-dimming lamp sensor. Transimpedance amplifiers are marked with a 'Z'.

information to design an auto-dimming lamp including auto-calibration and detection strategies as well as a demonstration of a real auto-dimming lamp. Section 3.6.6 presents a novel wireless link between adjacent lamps including the design, simulation and measurement of a phase-locked loop (PLL).

3.6.1 Dimming Ballast and Lamp Sensor Interface

A simplified schematic of the dimming ballast is shown in Figure 3-27. It is designed to operate the lamp between 1.3% and 90% of the full specified power for two T8 32W bulbs. The ballast adjusts the lamp power or brightness by changing its output (excitation) frequency relative to the natural frequency of the LC tank created by L_{res} and C_{res}. The ballast adjusts its excitation frequency from 64.4kHz to 41.7kHz for minimum to maximum lamp power respectively.

The frequency-controlled dimming ballast is designed around the International Rectifier part IR21592 [11]. The ballast consists of a utility-line rectifier and boost-mode power factor corrector (PFC). The STMicroelectronics part L6561 handles the power factor correction and dc-dc up-conversion for the high-voltage dc input to the

inverter stage of the ballast. The IR part controls the half-bridge inverter that drives the lamp output stage. The lamp output stage consists of two fluorescent bulbs in series with a "balance transformer", a shunt resonant capacitor and a series resonant inductor. The balance transformer matches the currents in the two bulbs to prevent "winner-take-all" situations in which one bulb strikes before the other, loading down the resonant tank output and preventing the other bulb from striking.

The IR part controls the lamp power as described in the IR21592 datasheet. During dimming, the output stage is effectively an inductance in series with a parallel bulb resistance and resonant capacitance. The current into the output stage is shifted from the half-bridge output voltage somewhere between 0 and -90 degrees during dimming. Zero phase-shift corresponds to maximum lamp power [11].

The IR21592 takes a dim level input voltage (0.5-5Vdc) command and generates a reference signal. The phase between this signal and the gate drive signal is the desired phase between the output current and voltage in order to achieve the proper lamp power. The phase reference signal is compared to the inverter output current and the resulting phase error forces the circuits voltage-controlled oscillator (VCO) to steer the inverter frequency in the right direction. The VCO steers the frequency until the phase error between the output stage current and the reference signal is forced to zero yielding the desired lamp power [11].

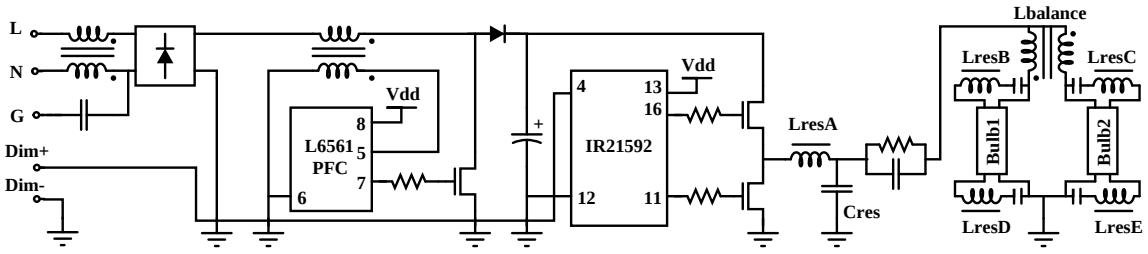


Figure 3-27: A simplified schematic of the frequency-controlled dimming ballast. The ballast is designed around the International Rectifier part IR21592 [11].

The lamp sensor-ballast interface consists of a buffered digital-to-analog converter (DAC) and an optical isolation barrier as indicated in Figure 3-26. The optical isolator and soft-start circuitry is shown in Figure 3-28. The optical isolator separates the lamp sensor's ground from the ballast's ground. It also provides a high-voltage safety

barrier so that the lamp sensor is not easily damaged by dramatic failures in the ballast. The soft-start is intended to protect the bulbs. It clamps the dimming signal to the range 0.5-5V. It also brings the lower limit down slowly on startup so that the bulbs are struck at a high dimming level and then brought down slowly if the lamp sensor is either off or commanding a low dimming level.

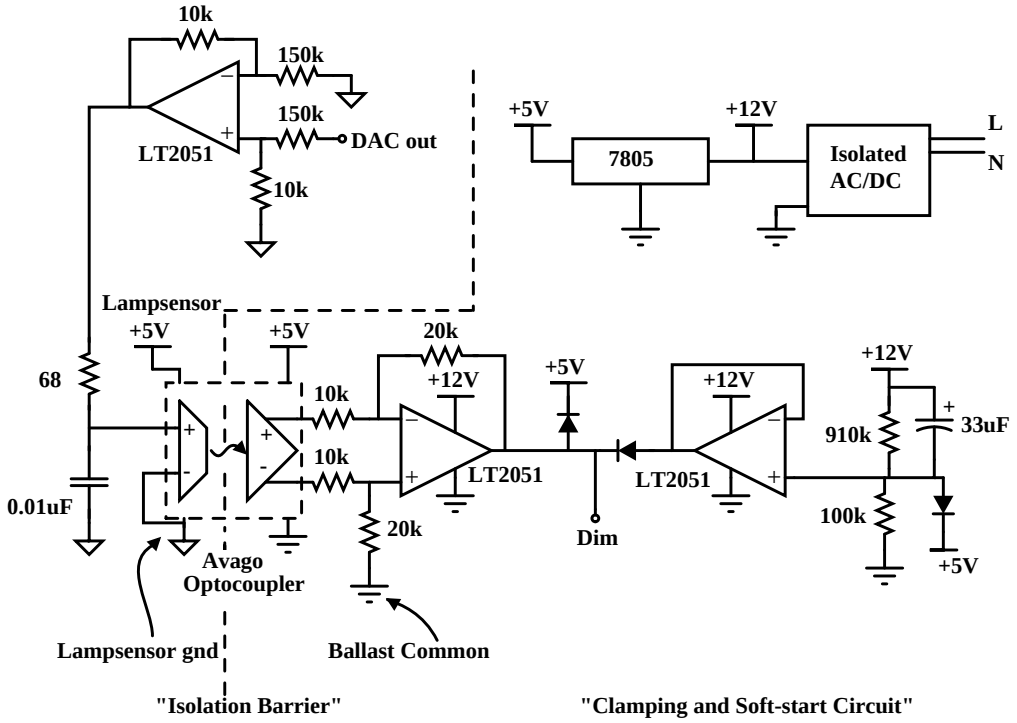


Figure 3-28: The optical isolator separates the lamp sensor common potential from the ballast common potential. The soft-start protects the bulb by clamping the dim signal to the range 0.5-5 V and brings the dim signal down slowly on startup.

3.6.2 Auto-dimming Considerations

This section presents examples of critical system characterizations, a strategy for using those characterizations to design auto-calibration and detection algorithms and a demonstration of the auto-dimming lamp.

Certain performance metrics depend strongly on the height of the lamp and the electrode configuration. For the following discussion of the auto-dimming lamp, the lamp height was 7ft. 4in. above the floor, the electrode depth was 5 in. and the electrode spacing was 38 in.

3.6.3 Lamp Sensor SNR across Dimming Levels

The signal-to-noise ratio (SNR) of the lamp sensor system across dimming levels must be determined as this constrains the detection range. To characterize the source, we measured the bulb rms voltage across power levels. It is well known that the bulb current-voltage (I-V) characteristics exhibit positive nominal resistance, but negative incremental resistance for some operating regions [100]. That is,

$$\frac{V}{I} > 0, \text{ but } \frac{dV}{dI} < 0. \tag{3.99}$$

This means that decreasing the current in the bulb increases the voltage across it. In Figure 3-29, the rms bulb voltage is plotted against lamp power. Lamp power is calculated as the average power, i.e.

$$P_{\text{avg}} = (I_{\text{rms}} V_{\text{rms}}) \cos\phi \tag{3.100}$$

where ϕ is the phase between the voltage and current. Percent lamp power is defined as the power relative to the maximum bulb power, e.g. 32W. For instance, the lowest lamp power shown, 1.3%, is 0.013×32W = 420mW.

Because lamp current increases monotonically with lamp power, the plot in Figure 3-29 can also be taken as the bulb's I-V characteristic. The plot shows the familiar negative incremental resistance to the right of the peak in the voltage near 25% lamp power.

To characterize the lamp sensor sensitivity across power levels, we performed an experiment with a hanging lamp sensor to measure the SNR with a 6ft.-tall person under the lamp. Each detection consisted of the target passing through the entire detection field of the lamp sensor yielding a peak-to-peak differential output voltage. Each detection was repeated 5 times for each dimming level. Also, at each dimming level, the windowed noise floor was measured in the time-domain by taking the average ac rms voltage from 15 5-second windows with no target. The noise window length was chosen to match the time it took to fully walk in and out of the detection field.

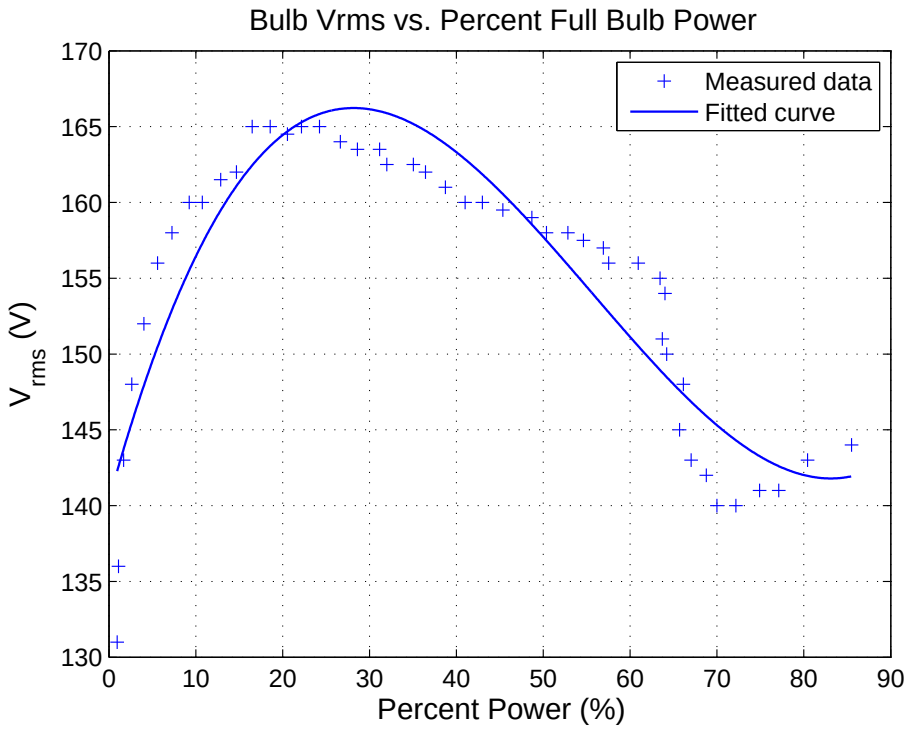


Figure 3-29: A curve fit of the rms bulb voltage plotted against lamp power (which increases with rms current) shows the familiar negative incremental resistance of the bulb.

The noise experiments were repeated after the entire first trial and these data were averaged into the first data set in order to minimize the effect of long-term changes in noise levels. The results are presented in Figures 3-30 and 3-31. SNR here is defined as the peak-to-peak detection voltage of the human target divided by the ac rms windowed noise voltage in the absence of a detection.

The signal from the lamp sensor increases to follow the bulb I-V characteristic curve so that it shows a maximum around 25% lamp power as shown in Figure 3-30. However, the sensitivity of the lamp sensor is quantified by the SNR. Because the dominant noise originates in the bulbs and ballast, we might expect it to also vary with the lamp power [96–99]. The SNR plot across lamp power levels in Figure 3-31, shows that the sensitivity actually shows a maximum around 40% lamp power. Such SNR characterizations will be necessary for the designer to determine at which power levels detection is possible. In this experiment, we have shown a situation in which detection is easily possible even at 1.3% (minimum) lamp power.

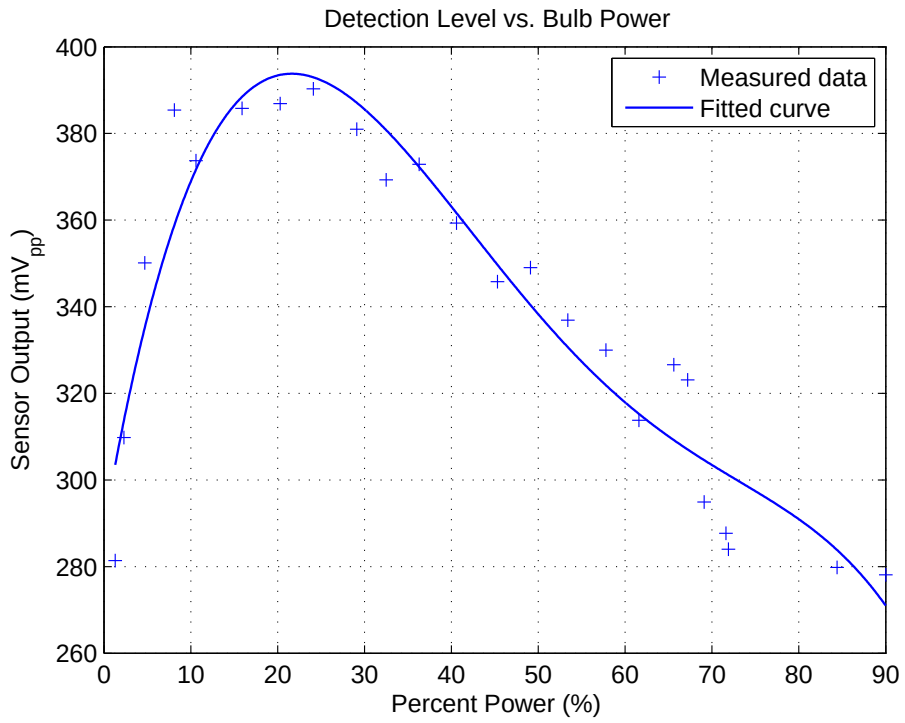


Figure 3-30: A curve fit of the detection signal bulb voltage plotted against lamp power.

3.6.4 Characterization of Non-idealities

Characterization of output voltage offsets and transients when switching between the dim and bright power levels are necessary for the design of auto-calibration and detection algorithms. Despite correcting for phase errors, there are still measurable offsets in the lamp sensor output voltage when switching between dimming levels. These offsets may be due to differences in the voltage profiles of the two bulbs as they are dimmed or due to un-corrected phase errors across dimming frequencies. Figure 3-32 shows a plot of the output voltage when repeatedly switching between dimming levels. For these particular bulbs and dimming levels (8.1% and 59.4%), the difference between output voltage offsets is about 40mV. The plot shows two important features. First, the offsets are repeatable. That is, when switching back to a dimming level, the output offset will be the same as it was the last time (ignoring drift). Second, there is a consistent transient after each switch, after which the output voltage flattens. The output voltage offsets and transients will determine the baselines for detection in the

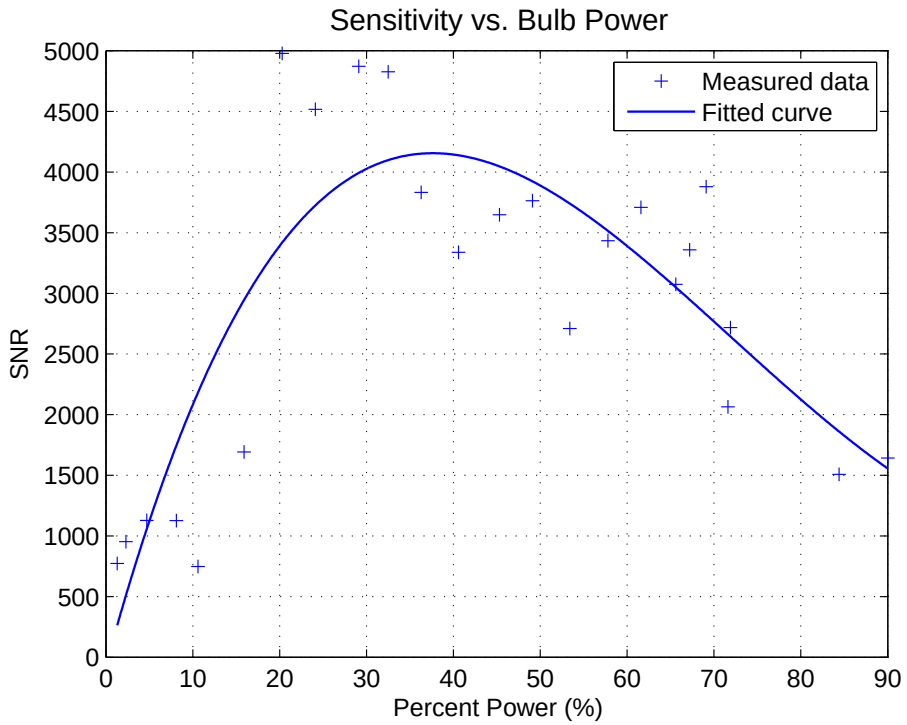


Figure 3-31: A curve fit of the SNR plotted against lamp power shows a maximum SNR around 40% power.

auto-dimming system. Deviations from the baselines will correspond to detections.

Characterization of output voltage drift ensures repeatable detection and triggering over time. Figures 3-33(a) and 3-33(b) show typical output voltage drift over a period of 60 minutes (long-term) and 3.5 minutes (short-term) respectively for the low lamp power level (8.1%). This data can be used to determine detection bands around the baselines to account for drift. We know from previous experiments, that several mechanisms contribute to drift including sources in the ballast and lamp [96–99]. Therefore, we may speculate that warming and cooling of the bulbs yields slowly varying asymmetries between the two signal sources that appear as differential modulations of the measured signal.

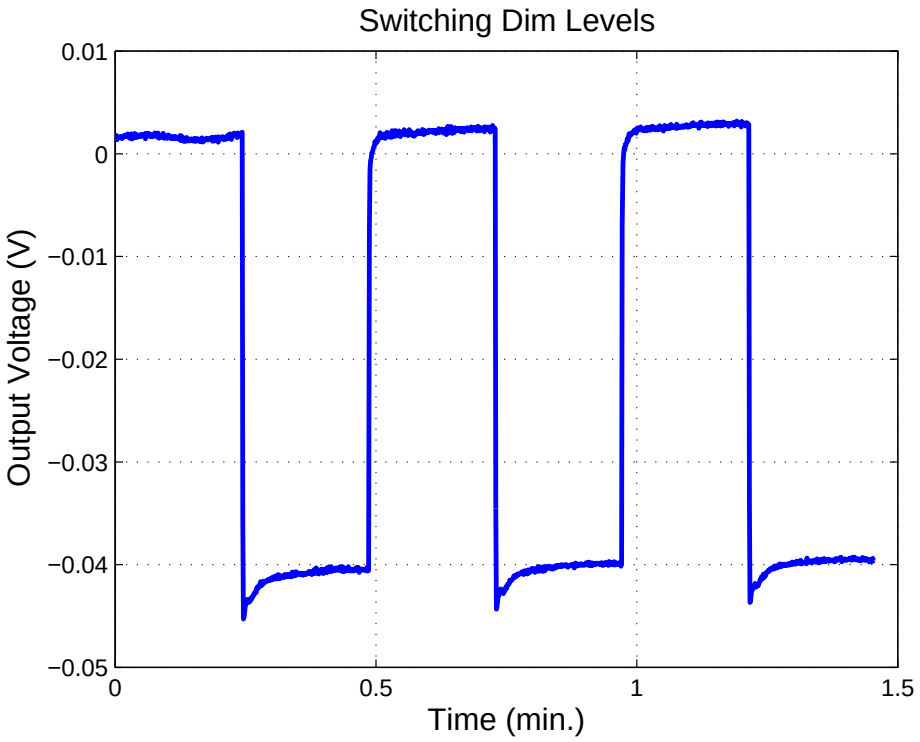
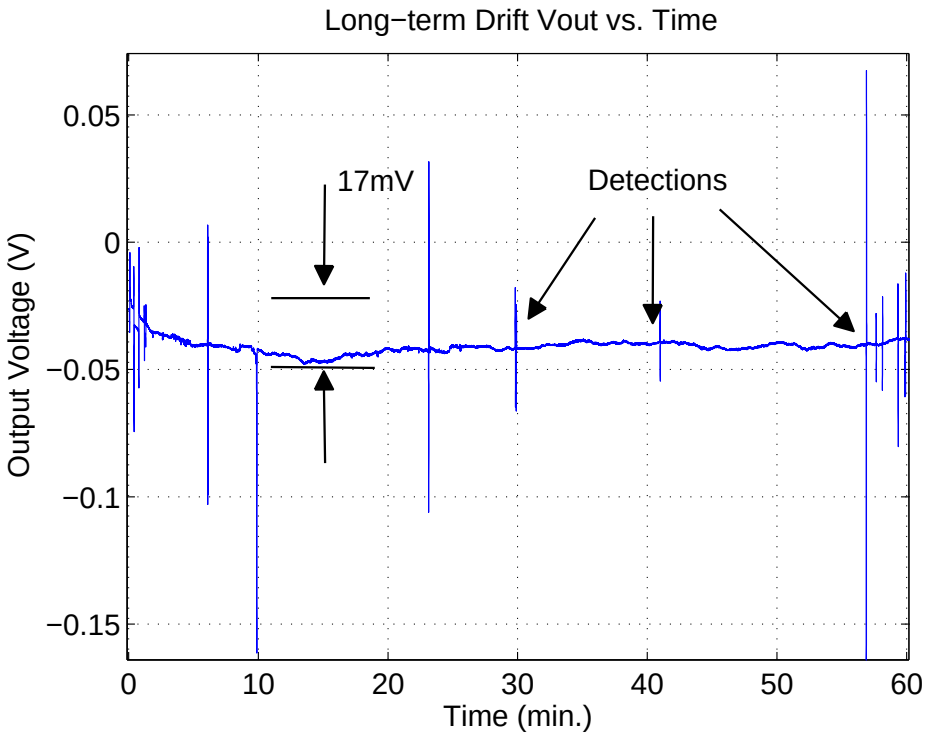
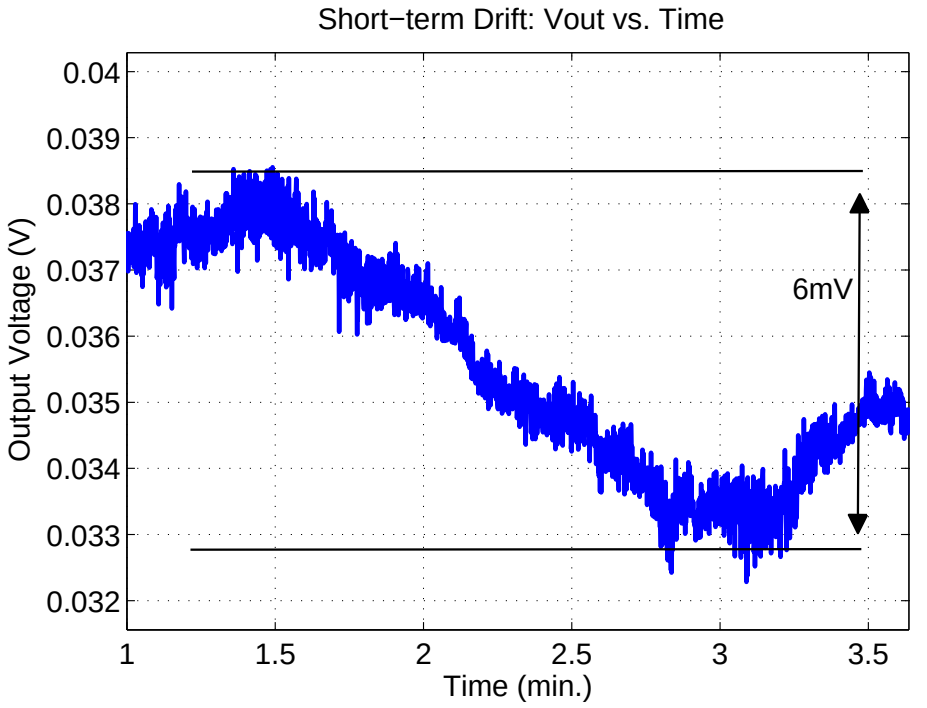


Figure 3-32: The lamp sensor output voltage for repeated switching between dimming levels. The two lamp power levels in this example are 8.1%(dim) and 59.4% (bright).



(a) An example long-term drift output voltage plot; 17 mV in 60 min.



(b) An example short-term drift output voltage plot; 6 mV in 3.5 min.

Figure 3-33: Example Drift Plots for the Lamp Sensor output voltage. Both plots show data taken for a lamp power level of 8.1% (dim).

3.6.5 Auto-calibration, Detection and Demonstration

This section shows how to use the characterization of non-idealities to implement an auto-dimming lamp. A screenshot of the output display from the prototype auto-dimming lamp is shown in Figure 3-34. The screen shot shows two different baselines for when the lamp is bright (59.4% lamp power) and dim (8.1% lamp power) respectively. The baselines are the approximate output voltage in the absence of detection and they are different because of the offsets described above. The two baselines are generated during the auto-calibration which takes place on start-up. The auto-calibration procedure uses the information gained from characterizing the output voltage offsets and transients when switching between dimming levels. The first auto-calibration procedure used was as follows. In the absence of a detection, the lamp is first brightened and the output voltage is measured. The first 80 points (about 6 seconds) are discarded as part of the switching transient depicted in Figure 3-32 and the remaining 20 points (about 1.5 seconds) are averaged. This average becomes the "bright baseline". The lamp is then dimmed and the procedure is repeated to generate the "dimmed baseline."

The detection algorithm uses the information gained from characterizing the output voltage offsets and drift. The detection algorithm used here was as follows. When the lamp is dimmed, if the output voltage deviates from the dimmed baseline by more than +/-17mV and the deviation persists for more than 200ms, then the lamp is undimmed. When the lamp is brightened, if the output voltage returns to within 10mV of the bright baseline and this persists for more than 200ms, the lamp is dimmed again. The turn-on deviation level (17mV) is greater than the turn-off level (10mV) to discourage multiple transitions. The timing delays serve at least 2 purposes. First, when the target passes under the lamp, it is possible for the output to reach the baseline if the target is symmetrically positioned below the center of the lamp. The delay in this case means that the target must not only be carefully positioned under the lamp but it must stay that way for a little while. Second, the delay adds further protection against multiple transitions when the output voltage is

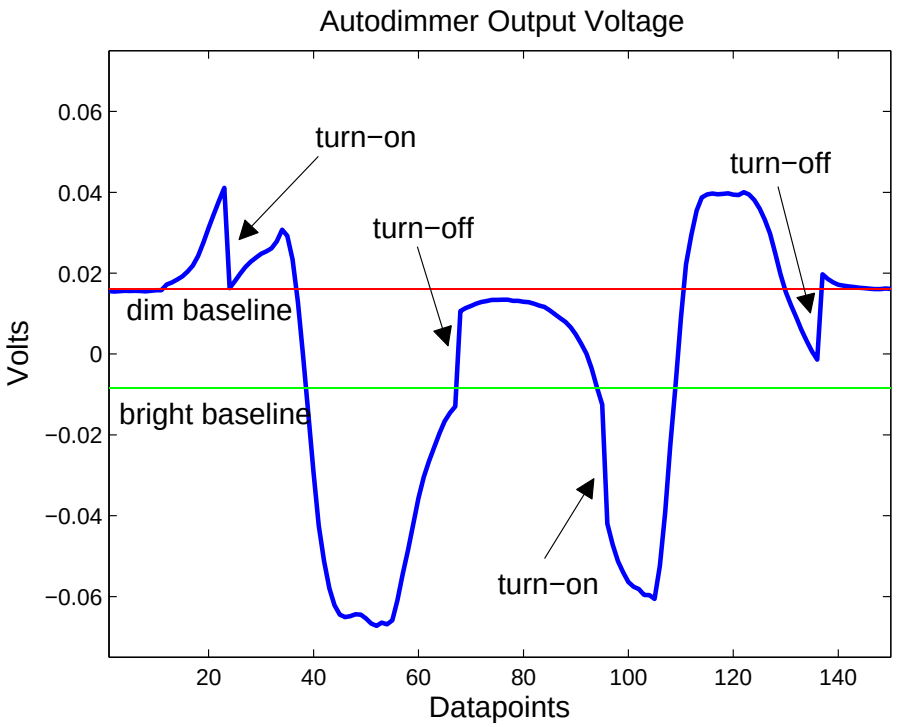


Figure 3-34: This plot is a screenshot of the display for the autodimmer. It shows the output voltage varying with the target and the two different baselines taken from the auto-calibration. Jumps in the output voltage can be used to determine when the lamp dimmed or brightened.

slowly varying.

More advanced auto-calibration procedures will make the auto-dimmer more robust and more sensitive. One obvious improvement would be to store the transient of the output voltage after switching between dimming levels and use this to adjust the baselines in real-time after switches. More advanced detection algorithms will also improve robustness and sensitivity. For instance, it may be possible to not only constrain the deviation from the baseline, but also the time derivative of the deviation. If the deviation is small, but the combination of the time derivative and the deviation is unlike any drift or noise expected from the lamp sensor, then it may be possible to rule that as a detection. Ultimately, we have the advantage that a "false-positive" detection is not tragic. Therefore, in our detection algorithms we may lean toward avoiding missed detections at the expense of a higher rate of false-positives.

3.6.6 Quasistatic FM Wireless Link

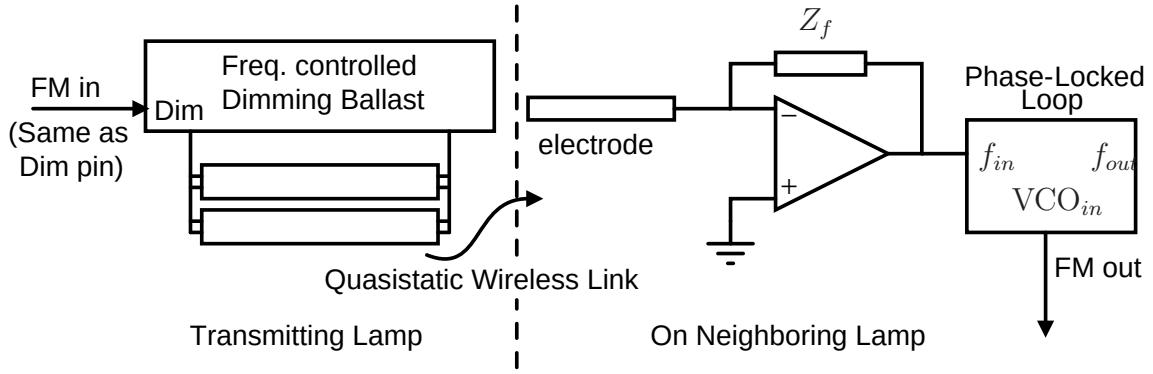
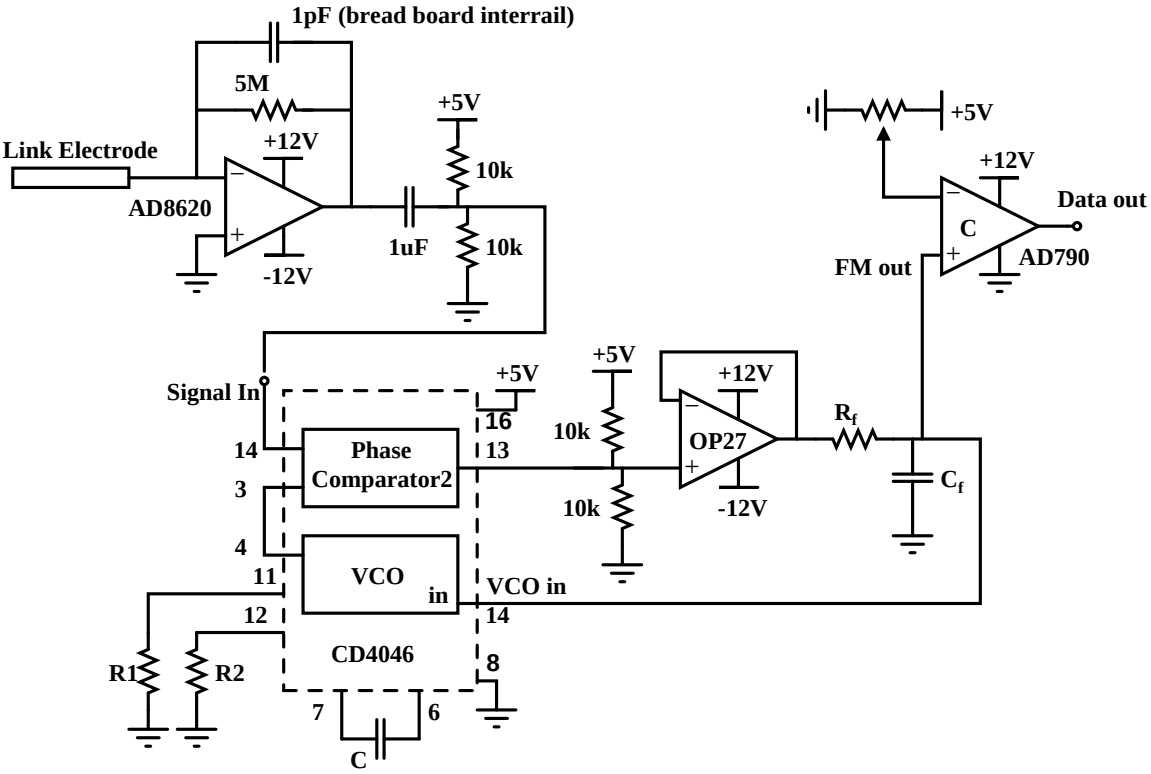
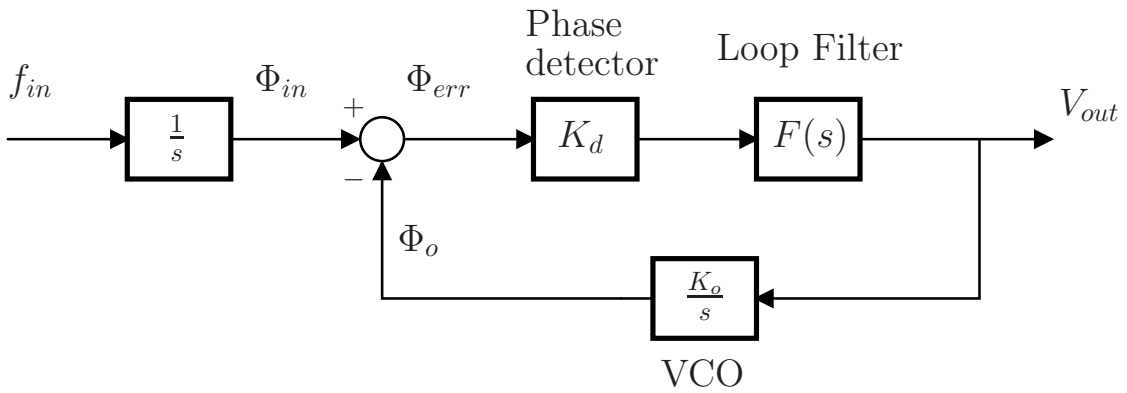


Figure 3-35: A notional picture of the quasistatic wireless link system.

This section details the design and performance of the quasistatic wireless link for communication between adjacent lamps. By communicating with neighboring lamps, a detection by a single lamp could, for instance, command its neighboring lamps to turn on as well, and command those lamps to tell their neighboring lamps to turn on. Thus a particular lighting scheme may cause a single lamp, a cluster of lamps, or an entire room of lamps to turn on upon an occupancy detection. Such a network of auto-dimming lamps would self-expand as more lamps were added because the lamps would each passively and wirelessly command their neighboring lamps to turn on.



(a) The schematic of the receiver including the PLL.



(b) The dynamical block diagram of the PLL from input frequency to output baseband voltage.

Figure 3-36: The wireless link receiver and the PLL dynamical block diagram.

The wireless link is quasistatic because it does not use propagating electromagnetic waves for transmission. It uses the same electric fields from the lamp that the lamp sensor uses to detect occupants. The electric fields vary slowly enough (∼50kHz) that the associated wavelengths for propagating waves at these frequencies are extremely long compared to the length-scales of the lamp sensor system. It is a frequency-modulated (FM) link because it transmits information by adding small frequency deviations or modulations (∼+/-500Hz) to the high-frequency (∼50kHz) ballast signal.

The notional drawing of the wireless link is shown in Figure 3-35. The baseband or frequency modulating signal is input as small voltage deviations on the dim pin of the dimming ballast. A single-ended transimpedance amplifier, similar to those used in the lamp sensor, measures the frequency-modulated electric fields at the receiving lamp's electrode. The signal that is detected is input to a phase-locked loop (PLL). When the PLL locks onto the input signal, the VCO input is a dc voltage which corresponds to the input signal frequency. When the input signal frequency changes, the PLL tracks those changes and the VCO input varies correspondingly. The baseband or modulating signal is then available at the VCO input, which we call the output of the PLL here.

3.6.7 PLL Design

The full schematic of the receiver including the PLL is shown in Figure 3-36(a). The dynamical block diagram is shown in Figure 3-36(b). This PLL uses a phase detector and VCO from the Fairchild Semiconductor part CD4046 [10]. The gain term, K_d, is determined by the phase detector output voltage function for the connection shown in Figure 3-36(a) [10]:

$$V_{pd} = 2.5\ \mathrm{V} + \frac{\Theta_{\mathrm{err}}}{2\pi} \times 2.5\mathrm{V} \tag{3.101}$$

$$K_d = \frac{dV_{pd}}{d\Theta_{\mathrm{err}}} = \frac{2.5}{2\pi}\frac{\mathrm{V}}{\mathrm{rad}}. \tag{3.102}$$

The gain term K_o is the VCO gain from input voltage to output frequency. The

external components R_1, R_2, and C determine K_o and the VCO center frequency, f_o. Using the CD4046 datasheet, these values were chosen to yield

$$f_o = 57.4 \text{ kHz} \tag{3.103}$$

and

$$K_o = 14.4 \frac{\text{krps}}{\text{V}}. \tag{3.104}$$

Smaller modulations of the ballast frequency yield less visible flicker in the light. The gain K_o could be as low as necessary for those modulations to fill the input dynamic range of the VCO (0.5-4.5V). However, such a small K_o will lead to a small gain-bandwidth product (GBW), $K_o K_d$, of the integrator in the loop. The transfer function from f_{in} to $\text{VCO}_{in} = V_{out}$ with a passive RC low-pass loop filter is

$$\frac{V_{out}(s)}{f_{in}(s)} = \frac{K_d/R_f C_f}{s^2 + s/R_f C_f + K_d K_o/R_f C_f}. \tag{3.105}$$

Recognizing $K_d K_o$ as the GBW and the entire denominator of eqn. (3.105) as the characteristic polynomial of a second-order system,

$$p(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{3.106}$$

$$\omega_n = \sqrt{\frac{\text{GBW}}{R_f C_f}} \tag{3.107}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{R_f C_f \times \text{GBW}}} \tag{3.108}$$

where ω_n is the natural frequency and ζ is the closed-loop damping ratio. From [92], the bandwidth of this second-order system is

$$\omega_h = \omega_n \sqrt{1 - 1\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}}, \tag{3.109}$$

which is always greater than ω_n so that the closed-loop bandwidth, ω_h, increases with the GBW, $K_o K_d$, of the loop.

A small K_o will also limit the frequency range which the PLL can lock onto (lock range). Instead, choosing a larger value of K_o increases the GBW of the loop and the lock range. As a consequence, small frequency modulations only produce small deviations of the VCO input voltage, so the threshold of the comparator at the output of the system must be trimmed to be centered on those small deviations. A tradeoff between noticeable flicker, PLL noise and PLL bandwidth falls out of this discussion. If, for instance, we wanted to reduce the change in dimming levels to reduce the noticeable light flicker, we could reduce the change in ballast frequencies or modulation depth but this would also reduce the VCO input deviations. At some point the VCO input deviations will fall below the VCO input-referred noise. To increase the deviations we only have two choices: increase the flicker in the lamp, or decrease the gain K_o of the VCO so that the reduced changes in frequency fill more of the VCO input range. However, from above, we know that decreasing K_o decreases the closed-loop bandwidth of the PLL. We can write a fundamental expression relating these trade-offs in the PLL described here.

$$\text{GBW} = K_o K_d \tag{3.110}$$

$$K_o \Delta\text{VCO}_{in} = \Delta f \tag{3.111}$$

$$\boxed{\frac{\text{GBW}}{K_d} = \frac{\Delta f}{\Delta\text{VCO}_{in}}} \tag{3.112}$$

To attenuate the high-frequency components of the phase-detector output while maintaining reasonable loop stability, the LPF 3db frequency was chosen to match the cross-over frequency of the integrator in the feedback loop shown in Figure 3-36(b). That is,

$$\omega_{3db} = \frac{1}{R_f C_f} = K_o K_d = \text{GBW} \tag{3.113}$$

This strategy leads to about 45° of phase margin. The values for R_f and C_f in Figure

3-36(a) are

$$R_f = 2\text{k}\Omega \tag{3.114}$$

$$C_f = 0.1\mu\text{F}. \tag{3.115}$$

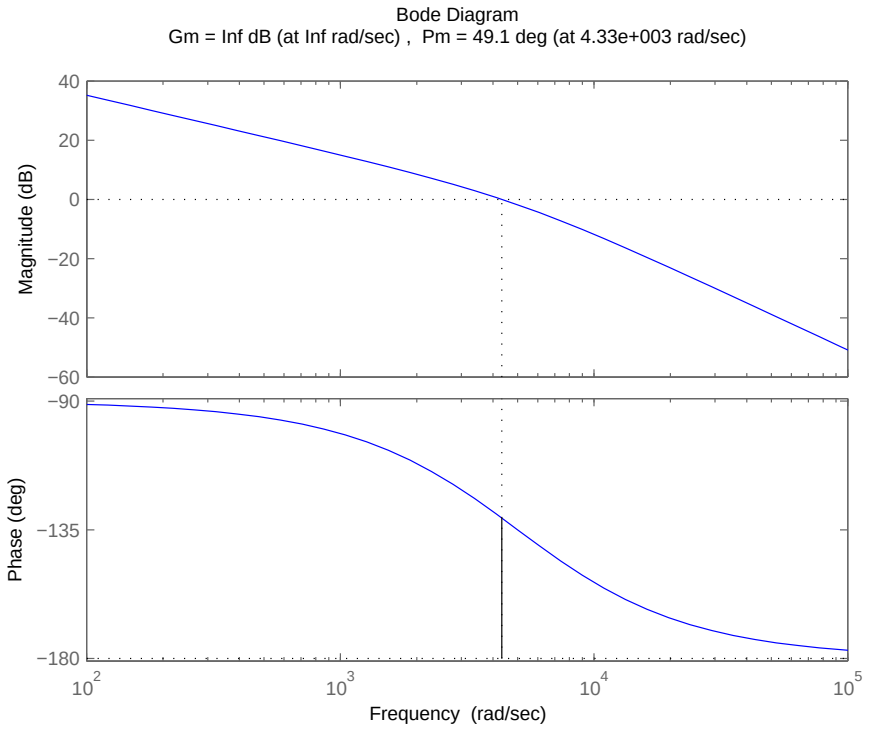


Figure 3-37: Bode plot of the loop transfer function of the PLL.

The Bode plots of the loop transfer function and the closed-loop transfer function are shown in Figures 3-37 and 3-38. They show 49° of phase margin and a closed-loop bandwidth of 6.9krps or 1.1kHz. In this PLL, because the loop filter is a first-order RC LPF, the average value of the phase detector output is the VCO input. Therefore, the steady-state phase error, $\Theta_e(t)$ and the corresponding phase detector output voltage varies with the steady-state VCO output frequency. Because the VCO input range is 0.5-4.5V, the extremes of the output frequency lock range in eqn. (3.101) correspond to a phase error range of about +/-5 rad. Therefore, for all frequencies within the lock range, the phase error is never more than +/-2π rad. and this PLL is not vulnerable to skipping cycles during step transients or "cycle slipping" [101].

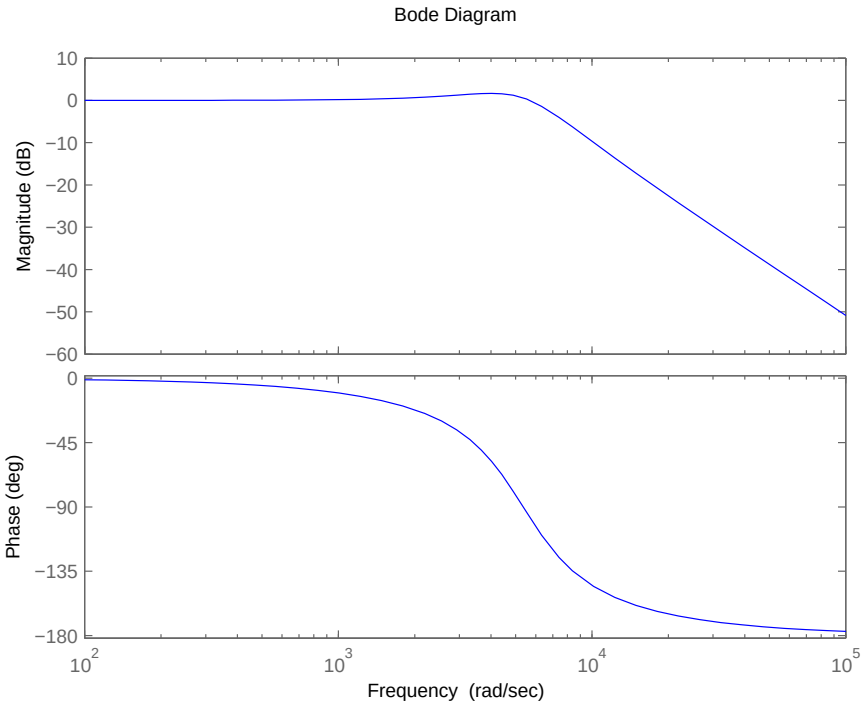


Figure 3-38: Bode plot of the closed-loop transfer function of the PLL.

The simulated and measured step response from the input signal to the VCO input voltage are shown in Figures 3-39, 3-40 and 3-41. The measured step response was generated with an FM-capable Agilent signal generator driving the input signal to the PLL. The measured peak overshoot in the step response is about 1.2 which for a second-order system corresponds to 45° of phase margin as predicted above [92]. The rise time of the measured step response is about 320μs which for a second order system corresponds to a bandwidth of

$$\text{BW} \approx \frac{2.2}{t_r} = 6.9 \text{ krps} = 1.1 \text{ kHz}, \tag{3.116}$$

also as predicted above [92].

Finally, Figure 3-41 shows the step response using a transmitting lamp in place of the FM signal generator. The lamp frequency in this example is modulated between 56.6 kHz and 55.6 kHz by modulating the lamp power between 36.3% and 45.3%.

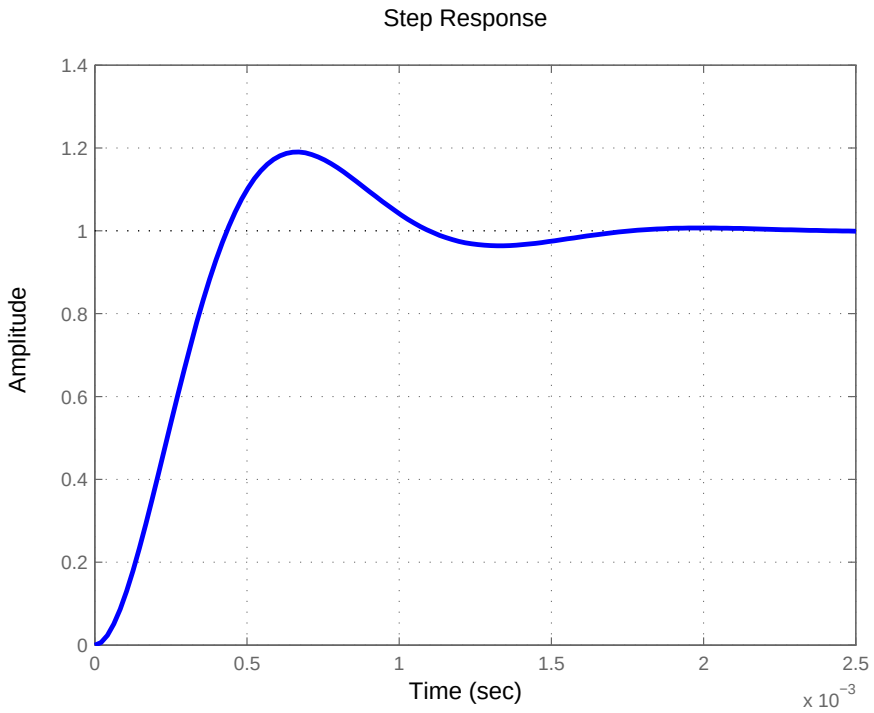


Figure 3-39: Simulated step response from the input signal to the VCO input in the PLL.

The rise time in Figure 3-41 is about 8.24 ms. This corresponds to a bandwidth of

$$\text{BW} = 43 \text{ Hz} \tag{3.117}$$

The PLL design is sufficient because the lamp is clearly the limiting factor in the signal bandwidth.

3.6.8 Wireless Link Demonstration and Range

Figures 3-42(a) and 3-42(b) depict bitstreams transmitted with the wireless link. For the system demonstrated here, the lamp power is modulated between 36.3% corresponding to $f = 56.6$kHz and 45.3% corresponding to $f = 55.6$kHz. These frequency deviations result in peak-to-peak VCO input voltage deviations of 700mV centered on 1.9V near the center of the VCO input voltage range. The output data is available at the comparator output in Figure 3-36(a).

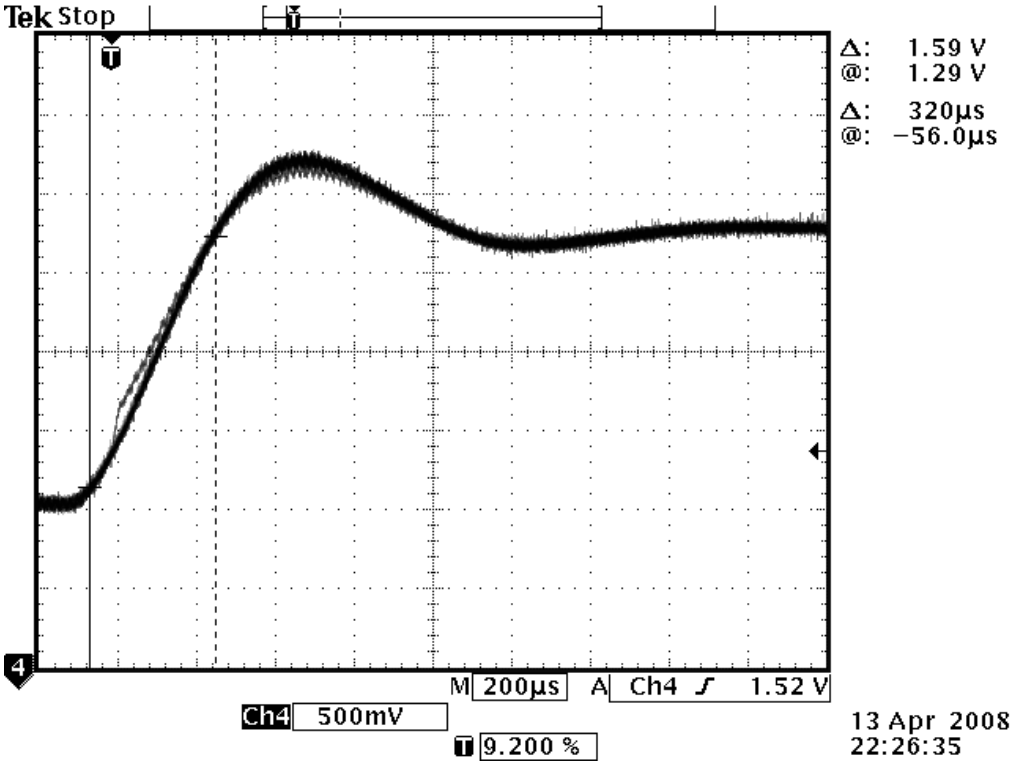


Figure 3-40: Measured step response using an FM-capable Agilent signal generator.

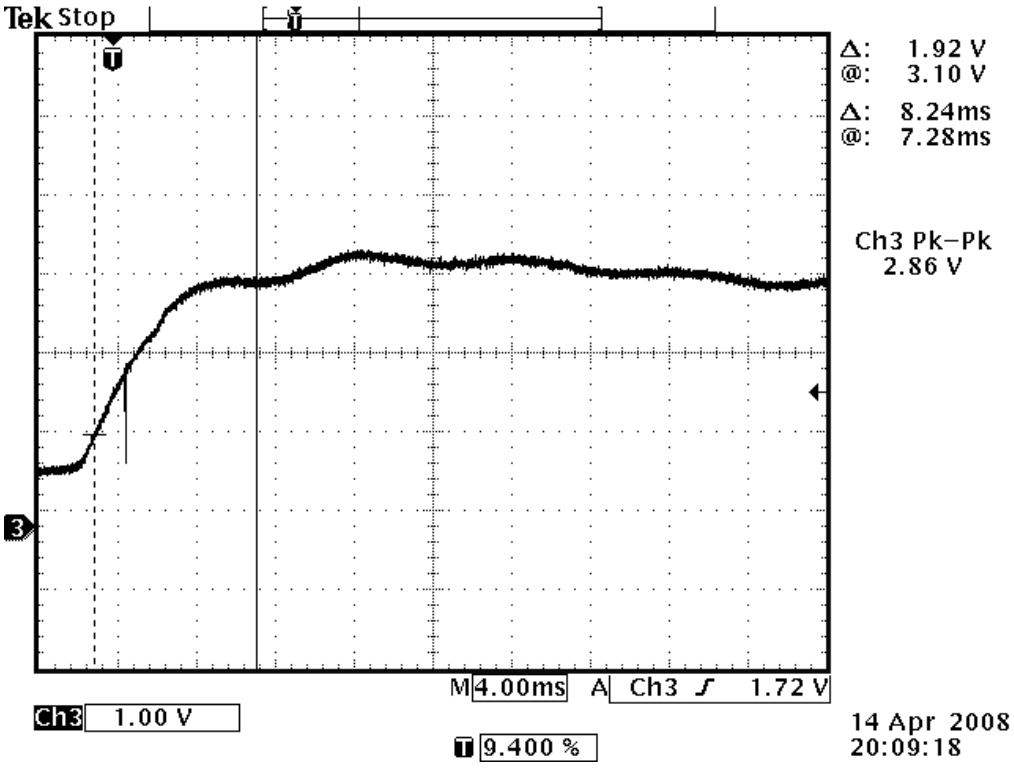
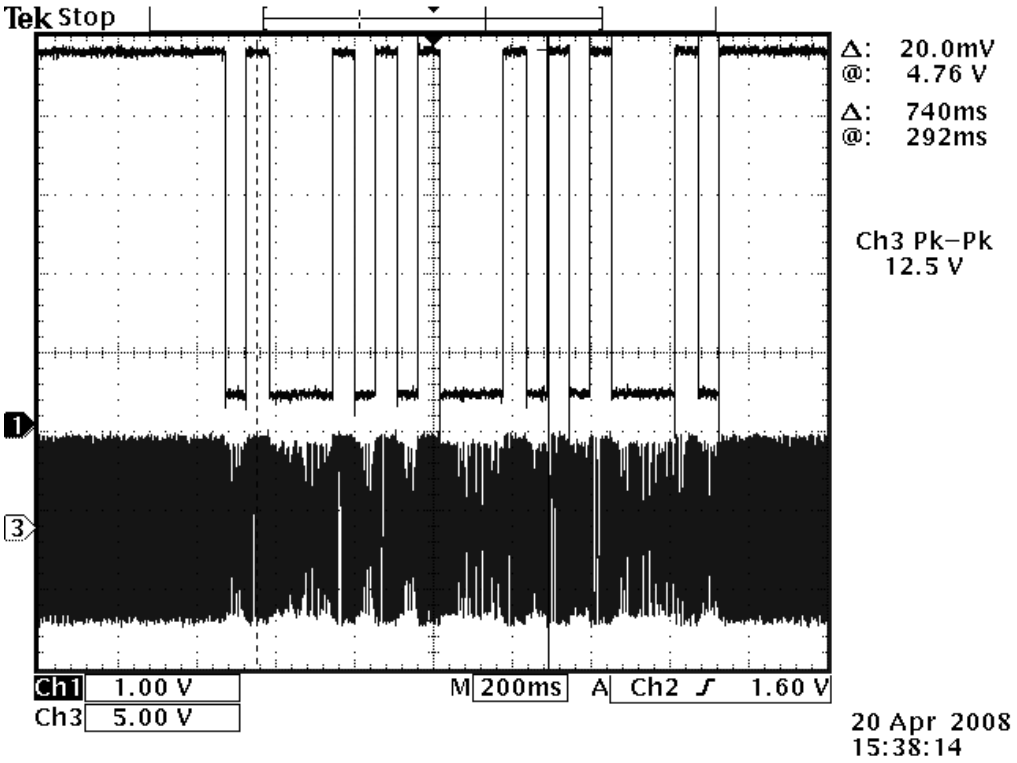
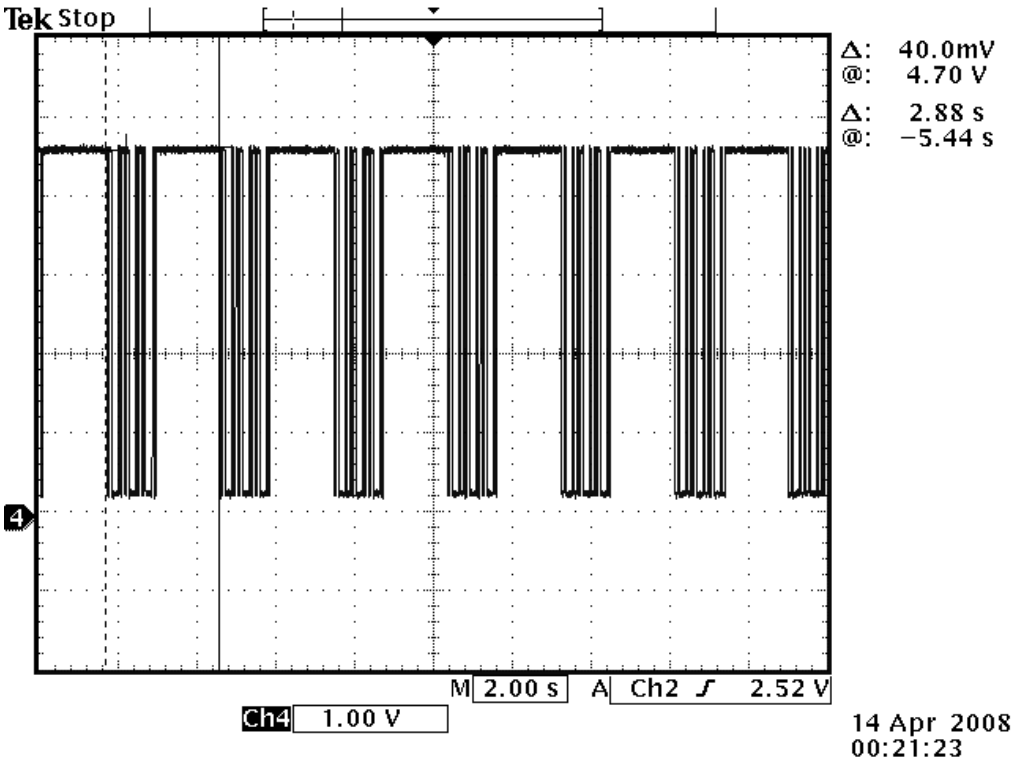


Figure 3-41: The PLL step response with the lamp in the system shows a slower rise time.



(a) A 3-byte long (24-bit) packet transmitted over the wireless link and demodulated by the PLL (top) and frequency modulations are evident in the output of the receiver front-end before demodulation (bottom).



(b) A sequence of 7 3-byte long packets.

Figure 3-42: Wireless link demonstration

The maximum distance between adjacent lamps for proper wireless link operation affects lighting network design. To determine the link range, one lamp was used to transmit data while a receiving electrode was moved away until there were visible bit errors in the received packets. A dummy lamp under the receiving electrode modeled the capacitive structure in a realistic system. As depicted in Figure 3-43, the adjacent lamp end-to-end maximum distance was 3ft. 8in. The range between two parallel lamps (broad-side range) was 2ft. 11in. The 45° range between the nearest corner of the transmitting lamp and the nearest corner of the receiving electrode was 2ft. 3in.

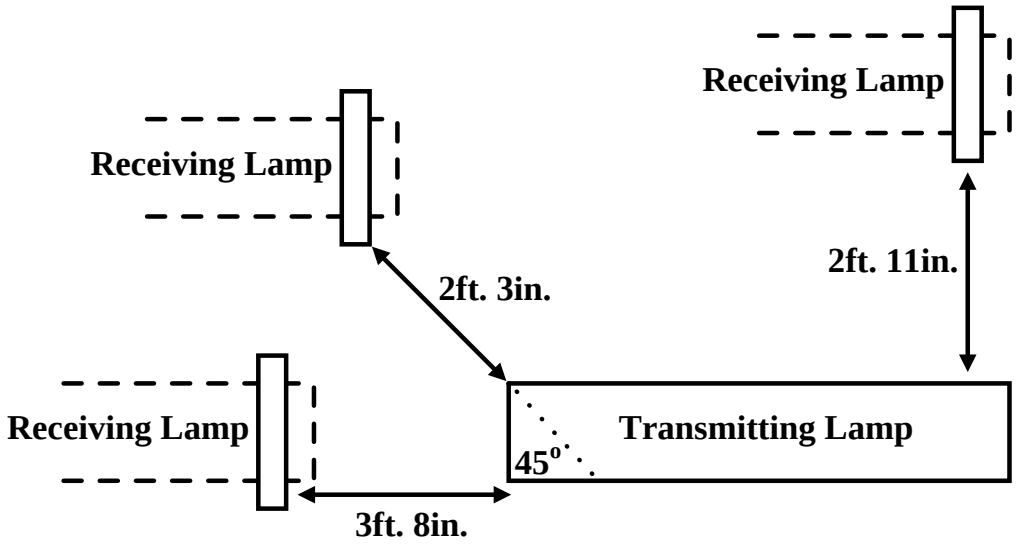


Figure 3-43: The measured wireless link range between the closest edge of the transmitting lamp and the receiving lamp's electrode.

Chapter 4

Dimmable Solid-state Lamp with Integral Occupancy Detection

4.1 Introduction: Energy efficient lighting technology

New illumination sources and new power electronic controls for lighting have the potential to produce energy efficiency gains of 240 percent in the residential sector and 150 percent in the commercial sector [102]. In 2007, lighting accounted for 15.6 percent and 23.3 percent of all electricity consumed in the residential and commercial sectors, respectively, in the USA, [102]. Efficiency gains from lighting sources and active control can substantially reduce overall energy consumption. In particular, solid-state lighting promises improved energy efficiency and long lifetime [103].

A fluorescent lamp with an integral occupancy sensor was demonstrated in [1]. By exploiting the lamp's own stray electric field, the sensor system is able to detect changes in the electric field below the lamp, [**which includes people, or perhaps autonomous mobile robotics that rely on machine vision**]. Unlike standard proximity sensors which require building planners to design for a proximity detection system separate from the lighting system, this proximity sensor is essentially a drop-in replacement for a standard commercial fluorescent lamp ballast.

This chapter describes

- the application of the lamp sensor to a solid-state (LED, i.e. light emitting diode) lighting array that detects occupancy both lighted and in the dark;
- the design and implementation of a wide dimming range LED driver ("ballast") using an inductor pre-charging method that is broadly applicable.

Design considerations for the ballast include those relevant to lighting, such as power efficiency and consistent color cast, or chromaticity, across dimming levels. Although, a hard-switching design using freewheeling diodes is demonstrated in this work, it is possible to use synchronous rectifiers and soft-switching such as in [104–106], to improve efficiency, with a tradeoff of additional active devices and related components. The effects of DC and PWM (pulse-width modulation) dimming has been studied for both RGB (red-green-blue) and phosphor-based LED light sources [107–109]. A PWM technique, which shorts the inductor during off-periods for the LED current is investigated in [110]. Multiple current-level driving techniques are discussed in [111] and [112]; and [113] proposes a hybrid PWM/AM dimming strategy. Not only is the effect of dimming modulation on chromaticity a concern in lighting, but also in LCD backlighting applications [114]. Although this work only discusses operation of the LED driver in the PWM mode, the topology easily allows for operation in similar multi-level schemes where both the peak drive current and duty-cycle can be independently controlled.

A PWM technique for multiple parallel LED strings that operates with power factor correction (PFC) off the AC line is described in [115], and a flyback topology also with PFC is detailed in [116]. If desired, PFC can similarly be applied to the ballast described in this work.

In addition, both the ballast and the LED array topology must be designed to support the lamp sensor electronics by driving the lamp with an alternating current to produce an alternating electric field. The design and implementation of the ballast for the LED lamp is discussed in Section 4.2. Finally, experimental data from the lamp sensor built around the LED lamp are presented and compared to quasistatic

models in Section 4.3.

4.2 Power Electronic LED Drive and Dimming

Power electronic drives represent a significant efficiency improvement over linear power sources. In LEDs, light output is best controlled by regulating current. Some difficulties in using the terminal voltage as the control include a negative temperature coefficient that leads to thermal runaway and a poorly behaved exponential relation to power output.

The salient characteristic of a linear regulator is that a voltage is dropped across an element that continuously carries current, resulting in an inescapable power dissipation. Linear current regulators can use active devices in either open-loop (e.g. current mirror) or closed-loop (e.g. op-amp with a pass transistor). A voltage source with a series resistor is also used in driving LEDs—the underlying approximation is that the voltage drop across the resistor is large, hence approximating a current source, which means that it is guaranteed that power is dissipated as heat by the resistor. This approximation weakens at low current levels when dimming, resulting in a drifting current level and hence light output.

Pulse width modulation of the current is an effective approach to driving an LED. Not only is there an advantage in efficiency, but a number of studies have suggested that there may be an advantage to the quality of lighting [107–109]. There are a number of choices for the design of a switching current source. Our design was based on several requirements, which include a bipolar source for proximity sensing, square current pulses for color quality, and a wide dimming range.

4.2.1 High Brightness LED Modules

Currently, we use commercially available modules with 14 LEDs within a diode bridge. Because these modules were originally intended to replace halogen lighting in low-voltage 60 Hz sockets, slow recovery rectifier diodes were used in the bridge, resulting in voltage waveform distortion and power loss when driven by a high frequency in-

verter. The solution is to use diodes with better recovery characteristics. As we see in the driver design below, the inverter operates at frequencies just above the audio upper limit of about 20 kHz, yet below frequencies where more expensive high performance diodes are needed.

The partitioning of these LEDs into bridged segments is an important consideration for capacitive sensing because it determines the shape of the electric field source. Ultimately, the design may consist of groups of LEDs consisting of fewer diode bridges with a voltage distribution that is optimal for sensing and would result in lower cost. The use of many uniform groups of bridged LEDs provides a proof-of-principle prototype and allows a comparison with previous results using a fluorescent lamp (linear voltage profile) field source [1].

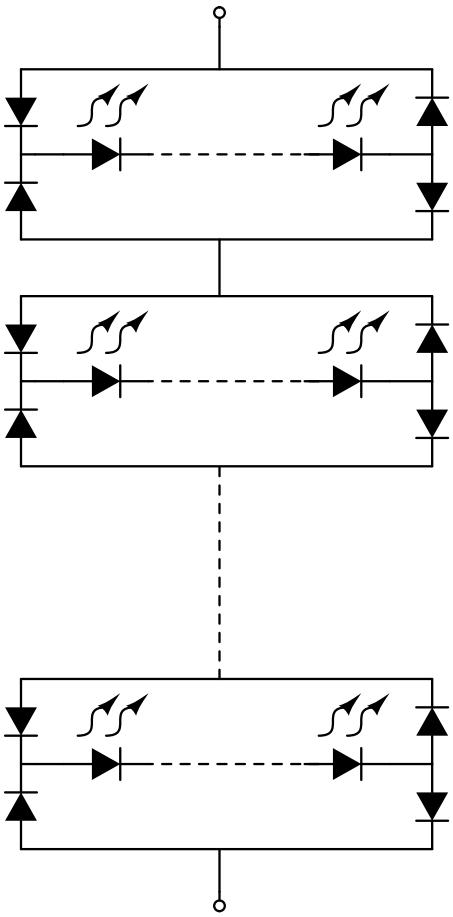


Figure 4-1: Bidirectional LED modules.

4.2.2 Switching Current Source LED Driver

We selected a topology that consists of a buck converter with a hysteretic current controller with a switching frequency in the range of a few hundreds of kilohertz and a post-inverter in the 20–30 kHz range. A hysteretic-controlled, hard-switched converter operating in the hundreds of kilohertz range provides a fast response without having a power efficiency that is overcome by switching losses. By operating the inverter in the 20–30 kHz range, capacitive sensing is effective, without driving too much reactive current into the metal fixture.

A schematic of the power system is shown in Figure 4-2. The circuit is designed to operate from a 170 V DC bus (nominal rectified line voltage) driving two parallel strings of 40 mA AC LED modules anti-symmetrically, which are illustrated in Figure 4-1. The DC bus can of course be derived from an AC front-end, and can tolerate variable levels of ripple to provide a complete ac-ac ballast solution. By operating the buck converter in the continuous inductor current mode, nearly square pulses of current are provided by the inverter to the LEDs, which has been suggested to help maintain consistent chromaticity, or "color-cast" [107–109]. An advantage to this topology is that it is possible to independently control both peak and average LED current, which is useful in multi-level driving schemes, while maintaining a constant brightness. The peak current is controlled by the buck converter and the duty cycle by the full bridge.

Because the full-bridge inverter is driven by a current source with free-wheel diode, D_2, no dead-time circuitry for the switches is necessary, which simplifies the design. Placing the current sense resistor at the bottom of the bridge enables ground-referenced measurement of the inductor current, which is easier than high-side differential measurements, or switch current measurements which tend to be corrupted by transients from gate drive charge injection or switch capacitance. Transformer T_1 is a $1:1$ provides galvanic isolation from the mains for safety and additionally allows one to choose a potential reference (e.g. fixture ground), which may result in an improved sensitivity in the lamp sensor.

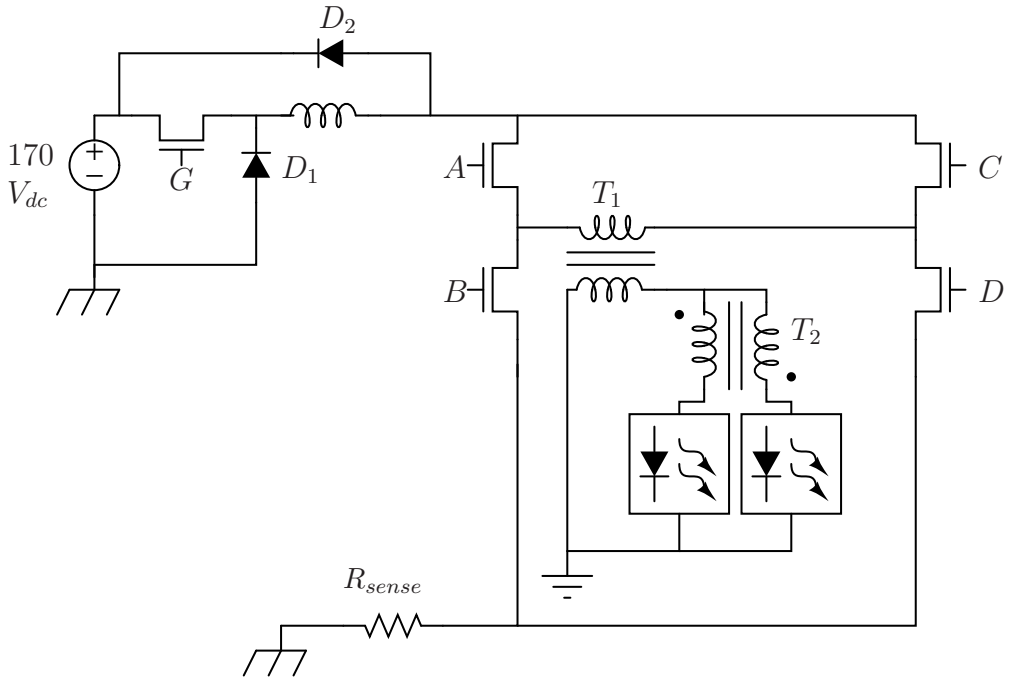


Figure 4-2: Schematic of the bipolar LED driver. Transformer T_1 isolates the inverter output. Transformer T_2 matches the currents between the two LED bulbs.

An advantage to using AC to drive the LEDs is the ability to use low-cost transformers to enforce current sharing among parallel lamps at good power efficiency. Transformer T_2 is a small current balancing transformer, similar to those that are used in fluorescent lamp ballasts. The volt-second demands on this transformer are small because they corresponds to the ensemble average of diode voltage mismatches among LEDs in each string.

4.2.3 Dimming and Inductor Pre-Charging

Dimming is performed by symmetric tri-state PWM at the inverter. There is a challenge in maintaining efficiency at high dimming (low-light) levels, where the duty cycle is small. Conduction losses dominate if the converter is run continuously, but alternatively, there are higher switching losses for on-off operation of the converter because square current pulses cannot be achieved without a high switching frequency. Square current pulses means a high current slew, which for on-off operation means that for a fixed input voltage, a small inductor value along with continuous inductor

current is necessary, hence a high switching frequency.

$$V_{input} = L\frac{dI_L}{dt} \propto L\Delta I_L f_{sw}, \tag{4.1}$$

where ΔI_L is the inductor current ripple and f_{sw} is the switching frequency.

We developed a driving method to help overcome the challenge of efficient dimming at reasonable frequencies for hard switching, using a relatively simple converter and control scheme, which is typically a factor in lowering cost.

4.2.4 Control Circuit Implementation

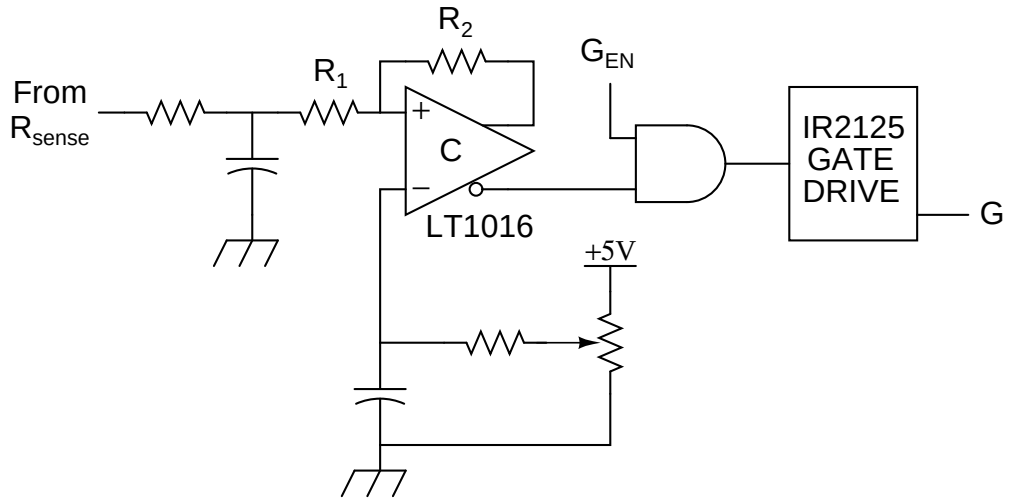


Figure 4-3: Hysteretic Current Controller.

The schematic for our hysteretic current-mode buck converter controller is shown in Figure 4-3. A reference voltage to match the desired current (expressed as a voltage across the current-sense resistor, R_{sense}) is set with a potentiometer at the inverting input of a high-speed comparator. A positive feedback loop splits this reference into two hysteresis bands, which can be determined through superposition of the comparator output and the voltage across the current-sense resistor, V_{sense}: when the comparator's non-inverting output is *LOW* (0V),

$$V_+ = V_{sense}\frac{R_2}{R_1 + R_2} \tag{4.2}$$

and, when the comparator's non-inverting output is $HIGH$ (5V),

$$V_+ = V_{sense}\frac{R_2}{R_1 + R_2} + V_{out}\frac{R_1}{R_1 + R_2} \tag{4.3}$$

The spread of these hysteresis bands is therefore equal to the difference between these two terms:

$$\text{Hysteresis Spread} = H_+ - H_- = V_{out}\frac{R_1}{R_1 + R_2} \tag{4.4}$$

Since typically $R_2 \gg R_1$, V_- will approximately set the top hysteresis band, with the bottom hysteresis band $V_{out}R_1/(R_1 + R_2)$ below.

We set the potentiometer to obtain current regulation at 80mA (for two LED strings at 40mA each). We set the hysteresis spread to correspond to a 10% current ripple, with an R_{sense} of 10 Ω:

$$H_+ - H_- = R_{sense}\Delta i = 10\ \Omega \cdot 8\ \text{mA} = 80\ \text{mV} \tag{4.5}$$

Example control waveforms are shown in Figure 4-4.

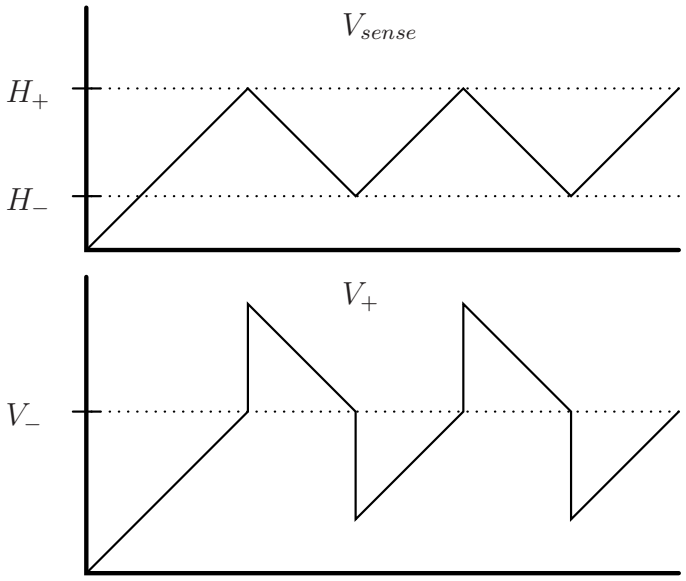


Figure 4-4: Example Hysteretic Controller Waveforms. Top: Current-sense voltage V_{sense}. Bottom: Comparator non-inverting input V_+.

A first-order low-pass filter is placed on the current-sense input to attenuate

switching transients and prevent erroneous transitioning.

The gate enable (G_{EN}) signal is controlled by a DSPIC33FJ2560GP710 microcontroller. This signal can be used to break open the control loop and shut down the buck converter during the off-duty periods in between PWM pulses to recover inductor current.

4.2.5 Symmetric Tri-State Pulse-Width Modulation

The switching pattern of the inverter generates a bipolar pulse-width modulated current through the LED strings in which the individual pulses alternate in polarity with each pulse, so there is zero DC current offset. Light output is controlled by modulating the duty of these bipolar pulses. This is known as "symmetric tri-state pulse-width modulation". Typical symmetric tri-state PWM waveforms can be seen in Figures 4-7 and 4-5, labeled "LED Current".

We execute symmetric tri-state PWM using two modes, depending on duty ratio. These two modes are continuous current mode (performed at high duty cycles greater than 60%) and pre-charge mode (performed at low duty cycles below 60%). Each mode is implemented in such a way as to preserve square current pulses through the LEDs in order to **[improve]** color quality.

Continuous Current Mode

In continuous current mode the control circuit shown in Figure 4-3 is run constantly ($G_{EN} = 1$ always). This means that during the off-duty period between pulses, the buck converter continues to regulate its current, which is shunted through a short consisting of two inverter switches in series: either A and B or C and D, with the corresponding complementary switches off. Keeping the buck in a continuous current-regulating state allows square LED current pulses without the need for a very large inductor di/dt. This way, we can still maintain tight current regulation using a large inductance at the buck output.

Figure 4-5 shows the switching pattern at high duty cycle when continuous induc-

tor current is used. Figure 4-6 illustrates the median-filtered results at 96% inverter duty-cycle, where the ballast is operating in continuous current mode. *End-to-End Lamp Voltage* is the differential voltage across a single LED string. *LED Current* corresponds to the primary current of T_1 and closely represents the sum of the currents into the two parallel LED strings. A filtered version of *Clock*, with the spikes from switching transient pickup eliminated, is used for synchronization by the lamp sensor.

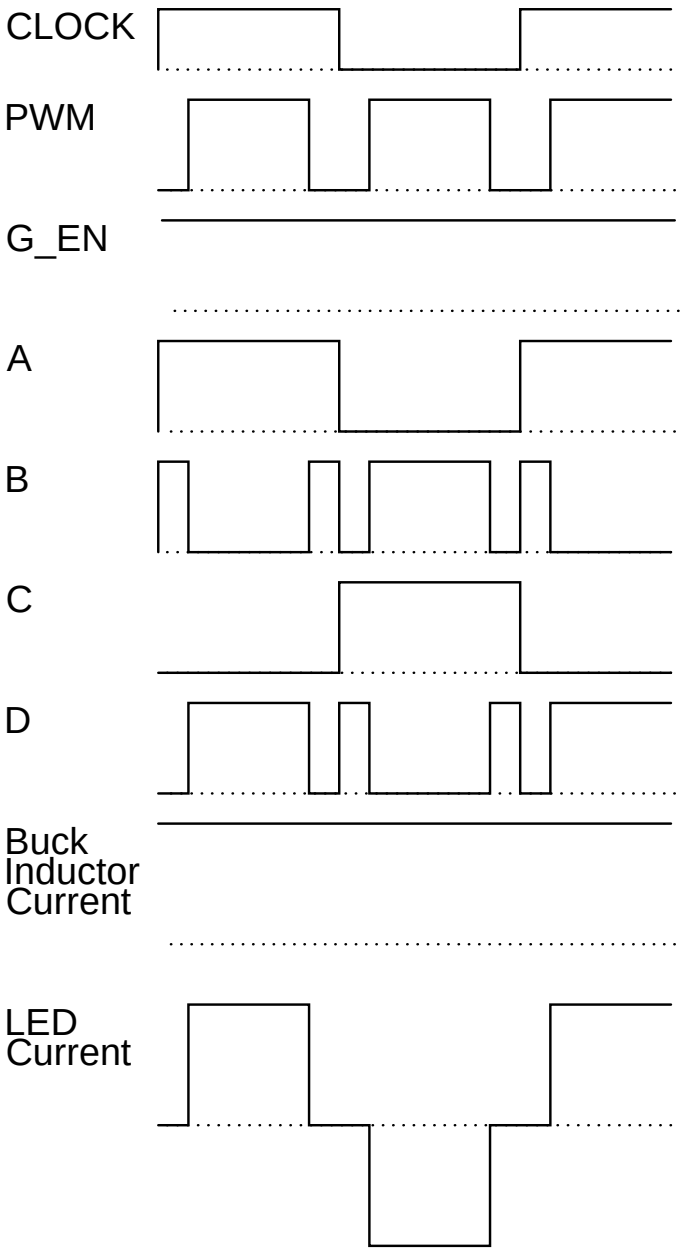


Figure 4-5: Timing Diagram Using Continuous Inductor Current.

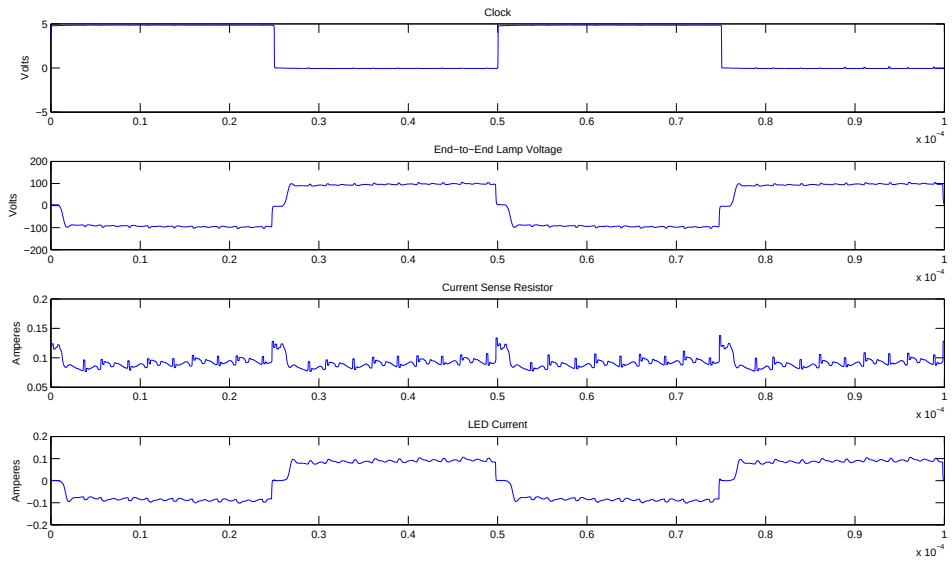


Figure 4-6: Waveforms at 96% Duty-Cycle with Continuous Inductor Current.

Pre-Charge Mode

At low duty ratios, there is enough time during the off-duty periods between pulses to turn off the current controller and recover inductor current. This is done by setting the gate enable (G_{EN}) signal OFF, which opens up the current control feedback loop. All switches in the inverter are likewise turned OFF. This turns diode D_2 ON, hence recovering inductor current. In order to maintain a square LED current, we pre-charge the inductor prior to inverter turn-on by letting the buck converter regulate into the short created by turning ON either A and B or C and D, with the complementary inverter switches OFF. Shorting the output of the buck converter in this way results in the fastest pre-charge for any given input voltage:

$$T_{rise} = LI_{pk}/V_{in} \tag{4.6}$$

Where T_{rise} is the rise time of the buck converter output current and L is a conservative estimate of the inductor value for all operating points and V_{in} is the input DC voltage to the buck converter, which could either be measured by the microcontroller, or set for worst-case low-line voltage. Note that the inductor fall

time during energy recovery is also equal to T_{rise}.

Figure 4-7 shows the pre-charge mode switching pattern. Figure 4-8 shows the median-filtered, low duty cycle waveforms where the ballast is operating in pre-charge mode. The *Current Sense Resistor* waveform is the current through the resistor at the bottom of the full-bridge, which represents the inductor current when the bridge switches are conducting.

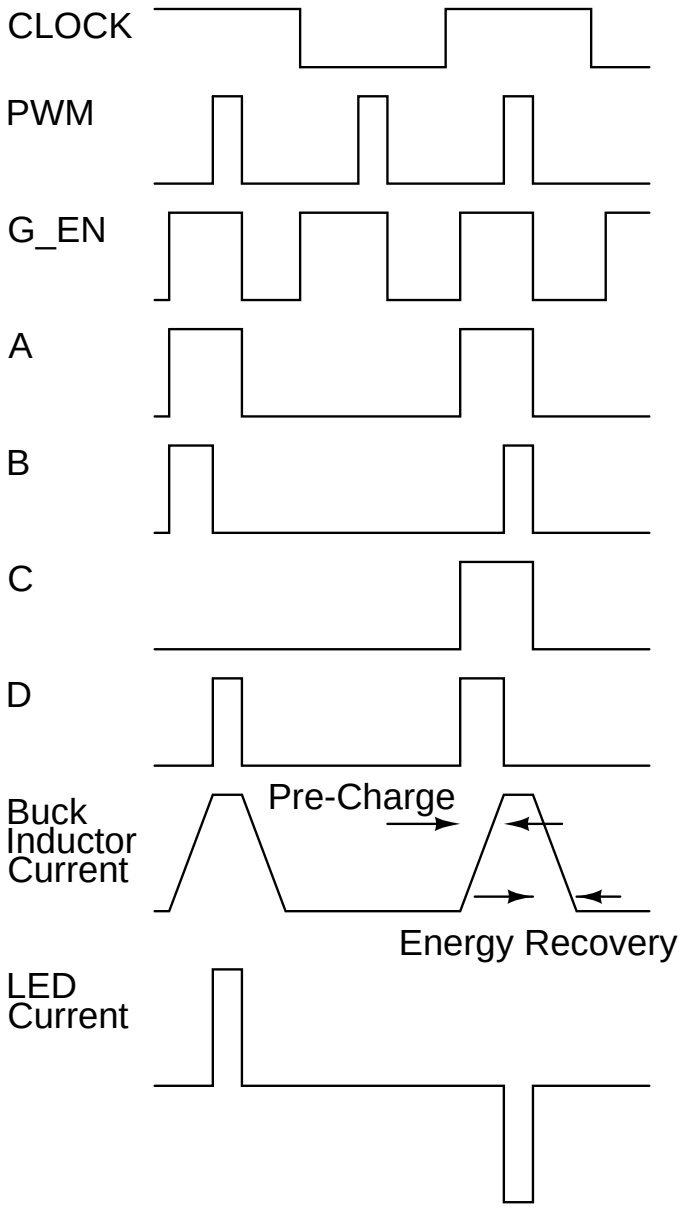


Figure 4-7: Timing Diagram Using Inductor Pre-Charging [**and Energy Recovery.**]

By turning off the buck converter and recovering the inductor current, conduction

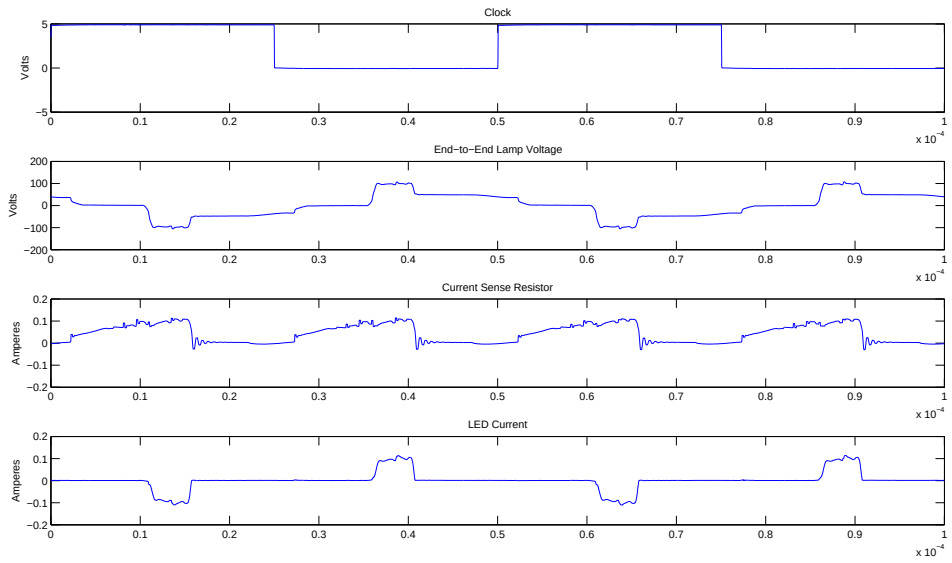


Figure 4-8: Waveforms at 10% Duty-Cycle with Inductor Current Pre-Charge.

losses are reduced for low duty ratios ($D < 60\%$). Pre-charging has the same advantage of allowing for a square LED current without needing a very large inductor di/dt, allowing us to utilize a large buck output inductance for tight current regulation, obviating the need for a very high switching frequency and the associated switching losses.

4.2.6 Logic Generation

The inverter switching patterns and the gate enable signal are generated by a DSPIC33-FJ2560GP710 microcontroller in combination with a fast programmable logic device (PLD). The microcontroller produces three signals: CLK, PWM and gate enable (G_{EN}). CLK controls the ballast operating frequency and corresponds to an internal clock that determines the polarity of the inverter, while PWM controls the duty ratio. G_{EN} turns on and off the hysteretic current controller for the buck converter, thereby setting the operating mode: continuous current ($G_{EN} = 1$ always) or inductor pre-charge. When operating in pre-charge mode, the duration of the G_{EN} pulse before the PWM pulse sets the pre-charge time.

The signals CLK, PWM, and G_{EN} are fed into the PLD, which generates the

MCU Signals			PLD Signals				Status
CLK	*PWM*	G_{EN}	**A**	**B**	**C**	**D**	
1	0	0	0	0	0	0	LED OFF
1	0	1	1	1	0	0	Pre-Charge
1	1	1	1	0	0	1	LED POS Current
1	0	0	0	0	0	0	LED OFF/Discharge
0	0	0	0	0	0	0	LED OFF
0	0	1	0	0	1	1	Pre-Charge
0	1	1	0	1	1	0	LED NEG Current
0	0	0	0	0	0	0	LED OFF/Discharge

Table 4.1: Truth table of all possible logic states.

drive signals for the four inverter switches (A, B, C, D) according to a truth table, shown above as Table 4.1. The logic states shown in Table 4.1 are listed in the sequence in which they would occur when operating in inductor pre-charge mode. Although, the switching patterns are creating using a microcontroller and PLD for research purposes, the logic table can easily be implemented as a simple state machine in a range of low-cost, high-volume technologies.

4.2.7 Analysis of Power Electronic Losses

Table 4.2 illustrates power loss calculations of the hard-switched/pre-charging method used in this work in comparison to maintaining the inductor current through a short through the inverter bridge similar to [110]. In addition, the decrease in power loss by using either synchronous rectifiers, or soft-switching alone along with pre-charging is investigated. The calculations are based on IRF740 MOSFETs and MUR120 diodes. The buck inductance (L) is 10.2 mH with a DC resistance (R_{dcL}) of 10 Ω. The flat-top current (I_{peak}) to the LEDs is 80 mA with 8 mA of ripple, which results in a buck switching frequency (f_s) of 216 kHz with an inverter frequency (f_{si}) of 25 kHz. The input (V_{in}) is 170 Vdc and the output LED voltage is 150 Vdc.

The main advantage of the pre-charge/energy recovery technique in comparison to only shorting the inductor is in the reduction of losses from the buck inductor at

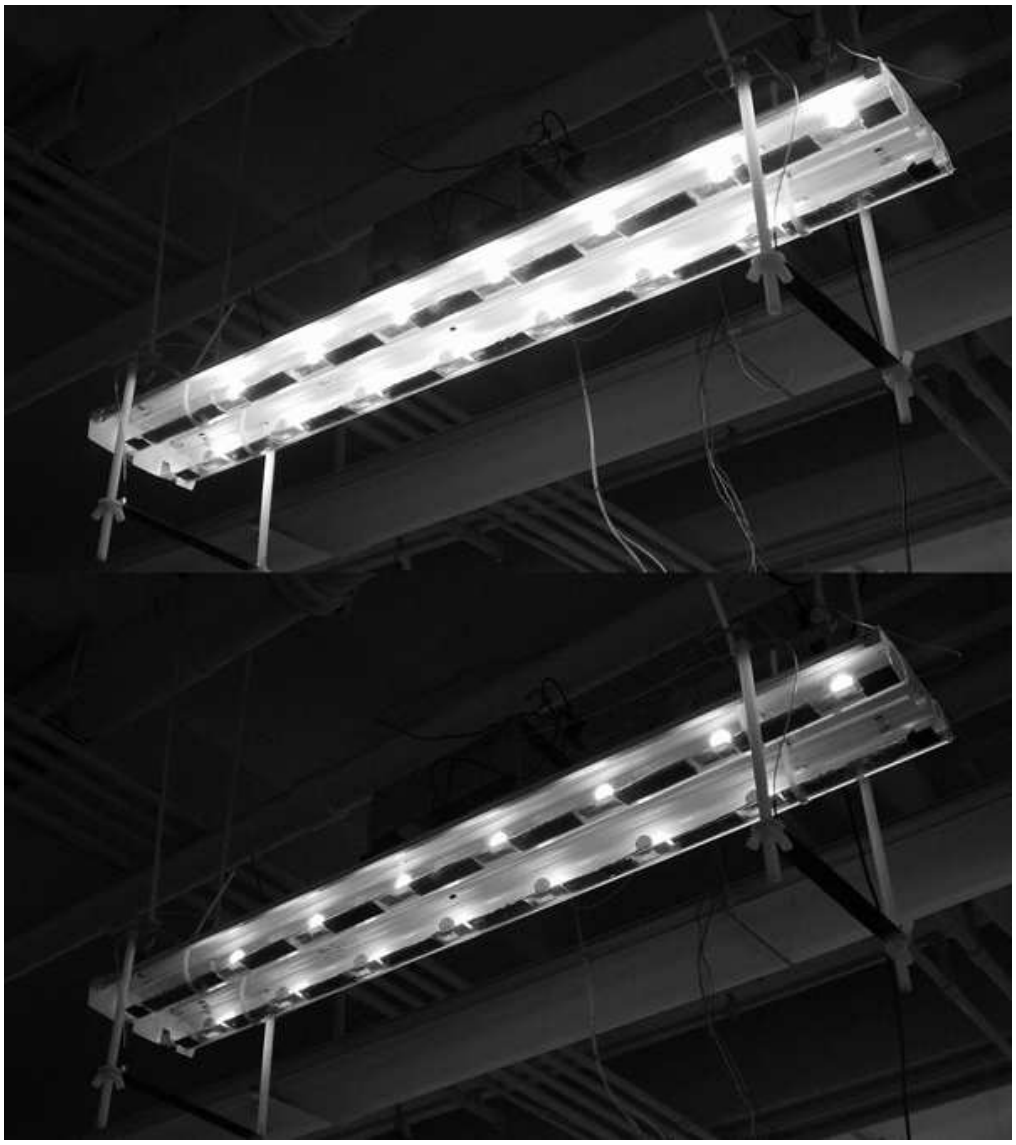


Figure 4-9: A photograph of the LED lamp. Top: bright, Bottom: dim.

low light dimming levels. The additional losses from each pre-charging, or energy recovery are mainly by the diode conduction during current ramp up, or down,

$$P_{pc} = \frac{1}{2} V_{diode} I_{peak} T_{rise} f_{si}.$$

These additional losses when instead, using a synchronous rectifier are dominated by the inductor during the current ramping period,

$$P_{pc} = \frac{1}{3} I_{peak}^2 R_{dcL} T_{rise} f_{si},$$

which might be slightly underestimated because the DC resistance is used, but is still useful in highlighting the improvement over only shorting the inductor. In the calculation of the inductor loss during the operation of the buck converter, the DC resistance is a good approximation in the continuous current mode with small inductor ripple.

The transition switching losses for the MOSFETs were calculated using linear ramp approximations of voltage and current [117], and the gating loss using a 12 V gate drive. The main switching loss mechanism, which can be eliminated by soft-switching, is the charge stored in the output capacitance in the buck MOSFET, that is dissipated every cycle the MOSFET turns on,

$$P_{cout} = \frac{1}{2} C_{out} V_{in}^2 f_s,$$

Different conversion efficiencies are given only as an index for comparison because only relevant, or dominating loss mechanisms are considered. Several tradeoffs can be made to improve efficiency. For example, lower current MOSFETs with higher on-resistance, but lower output capacitance and gate drive charge might be used instead of the IRF740. Also, a physically larger inductor with lower losses might be used, but this would impact power density. The purpose of the power electronic design is to provide a ballast, which supports proximity sensing, that can be modified to take into consideration the many requirements for a particular lighting use case.

4.3 Experimental Setup and Results

The experimental setup of the LED lamp and lamp sensor electronics is shown in Figure 4-10. The lamp sensor output was measured as a conducting sphere (the target) was passed under the lamp. Data was taken with the target fixed at 20 cm intervals in the y-dimension as depicted in Figure 4-10. For each interval, the lamp sensor output data was averaged for 20 seconds. The experiment was iterated for three lamp power settings “bright” (Duty ratio of 96%), “medium” (Duty ratio of 60%)”,

	Shorting Inductor		Proposed Pre-Charging		Synchronous Rectifier		Soft Switching		Units
Dimming Duty Cycle	*95%*	*10%*	*95%*	*10%*	*95%*	*10%*	*95%*	*10%*	
Buck Converter									
Low-side Diode/MOSFET	5.4	0.6	5.4	0.6	0.4	0.04	5.4	0.6	mW
Inductor	64	64	64	6.4	64	6.4	64	6.4	mW
High-side MOSFET									
Switching Losses									
Transition	59	5.9	59	5.9	59	5.9	0	0	mW
Output Capacitance	375	38	375	38	375	38	0	0	mW
Gating	125	13	125	13	125	13	125	13	mW
On Resistance	3	0.4	3	0.4	3	0.4	3	0.4	mW
Current Sense Resistor	64	6.4	64	6.4	64	6.4	64	6.4	mW
Inverter									
Switching Losses									
Transition	6.8	0.7	6.8	0.7	6.8	0.7	0	0	mW
Output Capacitance	43	4.3	43	4.3	45	4.3	0	0	mW
Gating	14.4	14.4	14.4	14.4	14.4	14.4	14.4	14.4	mW
On Resistance	7	7	7	0.7	7	0.7	7	0.7	mW
Precharge/ Energy Recovery									
Diode/MOSFET									
Conduction Loss			0	11.5	0	0.6		11.5	mW
Inductor			0	2.6	0	2.6		2.6	mW
Total Loss	767	160	767	104	761	92	282	55	mW
Power Delivered	11.4	1.2	11.4	1.2	11.4	1.2	11.4	1.2	W
Dc-to-Output Efficiency	93.7%	88%	93.7%	92%	93.7%	92.9%	97.6%	95.6%	

Table 4.2: Power Electronic Loss Comparisons

and "dim" (Duty ratio of 20%). A photograph of the lamp under the "bright" and "dim" settings is shown in Figure 4-9. The experiment was also repeated for three x-displacements: 0 cm, 22 cm, and 45 cm.

The analytical approach described in reference [118] was also used to model the lamp sensor system. The electrostatic model of the lamp sensor consisted of conducting spheres representing the source nodes, electrodes and the target. The calculated difference between the electrode potentials was taken to be proportional to the output of the lamp sensor. Also, the floor was taken to be a conductor, so the model also consisted of image spheres below the plane of the floor. Finally, the potential of the "Lo" source nodes and of the plane of the floor was assumed to be earth ground.

To compare the analytical approach to measured data, the signal source parameters used in the electrostatic model were first calibrated. A "training run" consisted of taking measured data from the lamp sensor for known x and y displacements. Then, an iterative least-squares optimization method was used to infer the effective signal source parameters based on the measured data.

In the least-squares optimization method, the signal source parameters were first

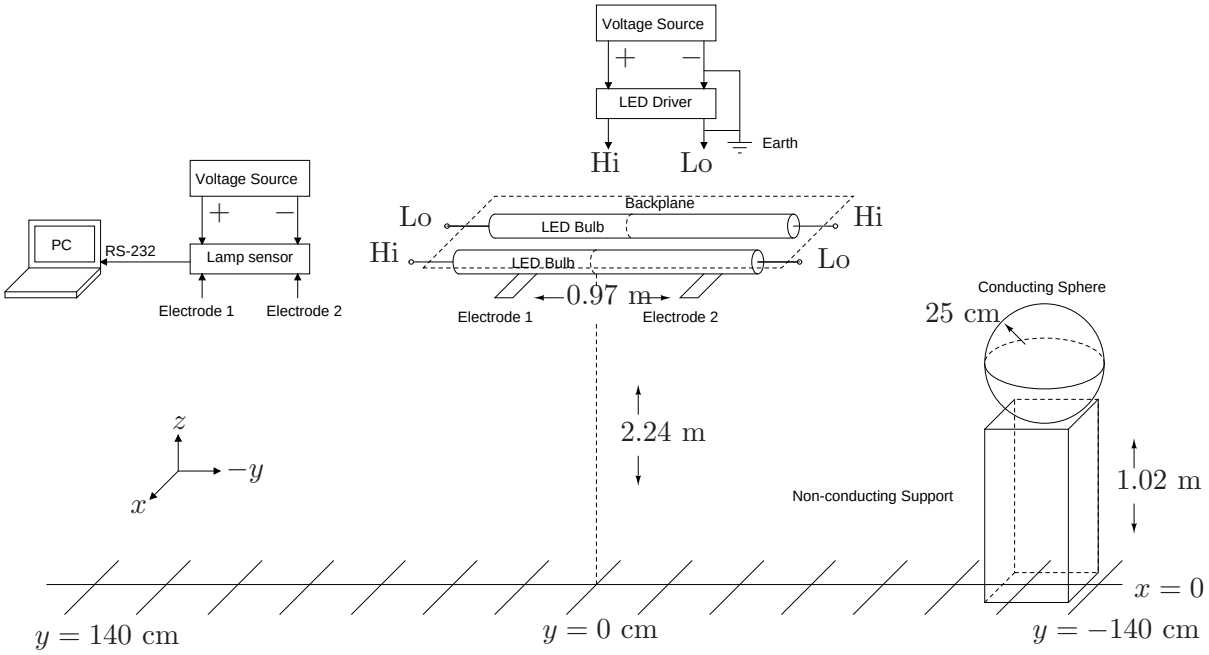


Figure 4-10: The experimental setup.

guessed. Then, the results of predicting the lamp sensor output using the electrostatic modeling approach from reference [118] and the guessed signal source parameters were compared to the measured data. Depending on the squared error between the predicted and measured data, the signal source parameters were perturbed and the process was repeated. This iterative process continued until the squared error between the predicted and measured lamp sensor output were less than a certain threshold. The signal source parameters from the last iteration were then taken as the actual effective signal source parameters in the lamp sensor system.

The measured and fitted data in Figure 4-11 correspond to training runs for each of the three lamp power settings. For each lamp power setting, we have different effective signal source parameters. Those effective signal source parameters were used to predict the lamp sensor response for different x-displacements. Figures 4-12(a), 4-12(b), and 4-12(c) compare those predictions to measured lamp sensor data at x-displacements of 22 cm and 45 cm for each of the three lamp power settings (dim, medium, and bright). The results in Figure 4-12 show that the modeling approach described in reference [118] yields predictive power for design-oriented estimation of the lamp sensor output voltage in response to a target.

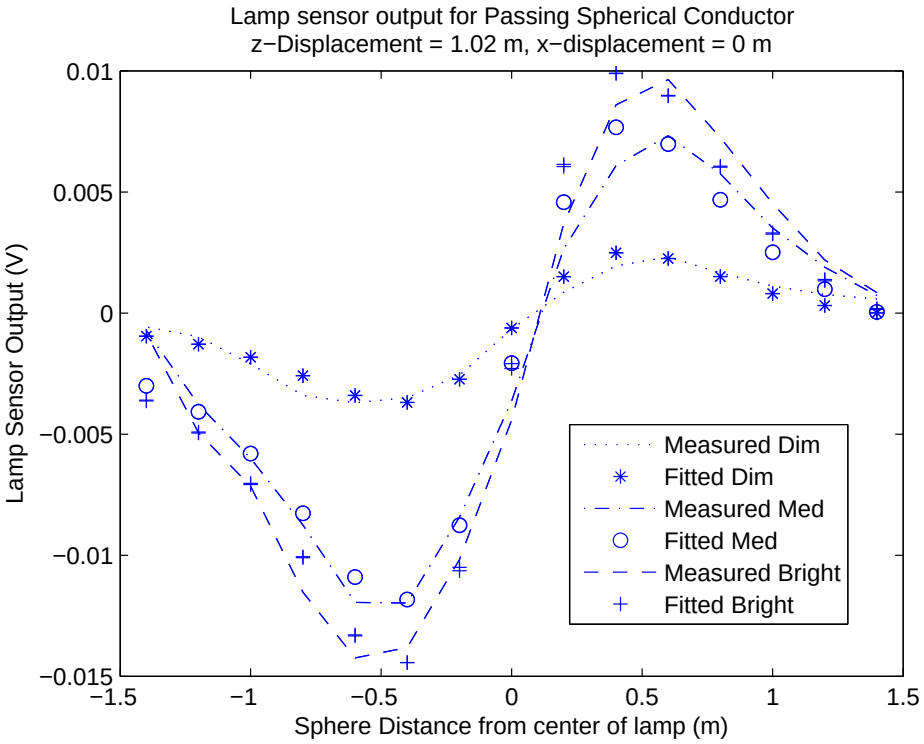
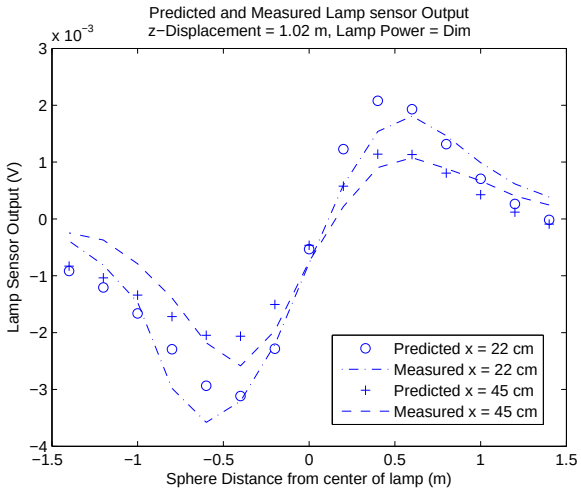
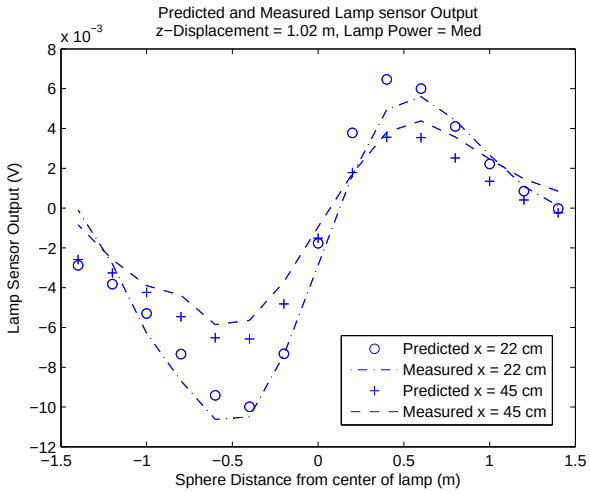


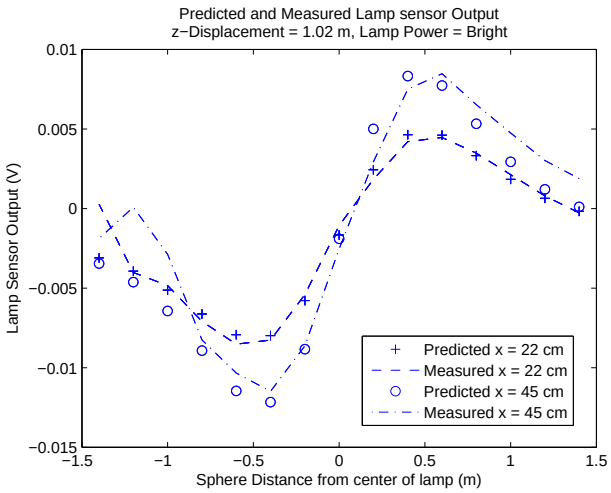
Figure 4-11: Training runs (source calibration) $x = 0$ cm



(a) Dim



(b) Medium



(c) Bright

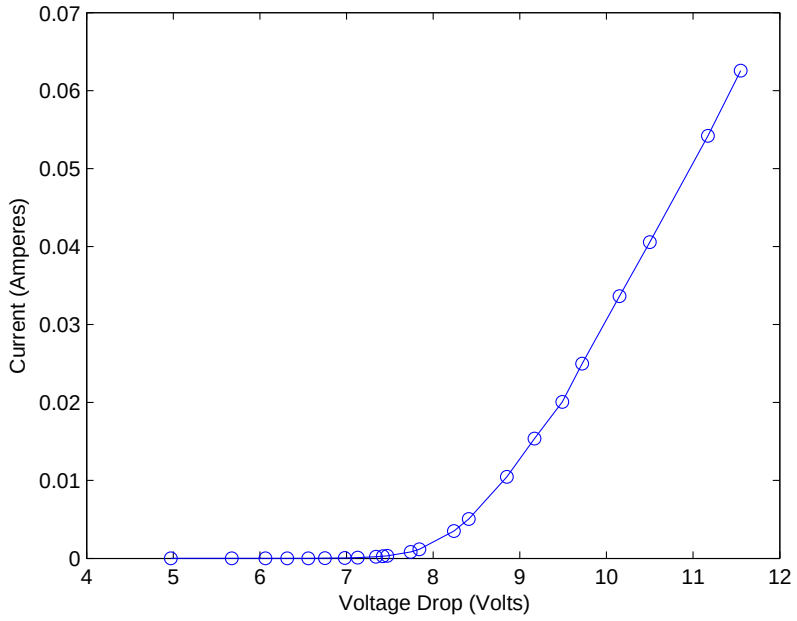
Figure 4-12: LED lamp sensor measured and predicted responses.

4.3.1 Dark Occupancy Sensing

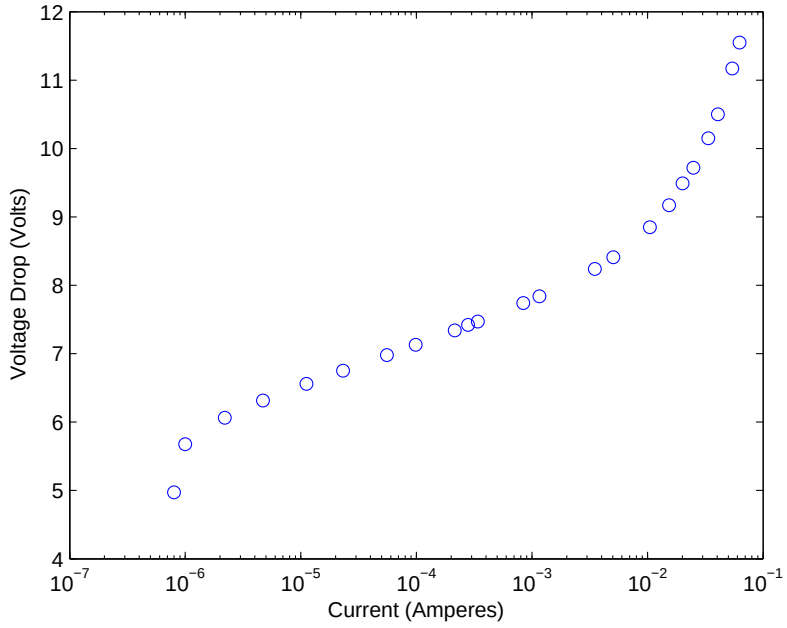
In this section, we address the ability to sense occupancy in the dark, which is relevant to the use cases such as entry into a dark room. In this section, we demonstrate excellent occupancy sensing at very low LED current levels. In fact, from the brightest to essentially dark there is about a three order of magnitude difference in power level, yet the electric field source for sensing drops by only a factor that is less than a half.

In Figure 4-8, a duty-cycled LED current also results in the lamp voltage also pulsating. This voltage is proportional to the electric field that drives the lamp sensor. From Chapter 3, the signal that is detected is an averaged magnitude that is proportional to the duty cycle. This means that as the lamp is dimmed, the sensor voltage output decreases proportionally, which can be observed in Figure 4-11. Despite the decreased voltage levels, the output voltage is above the noise floor for a wide range of dimming levels.

A special case arises in dark occupancy sensing, when one is no longer concerned about maintaining a constant peak LED current, hence relaxing the consideration for chromaticity. In this case, the LEDs are run at very low current levels at 50% duty cycle. This is advantageous, because as we observe in Figure 4-13(b), the voltage drop across one LED module changes roughly logarithmically with current. This means that most of the voltage that drives the sensing is maintained at very small current levels using the maximum available duty cycle, which results in the largest output voltage signal when using the demodulation scheme discussed in Chapter 3.



(a)



(b)

Figure 4-13: I-V curve of LED lamp module. (a) is the classic diode characteristic, but closer inspection of the log plot in (b) reveals the non-idealities in real devices.

The result for sensing in the dark is compared to sensing at moderate lighting levels in Figure 4-14. A careful comparison shows that there is actually an increase in the output signal at low LED current levels. This may be attributed to a shift in the electric field distribution from the LED lamps as we vary from low to high currents. At low current levels, the shape of the electric field is dominated by parasitic capacitances from the modules to the housing, as well as the capacitances associated with LEDs at small bias. At higher current levels, the effective resistance of the LEDs decreases, which results in a different type of distribution. The dynamics and geometry of this process is complicated and is currently under investigation.

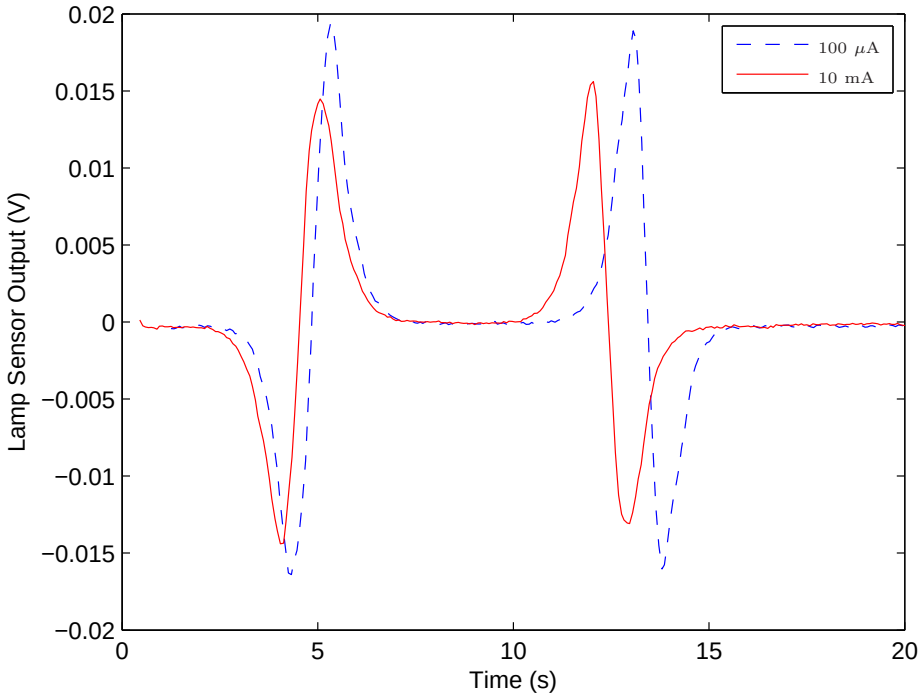


Figure 4-14: Comparison of capacitive sensor output at dark (100 μA) and lighted (10 mA) LED current levels for an average height subject walking back and forth along the axis of the lamps.

4.4 Conclusion

Reference [119] is one of many references that discusses curtailed demand and its value in the energy market. In curtailed demand, the supply company reduces the

effective energy demand by reclaiming unused or wasted energy. Reference [119] cites the sophisticated planning and knowledge of building characteristics necessary to implement curtailed demand and suggests that it can only be effective if "sensing and switching can be done cheaply" and with "a high level of automation." In particular, there is a great interest in controlling lighting to optimize energy consumption. Lighting in commercial and residential spaces consumes a significant portion of the end use demand for delivered energy in the United States. In 2005, lighting consumed 0.73 Quadrillion Btu (QBtu) in the residential sector and 1.18 QBtu in the commercial sector [120].

This work has presented a ballast or solid-state lamp driver that is suitable for dimmable operation of solid-state or LED lighting. The ballast design permits the possiblity for chromaticity control even at lower switching frequencies for the power electronic current drive, which results in the ability to use hard switching as opposed to resonant topologies, hence resulting in a relatively simple converter and control scheme. The ballast described in this work also creates the correct lamp current waveforms to permit a solid-state lamp to function effectively as a proximity sensor for occupants, not just for motion as is typically deployed today. This opens the door to distributed, autonomous control for lighting. That is, light fixtures can automatically alter their illumination based on the presence or absence of occupants, and any other important environmental variables such as time of day, through the actions of an embedded controller. The proximity sensor does not require motion or other intrusive occupant behavior to function. It is sensitive directly to the dielectric presence of an occupant. Interfacing the lamp sensor with a dimming ballast creates a smart auto-dimming lamp that can use the lamp sensor's occupancy detections to appropriately dim or brighten.

This work has also demonstrated an electro-quasistatic model that accurately predicts the behavior of the proximity sensor for both fluorescent and solid state lamps. The model can be used by building designers to predict detection range given a particular configuration of luminaire. It can also be used to select a luminaire design to achieve needed detection range.

The incorporation of automatic proximity detection in solid state lighting could be a "game changing" addition to solid-state lamps that accelerates their acceptance.

Chapter 5

Standalone Capacitive Sensing Occupancy Detectors

5.1 Introduction

This chapter explores capacitive sensing occupancy detectors that rely on their own source of electric fields. The principal advantages of these "standalone occupancy detectors" are that the signal source may be well controlled and optimized for sensing and that the electrode and source configuration may be customized. The principle drawbacks of the standalone occupancy detectors relative to retrofit systems like the one in Chapter 3 are that the signal source and source coupling surfaces must be provided. The underlying motivation of this work is to provide a superior replacement to PIR motion sensors like the one in Figure 5-1. The capacitive sensor would resemble the PIR motion sensor in both form and function, but would provide true presence detection. Recall from Chapter 3 that the ability of a PIR sensor to function as a presence detector is limited by low-frequency noise or drift from changes in background infrared radiation (IR). The measured signals can be bandlimited (high-pass filtered), but the sensor effectively becomes a motion sensor, not a presence sensor [69, 70].

The signal conditioning electronics from the fluorescent lamp sensor in Chapter 3 are reused in the standalone system. The analytical modeling of the fully-differential front-end amplifier from Chapter 2 is directly relevant to the operation and modeling

Figure 5-1: The capacitive sensor would resemble the PIR motion sensor in both form and function, but would provide true presence detection.

of the system in this Chapter.

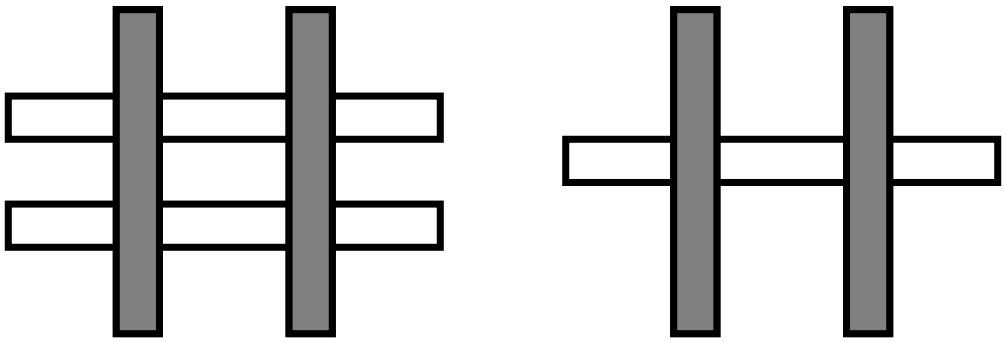
5.2 System Configurations

Several permutations of electrode configurations are considered here. The electrodes in the standalone sensor system include the measurement electrode(s) and the source electrode(s). The measurement and source electrodes may be closely spaced or distantly spaced. Closely spaced electrodes are separated by lengths that are small compared to the detection field length scales while distantly spaced electrodes are separated by lengths that are comparable to the detection field length scales. Both cases are explored in this chapter.

The signal source must have at least two coupling surfaces. These surfaces may generally be explicit electrodes or they may be manifested as stray coupling to conducting surfaces in the detection field. In this chapter, we consider systems having at least one explicit source electrode while the other coupling surface may be another explicit electrode or it may rely on stray coupling. The measurement must consist of

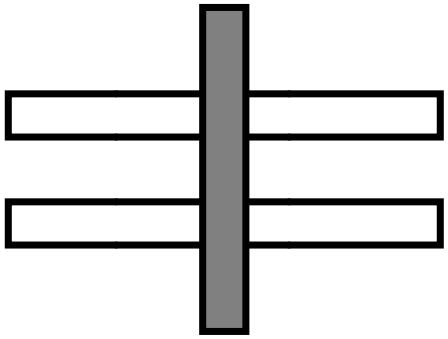
at least one coupling surface that provides a return path to the signal source reference. Here we consider systems having at least one explicit measurement electrode. Systems having two explicit measurement electrodes can achieve the natural carrier suppression inherent to the fluorescent lamp sensor system. Systems having only one measurement electrode generally require active carrier suppression to achieve the same effect. This is discussed in Section 5.4.

The signal source can be generated by any periodic electric field source, for example a signal generator with a sinusoidal output. Useful signal amplitudes range from tens to hundreds of volts. Useful signal frequencies range from tens to hundreds of kilohertz. The signal source may be earth referenced or not. If the signal source is earth referenced, then stray coupling to earth serves as a return path for coupled signals. In systems having only one explicit source electrode, stray coupling to earth is the only return path. A notable feature of those systems is that footsteps may be significantly detected in the sensor measurement as they may represent a substantial change in the coupling from the occupant to the stray earth coupling in the floor.

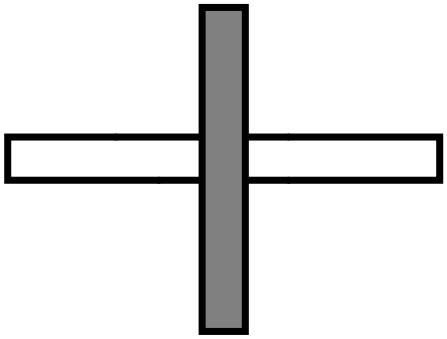


(a) 2 meas., 2 source

(b) 2 meas., 1 source

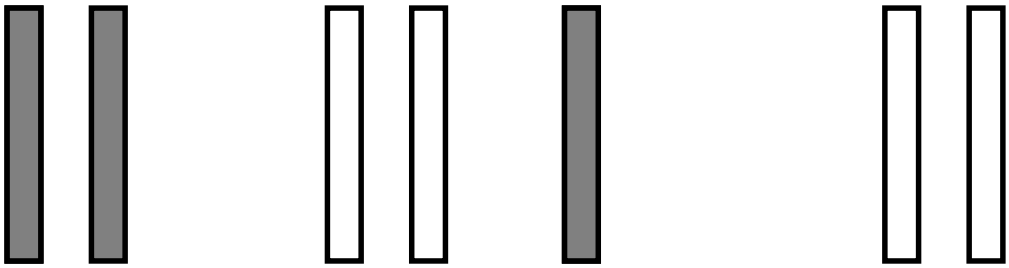


(c) 1 meas., 2 source



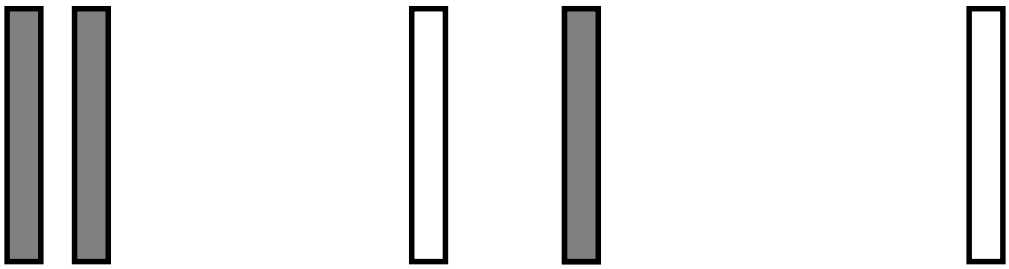
(d) 1 meas., 1 source

Figure 5-2: Closely spaced electrode configurations



(a) 2 meas., 2 source

(b) 1 meas., 2 source



(c) 2 meas., 1 source

(d) 1 meas., 1 source

Figure 5-3: Distantly spaced electrode configurations

5.3 System Modeling

The capacitive modeling of the standalone system may be guided by the modeling described for the fluorescent lamp sensor system in Chapter 3. In contrast to the lamp sensor system, modeling the signal source in the standalone system is relatively straightforward. The system may be modeled using the circuit model of the fully-differential front-end amplifier developed in Chapter 2.

An example system model corresponding to a system having two measurement electrodes is shown in Figure 5-4. The system model in Figure 5-4 represents systems having one or two explicit source electrodes. If the triangular ground symbol in Figure 5-4 is taken to be earth, then the model represents systems with an earth-referenced signal source. In systems having two explicit measurement electrodes, it is not necessary that the sensor electronics share the ground reference with the signal source.

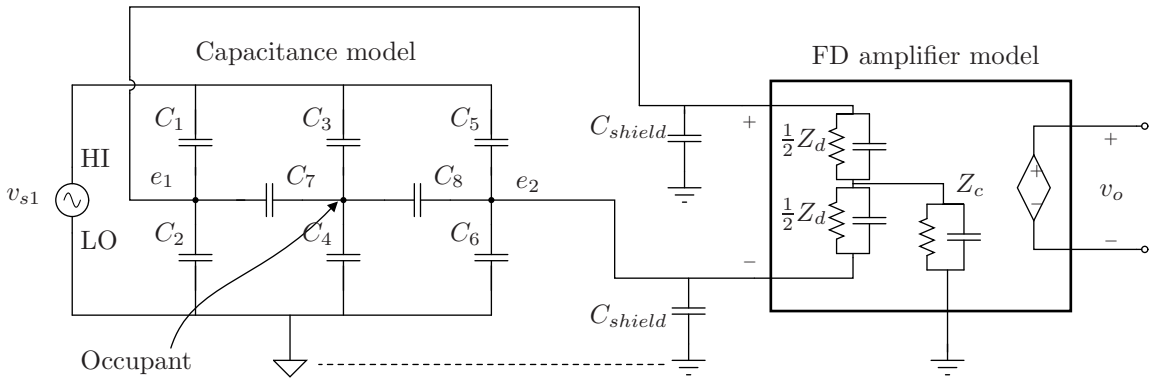


Figure 5-4: A simplified model of the two-electrode stand alone sensor using a FD measurement

An example system model corresponding to a system having one measurement electrode is shown in Figure 5-4. In systems having only one explicit measurement electrode, it is particularly useful if the sensor electronics share the ground reference with the signal source.

5.4 Active Carrier Suppression

Some practical system configurations relevant to the standalone sensor comprise only one measurement electrode. Here we describe a method for achieving active carrier suppression in otherwise unbalanced capacitive systems using an artificial secondary signal source and the multi-input structure of the fully-differential amplifier from Chapters 2 and 3.

In Chapter 3 carrier suppression was a key operating principle that allowed for detection of minute changes in the lumped capacitive network comprising the detection field. Without suitable suppression of the unneeded carrier content, there would be an awkward design tradeoff between front-end gain (transimpedance) and output dynamic range. Balanced multisource capacitive systems can achieve this carrier suppression naturally. Systems having one measurement electrode may require an added signal to actively suppress unwanted carrier content.

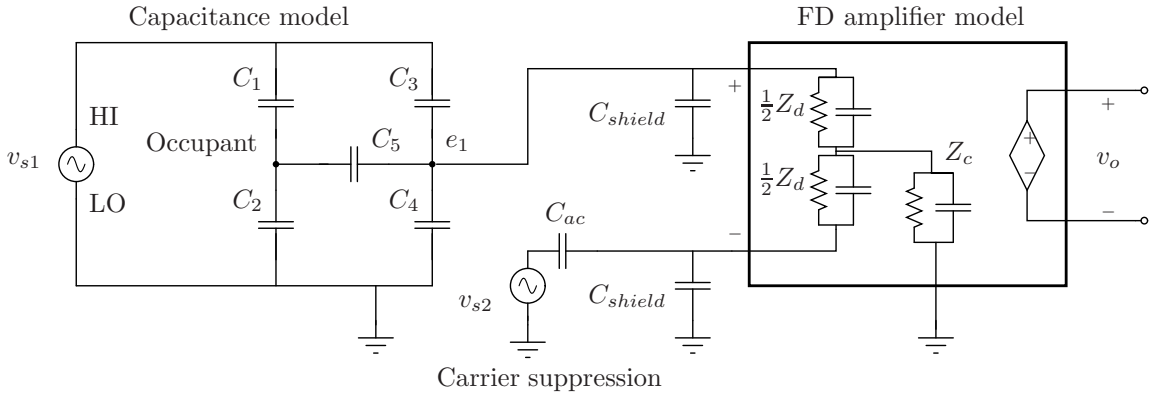


Figure 5-5: A simplified model of the single-electrode stand alone sensor with active carrier suppression using a FD measurement

In single measurement electrode configurations, the unused input on the fully-differential front-end amplifier provides a means for injecting an active carrier suppression signal. Active carrier suppression may be achieved with the configuration indicated for the system model in Figure 5-5. A discrete capacitor, C_{ac}, is placed in series with the unused input on the fully-differential front-end amplifier and a copy of the signal source, v_{s2}. The amplitude of v_{s2} or the value of the capacitance, C_{ac}, may be adjusted to null the output of the front-end amplifier in the absence of a de-

tection. The required adjustment depends on the physical configuration of the source and measurement electrodes and may be implemented with a variable gain op-amp connection.

5.5 Implementation

The implemented electronics for the stand alone sensor experimental setup are shown in Figure 5-13. The electronics are based on the signal conditioning electronics used in the fluorescent lamp sensor from Chapter 3.

In the stand alone sensor setup, the signal source, V_s, is assumed to be directly available to the signal conditioning electronics. For practical embodiments in which the source and measurement are distantly spaced, a signal source recovery circuit may be needed. An example of a signal source recover circuit is a phase-locked-loop (PLL).

Because the signal source is directly available in the experimental setup considered here, the phase reference is coupled to the signal source with a discrete capacitor, C_{phase}. Also, the active carrier suppression circuit shown in Figure 5-13 directly accesses the signal source to generate the carrier suppression signal. The active carrier suppression circuit takes a divided down copy of the signal source and applies a non-inverting variable gain. The intent of the two-stage inverting op-amp connection is to achieve a non-inverting gain that may be less than unity. The output of the carrier suppression circuit is coupled to the unused input on the front-end amplifier, when only one measurement electrode is used. The capacitive coupling simulates the capacitive coupling effect of the first measurement electrode. Typical passive component values are shown in Table 5.1.

5.6 Experimental Setup

An experimental setup was constructed to allow for investigation of all of the electrode and source configurations described in Section 5.2. A photograph of the experimental

Table 5.1: Typical system parameters and passive components.

Parameter	Value
$R_{f1,2}$	10 MΩ
$C_{f1,2}$	7.5 pF
R_{f3}	200 kΩ
C_{f3}	660 pF
R_{lim}	20 Ω
R_{pu}	500 Ω
R_{lpf}	10 kΩ
C_{lpf}	150 pF
C_{phase}	20 pF
C_{ac}	68 pF
R_{ac1}	3 MΩ
R_{ac2}	18 kΩ
R_{ac3}	100 kΩ
R_{ac4}	100 kΩ
R_{ac5}	102 pot
f_c	30 kHz
V_s	100 V_{p-p}

setup is shown in Figure 5-6. The experimental setup includes the signal conditioning electronics from Figure 5-13, and movable electrodes like the ones in Figure A-1. The signal source was generated with an HP 6827A bipolar amplifier and a Tektronix CFG250 signal generator. Data was taken using the same MATLAB® interface and PIC operating system employed for the fluorescent lamp sensor. The relevant software can be found in Appendix A.

Figure 5-7 shows a typical MATLAB® plot window. The upper two windows show the same detection signal in real time, but scaled differently in the vertical axis. The interesting portion of this particular plot window is shown in the bottom plot, which indicates a time history of what the software identified as a detection. This detection corresponds to an occupant walking approximately 10 m through the detection field for a system having one measurement electrode. From the discussion in Section 5.2, this system relies on an earth return through ambient coupling, e.g. through the floor. Therefore, footsteps should be captured in the detection as they constitute a significant time-varying change in the capacitive coupling from the occupant to the

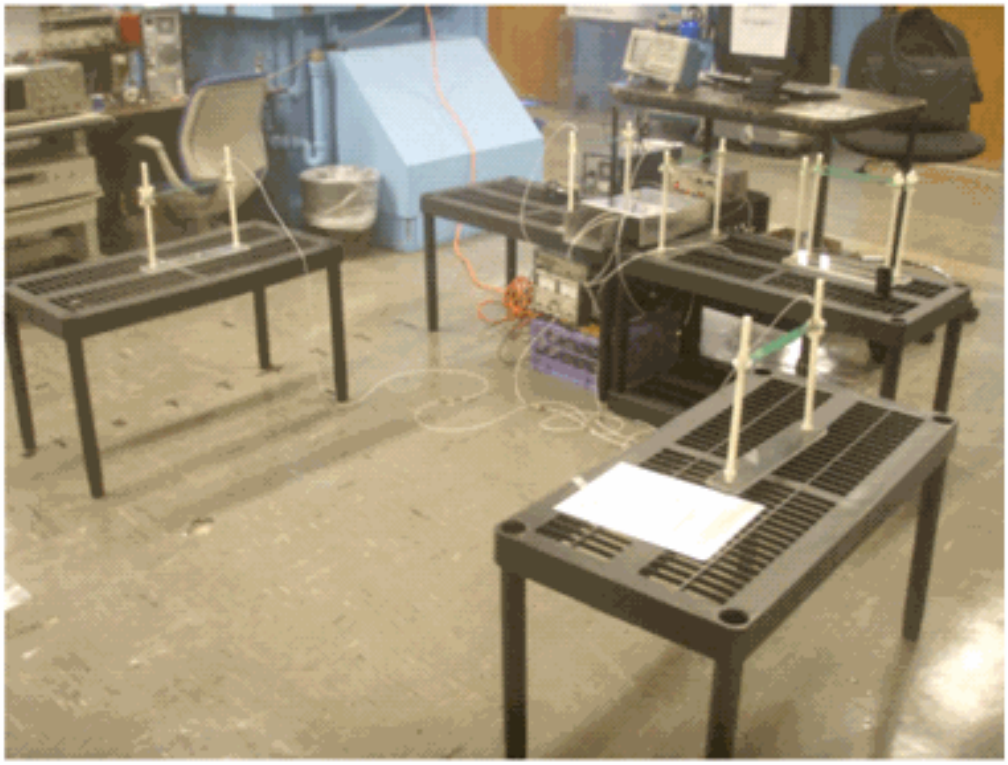
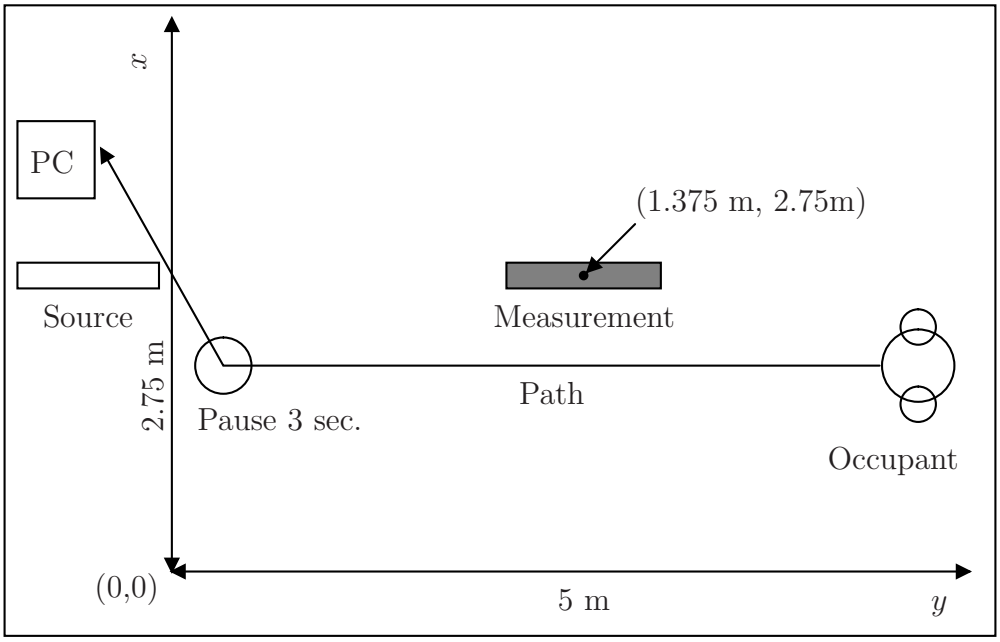


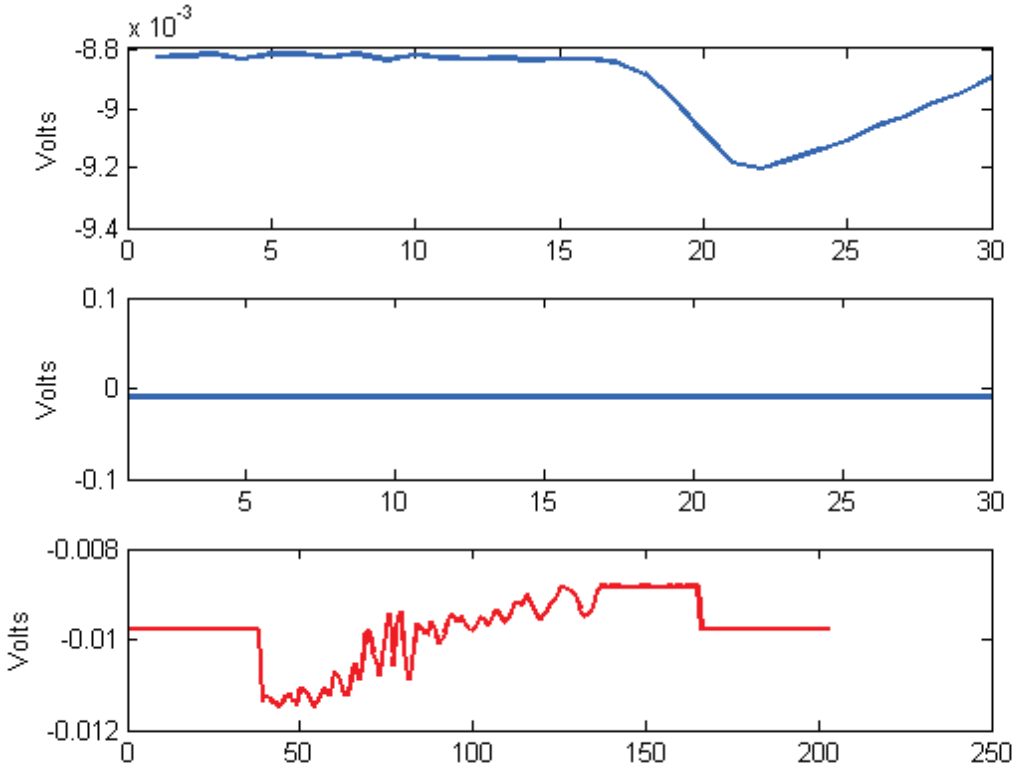
Figure 5-6: The stand alone sensor experimental setup with customizable electrode configurations.

earth return.

An overhead view of the detection field and occupant path in this example is shown in Figure 5-7(b). The drawing is not to scale, but approximate dimensions are shown in meters. The measurement electrode was centered in the detection field. The occupant passed by the measurement electrode. In the bottom plot in Figure 5-7(a), the small perturbations superposed on the detection correspond to the footsteps of the passing occupant. The amplitude of the footstep signal increases as the occupant passes by the measurement electrode. In the upper plot, the real-time data detects the occupant as he passes in front of the source to capture the data on the PC after a three second pause. The dip in the real-time detection window also appears at the end of the detection history in the bottom plot.



(a) Overhead view of detection field and occupant path



(b) MATLAB® plot window showing footsteps

Figure 5-7: A typical MATLAB® plot window and detection field experimental setup. In this single measurement electrode configuration, footsteps are apparent in the detection (bottom plot of (b)). Approximately 10 datapoints correspond to 1 sec.

5.7 Detection Patterns

Detection patterns can be found by plotting the sensor response to an occupant in a grid of positions about the detection field. These plots can be used to evaluate the characteristics of particular electrode and system configurations, e.g. sensitivity, range, directionality. In all of the detection patterns, the absolute offset voltage may be disregarded. Only the shape of the response about the offset is interesting for this discussion because the degree to which the carrier suppression achieves zero volts absolute offset is a practical matter and has no effect on the relative detection as long as the sensor output does not saturate.

Figure 5-8 shows an overhead view of the experimental setup and detection pattern for a distantly spaced electrode configuration. The detection pattern shows a "tunnel" between the source and the measurement. When the occupant is behind the measurement electrode, the detection pattern flattens. This detection pattern demonstrates an interesting example of a directional electrode configuration.

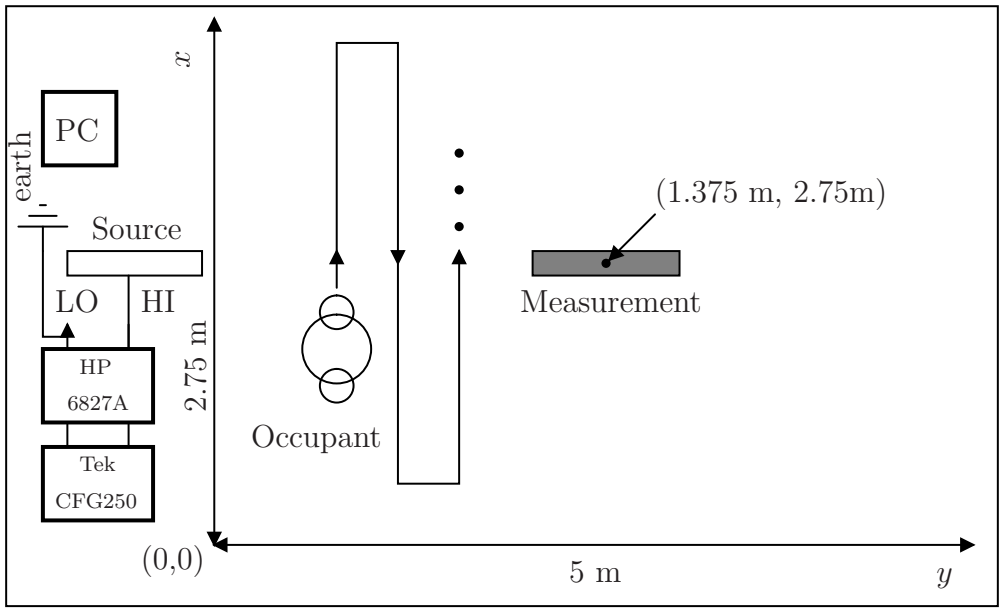
Figure 5-9 shows the experimental setup and detection pattern for a closely spaced electrode configuration. In this example there is one explicit source electrode and one measurement electrode. Active carrier suppression was needed in this example to achieve a nulling of the sensor output in the absence of a detection. The four detection pattern plots in Figure 5-9 correspond to four different vertical spacings between the source and measurement electrodes. From the data, the peak relative detection decreases as the vertical spacing increases. However, the detection level at increasingly further x and y positions increases as the vertical spacing increases. The detection pattern effectively "squashes" outward as the vertical spacing increases. This is a useful observation because it indicates that the detection range increases for larger spacing between the measurement and source electrodes, an effect that we intuitively expect.

Also evident in the detection patterns are two peaks about the source electrode that appear in all four cases. Asymmetries between those two peaks are likely due to measurement error. Those peaks indicate that the peak detection occurs when the

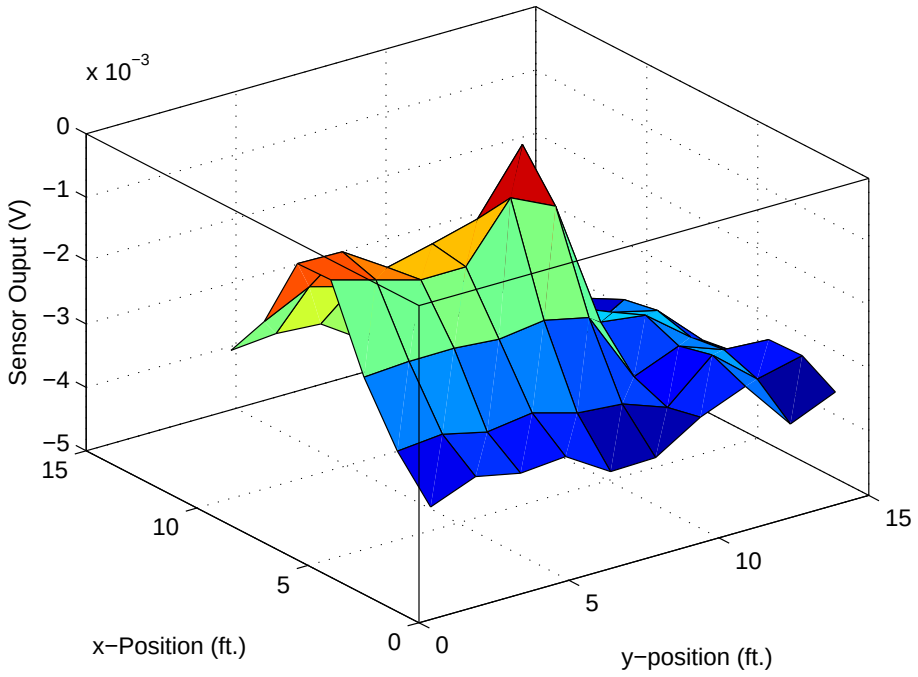
occupant is slightly to either side of the source electrode.

Figure 5-10 shows the experimental setup and detection pattern for a closely spaced electrode configuration with two measurement electrodes and two source electrodes (one high and one earth ground). The four detection pattern plots in Figure 5-9 correspond to four different vertical spacings between the source and measurement electrodes. From the data, the peak relative detection generally decreases as the vertical spacing increases. The $\Delta z = 5$ cm case shows a slight increase in the peak detection. Again, the detection pattern effectively "squashes" outward as the vertical spacing increases. This is a useful observation because it indicates that the detection range increases for larger spacing between the measurement and source electrodes, an effect that we intuitively expect.

Also evident in the detection patterns are two oppositely facing peaks about the two measurement electrodes that appear in all four cases. The differences between the two peaks are likely due to differences in earth coupling on the two sides of the electrode group. The sign reversal between the two peaks indicates directionality that may be useful in practical applications.

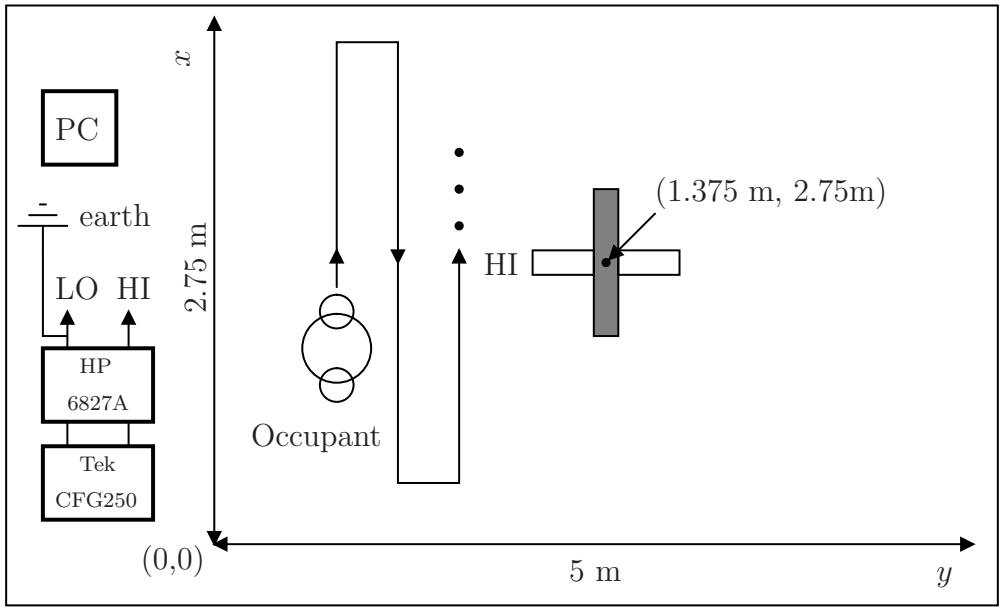


(a) Overhead view of detection field

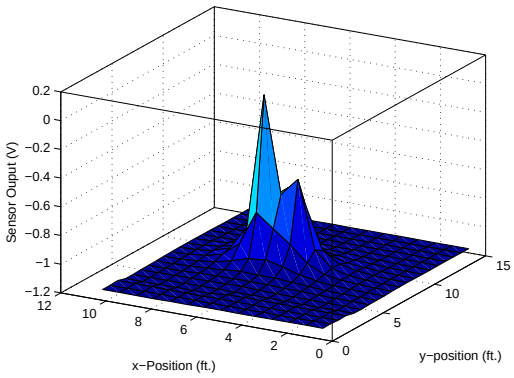


(b) Detection pattern

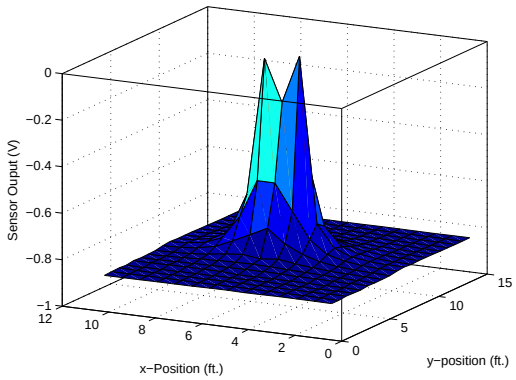
Figure 5-8: 1 meas., 1 source, distantly spaced.



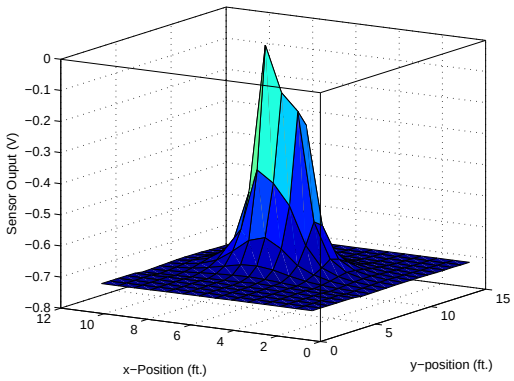
(a) Overhead view of detection field



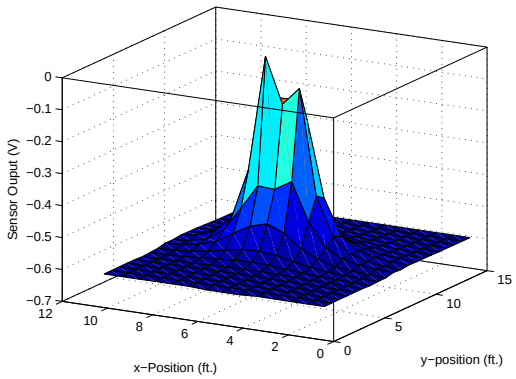
(b) $\Delta z = 1$ cm



(c) $\Delta z = 5$ cm

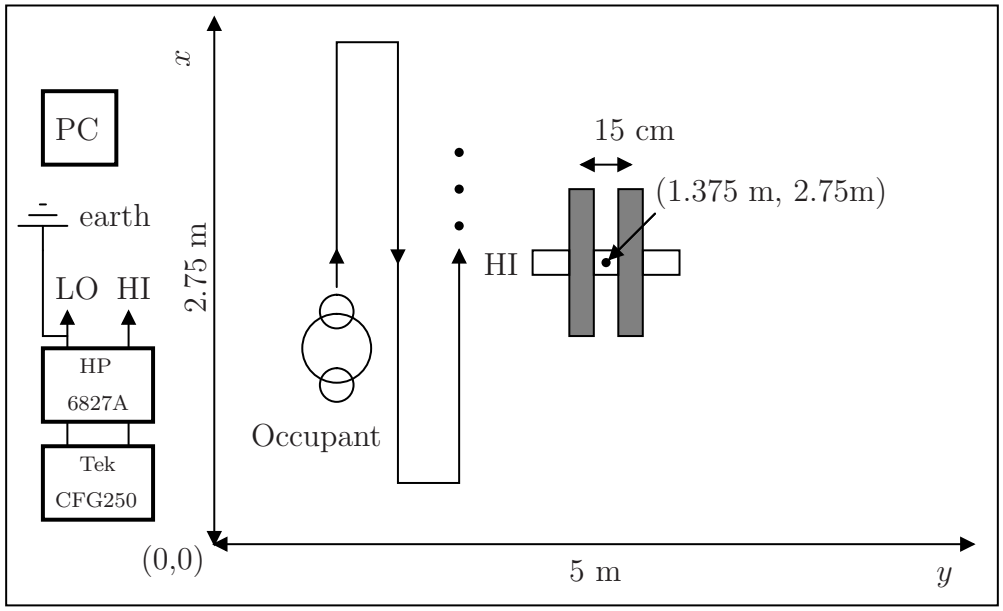


(d) $\Delta z = 20$ cm

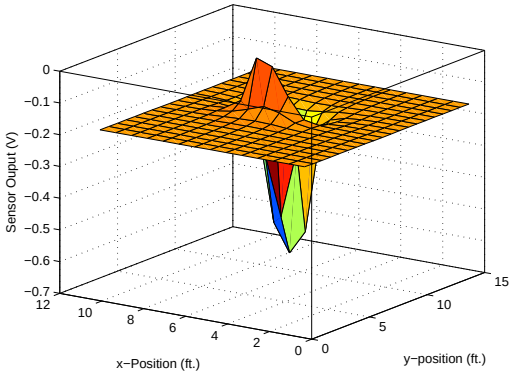


(e) $\Delta z = 27$ cm

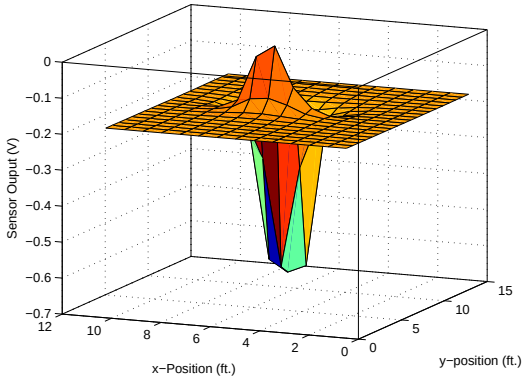
Figure 5-9: 1 meas., 1 source, closely spaced for various vertical spacings between source and measurement.



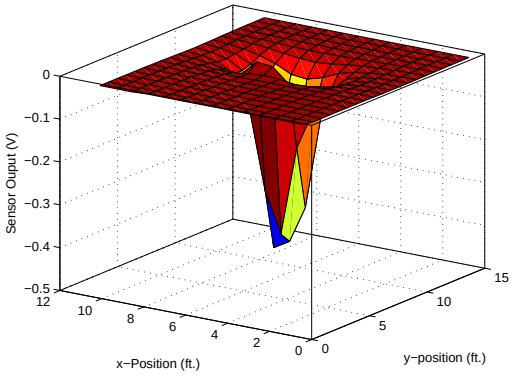
(a) Overhead view of detection field



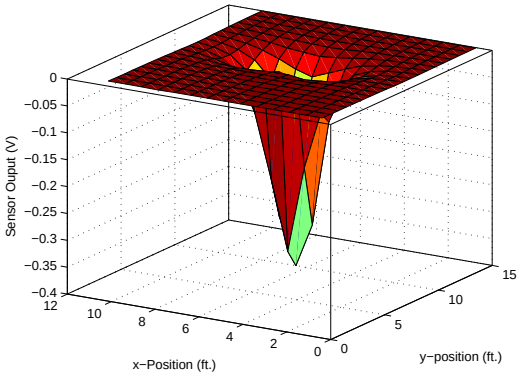
(b) $\Delta z = 1$ cm



(c) $\Delta z = 5$ cm

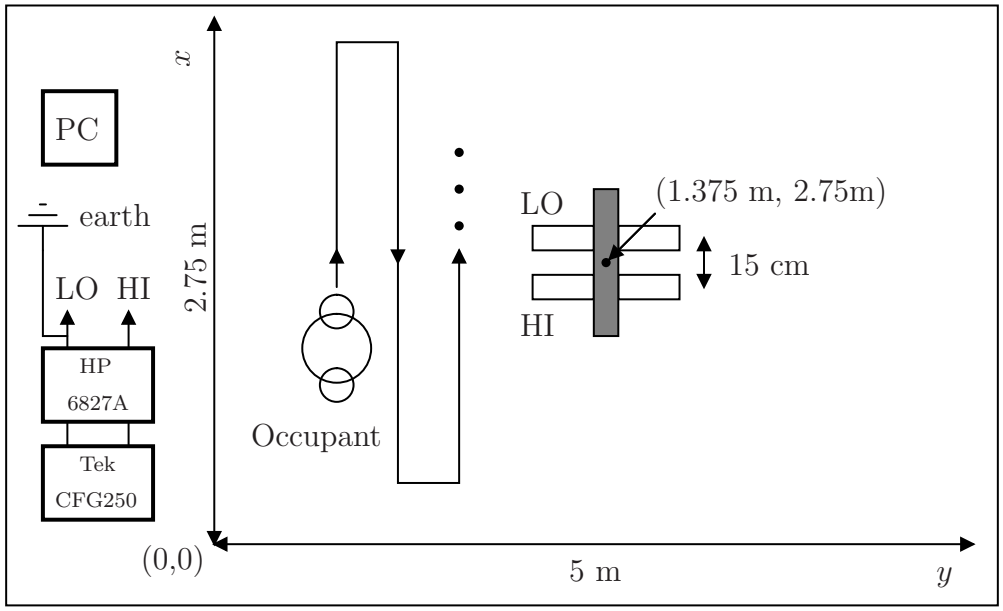


(d) $\Delta z = 20$ cm

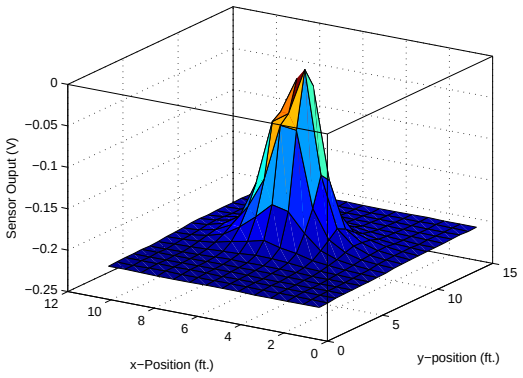


(e) $\Delta z = 27$ cm

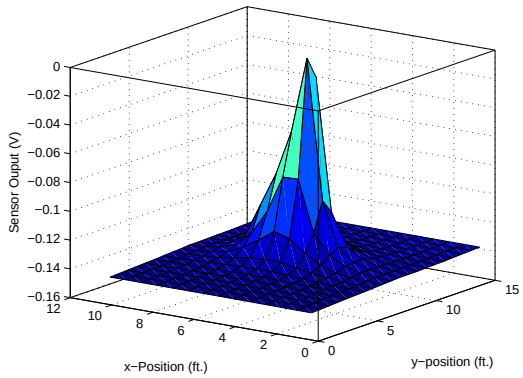
Figure 5-10: 2 meas., 1 source (high), closely spaced for various vertical spacings between source and measurement.



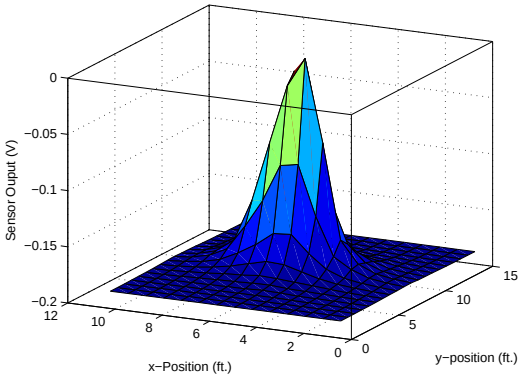
(a) Overhead view of detection field



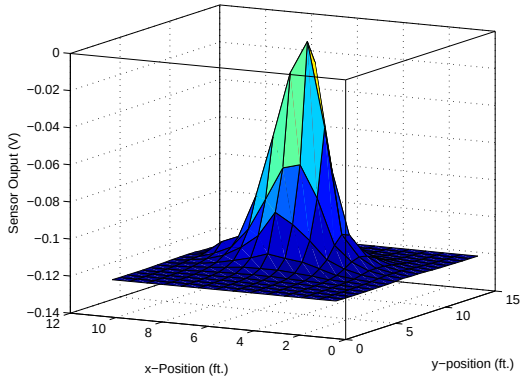
(b) $\Delta z = 1$ cm



(c) $\Delta z = 5$ cm

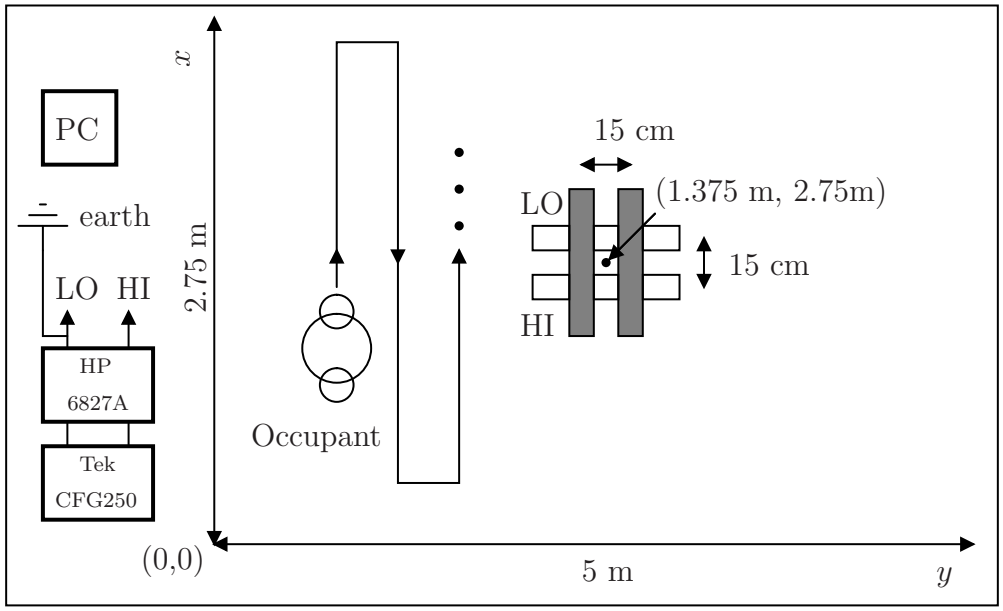


(d) $\Delta z = 20$ cm

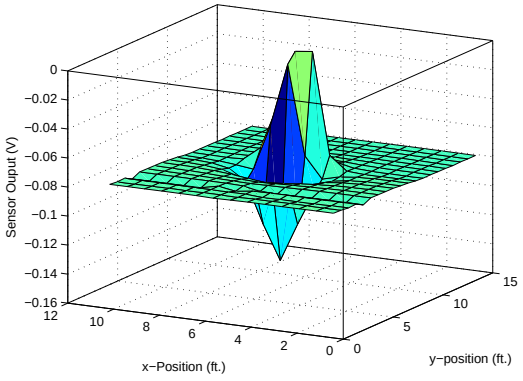


(e) $\Delta z = 27$ cm

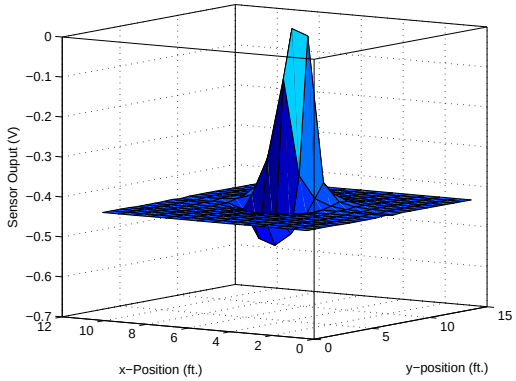
Figure 5-11: 1 meas., 2 source (high and earth ground), closely spaced for various vertical spacings between source and measurement. LO: earth ground.



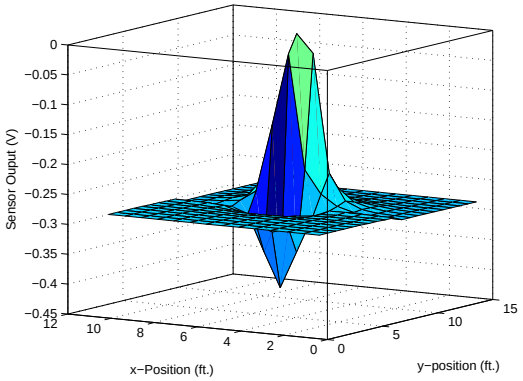
(a) Overhead view of detection field



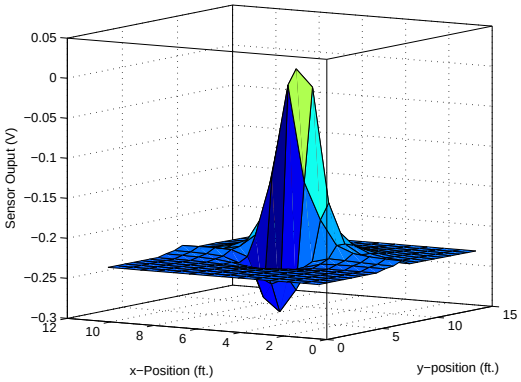
(b) $\Delta z = 1$ cm



(c) $\Delta z = 5$ cm



(d) $\Delta z = 20$ cm



(e) $\Delta z = 27$ cm

Figure 5-12: 2 meas., 2 source, closely spaced for various vertical spacings between source and measurement. LO: earth ground.

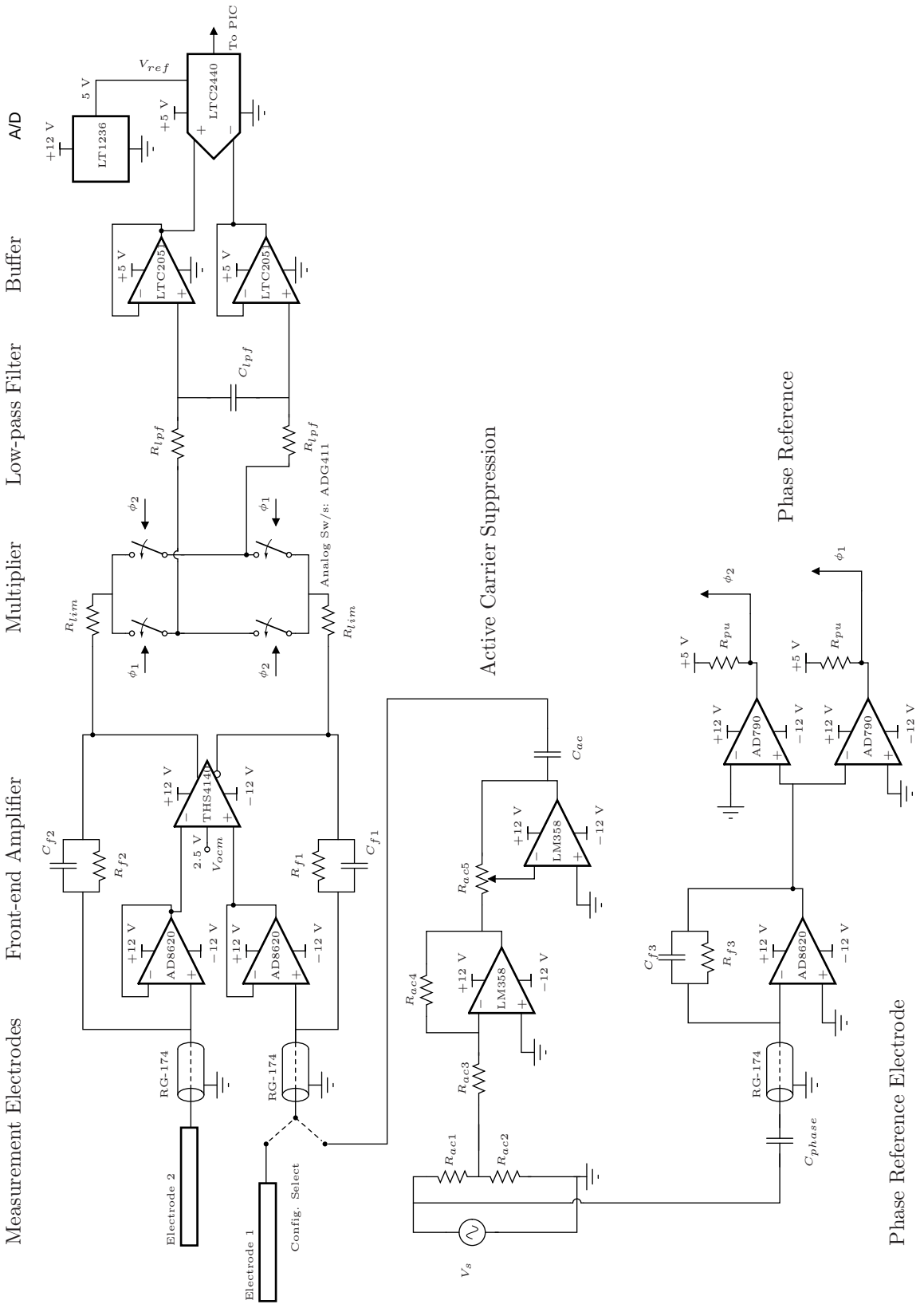


Figure 5-13: A simplified schematic of the fully-differential signal conditioning electronics

Chapter 6

Analysis and Modeling of Feedback-regulated Multi-converter, Multi-source Power Systems

6.1 Introduction

This chapter presents linearized modeling and analysis of multi-converter, multi-source power systems for fuel cell power processing applications. Specifically, the multi-converter system is intended to achieve current buffering of the fuel cell from variations in the load. Additionally, the multi-converter system is designed for integral diagnostics using impedance spectroscopy. The excitation for the impedance spectroscopy signal is generated with a small-signal control signal superposed on the control input of one of the converters in the multi-converter system. The small-signal response of the entire multi-converter system is designed to minimize the effect of the impedance spectroscopy on the load voltage and current. That is, the excitation current for impedance spectroscopy effectively flows from the secondary source, typically a battery in the design examples, and not from the load.

The analysis of multi-converter systems has been the subject of many previous investigations. Much of the previous work on multi-converter or "hybrid" power systems focuses on system level analyses [121–127]. These analyses treat the converters as simplified elements having ideal voltage or current outputs and perhaps some characteristic, usually the negative incremental input impedance effect of a feedback regulated converter [122, 125]. Conclusions are often drawn from simulation rather than analysis [126, 128].

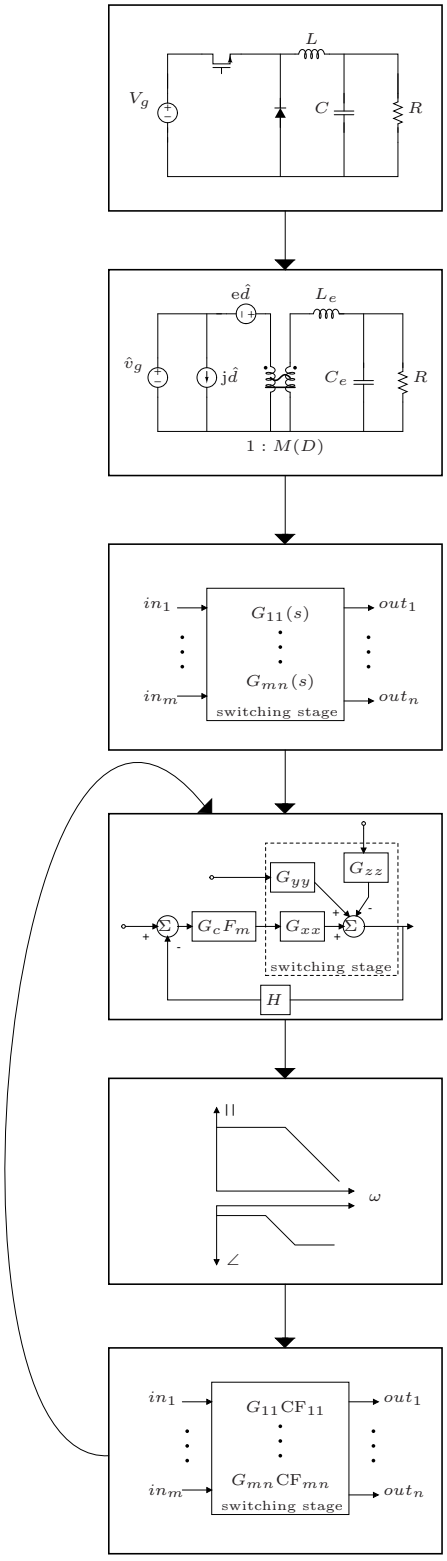
Previous work on paralleled converter systems has investigated actual converter dynamics and interactions leading to design-oriented conclusions. The analyses of paralleled converter systems has been focused on systems having a single input source [129–133]. Many of those analyses are focused on a particular control scheme [131–133]. The treatment of multiple input filters in a multi-converter system presented in this thesis was not found in the literature.

The work in [129] is closest to the developments in this thesis - the main difference being that [129] focuses on multi-converter systems having a single input source. References [130] and [131] focus on stability analysis through the examination of loop gains in a master-slave current sharing system. Reference [132] focuses on paralleled buck converters operating under average current share control and reference [133] focuses on paralleled voltage regulator modules for microprocessor power. Reference [134] derives a modeling approach that is distinct because it reduces the paralleled converter system to two subsystems - one differential mode and the other common mode. Much of the single converter systems review in this thesis is based on reference [14].

A key feature of any of these analyses is the version of the linearized converter model used in the analysis. Naturally, all of these linearized models can be shown to be equivalent in as much as they are similarly complete. Reference [129] employs the converter model developed by Vorperian in [135]. References [130, 133, 134] employ a Thevenin equivalent converter model and reference [136] employs the model developed by Middlebrook. Reference [137] does not directly reference any linearized circuit model and instead derives the linearized converter transfer functions directly from

the nonlinear converter topology of interest. Notably, reference [137] analyzes multi-converter systems with a single input source but discusses a method for extending the analysis to systems having different input voltages. Other references [131, 132, 138] employ linearized circuit models developed somewhat independently and always, in some sense, based on linear superposition principles.

A key stylistic feature of the analyses is the use of matrix formulations, block diagram representations, linear superposition arguments, or a mix. Again, all of these approaches can be argued as equivalent. References [129,131,138] employ linear superposition in the context of block diagram representations only. Reference [130] mixes linear superposition, block diagram representations and matrix formulations while [137] employs matrix formulations and block diagram representations only.



Step 0: Linearization, Derivation of Model Parameters

Step 1: Derivation of Converter Transfer Functions

Step 2: Construction of Feedback Control System

Step 3: Evaluation of C-L and O-L Transfer Functions

Step 4: Add Input Filter(s), Compute (N)EET Correction Factors

Figure 6-1: The analysis in this chapter focuses on steps 1-4. The approach is reviewed for single converter systems, then extended to multi-converter systems.

The analyses presented in this thesis were developed for a particular set of applications requiring specific large and small signal functionality with multiple distinct sources. More than one application and set of requirements is considered so some effort was made to generalize the modeling effort so that it can be applied to arbitrary feedback control approaches.

The linearized circuit model employed here is that developed by Middlebrook in [12, 139, 140]. The model is written in terms of three model parameters that may be related to any converter topology. A benefit of the model is that it includes input current perturbations. This has particular implications for the small-signal input current functionality needed in the design of the systems presented here. It also makes the multi-converter model directly useful for studying the effects of multiple input filters in Chapter 7.

The stylistic features of the analyses here are defined by a separation of the analytical process into distinct steps and the use of linear superposition in the context of block diagram representations. A schematic illustration of the analytical method followed in this thesis is shown in Figure 6-1. Step 0 is not directly addressed in this thesis, the results of which are essentially a tabulation of model parameters that may be inserted into the the linearized model. While the computation of the model parameters (Step 0) is not directly addressed here, the nature of those model parameters is discussed on a fundamental level. This understanding leads to a method presented in Section 6.4 for generalizing previously derived model parameters. The benefit of this generalization method is that those model parameters may be used to relate the linearized models of multi-converter systems developed in this thesis to actual converter topologies, e.g. buck, boost, or buck-boost. Steps 1-3 in Figure 6-1 are the topic of the current chapter. Step 4 represents a sufficiently distinct development that it is treated separately in Chapter 7.

In this chapter (steps 1-3 from Figure 6-1), converter transfer functions are derived from the linearized model. The converter transfer functions may be used to represent the behavior of the converter when it is inserted into a feedback regulation system. Closed-loop transfer functions (regulator transfer functions) and open-loop transfer

functions are considered separately. The analyses of two example feedback regulation systems are presented. Before applying this method to multi-converter power systems, we first review the analogous method for single converter systems.

6.1.1 Context - Fuel Cell Power Processing

This investigation was motivated by the application of multi-converter power systems to multi-source systems comprising a fuel cell and a second source. There is an increasing realization that the commercial viability of fuel cells depends on work to enhance reliability and durability [141, 142]. These limitations can be mitigated by furnishing the fuel cell with a fixed power operating point within the rated power of the device. However, many practical applications demand widely varying power. Incorporating the fuel cell into a multi-source power system adds enough degrees of freedom for fixed operating point fuel cell operation while the secondary source accommodates the variability in the load.

In practice, operating the fuel cell at a fixed and safe operating point may not completely mitigate degradation effects. Therefore, there is some interest in monitoring degradation phenomena during runtime, when fuel cells are integrated into real systems. As an example, in [143], Ramschak et. al. provide a method to detect the failure of a single cell within a stack by analyzing the harmonic distortion on the stack voltage. Similarly, in [144] Gemmen et. al. study the impact of inverter load dynamics on a fuel cell, with the conclusion that stack / inverter interaction is significant in the operating conditions and long term behavior of the stack. In references [145, 146], Ren et. al. examine the interactions between solid-oxide fuel cells and grid interface.

Fuel cell diagnostics may be achieved through impedance spectroscopy, commonly known as electrochemical impedance spectroscopy (EIS) when applied to an electrochemical device [142, 147–150]. Integral diagnostics may be achieved by integrating EIS functionality into the controls of the power system. In a single converter system, integral diagnostics functionality can lead to unwanted effects, for instance the EIS measurement may yield prohibitive or at least unwanted disturbance of the load voltage and / or current. The added degrees of freedom needed to reduce or eliminate

these unwanted effects can also be exploited with a multi-converter power system.

In Chapters 8 and 9, we present two design examples. In the first example the integral diagnostics functionality for a fuel cell is demonstrated in a stationary application. Buffering of the fuel cell current from load current variability is not demonstrated in this first example because the power system feeds directly to the grid and the load power is relatively fixed. The needed functionality in this first example is achieved with a dual voltage regulated power system using off-the-shelf power converters.

In the second example, the power system is intended to power an electric unmanned aerial vehicle (UAV). The load in this second example is by its nature highly variable. Both integral diagnostics and buffering of the fuel cell current from the load current variability are demonstrated. The needed functionality in this second example is achieved with a master-slave current-voltage regulated power system.

6.2 Single Converter Systems Review

This chapter analyzes the small-signal behavior of multi-converter, multi-source power systems starting from Middlebrook's linearized canonical models of CCM-operated power converters [12]. A parallel development could be carried out if the converters operate in DCM by using the corresponding models for DCM-operated converters [140].

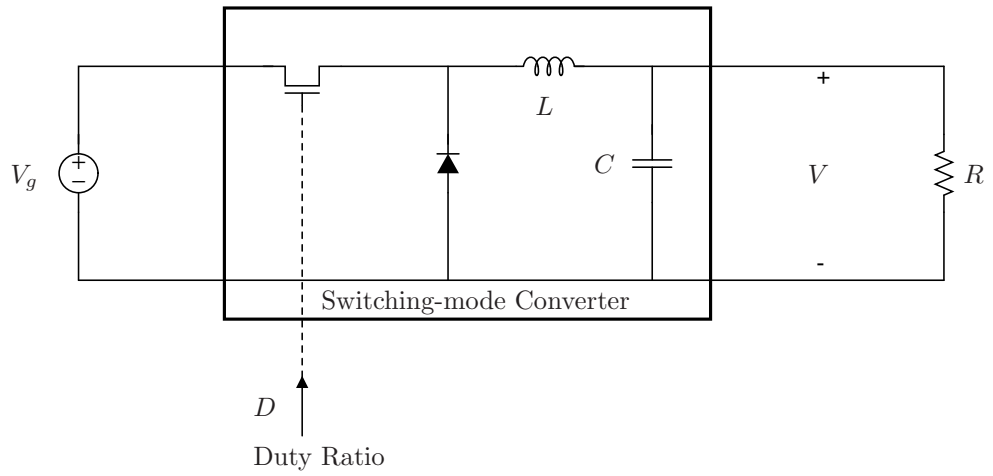
The analytical methods are first reviewed in the context of single converter systems. The single converter review begins with a review of Middlebrook's linearized converter model in Section 6.2.1. Some notable converter transfer functions are derived in Section 6.2.2. Finally, an example single-converter closed-loop power system is analyzed in Section 6.3.

The multi-converter developments mirror the single converter review. The generalizations necessary to build a linearized model of a multi-converter power system from Middlebrook's canonical circuit models are discussed in Section 6.4. A general linearized model of a multi-converter, multi-source power system based on Middlebrook's linearized converter model is presented in Section 6.5. Some particularly

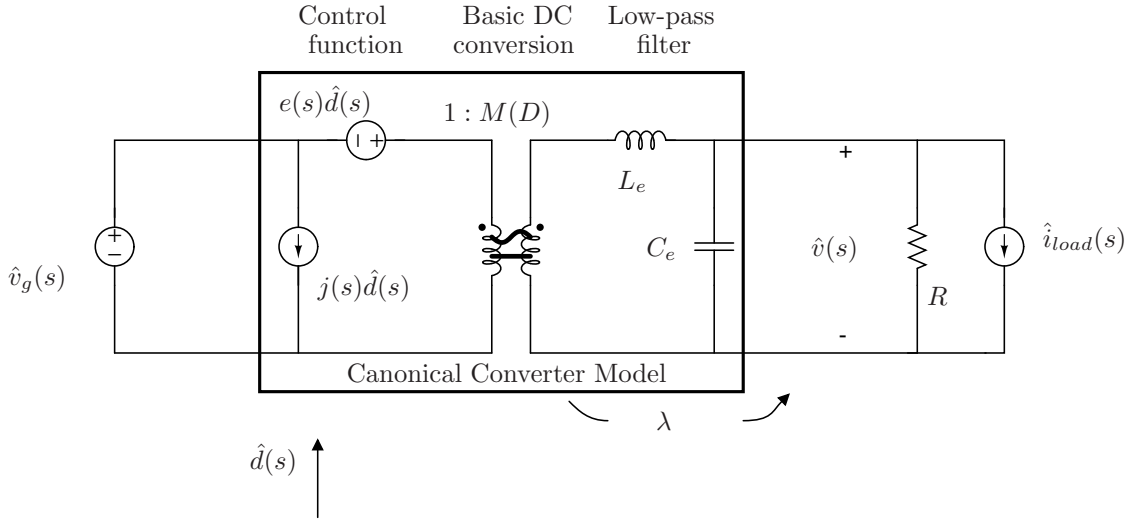
useful converter transfer functions are derived from that model. Finally, example closed-loop power systems are analyzed in Sections 6.6 and 6.7.

6.2.1 Middlebrook's Linearized Canonical Converter Model

In reference [12], Middlebrook develops linearized circuit models that can be used to represent the input, output and control properties of many switching power converters. The goal of that circuit modeling is well-understood in analogy to the small-signal modeling of the bipolar transistor [12]. While the nonlinear relations describing the terminal voltages and currents of the transistor are inconvenient to use when the device is embedded in an otherwise linear system, one approach is to establish a linear small-signal model that represents the AC properties of the transistor about a specified DC (large-signal) operating point [12]. Then, the linearized model is incorporated into the overall linear system. The objective of Middlebrook's canonical circuit models for power converters is the same. Those models represent the linearized small-signal properties of the converter about a given DC operating point [12].



(a) Basic Elements of a switching-mode regulator. The LC input filter and buck converter are shown as typical realizations [13].



(b) A small-signal regulator model using Middlebrook's linearized canonical circuit model of the power converter [13]. Hats (ˆ) denote small-signal quantities.

Figure 6-2: Canonical circuit modeling developed in references [12, 13] and [14].

Middlebrook demonstrates how CCM-operated converters can be manipulated into one fixed topology and DCM-operated converters into another fixed topology in references [12, 139, 140]. For example, the basic elements of a typical power converter are shown in Figure 6-2(a). In Figure 6-2(b), the buck converter has been replaced with the linearized canonical circuit model developed by Middlebrook in [12]. [1]

The canonical circuit model consists of three pieces (in boxes): an ideal transformer that represents the converter's ideal voltage and current transformation[2], an effective low-pass filter at the output that includes the effects of the energy storage elements involved in the switching action of the converter, and dependent current and voltage sources that capture the effect of the control signal, $\hat{d}$. Reducing every converter to this "canonical topology" means that a linearized input-output and control description of any converter reduces to looking up the, perhaps frequency-dependent values for each of the model parameters as in Table 6.1 [12, 14].

Table 6.1: Canonical Model Parameters for CCM-operated Buck, Boost and Buck-Boost converters with a fixed load R [14]

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1-\frac{sL}{D'^2R}\right)$	$\frac{V}{D'^2R}$
Buck-Boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$-\frac{V}{D^2}\left(1-\frac{sDL}{D'^2R}\right)$	$-\frac{V}{D'^2R}$

6.2.2 Converter Transfer Functions

The converter transfer functions describe the linearized dynamical behavior of the converter about a fixed operating point. Their derivation is a necessary starting point for any analysis of a closed-loop regulator.

The mathematical results of the converter transfer function derivations can be

[1] The hats (ˆ) denote small-signal quantities.

[2] the straight line and the wavy line drawn on the transformer element in Figure 6-2(b) are intended to indicate DC and AC respectively.

summarized in a block diagram representation. For example, Figure 6-3 describes how three converter transfer function superpose in a summing element to capture the effects of three respective input signals on the converter output voltage. The converter output voltage is only an example and any signal can be represented as an output.

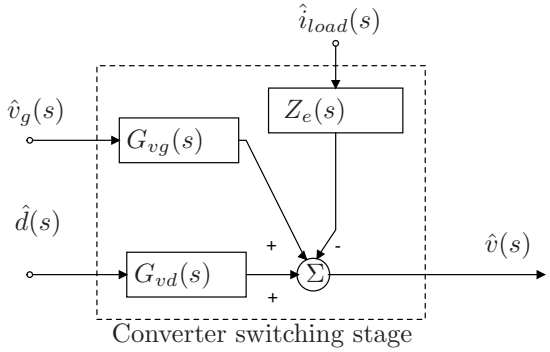


Figure 6-3: The converter switching section can be represented by an input output dynamical block diagram consisting of the relevant converter transfer functions.

In Figure 6-3, the superposition of the converter transfer function outputs on the final output signal reflects the manner in which the converter transfer functions are derived. Each converter transfer function in the example of Figure 6-3 can be derived from a circuit model of the converter in a linear superposition sense. Specifically, having defined the input signal pertaining to each converter transfer function, the other independent input signals are deactivated. Mathematically, the three notable converter transfer functions in Figure 6-3 may be defined as follows:

$$G_{vd}(s) \equiv \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_g=0 \\ \hat{i}_{load}=0}} \tag{6.1}$$

$$G_{vg}(s) \equiv \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{d}=0 \\ \hat{i}_{load}=0}} \tag{6.2}$$

$$Z_e(s) \equiv \left.\frac{\hat{v}(s)}{\hat{i}_{load}(s)}\right|_{\substack{\hat{d}=0 \\ \hat{v}_g=0}} . \tag{6.3}$$

Deriving the converter transfer functions from Middlebrook's canonical linearized converter model leads to generalized results. The behavior of any particular topology

can be represented by inserting canonical model parameters like the ones in Table 6.1 into the results. These generalized derivations are relatively straightforward. For instance, from Figure 6-2(b), the following converter transfer functions can be written down by inspection:

$$G_{vd}(s) = eM\lambda \tag{6.4}$$

$$G_{vg}(s) = M\lambda \tag{6.5}$$

$$Z_e(s) = Z_L||Z_{le}, \tag{6.6}$$

where we have defined

$$\lambda \equiv \frac{Z_L}{Z_L + Z_{le}} \tag{6.7}$$

$$Z_L \equiv R||Z_{ce} \tag{6.8}$$

$$Z_{ce} \equiv \frac{1}{sC_e}. \tag{6.9}$$

The choice of converter transfer functions to derive depends partly on the intended feedback system. For instance, in a PWM-controlled converter, the feedback system will control the converter via the duty cycle input. In a voltage-regulated converter, the feedback system will regulate the converter's output voltage. The converter transfer function from duty ratio to output voltage, e.g. G_{vd}, would ultimately be needed to form the final representation of the closed-loop regulator. On the other hand, if the feedback system regulates the converter output current by way of the duty cycle, the converter transfer function from duty cycle to output current would be critical. For a feedback system that controls the converter based on both output voltage and current, both transfer functions would be needed.

The converter transfer functions described above are critical because they are ultimately "in the loop." There is also generally a need to capture the effect of converter input signals that will not be in the loop. For instance, we are often interested in the "audio susceptibility" (the effect of the input voltage, $\hat{v}_g$, on the regulator) or the closed-loop output impedance (the effect of load current perturbations, $\hat{i}_{load}$, on

the regulator). The converter transfer functions needed to ultimately capture these effects on the closed-loop system are G_{vg} and Z_e in this example.

6.3 Regulator Example: Voltage Regulated Power System

Figure 6-4(a) shows a linearized model of a voltage regulated converter and Figure 6-4(b) shows a block diagram represenation of the same system. The dashed box depicts in Figure 6-4(b) the converter transfer functions defined in equations (6.1)-(6.3). From Figure 6-4(b), it is explicitly clear that the duty ratio input is "in the loop" and the other two converter inputs are not.

Regulator transfer functions, both closed-loop and open-loop may be taken directly from the block diagram. For instance, the closed-loop transfer function from the reference voltage, $\hat{v}_{ref}$, to the output voltage, $\hat{v}$, in Figure 6-4(b) is

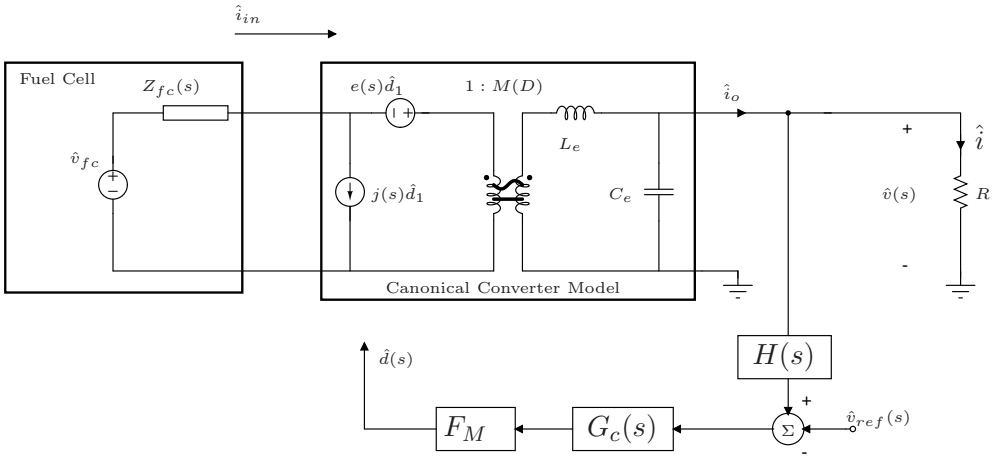
$$\left.\frac{\hat{v}(s)}{\hat{v}_{ref}(s)}\right|_{\substack{\hat{v}_g=0 \\ \hat{i}_{load}=0}} = \frac{1}{H(s)}\frac{T(s)}{1+T(s)} \tag{6.10}$$

in which the loop transfer function is

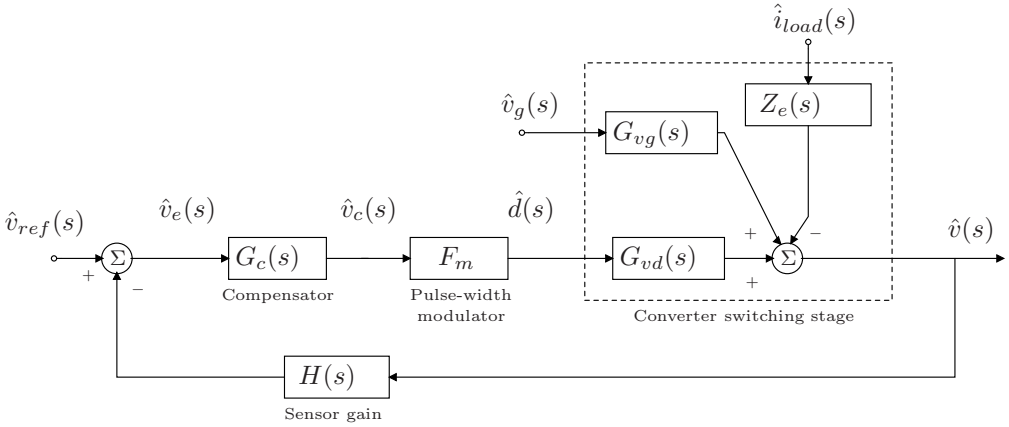
$$T(s) = G_c(s)F_m G_{vd}(s)H(s). \tag{6.11}$$

This classic result shows that the closed response of the regulator output voltage to changes in the control voltage approaches $\frac{1}{H(s)}$ when the loop gain, $T(s)$, is large compared to unity. While the other two converter transfer functions do not directly affect the loop-transfer function, they do impact the closed-loop transfer functions. For instance, the closed-loop transfer function from input voltage and load current to output voltage can be written as follows:

$$\left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = G_{vg}(s)\frac{1}{1+T(s)} \tag{6.12}$$



(a) A linear model of a voltage regulated single converter system



(b) A block diagram representation of a voltage regulated single converter system

Figure 6-4: A linearized converter model inserted into a voltage-mode feedback control loop [14].

and

$$\left.\frac{\hat{v}(s)}{\hat{i}_{load}(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} = Z_e(s)\frac{1}{1+T(s)}. \tag{6.13}$$

These results describe the closed-loop rejection of disturbances. Both of these converter transfer functions from extra input signals appear attenuated by the factor $(1+T(s))$. When the loop gain, $T(s)$, is large, the regulator response to variations in input voltage and output current will be reduced accordingly.

6.4 Canonical Model Generalizations

A linearized multi-converter, multi-source model will be developed based on the linearized canonical circuit models detailed above. This development will rely on sufficient generalization of the canonical circuit model so that it may be extended to multi-converter power systems.

To draw attention to the particular type of generalization needed for the hybrid power system analysis, the model parameters in Table 6.1, $e(s)$ and $j(s)$, contain instances of the load resistance, R. Some information is lost when deriving the model parameters for the single converter-resistive load case because the quantity R may appear in the results to represent two very different things: the impedance shunting the load – a small-signal quantity, or the ratio of the DC load current and voltage – a large signal quantity. In generalizing the model parameters, it is initially unclear whether to replace any instance of R, with the quantity V/I. However, it is possible to determine an appropriate generalization based on a fundamental understanding of the linearized models.

Because the model parameters, $e(s)$ and $j(s)$, are factors in the linearized canonical model that multiply the control signal, $\hat{d}$, they, by definition, cannot also include other small-signal factors (for instance, $e(s)\hat{d}(s)$ would be nonlinear and so would the resulting circuit model). In other words, $e(s)$ and $j(s)$ are terms that represent and depend on the DC (large-signal) operating point of the converter. They only depend on the load in that they may depend on the DC output current I and/or voltage V. This realization of the canonical circuit model is particularly useful for modeling multi-converter power systems, because the model parameters depend only internal converter characteristics and on the DC operating points of the output current and voltage.

To demonstrate this point, the previously derived canonical model parameters from Table 6.1 can be generalized from the single converter-resistive load case to the general case by replacing all factors of R in $e(s)$ and $j(s)$ with the ratio of DC output voltage and current, V/I. The results, shown in Table 6.2, are valid for CCM-operated

Table 6.2: Canonical Model Parameters for the Buck, Boost and Buck-Boost with a generalized load

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V}{D^2}$	I
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1-\frac{sLI}{D'^2V}\right)$	$\frac{I}{D'^2}$
Buck-Boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$-\frac{V}{D^2}\left(1-\frac{sDLI}{D'^2V}\right)$	$-\frac{I}{D'^2}$

converters driving a generalized load. Having developed this "intellectual shortcut" the results of hybrid power system analysis based on the canonical circuit model are more useful because previously-derived model parameters can be easily extended.

6.5 Multi-converter Systems

The methods for analyzing closed-loop feedback converters are now extended to multi-converter systems. The analysis starts with a presentation of the linearized circuit model and then follows with derivations of converter transfer functions. Two regulator examples are presented to demonstrate the manner in which the converter transfer functions may be used to arrive at closed-loop and open-loop regulator transfer functions.

6.5.1 Linearized Multi-converter Model

The linearized multi-converter model used for the analysis of converter transfer functions is shown in Figure 6-5. It is conceptually important that the analyses treat this model as a single circuit without any explicit division between the two converters. When converter transfer functions are derived directly from the circuit in Figure 6-5, the second converter loads the first and vice versa. The independent inputs shown include the two duty ratios, $\hat{d}_1$ and $\hat{d}_2$, the two input voltage perturbations, $\hat{v}_{fc}$ and $\hat{v}_{batt}$, and the load current perturbation, $\hat{i}_{load}$. The output signals labeled are the input currents, $\hat{i}_{in1}$ and $\hat{i}_{in2}$, the converter output currents, $\hat{i}_{o1}$ and $\hat{i}_{o2}$, and the load

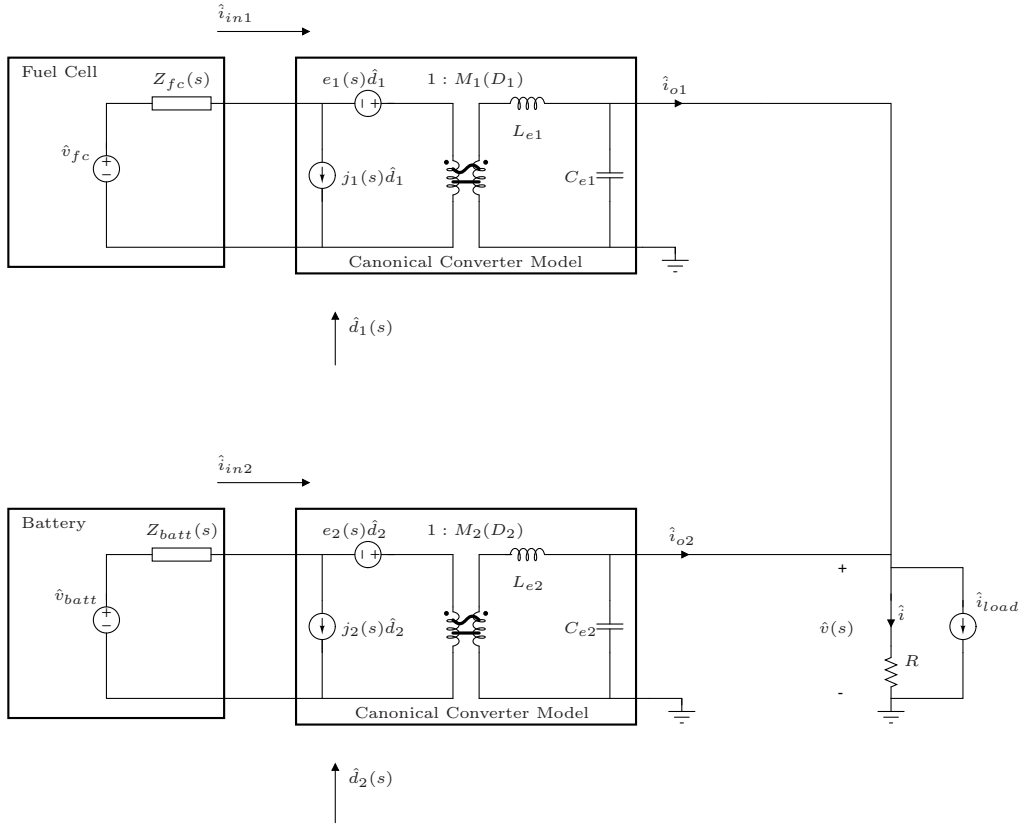


Figure 6-5: The linearized multi-converter model. The battery and fuel cell source are examples of sources in a multi-source power system.

current and voltage, $\hat{v}$, $\hat{i}$.

The source output impedances will be assumed zero-valued for now. The effect of finite source impedance can be examined in an identical fashion to the effect of input filters. Those developments will be detailed in Chapter 7.

6.5.2 Converter Transfer Functions

The converter transfer functions can be derived from the circuit in Figure 6-5. In our examples of closed-loop regulators, the feedback control will always control the converter using pulse-width modulation. The converter transfer functions having one of the duty ratios as an input will therefore be in the loop. Each of the key output variables can be written as a linear superposition of the output signals from the

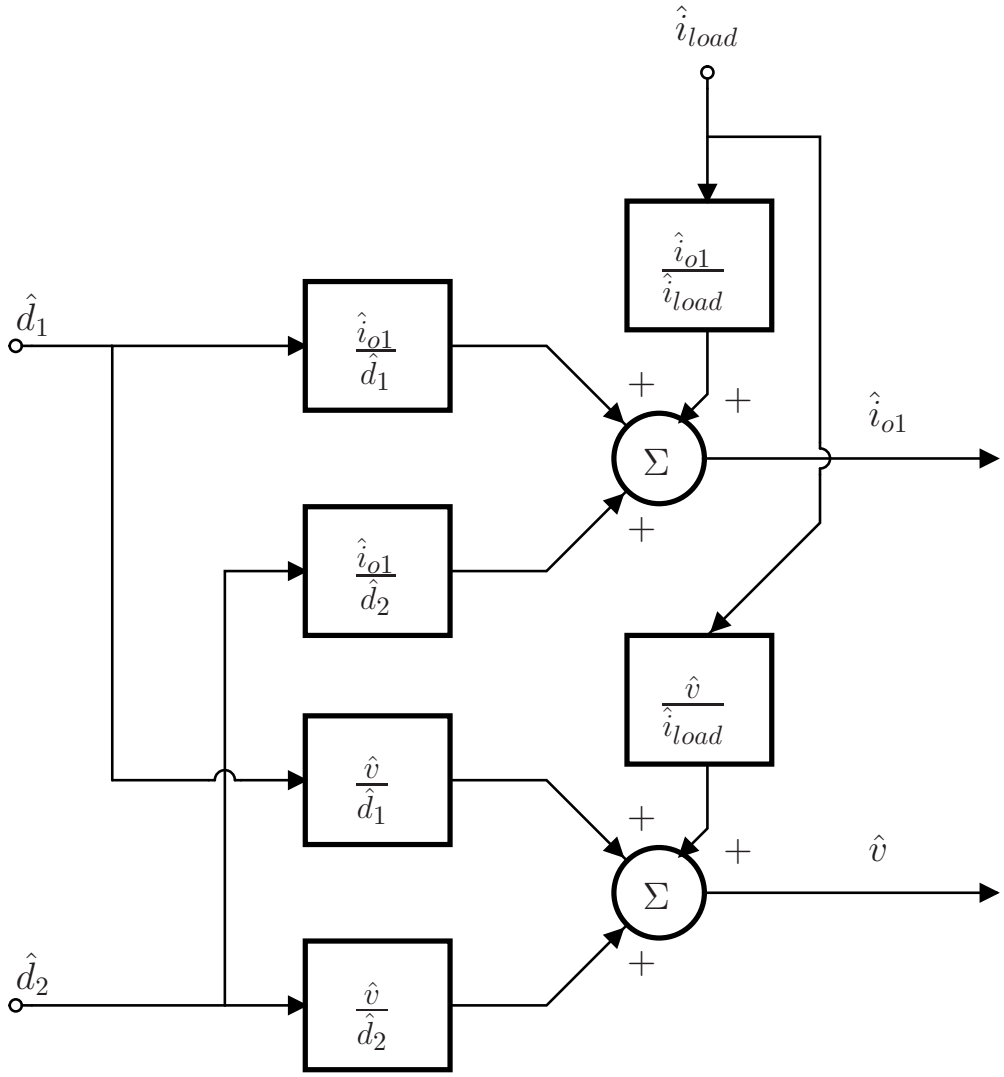


Figure 6-6: The multi-converter switching section can be represented by an input output dynamical block diagram consisting of the relevant converter transfer functions.

converter transfer functions for each of the two duty ratios as follows:

$$\hat{v}(\hat{d}_1, \hat{d}_2) = \left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0} \hat{d}_1 + \left.\frac{\hat{v}}{\hat{d}_2}\right|_{\hat{d}_1=0} \hat{d}_2 \tag{6.14}$$

$$\hat{i}(\hat{d}_1, \hat{d}_2) = \left.\frac{\hat{i}}{\hat{d}_1}\right|_{\hat{d}_2=0} \hat{d}_1 + \left.\frac{\hat{i}}{\hat{d}_2}\right|_{\hat{d}_1=0} \hat{d}_2 \tag{6.15}$$

$$\hat{i}_{o1}(\hat{d}_1, \hat{d}_2) = \left.\frac{\hat{i}_{o1}}{\hat{d}_1}\right|_{\hat{d}_2=0} \hat{d}_1 + \left.\frac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}_1=0} \hat{d}_2 \tag{6.16}$$

$$\hat{i}_{o2}(\hat{d}_1, \hat{d}_2) = \left.\frac{\hat{i}_{o2}}{\hat{d}_1}\right|_{\hat{d}_2=0} \hat{d}_1 + \left.\frac{\hat{i}_{o2}}{\hat{d}_2}\right|_{\hat{d}_1=0} \hat{d}_2. \tag{6.17}$$

In addition to the converter transfer functions having duty ratios as inputs, it is possible to derive the converter transfer functions having any other independent signal as an input. For instance, we may deactivate *both* duty ratios and activate $\hat{i}_{load}$ in Figure 6-5. In that case, we can find some interesting converter transfer functions, e.g. from the load current to the load voltage or from the load current to the first converter's output current. The corresponding superposition expressions above are expanded as follows:

$$\hat{v}(\hat{d}_1, \hat{d}_2, \hat{i}_{load}) = \left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0} \hat{d}_1 + \left.\frac{\hat{v}}{\hat{d}_2}\right|_{\hat{d}_1=0} \hat{d}_2 + \left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{\hat{d}_1=\hat{d}_2=0} \hat{i}_{load} \tag{6.18}$$

$$\hat{i}_{o1}(\hat{d}_1, \hat{d}_2, \hat{i}_{load}) = \left.\frac{\hat{i}_{o1}}{\hat{d}_1}\right|_{\hat{d}_2=0} \hat{d}_1 + \left.\frac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}_1=0} \hat{d}_2 + \left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{\hat{d}_1=\hat{d}_2=0} \hat{i}_{load}. \tag{6.19}$$

The two additional converter transfer functions having $\hat{i}_{load}$ as the input will also be derived here. A block diagram representation of the superposition expressions above is shown in Figure 6-6. This block diagram represents the dynamical behavior of the multi-converter system. It is analogous to the block diagram in Figure 6-3 for single converter systems. This section is focused deriving the converter transfer functions in the blocks of Figure 6-6. The blocks each correspond to a rational term in the superposition expressions above. Note that this representation only captures the effects of select inputs on select outputs that will be important later in our examples. Neither this representation, nor any representation captures all transfer functions from all inputs to all outputs.

Here we define the following quantities. The impedance Z_L is all of the impedance that shunts the output node, $Z_L \equiv R||Z_{ce1}||Z_{ce2}$ and the effective converter output impedances are $Z_{e1} \equiv Z_{le1}||Z_{ce1}$ and $Z_{e2} \equiv Z_{le2}||Z_{ce2}$, where $Z_{ce1,2} \equiv 1/sC_{e1,2}$ and $Z_{le1,2} \equiv sL_{e1,2}$.

From Figure 6-5, the two terms comprising the load voltage can be written down

by inspection:

$$\left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0} = e_1 M_1 \frac{Z_L||Z_{le2}}{Z_{le1}+Z_L||Z_{le2}} \tag{6.20}$$

$$\left.\frac{\hat{v}}{\hat{d}_2}\right|_{\hat{d}_1=0} = e_2 M_2 \frac{Z_L||Z_{le1}}{Z_{le2}+Z_L||Z_{le1}}. \tag{6.21}$$

These two terms are the converter transfer functions from the duty ratios to load voltage. The expression for the load current follows directly from that for the load voltage, i.e. $\hat{i} = \hat{v}/R$.

Having found the converter transfer functions from duty ratio to load voltage, we can used them to expedite the analyses of the converter output currents as follows. From Figure 6-5, the two terms comprising the first converter's output current are

$$\begin{aligned}\left.\frac{\hat{i}_{o1}}{\hat{d}_1}\right|_{\hat{d}_2=0} &= \left(e_1 M_1 - \left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0}\right)\frac{1}{Z_{le1}} - \left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0}\frac{1}{Z_{ce1}} \\ &= \frac{e_1 M_1}{Z_{le1}} - \left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0}\frac{1}{Z_{e1}}\end{aligned} \tag{6.22}$$

$$\left.\frac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}_1=0} = \left(-\left.\frac{\hat{v}}{\hat{d}_2}\right|_{\hat{d}_1=0}\right)\frac{1}{Z_{e1}} \tag{6.23}$$

Substituting the expressions for output voltage,

$$\left.\frac{\hat{i}_{o1}}{\hat{d}_1}\right|_{\hat{d}_2=0} = \left(\frac{1}{Z_{le1}} - \frac{1}{Z_{e1}}\frac{Z_L||Z_{le2}}{Z_{le1}+Z_L||Z_{le2}}\right)e_1 M_1 \tag{6.24}$$

$$\left.\frac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}_1=0} = -\frac{Z_L||Z_{le1}}{Z_{le2}+Z_L||Z_{le1}}\frac{e_2 M_2}{Z_{e1}} \tag{6.25}$$

The result for the second converter's output current can be found, using symmetry arguments, from the first without too much trouble:

$$\left.\frac{\hat{i}_{o2}}{\hat{d}_1}\right|_{\hat{d}_2=0} = -\frac{Z_L||Z_{le1}}{Z_{le2}+Z_L||Z_{le1}}\frac{e_1 M_1}{Z_{e2}} \tag{6.26}$$

$$\left.\frac{\hat{i}_{o2}}{\hat{d}_2}\right|_{\hat{d}_1=0} = \left(\frac{1}{Z_{le2}} - \frac{1}{Z_{e2}}\frac{Z_L||Z_{le2}}{Z_{le1}+Z_L||Z_{le2}}\right)e_2 M_2. \tag{6.27}$$

Having derived the converter transfer functions with duty ratios as inputs, we now derive the converter transfer functions having the load current perturbation as an input. From Figure 6-5, we have the two constraints:

$$\hat{i}_{o1} = \left(\hat{i}_{load} + \frac{\hat{v}}{R}\right)\frac{Z_{e2}}{Z_{e1}+Z_{e2}} \tag{6.28}$$

$$\hat{v} = -\hat{i}_{o1}Z_{e1}. \tag{6.29}$$

Combining these two constraints,

$$\hat{i}_{o1} = \left(\hat{i}_{load} - \frac{\hat{i}_{o1}Z_{e1}}{R}\right)\frac{Z_{e2}}{Z_{e1}+Z_{e2}} \tag{6.30}$$

simplifying and collecting terms,

$$\frac{\hat{i}_{o1}}{\hat{i}_{load}} = \frac{\frac{Z_{e2}}{Z_{e1}+Z_{e2}}}{1+\frac{Z_{e1}}{R}\frac{Z_{e2}}{Z_{e1}+Z_{e2}}} \tag{6.31}$$

$$= \frac{Z_{e2}}{Z_{e1}+Z_{e2}+\frac{Z_{e1}Z_{e2}}{R}}. \tag{6.32}$$

Combining the result for $\frac{\hat{i}_{o1}}{\hat{i}_{load}}$ above with the second constraint leads to

$$\frac{\hat{v}}{\hat{i}_{load}} = -\frac{\hat{i}_{o1}}{\hat{i}_{load}}Z_{e1} \tag{6.33}$$

$$= -\frac{Z_{e1}Z_{e2}}{Z_{e1}+Z_{e2}+\frac{Z_{e1}Z_{e2}}{R}}. \tag{6.34}$$

It is convenient to define the following quantities:

$$\lambda_1 \equiv \frac{Z_L||Z_{le2}}{Z_{le1}+Z_L||Z_{le2}} \tag{6.35}$$

$$\lambda_2 \equiv \frac{Z_L||Z_{le1}}{Z_{le2}+Z_L||Z_{le1}}. \tag{6.36}$$

These factors may be viewed as the impedance divider ratio from the open circuit converter output voltage to the load voltage for the first and second converter's respectively.

The converter transfer functions are summarized here

$$\left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{d}_2=0} = e_1 M_1 \lambda_1 \tag{6.37}$$

$$\left.\frac{\hat{v}}{\hat{d}_2}\right|_{\hat{d}_1=0} = e_2 M_2 \lambda_2 \tag{6.38}$$

$$\left.\frac{\hat{i}}{\hat{d}_1}\right|_{\hat{d}_2=0} = \frac{1}{R} e_1 M_1 \lambda_1 \tag{6.39}$$

$$\left.\frac{\hat{i}}{\hat{d}_2}\right|_{\hat{d}_1=0} = \frac{1}{R} e_2 M_2 \lambda_2 \tag{6.40}$$

$$\left.\frac{\hat{i}_{o1}}{\hat{d}_1}\right|_{\hat{d}_2=0} = \left(\frac{1}{Z_{le1}} - \frac{1}{Z_{e1}}\lambda_1\right) e_1 M_1 \tag{6.41}$$

$$\left.\frac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}_1=0} = -\lambda_2 \frac{e_2 M_2}{Z_{e1}} \tag{6.42}$$

$$\left.\frac{\hat{i}_{o2}}{\hat{d}_1}\right|_{\hat{d}_2=0} = -\lambda_1 \frac{e_1 M_1}{Z_{e2}} \tag{6.43}$$

$$\left.\frac{\hat{i}_{o2}}{\hat{d}_2}\right|_{\hat{d}_1=0} = \left(\frac{1}{Z_{le2}} - \frac{1}{Z_{e2}}\lambda_2\right) e_2 M_2 \tag{6.44}$$

$$\left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{\hat{d}_1=\hat{d}_2=0} = -\frac{Z_{e1} Z_{e2}}{Z_{e1} + Z_{e2} + \frac{Z_{e1} Z_{e2}}{R}} \tag{6.45}$$

$$\left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{\hat{d}_1=\hat{d}_2=0} = \frac{Z_{e2}}{Z_{e1} + Z_{e2} + \frac{Z_{e1} Z_{e2}}{R}} \tag{6.46}$$

Several linear combinations and transformations of the converter transfer functions above will be useful for computing closed-loop transfer functions. For instance, the load voltage:

$$\hat{v}(\hat{d}_1, \hat{d}_2) = M_1 \lambda_1 e_1 \hat{d}_1 + M_2 \lambda_2 e_2 \hat{d}_2; \tag{6.47}$$

the load current:

$$\hat{i}(\hat{d}_1, \hat{d}_2) = \frac{1}{R}\left(M_1 \lambda_1 e_1 \hat{d}_1 + M_2 \lambda_2 e_2 \hat{d}_2\right); \tag{6.48}$$

the first converter's output current:

$$\hat{i}_{o1}(\hat{d}_1, \hat{d}_2) = M_1 \left(\frac{1}{Z_{le1}} - \frac{1}{Z_{e1}}\lambda_1\right) e_1 \hat{d}_1 - M_2 \lambda_2 \frac{e_2 \hat{d}_2}{Z_{e1}}; \tag{6.49}$$

the second converter's output current:

$$\hat{i}_{o2}(\hat{d}_1, \hat{d}_2) = M_2 \left(\frac{1}{Z_{le2}} - \frac{1}{Z_{e2}} \lambda_2 \right) e_2 \hat{d}_2 - M_1 \lambda_1 \frac{e_1 \hat{d}_1}{Z_{e2}}. \tag{6.50}$$

Also, the first converter input current can be found using KCL in Figure 6-5:

$$\hat{i}_{in1}(\hat{d}_1, \hat{d}_2) = j_1 \hat{d}_1 + M_1 \left(\hat{i}_{o1}(\hat{d}_1, \hat{d}_2) + \frac{\hat{v}(\hat{d}_1, \hat{d}_2)}{Z_{ce1}} \right). \tag{6.51}$$

Finally, the results in (6.47)-(6.51) may be simplified in the case that the two converters are sufficiently identical, i.e. $M_1 = M_2 = M$, $Z_{le1} = Z_{le2} = Z_{le}$, $Z_{e1} = Z_{e2} = Z_e$, $\lambda_1 = \lambda_2 = \lambda$:

$$\hat{v}(\hat{d}_1, \hat{d}_2) = M\lambda \left(e_1 \hat{d}_1 + e_2 \hat{d}_2 \right) \tag{6.52}$$

$$\hat{i}(\hat{d}_1, \hat{d}_2) = \frac{M\lambda}{R} \left(e_1 \hat{d}_1 + e_2 \hat{d}_2 \right) \tag{6.53}$$

$$\hat{i}_{o1}(\hat{d}_1, \hat{d}_2) = M \left(\frac{e_1 \hat{d}_1}{Z_{le}} - \frac{1}{Z_e} \lambda \left(e_1 \hat{d}_1 + e_2 \hat{d}_2 \right) \right) \tag{6.54}$$

$$\hat{i}_{o2}(\hat{d}_1, \hat{d}_2) = M \left(\frac{e_2 \hat{d}_2}{Z_{le}} - \frac{1}{Z_e} \lambda \left(e_2 \hat{d}_2 + e_1 \hat{d}_1 \right) \right) \tag{6.55}$$

$$\hat{i}_{in1}(\hat{d}_1, \hat{d}_2) = j_1 \hat{d}_1 + M^2 \left(\frac{e_1 \hat{d}_1}{Z_{le}} + \left(\frac{1}{Z_{ce}} - \frac{1}{Z_e} \right) \lambda \left(e_1 \hat{d}_1 + e_2 \hat{d}_2 \right) \right). \tag{6.56}$$

6.6 Regulator Example 1: Dual Voltage-mode Regulated Power System

The linearized circuit in Figure 6-7 is a linearized model of a multi-converter power system with two power converters under voltage-mode feedback control. It includes the general linearized multi-converter model from Figure 6-5 as well as linearized blocks comprising the basic components required for feedback control.

Figure 6-8 is a block diagram representation of the dual voltage regulated converter system. The block diagram includes a simplified version of the converter block diagram from Figure 6-6. Because the feedback control for both converters only oper-

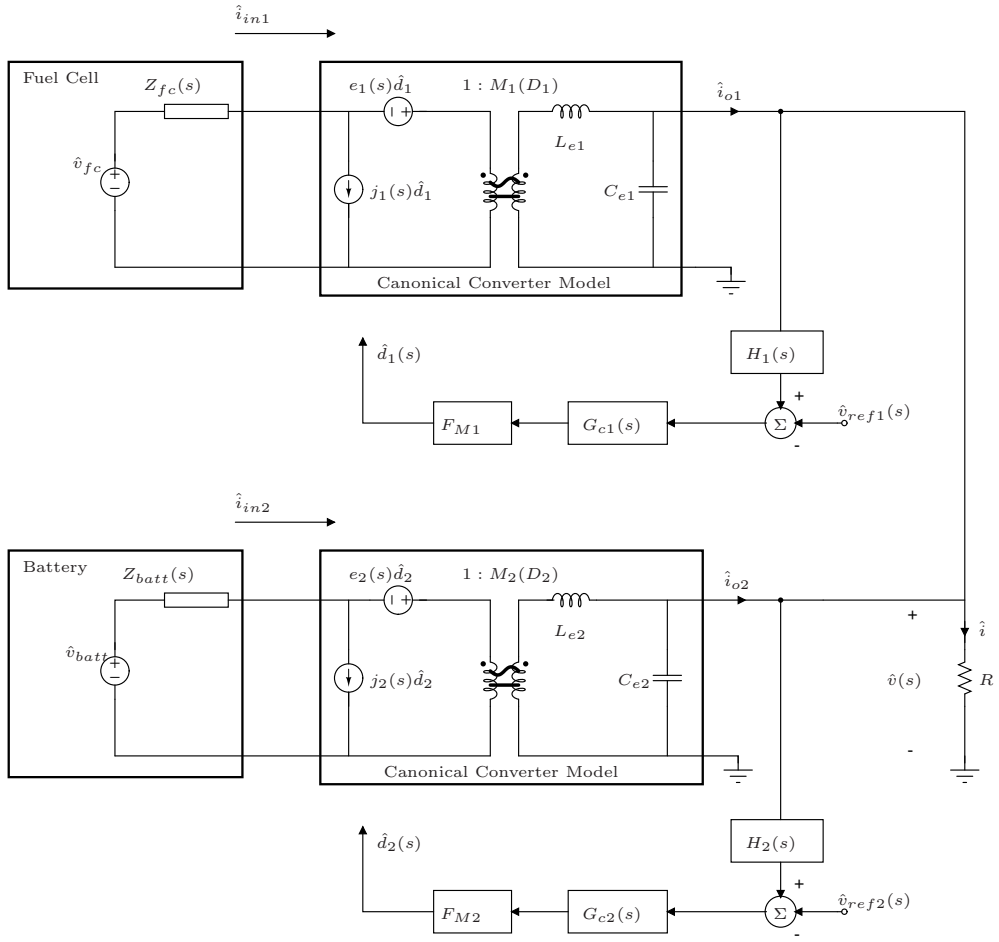


Figure 6-7: Dual voltage regulator system linearized model

ates on the output voltage measurement, the converter output currents are not needed in this example. Also, the load current perturbations will not be considered in this example. The $\times$'s are points that we will break in the block diagram to evaluate loop transfer functions.

Intuitively, we expect this system to enable the run time integral diagnostics functionality described in the introduction. The two voltage regulated converters should behave as low impedance outputs at the load. In generating an excitation current for EIS measurements of one source, that current should be diverted away from the load and into the output of the opposite converter. Thus the limitations that would normally come with and EIS-enabled single converter system are already overcome with this simple approach.

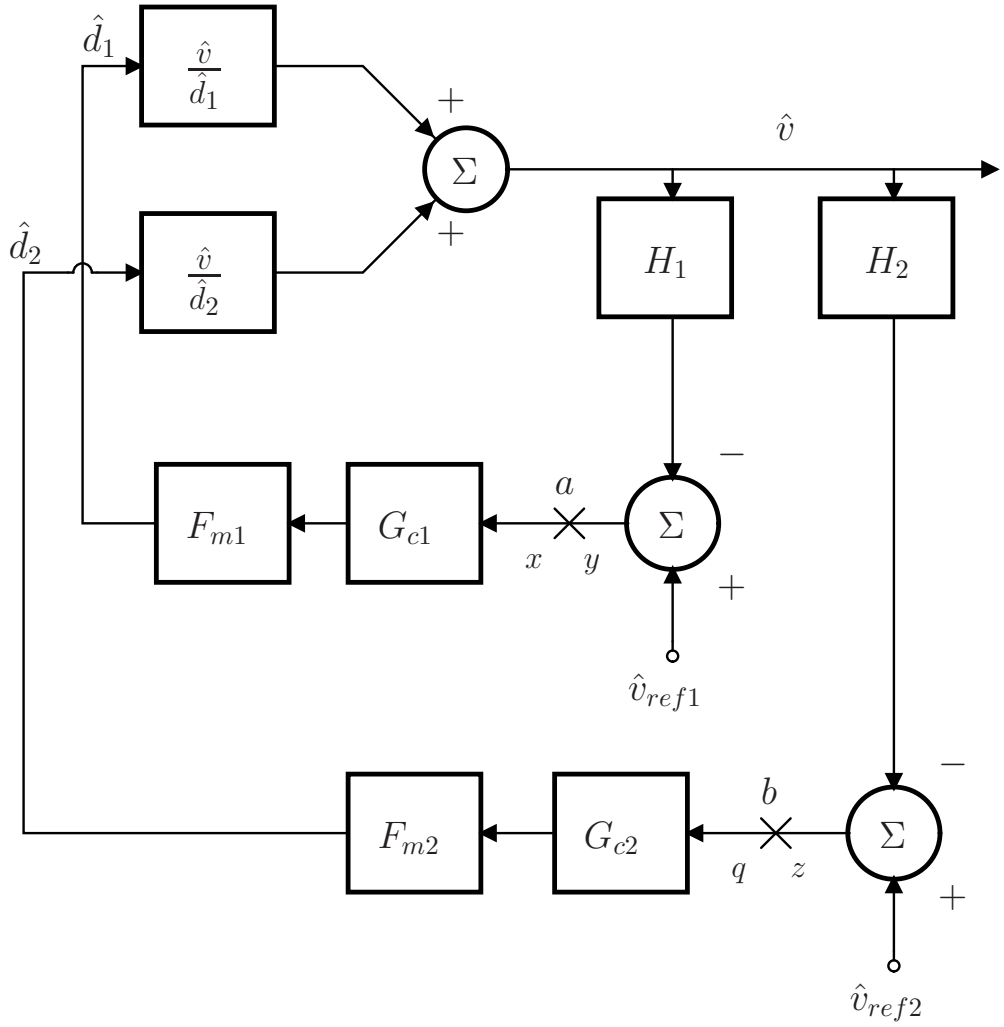


Figure 6-8: Dual voltage regulator system block diagram

6.6.1 Closed-Loop Transfer Functions

Here we consider the system in Figures 6-7 and 6-8 in which the second reference voltage is purely DC, but the first reference voltage is used as a control input. Thus, $\hat{v}_{ref1}$ is designated the "control voltage." That is,

$$\hat{v}_{ref1} \neq 0 \tag{6.57}$$

$$\hat{v}_{ref2} = 0. \tag{6.58}$$

In this case, the two duty ratios become

$$\hat{d}_1 = F_{m1}G_{c1}\left(\hat{v}_{ref1} - H_1\hat{v}\right) \tag{6.59}$$

$$\hat{d}_2 = -F_{m2}G_{c2}H_2\hat{v}, \tag{6.60}$$

in which it is explicit that, upon addition of voltage-mode feedback control, both duty ratios now exhibit a functional dependence on the load voltage, $\hat{v}$. In this system, $\hat{d}_1$ also has a functional dependence on the reference voltage $\hat{v}_{ref1}$ which has been taken as a small-signal control input. For simplicity, the rest of this analysis assumes identical feedback loops so that $F_{m1} = F_{m2} \equiv F_m$, $G_{c1} = G_{c2} \equiv G_c$, $H_1 = H_2 \equiv H$, $e_1 = e_2 \equiv e$, $j_1 = j_2 \equiv j$. With these simplifications,

$$e_1\hat{d}_1 + e_2\hat{d}_2 = e(\hat{d}_1 + \hat{d}_2) \tag{6.61}$$

and the duty ratios become

$$\hat{d}_1 = F_mG_c(\hat{v}_{ref1} - H\hat{v}) \tag{6.62}$$

$$\hat{d}_2 = -F_mG_cH\hat{v} \tag{6.63}$$

so that

$$e(\hat{d}_1 + \hat{d}_2) = e\left(F_mG_c(\hat{v}_{ref1} - 2\hat{v}H)\right) \tag{6.64}$$

$$e_1\hat{d}_1 = eF_mG_c\left(\hat{v}_{ref1} - H\hat{v}\right) \tag{6.65}$$

$$e_2\hat{d}_2 = -eF_mG_cH\hat{v}. \tag{6.66}$$

Here we consider the closed-loop transfer functions, $\frac{\hat{v}}{\hat{v}_{ref1}}$, $\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}$, $\frac{\hat{i_{o2}}}{\hat{i}_{o1}}$, and $\frac{\hat{i_{in1}}}{\hat{v}_{ref1}}$.

Closed Loop Transfer Function $\frac{\hat{v}}{\hat{v}_{ref1}}$:

From equation (6.47), the output voltage becomes

$$\hat{v} = M\lambda eF_mG_c\left(\hat{v}_{ref1} - 2H\hat{v}\right) \tag{6.67}$$

so that collecting terms leads to

$$\hat{v}\left(1+2HM\lambda eF_mG_c\right)=M\lambda eF_mG_c\hat{v}_{ref1} \tag{6.68}$$

and dividing by $\hat{v}_{ref1}$ yields the transfer function,

$$\frac{\hat{v}}{\hat{v}_{ref1}}=\frac{MeF_mG_c\lambda}{1+2MeF_mG_cH\lambda}. \tag{6.69}$$

It will be convenient to define the following quantity at this point:

$$T\equiv MeF_mG_cH, \tag{6.70}$$

so that the transfer function can be re-written:

$$\boxed{\frac{\hat{v}}{\hat{v}_{ref1}}=\frac{1}{H}\frac{T\lambda}{1+2T\lambda}}. \tag{6.71}$$

Closed Loop Transfer Function $\frac{\hat{i}}{\hat{v}_{ref1}}$:

The transfer function $\frac{\hat{i}}{v_{ref1}}$ can be taken from $\frac{\hat{v}}{v_{ref1}}$ quite simply as follows, i.e. $\hat{i}=\hat{v}/R$:

$$\boxed{\frac{\hat{i}}{\hat{v}_{ref1}}=\frac{1}{HR}\frac{T\lambda}{1+2T\lambda}}. \tag{6.72}$$

Closed Loop Transfer Function $\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}$:

From equation (6.49), the first converter's output current becomes

$$\hat{i}_{o1}=M\left(\frac{1}{Z_{le}}eF_mG_c(\hat{v}_{ref1}-H\hat{v})-\frac{1}{Z_e}\lambda eF_mG_c(\hat{v}_{ref1}-2H\hat{v})\right) \tag{6.73}$$

so that dividing by $\hat{v}_{ref1}$ leads to

$$\begin{aligned}\frac{\hat{i}_{o1}}{\hat{v}_{ref1}} &= M\left(\frac{1}{Z_{le}}eF_mG_c\left(1-H\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)\right)-\frac{1}{Z_e}\lambda eF_mG_c\left(1-2H\frac{v}{\hat{v}_{ref1}}\right)\right)\\ &= M\left(\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)\left(\frac{1}{Z_e}\lambda eF_mG_c2H-\frac{1}{Z_{le}}eF_mG_cH\right)+\frac{1}{Z_{le}}eF_mG_c-\frac{1}{Z_e}\lambda eF_mG_c\right)\\ &= \left(\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)\left(\frac{2\lambda T}{Z_e}-\frac{T}{Z_{le}}\right)+\frac{T}{HZ_{le}}-\frac{\lambda T}{HZ_e}\right)\\ &= \left(\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)\left(\frac{2\lambda T}{Z_e}-\frac{T}{Z_{le}}\right)+\frac{T}{H}\left(\frac{1}{Z_{le}}-\frac{\lambda}{Z_e}\right)\right),\end{aligned} \tag{6.74}$$

in which the expression for $\frac{\hat{v}}{\hat{v}_{ref1}}$ may be substituted from the results above leading to

$$\frac{\hat{i}_{o1}}{\hat{v}_{ref1}} = \frac{1}{Z_e}\left(\frac{1}{H}\frac{T\lambda}{1+2T\lambda}\left(\frac{2\lambda T}{Z_e}-\frac{T}{Z_{le}}\right)+\frac{T}{H}\left(\frac{1}{Z_{le}}-\frac{\lambda}{Z_e}\right)\right). \tag{6.75}$$

Simplifying yields the transfer function,

$$\boxed{\frac{\hat{i}_{o1}}{\hat{v}_{ref1}} = \frac{T}{HZ_e}\left(\frac{\lambda T(\frac{2\lambda}{Z_e}-\frac{1}{Z_{le}})}{1+2T\lambda}+\frac{1}{Z_{le}}-\frac{\lambda}{Z_e}\right)}. \tag{6.76}$$

Closed Loop Transfer Function $\frac{\hat{i}_{o2}}{v_{ref1}}$:

From equation (6.50), the second converter's output current becomes

$$\hat{i}_{o2} = M\left(-\frac{eF_mG_cH\hat{v}}{Z_{le}}-\frac{\lambda eF_mG_c}{Z_e}(\hat{v}_{ref1}-2H\hat{v})\right) \tag{6.77}$$

so that dividing by $\hat{v}_{ref1}$ leads to

$$\begin{aligned}\frac{\hat{i}_{o2}}{\hat{v}_{ref1}} &= M\left(-\frac{eF_mG_cH}{Z_{le}}\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)-\frac{\lambda eF_mG_c}{Z_e}\left(1-2H\left(\frac{v}{\hat{v}_{ref1}}\right)\right)\right)\\ &= \left(\frac{\hat{v}}{\hat{v}_{ref1}}\left(\frac{2\lambda T}{Z_e}-\frac{T}{Z_{le}}\right)-\frac{\lambda T}{HZ_e}\right).\end{aligned} \tag{6.78}$$

in which the expression for $\frac{\hat{v}}{\hat{v}_{ref1}}$ may be substituted from the results above leading to

$$\frac{\hat{i}_{o2}}{\hat{v}_{ref1}} = \left(\frac{1}{H} \frac{T\lambda}{1+2T\lambda} \left(\frac{2\lambda T}{Z_e} - \frac{T}{Z_{le}} \right) - \frac{\lambda T}{H Z_e} \right). \tag{6.79}$$

Simplifying in two steps leads to

$$\boxed{\frac{\hat{i}_{o2}}{\hat{v}_{ref1}} = \frac{\lambda T}{H} \left(\frac{T(\frac{2\lambda}{Z_e} - \frac{1}{Z_{le}})}{1+2T\lambda} - \frac{1}{Z_e} \right)}. \tag{6.80}$$

Closed Loop Transfer Function $\frac{\hat{i}_{o2}}{\hat{i}_{o1}}$:

The ratio of the first converter's output current to the second converter's output current under excitation from $\hat{v}_{ref1}$ can be found using a linear combination of two of the transfer functions above. That is

$$\frac{\hat{i}_{o2}}{\hat{i}_{o1}} = \frac{\hat{i}_{o2}}{v_{ref1}} \left(\frac{\hat{i}_{o1}}{v_{ref1}} \right)^{-1} \tag{6.81}$$

leading to

$$\boxed{\frac{\hat{i}_{o2}}{\hat{i}_{o1}} = \frac{\frac{\lambda T}{H} \left(\frac{T(\frac{2\lambda}{Z_e} - \frac{1}{Z_{le}})}{1+2T\lambda} - \frac{1}{Z_e} \right)}{\frac{\lambda T(\frac{2\lambda}{Z_e} - \frac{1}{Z_{le}})}{1+2T\lambda} + \frac{1}{Z_{le}} - \frac{\lambda}{Z_e}}}. \tag{6.82}$$

Note that it would be a misinterpretation to view this ratio as "the output current to the second converter upon injecting an output current to the first converter" because the denominator in this ratio was *not* the input signal in this case.

Closed Loop Transfer Function $\frac{\hat{i}_{in1}}{v_{ref1}}$:

Finally, the transfer function from control voltage to the first converter's input current can be found as follows. From equation (6.51), the first converter's input current becomes

$$\hat{i}_{in1} = jF_m G_c \left(\hat{v}_{ref1} - H\hat{v} \right) + M \left(\hat{i}_{o1} + \frac{\hat{v}}{Z_{ce1}} \right). \tag{6.83}$$

so that dividing by the control voltage yields

$$\boxed{\frac{\hat{i}_{in1}}{\hat{v_{ref1}}} = jF_mG_c\left(1 - H\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)\right) + M\left(\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}\right) + \frac{M}{Z_{ce}}\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)}, \tag{6.84}$$

in which the transfer functions $\frac{\hat{v}}{\hat{v}_{ref1}}$ and $\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}$ have already been derived above so no further simplification is required.

Summary

The results above are summarized here having substituted in the results for the converter transfer functions:

$$\frac{\hat{v}}{\hat{v}_{ref1}} = \frac{1}{H}\frac{\lambda T}{1+2T\lambda} \tag{6.85}$$

$$\frac{\hat{i}_{o1}}{\hat{v}_{ref1}} = \frac{T}{H}\left(\frac{\lambda T(\frac{2\lambda}{Z_e} - \frac{1}{Z_{le}})}{1+2T\lambda} + \frac{1}{Z_{le}} - \frac{\lambda}{Z_{le}}\right) \tag{6.86}$$

$$\frac{\hat{i}_{o2}}{\hat{i}_{o1}} = \frac{\frac{\lambda T}{H}\left(\frac{T(\frac{2\lambda}{Z_e} - \frac{1}{Z_{le}})}{1+2T\lambda} - \frac{1}{Z_e}\right)}{\left(\frac{\lambda T(\frac{2\lambda}{Z_e} - \frac{1}{Z_{le}})}{1+2T\lambda} + \frac{1}{Z_{le}} - \frac{\lambda}{Z_e}\right)} \tag{6.87}$$

$$\frac{\hat{i}_{in1}}{\hat{v_{ref1}}} = jF_mG_c\left(1 - H\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)\right) + M\left(\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}\right) + \frac{M}{Z_{ce}}\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right), \tag{6.88}$$

where we have defined

$$T \equiv HG_cF_meM \tag{6.89}$$

$$\lambda \equiv \frac{Z_L||Z_{le}}{Z_{le} + Z_{le}||Z_L}. \tag{6.90}$$

Discussion

From the results in (6.85)-(6.88), some interesting observations can be made about the behavior of the system in Figure 6-7. Equation (6.85) describes the output voltage variation in response to the control voltage. For large T, that transfer function approaches $1/2H$. For a sensor gain of unity ($H = 1$), the result is 1/2. Perturbing

the reference voltage for one converter in this two-converter system, perturbs the output voltage, half as much as it would in a single-converter system.

Equation (6.86) describes the first converter's output current variation in response to the control voltage. For large T, that transfer function approaches T/HZ_{le}. For a sensor gain of unity ($H = 1$), the result is T/Z_{le}. Equation (6.87) says that for large T, the second converter's output current is the opposite of the first converter's output current. That is, small-signal currents flow out of one converter and into the other. This behavior is consistent with the intuition that each converter, operating under voltage-mode feedback control, behaves as a low impedance to the load.

Equation (6.88) describes the first converter's input current variation in response to the control voltage. For large T, that transfer function approaches $M\left(\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}\right)$ because $\left(\frac{\hat{v}}{\hat{v}_{ref1}}\right)$ approaches $1/H$. The first converter's input current is largely its output current reflected back through the ideal transformer with transformation ratio M.

Dividing the limiting results for the load voltage response and the first converter's input current response leads to $\frac{1/2H}{MT/Z_{le}}$. Because the loop gain is in the denominator, this is a small quantity. Therefore, the control voltage amplitude needed to generate suitable excitation currents should lead to relatively small load voltage perturbations.

6.6.2 Open-Loop Transfer Functions

The open-loop transfer functions are needed, most notably to investigate the stability of the regulator. For this purpose, we examine the block diagram in Figure 6-8. Breaking the loop at one point for each error signal, e.g. points a and b, will reveal the required transfer functions. The open-loop transfer functions can be viewed as a measure of the signal that returns having broken the loop and injected a signal at the break. By convention, the open-loop transfer functions are the negative of that

ratio. Mathematically

$$T_1 = -\frac{y}{x} \tag{6.91}$$

$$T_2 = -\frac{z}{q}. \tag{6.92}$$

In the case of two voltage feedback loops, these transfer functions are

$$T_1 = H_1\frac{\hat{v}}{x} \tag{6.93}$$

$$T_2 = H_2\frac{\hat{v}}{q}. \tag{6.94}$$

Expanding the measured signal, $\hat{v}$, using linear superposition casts the transfer functions in a more useful form

$$T_1 = H_1\left(\frac{\hat{d}_1}{x}\frac{\hat{v}}{\hat{d}_1} + \frac{\hat{d}_2}{x}\frac{\hat{v}}{\hat{d}_2}\right) \tag{6.95}$$

$$T_2 = H_2\left(\frac{\hat{d}_2}{q}\frac{\hat{v}}{\hat{d}_2} + \frac{\hat{d}_1}{q}\frac{\hat{v}}{\hat{d}_1}\right). \tag{6.96}$$

The converter transfer functions $\frac{\hat{v}}{\hat{d}_1}$ and $\frac{\hat{v}}{\hat{d}_2}$ have already been determined. What is left is to compute the transfer functions $\frac{\hat{d}_1}{x}$, $\frac{\hat{d}_2}{x}$, $\frac{\hat{d}_1}{q}$, $\frac{\hat{d}_2}{q}$ as determined by the feedback structure.

The needed transfer functions may be found by inspecting the block diagram. The duty ratios are

$$\hat{d}_1 = xG_{c1}F_{m1} \tag{6.97}$$

and

$$\hat{d}_2 = -F_{m2}G_{c2}H_2\left(\hat{d}_1\frac{\hat{v}}{\hat{d}_1} + \hat{d}_2\frac{\hat{v}}{\hat{d}_2}\right) \tag{6.98}$$

so that

$$\frac{\hat{d}_1}{x} = G_{c1}F_{m1} \tag{6.99}$$

and

$$\frac{\hat{d}_2}{x} = -F_{m2}G_{c2}H_2\left(\frac{\hat{d}_1}{x}\frac{\hat{v}}{\hat{d}_1} + \frac{\hat{d}_2}{x}\frac{\hat{v}}{\hat{d}_2}\right). \tag{6.100}$$

Solving the system of equations above yields the needed transfer functions

$$\frac{\hat{d}_1}{x} = G_{c1}F_{m1} \tag{6.101}$$

and

$$\frac{\hat{d}_2}{x} = -\frac{F_{m2}G_{c2}H_2G_{c1}F_{m1}\frac{\hat{v}}{\hat{d}_1}}{1 + F_{m2}G_{c2}H_2\frac{\hat{v}}{\hat{d}_2}}. \tag{6.102}$$

The equivalent transfer functions for the second loop are trivial because of the symmetry in this example.

Combining the transfer functions in (6.101)-(6.102) with the converter transfer functions (6.37)-(6.38) and substituting into the expressions in (6.95)-(6.96) will yield the loop transfer functions required to evaluate the stability of the dual voltage regulated system.

Discussion

For large, $T = F_mG_cH$, the second transfer function approaches $G_{c1}F_{m1}H_1\frac{\hat{v}/\hat{d}_1}{\hat{v}/\hat{d}_2}$. Inserting this expression and the exact expression for $\frac{\hat{d}_1}{x}$ into the loop gain, T_1 from (6.95) leads to

$$T_1 \approx 2H_1G_{c1}F_{m1}. \tag{6.103}$$

The second loop transfer function similarly approaches

$$T_2 \approx 2H_2G_{c2}F_{m2}. \tag{6.104}$$

Thus the two loop transfer functions approach twice the loop transfer functions for two separate single converter systems. This result is due to the symmetrical nature of the regulator considered in this example.

6.7 Regulator Example 2: Master-Slave Current-Voltage Regulated Power System

The linearized circuit in Figure 6-9 is a linearized model of a multi-converter power system with two power converters, one under voltage-mode feedback control and the other under output current-mode feedback control. This system is sometimes called a master-slave current-voltage regulated system. The linearized model includes the general linearized multi-converter model from Figure 6-5 as well as linearized blocks comprising the basic components required for feedback control.

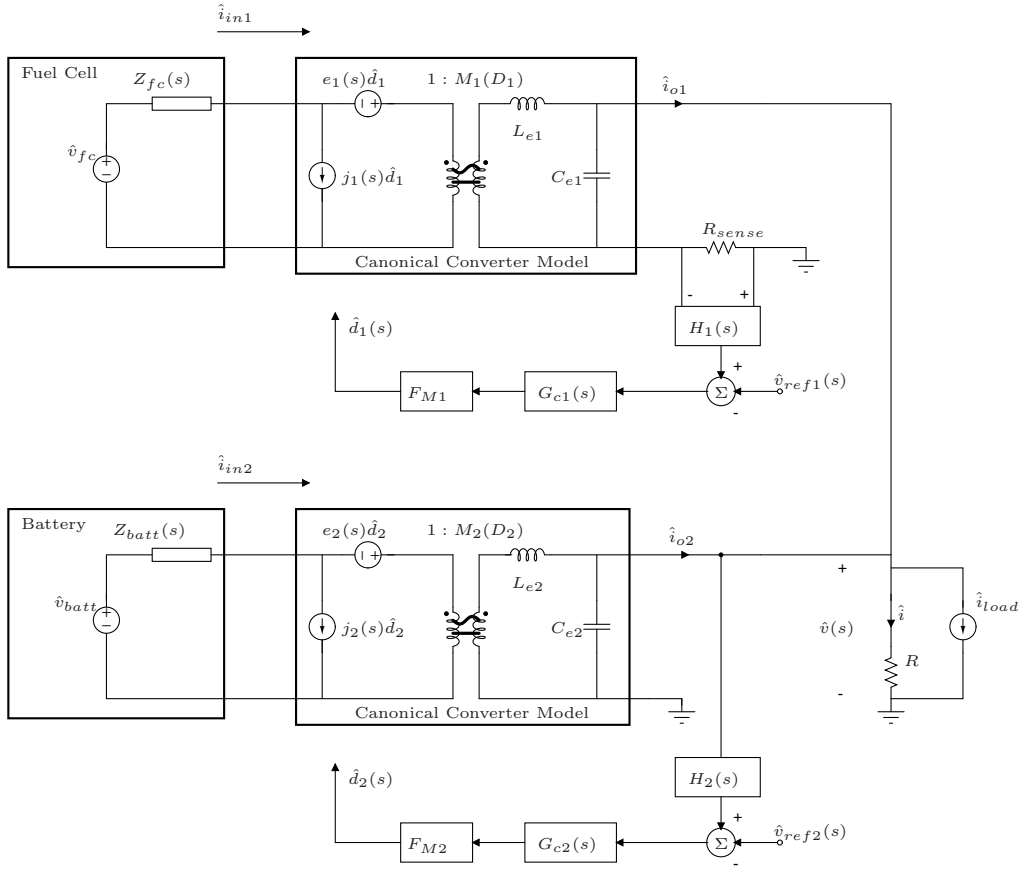


Figure 6-9: Master-slave regulator system linearized model

Figure 6-10 is a block diagram representation of the master-slave regulated converter system. The block diagram includes the converter block diagram from Figure 6-6. The $\times$'s are points that we will break in the block diagram to evaluate loop transfer functions.

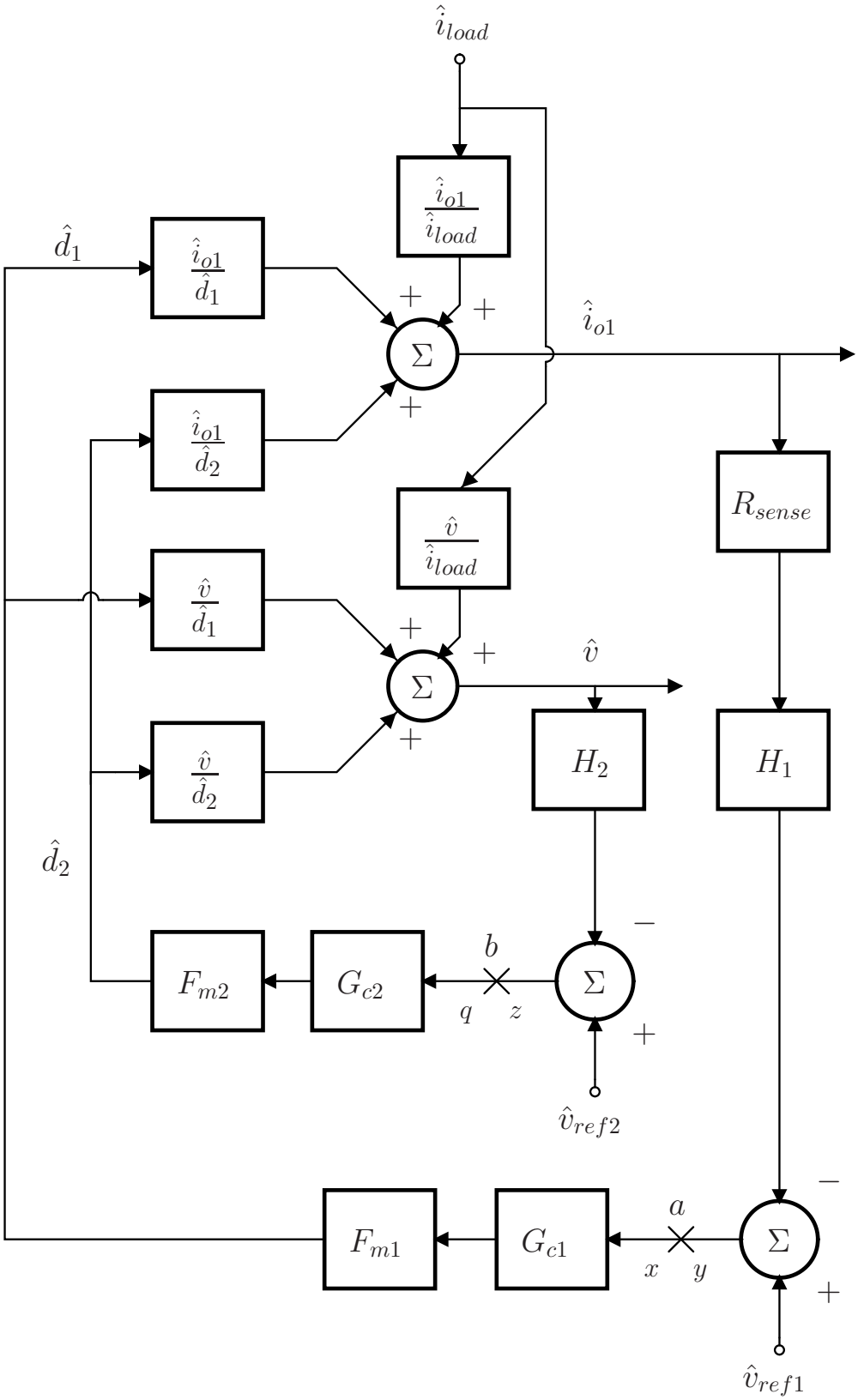


Figure 6-10: Master-slave regulator system block diagram

Intuitively, we expect this system to enable the run time integral diagnostics functionality described in the introduction. The voltage regulated converter should behave as a low impedance output at the load. In generating an excitation current for EIS measurements of the first source, that current should be diverted away from the load and into the output of the voltage-regulated converter. Thus the limitations that would normally come with and EIS-enabled single converter system are overcome with this approach. Also, because the first converter is current-regulated, its output current should remain fixed despite load current perturbations. We will see that this also implies a relatively fixed input current to the first converter despite load current perturbations. The voltage-regulated converter naturally accommodates the excess load current, whether it be positive or negative. Thus the master-slave system can achieve the current buffering feature needed for fuel cell power processing in applications having widely varying load power.

6.7.1 Closed-loop Transfer Functions

Here we consider the system in Figures 6-9 and 6-10 in which the second reference voltage is purely DC, but the first reference voltage is used as a control input. Thus, $\hat{v}_{ref1}$ is designated the "control voltage." That is,

$$\hat{v}_{ref1} \neq 0 \tag{6.105}$$

$$\hat{v}_{ref2} = 0. \tag{6.106}$$

In this case, the two duty ratios become

$$\hat{d}_1 = F_{m1}G_{c1}\left(\hat{v}_{ref1} - H_1 R_{sense}\hat{i}_{o1}\right) \tag{6.107}$$

$$\hat{d}_2 = -F_{m2}G_{c2}H_2\hat{v}, \tag{6.108}$$

in which it is explicit that, upon addition of voltage-mode and current-mode feedback control, the duty ratios now exhibit a functional dependence on the load voltage, $\hat{v}$, and the first converter's output current, $\hat{i}_{o1}$, respectively. In this system, $\hat{d}_1$ also has

a functional dependence on the reference voltage $\hat{v}_{ref1}$ which has been taken as a small-signal control input. We also consider the case a superimposed load current perturbation. In this case, the two duty ratios are

$$\hat{d}_1 = -F_{m1}G_{c1}H_1R_{sense}\hat{i}_{o1} \tag{6.109}$$

$$\hat{d}_2 = -F_{m2}G_{c2}H_2\hat{v}. \tag{6.110}$$

In contrast to the first example, we do not assume identical converters here. Additionally identical feedback loops is not a valid assumption because the two feedback loops regulate nonequivalent output variables. Because the analysis of this system is somewhat more complicated, we approach the analysis starting from a linear signal decomposition of the transfer functions of interest.

The closed loop transfer functions of interest are $\frac{\hat{v}}{\hat{v}_{ref1}}$, $\frac{\hat{i}}{\hat{v}_{ref1}}$, $\frac{\hat{i_{in1}}}{\hat{v}_{ref1}}$, and $\frac{\hat{i_{in1}}}{\hat{i}_{load}}$. The first three of those closed-loop transfer functions take as an input the control signal $\hat{v}_{ref1}$. The last of those closed-loop transfer functions, $\frac{\hat{i_{in1}}}{\hat{i}_{load}}$, takes the load current perturbation as the input. For the closed loop transfer responses to the input $\hat{i}_{load}$ we leave the results in terms of the already-derived converter transfer functions for brevity. Because $\hat{i}_{load}$ is an external input in both the open-loop and closed-loop cases, the notation for the closed-loop transfer functions from $\hat{i}_{load}$ should be specified to avoid confusion. We will use the following notation to specify the closed-loop transfer functions as opposed to the converter transfer functions from $\hat{i}_{load}$: $\left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{CL}$, $\left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{CL}$.

The closed loop transfer functions may be written as linear decompositions as follows (for the control signal input). The transfer function from the control signal to the load voltage:

$$\left.\frac{\hat{v}}{\hat{v}_{ref1}}\right|_{CL} = \frac{\hat{v}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{v}_{ref1}} + \frac{\hat{v}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{v}_{ref1}}, \tag{6.111}$$

to the load current:

$$\left.\frac{\hat{i}}{\hat{v}_{ref1}}\right|_{CL} = \frac{1}{R}\left(\frac{\hat{v}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{v}_{ref1}} + \frac{\hat{v}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{v}_{ref1}}\right), \tag{6.112}$$

to the first converter's output current:

$$\left.\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}\right|_{CL} = \frac{\hat{i}_{o1}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{v}_{ref1}} + \frac{\hat{i}_{o1}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{v}_{ref1}}, \tag{6.113}$$

and to the second converter's output current:

$$\left.\frac{\hat{i}_{o2}}{\hat{v}_{ref1}}\right|_{CL} = \frac{\hat{i}_{o2}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{v}_{ref1}} + \frac{\hat{i}_{o2}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{v}_{ref1}}. \tag{6.114}$$

Additionally, the first converter's input current can be written as a linear superposition as follows

$$\left.\frac{\hat{i}_{in1}}{\hat{v}_{ref1}}\right|_{CL} = j_1\frac{\hat{d}_1}{\hat{v}_{ref1}} + M_1\left(\left.\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}\right|_{CL} + \left.\frac{\hat{v}}{\hat{v}_{ref1}}\right|_{CL}\frac{1}{Z_{ce1}}\right). \tag{6.115}$$

The closed-loop transfer with the load current perturbation input may be similarly written as follows. The transfer function from the load current to the load voltage:

$$\left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{CL} = \frac{\hat{v}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{i}_{load}} + \frac{\hat{v}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{i}_{load}}, \tag{6.116}$$

to the first converter's output current:

$$\left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{CL} = \frac{\hat{i}_{o1}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{i}_{load}} + \frac{\hat{i}_{o1}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{i}_{load}}, \tag{6.117}$$

and to the second converter's output current:

$$\left.\frac{\hat{i}_{o2}}{\hat{i}_{load}}\right|_{CL} = \frac{\hat{i}_{o2}}{\hat{d}_1}\frac{\hat{d}_1}{\hat{i}_{load}} + \frac{\hat{i}_{o2}}{\hat{d}_2}\frac{\hat{d}_2}{\hat{i}_{load}}. \tag{6.118}$$

Additionally, the first converter's input current can be written as a linear superposition as follows

$$\left.\frac{\hat{i}_{in1}}{\hat{i}_{load}}\right|_{CL} = j_1\frac{\hat{d}_1}{\hat{i}_{load}} + M_1\left(\left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{CL} + \left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{CL}\frac{1}{Z_{ce1}}\right). \tag{6.119}$$

The linear decomposition forms of the closed-loop transfer functions above highlight the contributions of the converter transfer functions and the feedback structure.

The analysis of the closed-loop transfer functions having $\hat{v}_{ref1}$ as the input can be reduced to deriving the transfer functions $\frac{\hat{d}_1}{\hat{v}_{ref1}}$ and $\frac{\hat{d}_2}{\hat{v}_{ref1}}$ based on the feedback control in this particular example. The analysis of the closed-loop transfer functions having $\hat{i}_{load}$ as the input can be reduced to deriving the transfer functions $\frac{\hat{d}_1}{\hat{i}_{load}}$ and $\frac{\hat{d}_2}{\hat{i}_{load}}$ based on the feedback control in this particular example.

Closed Loop Transfer Function $\frac{\hat{d}_2}{\hat{d}_1}$:

From the expressions for the duty ratios above, we have

$$\hat{d}_1 = F_{m1}G_{c1}\left(\hat{v}_{ref1} - H_1 R_{sense}\hat{i}_{o1}(\hat{d}_1, \hat{d}_2)\right). \tag{6.120}$$

Substituting in the expression for $\hat{i}_{o1}$ and solving, we arrive at

$$\hat{d}_1 = \frac{F_{m1}G_{c1}\left(\hat{v}_{ref1} + H_1 R_{sense}M_2\lambda_2\frac{e_2\hat{d}_2}{Z_{e1}}\right)}{1 + F_{m1}G_{c1}H_1R_{sense}M_1\left(\frac{1}{Z_{le1}} - \lambda_1\frac{1}{Z_{e1}}\right)e_1}. \tag{6.121}$$

The expression for the second converter duty ratio provides a second constraint:

$$\hat{d}_2 = -H_2F_{m2}G_{c2}\hat{v}(\hat{d}_1, \hat{d}_2) \tag{6.122}$$

$$\tag{6.123}$$

Substituting in the expression for $\hat{v}$ and solving, we arrive at

$$\hat{d}_2 = -\frac{H_2F_{m2}G_{c2}M_1\lambda_1e_1\hat{d}_1}{1 + H_2F_{m2}G_{c2}M_2\lambda_2e_2}. \tag{6.124}$$

From this second constraint, we identify the intermediate transfer function

$$\boxed{\frac{\hat{d}_2}{\hat{d}_1} = -\frac{H_2F_{m2}G_{c2}M_1\lambda_1e_1}{1 + H_2F_{m2}G_{c2}M_2\lambda_2e_2}}. \tag{6.125}$$

Closed Loop Transfer Function $\frac{\hat{d}_1}{\hat{v}_{ref1}}$:

Replacing $\hat{d}_2$ with the quantity $\hat{d}_1\frac{\hat{d}_2}{\hat{d}_1}$ in the expression for $\hat{d}_1$ above and solving for $\hat{d}_1$ we arrive at

$$\boxed{\frac{\hat{d}_1}{\hat{v}_{ref1}} = \frac{F_{m1}G_{c1}}{\alpha}\left(1 - \frac{F_{m1}G_{c1}H_1R_{sense}M_2\lambda_2\frac{e_2}{Z_{e1}}\frac{\hat{d}_2}{\hat{d}_1}}{\alpha}\right)^{-1},} \tag{6.126}$$

where we define

$$\alpha \equiv 1 + F_{m1}G_{c1}H_1R_{sense}M_1\left(\frac{1}{Z_{le1}} - \lambda_1\frac{1}{Z_{e1}}\right)e_1. \tag{6.127}$$

Closed Loop Transfer Function $\frac{\hat{d}_2}{\hat{v}_{ref1}}$:

The transfer function from the control input to the second duty ratio can then be found using the following transformation

$$\boxed{\frac{\hat{d}_2}{\hat{v}_{ref1}} = \frac{\hat{d}_1}{\hat{v}_{ref1}}\frac{\hat{d}_2}{\hat{d}_1}.} \tag{6.128}$$

Closed Loop Transfer Function $\frac{\hat{d}_1}{\hat{i}_{load}}$:

From the expressions for the duty ratios in the case that $\hat{i}_{load}$ is activated and $\hat{v}_{ref1}$ is deactivated we have

$$\hat{d}_1 = -F_{m1}G_{c1}H_1R_{sense}\left(\hat{d}_1\left(\frac{\hat{i}_{o1}}{\hat{d}_1}\right) + \hat{d}_2\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right) + \hat{i}_{load}\left(\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right)\right) \tag{6.129}$$

It will be useful to identify the following quantities

$$F_1 \equiv F_{m1}G_{c1}H_1R_{sense} \tag{6.130}$$

$$F_2 \equiv F_{m2}G_{c2}H_2. \tag{6.131}$$

Now solving for the first duty ratio we have

$$\hat{d}_1 = -\frac{F_1\left(\hat{d}_2\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right) + \hat{i}_{load}\left(\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right)\right)}{1 + F_1\left(\frac{\hat{i}_{o1}}{\hat{d}_1}\right)}. \tag{6.132}$$

The second duty ratio provides the needed constraint such that

$$\hat{d}_2 = -F_2\left(\hat{d}_1\left(\frac{\hat{v}}{\hat{d}_1}\right) + \hat{d}_2\left(\frac{\hat{v}}{\hat{d}_2}\right) + \hat{i}_{load}\left(\frac{\hat{v}}{\hat{i}_{load}}\right)\right). \tag{6.133}$$

and solving for the second duty ratio leads to

$$\hat{d}_2 = -\frac{F_2\left(\hat{d}_1\left(\frac{\hat{v}}{\hat{d}_1}\right) + \hat{i}_{load}\left(\frac{\hat{v}}{\hat{i}_{load}}\right)\right)}{1 + F_2\left(\frac{\hat{v}}{\hat{d}_2}\right)}. \tag{6.134}$$

Substituting this expression for the second duty ratio into the expression for the first leads to

$$\hat{d}_1 = \frac{F_1\left(\frac{F_2\hat{d}_1\left(\frac{\hat{v}}{\hat{d}_1}\right) + F_2\hat{i}_{load}\left(\frac{\hat{v}}{\hat{i}_{load}}\right)}{1+F_2\left(\frac{\hat{v}}{\hat{d}_2}\right)}\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right) - \hat{i}_{load}\left(\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right)\right)}{1 + F_1\left(\frac{\hat{i}_{o1}}{\hat{d}_1}\right)} \tag{6.135}$$

and solving leads to

$$\boxed{\frac{\hat{d}_1}{\hat{i}_{load}} = \frac{\frac{F_1F_2\left(\frac{\hat{v}}{\hat{i}_{load}}\right)\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right)}{1+F_2\left(\frac{\hat{v}}{\hat{d}_2}\right)} - F_1\left(\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right)}{\left(1 + F_1\left(\frac{\hat{i}_{o1}}{\hat{d}_1}\right)\right)\left(1 - \frac{F_1F_2\left(\frac{\hat{v}}{\hat{d}_1}\right)\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right)\left(1+F_1\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right)\right)}{1+F_2\left(\frac{\hat{v}}{\hat{d}_2}\right)}\right)}}. \tag{6.136}$$

Closed Loop Transfer Function $\frac{\hat{d}_2}{\hat{i}_{load}}$:

The second transfer function can be found having derived the first transfer function simply:

$$\boxed{\frac{\hat{d}_2}{\hat{i}_{load}} = -\frac{F_2\left(\left(\frac{\hat{d}_1}{\hat{i}_{load}}\right)\left(\frac{\hat{v}}{\hat{d}_1}\right) + \left(\frac{\hat{v}}{\hat{i}_{load}}\right)\right)}{1 + F_2\left(\frac{\hat{v}}{\hat{d}_2}\right)}}. \tag{6.137}$$

Summary

Having substituted the results for the converter transfer functions (6.37)-(6.46) into the linear decompositions in (6.114)-(6.115), the results above with $\hat{v}_{ref1}$ as the closed-loop transfer function input are summarized here. The closed-loop transfer function from the control signal to the load voltage:

$$\left.\frac{\hat{v}}{\hat{v}_{ref1}}\right|_{CL} = e_1 M_1 \lambda_1 \frac{\hat{d}_1}{\hat{v}_{ref1}} + e_2 M_2 \lambda_2 \frac{\hat{d}_2}{\hat{v}_{ref1}}, \tag{6.138}$$

to the load current:

$$\left.\frac{\hat{i}}{\hat{v}_{ref1}}\right|_{CL} = \frac{\hat{v}}{\hat{v}_{ref1}} \frac{1}{R}, \tag{6.139}$$

to the first converter's output current:

$$\left.\frac{\hat{i}_{o1}}{\hat{v}_{ref1}}\right|_{CL} = M_1 \left(\frac{1}{Z_{le1}} - \frac{1}{Z_{e1}}\lambda_1\right) e_1 \frac{\hat{d}_1}{\hat{v}_{ref1}} - M_2 \lambda_2 \frac{e_2}{Z_{e1}} \frac{\hat{d}_2}{\hat{v}_{ref1}}, \tag{6.140}$$

and to the first converter's input current:

$$\left.\frac{\hat{i}_{in1}}{\hat{v_{ref1}}}\right|_{CL} = j_1 \frac{\hat{d}_1}{\hat{v}_{ref1}} + M_1 \frac{\hat{i}_{o1}}{\hat{v}_{ref1}} + M_1 \frac{\hat{v}}{\hat{v}_{ref1}} \frac{1}{Z_{ce1}}. \tag{6.141}$$

Additionally, we have found

$$\frac{\hat{d}_2}{\hat{d}_1} = -\frac{H_2 F_{m2} G_{c2} M_1 \lambda_1 e_1}{1 + H_2 F_{m2} G_{c2} M_2 \lambda_2 e_2} \tag{6.142}$$

$$\frac{\hat{d}_1}{\hat{v}_{ref1}} = \frac{F_{m1} G_{c1}}{\alpha} \left(1 - \frac{F_{m1} G_{c1} H_1 R_{sense} M_2 \lambda_2 \frac{e_2}{Z_{e1}} \frac{\hat{d}_2}{\hat{d}_1}}{\alpha}\right)^{-1} \tag{6.143}$$

$$\frac{\hat{d}_2}{\hat{v}_{ref1}} = \frac{\hat{d}_1}{\hat{v}_{ref1}} \frac{\hat{d}_2}{\hat{d}_1} \tag{6.144}$$

and defined

$$\alpha \equiv 1 + F_{m1} G_{c1} H_1 R_{sense} M_1 \left(\frac{1}{Z_{le1}} - \lambda_1 \frac{1}{Z_{e1}}\right) e_1. \tag{6.145}$$

Having substituted the results for the converter transfer functions (6.37)-(6.46) into the linear decompositions in (6.118)-(6.119), the results above with $\hat{i}_{load}$ as the closed-loop transfer function input are summarized here. The closed-loop transfer function from the load current perturbation to the load voltage:

$$\left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{CL} = e_1 M_1 \lambda_1 \frac{\hat{d}_1}{\hat{i}_{load}} + e_2 M_2 \lambda_2 \frac{\hat{d}_2}{\hat{i}_{load}}, \tag{6.146}$$

to the first converter's output current:

$$\left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{CL} = M_1 \left(\frac{1}{Z_{le1}} - \frac{1}{Z_{e1}}\lambda_1\right) e_1 \frac{\hat{d}_1}{\hat{i}_{load}} - M_2 \lambda_2 \frac{e_2}{Z_{e1}} \frac{\hat{d}_2}{\hat{i}_{load}}, \tag{6.147}$$

and to the first converter's input current:

$$\left.\frac{\hat{i}_{in1}}{\hat{i_{load}}}\right|_{CL} = j_1 \frac{\hat{d}_1}{\hat{i}_{load}} + M_1 \left.\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right|_{CL} + M_1 \left.\frac{\hat{v}}{\hat{i}_{load}}\right|_{CL} \frac{1}{Z_{ce1}}. \tag{6.148}$$

Additionally, we have found

$$\frac{\hat{d}_1}{\hat{i}_{load}} = \frac{F_1 F_2 \left(\frac{\hat{v}}{\hat{i}_{load}}\right)\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right) - F_1 \left(\frac{\hat{i}_{o1}}{\hat{i}_{load}}\right)\left(1 + F_2 \left(\frac{\hat{v}}{\hat{d}_2}\right)\right)}{\left(1 + F_1 \left(\frac{\hat{i}_{o1}}{\hat{d}_1}\right)\right)\left(1 + F_2 \left(\frac{\hat{v}}{\hat{d}_2}\right) - F_1 F_2 \left(\frac{\hat{v}}{\hat{d}_1}\right)\left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right)\left(1 + F_1 \left(\frac{\hat{i}_{o1}}{\hat{d}_2}\right)\right)\right)} \tag{6.149}$$

$$\frac{\hat{d}_2}{\hat{1}_{load}} = -\frac{F_2 \left(\left(\frac{\hat{d}_1}{\hat{i}_{load}}\right)\left(\frac{\hat{v}}{\hat{d}_1}\right) + \left(\frac{\hat{v}}{\hat{i}_{load}}\right)\right)}{1 + F_2 \left(\frac{\hat{v}}{\hat{d}_2}\right)} \tag{6.150}$$

and defined

$$F_1 \equiv F_{m1} G_{c1} H_1 R_{sense} \tag{6.151}$$

$$F_2 \equiv F_{m2} G_{c2} H_2. \tag{6.152}$$

Discussion

As the voltage feedback gain, G_{c2}, increases toward ∞, the ratio $\frac{\hat{d}_2}{\hat{d}_1} \to -1$. The load voltage response to perturbations of the other control signal, $\hat{v}_{ref1}$, approaches

the quantity $e_1 M_1 \lambda_1 - e_2 M_2 \lambda_2$, a term that defines the difference between the two converter elements, and will be zero for identical converters. That is as the voltage feedback gain increases, the output voltage is better regulated as expected.

As the loop gains, F_1 and F_2 increase toward ∞, the closed-loop transfer functions $\frac{\hat{d}_1}{\hat{i}_{load}}$ $\frac{\hat{d}_2}{\hat{i}_{load}}$ both collapse. Then, all of the closed-loop transfer functions collapse as well. Significantly, the input current response to load current perturbations collapses implying that the current regulated converter input current is well buffered from transients in the load. Note however that the closed-loop transfer function from $\hat{i}_{load}$ to the first converter's output current depends on the reciprocal of that converters total open-loop output impedance. At zero frequency (DC), an ideal inductor will yield a converter open-loop output impedance of zero so the reciprocal will approach ∞. The dependence of the first converter's input current transfer function on the first converter's output current transfer function leads to the subtle point that the quality of the buffering of the first converter's input current depends quite strongly on the ESR's and other added resistances in series with the first converter's output. Only those resistances comprise the zero frequency total converter output impedance. In other words, the current regulation may be viewed as a means for increasing the open-loop output impedance of the converter. If, however, there is zero open-loop output impedance, e.g. at zero frequency having zero ESR, the current regulation can not present a large output impedance.

6.7.2 Open-Loop Transfer Functions

The open-loop transfer functions can be derived in a similar fashion to those in the first example. Starting from the general expressions and the block diagram in Figure 6-10

$$T_1 = -\frac{y}{x} \tag{6.153}$$

$$T_2 = -\frac{z}{q}. \tag{6.154}$$

In the case of one voltage and one current feedback loop, these transfer functions are

$$T_1 = H_1 R_{sense} \frac{\hat{i}_{o1}}{x} \tag{6.155}$$

$$T_2 = H_2 \frac{\hat{v}}{q}. \tag{6.156}$$

Expanding the measured signals using linear superposition casts the transfer functions in a more useful form

$$T_1 = H_1 R_{sense} \left(\frac{\hat{d}_2}{x} \frac{\hat{i}_{o1}}{\hat{d}_2} + \frac{\hat{d}_1}{x} \frac{\hat{i}_{o1}}{\hat{d}_1} \right) \tag{6.157}$$

$$T_2 = H_2 \left(\frac{\hat{d}_1}{q} \frac{\hat{v}}{\hat{d}_1} + \frac{\hat{d}_2}{q} \frac{\hat{v}}{\hat{d}_2} \right). \tag{6.158}$$

The loop transfer function, T_2, corresponds to the voltage feedback loop evidenced by the converter transfer functions that it depends on most directly and by the error signal that it corresponds to in the block diagram of Figure 6-10. The loop transfer function, T_1, corresponds to the current feedback loop.

The converter transfer functions $\frac{\hat{v}}{\hat{d}_1}$ and $\frac{\hat{i}_{o1}}{\hat{d}_2}$ have already been determined. What is left is to compute the transfer functions $\frac{\hat{d}_1}{x}$, $\frac{\hat{d}_2}{x}$, $\frac{\hat{d}_1}{q}$, $\frac{\hat{d}_2}{q}$ as determined by the feedback structure. The needed transfer functions may be found by inspecting the block diagram. We break the loop at one point at a time to inspect one loop transfer function at a time.

Breaking the loop at point a, the duty ratios are

$$\hat{d}_1 = x G_{c1} F_{m1} \tag{6.159}$$

$$\hat{d}_2 = -F_{m2} G_{c2} H_2 \hat{v} \tag{6.160}$$

$$= -F_{m2} G_{c2} H_2 \left(\frac{\hat{v}}{\hat{d}_1} \hat{d}_1 + \frac{\hat{v}}{\hat{d}_2} \hat{d}_2 \right) \tag{6.161}$$

so that

$$\frac{\hat{d}_1}{x} = G_{c1}F_{m1} \tag{6.162}$$

$$\frac{\hat{d}_2}{x} = -F_{m2}G_{c2}H_2\left(\frac{\hat{v}}{\hat{d}_1}\frac{\hat{d}_1}{x} + \frac{\hat{v}}{\hat{d}_2}\frac{\hat{d}_2}{x}\right). \tag{6.163}$$

Solving the system of equations above yields the needed transfer functions

$$\frac{\hat{d}_1}{x} = G_{c1}F_{m1} \tag{6.164}$$

$$\frac{\hat{d}_2}{x} = -\frac{F_{m2}G_{c2}H_2G_{c1}F_{m1}\frac{\hat{v}}{\hat{d}_1}}{1 + F_{m2}G_{c2}H_2\frac{\hat{v}}{\hat{d}_2}}. \tag{6.165}$$

Breaking the loop at point b, the duty ratios are

$$\hat{d}_2 = qG_{c2}F_{m2} \tag{6.166}$$

$$\hat{d}_1 = -F_{m1}G_{c1}H_1R_{sense}\hat{i}_{o1} \tag{6.167}$$

$$= -F_{m1}G_{c1}H_1R_{sense}\left(\frac{\hat{i}_{o1}}{\hat{d}_1}\hat{d}_1 + \frac{\hat{i}_{o1}}{\hat{d}_2}\hat{d}_2\right) \tag{6.168}$$

so that

$$\frac{\hat{d}_2}{q} = G_{c2}F_{m2} \tag{6.169}$$

$$\frac{\hat{d}_2}{q} = -F_{m1}G_{c1}H_1R_{sense}\left(\frac{\hat{i}_{o1}}{\hat{d}_1}\frac{\hat{d}_1}{q} + \frac{\hat{i}_{o1}}{\hat{d}_2}\frac{\hat{d}_2}{q}\right). \tag{6.170}$$

Solving the system of equations above yields the needed transfer functions

$$\frac{\hat{d}_1}{q} = G_{c1}F_{m1} \tag{6.171}$$

$$\frac{\hat{d}_2}{q} = -\frac{F_{m1}G_{c1}H_1R_{sense}F_{m2}G_{c2}\frac{\hat{i}_{o1}}{\hat{d}_2}}{1 + F_{m1}G_{c1}H_1R_{sense}\frac{\hat{i}_{o1}}{\hat{d}_1}}. \tag{6.172}$$

Combining the transfer functions in (6.164)-(6.165) and (6.171)-(6.172)with the converter transfer functions (6.37)-(6.38) and (6.41)-(6.42) and substituting into the

expressions in (6.157)-(6.158) will yield the loop transfer functions required to evaluate the stability of the master-slave voltage-current regulated system.

Chapter 7

The Effect of Multiple Input Filters in Multi-converter, Multi-source Power Systems

In the analyses so far, we have assumed an ideal input source - one that has zero-valued output impedance. Typical requirements for practical designs specify a maximum amount of input current ripple. An input filter is often needed to meet these requirements. However, the addition of an input filter modifies the effective source impedance presented to the converter. The designer must know how to select input filter components so that the ideal input source assumption that was implicit in the converter design is not significantly undermined.

This chapter complements the multi-converter analysis in Chapter 6 with a methodology for choosing the components of multiple input filters in a multi-converter system. The design guidelines and the methods for quantifying the impact of the added input filters are developed from an application of the two extra element theorem (2EET). The methodology could be extended to a system having N converters and N input filters using the N extra element theorem (NEET). Before addressing the addition of multiple input filters in a multi-converter system, we first review the analogous problem for single converter systems.

7.1 Single Converter Systems Review: The Extra Element Theorem for Input Filter Evaluation

The treatment of an input filter as a "post-facto" element in a power converter design is a likely outcome of natural design processes. Incidentally, this treatment is also analytically advantageous because the converter can be designed without the input filter and then the extra element theorem (EET) applied to determine the resulting modification of the converter dynamics. The extra element theorem, best summarized by Middlebrook in [151], allows the designer to replace one cumbersome and uninsightful calculation, with a few simple and elegant calculations.

7.1.1 Review of the EET

The extra element theorem follows from an application of the principle of "null double injection" to a linear circuit [151]. Upon addition of an extra element to the circuit, the transfer function of interest can be modified by using the calculated impedance seen at the "extra element port" under *two* special cases:

1. The "null-condition" impedance, $Z_{n-c}(s)$, is calculated for the case corresponding to null-double injection. It is the impedance seen at the extra element port when the transfer function input signal is directed in such a way that the transfer function output signal is nulled (equal to zero).

2. The "open-loop" impedance, $Z_{o-l}(s)$, is calculated for the case corresponding to the open-loop behavior. It is the impedance seen at the extra element port when the transfer function input signal is deactivated (set to zero).

Based on these definitions of the special-case impedances, it should be clear that any pair of special-case impedances corresponds to a particular transfer function. That particular transfer function is specified by its input and output signals.

Fundamentally, the extra element theorem uses the unique information obtained about the circuit by calculating those two special-case impedances to derive the circuit's interaction with the extra element itself. The primary result of the ensuing

mathematical manipulations is a statement of the correction factor that multiplies the original transfer function. For a series extra element (one that replaces a short-circuit in the original circuit), the correction factor is

$$\boxed{CF = \left(\frac{1 + \frac{Z_o(s)}{Z_{n-c}(s)}}{1 + \frac{Z_o(s)}{Z_{o-l}(s)}} \right)}, \tag{7.1}$$

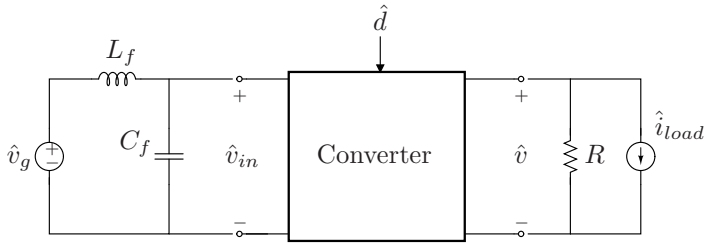
in which $Z_{n-c}(s)$ is the special-case impedance calculated for the null condition, $Z_{o-l}(s)$ is the special-case impedance calculated for the open-loop condition and $Z_o(s)$ is the impedance of the extra element itself.

7.1.2 Modified Converter Transfer Functions in Single-Converter Systems

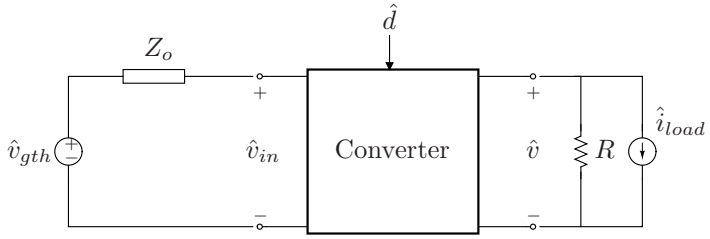
The addition of an input filter modifies the converter transfer functions from Chapter 6. This effect is due to the interaction of the input current perturbation, represented by $\jmath(s)\hat{d}(s)$ in the canonical circuit model of Figure 6-2(b), with the input filter.

Figure 7-1(a) depicts an input filter added onto a converter. The input filter may be represented to the converter by its Thevenized output impedance (and output voltage) as suggested by Figure 7-1(b). To calculate the special-case impedances, the input filter output impedance element, Z_o, is left out in favor of the "extra element port" as suggested by Figure 7-1(c).

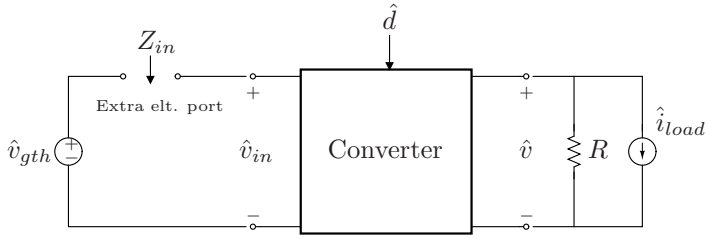
Having chosen the converter transfer function to be studied, one can proceed to derive the corresponding special-case impedances, Z_{o-l} and Z_{n-c}. Based on the definitions in Section 7.1.1, the converter transfer function input and output signals establish the constraints leading to the corresponding special-case impedances. Deriving the special-case impedances, inserting them into the correction factor from (7.1) and multiplying by the original converter transfer function yields the corrected converter transfer function. For instance, the corrected converter transfer function



(a) An input filter added onto a converter's input.



(b) The input network is replaced with its Thevenin equivalent.



(c) The filter output impedance is removed leaving the extra element port.

Figure 7-1: The EET can be applied by considering the special-case impedances at the extra element port.

from duty ratio to output voltage can be written

$$G'_{vd}(s) = CF_{vd}G_{vd}(s). \tag{7.2}$$

Some example special-case impedances are shown in Table 7.1 for three different converter types [14]. The results in Table 7.1 were calculated for correcting the duty-ratio to output voltage converter transfer function, $G_{vd}(s)$, upon addition of an input filter [14]. The converter transfer function, $G_{vd}(s)$, is usually of particular interest because it is typically "in the loop." The modification of $G_{vd}(s)$ by multiplication with the appropriate correction factor yields a change, and sometimes a degradation, in the stability of the closed-loop system. For this reason, the special-case impedances shown in Table 7.1 are historically named Z_N and Z_D because they appear in the

Table 7.1: Special-case impedances for correcting $G_{vd}(s)$ in CCM-operated converters with a fixed load, R [14].

Converter	$Z_{n-c}(s)$	$Z_{o-l}(s)$
Buck	$-\frac{R}{D^2}$	$\frac{R}{D^2}\frac{\left(1+s\frac{L}{R}+s^2LC\right)}{(1+sRC)}$
Boost	$-D'^2R\left(1-\frac{sL}{D'^2R}\right)$	$D'^2R\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{(1+sRC)}$
Buck-Boost	$-\frac{D'^2R}{D^2}\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{D'^2R}{D^2}\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{(1+sRC)}$

numerator and denominator, respectively, of the correction factor for this (typically) critical transfer function.

7.1.3 Modified Feedback Control in Single-Converter Systems

From Chapter 7, the converter transfer functions play an important role in the closed-loop transfer functions for a feedback regulated system. Carrying the correction factors for the converter transfer functions through to the results for the open-loop and closed loop transfer functions yields the corrected feedback control behavior.

For example, in equation (6.11), the converter transfer function $G_{vd}(s)$ appears in the expression for $T(s)$. The corrected open-loop transfer function becomes

$$T'(s) = G_c(s)F_mG'_{vd}(s)H(s) \tag{7.3}$$

$$= G_c(s)F_mCF_{vd}G_{vd}(s)H(s) \tag{7.4}$$

$$= CF_{vd}T(s). \tag{7.5}$$

The closed-loop transfer function from reference voltage to output voltage is written as a function of the loop transfer function. Therefore the corrected closed-loop transfer

function can be written

$$\left.\frac{\hat{v}(s)}{\hat{v}_{ref}(s)}\right|'_{\substack{\hat{v}_g=0\\ \hat{i}_{load}=0}} = \frac{1}{H(s)}\frac{T'(s)}{1+T'(s)} \tag{7.6}$$

$$= \frac{1}{H(s)}\frac{CF_{vd}T(s)}{1+CF_{vd}T(s)}. \tag{7.7}$$

7.1.4 Practical Interpretations and Impedance Inequalities

The expression for the correction factor in (7.1) reveals guidelines for choosing input filter elements. If the following "impedance inequalities" are met, the corrected transfer function reduces to the original transfer function and the corresponding converter dynamics are not significantly altered:

$$|Z_o| << |Z_{n-c}| \tag{7.8}$$

$$|Z_o| << |Z_{o-l}|. \tag{7.9}$$

Those impedance inequalities qualitatively set upper bounds on the magnitude of the input filter's output impedance. The impedance inequalities constitute useful design criteria because we can plot the three impedances of interest across frequency (bode plots) and make sure that, at all frequencies, $|Z_o(s)|$ is much less than $|Z_{o-l}(s)|$ and $|Z_{n-c}(s)|$.

In the context of the duty ratio to output voltage transfer function, $G_{vd}(s)$, meeting the first inequality will ensure that the filter output impedance is always less than the negative incremental resistance presented by the inputs of a regulated converter. For instance, from Tables 6.2 and 7.2, $Z_{n-c}(s)$ for the Buck converter is $-V/ID^2$. The same result can be derived for a lossless ($P_{out} = P_{in}$), perfectly-regulated converter ($V_{out} = V = \text{const.}$) with a fixed load ($I_{out} = I = \text{const.}$) as follows:

$$\begin{aligned} Z_{n-c}(s) = \frac{\partial V_{in}}{\partial I_{in}} &= \frac{\partial}{\partial I_{in}}\left(\frac{P_{out}}{I_{in}}\right) \\ &= -\frac{P_{out}}{I_{in}^2} = -\frac{V}{ID^2}. \end{aligned} \tag{7.10}$$

A typical plot of the three impedances of interest in Figure 7-2 illustrates the design choices required to meet the inequalities in (7.8)-(7.9). In practice, meeting the inequality in (7.8) is often achieved for LC filter designs by using a damping leg (a series RC) shunting the input terminals to decrease the magnitude peaking in the LC filter output impedance. Meeting the second inequality (7.9) is usually achieved by setting the frequency of the 2nd-order peak in the input filter output impedance below that of the 2nd-order dip in the output filter input impedance (represented by $Z_{o-l}(s)$).

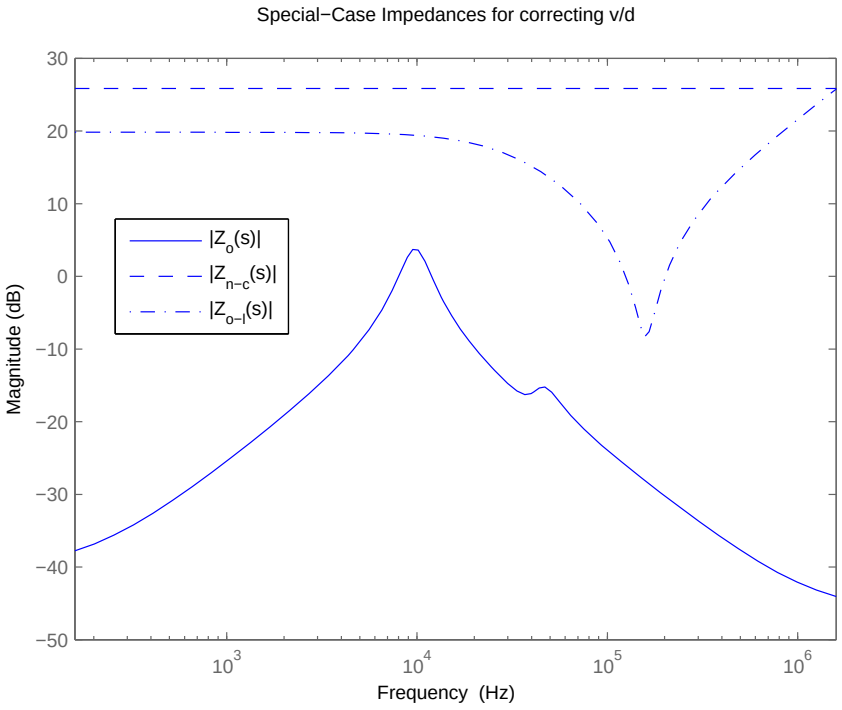
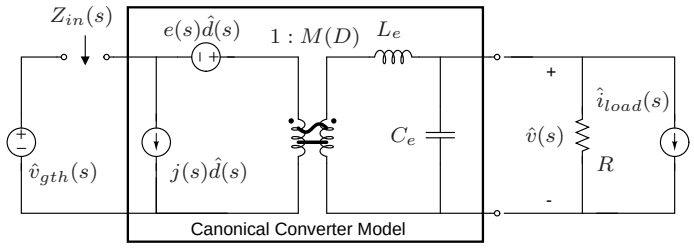


Figure 7-2: A typical frequency plot of the special case impedances, $Z_{n-c}(s)$, $Z_{o-l}(s)$, and the input filter output impedance, $Z_o(s)$, for a single converter system.

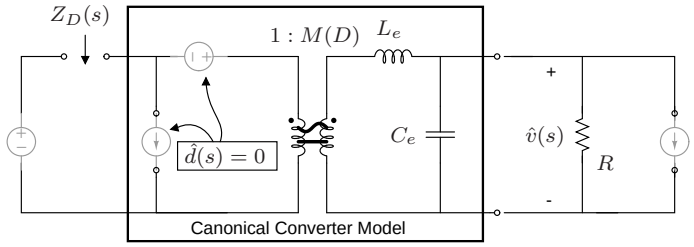
The corrected transfer functions can also be used to determine and bound the effect of adding an input filter if the impedance inequalities are not strictly met. For example, bode plots of the corrected open-loop transfer functions can reveal the degradation of the phase margin and therefore the impact of the input filter on the closed-loop system stability.

7.1.5 Example: Generalized Corrections for Single Converter Systems

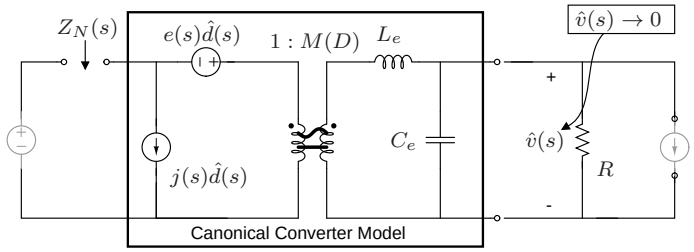
This section presents example derivations of the special-case impedances needed in the correction factor (7.1). The special-case impedances are derived from the canonical circuit model from Chapter 7. The special-case impedances derived here are generalized. Their numerical values may be found by looking up the canonical model parameters in a table like Table 6.2 for the converter topology and transfer function of interest.



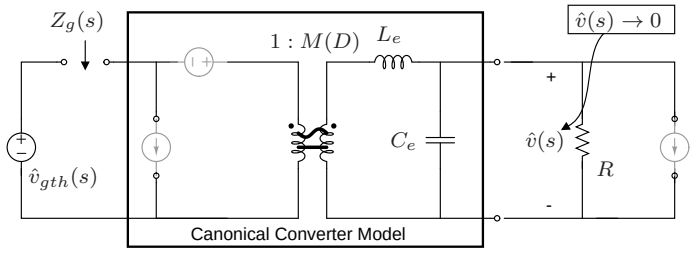
(a) A linearized converter model for calculating the special-case impedances in the extra element correction factors.



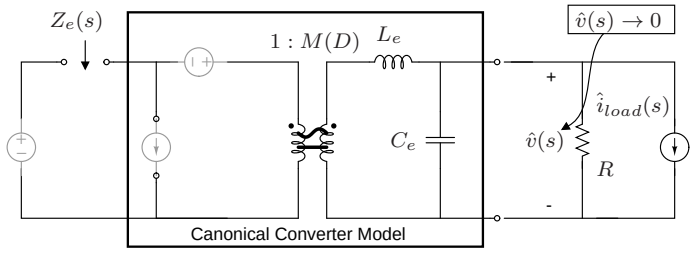
(b) $Z_D(s)$



(c) $Z_N(s)$



(d) $Z_g(s)$



(e) $Z_e(s)$

Figure 7-3: Calculating special-case impedances from the canonical circuit model

The circuit used for analysis in this section is shown in Figure 7-3(a). The independent inputs in that system include the duty ratio, $\hat{d}(s)$, as well as the (Thevinin) input voltage, $\hat{v}_{gth}(s)$. It should be understood, before proceeding, that deactivating the duty ratio signal shorts the corresponding $e\hat{d}(s)$ source and opens the corresponding $j\hat{d}(s)$ source in that converter model. In analyzing each transfer function, defined by an independent input and a corresponding output, all other independent inputs are deactivated resulting in a circuit that is a simplified version as shown in Figure 7-3. Here we consider three converter transfer functions, $G_{vd}(s)$, $G_{vg}(s)$, and $Z_e(s)$.

Open-loop Special-Case Impedance: $Z_D(s)$

For the three converter transfer functions considered here, the open-loop special-case impedance, $Z_{o-l}(s)$ is the same. In analyzing any of the three converter transfer functions, the independent inputs not corresponding to the transfer function are deactivated. Further, for the open-loop special-case impedance, the independent input corresponding to the transfer function of interest is also deactivated leaving no active independent inputs. The result for the three transfer functions is the same circuit shown in Figure 7-3(b), and thus the same input impedance, $Z_{in}(s)$. Historically, the open-loop impedance has been named $Z_D(s)$ because it is the special-case impedance that appears in the denominator of the correction factor for correcting the transfer function from duty ratio to output voltage [13]. Because the open-loop special-case impedances are all the same we name them $Z_{o-l}(s) = Z_D(s)$ for all of the transfer functions.

From the circuit in Figure 7-3(b), Z_D can be found as follows. The input impedance is simply the impedance at the secondary,

$$Z_{sec}(s) = Z_{le} + R||Z_{ce}(s) \tag{7.11}$$

reflected back through the ideal transformer:

$$\boxed{Z_D(s) = \frac{Z_{le} + R||Z_{ce}(s)}{M^2(D)}}, \tag{7.12}$$

where we have defined

$$Z_{ce}(s) \equiv \frac{1}{sC_e} \tag{7.13}$$

$$Z_{le}(s) \equiv sL_e. \tag{7.14}$$

Null-Condition Special-Case Impedance for $G_{vd}(s)$: $Z_N(s)$

The null-condition does not generally allow us to simplify the circuit topologically, or even to easily write down a closed-form expression of the control signal that leads to the nulled output signal. In fact, it would (generally) be a misinterpretation of the null-condition to simply short-circuit the output of the converter in Figure 7-3(a) and, in most cases, would lead to different and incorrect results. But, the null-condition often allows us to make observations about the circuit that simplify the calculation, not of the control signal itself, but of the impedance at the extra element port as a result of the conditions that the control signal must impose on that circuit to null the output. For example, to calculate $Z_{n-c}(s)$ for correcting $G_{vd}(s)$, the transfer function from $\hat{d}$ to $\hat{v}$, in the circuit of Figure 7-3(a), we deactivate the other independent inputs, $\hat{v}_g$ and $\hat{i}_{load}$, and null the output $\hat{v} \rightarrow 0$. The resulting circuit is shown in Figure 7-3(c).

The analysis is simplified by realizing that for a nulled output, the small-signal voltage across the load impedance is zero so no small-signal current flows through the load. Therefore, no current flows through L_e or through the secondary winding of the ideal transformer. The primary winding current is therefore also zero. Because the current through L_e is zero, the voltage across it is also zero and the zero-valued (nulled) output voltage appears at the secondary winding of the ideal transformer. Therefore, the input voltage and current are simply

$$\hat{v}_{in} = -e(s)\hat{d}(s) \tag{7.15}$$

$$\hat{i}_{in} = j(s)\hat{d}(s), \tag{7.16}$$

so that dividing the two reveals the null-condition input impedance,

$$\boxed{Z_N(s) = -\frac{e(s)}{j(s)}}. \tag{7.17}$$

Again, for historical reasons, and its importance to the key transfer function, $G_{vd}(s)$, the null-condition impedance for this case is reserved the name $Z_N(s)$ because it appears in the numerator of the correction factor (7.1).

Null-Condition Special-Case Impedance for $G_{vg}(s)$: $Z_g(s)$

Having Thevenized the input filter to account for its output impedance, the Thevenized input voltage is written

$$\hat{v}_{gth}(s) = H(s)\hat{v}_g(s), \tag{7.18}$$

where $H(s)$ is the multiplicative Thevenin factor. Deactivating the input voltage ($\hat{v}_g = 0$) will necessarily deactivate the Thevenized input voltage ($\hat{v}_{gth} = 0$), i.e.

$$\hat{v}_g = 0 \implies \hat{v}_{gth} = 0. \tag{7.19}$$

To calculate $Z_{n-c}(s)$ for correcting $G_{vg}(s)$, the transfer function from $\hat{v}_{gth}$ to $\hat{v}$, in the circuit of Figure 7-3(a), we deactivate the other independent inputs, $\hat{d}$ and $\hat{i}_{load}$, and null the output $\hat{v} \to 0$. The resulting circuit is shown in Figure 7-3(d).

Again, for a nulled output, the small-signal voltage across the load impedance is zero so no small-signal current flows through the load. Therefore, no current flows through L_e or through the secondary winding of the ideal transformer. The primary winding current is therefore also zero. Because the current through L_e is zero, the voltage across it is also zero and the zero-valued (nulled) output voltage appears at the secondary winding of the ideal transformer. Therefore, the input voltage and

current are simply

$$\hat{v}_{in} = \hat{v}_{gth}(s) \tag{7.20}$$

$$\hat{i}_{in} = 0, \tag{7.21}$$

so that dividing the two reveals the null-condition input impedance,

$$\boxed{Z_g(s) = \infty}. \tag{7.22}$$

It is important to include the nonzero multiplicative factor of $H(s)$ in the corrected transfer function, $G'_{vg}(s)$. For instance, the original transfer function from input voltage to output voltage is $G_{vg}(s)$. Upon addition of the input filter, the corrected transfer function becomes,

$$G'_{vg}(s) = CF_{vg}G_{vg}(s)H(s). \tag{7.23}$$

Null-Condition Special-Case Impedance for $Z_e(s)$: $Z_e(s)$

To calculate $Z_{n-c}(s)$ for correcting $Z_e(s)$, the transfer function from $\hat{i}_{load}$ to $\hat{v}$, (the converter open-loop output impedance) in the circuit of Figure 7-3(a), we deactivate the other independent inputs, $\hat{d}$ and $\hat{v}_{gth}$, and null the output $\hat{v} \to 0$. The resulting circuit is shown in Figure 7-3(e).

Now, with a nulled output, the small-signal voltage across the load impedance is zero so the load current source, $\hat{i}_{load}$ requires that the current through L_e and through the secondary winding of the ideal transformer is equal to $-\hat{i}_{load}$. The primary winding current is therefore equal to $-M(D)\hat{i}_{load}$. The corresponding voltage across L_e is reflected back through the ideal transformer so that the input voltage and current are

$$\hat{v}_{in} = -\frac{\hat{i}_{load}Z_{le}}{M(D)} \tag{7.24}$$

$$\hat{i}_{in} = -M(D)\hat{i}_{load}, \tag{7.25}$$

so that dividing the two reveals the null-condition input impedance,

$$\boxed{Z_e(s) = \frac{Z_{le}}{M^2(D)}}. \tag{7.26}$$

Summary

The generalized results above are summarized in Table 7.2. Those results hold for CCM-operated converters, and the special-case impedances can be found by looking up the canonical model parameters in a table such as Table 6.2, where we have defined

$$Z_{ce}(s) \equiv \frac{1}{sC_e} \tag{7.27}$$

$$Z_{le}(s) \equiv sL_e. \tag{7.28}$$

Table 7.2: Generalized Input Filter Design Constraints for Single-Converter Systems

Special-case	Impedance	Generalized Value	Transfer Function
open-loop	$Z_D(s)$	$\frac{Z_{le}+R\|\|Z_{ce}(s)}{M(D)^2}$	All
null-condition	$Z_N(s)$	$\frac{-e(s)}{j(s)}$	$G_{vd}(s)$
	$Z_e(s)$	$\frac{Z_{le}}{M(D)^2}$	$Z_e(s)$
	$Z_g(s)$	∞	$G_{vg}(s)$

It is noteworthy that substituting the generalized canonical model parameters from Table 6.2 into our generalized special-case impedances in Table 7.2, and replacing V/I with R, one arrives at the special-case impedance entries in Table 7.1 for the less general case having a load R taken from reference [14].

7.2 Multi-converter Systems: The 2EET for Multiple Input Filter Evaluation

"Although it would be unlikely that one would want to modify a transfer function to account simultaneously for two previously unrecognized extra elements, there is considerable potential advantage to be obtained from a Low-Entropy Expression for a transfer function in which the influences of two designated elements are directly exposed, in terms of their [driving point impedances]."
– R.D. Middlebrook, The Two Extra Element Theorem [152]

In this section we extend the application of the extra element theorem to account simultaneously for two added input filters in a multi-converter, multi-source power system. The extended version of the EET is the 2EET, which will be reviewed first before deriving the special-case impedances needed in the correction factors for some key multi-converter transfer functions.

7.2.1 The 2EET

In [152], Middlebrook presents the two extra element theorem (2EET), the principle result of which is the correction factor for the i^{th} transfer function:

$$CF^{(i)} = \frac{1 + \frac{Z_1}{Z_{N1}|^{(i)}_{Z_2=0}} + \frac{Z_2}{Z_{N2}|^{(i)}_{Z_1=0}} + K_N^{(i)} \frac{Z_1 Z_2}{Z_{N1}|^{(i)}_{Z_2=0} Z_{N2}|^{(i)}_{Z_1=0}}}{1 + \frac{Z_1}{Z_{D1}|^{(i)}_{Z_2=0}} + \frac{Z_2}{Z_{D2}|^{(i)}_{Z_1=0}} + K_D^{(i)} \frac{Z_1 Z_2}{Z_{D1}|^{(i)}_{Z_2=0} Z_{D2}|^{(i)}_{Z_1=0}}}, \tag{7.29}$$

where Z_1 and Z_2 are the output impedances of the first and second input filters respectively. The subscripts N and D historically represent "numerator" and "denominator" [14]. In the expression shown in (7.29), impedances with an N subscript are the null-condition impedances while those with a D subscript are the open-loop impedances. The interaction parameters can be written (they each have two possible

forms) [152]:

$$K_N^{(i)} = \frac{Z_{N1}|_{Z_2=0}^{(i)}}{Z_{N1}|_{Z_2=\infty}^{(i)}} = \frac{Z_{N2}|_{Z_1=0}^{(i)}}{Z_{N2}|_{Z_1=\infty}^{(i)}} \tag{7.30}$$

$$K_D^{(i)} = \frac{Z_{D1}|_{Z_2=0}^{(i)}}{Z_{D1}|_{Z_2=\infty}^{(i)}} = \frac{Z_{D2}|_{Z_1=0}^{(i)}}{Z_{D2}|_{Z_1=\infty}^{(i)}}, \tag{7.31}$$

For the i^{th} open-loop transfer function, there are four special-case impedances shown explicitly in the expression for the corresponding correction factor (7.29): $Z_{N1}|_{Z_2=0}^{(i)}$, $Z_{N2}|_{Z_1=0}^{(i)}$, $Z_{D1}|_{Z_2=0}^{(i)}$, and $Z_{D2}|_{Z_1=0}^{(i)}$. Additionally, two more special-case impedances are required to calculate the interaction parameters, $K_N^{(i)}$ and $K_D^{(i)}$ as shown in equations (7.31).

7.2.2 Modified Converter Transfer Functions in Multi-Converter Systems

In analogy to the EET for single converter systems, the converter transfer functions may be corrected by multiplying the converter transfer function by the corresponding correction factor. Those converter transfer functions that are "in the loop" will carry the effect of the correction factor to the loop transfer functions and may impact the stability of the closed-loop system. Some examples of the computations for those correction factors will be presented at the end of this section.

7.2.3 Modified Feedback Control in Multi-Converter Systems

Also in analogy to the EET for single converter systems, the closed-loop transfer functions may be modified upon addition of an input filter by inserting the corrected converter transfer functions into the feedback system.

7.2.4 Practical Interpretations and Impedance Inequalities

In analogy to the impedance inequalities from (7.8) and (7.9), the expression for the correction factor in (7.29) or (7.77) suggests that the i^{th} open-loop converter transfer function will not be impacted significantly if the following impedance inequalities are met. Recall that meeting these impedance qualities may be sufficient but not necessary to preserve stability of an otherwise stable regulated power system.

$$|Z_1| << |Z_{N1}|^{(i)}_{Z_2=0}| \tag{7.32}$$

$$|Z_2| << |Z_{N2}|^{(i)}_{Z_1=0}| \tag{7.33}$$

$$|Z_1| << |Z_{D1}|^{(i)}_{Z_2=0}| \tag{7.34}$$

$$|Z_2| << |Z_{D2}|^{(i)}_{Z_1=0}| \tag{7.35}$$

7.2.5 Example: Correction Factors for $\hat{v}/\hat{d}_1$, $\hat{v}/\hat{d}_2$, $\hat{i}_{o1}/\hat{d}_1$, and $\hat{i}_{o1}/\hat{d}_2$ in a Hybrid Power System

This section derives the special-case impedances needed to find the correction factors for some of the key converter transfer functions from Chapter 7. Figure 7-4 demonstrates the addition of input filters to the linearized model of a feedback regulated multi-converter, multi-source system.

The circuit used for analysis in this section is shown in Figure 7-5. The independent inputs in that system include the duty ratios for the two converters, $\hat{d}_1(s)$ and $\hat{d}_2(s)$, as well as their (Thevenin) input voltages, $\hat{v}_{gth1}(s)$ and $\hat{v}_{gth2}(s)$. It should be understood, before proceeding, that deactivating one of the duty ratio signals shorts the corresponding $e\hat{d}(s)$ source and opens the corresponding $j\hat{d}(s)$ source in that converter model. In analyzing each transfer function, defined by an independent input and a corresponding output, all other independent inputs are deactivated resulting in a circuit that is a simplified version of the one in Figure 7-5. Here we consider the converter transfer functions $\hat{v}/\hat{d}_1$, $\hat{v}/\hat{d}_2$, $\hat{i}_{o1}/\hat{d}_1$, and $\hat{i}_{o1}/\hat{d}_2$.

The following quantities are defined. The impedance Z_L is all of the impedance that shunts the output node, $Z_L \equiv R||Z_{ce1}||Z_{ce2}$ and the effective converter output

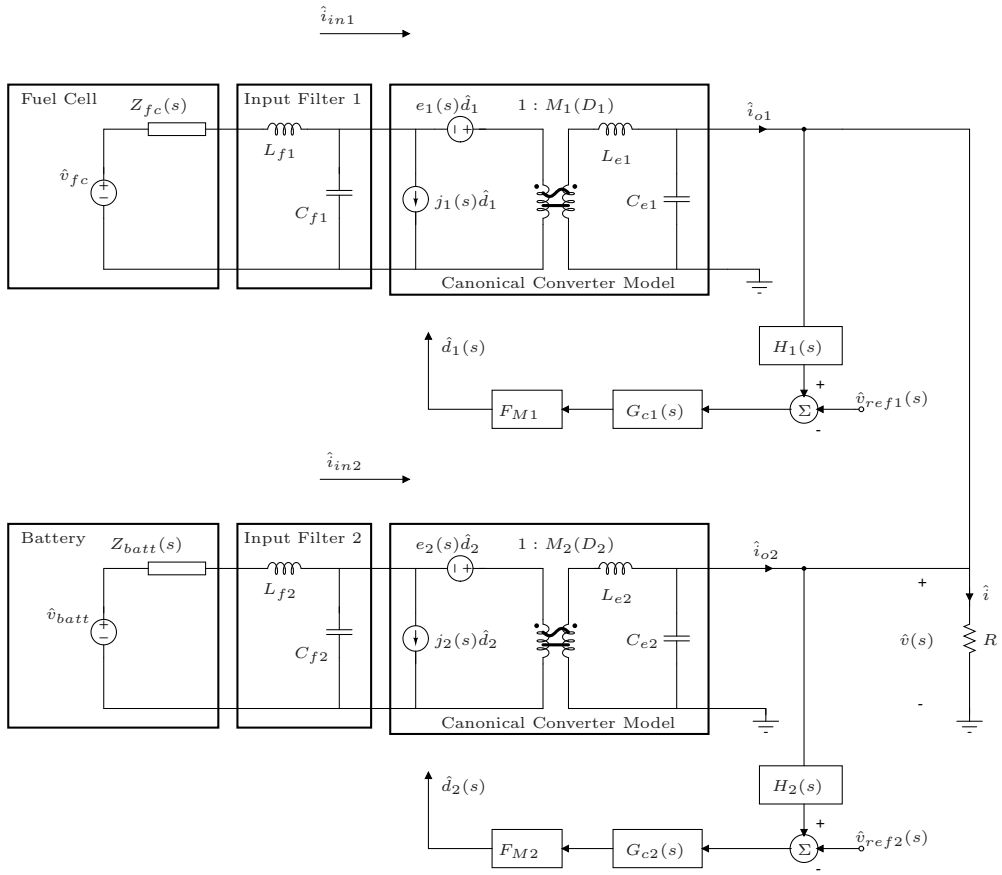


Figure 7-4: Multiple input filters added to a dual voltage-regulated power system.

impedances are $Z_{e1} \equiv Z_{le1}||Z_{ce1}$ and $Z_{e2} \equiv Z_{le2}||Z_{ce2}$, where $Z_{ce1,2} \equiv 1/sC_{e1,2}$ and $Z_{le1,2} \equiv sL_{e1,2}$.

Correction Factor for $\hat{v}/\hat{d}_1$

Designating $\hat{v}/\hat{d}_1$ as the 1^{st} transfer function, the superscripts for the six special-case impedances are all (1). The other independent inputs, $\hat{d}_2(s)$, $\hat{v}_{gth1}(s)$ and $\hat{v}_{gth2}(s)$, are all deactivated leading to some simplification of the circuit in Figure 7-5.

The first special-case impedance, $Z_{N1}|^{(1)}_{Z_2=0}$, is the null-condition impedance at the first extra element port with the second extra element port shorted. Because it is a null-condition impedance, analysis of the circuit should address the fact that the independent input in this transfer function, $\hat{d}_1$, will be directed such that the output voltage, $\hat{v}$, is nulled. With this condition, and with the other independent inputs deactivated, the second inductor voltage is zero, $\hat{v}_{le2} = 0$, so the current through that

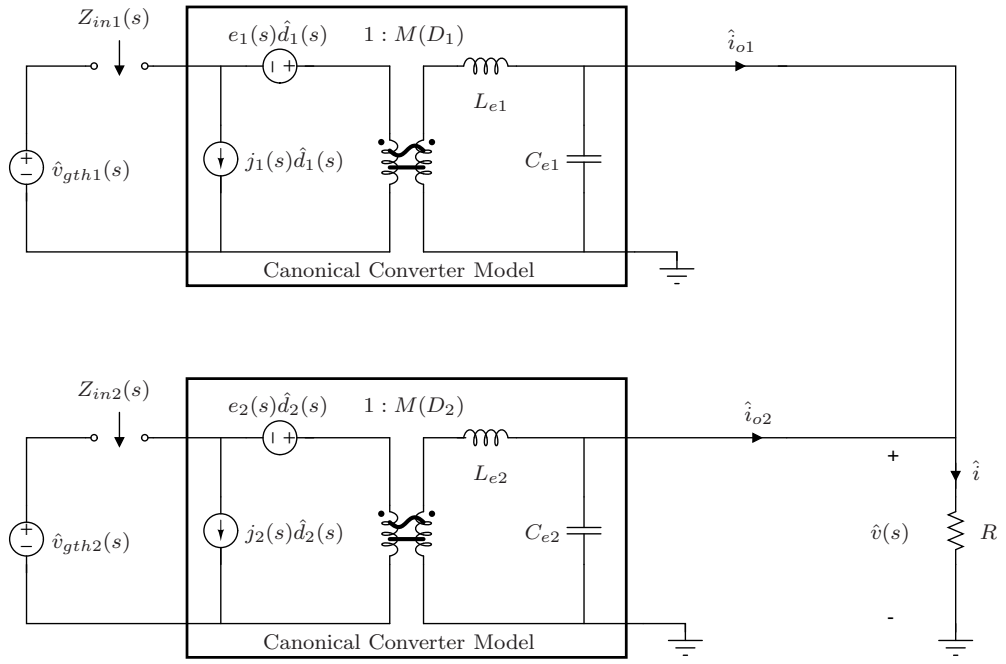


Figure 7-5: The circuit used for calculating the special-case impedances for the 2EET correction factors.

inductor is zero, $\hat{i}_{le2} = 0$. Since the output voltage is nulled, $\hat{v} = 0$, the load current is also zero, $\hat{i} = 0$, and by KCL the inductor current of the first converter must then be zero, $\hat{i}_{le1} = 0$. There is no current flowing through the first inductor so the voltage drop across it is zero, $\hat{v}_{le1} = 0$, and, by KVL, the voltage across the first secondary and therefore its primary is zero, $\hat{v}_{pri1} = 0$. Therefore, the voltage across the extra element port is simply $\hat{v}_{in} = -e_1\hat{d}_1(s)$ and the current through the extra element port must be $\hat{i}_{in} = j_1\hat{d}_1(s)$ so that their ratio - the impedance seen at the extra element port - is

$$\boxed{Z_{N1}|_{Z_2=0}^{(1)} = -\frac{e_1}{j_1}}. \tag{7.36}$$

The second special-case impedance, $Z_{N2}|_{Z_1=0}^{(1)}$, is the null-condition impedance at the second extra element port with the first extra element port shorted. Solving the

circuit in Figure 7-5 leads to the following two constraints:

$$\hat{i}_{in} = \hat{i}_{le2} M_2 \tag{7.37}$$

$$\hat{v}_{in} = \frac{\hat{v}_{le2}}{M_2} = \frac{\hat{i}_{le2} Z_{le2}}{M_2}. \tag{7.38}$$

Dividing these two constraints leads directly to a statement of the impedance seen at the second extra element port:

$$\boxed{Z_{N2}|_{Z_1=0}^{(1)} = \frac{Z_{le2}}{M_2^2}}. \tag{7.39}$$

The third special-case impedance, $Z_{D1}|_{Z_2=0}^{(1)}$, is the open-loop impedance at the first extra element port with the second extra element port shorted. Now the independent input in the transfer function of interest is deactivated leaving all of the independent inputs deactivated. Solving the circuit in Figure 7-5 among these conditions leads to four constraints:

$$\hat{i}_{in} = M_1 \hat{i}_{le1} \tag{7.40}$$

$$\hat{i}_{le1} = \frac{\hat{v}}{Z_L} \frac{Z_{le2} + Z_L}{Z_{le2}} \tag{7.41}$$

$$\hat{v}_{in} = \frac{\hat{v_{sec}}}{M_1} \tag{7.42}$$

$$\hat{v}_{sec} = \frac{\hat{v}\,(Z_L || Z_{le2} + Z_{le1})}{Z_L || Z_{le2}}. \tag{7.43}$$

Combining the first two constraints and combining the last two constraints leads to

$$\hat{i}_{in} = M_1 \frac{\hat{v}}{R} \frac{Z_{le2} + Z_L}{Z_{le2}} \tag{7.44}$$

$$\hat{v}_{in} = \frac{1}{M_1} \hat{v} \frac{Z_L || Z_{le2} + Z_{le1}}{Z_L || Z_{le2}}. \tag{7.45}$$

Dividing the two leads to the special-case impedance

$$\boxed{Z_{D1}|_{Z_2=0}^{(1)} = \frac{Z_{le1} + Z_L || Z_{le2}}{M_1^2}}. \tag{7.46}$$

The fourth special-case impedance can be taken from the third from symmetry arguments:

$$\boxed{Z_{D2}|_{Z_1=0}^{(1)} = \frac{Z_{le2} + Z_L||Z_{le1}}{M_2^2}}. \tag{7.47}$$

The remaining two special-case impedances are needed to determine the interaction parameters in the correction factor. Note that from (7.31), there is some redundancy in the choice of these final special-case impedances. Here we derive, $Z_{N1}|_{Z_2=\infty}^{(1)}$ and $Z_{D1}|_{Z_2=\infty}^{(1)}$. The fifth special-case impedance, $Z_{N1}|_{Z_2=\infty}^{(1)}$, is the null-condition impedance at the first extra element port with the second extra element port open-circuited. Because the second port is open-circuited, the current through the second primary must be zero, $\hat{i}_{pri2} = 0$, and so must the current through the second inductor, $\hat{i}_{le2} = 0$. Since the output voltage is nulled, $\hat{v} = 0$, the load current is also zero, $\hat{i} = 0$, and by KCL the inductor current of the first converter must then be zero, $\hat{i}_{le1} = 0$. Then, there is no current flowing through the first inductor so its voltage drop is zero, $\hat{v}_{le1} = 0$ so that by KVL, the voltage across the first secondary and therefore its primary is zero, $\hat{v}_{pri1} = 0$. Therefore, the voltage across the extra element port is simply $\hat{v}_{in} = -e_1\hat{d}_1(s)$ and the current through the extra element port must be $\hat{i}_{in} = j_1\hat{d}_1(s)$ so that their ratio - the impedance seen at the extra element port - is

$$\boxed{Z_{N1}|_{Z_2=\infty}^{(1)} = -\frac{e_1}{j_1}}. \tag{7.48}$$

This result is identical to the result for the first special-case impedance. This fact leads to a numerator interaction parameter of unity and an interesting simplification of the resulting correction factor.

The sixth and final special-case impedance, $Z_{D1}|_{Z_2=\infty}^{(1)}$, is the open-loop impedance at the first extra element port with the second extra element port open-circuited. Because the second port is open-circuited, the current through the second primary must be zero, $\hat{i}_{pri2} = 0$, and so must the current through the second inductor, $\hat{i}_{le2} = 0$. Then, the current through the first inductor becomes

$$\hat{i}_{le1} = \frac{\hat{v}_{sec1}}{Z_L + Z_{le1}}. \tag{7.49}$$

The input voltage and current are

$$\hat{v}_{in} = \frac{\hat{v}_{sec1}}{M_1} \tag{7.50}$$

$$\hat{i}_{in} = M_1 \hat{i}_{le1} = M_1 \frac{\hat{v}_{sec1}}{Z_L + Z_{le1}}. \tag{7.51}$$

Dividing the two leads to the special-case impedance

$$\boxed{Z_{D1}|^{(1)}_{Z_2=\infty} = \frac{Z_L + Z_{le1}}{M_1^2}}. \tag{7.52}$$

The special case impedances for calculating the correction factor of the open-loop transfer function $\hat{v}/\hat{d}_1$ derived above are summarized here:

$$Z_{N1}|^{(1)}_{Z_2=0} = \frac{-e_1(s)}{j_1(s)} \tag{7.53}$$

$$Z_{N2}|^{(1)}_{Z_1=0} = \frac{Z_{le2}}{M_2^2(D_2)} \tag{7.54}$$

$$Z_{D1}|^{(1)}_{Z_2=0} = \frac{Z_{le1} + Z_L||Z_{le2}}{M_1^2(D_1)} \tag{7.55}$$

$$Z_{D2}|^{(1)}_{Z_1=0} = \frac{Z_{le2} + Z_L||Z_{le1}}{M_2^2(D_2)}, \tag{7.56}$$

The additional special-case impedances required to calculate the interaction parameters, $K_N^{(1)}$ and $K_D^{(1)}$, are

$$Z_{N1}|^{(1)}_{Z_2=\infty} = \frac{-e_1(s)}{j_1(s)} \tag{7.57}$$

$$Z_{D1}|^{(1)}_{Z_2=\infty} = \frac{Z_L + Z_{le1}}{M_1^2(D_1)}. \tag{7.58}$$

Correction Factor for $\hat{v}/\hat{d}_2$

Designating $\hat{v}/\hat{d}_2$ as the 2^{nd} transfer function, the superscripts for the six special-case impedances are all (2). The other independent inputs, $\hat{d}_1(s)$, $\hat{v}_{gth1}(s)$ and $\hat{v}_{gth2}(s)$, are all deactivated leading to some simplification of the circuit in Figure 7-5.

The special case impedance for calculating the correction factor of the second

open-loop transfer function of interest, $\hat{v}/\hat{d}_2$, can be similarly derived or inferred from the correction factor for the first by symmetry arguments. This leads to:

$$Z_{N1}|_{Z_2=0}^{(2)} = \frac{Z_{le1}}{M_1^2(D_1)} \tag{7.59}$$

$$Z_{N2}|_{Z_1=0}^{(2)} = \frac{-e_2(s)}{j_2(s)} \tag{7.60}$$

$$Z_{D1}|_{Z_2=0}^{(2)} = \frac{Z_{le1} + Z_L||Z_{le2}}{M_1^2(D_1)} \tag{7.61}$$

$$Z_{D2}|_{Z_1=0}^{(2)} = \frac{Z_{le2} + Z_L||Z_{le1}}{M_2^2(D_2)} \tag{7.62}$$

and the additional special-case impedances required to calculate the interaction parameters, $K_N^{(2)}$ and $K_D^{(2)}$, are

$$Z_{N2}|_{Z_1=\infty}^{(2)} = \frac{-e_2(s)}{j_2(s)} \tag{7.63}$$

$$Z_{D2}|_{Z_1=\infty}^{(2)} = \frac{Z_L + Z_{le2}}{M_2^2(D_2)}. \tag{7.64}$$

Correction Factor for $\hat{i}_{o1}/\hat{d}_1$

Similar calculations lead to the special-case impedances for correcting the converter transfer functions from the duty ratios to the first converter's output current. The derivations can be found in Appendix B.3. The special case impedances for calculating the correction factor of the open-loop transfer function $\hat{i}_{o1}/\hat{d}_1$ derived above are summarized here:

$$Z_{N1}|_{Z_2=0}^{(3)} = \frac{-e_1(s)}{j_1(s)} \tag{7.65}$$

$$Z_{N2}|_{Z_1=0}^{(3)} = \frac{R\left(\frac{Z_{ce2}+Z_{le2}}{Z_{ce2}}\right) + Z_{le2}}{M_2^2(D_2)} \tag{7.66}$$

$$Z_{D1}|_{Z_2=0}^{(3)} = \frac{Z_{le1} + Z_L||Z_{le2}}{M_1^2(D_1)} \tag{7.67}$$

$$Z_{D2}|_{Z_1=0}^{(3)} = \frac{Z_{le2} + Z_L||Z_{le1}}{M_2^2(D_2)}, \tag{7.68}$$

where Z_L is the total impedance shunting the converter outputs, i.e. $Z_L = R||1/(s(C_1+C_2))$, in Figure 7-4. The additional special-case impedances required to calculate the interaction parameters, $K_N^{(1)}$ and $K_D^{(1)}$, are

$$Z_{N1}|_{Z_2=\infty}^{(3)} = \frac{-e_1(s)}{j_1(s)} \tag{7.69}$$

$$Z_{D1}|_{Z_2=\infty}^{(3)} = \frac{Z_L + Z_{le1}}{M_1^2(D_1)}. \tag{7.70}$$

Correction Factor for $\hat{i}_{o1}/\hat{d}_2$

The special case impedances for calculating the correction factor of the open-loop transfer function $\hat{i}_{o1}/\hat{d}_2$ are derived in Appendix B.4. The results are summarized here:

$$Z_{N1}|_{Z_2=0}^{(4)} = \frac{Z_{ce1} + Z_{le1}}{M_1^2(D_1)} \tag{7.71}$$

$$Z_{N2}|_{Z_1=0}^{(4)} = \frac{-e_2(s)}{j_2(s)} \tag{7.72}$$

$$Z_{D1}|_{Z_2=0}^{(4)} = \frac{Z_{le1} + Z_L||Z_{le2}}{M_1^2(D_1)} \tag{7.73}$$

$$Z_{D2}|_{Z_1=0}^{(4)} = \frac{Z_{le2} + Z_L||Z_{le1}}{M_2^2(D_2)}, \tag{7.74}$$

where Z_L is the total impedance shunting the converter outputs, i.e. $Z_L = R||1/(s(C_1+C_2))$, in Figure 7-4. The additional special-case impedances required to calculate the interaction parameters, $K_N^{(1)}$ and $K_D^{(1)}$, are

$$Z_{N1}|_{Z_2=\infty}^{(4)} = \frac{Z_{ce1} + Z_{le1}}{M_1^2(D_1)} \tag{7.75}$$

$$Z_{D1}|_{Z_2=\infty}^{(4)} = \frac{Z_L + Z_{le1}}{M_1^2(D_1)}. \tag{7.76}$$

Discussion

Note that from the results above, the "numerator interaction parameter" equals one ($K_N^{(i)} = 1$) for each of the transfer functions. This fact, which is characteristic of the hybrid power system in Figure 7-5, simplifies the numerical computation of the

correction factors, $CF^{(i)}$, because, in that case, the numerator is exactly factorable as follows:

$$CF^{(i)} = \frac{\left(1 + \frac{Z_1}{Z_{N1}|^{(i)}_{Z_2=0}}\right)\left(1 + \frac{Z_2}{Z_{N2}|^{(i)}_{Z_1=0}}\right)}{1 + \frac{Z_1}{Z_{D1}|^{(i)}_{Z_2=0}} + \frac{Z_2}{Z_{D2}|^{(i)}_{Z_1=0}} + K_D^{(i)}\frac{Z_1 Z_2}{Z_{D1}|^{(i)}_{Z_2=0} Z_{D2}|^{(i)}_{Z_1=0}}}. \tag{7.77}$$

7.3 Numerical Computation of High Order Rational Polynomials

The transfer functions and correction factors in Chapters 6 and 7 lead to high order rational polynomials in many practical cases. The numerical computation of those rationals requires some care. It is helpful and sometimes necessary to compute intermediate numerical values in order to overcome the limits of finite precision computation. The final numerical value may be computed by forming linear combinations of the intermediate values according to the form of the correction factor. This technique is not unlike the cascade implementation for FIR filter design to limit the noisy effects of finite precision in digital signal processing. Below is an example computation of a closed loop transfer function in MATLAB®. In the style of the analysis here, the transfer function is left in terms of impedances. The needed impedances are defined as transfer functions at the beginning of the computation. This eliminates the need to write the transfer function down explicitly in terms of element values. Intermediate numerical values are computed using the `freqresp()` function and evaluating the intermediate transfer functions across the desired frequency vector. The result is always a vector of complex numbers and must be treated with vector arithmetic.

`iin1overiload.m`

This function returns magnitude and phase vectors for the closed-loop transfer function $\left.\frac{\hat{i}_{in1}}{\hat{i}_{load}}\right|_{CL}$ for the master-slave current-voltage regulated power system. This is an example transfer function computation demonstrating the approach to computing numerical values for high order rational polynomials. This example also demonstrates

how MATLAB® can be allowed to perform mathematical formulations of transfer functions in a quasi-symbolic way by using the dummy transfer function `s` to automatically convert impedances to transfer functions.

```
function [mag,phase] = iin1overiload(M1,M2,e1,e2,j1,j2,Le1,Le2,ESRle1,...
    ESRle2,Ce1,Ce2,ESRce1,ESRce2,Fm1,Fm2,Gc1,Gc2,H1,H2,R, Rsense, eval_vector);
s = tf('s');

zle1 = ESRle1+s*Le1;
zle2 = ESRle2+s*Le2;
zce1 = ESRce1+1/(s*Ce1);
zce2 = ESRce2+1/(s*Ce2);
ze1 = 1*zle1*zce1/(zle1+zce1);
ze2 = zle2*zce2/(zle2+zce2);
zc = zce1*zce2/(zce1+zce2);
zl = zc*R/(zc+R);
zlpzle1 = (zl*zle1/(zl+zle1));
zlpzle2 = (zl*zle2/(zl+zle2));

lambda1 = freqresp(zlpzle2,eval_vector)./freqresp(zle1+zlpzle2,eval_vector);
lambda2 = freqresp(zlpzle1,eval_vector)./freqresp(zle2+zlpzle1,eval_vector);

F1 = freqresp(tf(Fm1*Gc1*H1*Rsense),eval_vector);
F2 = freqresp(tf(Fm2*Gc2*H2),eval_vector);

voveriload_ol = -freqresp(ze1*ze2,eval_vector)./freqresp(ze1+ze2+ze1*ze2/R,eval_vector);
io1overiload_ol = freqresp(ze2,eval_vector)./freqresp(ze1+ze2+ze1*ze2/R,eval_vector);
io1overd2 = -lambda2.*freqresp(e2*M2/ze1,eval_vector);
io2overd1 = -lambda1.*freqresp(e1*M1/ze2,eval_vector);
io1overd1 = freqresp(e1*M1/zle1,eval_vector)-lambda1.*freqresp(e1*M1/ze1,eval_vector);
io2overd2 = freqresp(e2*M2/zle2,eval_vector)-lambda2.*freqresp(e2*M2/ze2,eval_vector);
voverd1 = lambda1.*freqresp(tf(e1*M1),eval_vector);
voverd2 = lambda2.*freqresp(tf(e2*M2),eval_vector);

d1overiload = (((F1.*F2.*voveriload_ol.*io1overd2)./(freqresp(tf(1),eval_vector)...
    +F2.*voverd2))-F1.*io1overiload_ol)./((freqresp(tf(1),eval_vector)+...
    F1.*io1overd1).*(freqresp(tf(1),eval_vector)-(F1.*F2.*voverd1.*io1overd2)...
    .*(freqresp(tf(1),eval_vector)+F1.*io1overd1)./(freqresp(tf(1),eval_vector)+F2.*voverd2)));
d2overiload = -F2.*(d1overiload.*voverd1+voveriload_ol)./(freqresp(tf(1),eval_vector)...
    +F2.*voverd2);

io1overiload_cl = (freqresp(M1/zle1,eval_vector)-lambda1./...
    freqresp(ze1,eval_vector)).*freqresp(tf(e1),eval_vector).*d1overiload -...
    lambda2.*d2overiload.*freqresp(M2*e2/ze1,eval_vector);
voveriload_cl = lambda1.*d1overiload.*freqresp(tf(e1*M1),eval_vector)+...
    lambda2.*d2overiload.*freqresp(tf(e2*M2),eval_vector);

result = freqresp(tf(j1),eval_vector).*d1overiload+...
    freqresp(tf(M1),eval_vector).*io1overiload_cl+...
    freqresp(tf(M1),eval_vector).*voveriload_cl./freqresp(zce1,eval_vector);

%% Results
mag = 20*log10(abs(result(:)));
phase = 180/pi*(unwrap(angle(result(:))));

end
```

Chapter 8

Design Example 1: Run-time Integral Diagnostics of a Grid-Tied Fuel Cell

In this example, we present the performance of a multi-converter system with integral EIS functionality for a stationary (grid-tied) application. The load power in this example is relatively fixed. A dual voltage-regulated system with an auxiliary small-signal control input provides the needed functionality. In this example, the power system was built using off-the-shelf switching sections.

For experimentation, a 5 kW Siemens fuel cell stack was available through a collaboration with Montana State University. This chapter begins with a description of the fuel cell technology and the configuration of the experimental fuel cell. Two system identification techniques used in the evaluation of the experimental data are discussed. The power electronic system is presented along with design considerations and the resulting performance. Impedance data collected from the experiments using the multi-converter power system agrees well with impedance data collected using an exogenous signal source.

In our SOFC stack, and in many similar fuel cell applications, it is neither feasible nor desirable to remove the stack from service for the purpose of connecting impedance spectroscopy instrumentation. However, in principle, it is not necessary to remove the

load provided that a sufficiently rich test signal can be introduced in addition to the load, as in [153]. This work demonstrates the use of power electronics to impose a test signal while delivering power to a load. This characterization consists of calculations of whole stack impedance spectroscopy and time-domain model parameters, using both the switching waveform, or "ripple", of the power electronics connected to the stack and an exogenous excitation. This method requires only instrumentation at the stack electrical terminals, and could be integrated with the controls of existing power electronics to provide non-invasive, low cost stack prognostics. The underlying motivation of this work, not directly addressed here, is that we may ultimately be able to improve reliability and mitigate materials challenges through controls at the electrical terminals that are richly informed of the state of the stack.

8.1 Fuel Cell Overview

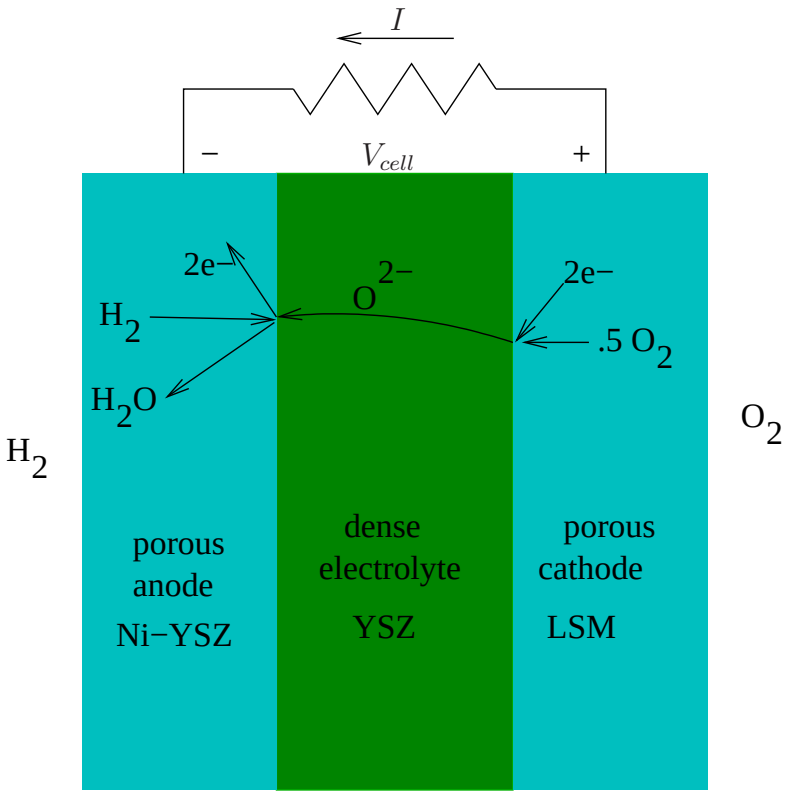


Figure 8-1: Conceptual diagram of SOFC energy conversion.

Figure 8-1 is a conceptual illustration of the energy conversion mechanism in a solid oxide fuel cell (SOFC). The cell comprises three layers. The cathode (right) is a porous, electrically conductive material. Molecular oxygen is reduced to oxygen ions in the cathode, with electrons supplied by the external circuit. These oxygen ions move readily from the cathode through a dense electrolyte, which is ion-conducting but is an electronic insulator. At appropriate temperatures, typically in the vicinity of 750°C, the electrolyte becomes conductive to oxygen by means of oxygen vacancies in the lattice structure of the material. The anode layer is another porous, electrically conductive cermet material. Oxygen ions arriving from the electrolyte serve to oxidize fuel and release their electrons to the external circuit. Typical materials for the cathode/electrolyte/anode structure include lanthanum strontium manganate (LSM), ytria stabilized zirconia (YSZ), and nickel/YSZ cermet, respectively. While the overall reaction in 8-1 shows hydrogen as a fuel and water as a product, a basic advantage of SOFC technology is that the electrolyte is an oxygen ion conductor. This allows the use of fuels containing carbon, as opposed to hydrogen-conducting fuel cell technologies.

Figure 8-2 shows a photograph of the actual stack used for testing in this work. The stack is a 5 kW nominal, Fuel Cell Technologies / Siemens Alpha-8 tubular solid oxide fuel cell using city natural gas as a fuel. The vents at the top are for intake and exhaust, and this particular unit was also configured with a recuperator that could be used to heat water for a combined heat and power application. This unit is designed for three-phase grid-tie operation. However, for purposes of this study we were able to access and connect power electronics to the terminals of the stack and monitor the response of the stack to test signals imposed by those power electronics.

8.1.1 Fuel Cell Impedance Spectroscopy

Electrochemical impedance spectroscopy models the AC electrical terminal response of a fuel cell (or other electrochemical system) in the vicinity of an operating point

Figure 8-2: A 5 kW Siemens / Fuel Cell Technology stack used for testing.

as a linear impedance $Z(j\omega)$. In particular, for cell voltage and current

$$v_c(t) = V_o + v(t) \tag{8.1}$$

$$i_c(t) = I_0 + i(t), \tag{8.2}$$

at a DC operating point V_0, I_0, the impedance captures the frequency domain relationship between the small signal quantities $v(t)$, $i(t)$. Use of this model presumes that the cell responds linearly over the range of excitation in the vicinity of the bias point, i.e. that excitation at a single frequency produces a response at that frequency.

Impedance spectroscopy results are generally presented using a Nyquist plot showing real and complex parts of the impedance with frequency as an implicit argument. An electrochemist can recognize the shapes characteristic of processes in the Nyquist diagram [147]. Practitioners often extend this non-parametric analysis by fitting lumped-parameter circuit models, in the frequency domain, and in some cases asso-

ciate physical processes with individual circuit elements. In [148], a parameterized impedance spectroscopy model is used to synthesize an equivalent circuit of an SOFC. Other examples include the analysis of a PEM cell in [149] and the application to an SOFC cell in [148]. Frequencies of 0.01Hz to 1MHz are generally used for studying SOFC systems [142]. For a survey of impedance spectroscopy in fuel cells, see [150].

Under sufficiently rich excitation, an estimate $\hat{Z}(j\omega)$ of the impedance response can be extracted from the terminal voltage and current of a cell. In particular, an impedance estimate is

$$\hat{Z}(j\omega) = \frac{\hat{V}_c(j\omega)}{\hat{I}_c(j\omega)}, \quad |\omega| > 0, \tag{8.3}$$

where $\hat{V}_c(j\omega)$ and $\hat{I}_c(j\omega)$ are estimates of the spectral content of the electrical terminal responses $v_c(t)$ and $i_c(t)$. The process of estimating spectral content of signals using sampled data and discrete-time Fourier transform techniques, including windowing and other considerations, is reviewed in [154] among others. The excitation $i_c(t)$ imposed at the electrical terminals must be broadly exciting, in the sense of having significant power at frequencies where it is desired to have a good estimate of $Z(j\omega)$. If $\hat{I}_c(j\omega)$ at some frequency is small or dominated by noise, the variance in $\hat{Z}(j\omega)$ can be large. In practice, we avoid this by not evaluating $Z(j\omega)$ for frequencies where the signal content in the $I_c(j\omega)$ is small in comparison to a threshold.

8.1.2 Parametric Modeling and Identification

In addition to impedance spectroscopy, it is sometimes useful to model fuel cell responses using a parameterized model, often in the form of a differential equation that represents specific physical processes. For example, Hall [155] develops a transient model of a tubular SOFC including electrochemical, thermal, and mass flow elements. Wang et al. [156] develop a dynamic model for a proton exchange membrane fuel cell using electrical circuit elements, and Pasricha et al. [157] provide a dynamic electrical terminal model of a proton exchange membrane fuel cell. A challenge in developing parametric, physically-baed models of fuel cells is to restrict the phenomena in the model to those which are well supported by the observations.

With preliminary, non-parametric observations in mind, we propose a very simple three-parameter model of the stack, i.e.

$$v(t) = V_{oc} - Ri(t) - Ls\, i(t), \tag{8.4}$$

where $v(t)$ is the stack voltage, $i(t)$ is the stack current, V_{oc} is the open circuit stack voltage, R is a resistance, L is a inductance, and s is the $\frac{d}{dt}$ operator.

The parameters of (8.4) are conveniently estimated using the operator substitution technique in [154]. The low-pass filter operator

$$\lambda = \frac{1}{1 + s\tau}. \tag{8.5}$$

can be manipulated to isolate s, i.e.

$$s = \frac{1 - \lambda}{\lambda\tau}. \tag{8.6}$$

Substituting s into (8.4) and rearranging so λ appears in the numerator provides

$$\lambda\tau V_{oc} - \tau\lambda i(t)R + (\lambda - 1)i(t)L = \tau\lambda v(t). \tag{8.7}$$

This is appealing because $\lambda\tau$, $\lambda i(t)$, and $\lambda v(t)$ can be evaluated using a discrete-time implementation of λ applied to the data. These quantities can be arranged in a least-squares tableau to obtain estimates for the parameters V_{oc}, R, and L. Setting $\lambda\tau V_{oc}$ to the final value, we form the following equations

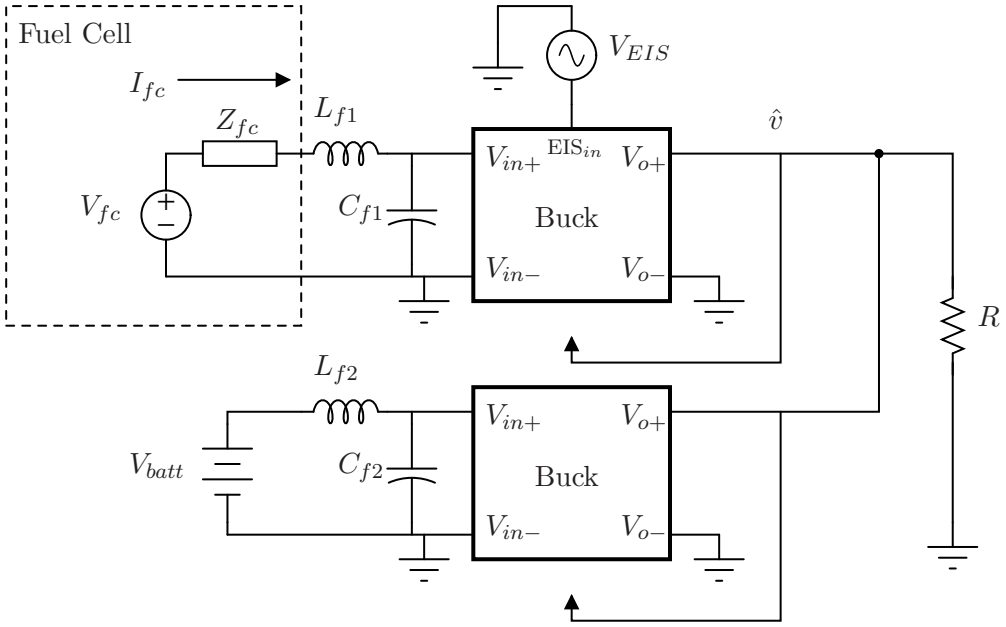
$$\begin{pmatrix} \tau & -\tau\lambda i[1] & (\lambda - 1)i[1] \\ \tau & -\tau\lambda i[2] & (\lambda - 1)i[2] \\ \vdots & \vdots & \vdots \\ \tau & -\tau\lambda i[n] & (\lambda - 1)i[n] \end{pmatrix} \begin{pmatrix} V_{oc} \\ R \\ L \end{pmatrix} = \begin{pmatrix} \tau\lambda v[1] \\ \tau\lambda v[2] \\ \vdots \\ \tau\lambda v[n] \end{pmatrix} \tag{8.8}$$

to estimate the parameters of (8.4).

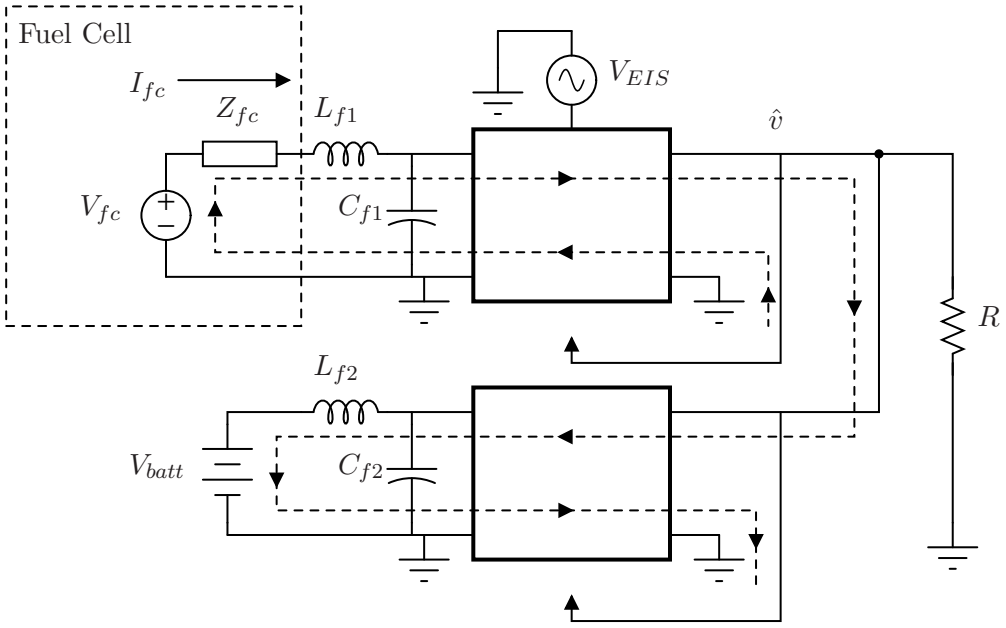
8.2 Dual Voltage Regulated Power System Architecture

A simplified connection diagram for the EIS-capable multi-converter power system is shown in Figure 8-3(a). The multi-converter power system was built from off-the-shelf buck converters, SynQor ® part number PQ48120HTA14NKF. The current share pins on the two converters were connected so that they shared load current at startup. The trim pins on the two converters were adjusted after startup so that the current share control was defeated leaving two voltage regulated converters [1]. The EIS control signal was superposed on the voltage reference for the fuel cell converter.

[1] This was confirmed by SynQor Applications Engineering.



(a) A simplified connection diagram of the hybrid system built from off-the-shelf components.



(b) Desired small-signal current paths for EIS excitation signals.

Figure 8-3: A hybrid power system with EIS functionality built from off-the-shelf components.

Conceptually, the hybrid system enables run-time fuel cell diagnostics by providing a means for exciting the fuel cell with a small-signal current originating at the secondary source (the battery in this case), while the load current itself is largely unaffected by the EIS measurement. The small-signal current paths corresponding to this behavior are depicted in Figure 8-3(b).

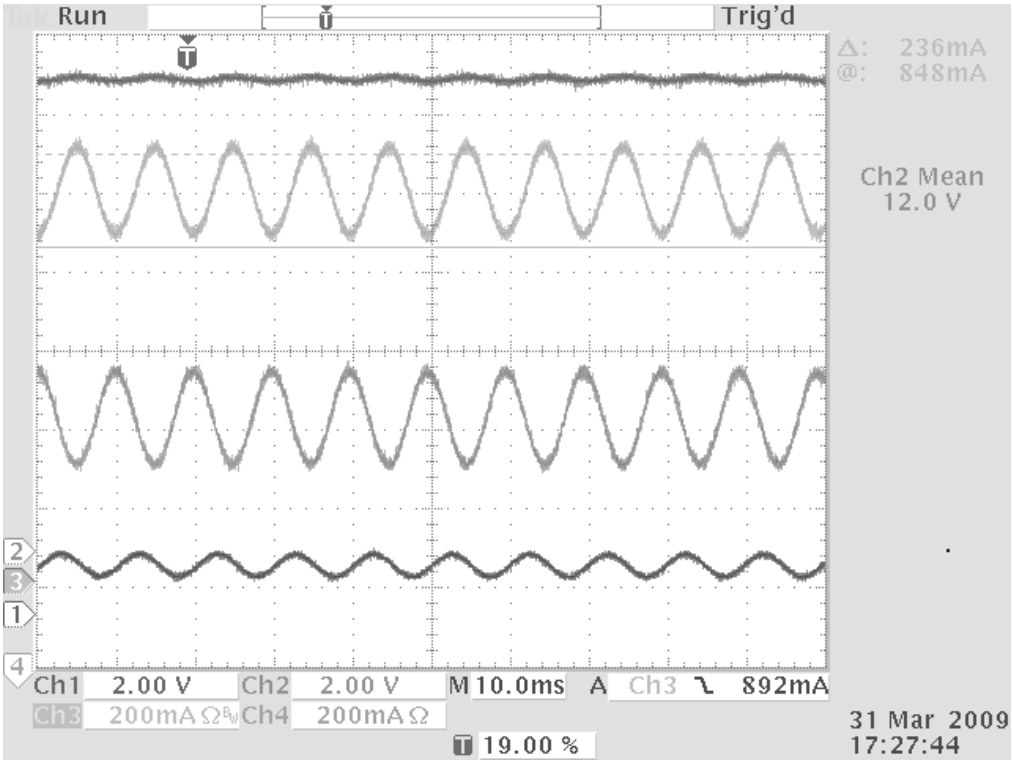
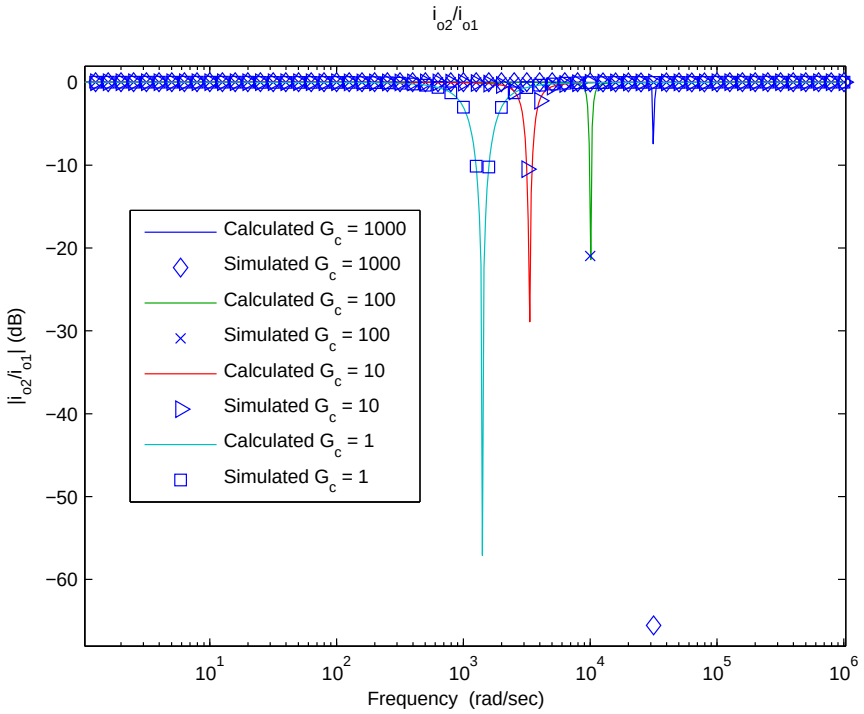


Figure 8-4: An oscilloscope screen shot showing the battery and fuel cell currents during run-time EIS (≈100 Hz). Top to bottom: load voltage (ch2), fuel cell current (ch3),battery current (ch4), control signal (ch1).

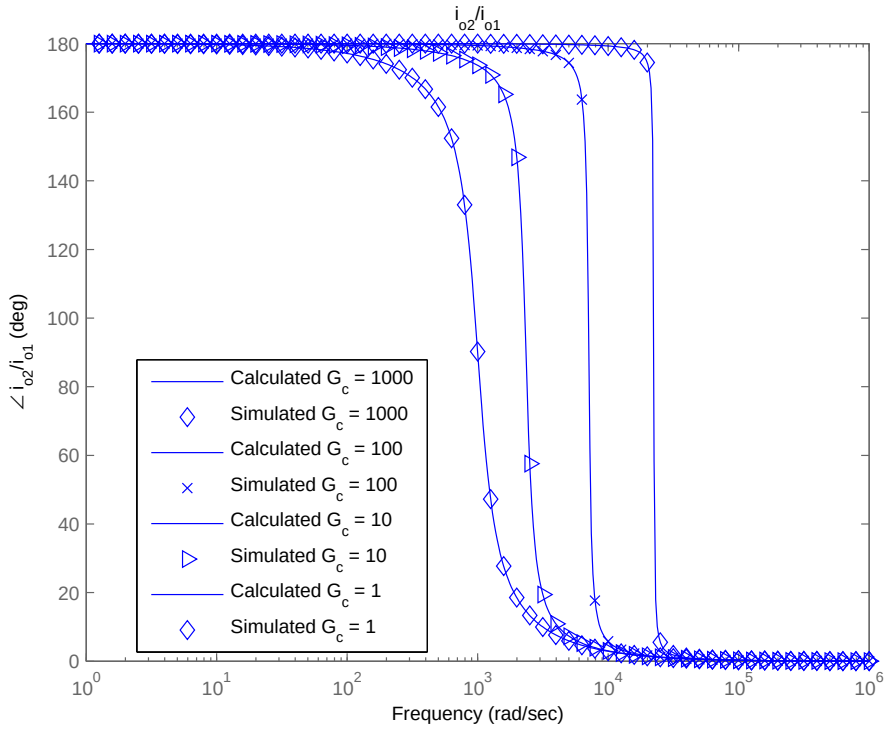
Figures 8-5, 8-6, and 8-7 show calculated and simulated closed-loop transfer functions for the multi-converter power system. The magnitude and phase plots of $\hat{i}_{o2}/\hat{i}_{o1}$ in Figure 8-5, confirm our intuition that, at low frequency, the currents out of the two converters are equal and opposite (small-signal currents flow out of one and into the other). This behavior corresponds to the time-domain data shown in the scope shot of Figure 8-4, taken from the experimental system of Figure 8-3.

Figures 8-6 and 8-7 show that the transconductance from the control voltage, $\hat{v}_{ref1}$, to input current, $\hat{i}_{in1}$, is large and the corresponding load voltage perturbation,

$\hat{v}$, is small. This amounts to the desired characteristic of an EIS-capable hybrid power system that the load voltage will be largely unaffected by the run-time EIS behavior.



(a) Magnitude



(b) Phase

Figure 8-5: i_{o2}/i_{o1}.

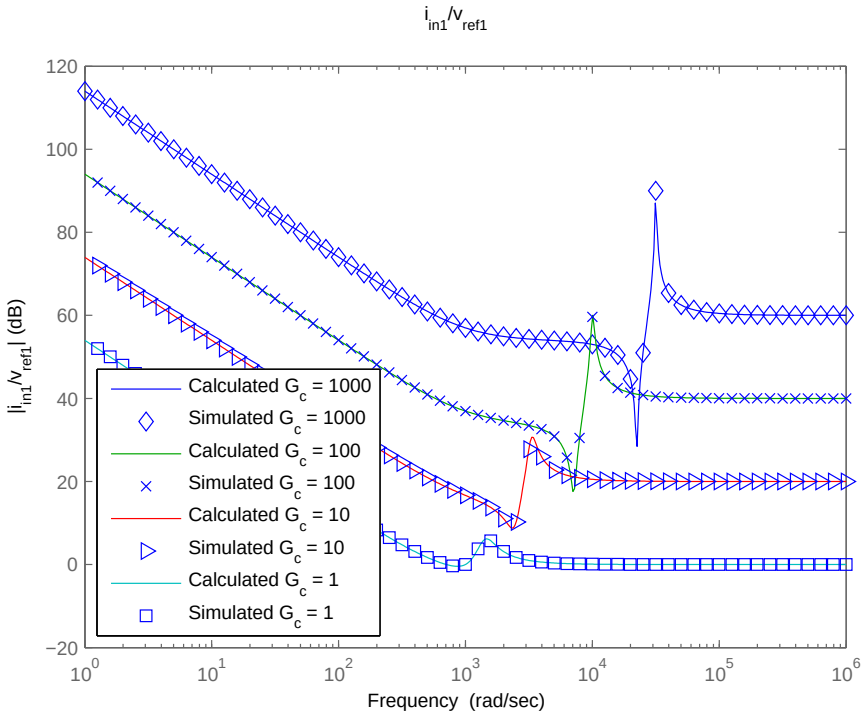


Figure 8-6: $|i_{in1}/v_{ref1}|$.

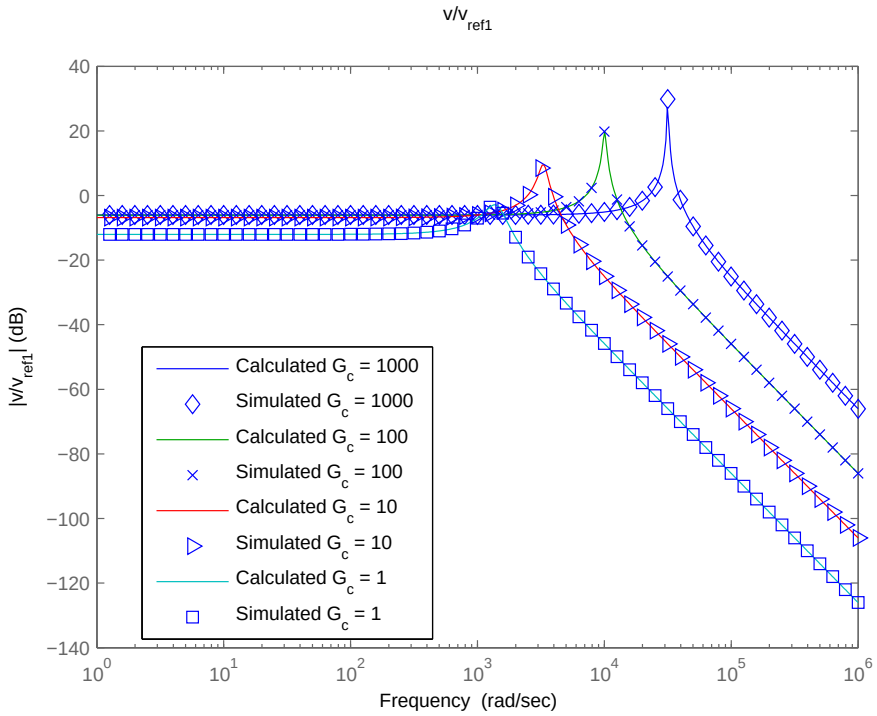


Figure 8-7: $|v/i_{ref1}|$.

8.3 Input Filter

The input filters in an EIS-capable hybrid power system may be designed to achieve several goals simultaneously:

1. Attenuate converter switching ripple
2. Avoid converter instability
3. Pass or even amplify excitation signals

Goals 1) and 2) are typical. Goal 3) is unique to the EIS-capable multi-converter system because the filter must be designed to allow excitation currents to flow from the converter input to the terminals of the fuel cell up to a specified frequency.

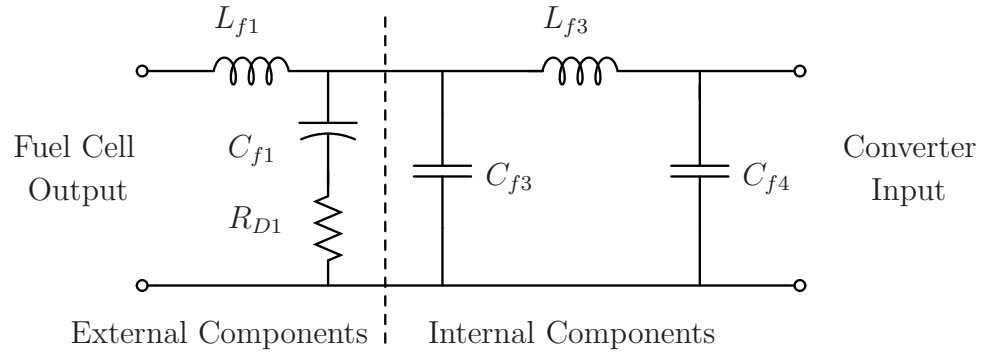


Figure 8-8: The input filter for the fuel cell converter.

For this example, we consider the input filter shown in Figure 8-8, which includes both the internal input filter components provided on the off-the-shelf Buck converter from Figure 8-3(a) as well as the external input filter components that we added, L_{f1}, C_{f1} and R_{D1}. The internal input filter components are:

$$C_{f3} = 8.8\ \mu\text{F} \tag{8.9}$$

$$L_{f3} = 2.2\ \mu\text{H} \tag{8.10}$$

$$C_{f4} = 26.4\ \mu\text{F}. \tag{8.11}$$

Having set the pass band and rollover frequencies, largely by choosing L_{f1}, the filter

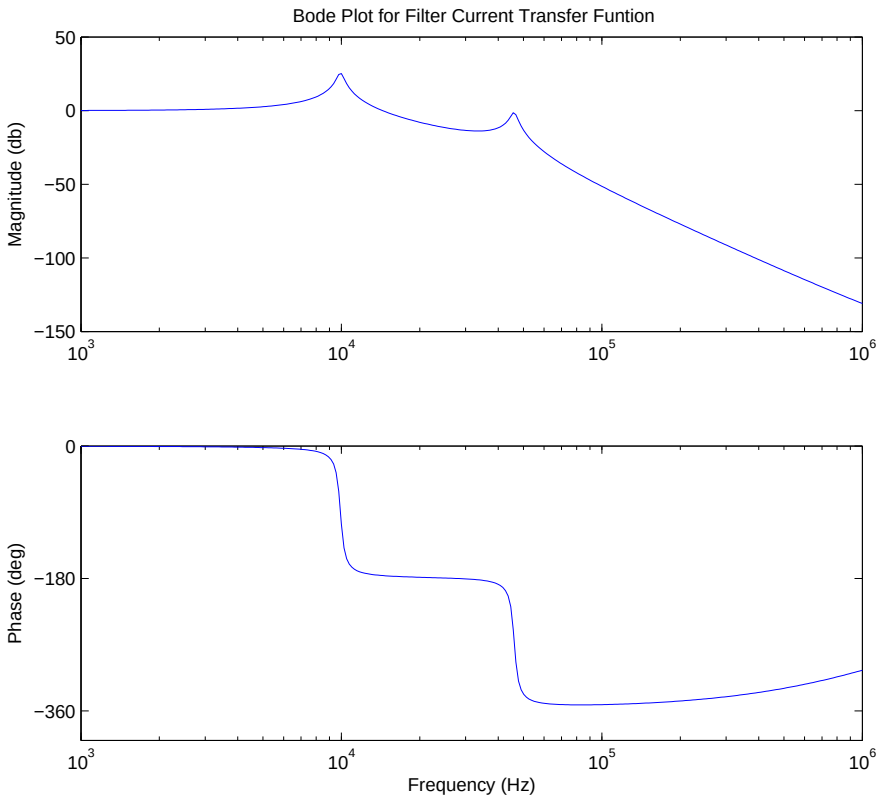


Figure 8-9: The current transfer function for the fuel-cell leg input filter

transfer function is shown in Figure 8-9. The damping leg formed by C_{f1} and R_{D1} in Figure 8-8 is intended to limit the magnitude peaking in the output impedance of the filter. However, as the impedance of the damping leg decreases it provides a shunt path that diminishes the transmission of excitation currents to the fuel cell terminals. Moreover, due to natural bandlimiting in the system, the designer may actually want to exploit the resonance at the edge of the pass band in Figure 8-9 to achieve some current amplification at that frequency. Both of these considerations qualitatively lower-bound the damping resistor, R_{D1}, a constraint which directly contends with the impedance inequalities in (7.32)-(7.35).

Figure 8-10 shows a magnitude plot of the special-case impedances for correcting $\hat{v}/\hat{d}_1$ as well as the output impedances from the filters used in our system. Note that the two resonances in Z_o (solid line) correspond to the two resonances in the filter transfer function of Figure 8-9. Because the impedance inequalities in (7.32)-(7.35)

are not strictly met, as is evidenced by the plot in Figure 8-10, we need to examine the quantitative impact of the input filters on the converter open-loop transfer functions. A plot of the correction factors, $CF^{(i)}$, for the i^{th} converter open-loop transfer function from (7.29) is the most direct way of analyzing the effect of the input filters on system stability.

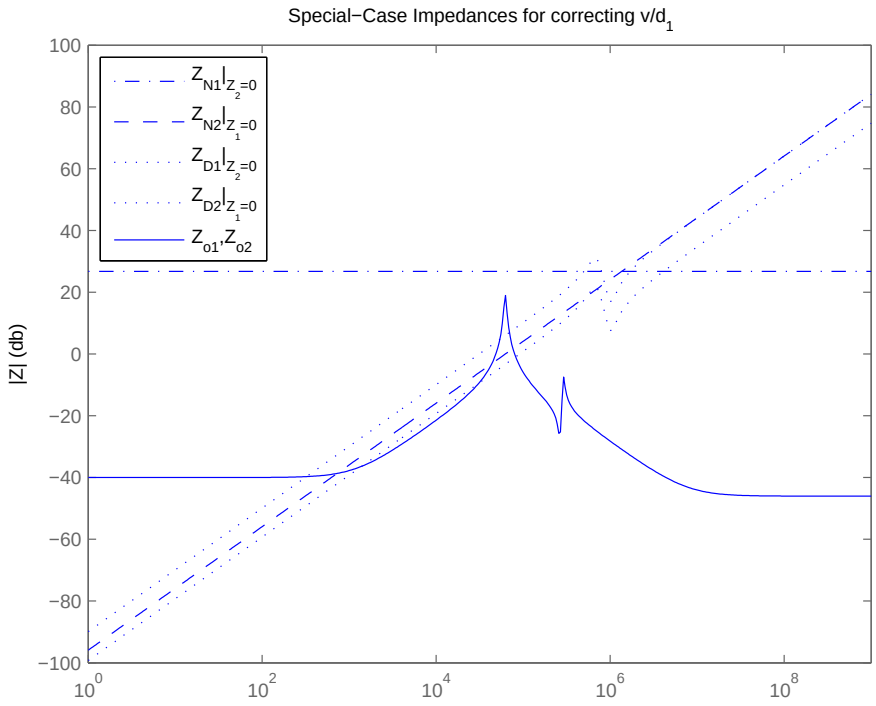


Figure 8-10: The special case impedances for correcting $\hat{v}/\hat{d}_1$ and the input filter output impedances with system parameters: $V_{FC} = 28\text{V}$, $V_{batt} = 48\text{V}$, V_{out}=12V, $R = 2\Omega$, $L_e = 1\mu\text{H}$, $C_e = 1\mu\text{F}$

Bode plots of the correction factors, $CF^{(1)}$ and $CF^{(2)}$, for the converter open-loop transfer functions, $\hat{v}/\hat{d}_1$ and $\hat{v}/\hat{d}_2$ respectively, are shown in Figure 8-11.[2] The correction factor, $CF^{(2)}$, introduces a significant additional phase lag near 10^5 rps. However, the phase lag will not degrade the phase margin unless that phase lag occurs at the cross-over frequency of the entire regulator loop transfer function. In some cases, i.e. when the impedance inequalities in (7.32)-(7.35) are grossly violated,

[2]The simulated data overlayed in the plots of Figure 8-11 was extracted from LTSPICE by comparing simulations of the open-loop transfer functions with and without the input filters in place.

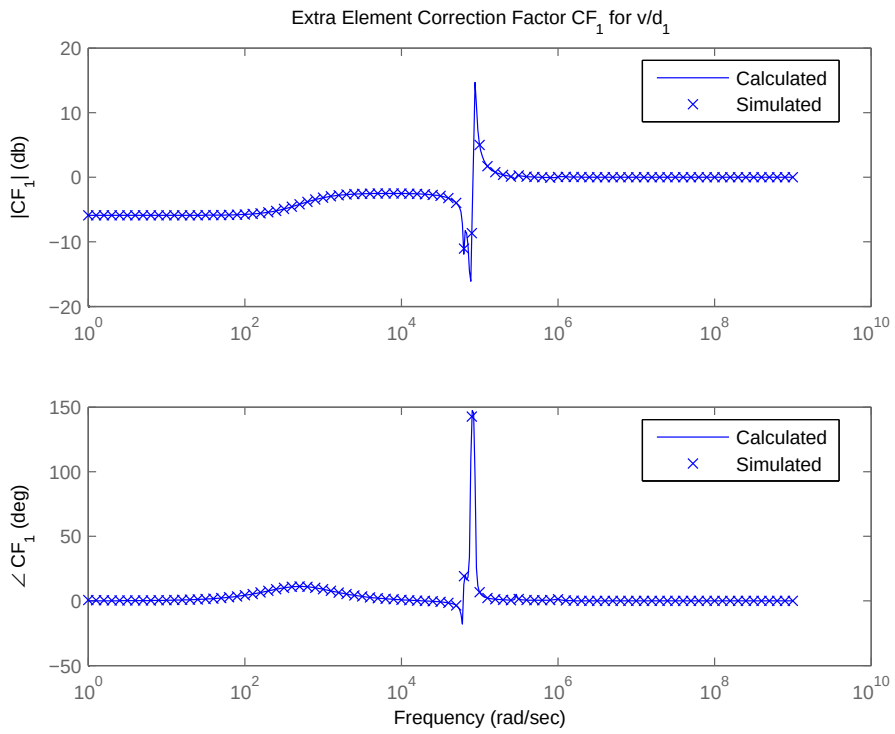
the correction factor will contribute phase lag for a wide band of frequencies likely causing instability. Because the phase lag in this example is contributed for only a narrow range of frequencies it is unlikely to cause instability. The values for the external input filter components in this example were

$$C_{f1} = 100\ \mu\text{F} \tag{8.12}$$

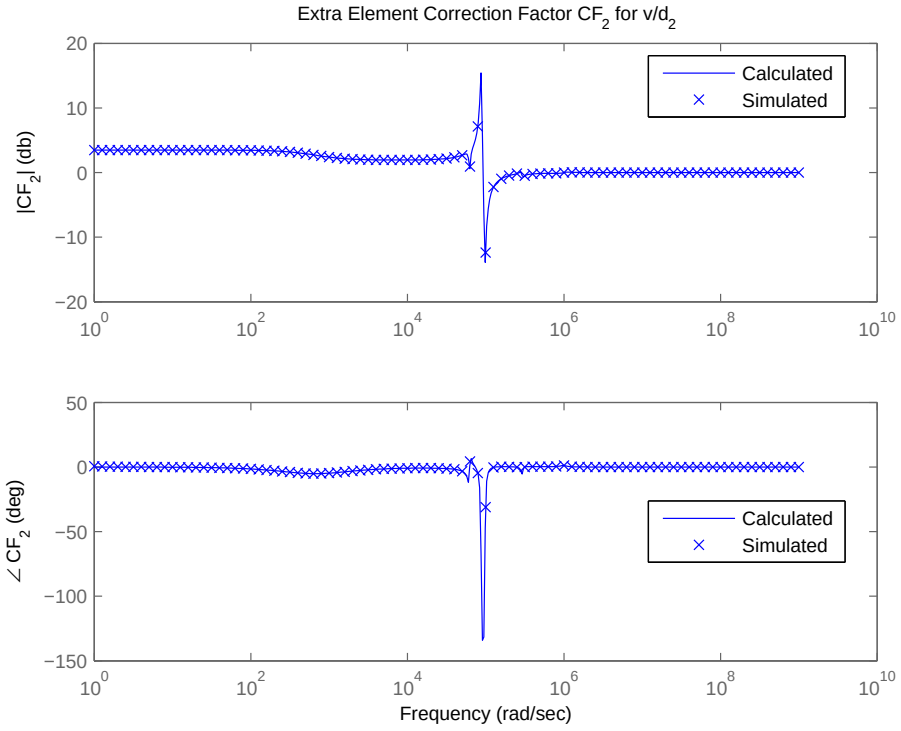
$$R_{D1} = 10\ \Omega \tag{8.13}$$

$$L_{f1} = 6\ \mu\text{H}. \tag{8.14}$$

These were also the values for the filters used in the system of Figure 8-3 represented by L_f and C_f.



(a) $CF^{(1)}$



(b) $CF^{(2)}$

Figure 8-11: Correction factors $CF^{(1)}$ and $CF^{(2)}$ with system parameters: $V_{FC} = 28\text{V}$, $V_{batt} = 48\text{V}$, V_{out}=12V, $R = 2\Omega$, $L_e = 1\mu\text{H}$, $C_e = 1\mu\text{F}$

8.4 Experimental Setup

Figure 8-12 shows an overall schematic of the Siemens 5 kW stack, connections to the built-in power electronics and storage, and the locations of our measurements. Under steady-state operation, the unit is remotely configured to regulate current from the stack. This power is then put on the grid through a three-phase inverter. The stack current is measured using a Tektronix A6303 current probe, while the voltage is measured using an isolated, differential Tektronix 5205 probe. Signals from both probes are recorded using a National Instruments data acquisition system with a PXI-5122 14-bit analog to digital converter. Sampling was conducted at a minimum of 2MS/s to avoid under-sampling issues. Figures 8-14(a) and 8-14(b) show typical data collected from this test setup under steady state operating conditions. The current and voltage levels in Figures 8-14(a) and 8-14(b), nominally 100A and 28V, were typical of the stack load during testing.

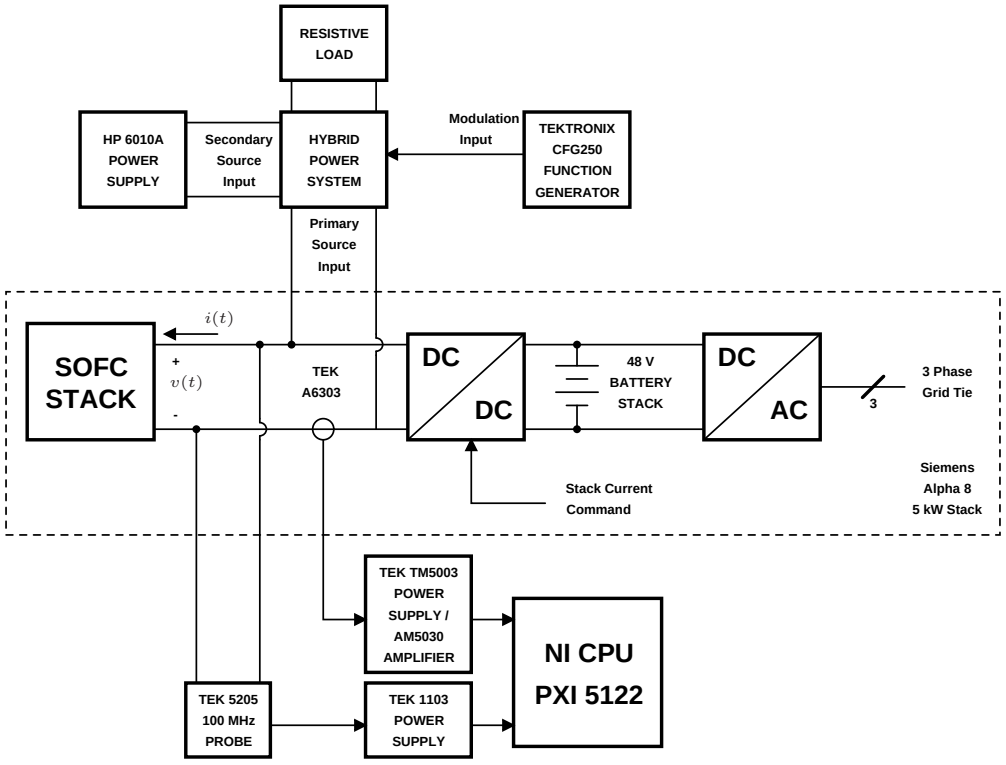


Figure 8-12: Schematic illustration of stack, power electronics, and measurements. Components within the dashed line are within the physical envelope of the Siemens Alpha 8 unit.

8.5 Results

Figure 8-14 shows typical data collected from the test setup in Figure 8-12 with a 1 kHz exogenous excitation imposed by control of the test power electronics. The triangular ripple current in 8-14 at roughly 12 kHz is due to the operation of the front-end boost converter in the Siemens power management system. The current and voltage levels in 8-14, nominally 90 A and 28 V, were typical of the stack load during testing.

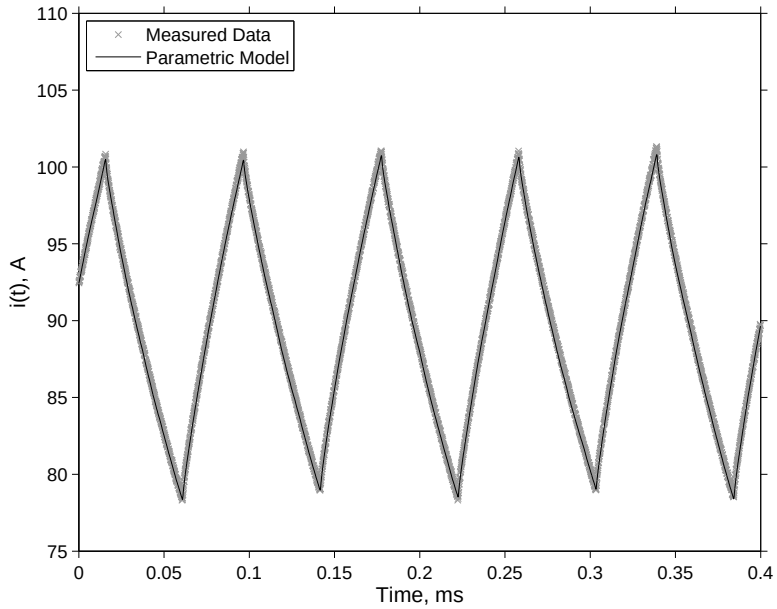
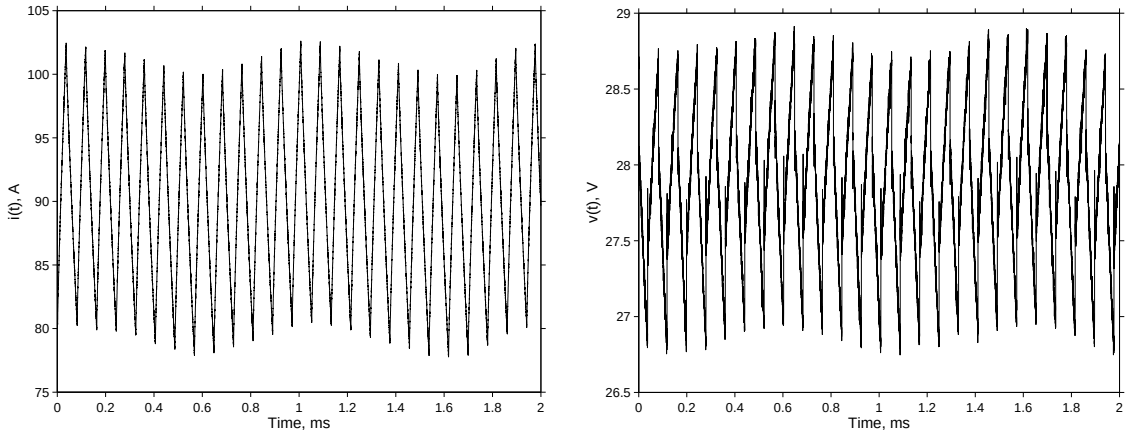


Figure 8-13: Measured and predicted stack current as a function of time.

Figure 8-15 shows Nyquist plots of the impedance $\hat{Z}(j\omega)$ obtained from the response of the stack to the built-in power electronics ripple and the power electronic test signal. The plots were prepared according to the convention for electrochemical impedance spectroscopy results. Figure 8-15(a) shows a plot representing impedances for all frequencies with significant content. The discrete clusters correspond to harmonics of the triangular boost-converter switching waveform, while the more continuous low-frequency data shows the response to the test signal. As the frequency of the harmonics increases, the amplitude decreases, and the variance in the impedance estimate increases. Figure 8-15(b) is an expanded view of the low frequency portion corresponding to the exogenous excitation. The arc shape of the curve in Figure 8-

15(b) is consistent with the series connection of parallel RC elements often used in equivalent circuit models of fuel cells.

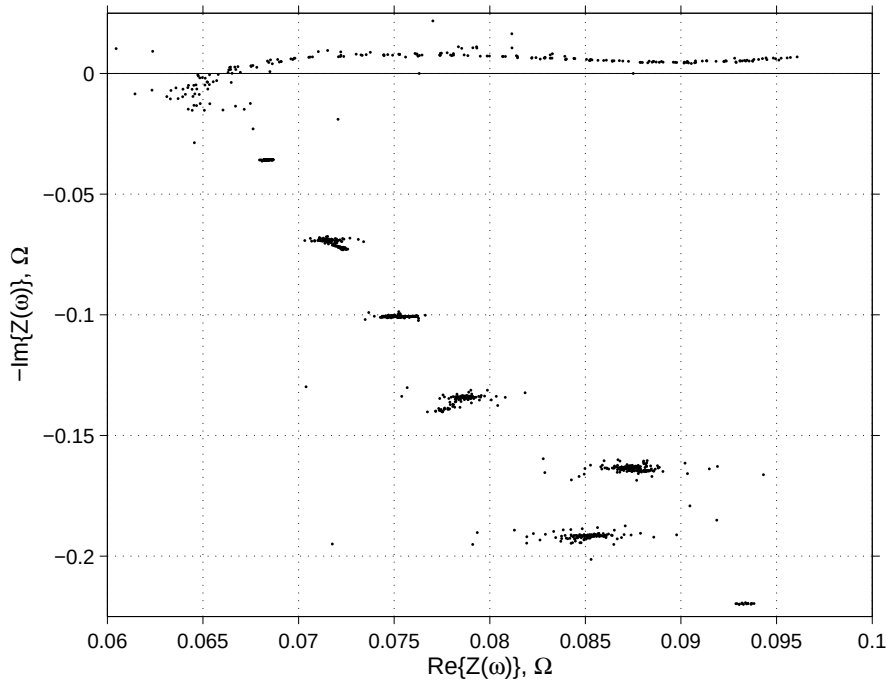


(a) Stack current as a function of time.

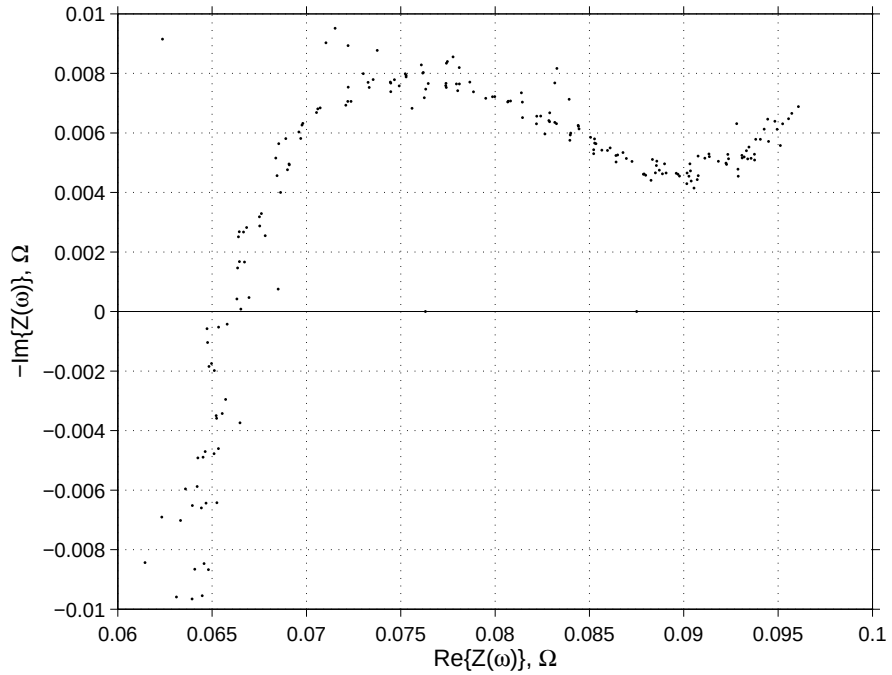
(b) Stack voltage as a function of time.

Figure 8-14: Stack current and voltage, measured as indicated in fig:hybridex1 8-12. The triangle current waveform in 8-14(a) is due to the operation of the DC/DC converter in the system. The corresponding voltage of the stack appears in 8-14(b).

Data corresponding to a 1 kHz power electronic excitation were used to identify the parametric model in 8.1.2. The parameter estimates were $V_{oc} = 34.1V$, $R = 0.0690\Omega$, and $L = 0.43\ \mu H$. These results compare favorably to those in [153], where the values for these parameters based on data taken months earlier were found to be $V_{oc} = 34.7$ V, $R = 0.0677\ \Omega$, and $L = 0.471\ \mu H$. The decrease in voltage and increase in resistance are likely due to the gradual degradation of stack performance observed over this time period. The latest parameters were used for an output-error prediction of the time-domain current waveform in response a 5.4 kHz excitation. This cross-validation result is shown in 8-13.



(a)



(b)

Figure 8-15: Whole stack impedance spectroscopy results. (a) Stack response to ripple current and power electronic test signal. (b) Low-frequency portion of stack response showing response to power electronic test signal.

Chapter 9

Design Example 2: Run-time Integral Diagnostics of a Fuel Cell under Unmanned Aerial Vehicle Load Profiles

This section presents a hybrid power system designed for integral fuel cell diagnostics in applications having widely varying load power. The primary function of the hybrid power system will be to provide a fixed fuel cell operating current with a superposed frequency sweepable EIS signal despite varying load currents. As an illustrative example, the integral diagnostic functionality of the hybrid power system is demonstrated under simulated unmanned aerial vehicle (UAV) time-domain load profiles. The underlying motivation to diagnose and even heal a damaged fuel cell is demonstrated experimentally through intentional damaging followed by recovery in conjunction with runtime impedance measurements that support predegradation, postdegradation, and postrecovery conditions of the fuel cell.

9.1 Current-Voltage Regulated Power System Architecture

The system architecture is a master-slave current-voltage regulated hybrid power system like the one analyzed in Section 6.7. Figure 9-1 shows a schematic depiction of the hybrid power system and the basic elements of the feedback control. Figure 9-1(b) shows the small-signal current path for the EIS signal. The nominal system parameters are shown in Table 9.1.

Table 9.1: Nominal fuel cell master-slave system parameters

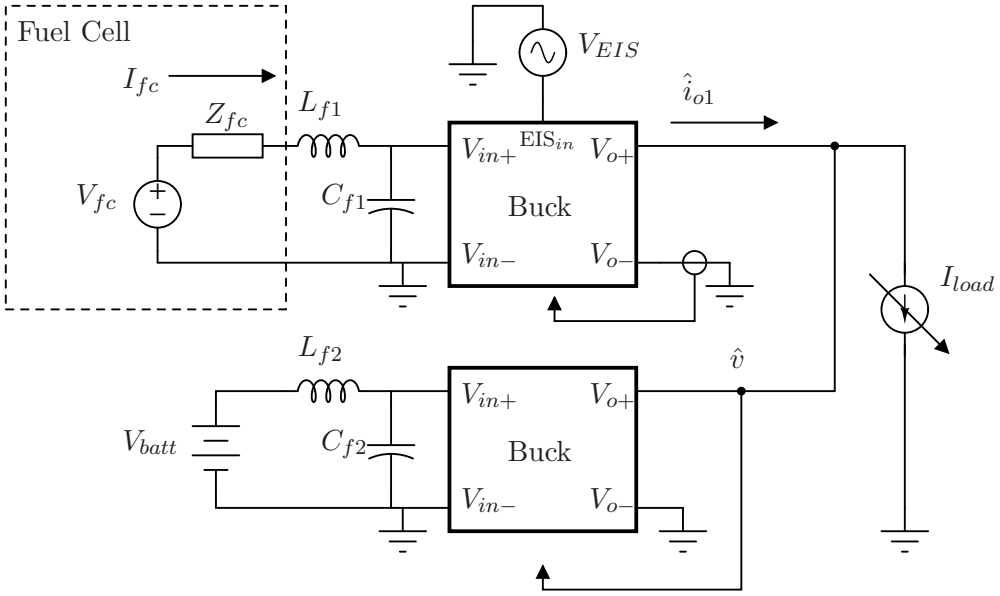
Parameter	Symbol	Value
Fuel cell Voltage	V_{fc}	12 V
Battery Voltage	V_{batt}	12 V
Fuel cell Current	I_{fc}	4 A
Battery Current	I_{batt}	-2 A to $+8$ A
Buck switching freq.	f_{sw}	400 kHz
Buck switching devices	M_i	IRFB3607

In our experimental setup, the load is modeled as a time-varying current source. The fuel cell is furnished by the current-regulated DC/DC converter so that the fuel cell operating current may be fixed despite variations in the load current. The battery is furnished by the voltage-regulated DC/DC converter so that it provides the excess load current while constraining the load voltage. The excess load current may be positive or negative so the voltage-regulated converter was designed to support bidirectional current flow. Notably, when the excess load current is negative, the battery is automatically recharged by the fuel cell.

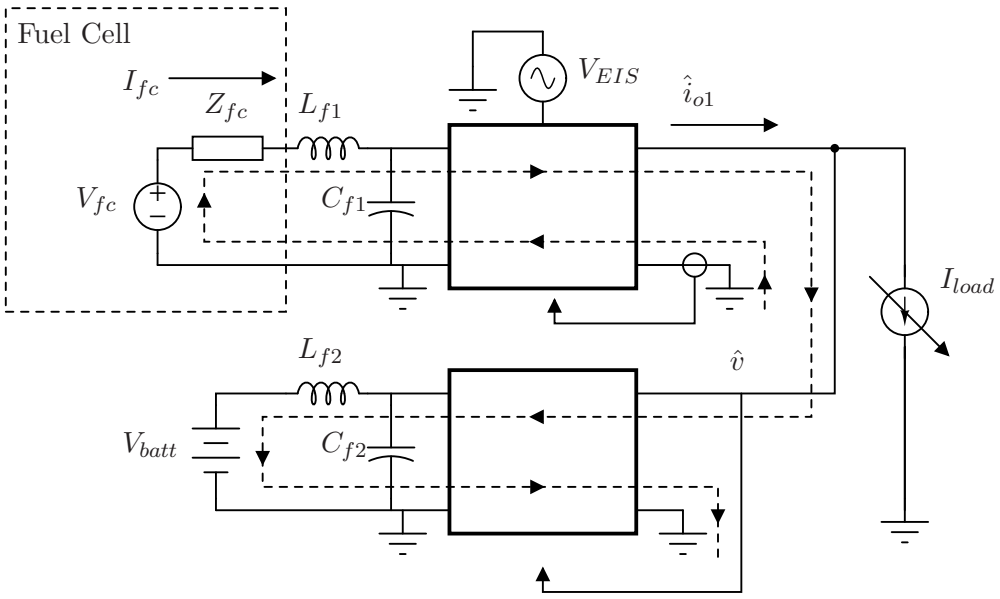
The design of the buck converters and the feedback control is detailed here. The feedback control circuitry was designed for good voltage and current regulation, wide bandwidth to support the frequency sweepable EIS signal as well as the obvious need for stable closed loop operation. A useful target for the fuel cell (FC) EIS signal bandwidth is 1 kHz.

9.2 Feedback Compensation

In this hard-switched converter topology, there is a fundamental tradeoff among converter efficiency and closed-loop bandwidth that is manifested in the choice of switching frequency. The requirement for good switching frequency attenuation in the loop transfer functions contends directly with the requirement for wide loop bandwidth. The feedback compensation strategy employs a lead compensator to improve the loop bandwidth and an additional high frequency pole for added attenuation at the switching frequency. The location of the added high frequency pole was chosen to tradeoff closed-loop stability (phase margin) for switching frequency attenuation. The loop transfer functions in Figure 9-2 indicate the tradeoffs described above with reasonable phase margin and loop bandwidths that ultimately support EIS excitation signals having sufficient bandwidth.

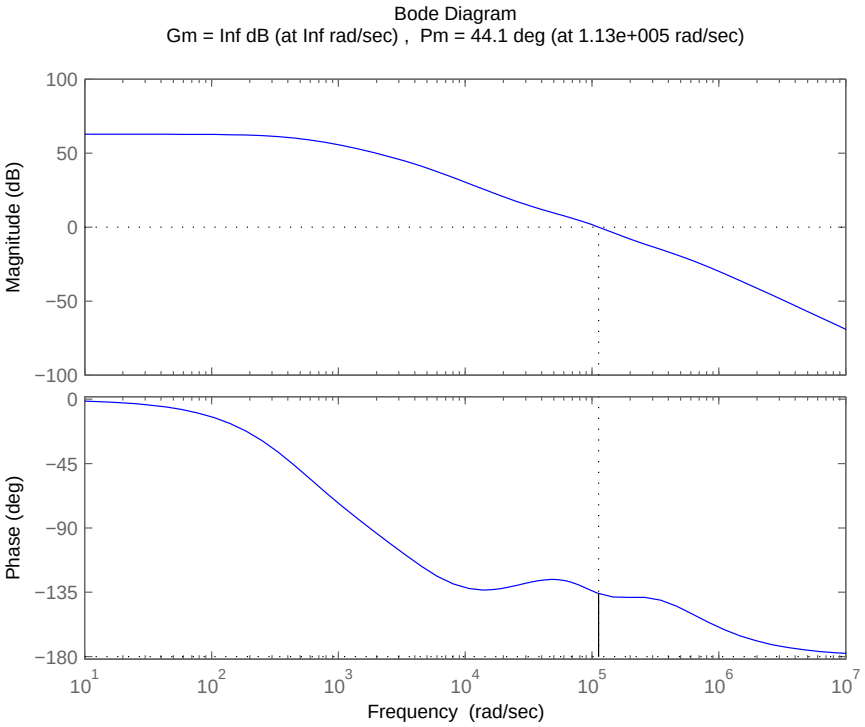


(a) A simplified connection diagram of the hybrid system.

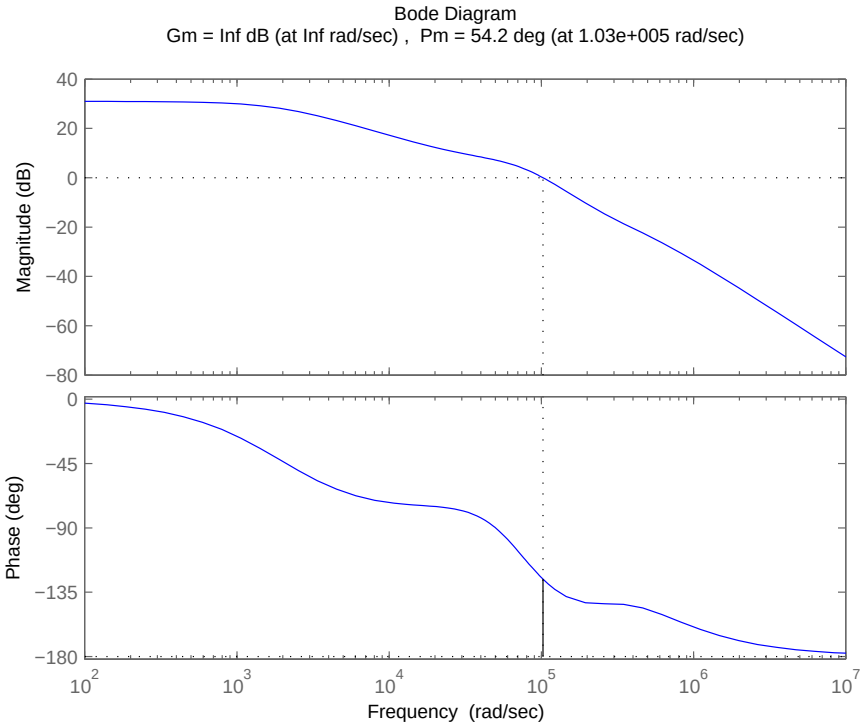


(b) Desired small-signal current paths for EIS excitation signals.

Figure 9-1: A hybrid power system with EIS functionality built upon a Master-Slave current-voltage regulated architecture.



(a) Current feedback loop

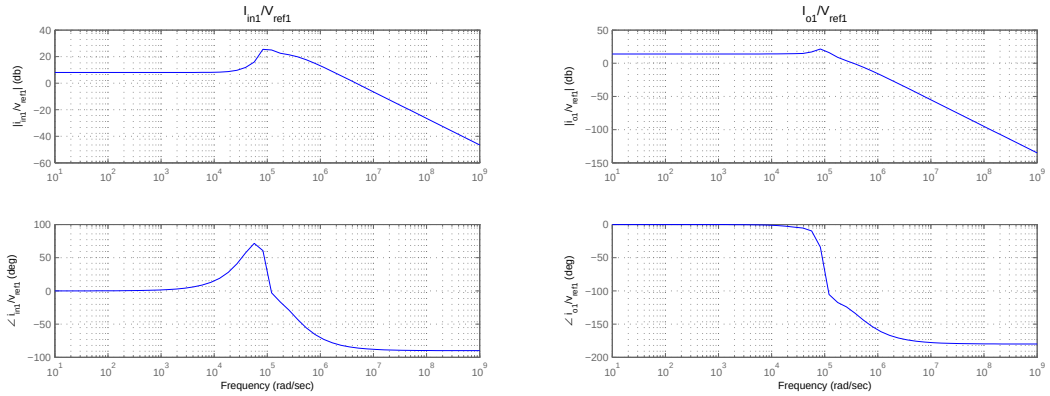


(b) Voltage feedback loop

Figure 9-2: Open-loop bode plots indicate tradeoffs among loop bandwidth, switching frequency attenuation and stability.

9.3 Closed-Loop Responses

The closed-loop response was simulated based on the analysis in Chapter 6. The key closed-loop transfer functions are shown in Figure 9-3.



(a) Control voltage to fuel cell current

(b) Control voltage to first converter's output current

(c) Control voltage to load voltage

(d) Load current to fuel cell current

Figure 9-3: Simulated closed-loop bode plots indicate suitable fuel cell excitation current bandwidth, good load voltage regulation and good fuel cell current buffering.

Figure 9-3(a) shows the fuel cell current in response to the control voltage. It shows a bandwidth that is sufficient for the target 1 kHz upper band limit on fuel EIS currents. Figure 9-3(c) indicates a relatively small magnitude transfer function from the control voltage to the load voltage. The response in Figures 9-3(a) and 9-3(c) confirm that the control signal needed to achieve suitable excitation currents for the EIS measurements should lead to a relatively small disturbance of the load. Finally, Figure 9-3(d) shows the fuel current response to load current perturbations.

The plot shows a significant attenuation at low frequency in this regard indicating suitable buffering of the fuel cell current from the variations in the load current.

9.3.1 Low Frequency Fuel Cell Current Buffering

From the discussion in Section 6.7, the zero frequency closed-loop output impedance of the current-regulated converter relies on series resistances. Figure 9-4 shows the closed loop transfer function of the first converter's input current to load current perturbations having added 500 mΩ of series resistance to that converter's output inductor. The plots shows an added 20 db of attenuation at low frequency. However the added resistance represents an extra 50 W of dissipation for 10 A of output current. Clearly, if this method is used to improve current buffering, there will be a tradeoff in efficiency, not to mention complexity in thermal management.

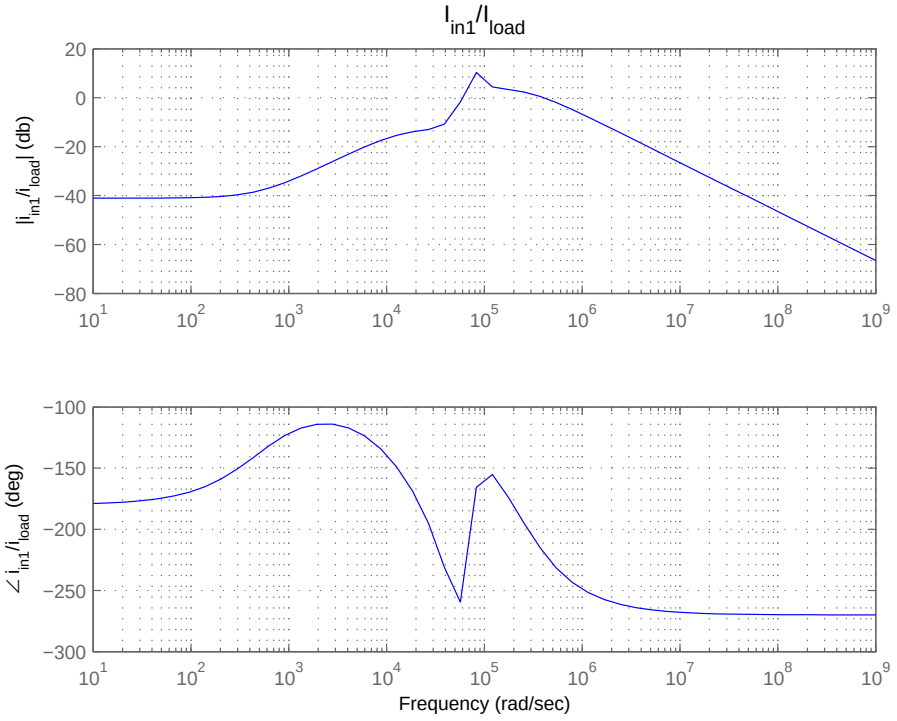


Figure 9-4: Closed loop response from load current to fuel cell current with 500 mΩ of extra inductor ESR.

9.4 Input Filter

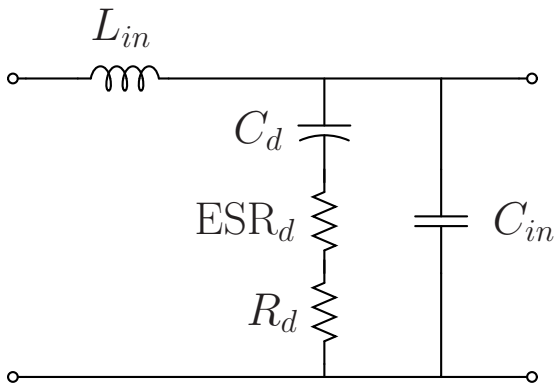
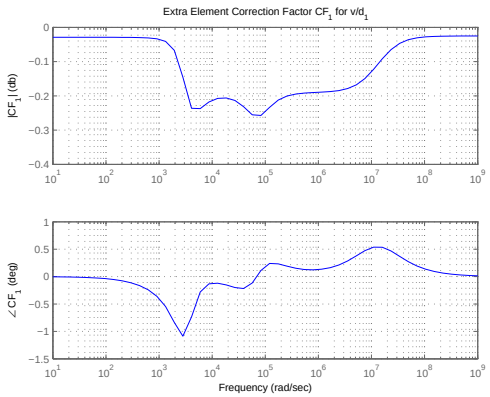
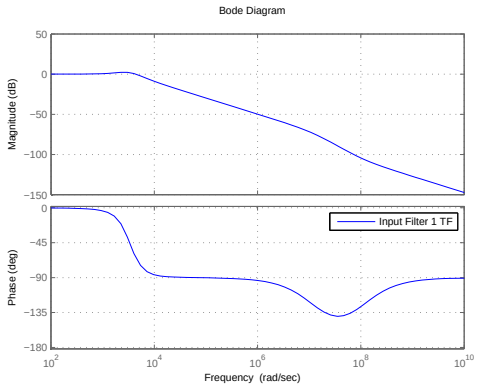


Figure 9-5: The basic input filter topology

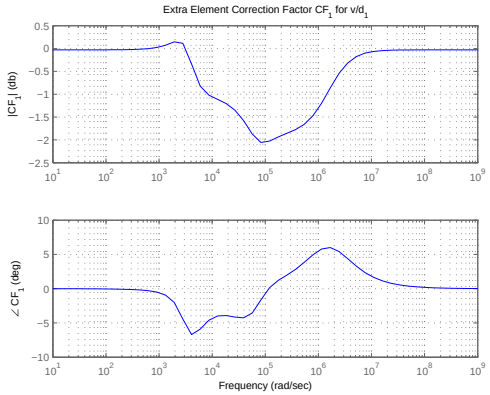
Having designed the converter to meet the dynamic requirements of the runtime integral diagnostics, we add an input filter to attenuate switching frequency content at the fuel cell and battery terminals. The evaluation of the chosen input filters for regarding their impact on closed-loop stability was guided by the application of the 2EET detailed in Section 7.2. The filter was chosen not only to attenuate switching ripple, but to pass the excitation signal among the stability guidelines imposed by the 2EET.



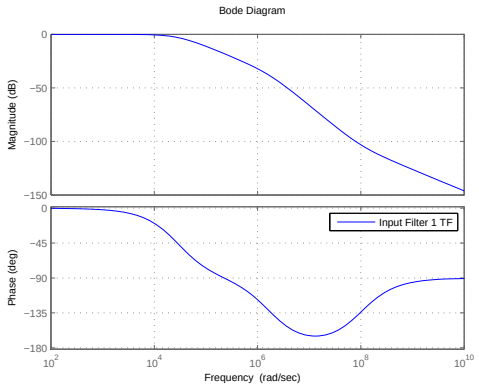
(a) $\mathrm{CF}_1, R_d = 0\ \Omega$



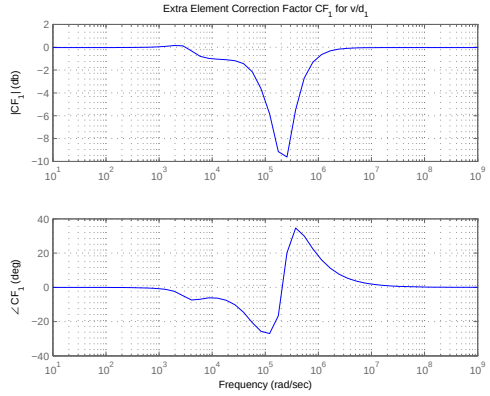
(b) Input filter 1, $R_d = 0\ \Omega$



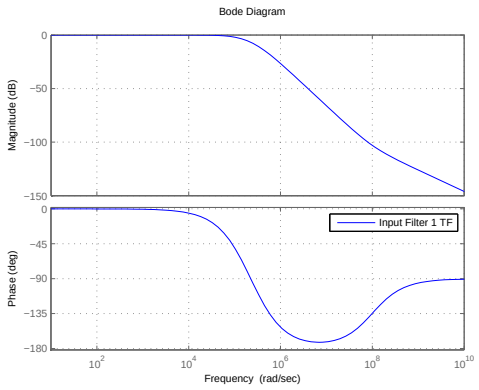
(c) $\mathrm{CF}_1, R_d = 0.5\ \Omega$



(d) Input filter 1, $R_d = 0.5\ \Omega$



(e) $\mathrm{CF}_1, R_d = 2\ \Omega$

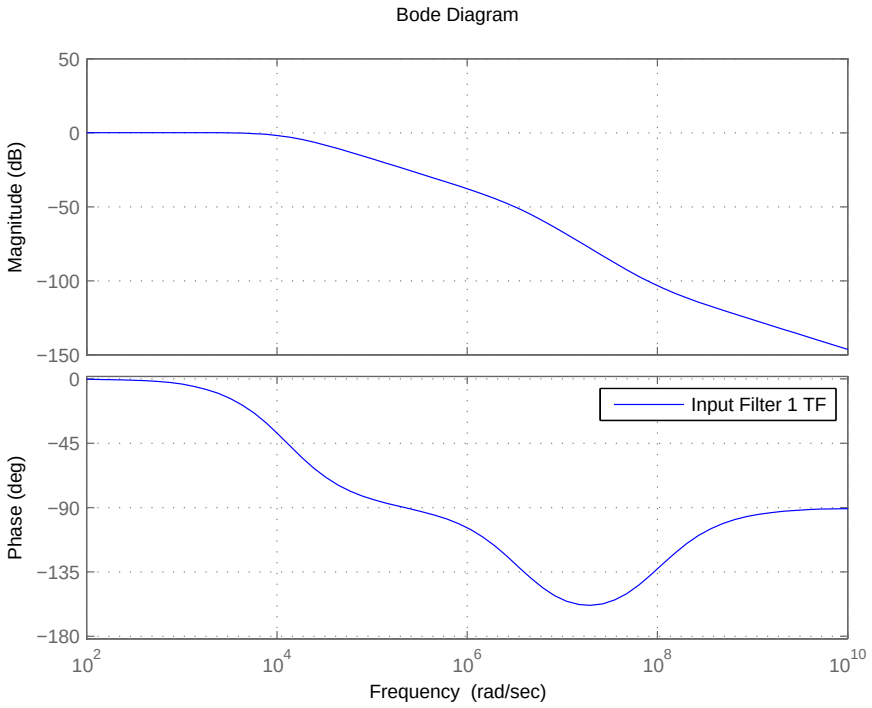


(f) Input filter 1, $R_d = 2\ \Omega$

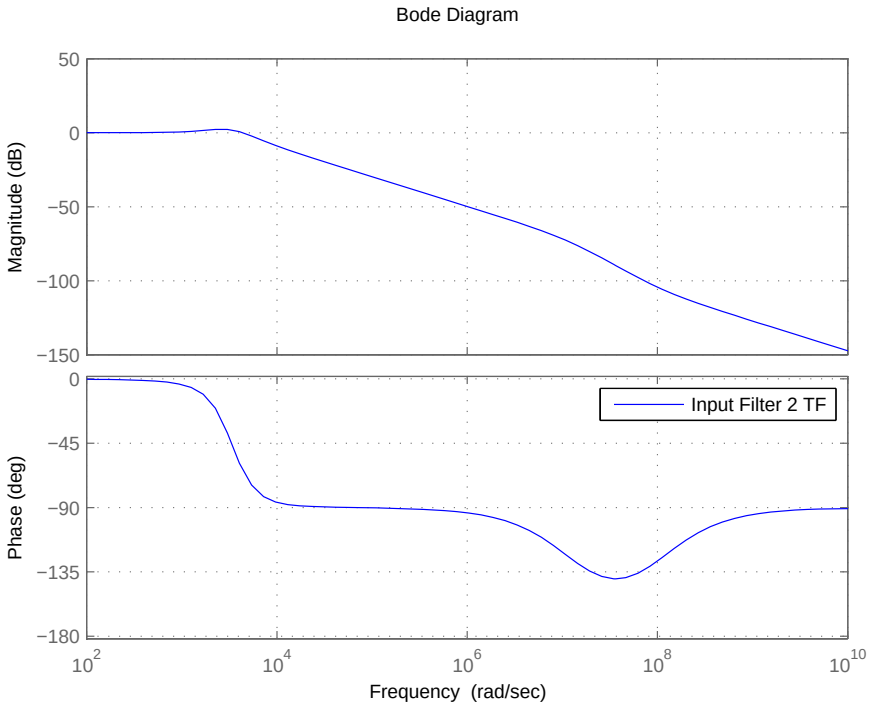
Figure 9-6: The tradeoff between input filter negative phase contribution and bandwidth

The basic input filter topology is shown in Figure 9-5. The filter elements L_{in} and C_{in} are chosen for good attenuation at the switching frequency. The capacitor C_d is chosen to be very large so that it represents a low impedance at frequencies near the bandwidth imposed by L_{in} and C_{in}. The damping resistor, R_d, is chosen to limit the peaking the output impedance of the input filter in order to satisfy the impedance inequalities derived from the 2EET in Section 7.2. Decreasing the value of R_d improves this effect. However, the value of R_d can be optimized to pass EIS excitation signals. Figure 9-6 illustrates the tradeoff between the first converter's input filter bandwidth and the negative phase contribution for one of the correction factors.

A compromise in the value of R_d was chosen for acceptable phase margin and optimized transmission of EIS signals to the fuel cell terminals. The input filter transfer functions are shown in Figure 9-7. The corresponding extra-element correction factor bode plots are shown in Figures 9-8 and 9-9. The input filter transfer function for the fuel cell converter shows good transmission of the EIS signal while the correction factors indicate acceptable maximum negative phase contributions. Note also that the negative phase contributions indicated by the correction factors are narrowband. That is, they will only impact the stability if the location of the negative phase contribution is very close to the cross-over frequency of the corresponding loop transfer function.

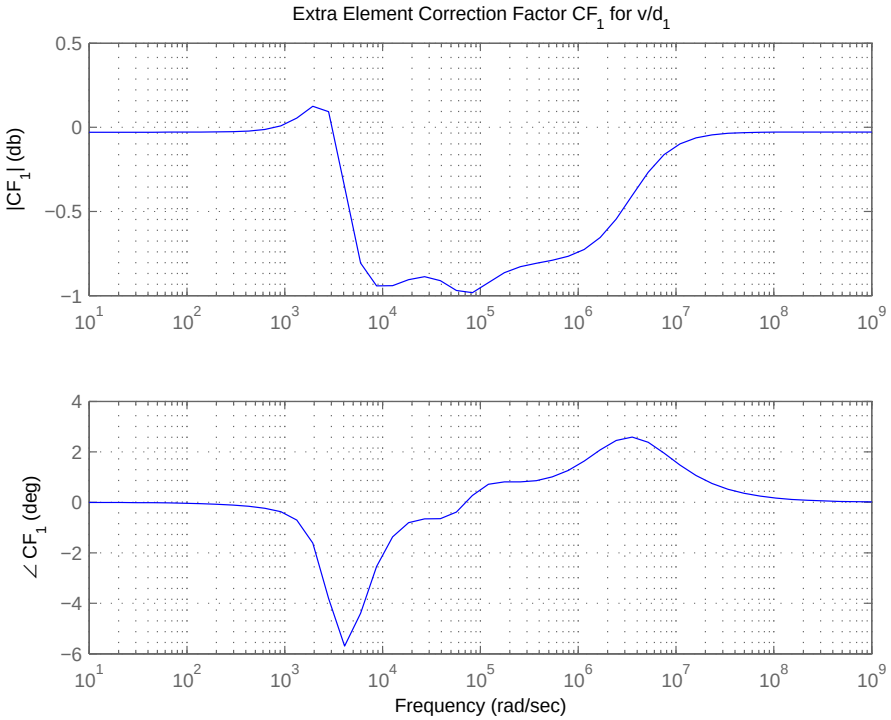


(a) Fuel Cell side Input Filter

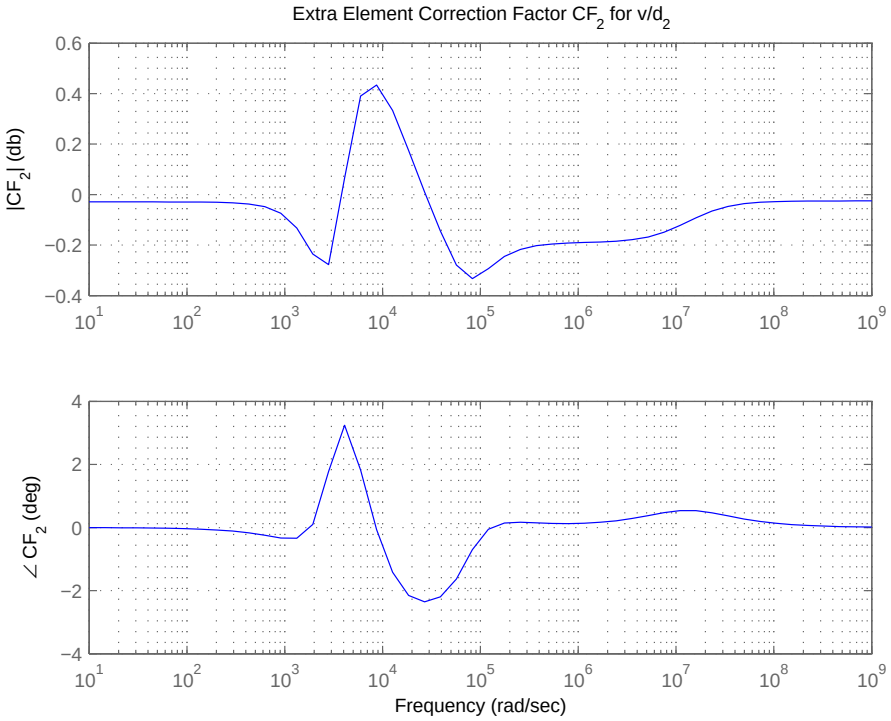


(b) Battery side Input Filter

Figure 9-7: Input filter transfer functions

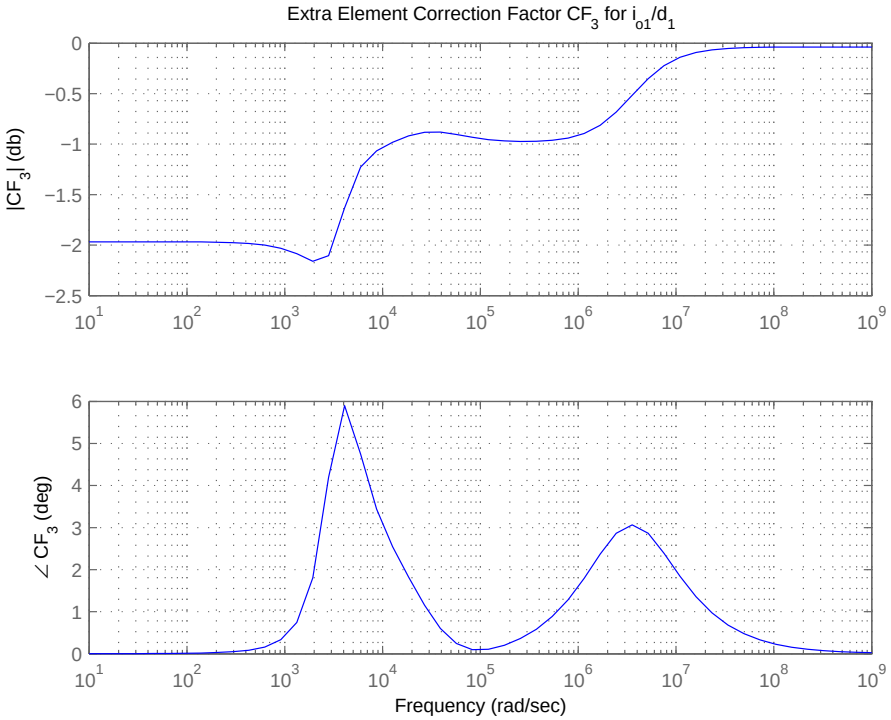


(a) CF_1

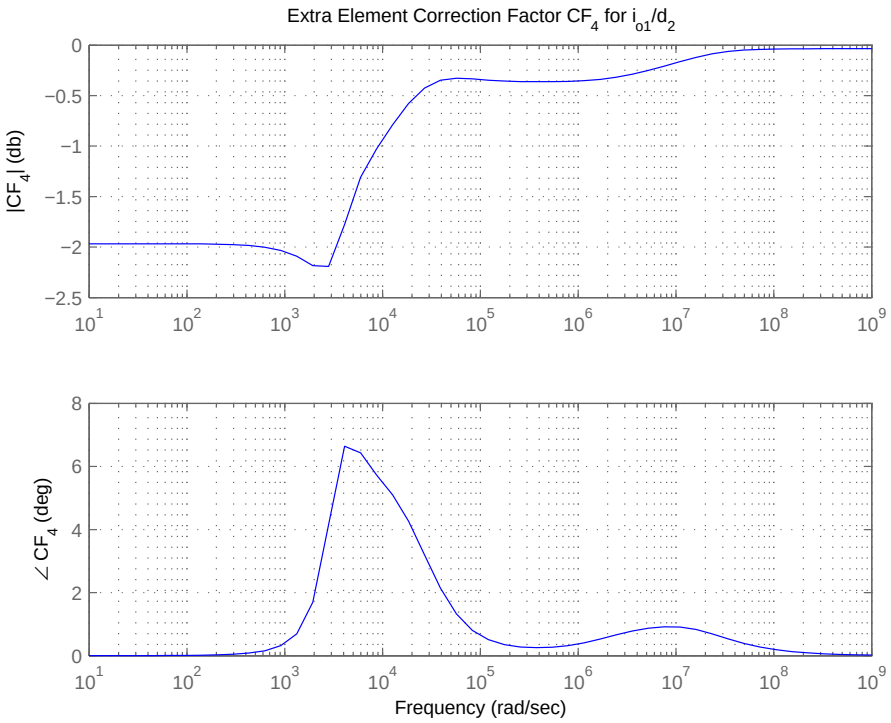


(b) CF_2

Figure 9-8: Extra element correction factors for the voltage feedback loop



(a) CF_3



(b) CF_4

Figure 9-9: Extra element correction factors for the current feedback loop

9.5 Implementation

The implemented hybrid power system schematic is shown in Appendix B.1.2. The switching sections are Buck converters using synchronous rectifiers to enable bidirectional current flow. The MOSFETs were chosen to support an output current of 20 A and an input voltage of 15 V. Light RC snubbers reduce losses resulting from ringing drain-source ringing. The EIS control signal is ac-coupled into the fuel cell side control loop at v_{refac}. To accommodate the possibility of a negative fuel cell operating current e.g. one that would be appropriate for a reversible fuel cell, an adjustable offset is added to the fuel cell side output current measurement ("Negative output current adjust").

9.5.1 Gain-Lead Compensator-Subtractor

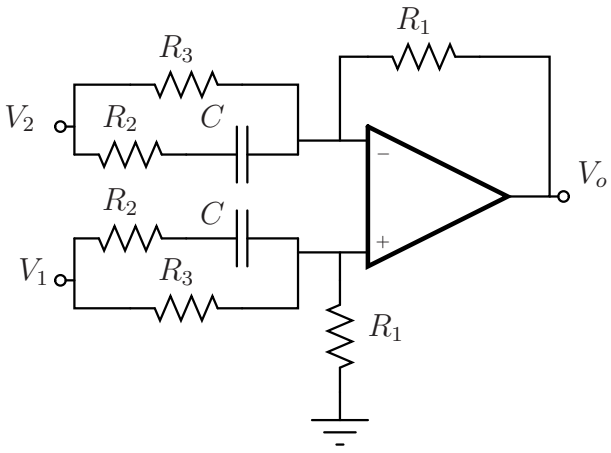
A single op-amp circuit serves as a lead compensator, gain and subtractor on the fuel cell side. The additional high frequency pole is added by the simple RC low-pass filter that follows the lead compensator. The lead compensator-gain-subtractor in Figure 9-10(a) has the transfer function

$$v_o = \frac{R_1}{R_3}\frac{1 + sC(R_2 + R_3)}{1 + sCR_2}\left(v_1 - v_2\right). \tag{9.1}$$

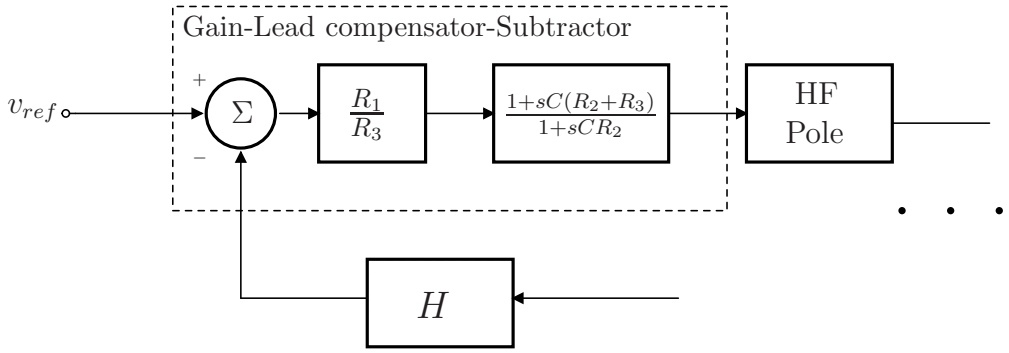
A block diagram representation of the compensator circuit in the context of the feedback control loop is shown in Figure 9-10(b).

9.6 Measured Step Responses

Step responses were taken from the implemented system most notably to verify closed-loop stability. Figure 9-11 shows the step response from the first converter's control voltage to the first converter's output current. The step response indicates suitable phase margin for the current-feedback loop in agreement with the simulated loop transfer function in Figure 9-2(a). The small-signal step response shows a 90% rise



(a) The gain-lead compensator-subtractor



(b) The gain-lead compensator-subtractor block diagram representation

Figure 9-10: The lead compensator subtractor and gain circuit

time of approximately 25 μs. From [92], this corresponds to a closed-loop bandwidth for a second order system of approximately

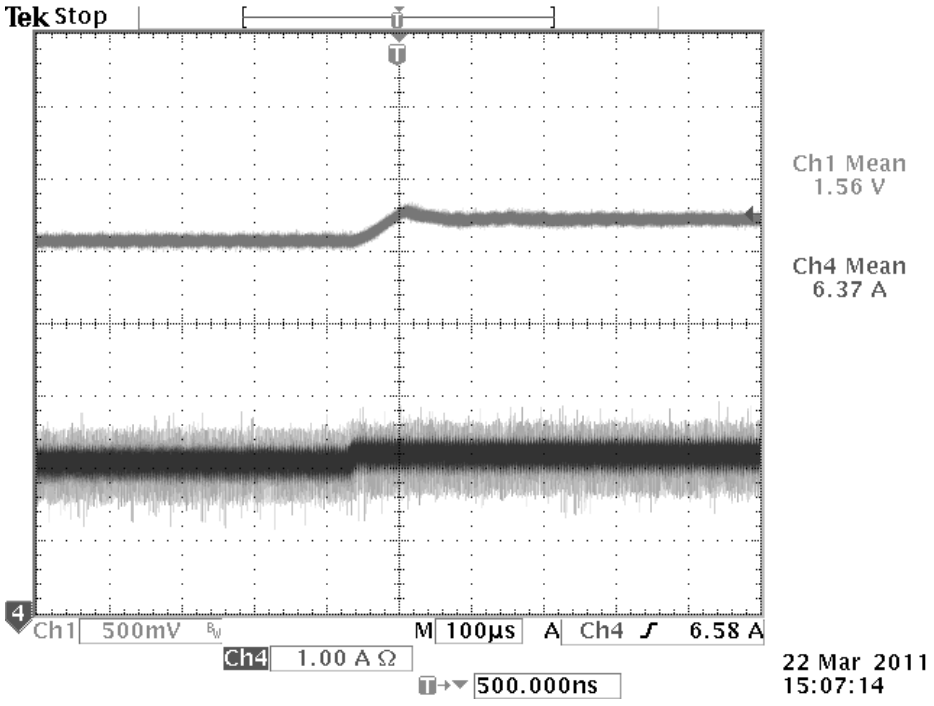
$$\omega_h \approx \frac{2.2}{t_r} = 88 \text{ krps}, \tag{9.2}$$

which is in good agreement with the simulated closed loop response in Figure 9-3(b). From [92], because the current-control loop exhibits a phase margin of 45°, we expect approximately a 20% overshoot in the small-signal step response also in agreement with Figure 9-11(a).

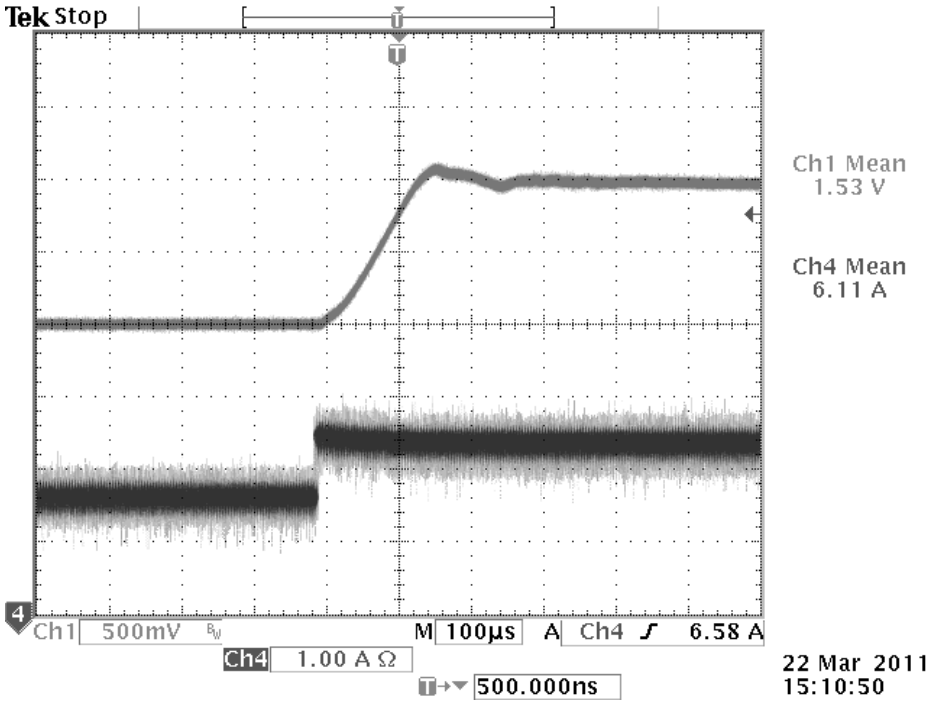
Figure 9-12 shows the large and small step responses from the second converter's control voltage to the load voltage. The step responses indicate suitable phase margin in agreement with the simulated loop transfer function in Figure 9-2(b) and good

voltage regulation. The ripple visible on the small step response in Figure 9-12(a) is converter ripple not an oscillation.

Figure 9-13 shows the step response from the load current to the first converter's input current (the fuel cell current). The low frequency behavior shows an attenuation in agreement with the simulated low frequency behavior in Figure 9-3(d). The high frequency magnitude response shown in Figure 9-3(d) peaks around 15 kHz corresponding to a timescale of about 100 μs. The step response in Figure 9-13 shows a larger response on the timescale of about 100 μs in agreement with the simulated frequency behavior.

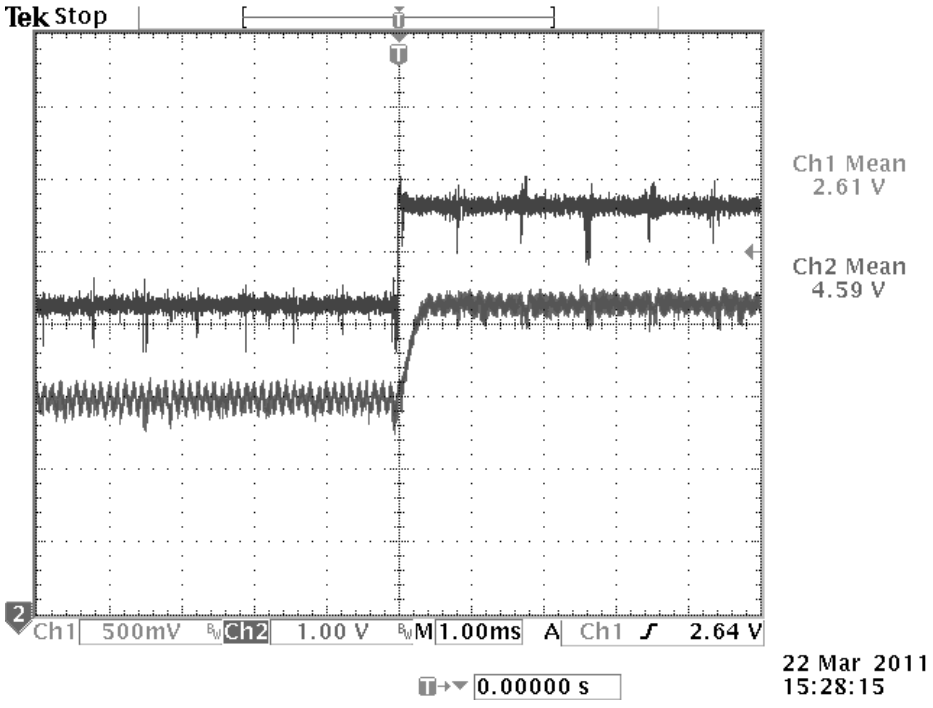


(a) Small step

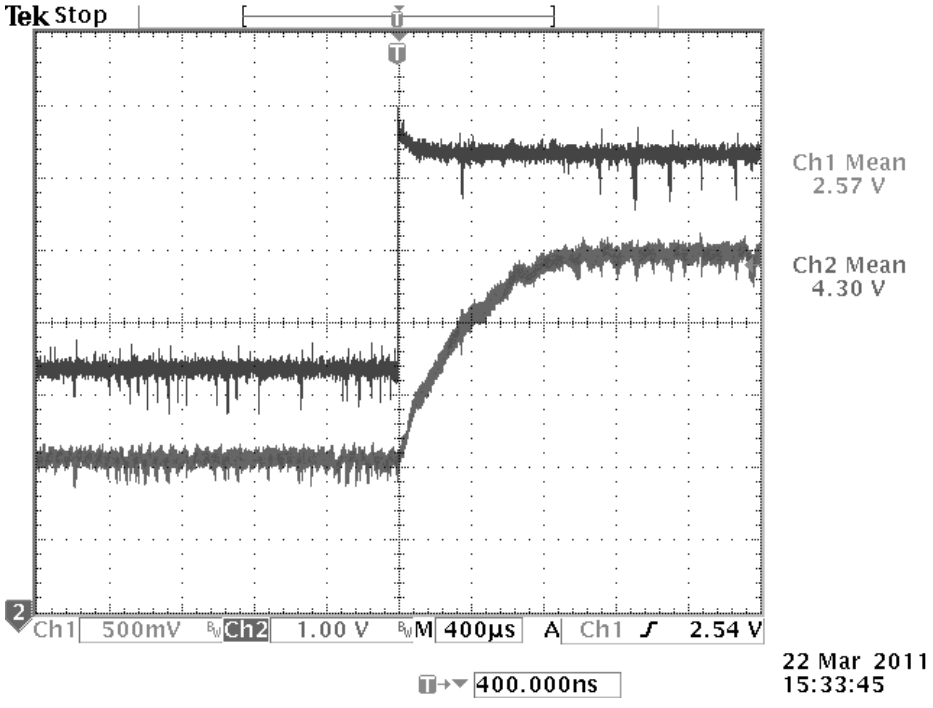


(b) Large step

Figure 9-11: First converter's control voltage to first converter's output current. Ch1: $\hat{v}_{ref1}$, ch4: $\hat{i}_{o1}$

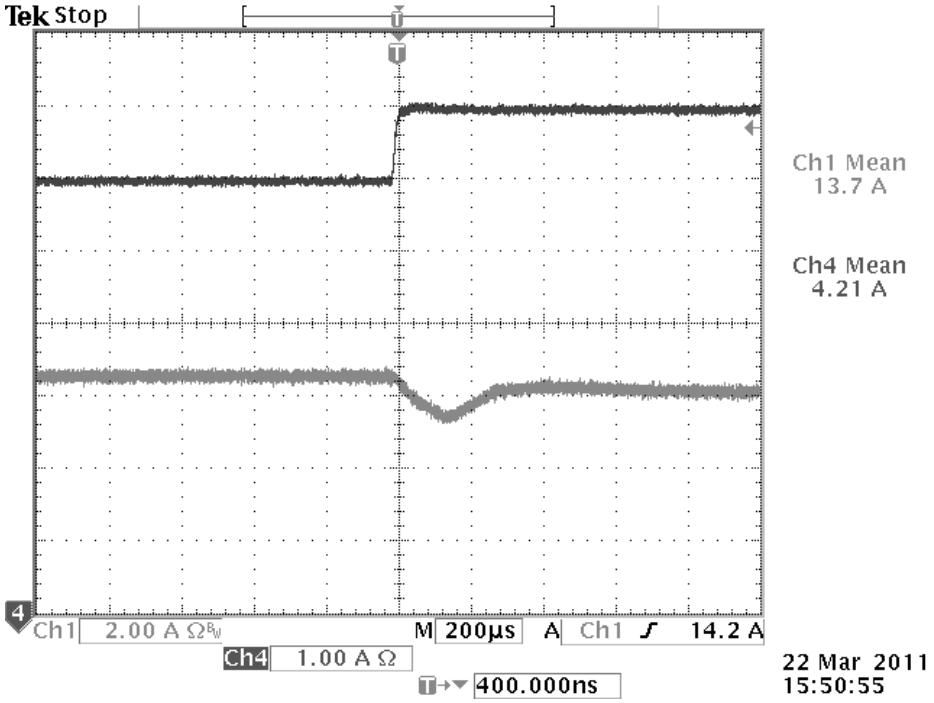


(a) Small step

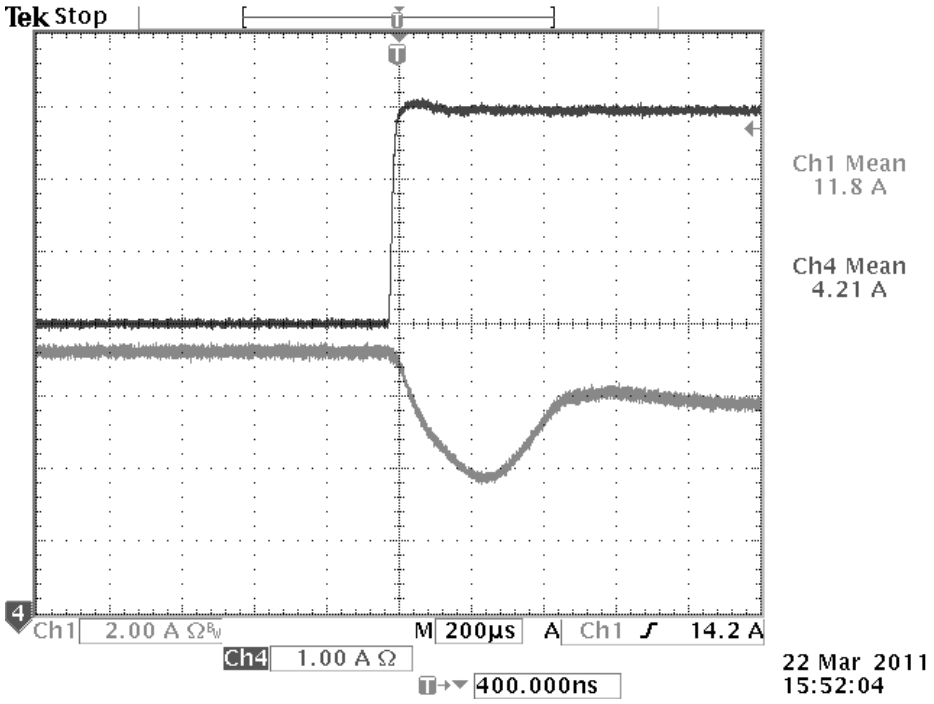


(b) Large step

Figure 9-12: Second converter's control voltage to load voltage. Ch1: $\hat{v}_{ref2}$, ch2: $\hat{v}$



(a) Small step



(b) Large step

Figure 9-13: Load current to first converter's input current. Ch1: $\hat{i}_{load}$, ch4: $\hat{i}_{iin1}$

9.7 Experimental Setup

A connection diagram of the experimental setup is shown in Figure 9-14. The experimental setup consists of the two-converter current-voltage regulated power system, two power sources and an Agilent N3300A electronic load. The solid-oxide fuel cell (SOFC) in this experiment was available through a collaboration with Montana State University (MSU). The fuel cell power source consisted of a subsystem - an electronically simulated fuel cell stack - the reference simulator. This subsystem, shown on the left side of Figure 9-14, will be described in Section 9.7.1. The second power source was a bidirectional power source, either a lead-acid battery or a bipolar linear power amplifier depending on the particular experiment.

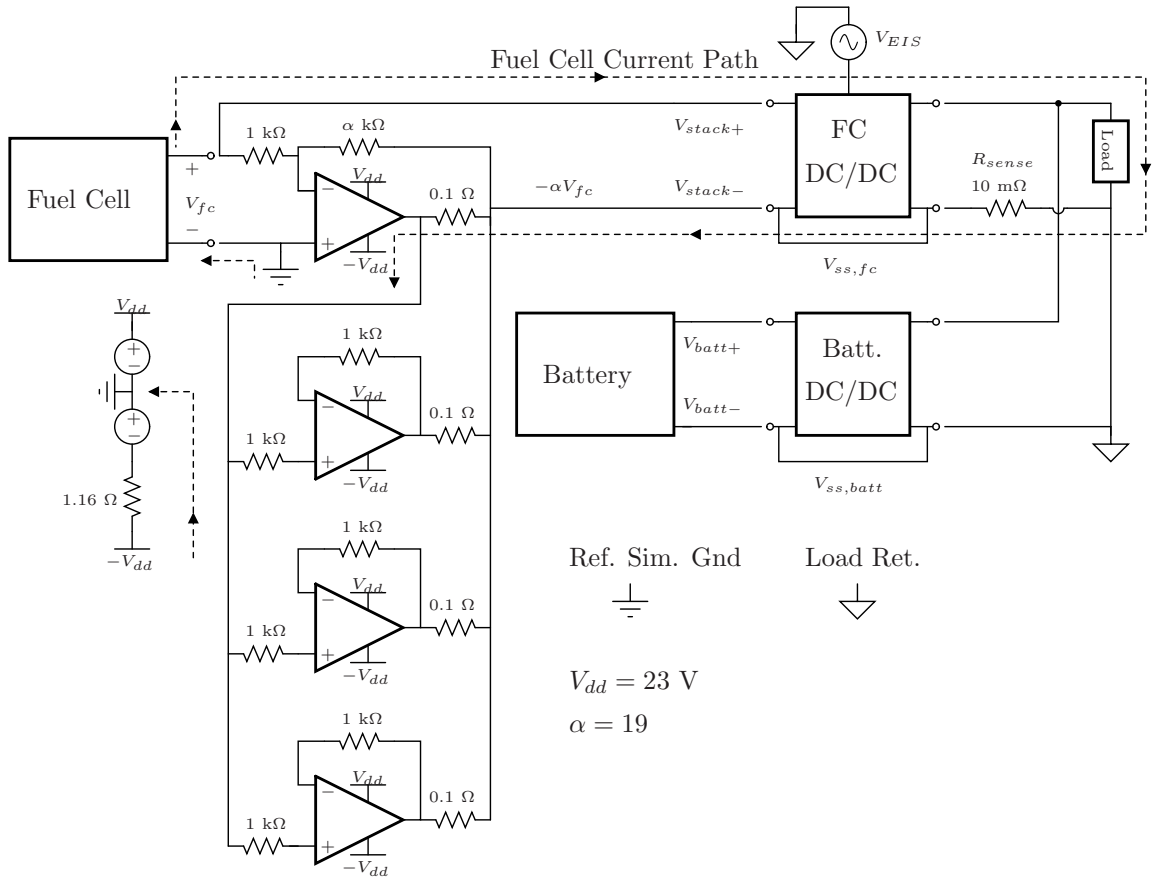


Figure 9-14: The experimental setup block diagram with the Montana State University fuel cell reference simulator.

A photograph of the full experimental setup is shown in Figure 9-15. The power

converters and the data acquisition inputs are shown on the left. The measurement, signal generation and power supplies are shown in the middle of the photo. The fuel cell reference simulator, fuel cell ovens, mass flow and temperature controllers, and fuel bottles are shown on the right.

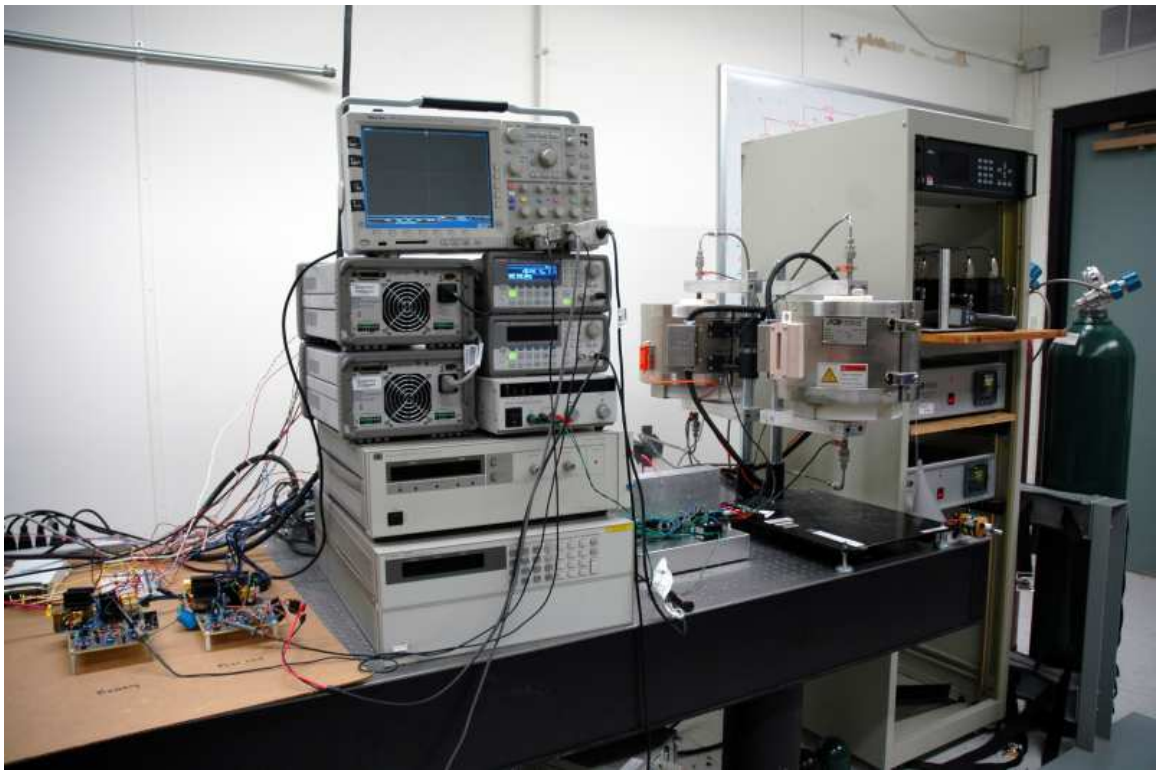


Figure 9-15: A photograph of the full experimental setup including the data acquisition system, power converters, measurement and power supplies, and the fuel cell setup.

Photographs of the full fuel cell setup are shown in Figures 9-16, 9-16 and 9-18. Figure 9-16 shows the solid-oxide fuel cell ovens, the mass flow and temperature controllers and the hydrogen and oxygen fuel bottles. The solid-oxide fuel cell ovens with gas feed-throughs are shown in Figure 9-17. The ovens were heated to a temperature of 750°C. Electrical terminal were available at the top and bottom of each oven. Figure 9-18 shows a closupe of the mass flow controllers that control the flow of fuel into the ovens. The nominal fuel rates were 260 SCCM H2, 100 SCCM O2.

Figure 9-16: A photograph of the two solid-oxide fuel cell ovens, temperature control units and mass flow controllers used in the integral diagnostics experiments.

Figure 9-17: A closeup photograph of the two solid-oxide fuel cell ovens, temperature control units and mass flow controllers used in the integral diagnostics experiments.

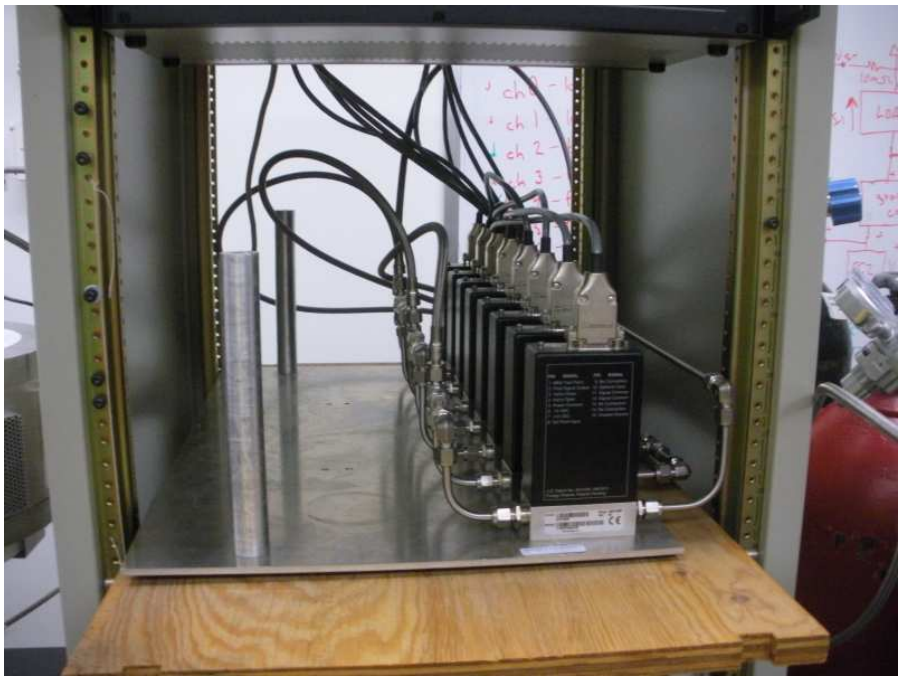


Figure 9-18: A closeup photograph of the mass flow controllers used to control the flow of Oxygen and Hydrogen into the solid-oxide fuel cell ovens.

Figures 9-19 and 9-20 show the power converter and data acquisition (DAQ) system connections. The DAQ connections were buffered and low pass filtered. The array of buffers and low-pass filters built for this purpose is shown on a breadboard in Figure 9-20.

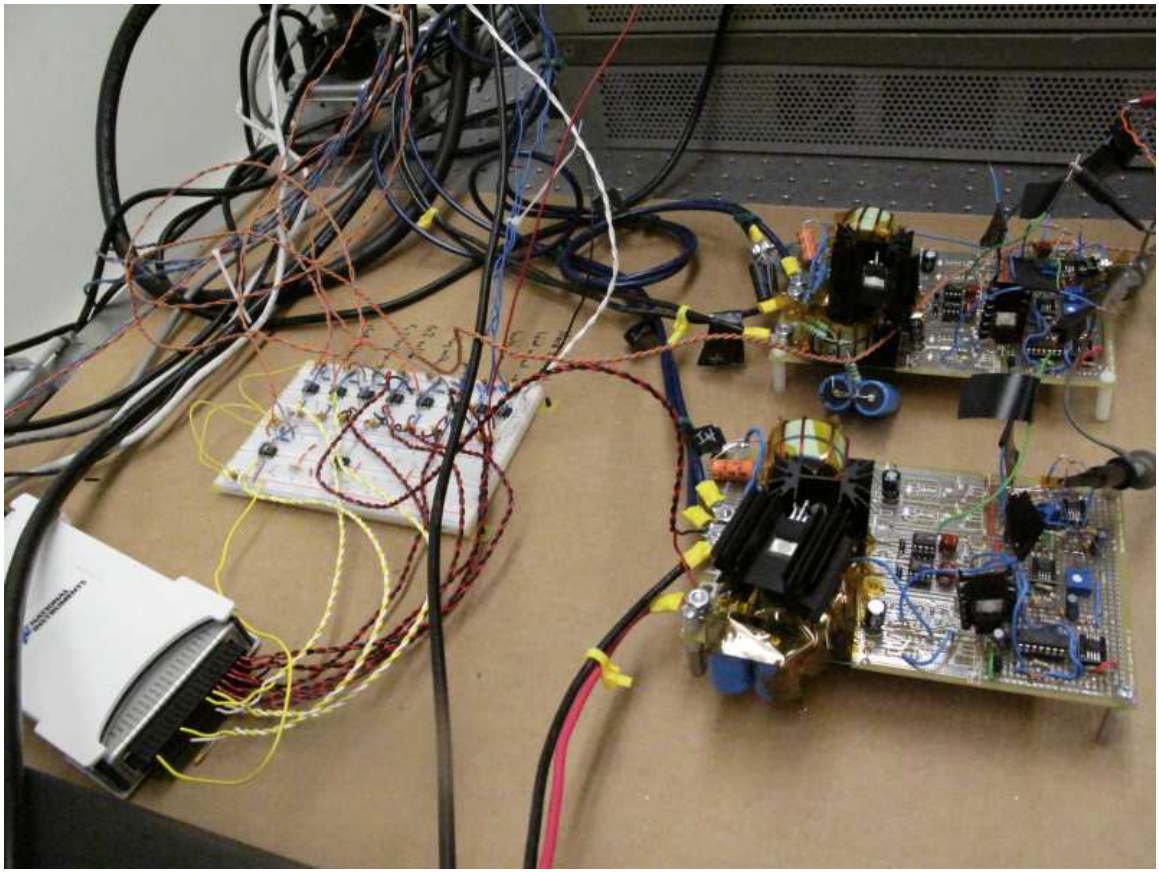


Figure 9-19: A photograph of the two-converter current-voltage regulated power system connected to the data acquisition system in the fuel cell experimental setup.

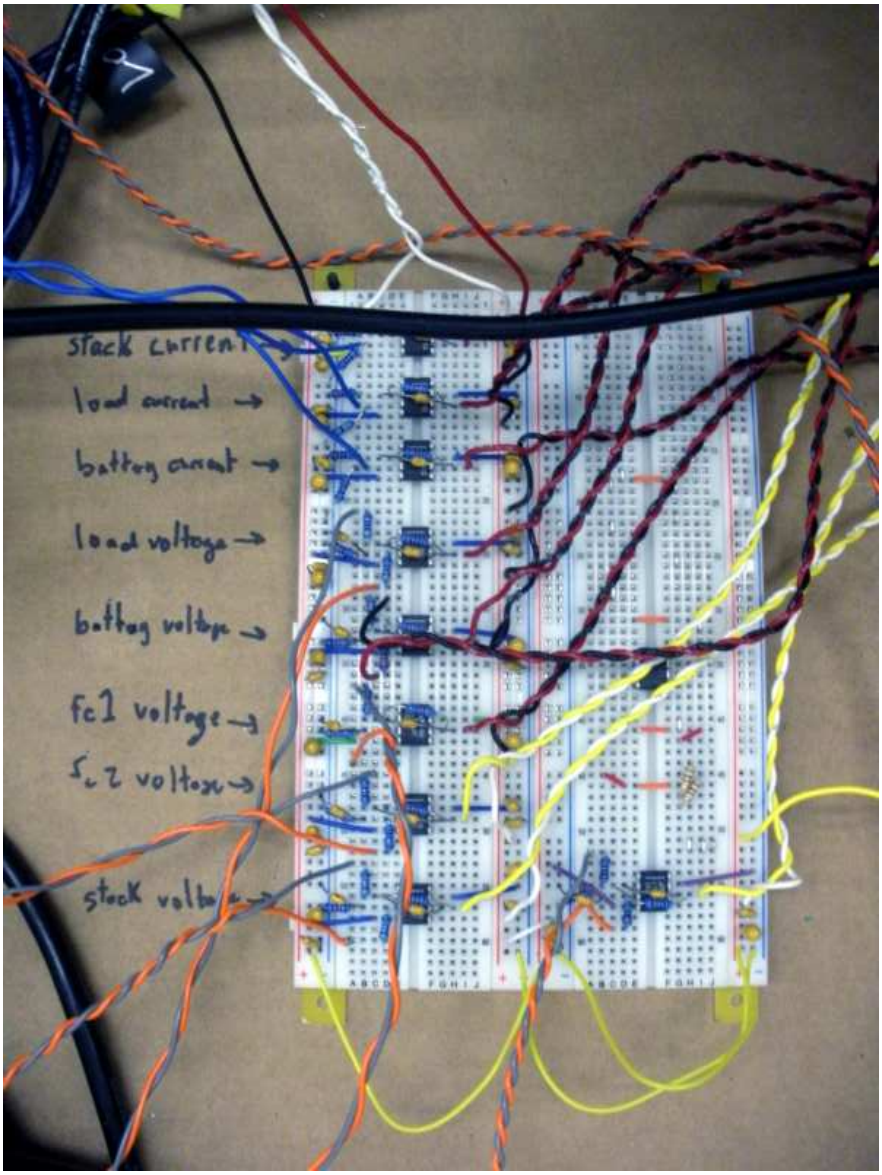


Figure 9-20: A closeup photograph of the data acquisition system buffers and low pass filters in the fuel cell experimental setup.

9.7.1 Reference Simulator

An independent research effort at MSU has led to the successful implementation of a "Fuel Cell Reference Simulator." The reference simulator allows for laboratory tests of a simulated fuel cell stack having only one or two fuel cells. A schematic diagram of the reference simulator in the context of the experimental setup is shown in Figure 9-14.

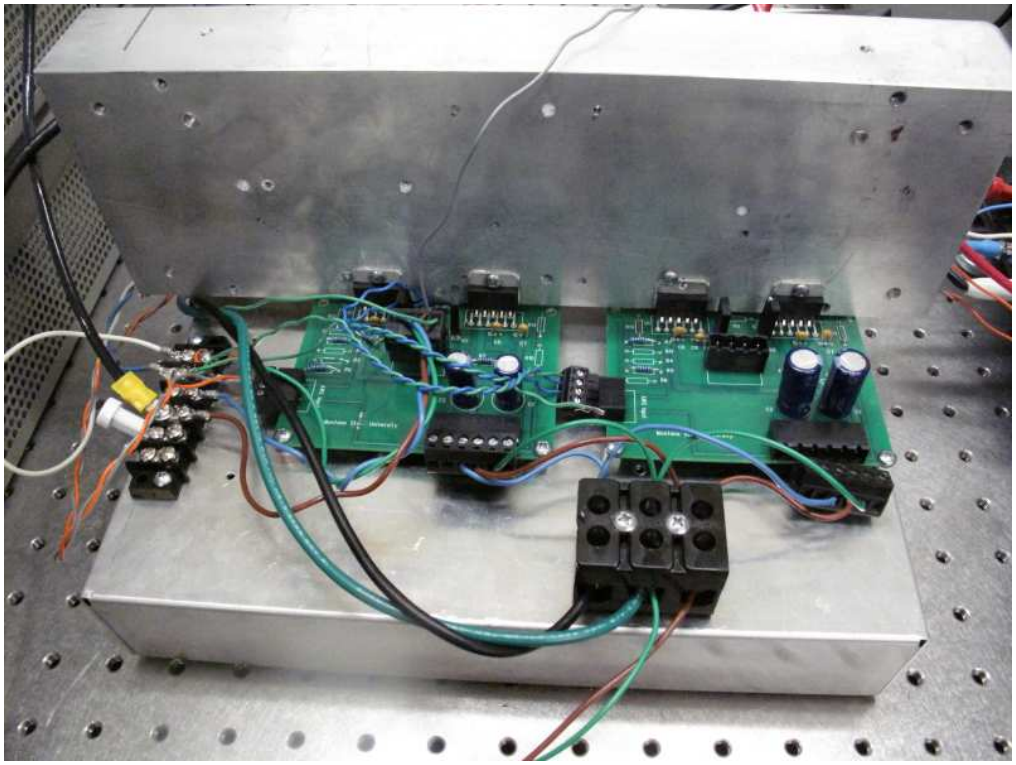


Figure 9-21: A closeup photograph of the reference simulator electronics in the fuel cell experimental setup.

The reference simulator is intended to simulate a series connection (stack) based on the behavior of only one fuel cell. The simulator measures the fuel cell output voltage at V_{fc} and provides a gained and inverted ($-\alpha$) version at the node labeled V_{stack-}. The fuel cell voltage is itself included in the simulated stack voltage because

the total simulated stack voltage, $V_{stack+} - V_{stack-}$, is

$$\begin{aligned} V_{stack} &= V_{fc} - V_{stack-} \\ &= V_{fc} + \alpha V_{fc}. \end{aligned} \tag{9.3}$$

The simulated stack voltage is therefore

$$\boxed{V_{stack} = V_{fc}\,(1+\alpha)}. \tag{9.4}$$

The topology allows the load current to flow through the fuel cell itself. Because all of the fuel cells in a stack would see the same current, the current through the single fuel cell is equivalent to the simulated stack current. Therefore the terminals V_{stack+} and V_{stack-} simulate a stack of $1 + \alpha$ replicas of the fuel cell. Additional high power op-amp gain stages are connected as slave devices to increase the current handling capability of the reference simulator. Note that the reference simulator ground is an intermediate reference that is distinct from the simulated stack reference. The simulated stack reference is generally V_{stack-} and in this case is connected (through the current sense resistor) to the load ground ("load return").

The experimental data presented at the end of this section validates the practical use of the hybrid power system for EIS of the fuel cell. It also validates the operation of the reference simulator itself.

9.8 UAV Flight Plans

Electric flight data for an actual unmanned aerial vehicle was available through a collaboration with the US Air Force. Data showing the total load current and the UAV velocity time domain profiles (flight plans) are shown for three different flights in Figure 9-22. The three different flight plans exhibit some notable and useful features for the run time integral diagnostics experiments. Flight plan 1 exhibits a rapidly and widely varying load current through the flight. Flight plan 2 is similar to flight plan 1 but shows an intermediate landing and takeoff. Flight plan 3 exhibits a slowly varying load current with one distinct abrupt feature near the middle of the flight. Flight plan 3 is particularly useful because it can be used in a simple experiment to determine the extent of the abrupt load transient effects on the EIS measurements.

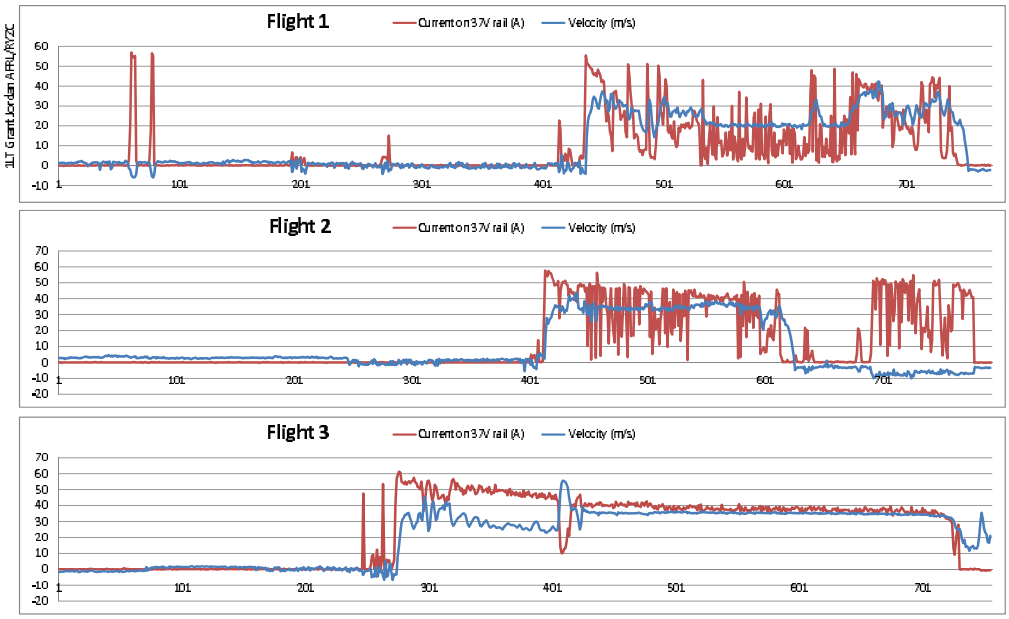


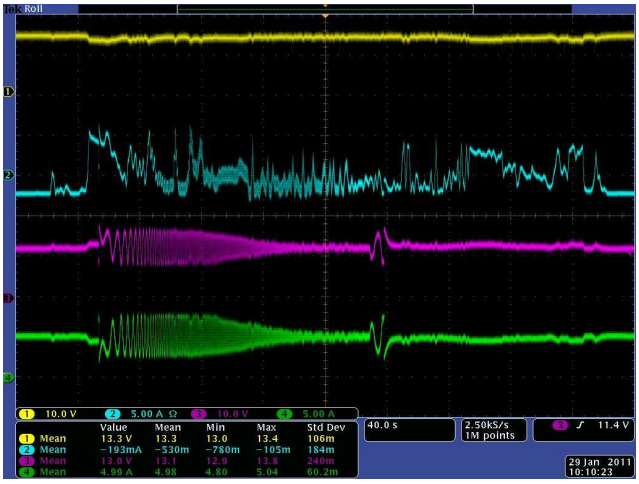
Figure 9-22: Data for three different flight plans made available through a collaboration with the USAF.

The oscilloscope traces in Figure 9-23 show time domain waveforms about 10 minutes long each corresponding to runtime EIS experiments for the three flight plans. The channels in the traces are ch1: Battery voltage, ch2: Battery current, ch3: Fuel cell voltage, ch4: Fuel cell current.

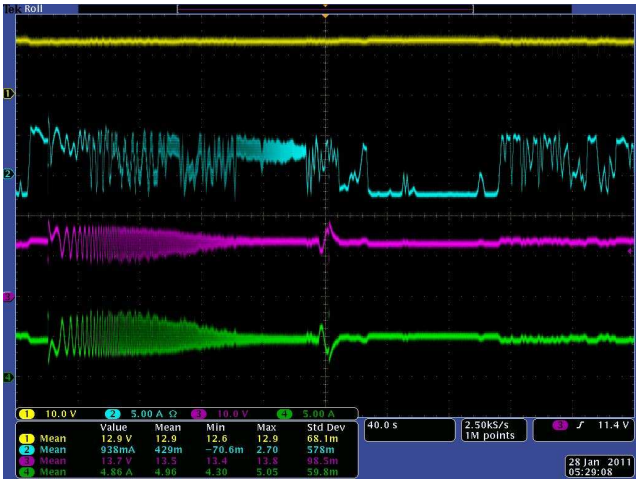
In the oscilloscope traces, the battery current varies widely throughout the flight

plan. When the load current is low, the battery current is actually negative indicating that the battery is being recharged from the fuel cell. The battery voltage varies somewhat due to its internal resistance as the battery current varies with the load. Meanwhile, the fuel cell current (and voltage) are largely fixed at the desired operating point with a superposed EIS signal. The traces clearly show the frequency-swept EIS signal superposed on the fuel cell current and voltage and the battery current. To a lesser extent the EIS signal is visible on the battery current signal.

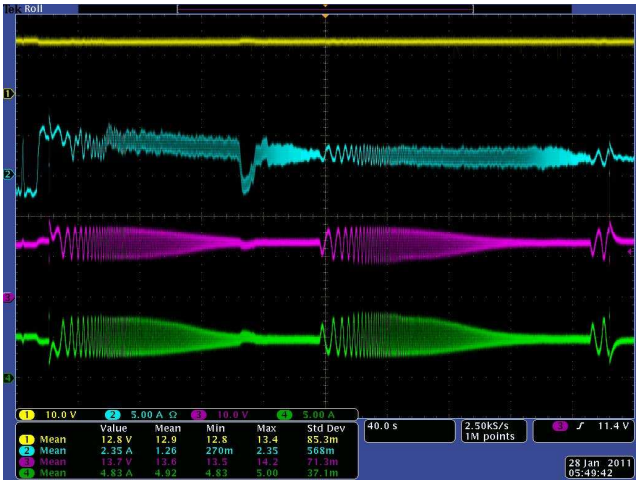
Two EIS sweeps were performed for each iteration of flight plan 3. The two time segments were chosen such that one occurs during a time when the load current is slowly varying while the other includes one abrupt transient in the load current.



(a) Flight Plan 1



(b) Flight Plan 2

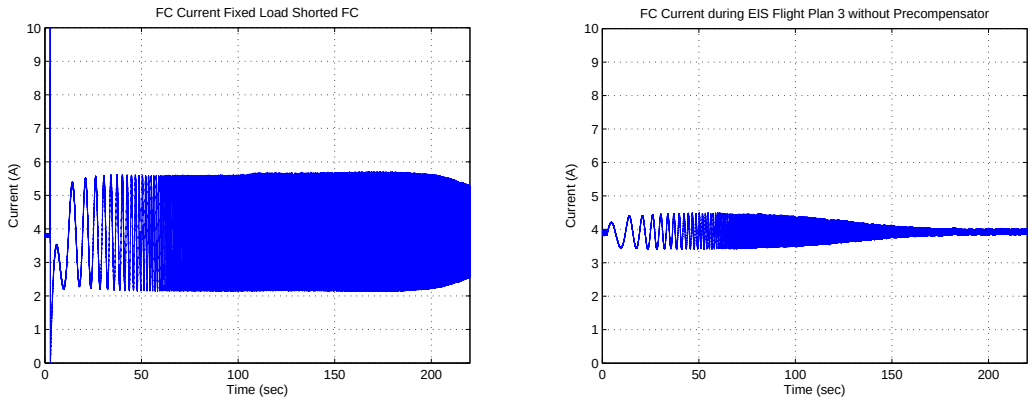


(c) Flight Plan 3

Figure 9-23: Oscilloscope traces showing EIS operation during flight plans: ch1: Battery Voltage ch2: Battery Current ch3: Fuel Cell Voltage ch4: Fuel Cell Current

9.9 Empirically-based Frequency Precompensator

The fuel cell current during EIS sweeps is shown in Figure 9-24 for three different cases. The first plot, in Figure 9-24(a) shows the fuel cell current when the fuel cell in the reference simulator has been shorted. This is an indication of the ideal input voltage source transfer function from the control voltage to the first converter's input current e.g. the bode plot in Figure 9-3(a). The data in Figure 9-24(a) confirms the flatness of the passband shown in the simulated bode plot of Figure 9-3(a). The bandlimiting shown during the high frequency portion of the EIS sweep (near 1 kHz) is due to the first converter's input filter transfer function whose bandwidth is roughly 1.5 kHz as shown in Figure 9-7(a). While this particular data is not well-representative of small-signal behavior, the magnitude response is roughly in agreement with the small-signal transfer function in Figure 9-3(a), given the control signal amplitude.



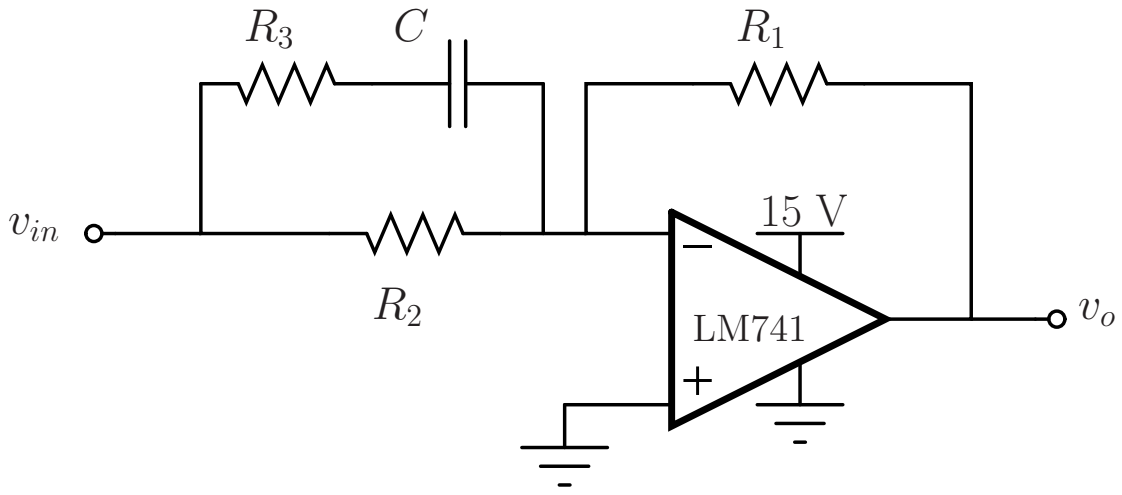
(a) EIS sweep with FC Shorted: 500 mV_{p-p} control signal from EIS5 (no Flight Plan)

(b) Without Precompensator: 200 mV_{p-p} from EIS12 (Flight Plan 3)

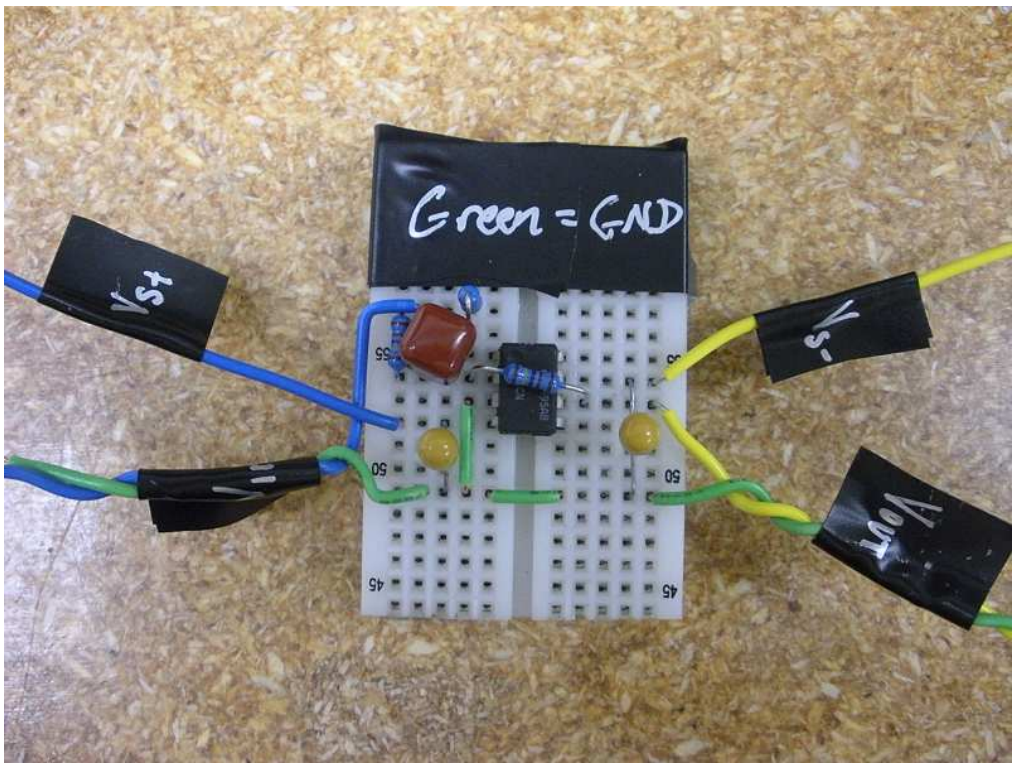
Figure 9-24: FC currents during EIS sweeps 0.1 Hz to 1 kHz showing the need for the frequency precompensator.

During experimentation, we observed the effect of the non-zero fuel cell impedance on the closed loop transfer function from the control voltage, $\hat{v}_{ref1}$ to the fuel cell current, $\hat{i}_{fc}$. An example of this effect is indicated by the data in Figure 9-24(b). Because the fuel cell output impedance is inductive, the excitation current transmission to the fuel cell decreased in magnitude with frequency despite the relatively flat pass-band indicated in the closed-loop transfer function of Figure 9-3(a). This added frequency

dependence constitutes a practical challenge for running frequency-swept EIS experiments particularly if the control signal amplitude is fixed. A fixed amplitude control signal leads to an excitation current that may be too small at high frequency or too large at low frequency. If it is too small, the fuel cell current and voltage perturbations may be below the noise floor of the measurement. If it is too large, the small-signal assumptions collapse. To solve this problem, an empirically based precompensator was constructed to recover the flat pass-band that was initially expected. The precompensator was connected in series with the control signal $v_{ref1,ac}$ in Figure 9-14.



(a) Schematic



(b) Photograph

Figure 9-25: The EIS control signal frequency precompensator constructed based on observations of the inductive fuel cell source impedance effect on the transmission of excitation currents to the fuel cell terminals.

The schematic of the precompensator is shown in Figure 9-25(a). The transfer function of the precompensator is

$$\frac{v_o}{v_{in}} = \frac{R_1}{R_3}\frac{1 + sC(R_2 + R_3)}{1 + sCR_2}. \tag{9.5}$$

Based on the dynamics observed during experimentation the pole and zero were placed at 50 Hz and 10 Hz respectively. The zero-frequency gain, R_1/R_3, was unity so $R_1 = R_3$. The values used for this design were $R_1 = 15$ kΩ, $R_2 = 1$ kΩ, $R_3 = 15$ kΩ, and $C = 1$ μF. Figure 9-26 shows the fuel cell current having added the precompensator. With the precompensator, a fixed amplitude control signal leads to a relatively fixed amplitude excitation current.

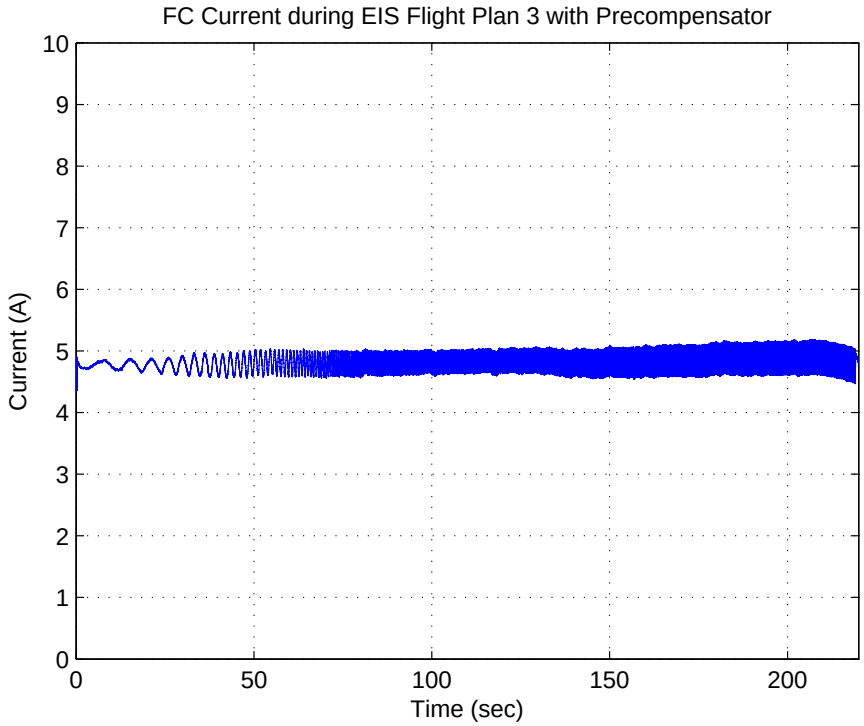


Figure 9-26: With Precompensator: 50 mV$_{p-p}$ from EIS37 (Flight Plan 3)

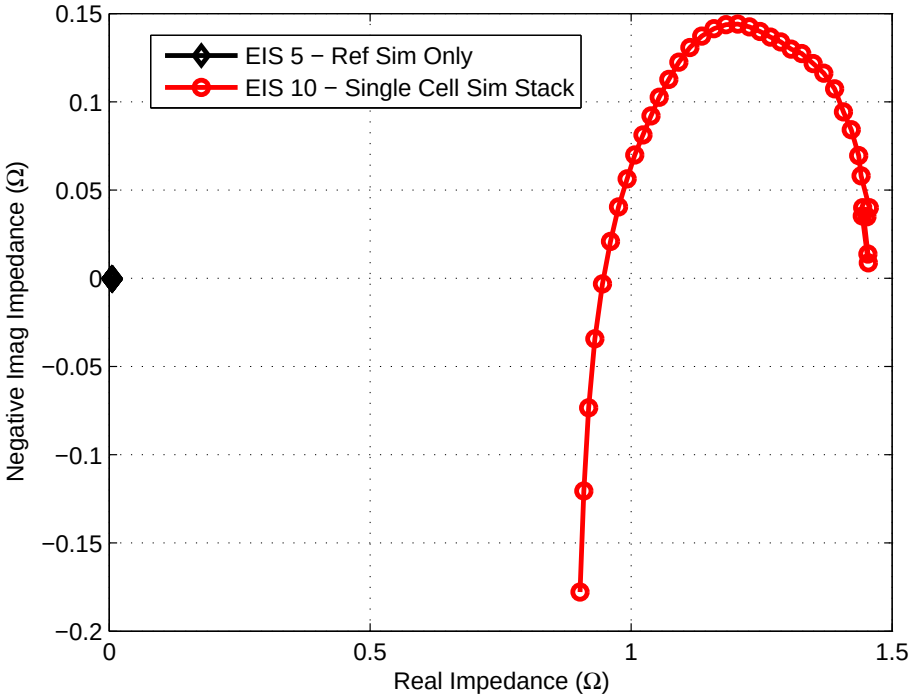
9.10 Fuel Cell Impedance Results

Impedance measurements of the simulated fuel cell stack were taken among various configurations and load profiles. The frequency range of the impedance measurement was 0.1 Hz to 1 kHz. The fuel cell operating point was chosen based on its large signal $I - V$ characteristic. That operating point was a nominal fuel current of $I_{fc} = 4$ A.

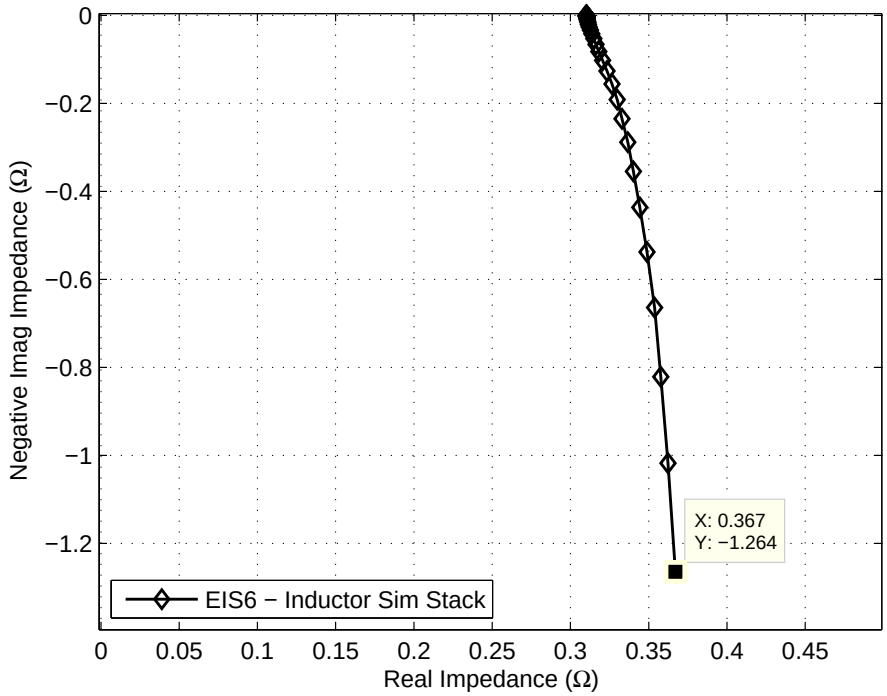
Figure 9-27 shows the results from two control experiments. Figure 9-27(a) shows a comparison of the impedance measured using the reference simulator first with the fuel cell in place and second with the fuel cell shorted. The Nyquist plot indicates that the added impedance from the reference simulator and interconnects is negligible compared to the impedance contributed by the fuel cell.

Figure 9-27(b) shows the impedance measured for a known inductor. The inductor was independently measured to have an inductance of 10.1 μH and a series resistance of 4 mΩ measured at 100 Hz. The data in the plot shows the impedance measured for the inductor with 1.5 μH and 15 mΩ of wire inductance and resistance. The impedance is multiplied by a factor of 20 due to the working operation of the reference simulator. According to Figure 9-27(b), the inductance at the high frequency operating point (893 Hz in this case) was

$$L \approx 1.264 \times \frac{1}{2\pi \times 893\text{Hz}} \times \frac{1}{20} = 11.26\ \mu\text{H}. \tag{9.6}$$



(a) Control Expt 1: EIS with FC compared to EIS with the FC shorted



(b) Control Expt 2: EIS with known inductor

Figure 9-27: Control experiments

Figure 9-28 shows the impedance measured for the simulated fuel cell stack with a fixed load (no flight plan). Also shown is a multiplied impedance measurement for the single fuel cell. The comparison shows that the simulated output closely represents a simulation of a stack of fuel cell replicas.

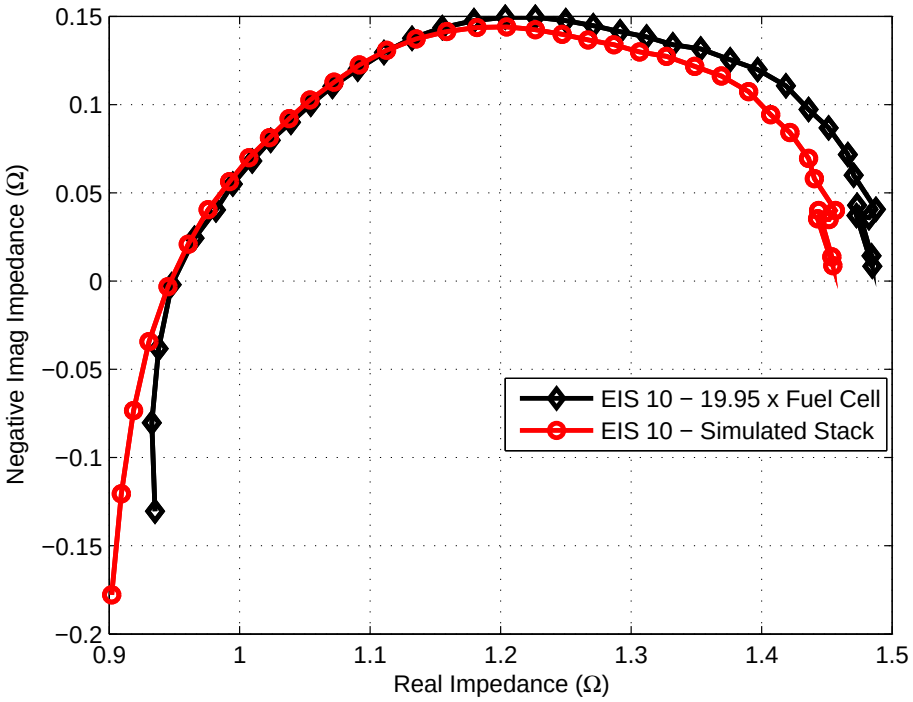


Figure 9-28: EIS with a fixed load (no flight plan), $I_{fc} = 4$ A

Figure 9-29 shows the comparison of impedance measured at the single cell level for the two distinct time segments in flight plan 3 at the same fuel cell operating point. Time segment 1 includes a single abrupt transient in the load while time segment 2 does not. The two impedance measurements are very closely matched suggesting that the effect of abrupt transients in the load current have a small impact on the impedance measurement. This is a natural outcome of the hybrid power system design. Specifically, the current-regulated fuel cell side converter buffers the fuel cell current from load current transients.

Figure 9-30 shows impedance data measured during the three flight plans. In the Nqyuist plots the impedance of the simulated stack is overlayed on a multiplied impedance measured for the single cell. The close matching between the two indicates

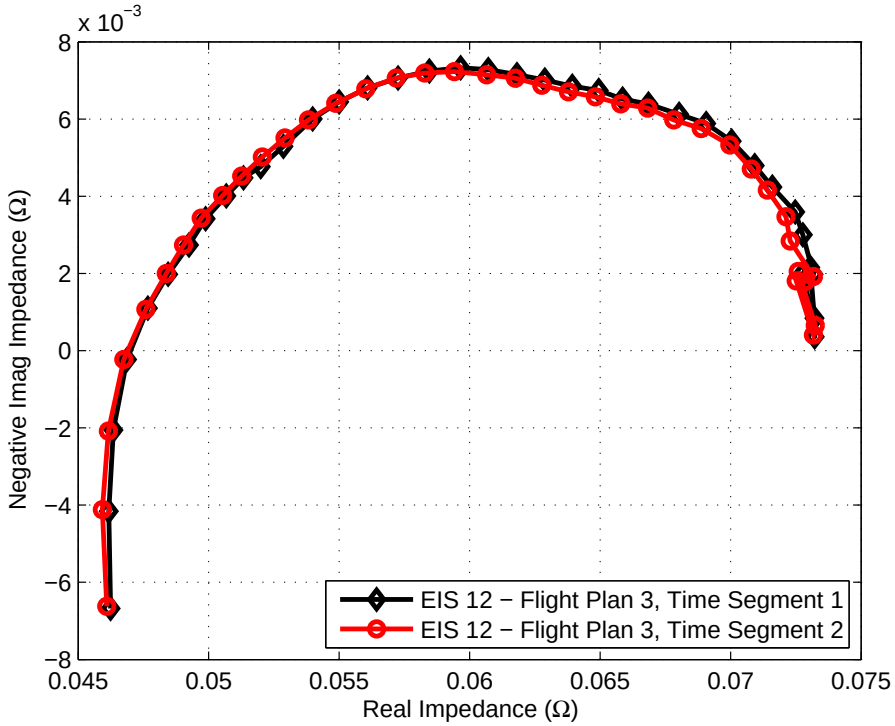
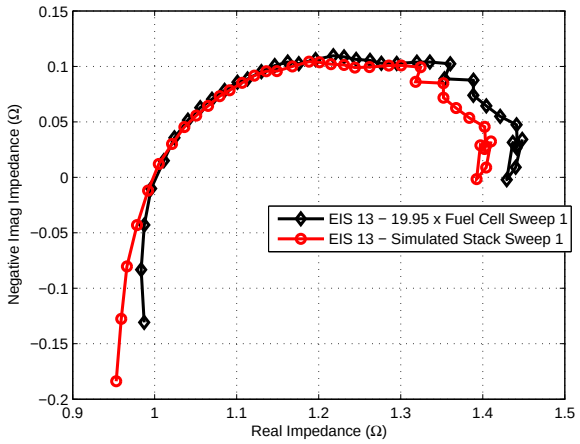


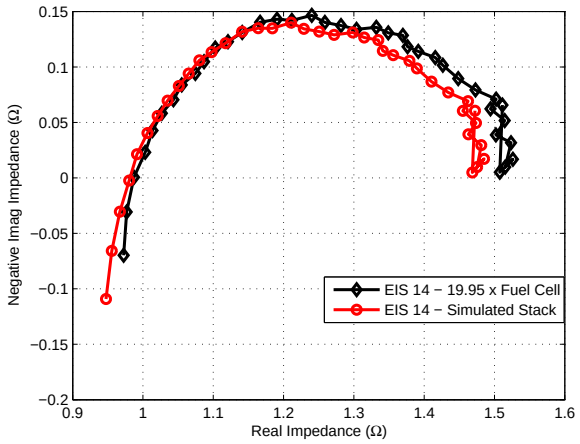
Figure 9-29: Single Cell EIS during Flight Plan 3 for two different time segments, $I_{fc} = 4$ A

that the reference simulator accurately simulates a stack of replica fuel cells. The experiments indicated in the Figure for flight plans 1 and 3 are shown for two slightly different fuel cell operating points. The data in Figure 9-30(a) was taken for $I_{fc} = 4.4$ A while the data in Figure 9-30(c) was taken for $I_{fc} = 4$ A.

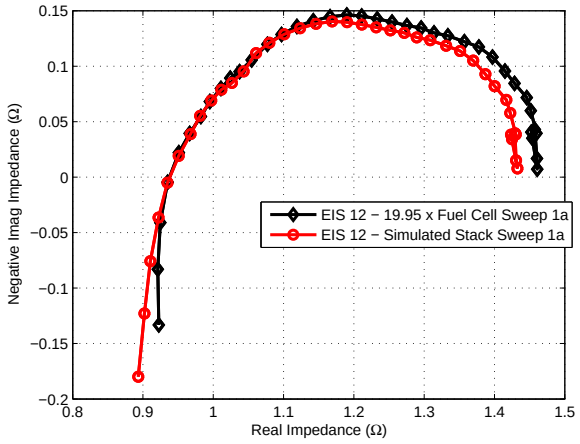
Comparing Figure 9-30(c) to 9-28 indicates good matching between the data taken with a fixed load and data taken during the flight plan. Comparing Figure 9-30(a) to Figure 9-30(c) indicates a decrease in the impedance magnitude at higher fuel cell current.



(a) EIS during Flight Plan 1, $I_{fc} = 4.4$ A



(b) EIS during Flight Plan 2, $I_{fc} = 4.3$ A



(c) EIS during Flight Plan 3, $I_{fc} = 4$ A

Figure 9-30: Nyquist plots showing measured impedances during flight plans.

Figure 9-31 shows a comparison of impedance data for a second fuel cell that was intentionally damaged and then allowed to recover. The cell was degraded for about 11 hours while holding the cell voltage between 50 mV and 30 mV. The fuel cell current was initially 15 A, but by morning had decreased to 14 A. Fuel rates were 260 SCCM H2, 100 SCCM O2. The cell temperature was 750°C.

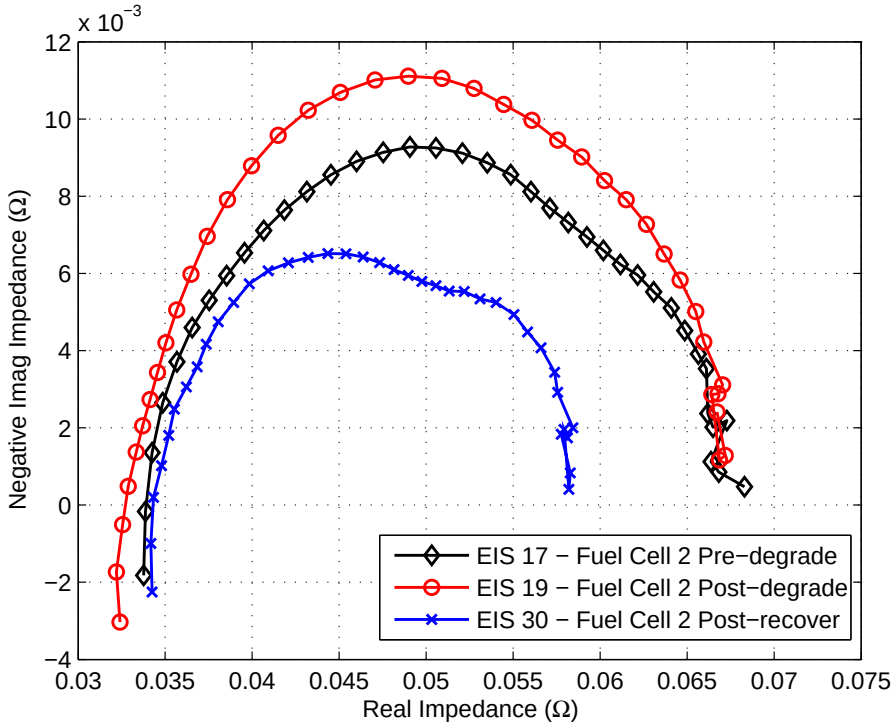


Figure 9-31: Pre-degrade, $I_{fc} = 4.1$ A, degraded $I_{fc} = 4$ A, post-recovery, $I_{fc} = 4$ A

The three plots correspond to pre-degradation, post-degradation, and post-recovery. The data suggest that the capacitive impedance increases when the fuel cell has been damaged and decreases when the fuel cell is recovered. The low-frequency resistance (real-axis intercept) also decreases when the fuel cell is recovered. Additionally, the data suggest that the fuel cell was somewhat unhealthy prior to degradation.

9.10.1 Discussion

The three states of the fuel cell in Figure 9-31 may be related to changes in the physical properties of the cell modeled by the incomplete circuit model shown in

Figure 9-32 taken from reference [15]. Key elements not included in the circuit model are the series inductance leading to the crossing of the real axis in all of the Nyquist plots and additional RC combinations to describe multiple humps in those plots. In the circuit model of Figure 9-32, C is the equivalent capacitance of double-layer charge effect, and $R_{act,cell}$, $R_{ohm,cell}$, and $R_{conc,cell}$ are equivalent resistances of the activation, ohmic and concentration voltage drops. At low currents, when chemical reactions start to take place inside the SOFC, a voltage loss (drop) results due to an activation energy barrier that must be overcome. This is the activation drop [15]. The ohmic resistance of the SOFC consists mainly of the resistance of the electrodes, electrolyte, and the interconnection between cells [15]. The concentration drop is a more subtle effect described in detail in reference [15]. "In a SOFC, the two electrodes are separated by the electrolyte, and two boundary layers are formed, that is, anode-electrolyte layer and electrolyte-cathode layer. Due to the polarization effect, these layers, known as electrochemical double-layer charge effect, can store electrical energy and behave like a super-capacitor [15]."

The low frequency resistance (the real-axis intercept at the right side of the Nyquist plot), would correspond to the series combination of $R_{ohm,cell} + R_{act,cell} + R_{conc,cell}$ because, at low-frequency, the capacitor, C, can be represented as an open-circuit. The high frequency resistance (the real-axis intercept at the left side of the Nyquist plot), would correspond to the resistance, $R_{ohm,cell}$ because, at high frequency, the capacitor, C, can be represented as a short-circuit. Therefore, the decrease in the low-frequency real-axis intercept indicated by the cell impedance post-recovery would correspond to a decrease in the series combination, $R_{ohm,cell}+R_{act,cell}+R_{conc,cell}$. Meanwhile the high-frequency resistance, $R_{ohm,cell}$, has not changed post-recovery, so we may conclude that the series combination $R_{act,cell}+R_{conc,cell}$ has decreased in value.

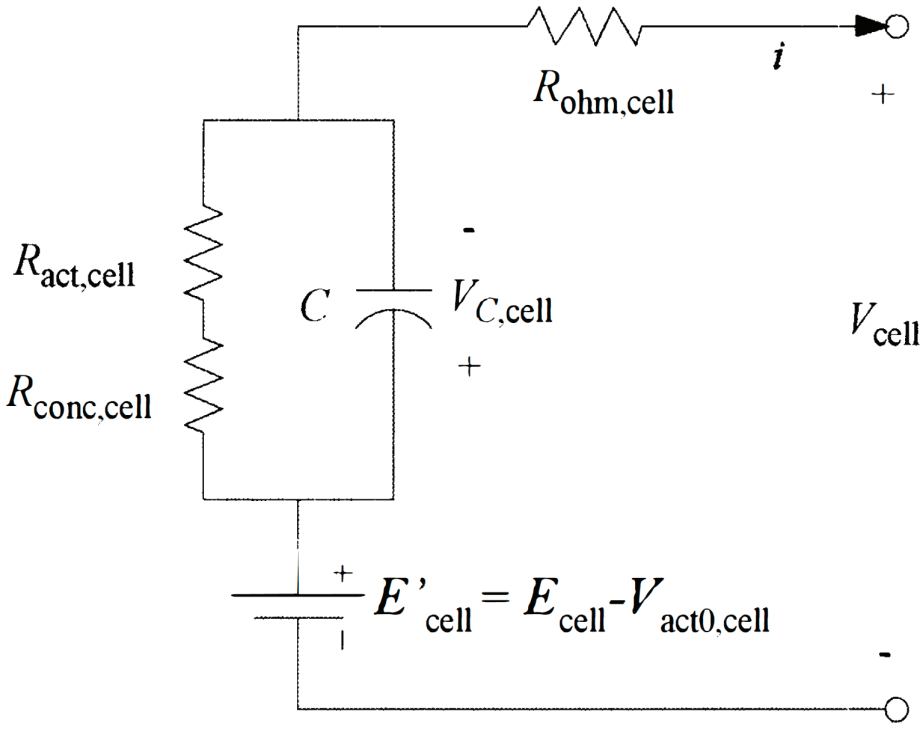


Figure 9-32: A circuit model of a solid-oxide fuel cell taken from reference [15].

Chapter 10

Per-Panel Photovoltaic Energy Extraction with Switched-capacitor Multilevel Output DC/DC Converters

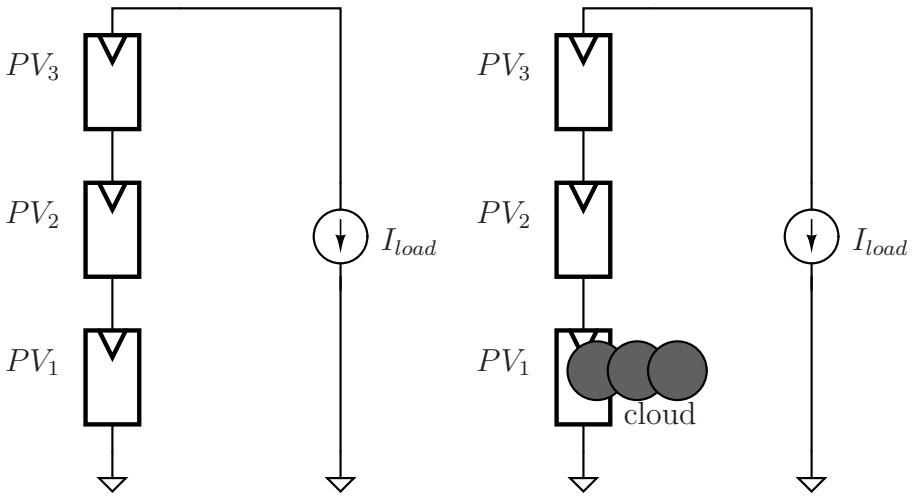
10.1 Introduction

The total installed cost ($/W) and total cost of ownership ($/Wh) have been well-studied as the key metrics controlling the grid penetration of solar power [158–161]. Among the factors impacting installed cost (per Watt) are power converter cost and total (tracking × conversion) efficiency, both of which share strong relations to converter and system complexity. A critical factor impacting the cost of ownership is the lifetime of the power converter (and implied replacement costs). Cost-effective solutions for solar energy extraction should address system cost and complexity, conversion and tracking efficiencies and converter lifetime simultaneously.

The need for suitable tracking efficiency is normally addressed with a maximum power point tracking (MPPT) algorithm embedded in the control of the converter or inverter [24, 162]. In the important grid-tied case, 120 Hz power ripple at the

panel terminals negatively impacts the MPPT function, but this may be addressed by augmenting the source with a large electrolytic capacitor [16, 17, 163–169]. However, the limited lifetime of electrolytic capacitors contends directly with the long-life characteristic of cost-effective solar conversion. To reconcile this, [158] proposed the "ripple port" inverter, which still directly interfaces the PV cell, but directs the 120 Hz ripple power to a transformer coupled ripple port and away from the cell.

There is a growing need to implement per-panel MPPT to contend with varying light levels, temperatures, panel ages, etc. across physically widespread solar arrays [16, 17, 163–169]. Figures 10-1 and 10-2 illustrate the problem.



(a) Simple series string

(b) Simple series string, one panel 75 % shaded

Figure 10-1: Simple series connections of PV panels, unshaded and partially shaded

For a series connection of three identical PV panels as in Figure 10-1(a), a simple string current sweep leads to perfect tracking efficiency, η_p, for a particular value of string current. However, when one panel is shaded as in Figure 10-1(b), the same simple global maximum power point tracking approach can lead to significantly degraded tracking efficiency. Figure 10-2 shows a comparison between the three panel tracking efficiency, defined as the ratio of the power extracted from the string to the maximum achievable extracted power, between the unshaded and partially shaded cases. When on panel is 75% shaded (its maximum power is one-fourth that of the other panels), the string tracking efficiency with this simple global maximum power

tracking scheme is reduced to less than 40%.

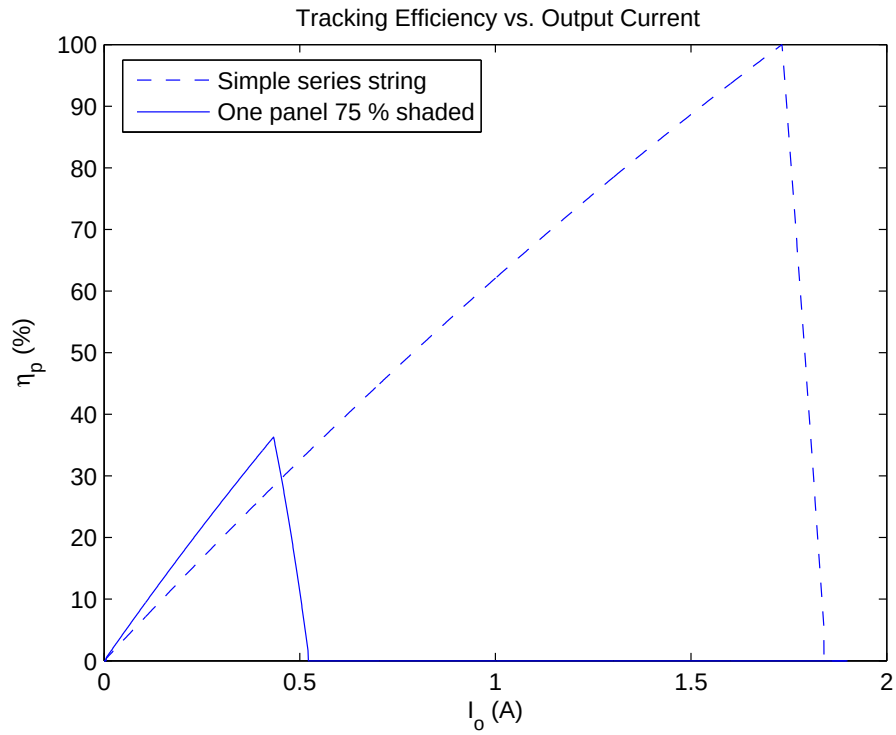


Figure 10-2: 3 panel system tracking efficiencies showing the effect of partial shading on a series string with an oversimplified global maximum power tracking approach.

The solution to the partial shading problem is per-panel MPPT. A series connection of PV panels becomes a series connection of converters processing power from their respective panels. A simplified block diagram illustrating this concept is shown in Figure 10-3.

There are advantages of a DC/DC module integrated converter (MIC) + central DC/AC approach over a DC/AC MIC approach. These include the availability of a single DC bus for an entire array and intermediate power ripple filtering, as well as added degrees of freedom for MPPT control [16, 17, 170]. With per-panel MPPT, global tracking efficiency can be significantly improved over simple series or parallel connections of those panels (see Section 10.2.4), but the installation of per-panel converters impacts the important cost metrics above. Converter lifetime and replacement costs become even more critical with per-panel conversion.

Many inductor-based converters and inverters have been proposed as module inte-

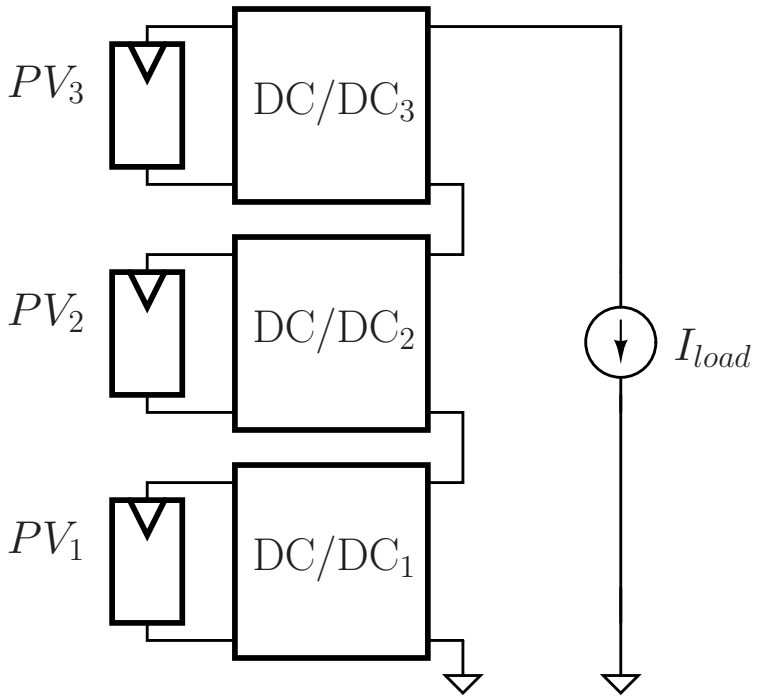


Figure 10-3: A series connection of PV panels becomes a series connection of converters processing power from their respective panels.

grated converter (MIC) topologies, but they require magnetic components to be either purchased per-panel or to be integrated into the converter IC [16,17,163–165]. Multilevel converters have been proposed as per-panel DC/AC converters, but they suffer from either 120 Hz power ripple at the panel terminals or the need for cost-prohibitive and / or electrolytic energy storage [166–169].

10.1.1 System Overview

The system level approach in this thesis is illustrated by the DC linearized circuit model in Figure 10-4. This system shares some key features with other systems employing DC/DC MICs and a central inverter but differs in at least one key way [16]. The DC/DC MICs typically operate with local autonomous MPPT control. In the system proposed here, the responsibility of MPPT is shared among the DC/DC modules and the central inverter. As a result, the required complexity of the DC/DC MICs is simplified. Significantly, the system can be implemented with switched-capacitor multilevel DC/DC converters and a central ripple-port inverter. Per-panel

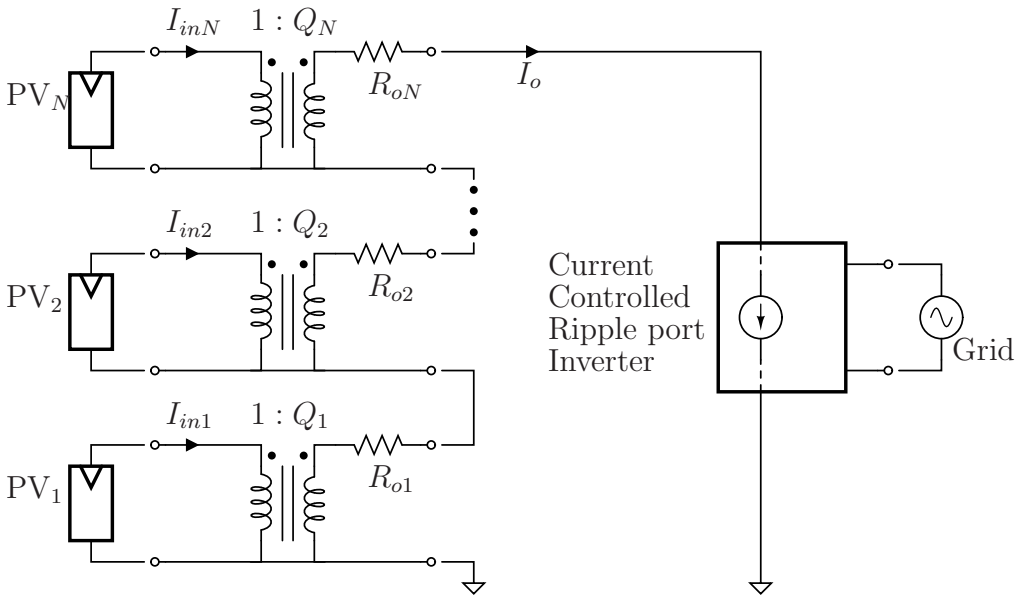


Figure 10-4: A DC linearized model with an N-panel PV string illustrates the system-level approach. The ideal transformers model the function of the DC/DC MICs.

magnetics are eliminated as are electrolytic capacitors if desired. Any magnetics that are required for the ripple port inverter need only be purchased once per string. The DC/DC module conversion ratios are selectable, but discrete. A central question that is addressed in this work concerns the tracking efficiency that is possible with this system.

10.1.2 Switched-capacitor Benefits

Switched-capacitor converters achieve current and voltage conversion without magnetic energy storage. Figure 10-5 shows the cost and volume per energy storage (μJ) for a sample of discrete capacitors and inductors suitable for power applications. These data imply *a-priori* expected cost and volume benefits of switched-capacitor converters when compared to inductor-based converters. A detailed discussion can be found in [171].

Having eliminated magnetic energy storage, discrete implementations can benefit from the higher energy density and lower specific cost of capacitive energy storage. There is also a potential to achieve higher levels of integration. Benefits of integration include reduced parasitic inductances leading to reduced switching loss as well as the

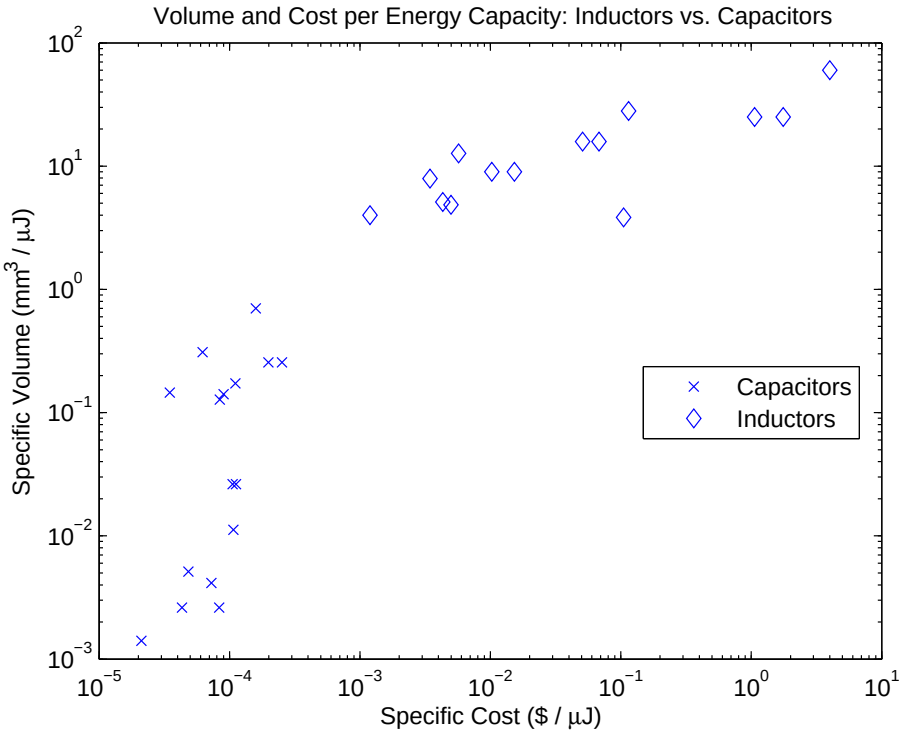


Figure 10-5: Specific cost and volume: Discrete inductors (10 μH- 1 mH/100 mA-1 A) and capacitors (Ceramic and Film 1-10 μF/10-100 V) sampled from Digikey. Energy was calculated as $\frac{1}{2}CV^2$ or $\frac{1}{2}LI^2$ for maximum rated voltages and currents.

cost benefits yielded by batch fabrication techniques for integrated circuits and co-packaged systems [172].

10.1.3 Total Efficiency

Total efficiency is central to the design and evaluation of the systems in this work. Here we define total efficiency, η, as the product of tracking efficiency, η_p, and conversion efficiency, η_c:

$$\boxed{\eta = \eta_p \times \eta_c}. \tag{10.1}$$

Figure 10-6 depicts a sample of reported tracking and conversion efficiencies in MPPT algorithms and DC/DC MICs respectively. The two ranges are multiplied yielding a third range corresponding to total efficiency, η.

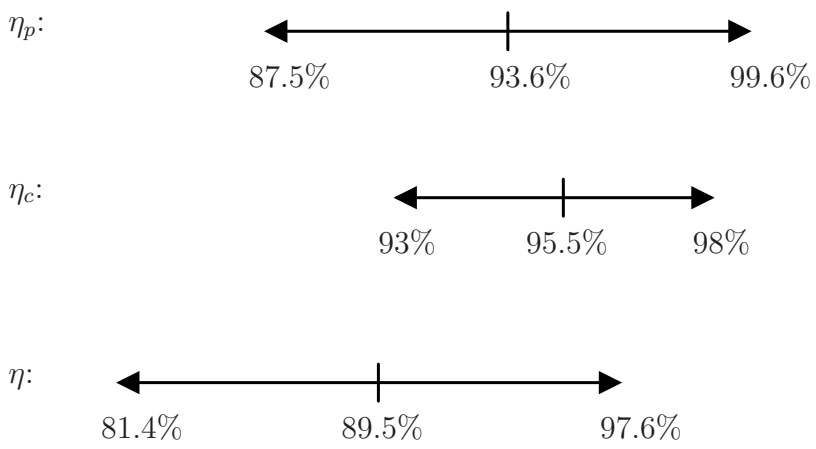


Figure 10-6: A literature survey of total energy extraction efficiency, DC/DC MICs: [16–23] and MPPT algorithms: [23–28]

10.2 Maximum Power Point Tracking

Maximum power point tracking in the system of Figure 10-4 is simplified by the input current control of the central inverter and the series connection of the MICs. The selectable conversion ratios, Q_i, allow the DC/DC modules to track local MPP's as the string current varies. The central inverter tracks the global MPP by adjusting its input current.

The run-time global MPPT can be implemented by exploiting time-scale separation. Here, we take the local MPPT control to operate fast, and the global MPPT control to operate relatively slowly. Specifically, on the time-scale of local MPPT control, the string current, I_o, may be taken to be static or "quasi-static." Because the maximum power point of each panel is defined by a unique maximum power current, $I_{mp,i}$, the quasi-static string current naturally decouples MPPT control among the modules.

10.2.1 PV Model

Before discussing system performance further, we establish a model of the photovoltaic panel and its parameters. The circuit model used here (Figure 10-7) is common in the literature, e.g. [170]. Given the parameters quoted in a typical datasheet, open-

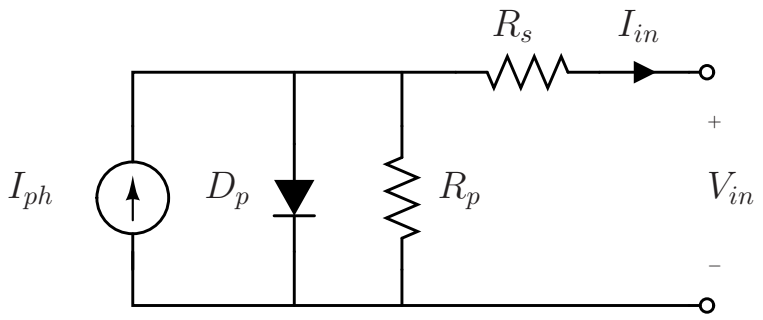


Figure 10-7: PV circuit model

circuit voltage, V_{oc}, and short-circuit current, I_{sc}, and the maximum power voltage and current, V_{mp}, and I_{mp}, analysis of the circuit in Figure 10-7 yields the following results. The circuit model diode forward voltage is

$$V_{dp} = V_{oc} \tag{10.2}$$

and the resistive elements are, respectively,

$$R_s = \frac{V_{oc} - V_{mp}}{I_{mp}} \tag{10.3}$$

$$R_p = \frac{I_{sc}R_s - V_{oc}}{I_{mp} - I_{sc}}, \tag{10.4}$$

while the photovoltaic current is

$$I_{ph} = I_{mp} + \frac{V_{dp}}{R_p}. \tag{10.5}$$

In Figure 10-7, when $I_{in} < I_{mp}$, the diode, D_p, is forward-biased and it is reverse-biased otherwise. The resulting panel voltages are

$$\begin{aligned} V_{in} &= V_{dp} - I_{in}R_s, & I_{in} &< I_{mp} \\ V_{in} &= R_pI_{ph} - (R_s + R_p)I_{in}, & I_{in} &\geq I_{mp} \end{aligned} \tag{10.6}$$

and the panel power is simply

$$P_{in} = I_{in}V_{in}. \tag{10.7}$$

For simplicity, the rest of this work assumes the following nominal datasheet values adapted from a Mitsubishi PV-MF170EB4 [173]. The maximum power (MP) current and voltage are

$$I_{mp} = 6.93 \text{ A}$$
$$V_{mp} = 24.6 \text{ V}.$$

The short-circuit current is

$$I_{sc} = 7.38 \text{ A},$$

and the open-circuit voltage is

$$V_{oc} = 29 \text{ V}. \tag{10.8}$$

These nominal values correspond to the following PV circuit model parameters: $V_{dp} = 29$ V, $R_s = 0.635\ \Omega$, $R_p = 54\ \Omega$, and $I_{ph} = 7.47$ A. The Mitsubishi PV-MF170EB4 includes 50 cells connected in series and it is 1.58 m x 0.8 m in dimension.

10.2.2 Local Maximum Power Point Tracking

Local MPPT control consists of matching the string current, to the panel's own $I_{mp,i}$'s. From Figure 10-4, the i^{th} panel current is

$$I_{in,i} = Q_i I_o. \tag{10.9}$$

Given a quasi-static string current, I_o, the modules each choose a Q_i to maximize their panel power. This maximization step can be performed a number of ways. For instance, the modules may estimate their $I_{mp,i}$'s via short-circuit current measurements. References [174–178] discuss MPPT control by this method. A perturb and observe step may be necessary for good accuracy following the initial I_{mp} guess. In our system, having discrete conversion ratios, a maximum of two additional observations

should be required to determine the actual optimal conversion ratio.

In the simulations that follow, the local algorithm for choosing conversion ratios was implemented as follows. Given $I_{mp,i}$ either by the short-circuit method described above or otherwise, the modules attempt to minimize the error $|I_{in,i} - I_{mp,i}|$. This minimization is constrained according to the nonlinear behavior of the PV indicated in Figure 10-7. Combining equations (10.6) and (10.7), the panel power for the i^{th} panel can be written:

$$\begin{aligned} P_{in,i} &= I_{in,i}V_{dp,i} - I_{in,i}^2 R_{s,i}, && I_{in,i} < I_{mp,i} \\ P_{in,i} &= I_{in,i}R_{p,i}I_{ph,i} - (R_{s,i} + R_{p,i})I_{in,i}^2, && I_{in,i} \geq I_{mp,i}. \end{aligned} \tag{10.10}$$

Taking the derivative of (10.10) with respect to I_{in} yields

$$\begin{aligned} \frac{\partial P_{in,i}}{\partial I_{in,i}} &= V_{dp,i} - 2I_{in,i}R_{s,i}, && I_{in,i} < I_{mp,i} \\ \frac{\partial P_{in,i}}{\partial I_{in,i}} &= R_{p,i}I_{ph,i} - 2(R_{s,i} + R_{p,i})I_{in,i}, && I_{in,i} \geq I_{mp,i}. \end{aligned} \tag{10.11}$$

The term, $-2(R_{s,i} + R_{p,i})I_{in,i}$, in the derivative typically leads to a steep decrease in panel power for $I_{in} \geq I_{mp}$. Absolute errors $|I_{in,i} - I_{mp,i}|$ impact the panel power less for $I_{in,i} < I_{mp,i}$. Accordingly, the algorithm adopted in this work attempts to minimize the error $|I_{in,i} - I_{mp,i}|$ with the following order of preference:

1. $I_{in,i} = I_{mp,i}$
2. $I_{in,i} < I_{mp,i}$
3. $I_{in,i} > I_{mp,i}$.

In the examples presented here, the DC/DC modules each continuously attempt to match the string current to their own MP currents according to the above algorithm. Generally, the modules can choose from a set of integral conversion ratios [0,1...Q_{max}]. The Q = 0 module configuration is important for good average tracking efficiency. It is equivalent to the pass-through mode discussed in reference [16] and represents the

option for a panel to "sit out" when its maximum power is so low that including it in the string would have a negative impact on the global MPP.

10.2.3 Global Maximum Power Point Tracking

The string inverter can track the global MPP by adjusting its input current. Figure 10-8 depicts an example of the tracking efficiency achieved as I_o is swept, while the DC/DC modules adjust their conversion ratios. For this example, and for the rest of this section, tracking efficiency is considered in an otherwise lossless system ($\eta_c = 100\%$). The I_o sweeps, like the one depicted in Figure 10-8, may be performed

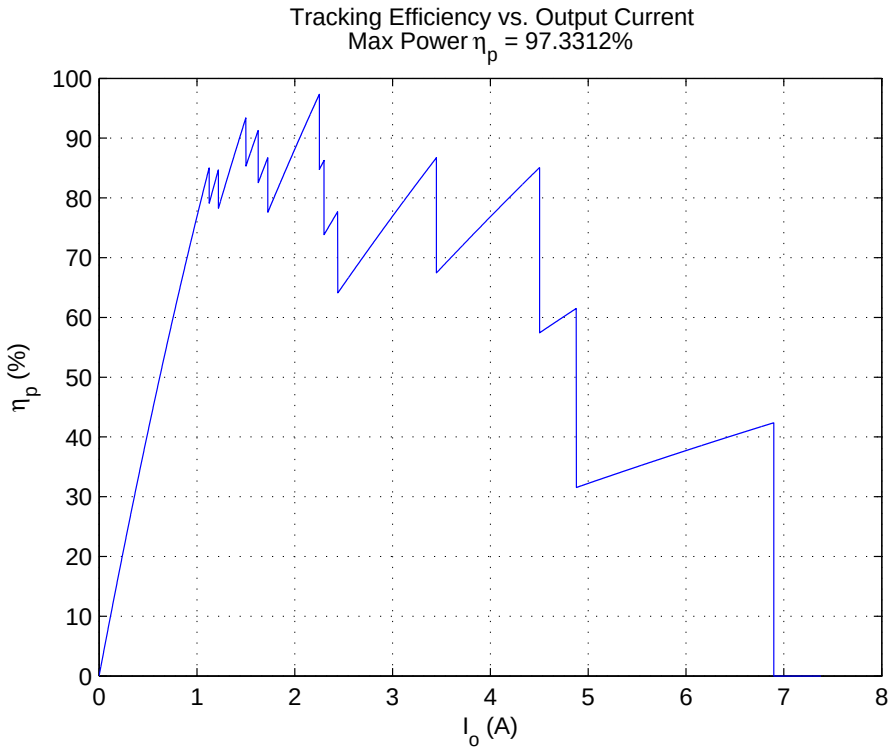


Figure 10-8: A single I_o sweep: 3 panels, Q_{avail} = [0,1,2,3,4], $I_{mp,vec}$ = [6.898, 4.503, 4.878] A, $\Delta I_o = 1$ mA

on a scheduled basis. Alternatively, I_o may be varied continuously according to a particular runtime MPPT algorithm. Section 10.7 presents a simulation of a likely input current-controlled inverter.

Figure 10-9 shows one cycle of a hypothetical timing diagram that may be used to quantify the tradeoffs in implementing the global MPPT algorithm. The timing

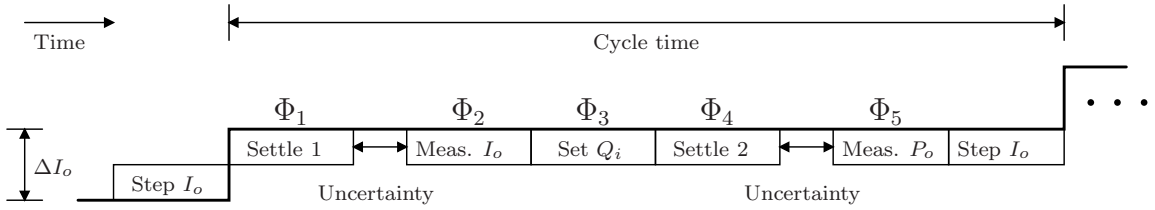


Figure 10-9: A hypothetical MPPT timing diagram for one inverter input current step.

diagram consists of six distinct phases. Additionally, because the local and global MPPT are asynchronous, i.e. the local MPPT algorithm phases 2-5 are cycled continuously at each panel, there is timing uncertainty equal to the total amount of time occupied by phases 2 through 5. In other words, the central inverter must wait a total of twice the time that it takes a panel to cycle through phases 2 through 5 in order to guarantee that all of those phases have been completed. The distinct phases are indicated by the following operations:

Φ_1 [Settle 1]: Larger of inverter input current settling time following inverter command step and module current settling time following a step in load current

Φ_2 [Meas. I_o]: Modules measure panel I_o

Φ_3 [Set Q_i]: Modules select and set conversion ratios, Q_i

Φ_4 [Settle 2]: Larger of inverter input current settling time following DC bus voltage step and module current settling time following a change in conversion ratio

Φ_5 [Meas. P_o]: Inverter measures its own input power

Here we have assumed that the first choice of conversion ratio is sufficient and that no perturb and observe step is required. The validity of this assumption depends on the accuracy of the short-circuit current maximum power point estimation method. We also assume that the short-circuit current measurement takes place approximately once per inverter input current sweep, not continuously. This assumption is important because the short-circuit current measurement disrupts the module currents and therefore necessitates a period of settling time following that measurement.

From the timing diagram, there will be tradeoffs among inverter input current step resolution, sweep width, and sweep time. Instantaneous tracking efficiency will improve with inverter input current step resolution, but time average tracking efficiency will suffer as the inverter input current sweep time increases. If the sweep is to take place on a scheduled basis, e.g. every 5 seconds, then the sweep time represents a down-time. The fractional down-time decreases as the sweep time decreases and the period between sweeps increases. However, tracking efficiency may also suffer if the period between sweeps becomes long enough that transient phenomena in lighting levels, temperature changes etc. are not sufficiently captured.

Here we consider an example. Simulated prototype data in Sections 10.4 and 10.7 will indicate that the cycle time will be dominated by the settling time in the module currents following a step change in the inverter input current or a change in conversion ratio. Here we assume that a change in conversion ratio takes place rarely during the sweep so the cycle time is dominated by the former.

The simulated data in Section 10.4 indicates a settling time of 250 μs in the module currents following a step change in the load current. The corresponding cycle time will be approximately 500 μs due to the uncertainty consideration. This cycle time accommodates 2000 inverter current steps per second. If we assume that the inverter will sweep from zero to the short-circuit current of the panels (7.38 A in this example) in 20 mA steps, then a full sweep will take approximately 185 ms. For a sweep period of 5 seconds, this sweep time represents a fractional downtime of 3.7 %. The sweep resolution in this example is the same as the sweep resolution used in the statistical performance evaluations later in this chapter.

10.2.4 Statistical Performance Evaluation

A statistical performance evaluation method was adopted to account for variations in panel MPP's. The relevant MATLAB® code can be found in Appendix C. Monte Carlo simulations were performed by allowing MATLAB® to choose random (normalized) $I_{mp,i}$'s for each panel. For each simulation, the string current, I_o, was swept as in Figure 10-8 and the maximum efficiencies (tracking, converter, and total) were

recorded. Repeating this many times and averaging the results yielded a prediction of average performance. An example output plot is shown in Figure 10-10. The

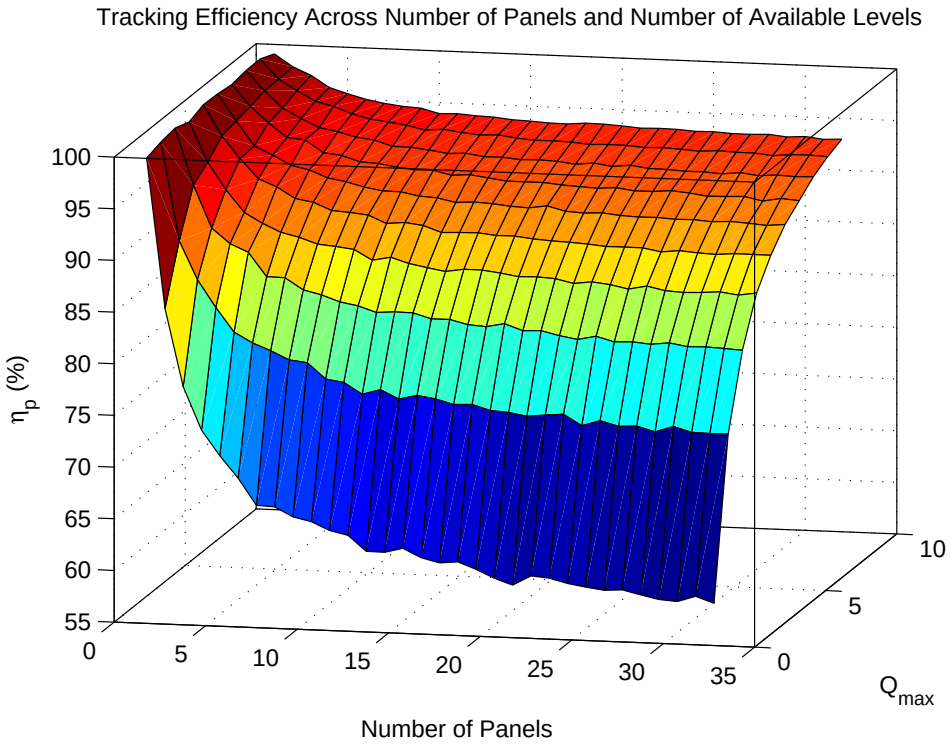


Figure 10-10: Monte Carlo performance prediction: $Q_{avail} = [0 : 1 : Q_{max}]$, Monte Carlo Length = 200, $I_{o,sweep} = [0.01 : 0.02 : 6.93]$ A

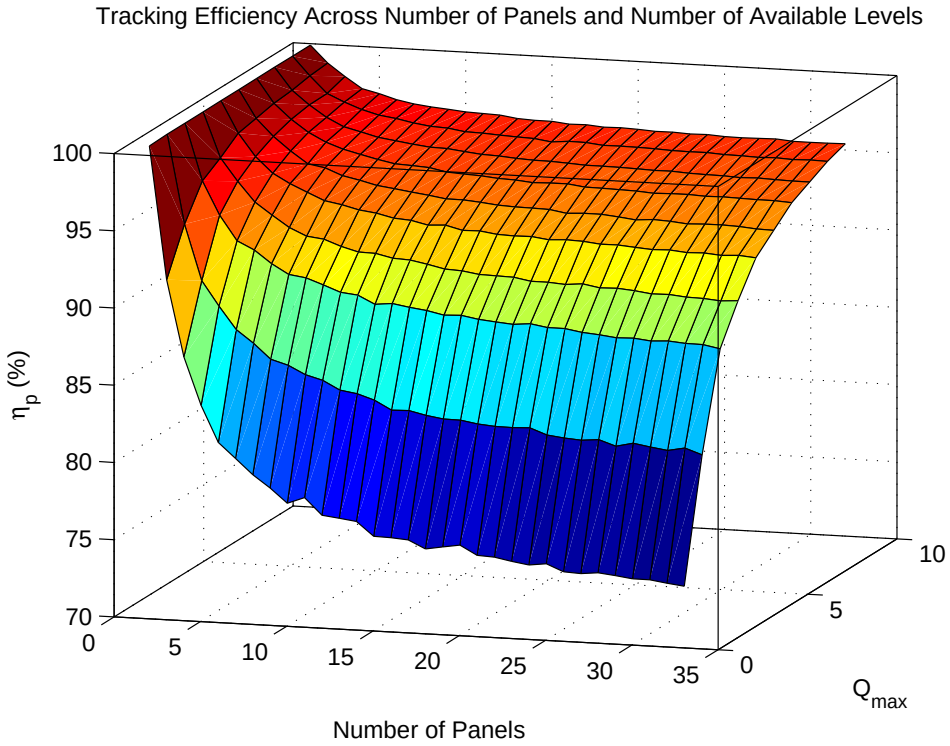
plot in Figure 10-10 reveals that tracking efficiency can be very high for only a few panels. As panels are added, η_p diminishes to a limited extent. The local MPPT algorithm implemented impacts this behavior significantly. For instance, if the order of preferences listed in Section 10.2.2 is reversed, the tracking efficiency diminishes steadily as panels are added rather than flattening as it does in Figure 10-10. The Monte Carlo simulation results also show how average tracking efficiency improves as the number of available levels increases. The tracking efficiency predicted for a 3-panel, 5-level system is approximately 90%. Increasing the number of available levels to 8 increases the predicted tracking efficiency to 95%.

Finally, it should be noted that the $Q_{max} = 1$ case (i.e. $Q_{avail} = [0, 1]$) is somewhat representative of a simple series string of panels with bypass diodes. The statistical data predict roughly 65% average tracking efficiency while a 5-level MIC would im-

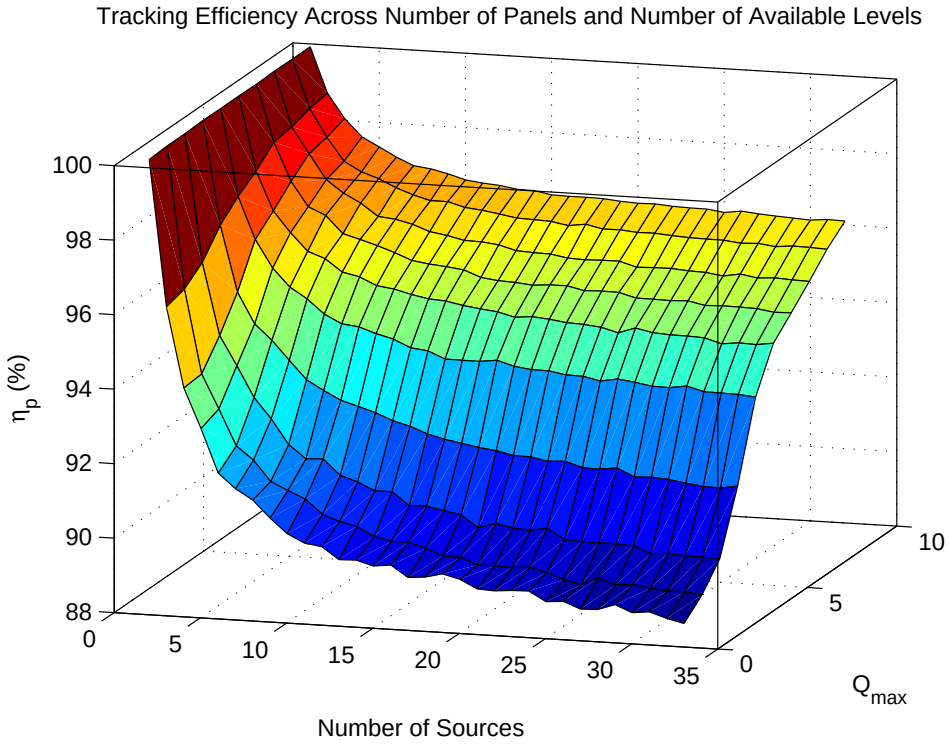
prove that efficiency to roughly 90%

10.2.5 Effect of spatial panel separation

In the above example, the panels are assumed to have a random and uncorrelated distribution of MPP's. Intuitively, this model becomes inappropriate as panels become closely spaced. To model the effect of statistical correlation between MPP's for panels arranged in a non-infinite area, the randomly assigned panel MPP's can be constrained to a fraction of the full range. The simulation above was repeated having forced the MPP's to lie within 50% and 25% of the full range for each Monte Carlo iteration. The results show universally higher average tracking efficiencies. For instance, the tracking efficiency predicted for a 3-panel, 5-level system is approximately 95.5% and for a 3-panel, 8-level system, 97.4% with a distribution compression of 50%. The simulated results are shown in Figure 10-11.



(a) Compressed Distribution (50%)



(b) Compressed Distribution (25%)

Figure 10-11: Monte Carlo simulation: $Q_{avail} = [0 : 1 : Q_{max}]$, Monte Carlo Length = 200, $I_{o,sweep} = [0.01 : 0.02 : 6.93]$ A, Compressed Distributions

10.3 Switched-capacitor Implementation

One particular realization of the switched-capacitor MICs in Figure 10-4 is the Marx Multilevel converter. By forming series and parallel combinations of the the input source and the switched-capacitors, the 5-level Marx converter shown in Figure 10-12 can achieve conversion ratios $Q_{avail} = [0, 1, 2, 3, 4]$.

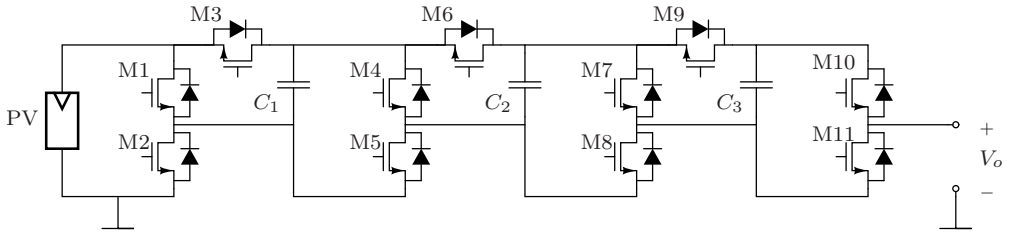


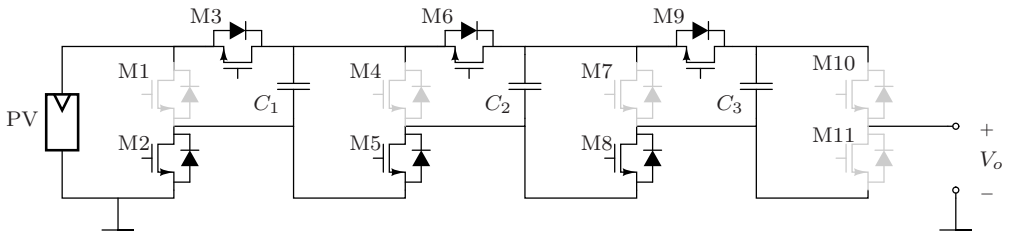
Figure 10-12: A 5-Level Marx converter

10.3.1 Efficient Switching Patterns

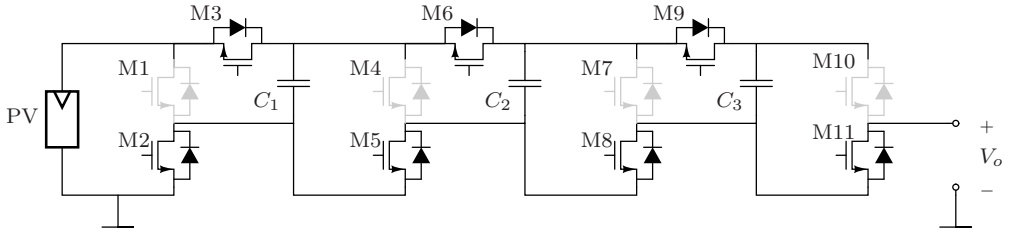
Switching cycles consist of a recharge phase, ϕ_1, and an output phase, ϕ_2. During ϕ_1, the switched-capacitors are disconnected from the load and charged in parallel with the source. During ϕ_2, one of several series-parallel configurations of the switched-capacitors and input source is chosen to achieve the desired conversion ratio. Many redundant switching configurations are possible (see Appendix D). The switching configurations shown in Figure 10-13 were chosen for the 5-level Marx to minimize the conduction losses that will be quantified shortly. Generally, the switching configurations were chosen to minimize capacitor droop and the number of switches in the output current path, both of which lead to loss and load regulation. Rules of thumb to minimize capacitor droop include 1) utilize the input source to drive the output during ϕ_2 when possible and 2) utilize all of the switched-capacitors when driving the output, e.g. parallel-connect redundant capacitors when possible. Note that the short-circuit current measurement needed for run-time local maximum power point tracking may be implemented by temporarily activating devices M_1 and M_2. The body diode of device M_3 should normally be reverse-biased during the short-circuit current measurement because the panel voltage should fall below the instantaneous

capacitor voltage.

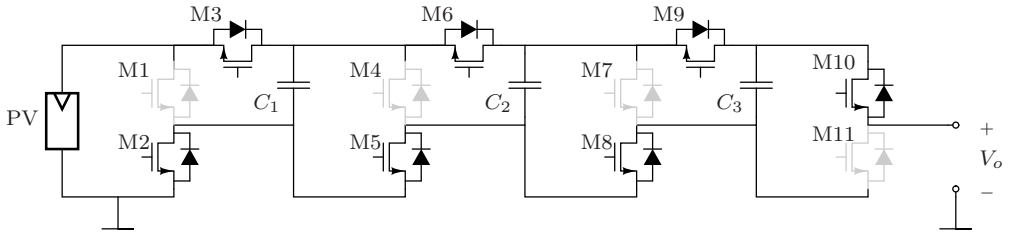
Switched-capacitor circuits can achieve very high conversion efficiency by minimizing the instantaneous current flow through their effective output resistance, $R_{out,i}$. In a DC/DC switched-capacitor circuit, the output is slowly-varying on the time-scale of one switching period. These facts guide us to particular modes of operation. In particular, efficient operation can be achieved when the same output phase (ϕ_2) configuration is repeated every cycle. In contrast, modulation of the ϕ_2 configuration on a per cycle basis, e.g. to achieve intermediate conversion ratios, would be ill-advised as it would lead to continuously varying open circuit converter voltages resulting in high instantaneous currents (high AC rms currents) through $R_{out,i}$. This observation leads directly to the constraint that the Marx Multilevel converter can (efficiently) achieve a discrete set of conversion ratios.



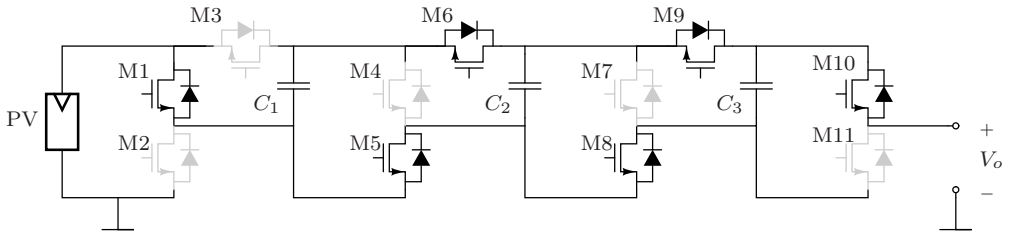
(a) Recharge



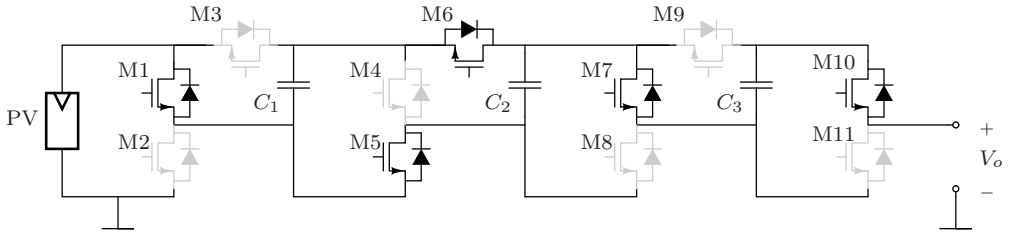
(b) $Q = 0$



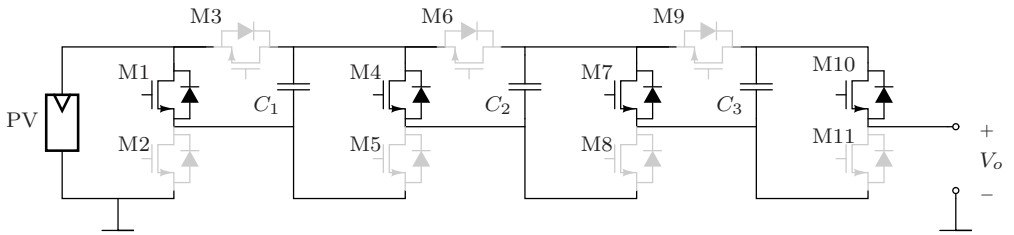
(c) $Q = 1$



(d) $Q = 2$



(e) $Q = 3$



(f) $Q = 4$

Figure 10-13: Switching configurations

10.3.2 Linear Modeling

A linear modeling approach was adapted from the work in [30]. This linear modeling effort yielded quantitative support for the linear circuit models shown in Figure 10-4 including the output resistances, $R_{o,i}$ which represent both loss and load regulation in the switched-capacitor circuits [30].

According to [30], loss and load regulation mechanisms can be differentiated among two switching speed limiting cases. In the slow-switching-limit (SSL), the switched-capacitors fully equilibrate yielding impulsive capacitor currents. In the fast-switching-limit (FSL), the switched-capacitors maintain fixed voltages while capacitor currents during each switching state are constant [30]. The two switching

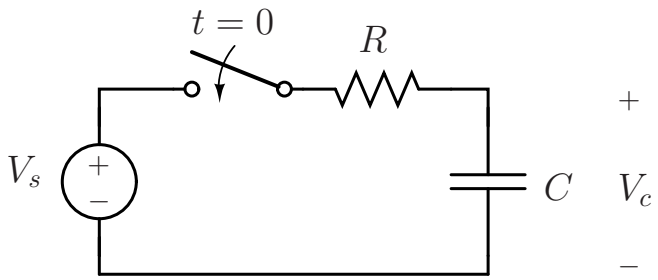


Figure 10-14: The canonical circuit for studying the fundamental loss associated with charging a capacitor.

speed limits can be understood by considering the classic capacitor charging loss problem depicted in Figure 10-14. The total energy lost in charging the capacitor is the time-integral of $I_C(t)^2R$:

$$E_{tot} = -\frac{(V_s - V_C(0))^2}{2R} RC \left(e^{-2t/RC}\right)\Big|_0^t. \tag{10.12}$$

In the SSL, the exponential term is allowed to collapse to -1 and the energy lost becomes

$$E_{tot,SSL} = \frac{1}{2} C \Delta V_C^2, \tag{10.13}$$

independent of R, and in agreement with the classical result. In the FSL, (10.12) can be viewed near $t = 0$ with the Taylor series approximation to the exponential term.

This leads to

$$E_{tot,FSL}(t) = \frac{(V_s - V_C(0))^2 t}{R}, \tag{10.14}$$

i.e. the loss we would expect for two fixed voltages connected across the resistor. Reference [30] shows how these two loss mechanisms yield asymptotic limits to the output resistance with proportionalities

$$R_{SSL} \propto \frac{1}{C f_{sw}} \tag{10.15}$$

and

$$R_{FSL} \propto R_{ds,on}. \tag{10.16}$$

The method developed in [30] for computing the multipliers to quantify R_{SSL} and R_{FSL} was adapted to the Marx Multilevel converter here. Example computations of the effective output resistances can be found in Appendix D. The results are summarized in Tables 10.1 and 10.2 for Marx converters having between two and eight available levels. Note that the multipliers in the tables need to be computed for each conversion ratio (switching pattern) for each number of available levels (topology). Also note that R_{FSL} depends on the duty ratio between ϕ_1 and ϕ_2, which was taken as $D = 0.5$ (the optimum based on Appendix D) for all switching patterns here. Given the asymptotic limits, the actual output resistance for any combination of topology, C, f_{sw}, and $R_{ds,on}$ is generally

$$\boxed{R_{out} \approx \max(R_{FSL}, R_{SSL})} \tag{10.17}$$

and the conduction loss per module is simply

$$P_{rloss} = I_o^2 R_{out}. \tag{10.18}$$

Table 10.1: R_{SSL} Multipliers: $(\times 1/Cf_{sw})$

Levels Available:	2	3	4	5	6	7	8
Q = 0	0	0	0	0	0	0	0
Q = 1	0	0	0	0	0	0	0
Q = 2	–	1	1/2	1/3	1/4	1/5	1
Q = 3	–	–	2	3/2	1	5/6	2/3
Q = 4	–	–	–	3	5/2	2	3/2
Q = 5	–	–	–	–	4	7/2	3
Q = 6	–	–	–	–	–	5	9/2
Q = 7	–	–	–	–	–	–	6

Table 10.2: R_{FSL} Multipliers: $(\times R_{ds,on})$

Levels Available:	2	3	4	5	6	7	8
Q = 0	2	4	6	8	10	12	14
Q = 1	2	4	6	8	10	12	14
Q = 2	–	8	10	12.4	8.2	17.6	32.4
Q = 3	–	–	26	24	38	48.4	50.8
Q = 4	–	–	–	64	90	100	100
Q = 5	–	–	–	–	130	180	206
Q = 6	–	–	–	–	–	232	307
Q = 7	–	–	–	–	–	–	378

10.3.3 Switching Loss

The linearized model above captures loss due to output current conduction. Switching loss is a loss mechanism not explicitly contained in the linearized circuit model of Figure 10-4. The switching loss for any active switch (one that changes state between the two switching phases) can be quantified by considering the circuit shown in Figure 10-15. All MOSFETs in the Marx converter reside in at least one loop consisting only

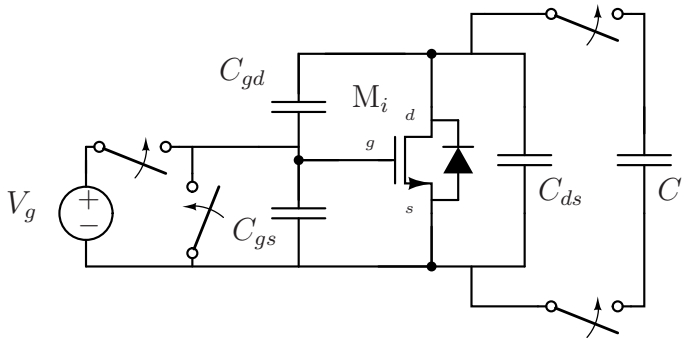


Figure 10-15: Switching loss evaluation in the Marx converter for active MOSFETs

of one or two other MOSFETs and a switched-capacitor. In the Marx converter, the switched-capacitor, C, in Figure 10-15 will nominally exhibit a voltage equal to the

panel voltage, V_{in}, because it is recharged to that potential each cycle. The total switching loss was estimated in terms of typical data sheet values using [179] for N active devices as

$$P_{swloss} = N\left(Q_g V_g + \frac{1}{2}Q_{oss}|V_{in}| + Q_{rr}|V_{in}|\right) f_{sw}. \tag{10.19}$$

Examining the switching patterns shown in Figure 10-13, one can extract the following pattern generalizing the number of active switches according to conversion ratio:

$$N = 1, \qquad Q = 0 \tag{10.20}$$

$$N = 3Q - 2, \qquad Q > 0. \tag{10.21}$$

10.3.4 Inherent Features

Inherent to the topology of the Marx converter are a few interesting features that may add significant value to a solar power array. As mentioned previously, the Marx converter has a natural pass-through feature, replicating the function of bypass diodes and also the pass-through mode presented in [16].

The ability to disconnect each module from the load may be beneficial when implementing safety disconnect features. Reference [180] discusses the need for a disconnect in the event of a fire to prevent electrocution hazards that would otherwise result from the high voltage string output. This disconnect feature may also be particularly beneficial in implementing an anti-islanding mode. A good discussion of anti-islanding control and solutions for solar power systems can be found in [181].

The run-time local MPPT algorithm described above can be designed to automatically prevent under-voltage conditions at the panel output. Because the DC/DC modules continuously choose Q_i to closely match $I_{in,i}$ to $I_{mp,i}$, they automatically adjust to over-current conditions, choosing $Q_i = 0$ in the limiting case. This feature is advantageous when the local control circuitry is powered by the panel itself.

10.3.5 Gate Drive

In general, some or all of the MOSFETs in switched-capacitor multilevel output converters may require a gate drive with a continuous floating gate drive voltage because, the converter itself may not guarantee a periodic charging path to recharge a bootstrap capacitor. In the Marx converter with the switching patterns shown in Figure 10-13, these devices are M3, M6, M9, M10. A level shift circuit is also required to translate ground-referenced logic signals to the gate drive output. The recommended topology (not necessarily the specific parts), adapted from [29], is shown in Figure 10-16.

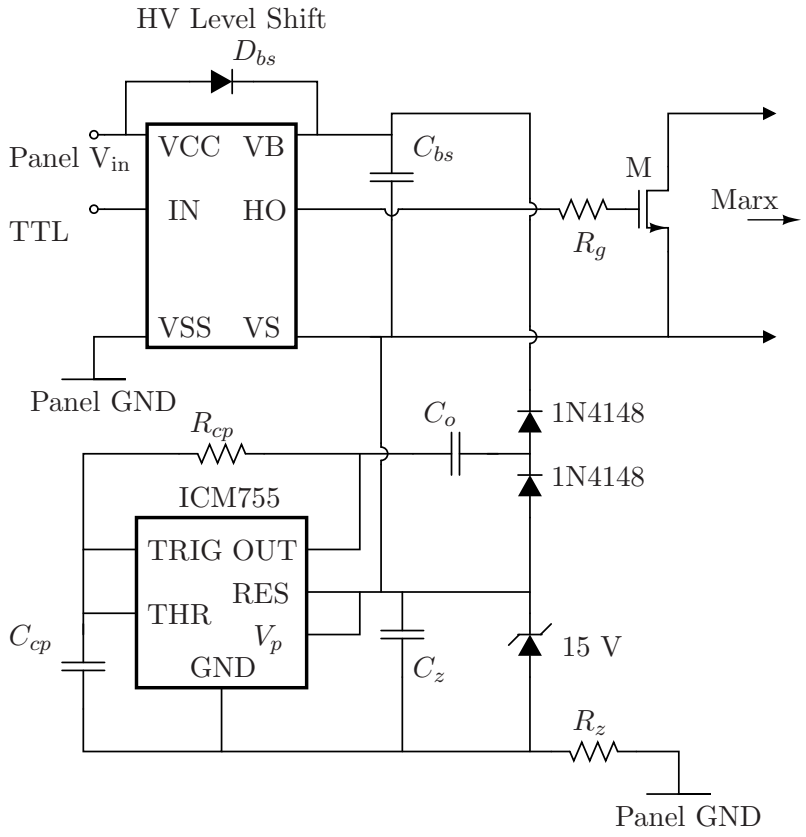


Figure 10-16: The recommended gate drive adapted from IR AN-978 [29].

The 555 timer IC, 1N4148 diodes and floating capacitor form a charge pump circuit. The resistor between the 555 timer GND and Panel GND and the 15 V zener, R_z, allows the timer IC to float 15 V below the source of the driven MOSFET. The low power version of the 555 timer IC (ICM755) is needed in this circuit to

achieve low power dissipation in the part itself and to achieve sufficient quiescent current despite the resistor to ground. The charge pump drives the V_B node to twice its supply voltage referenced to its own floating GND leading to a 15 V floating drive referenced to the MOSFET source. This voltage can be adjusted by choosing the voltage of the Zener diode. The "HV Level Shift" could be a commercial high side driver IC such as the IR2125. However, the high voltage rating of such a part would be under-utilized for a typical implementation of the system in this work. Therefore, a more cost-effective gate drive would include a custom level shift circuit.

10.3.6 Non-integral Level Selections

So far, we have considered only switched-capacitor multilevel converters having integral, boosting sets of conversion ratios. There are many switched-capacitor topologies that can achieve rational and bucking conversion ratios as well. Such a topology choice may be beneficial when considering upper bounds on DC bus voltages or other practical issues. A more thorough investigation will be the subject of future work.

10.4 Simulated Prototype

A 3-panel 510 W system was designed and simulated in SPICE and in MATLAB®. Among the key topological considerations for implementing a practical Marx DC/DC MIC is the need for a power diode in series with the output of each module. This diode is required to block current from conducting backwards through the body diode of the upper MOSFET in the output stage during ϕ_1. In order to alleviate any need to synchronize switching action among modules, a local output non-electrolytic capacitor was placed across each module to create a local DC bus. Figure 10-17 shows the addition of the output diode, D_o, and capacitor, C_o, to a 5-level Marx converter.

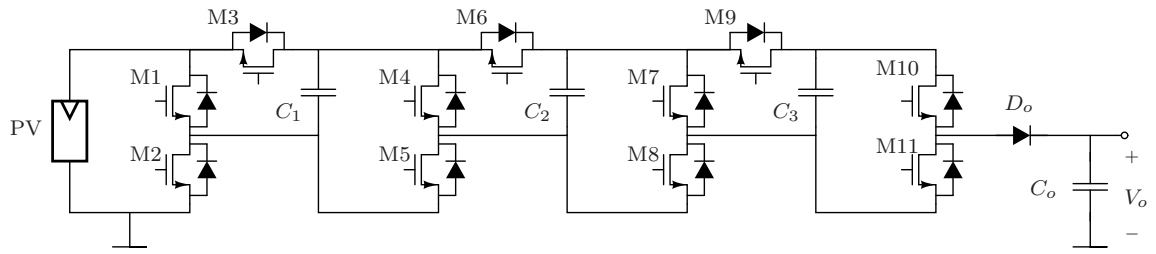


Figure 10-17: A 5-Level Marx converter having the added output diode and capacitor.

10.4.1 Number of Levels

The number of levels was chosen using the same Monte Carlo prediction methods described in Section 10.2.4. Having enumerated loss mechanisms, total efficiency was used to determine performance. To choose an appropriate number of levels, an unoptimized but lossy system was simulated using nominal circuit parameters and MOSFET device characteristics. The predicted performance is plotted in Figure 10-18. The data show diminishing returns in total efficiency beyond 5 levels. Therefore a 5-level Marx converter was chosen as the MIC.

10.4.2 MOSFET

Because all of the MOSFETs in the Marx converter reside in loops containing a switched-capacitor and other MOSFETs only, MOSFET drain-source voltages are upper bound by the maximum panel voltage. It is particularly advantageous to choose a panel whose open-circuit voltage is just below a standard value for V_{dss}. Over-sizing the MOSFET beyond the required V_{ds} rating would lead to unneeded switching or conduction loss and a suboptimal design. The MOSFET used in the simulated and experimental prototypes was chosen for a suitable compromise between on-resistance and gate charge.

10.4.3 Power Diode

The power diode was chosen primarily to support the peak output current and to block the peak reverse voltage safely. Secondly, it was chosen for low capacitance, forward voltage, and ESR. Having added output diodes to the implemented system,

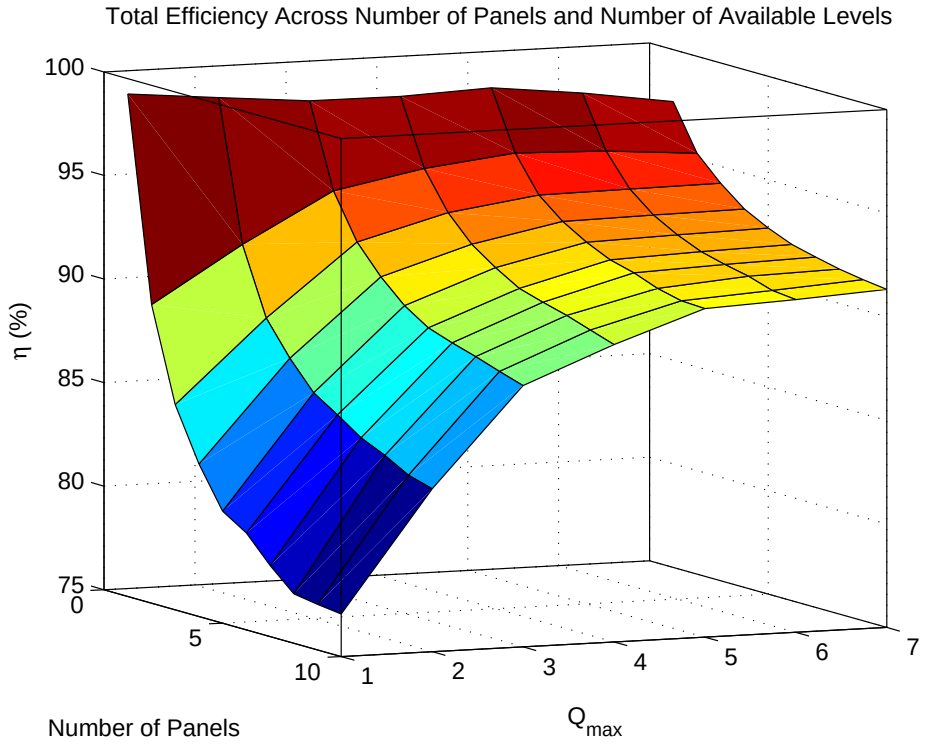


Figure 10-18: Unoptimized system performance prediction: $Q_{avail} = [0 : 1 : Q_{max}]$, Monte Carlo Length = 400, $I_{o,sweep} = [0.01 : 0.02 : 6.93]$ A, C = 12.5 μF, $f_{sw} = 250$ kHz, $R_{dson} = 10$ mΩ, $Q_g = 10$ nC, $Q_{oss} = 5$ nC, $Q_{rr} = 25$ nC,$V_g = 15$ V, $V_{oc} = 29$ V, $V_{mp} = 24.6$ V, $I_{sc} = 7.38$ A, $I_{mp} = 6.93$ A, Distribution Compression = 50%

the additional losses can be estimated as follows:

$$V_{fwd,i} = \ln\left(\frac{I_o}{I_s + 1}\right) n\frac{kT}{q} + ESR_{diode} I_o \tag{10.22}$$

$$P_{diode} = I_o \sum_i V_{fwd,i} + f_{sw} C_{j,i} V_{rr,i}^2, \tag{10.23}$$

where V_{rr} is the reverse voltage during ϕ_1 and C_j is the junction capacitance of the diode. This expression can be used to improve the accuracy of the Monte Carlo performance predictions. The power diode chosen for this example was the Motorola MBR20100C Shottky [182]

10.4.4 Simulated Performance

A 3-panel system was simulated using SPICE and MATLAB®. The performance of this system was predicted with Monte Carlo methods having incorporated the losses derived in (10.18), (10.19) and (10.23). A switching frequency of 360 kHz was chosen based on the simulated loss mechanisms computed above. The results are shown in Table 10.3. A summary of circuit elements selected for the simulated prototype is shown in Table 10.4.

Table 10.3: Simulated statistical performance: 5-level, 3 Panel optimized system: Monte Carlo Length = 100, Distribution Compression = 50%, $\Delta I_o = 1$ mA, Diode Loss = [on], $f_{sw} = 360$ kHz

efficiency	symbol	simulated result
tracking	η_p	95.43%
conversion	η_c	97.56%
total	η	93.10%

Table 10.4: Circuit component summary

Component	Part No. / Value	Note
Switched-capacitors, Output Capacitor	12.5 μF	Metal Film 1 $\parallel$ 4.7 $\parallel$ 6.8 μF
Panel Capacitor	25 μ F	12.5 $\parallel$ 12.5 μF
MOSFET	IRF8721	
Output Diode	MBR20100C Schottky	

It is important to realize that the central inverter cannot track panel power, corresponding to η_p, directly. Instead it tracks its input power, corresponding to η. Having incorporated the loss mechanisms from Section 10.3 and in equation (10.23), this observation was accounted for in simulation by allowing the inverter to choose the I_o that maximized its input power. Tracking efficiency was recorded for comparison to total efficiency.

10.4.5 Model Validation

A single experiment was performed in simulation to validate the linear modeling effort and loss calculations above. A fixed set of conversion ratios and MPPs was

chosen for the three panels. Tracking, conversion, and total efficiencies were plotted for a single I_o sweep. Figure 10-19 compares the results for calculated data based on Section 10.3 and equation (10.23), a SPICE simulation of the linearized model and a SPICE simulation of the MOSFET system. The difference in η_c between the linearized model and the other two data sets represents switching and output diode loss. Errors between the calculated model and FET simulation are likely due to estimation errors in computing diode and switching losses. Note that in the plots of Figure 10-19, the maximum in total efficiency lines up closely with the maximum in tracking efficiency.

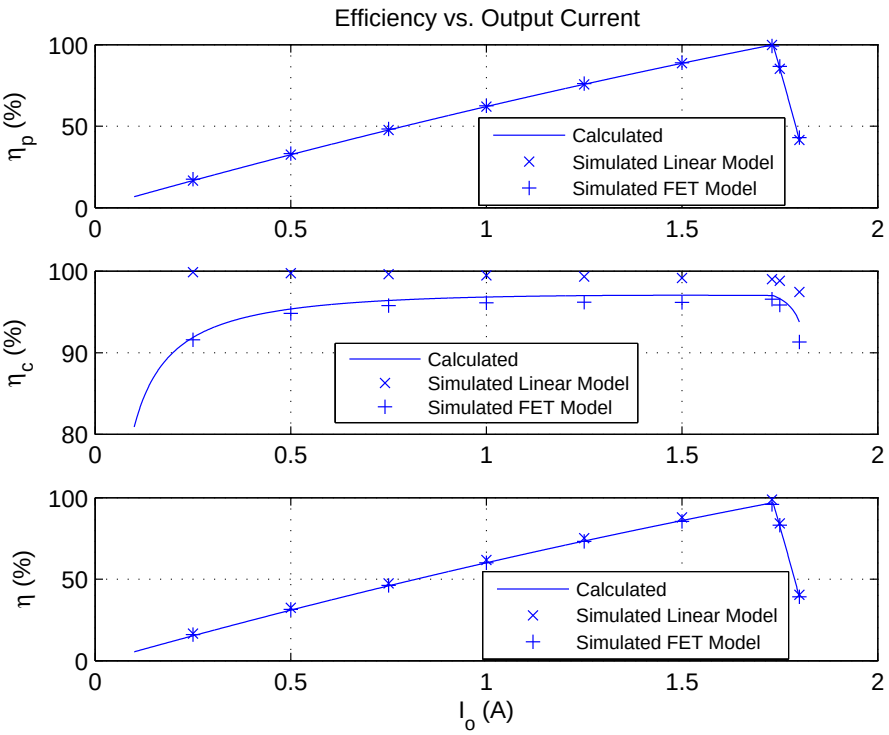
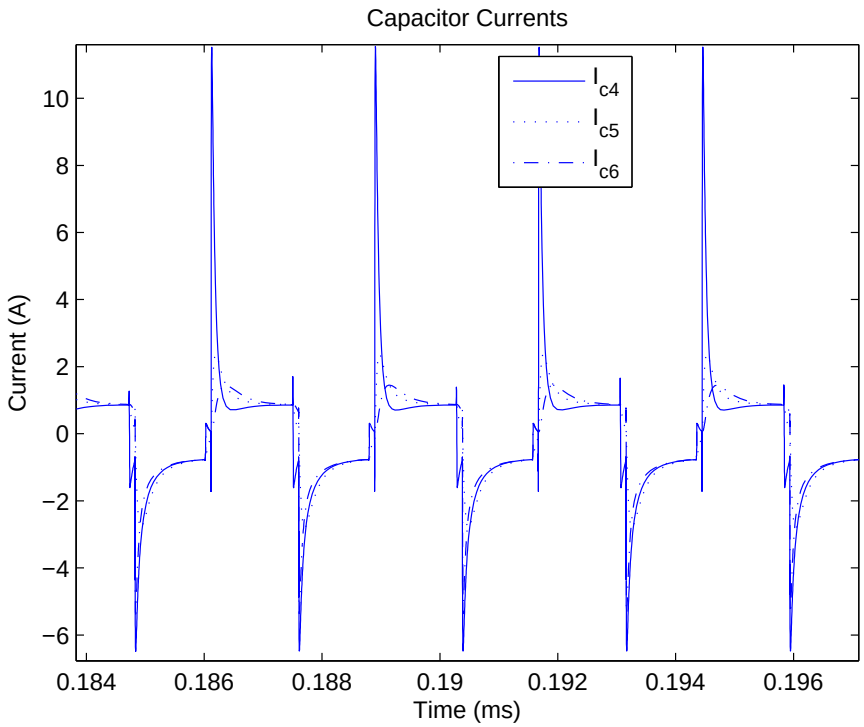
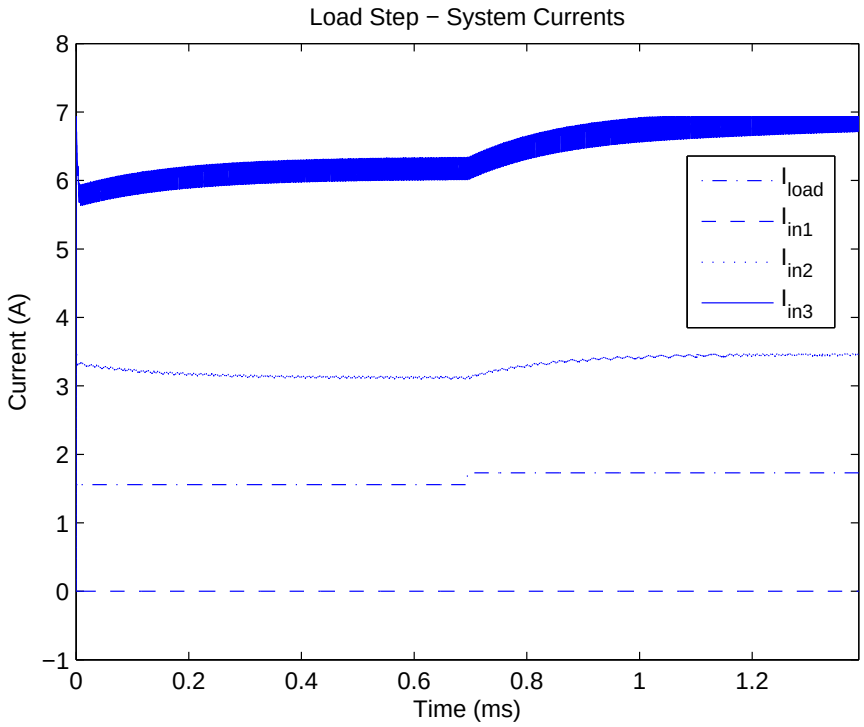


Figure 10-19: Model Validation: Single I_o sweep, 3 sources, $Q = [0, 2, 4]$, $I_{mp,vec} = [0.007\ 3.465\ 6.93]$ A, $C = 12.5\ \mu$F, $f_{sw} = 360$ kHz, MOSFET: IRF8721, $V_g = 10$ V, deadtime $= 100$ ns, $R_g = 4\ \Omega$

Time domain waveforms from the simulated system are shown in Figure 10-20. Figure 10-20(a) shows a zoom-in of the capacitor currents. The shape of those currents indicates operation between the slow and fast switching limits defined in Section 10.3.2.



(a) Capacitor Currents



(b) Load Step - Currents

Figure 10-20: Time-domain waveforms.

Figure 10-20(b) shows panel input currents during a step change in the load current from 90% to 100% of the predicted maximum power current. In this example, Panel 1 is bypassed ($Q_1 = 0$) because its MPP is quite low; $I_{in1} = 0$ in the plots. The other two panels initially settle close to their respective $I_{mp,i}$'s - Panel 2 exhibits half of the photovoltaic current that Panel 3 does. When the load current steps to its maximum power value, I_{in2} and I_{in3} settle on their respective $I_{mp,i}$'s.

10.5 Experimental Prototype

An experimental prototype was constructed to prove the concepts developed above. The printed circuit board and schematic can be found in Appendix C. Summaries of the circuit components and parameters for each of the implemented conversion ratios are shown in Tables 10.5 and 10.7.

Table 10.5: Experimental prototype parameter summary

Parameter	Symbol	Value
Switched-capacitor	C	12.5 μF
Switching Device	M_i	IRF8721
Panel Capacitor	C_{pi}	25 μF
Local output Capacitor	C_{oi}	12.5 μF
Local output Diode	D_{oi}	MBR20100C Schottky
Switching freq. $Q = 2$	$f_{sw,Q2}$	100 kHz
Switching freq. $Q = 3$	$f_{sw,Q3}$	88 kHz
Switching freq. $Q = 4$	$f_{sw,Q4}$	127 kHz
Panel 1 MP Voltage	V_{MP1}	24.6 V
Panel 1 MP Current	I_{MP1}	6.93 A
Panel 2 MP Voltage	V_{MP2}	24.6 V
Panel 2 MP Current	I_{MP2}	3.47 A
Panel 1 MP	P_{MP1}	170 W
Panel 2 MP	P_{MP2}	85 W

Figure 10-21 shows a connection diagram for the experimental setup consisting of two series connected modules and the constructed PV circuit models. In this experiment, a $Q = 4$ and a $Q = 2$ module was constructed for comparison to the model validation simulated data from Figure 10-19. Construction of the $Q = 0$ module in that simulation was not warranted as it simply represents a short circuit.

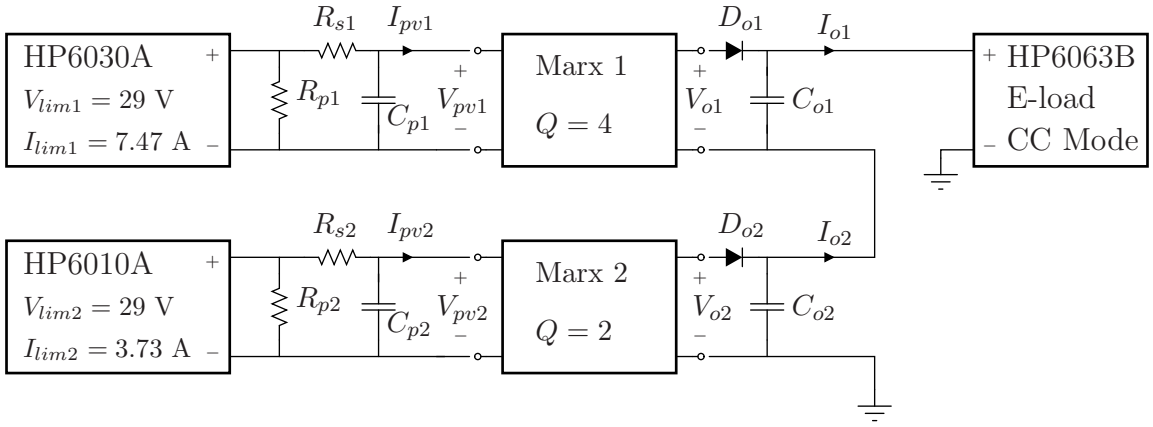


Figure 10-21: A connection diagram depicting the experimental setup for the series connection of Marx modules and PV circuit models.

Conversion efficiency was measured using HP34401A digital multimeters (DMM's). Input and output voltages for each converter were measured at the PCB terminals. Current sense resistors with nominal values of 10 mΩ each were used to measure input and output currents. The precise value for each current sense resistor was measured separately. to within 0.01mΩ using a current-mode and a voltage-mode DMM simultaneously.

Figures 10-22 and C-1 show photographs of the Marx converter experimental setup. Figure 10-22 shows the power supplies and measurement equipment. On the left are the power resistors used to model the photovoltaic panels in this experiment. Figure C-1 shows a closeup photograph of the two Marx converters and the resistive elements. The rotary switches along the bottom of each converter determine the switching pattern and thus the conversion ratio for each converter. Sense resistors are visible on the input side (left side) for each converter.

10.5.1 Photovoltaic Circuit Model Implementation

Figure 10-23 depicts the experimental construction of the PV circuit models. To simulate the PV circuit mode from Figure 10-7, the power supplies were set with a current limit equal to the simulated photovoltaic current I_{ph} (not the short-circuit current) and a voltage limit equal to the open-circuit or diode forward voltage V_{dp}.

The values of the resistive elements were computed based on the simulated PV

Figure 10-22: A photograph of the switched-capacitor (Marx) converter photovoltaic experimental validation system.

parameters from the simulation in Figure 10-19 and the mathematical expressions in equations (10.2)-(10.5) and the nominal panel parameters from (10.8). The first PV panel, PV_1, was modeled having the peak maximum power conditions (170 W) while the second, PV_2, was modeled having half the maximum power of the first. The target and implemented values are summarized in Table 10.6.

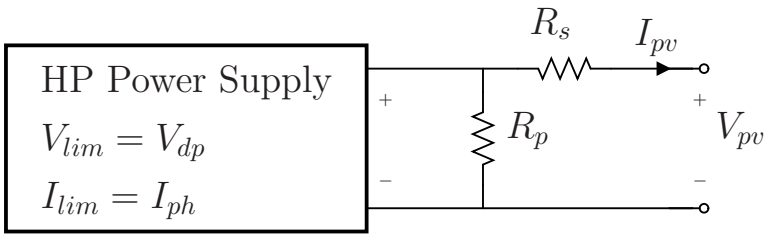


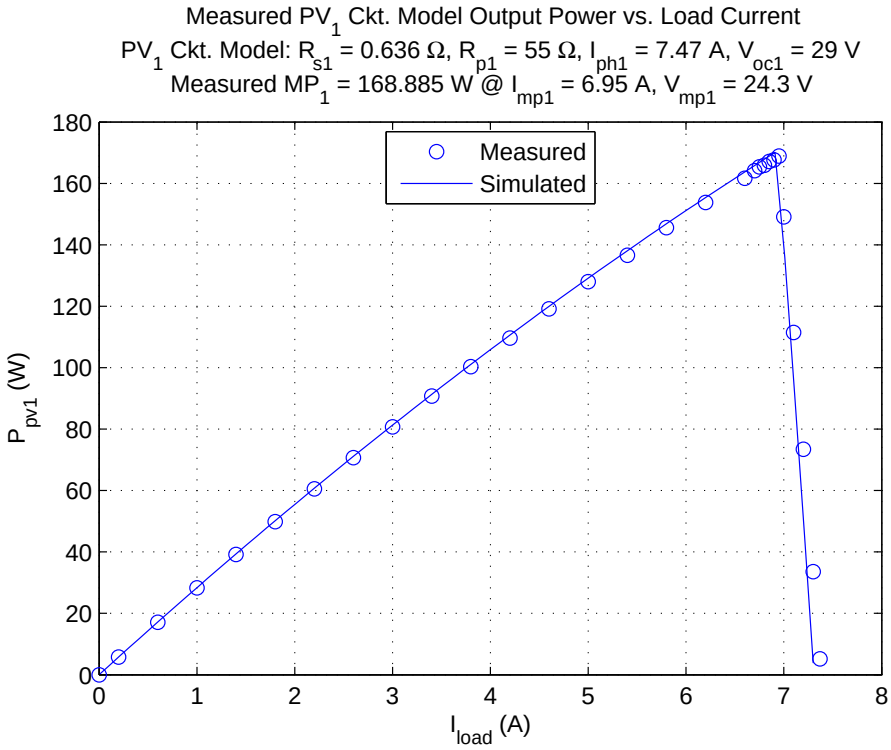
Figure 10-23: The experimental PV circuit model construction.

Table 10.6: The implemented PV circuit model elements

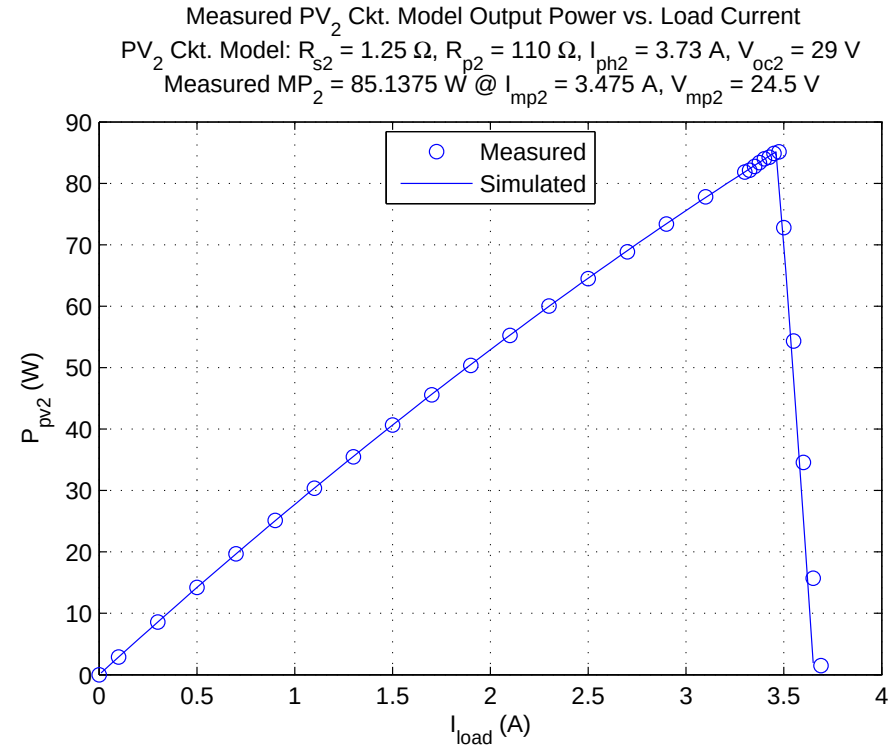
Name	Target Value	Implementation	Actual Value
R_{s1}	0.635 Ω	0.6 Ω / 50 W + 0.036 Ω / 10 W	0.636 Ω
R_{p1}	54 Ω	55 Ω / 50 W	55 Ω
R_{s2}	1.27 Ω	1.25 Ω / 50 W	1.25 Ω
R_{p2}	108.1 Ω	2×55 Ω / 50 W	110 Ω

Table 10.7: Detailed experimental prototype circuit component values

Component, Parameter	Value
R_{gi}	30 Ω
D_{zi}	15V 1N5929+2.5V1N5222B
R_{cp}/C_{cp}	220 Ω/102
C_{bs}	104
C_z	104
C_o	103
R_{osc}/C_{osc}	105 pot / 104
R_{dead}/C_{dead}	270 Ω/102
Deadtime	150 ns
Q	2
R_{z3}	330
R_{z6}	2 kΩ
R_{z9}	2 kΩ
R_{z10}	50 $\frac{1}{2}$W
Q	3
R_{z3}	330 Ω
R_{z6}	2 kΩ
R_{z9}	2 kΩ
R_{z10}	100 Ω
Q	4
R_{z3}	330 Ω
R_{z6}	1 kΩ $\frac{1}{2}$W
R_{z9}	200 Ω $\frac{3}{4}$W
R_{z10}	200 Ω $\frac{3}{4}$W



(a) PV_1



(b) PV_2

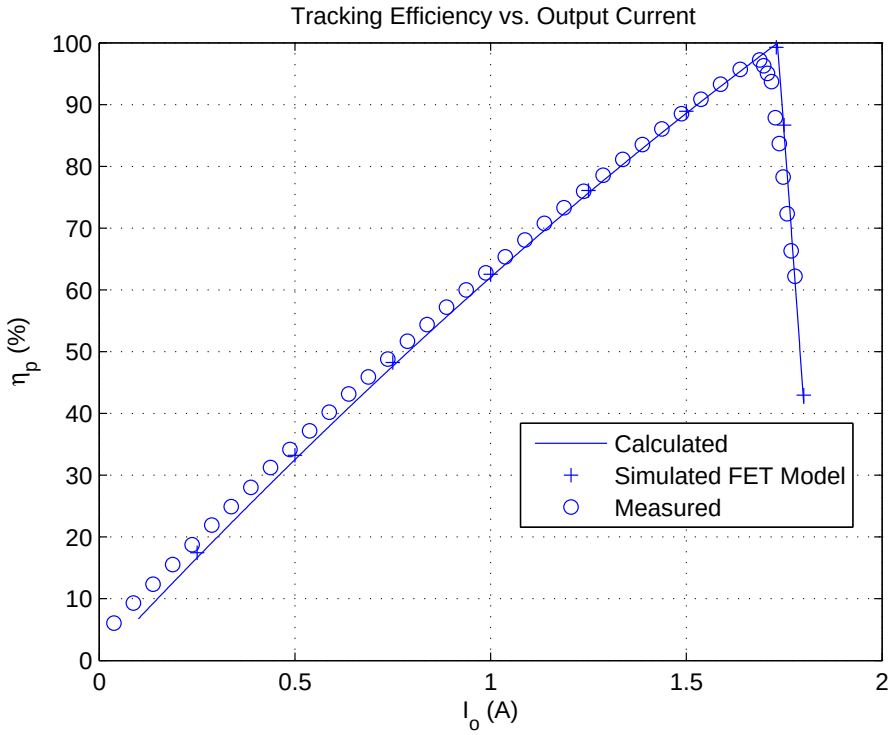
Figure 10-24: Experimental validation of the artificial PV circuit models.

Figure 10-24 shows experimental data validating the large-signal operation of the PV circuit models constructed as described above. The experimental data is overlayed on simulated data found using the circuit model in Figure 10-7. The target maximum power points were 170 W and 85 W respectively. The measured maximum power points were 168.9 W and 85.1 W. The errors are most likely due to differences between the implemented and target resistive element values.

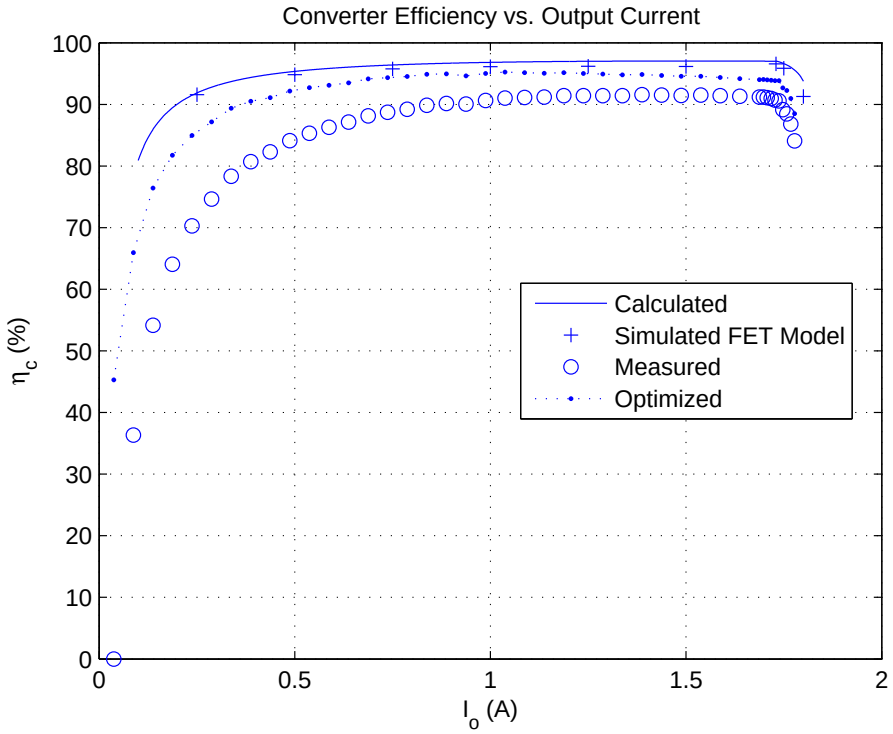
10.5.2 Experimental Prototype Performance

The plots in Figure 10-25 show measured efficiency data compared to simulated and calculated values. The rounding of the peak in the tracking efficiency plot (Figure 10-25(a) is likely due to the slight error in the implementation of the resistive elements in the PV circuit models. The added loss in the conversion efficiency plot (Figure 10-25(b)) is due to added standby power dissipation and added switching loss. The plots also included conversion efficiency for a fully discrete implementation whose standby power dissipation has been optimized. The optimizations are computed in Section 10.6.

The switching frequencies for modules in the experimental prototype were chosen based on the measured data in Figure 10-26. A fixed load of 1.5 A was impressed on each module while the switching frequency was swept within a range yielding safe operating efficiencies. The switching frequency showing the maximum conversion efficiency was chosen for each module. Note that the switching frequency yielding the maximum conversion efficiency generally depends on the conversion ratio.

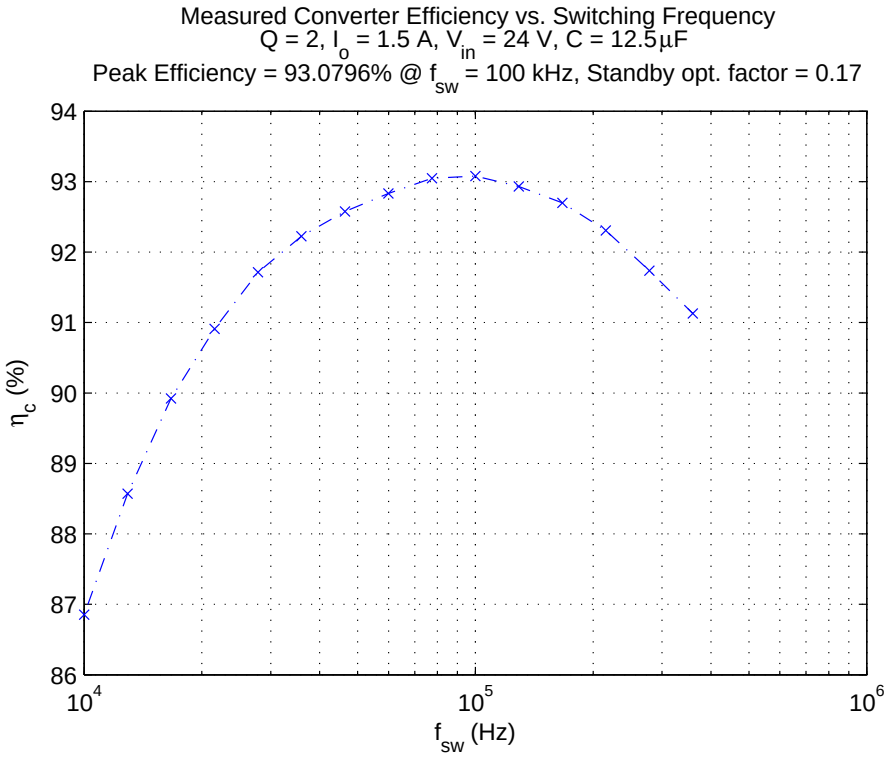


(a) Tracking Efficiency

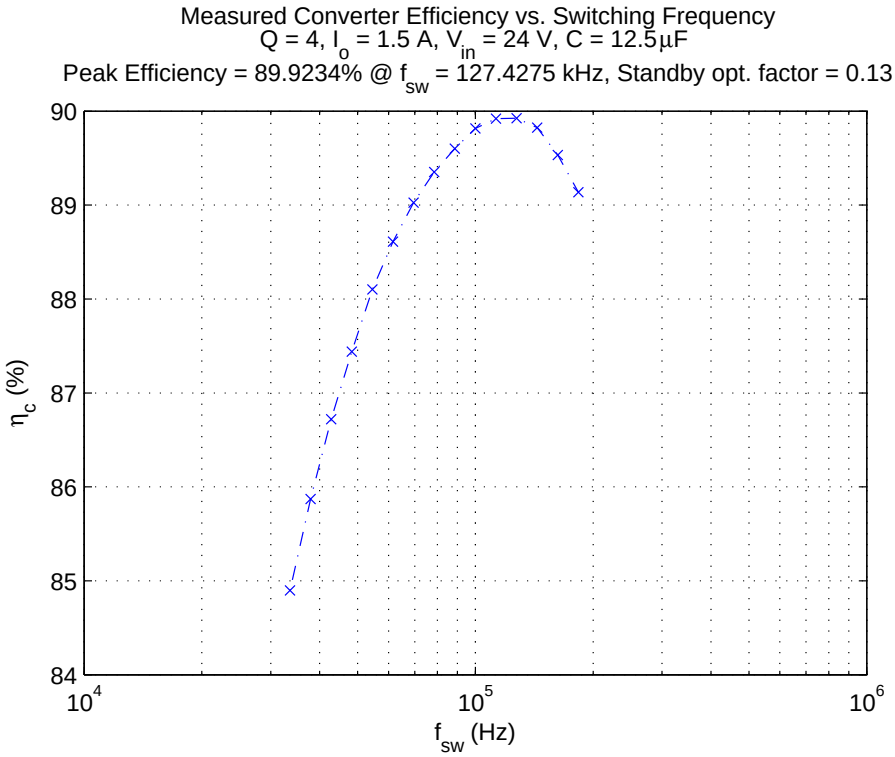


(b) Converter Efficiency

Figure 10-25: Model Validation: Single I_o sweep, 3 sources, $Q = [0, 2, 4]$, $I_{mp,vec} = [0.007\ 3.465\ 6.93]$ A, $C = 12.5\ \mu$F



(a) $Q = 2$



(b) $Q = 4$

Figure 10-26: Switching frequency choice for the experimental system

Figure 10-27 shows a scope shot depicting the operation of the gate drive charge pump circuit from Figure 10-16 for transistor $M6$ in the $Q = 2$ module. The upper trace is the output voltage of the timer IC and shows the charge pump control voltage superposed on the transistors source voltage. The transistor source voltage and the bootstrap node voltage for the high-voltage level shift circuit are shown in the middle two traces. The total bootstrap voltage is the difference between V_S and V_B and is computed on the math channel which shows a DC value of 12.9 V, a voltage suitable for the working operation of the gate drive circuit.

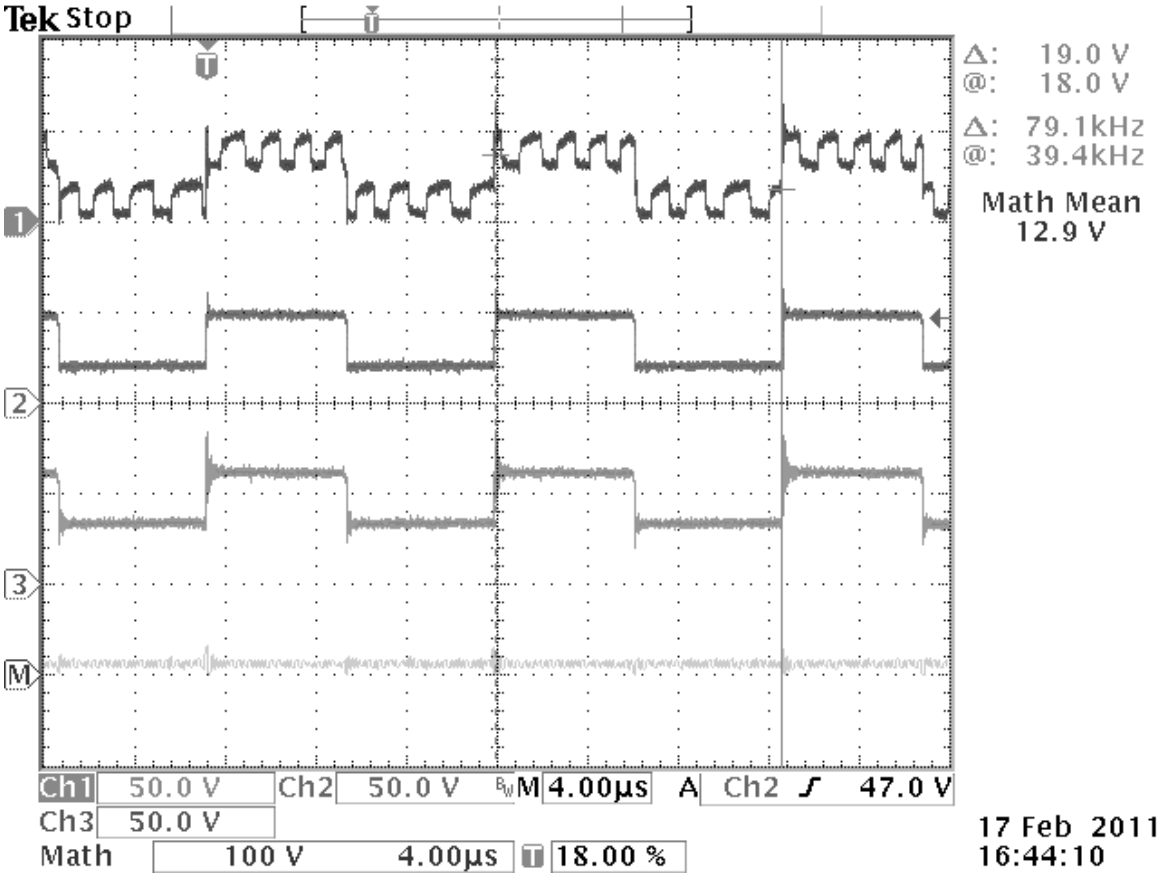


Figure 10-27: Charge pump operation for $M6$ in the $Q = 2$ module. Ch1: V_{OUT}, ch2: V_S, ch3: V_B, math: V_{BS}

10.6 Efficiency Optimizations

Several conversion efficiency optimizations are immediately clear based on the operation of the Marx converter. They are discussed here.

10.6.1 Standby Power

Here we compute the standby power dissipation in the experimental system and speculate what it could be for a reasonably optimized prototype. These optimizations were taken into account in the experimental performance of Section 10.5.

A significant portion of the standby power dissipation originates in the biasing resistors for the zener diodes in the gate drive charge pump circuits. Those biasing resistors should be optimized to provide sufficient bias current for the zener without dissipating unneeded power. Appropriate values for the zener biasing resistors can be chosen based on the time-averaged voltage across that resistor. The time-averaged voltage across the bias resistor divided by the resistance should yield sufficient bias current for the zener diode. The time-averaged bias resistor voltage is the time-averaged MOSFET source voltage minus the zener voltage based on the circuit in Figure 10-16. Therefore the bias resistor value is related to both the MOSFET and the conversion ratio. Table 10.8 indicates the MOSFET source voltages normalized by the input voltage across conversion ratios.

Table 10.8: MOSFET source voltages normalized to the input voltage

	Recharge	$Q = 0$	$Q = 1$	$Q = 2$	$Q = 3$	$Q = 4$
M1	0	0	0	1	1	1
M2	0	0	0	0	0	0
M3	1	1	1	1	1	1
M4	0	0	0	1	1	2
M5	0	0	0	1	1	1
M6	1	1	1	2	2	2
M7	0	0	0	1	2	3
M8	0	0	0	1	1	2
M9	1	1	1	2	2	3
M10	$\approx \frac{1}{2}$	0	1	2	3	4
M11	0	0	0	1	2	3

In the experimental system here, the only MOSFETS needing a charge-sustaining gate drive are M3, M6, M9, and M10. To compute the biasing resistor we would consider the minimum input voltage and the minimum zener bias current. For instance, with $V_{vin,min} = 24$ V and $I_{z,min} = 18$ mA, the time-averaged bias voltage for the MOSFET M6 in the $Q = 2$ module is

$$< V_{bias,M6,Q2} >= 24\frac{1+2}{2} = 36 \text{ V}. \tag{10.24}$$

The maximum zener bias resistor value for the M6 device in the $Q = 2$ switching pattern is then

$$R_{z6,Q2} \leq \frac{< V_{bias,M6,Q2} >}{I_{z,min}} \tag{10.25}$$

$$= \frac{36 \text{ V}}{0.018 \text{ mA}} = 2 \text{ k}\Omega. \tag{10.26}$$

The time-averaged power dissipated in that resistor is

$$P_{bias,M6,Q2} = \frac{< V^2_{bias,M6,Q2} >}{R_{z6,Q2}} \tag{10.27}$$

$$= \frac{V^2_{bias,M6,Q2,rms}}{R_{z6,Q2}} \tag{10.28}$$

$$= \frac{< V_{bias,M6,Q2} >^2 + \left(0.707\frac{\Delta V_{bias,M6,Q2}}{2}\right)^2}{R_{z6,Q2}} \tag{10.29}$$

$$= \frac{36^2 + \left(0.707\frac{24}{2}\right)^2}{2 \times 10^3} = 684 \text{ mW}, \tag{10.30}$$

having assumed a square wave of bias voltage and the maximum allowable bias resistance. Clearly, the standby power for the zener bias diode is significant and depends on the needed bias current to establish the desired nominal zener voltage. As a corollary, the standby power needed to bias the zener diode can be minimized by choosing a zener diode that requires a minimal amount of bias current. Of course, this suggestion is valid to the extent that the zener bias current is larger than the current demanded by the charge pump circuit.

A related source of standby power dissipation is the power dissipated in the zener diode itself. This is simply approximated as

$$P_{zi} = I_{bias,zi} V_{zi}. \tag{10.31}$$

Clearly, reducing the needed bias current reduces this source of standby power dissipation.

A third source of standby power dissipation originates in the capacitor loss for charging and discharging the timing capacitor in the charge pump circuit. This loss is simply

$$P_{cp,timing} = 2 \times \frac{1}{2} C_{cp} V_{zi}^2 f_{cp}, \tag{10.32}$$

where we have assumed that the timing capacitor is fully charged to the zener voltage and fully discharged each switching cycle. Reducing the capacitance value may constitute a significant optimization. The charge pump switching may be fixed by increasing the timing resistor by the same factor.

Finally, the 12 V linear regulator used to power the gate drives indicates a maximum efficiency of 50% given a minimum input voltage of 24 V. This constitutes a power dissipation equal to the power delivered by the 12 V rail. If the linear regulator voltage is increased somewhat, its loss is reduced by the same factor. For instance, the 12 V rail could safely be increased to 18 V without damaging the gate drive circuits.

All of these unoptimized standby power dissipation sources were tabulated. Reasonable optimized values for the fully discrete implementation of the Marx experimental prototype were tabulated as well. The optimized standby power dissipation numbers were assumed in the conversion efficiency data from Section 10.5. The results of this exercise are summarized in Table 10.9 for the $Q = 2$ module.

10.6.2 Run-Time Zener Biasing Optimization

Because the optimal zener bias resistor depends on the conversion ratio, it should be chosen in run-time to minimize standby power. One approach could be to im-

Table 10.9: Standby power optimization results: $Q = 2$ module.

Source	Unoptimized	Ref.	Optimized
Charge pump Zener M3	684 mW	Calc./Meas.	66 mW
Charge pump Zener M6	429 mW	Calc./Meas.	66 mW
Charge pump Zener M9	394 mW	Calc./Meas.	66 mW
Charge pump Zener M10	1.05 W	Calc./Meas.	66 mW
Charge pump Timing Caps ×4	130 mW	Calc.	26 mW
HV Level Shift ×11	158 mW	Assumed	100 mW
ICM7555 ×5	6 mW	Datasheet	6 mW
LM7812	162 mW	Calc./Meas.	35 mW
LM7805	6 mW	Calc.	6 mW
Total	2.9 W	→	617 mW

plement a switched set of fixed resistors for each gate drive. The embedded control in the converter could choose the needed resistor depending on the conversion ratio. This scheme could be implemented with ground-referenced MOSFETS and TTL level control signals as indicated by Figure 10-28.

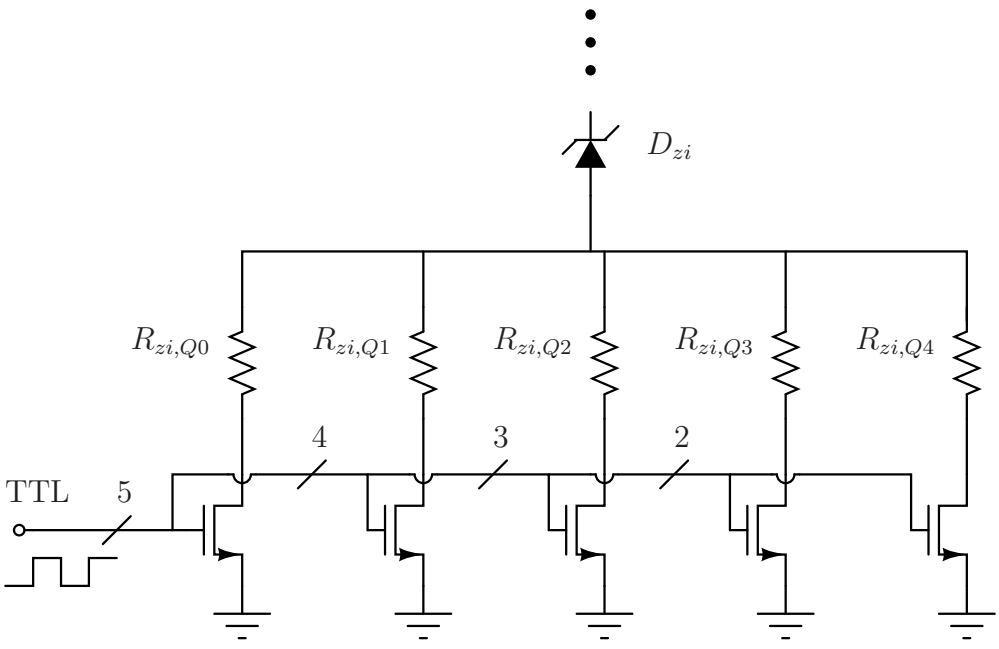


Figure 10-28: A possible run time zener bias resistor selection circuit

10.6.3 Run-Time Frequency Scaling

Based on Figure 10-26, the switching frequency yielding the highest conversion efficiency also depends on the conversion ratio. Therefore, the switching frequency should also be selected in run-time. This selection may be based on a known set of optimum switching frequencies for a specific load current.

10.7 Input Current-controlled Inverter Dynamics

A linearized model of the central input current-controlled inverter is shown in Figure 10-29. The closed-loop transfer functions of particular interest can be derived from that circuit. The transfer function from the inverter input voltage to the inverter input current is

$$\frac{\hat{i}_{in}}{\hat{v}_{in}}(s) = \frac{M^2(D)}{sL_e + R_e + R \parallel \frac{1}{sC}} \left(\frac{1}{1 + T(s)} \right) \tag{10.33}$$

and the transfer function from the inverter control voltage to the inverter input current is

$$\frac{\hat{i}_{in}}{\hat{v}_{ref}}(s) = \frac{A(s)}{1 + A(s)F(s)}, \tag{10.34}$$

where

$$A(s) = G_c(s)F_m \left(j(s) + e(s) \frac{M^2(D)}{sL_e + R_e + R \parallel \frac{1}{sC}} \right) \tag{10.35}$$

$$F(s) = HR_{sense} \tag{10.36}$$

$$T(s) = AF. \tag{10.37}$$

The linear model parameters, e, j, $M(D)$, L_e, and R_e were chosen for a 500 W buck-derived inverter topology.[1] Figure 10-30 shows step responses of the closed-loop transfer functions in (10.33) and (10.34). They show relatively fast settling times

[1] See reference [183] Chapter 8 for a supporting discussion.

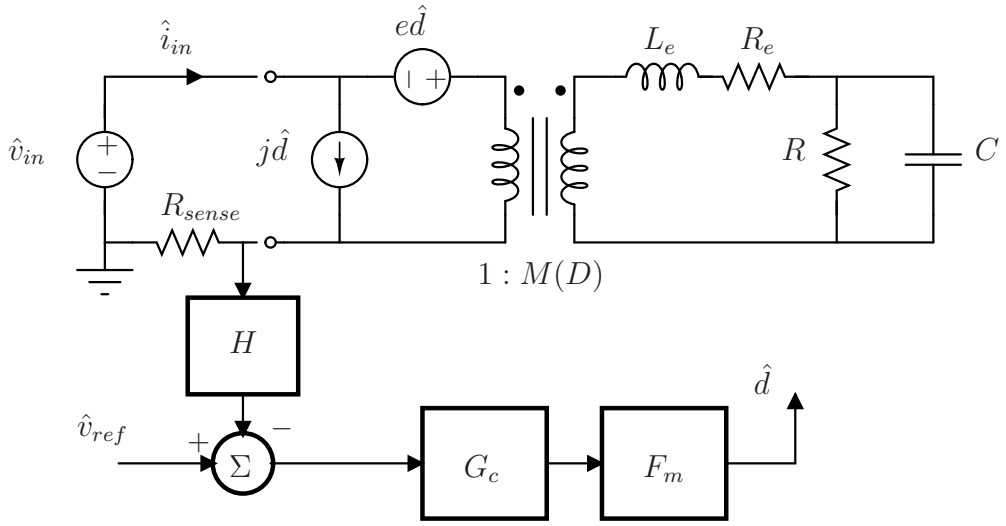


Figure 10-29: A linearized model of an input current-controlled inverter front-end.

in the input current upon step transients in the input voltage (corresponding to the string DC bus voltage) and the reference voltage (corresponding to the control for the sweepable input current). The lower plot also indicates a significant attenuation of the input current response to changes in the input voltage. This attenuation is largely dependent on the low-frequency magnitude of the loop gain $T(s)$ as indicated by equation (10.33).

10.8 Conclusions and Further Work

Widespread grid penetration of PV will rely on the reduction of capital cost and total cost of ownership for solar power systems. It is critical that these factors guide the design of photovoltaic power circuits and system architectures. This work has presented a full system approach utilizing switched-capacitor multilevel DC/DC converters. Substantial cost reductions may be possible by providing per-panel MPPT without the need for per-panel magnetics. Coupling the DC/DC modules with a ripple port inverter eliminates the need for electrolytic capacitors, enabling long-life operation.

The approach presented in this chapter can be viewed as follows. Rather than implementing sophisticated power conversion and MPPT control at each panel, we

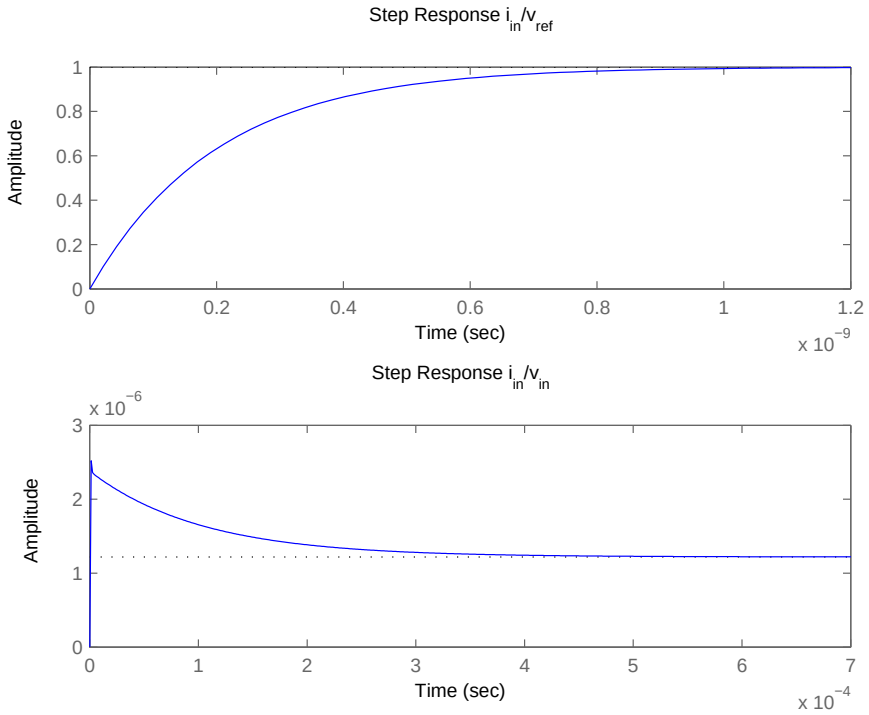


Figure 10-30: Inverter closed-loop step responses

augment each panel with just enough power conversion and control that a centralized inverter with MPPT control can largely recover the power that would otherwise be lost due to partial shading, variations in temperatures, etc. across the solar array. From this perspective, the system level approach is fundamentally different from the standard approach to per-panel MPPT. The responsibility of MPPT control is shared among the panel converters and the central inverter. The result is a simplification of the needed control at the panel level, allowing the use of switched-capacitor converters that would otherwise suffer prohibitive drawbacks in this context. Ultimately, the cost and complexity of the needed per-panel MPPT system may be significantly reduced compared to other approaches while sacrificing little to no total efficiency.

Topics of ongoing research include investigation of MPPT algorithms and related system level tradeoffs for control of the central inverter. There exist necessary tradeoffs among switching frequency, converter efficiency, and global tracking efficiency (I_o step size) when considering the dynamics and runtime MPPT approaches for the full system.

Chapter 11

Conclusion

This thesis has investigated the analysis and design of several multisource electrical networks. Applications include power consuming and power generating systems. Sensing applications are highlighted as a means for controlling power consuming systems. Hybrid fuel cell systems and multipanel solar arrays are highlighted as multisource systems for power generation.

An underlying motivation of this thesis has been to demonstrate the benefits of multisource electrical networks in energy applications. Fundamentally, multisource electrical networks provide added degrees of freedom that can add significant advantages in sensing applications and in energy harvesting applications. The advantages typically come with added complexity in analysis. Therefore an overarching theme in this thesis has been strategic approaches to the analysis and modeling of multisource systems. A primary takeaway from this thesis should be an awareness that the analytical modeling approach can impact significantly our ability to understand the behavior of complicated electrical networks. The level of understanding that we have directly impacts our ability to tailor the design of those systems so that they serve our application.

This thesis began with the detailed analysis and modeling of the fully-differential amplifier in Chapter 2. That amplifier constitutes a multisource network in at least two key ways. First, because the amplifier has a differential-mode input, it can be viewed as a dual input amplifier. Second, the transformation of the generalized

input signal into common-mode and differential-mode signal components yields a multisource network in the analysis of the fully-differential amplifier response.

Chapters 3-5 explored multisource capacitive sensing occupancy detection systems. The fully-differential amplifier served as a measurement tool in the multisource distributed networks. The understanding and design of those systems weighed heavily on the circuit model and analytical results from Chapter 2. The analytical model of the fully-differential amplifier was useful in describing carrier suppression techniques that were central to achieving the performance demonstrated in those examples. Both natural carrier suppression and active carrier suppression based on multiple signal sources were demonstrated in examples.

Chapters 6-9 presented the analysis and modeling of multisource multi-converter power systems for fuel cell power processing. Specific features of the multisource systems were specified as *a-priori* design goals. These included fuel cell current buffering to contend with reliability issues therein and integral diagnostics enabled by run-time impedance spectroscopy. The linear analysis of the multi-converter systems led to design guidelines and evaluation methods that enabled successful implementations of those features in two examples.

Chapter 10 described a method for deploying magneticless per panel solar power converters. Limitations of the switched-capacitor multilevel output converters were overcome by examining a linearized model of the system and considering system level approaches. Decoupling of the maximum power point tracking control among the panel converters and reasonable tracking efficiency were both achieved as a result of this analytical approach.

Appendix A

Capacitive Sensing Occupancy Detection

- Lamp sensor hardware
- Dimming ballast hardware
- Lamp sensor software
- Lamp sensor full system simulation
- Lamp sensor practice
- Standalone sensor software
- Fully-differential amplifier detailed derivations

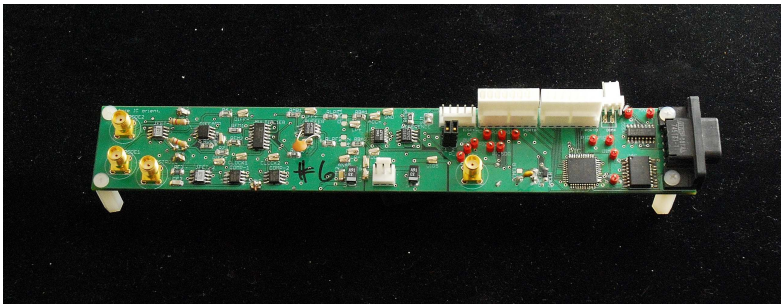
A.1 Lamp Sensor Hardware

- Photographs
- PCB layout
- Schematic drawings
- Build notes
- Bill of materials.

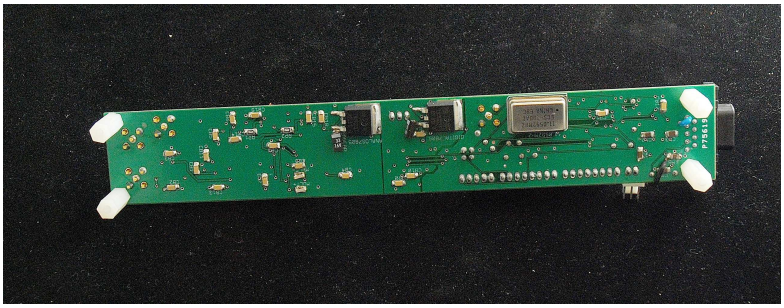
The lampsensor circuit and PCB, (Rev 2) includes the analog electronics needed for synchronous detection, the digital electronics needed for interfacing with a PC, and a DAC for adjusting the DC control voltage on a dimming lamp ballast. The circuit is implemented on a 4-layer PCB with split ground planes, one for the analog side and one for the digital side. The ground planes join at the power supply connection in the middle of the board. The split ground plane layout minimizes the effect of digital signal return currents on the analog signal processing and vice versa. With split ground planes it is important to pay attention to inductive loops that may be formed when bridging the two ground planes. Specifically, traces that bridge the two ground planes should be accompanied by return traces on the layer below.

A.1.1 Photographs

Photographs of the lamp sensor PCB and various measurement electrodes are shown in the Figure below.



(a) Top



(b) Bottom

(c) Electrodes

Figure A-1: Photographs of the lamp sensor electronics and electrodes.

A.1.2 PCB Layout

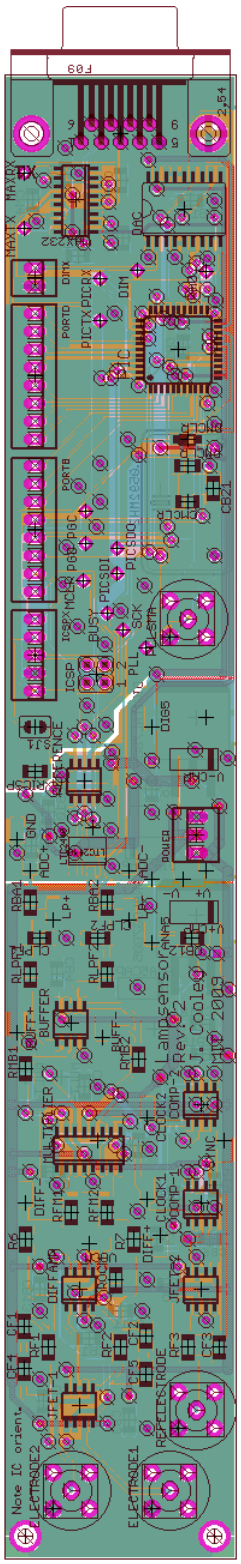


Figure A-2: The Eagle Cad® PCB layout of the lamp sensor, Rev 2.

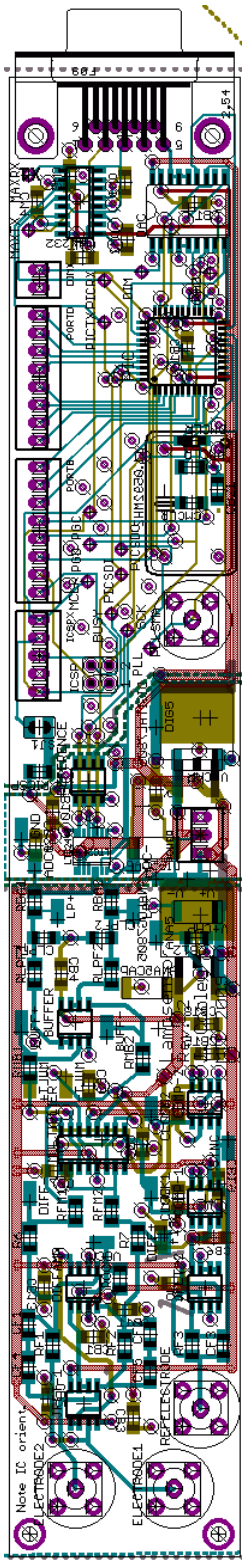


Figure A-3: The Eagle Cad® PCB layout of the lamp sensor, Rev 2 without ground and power planes drawn.

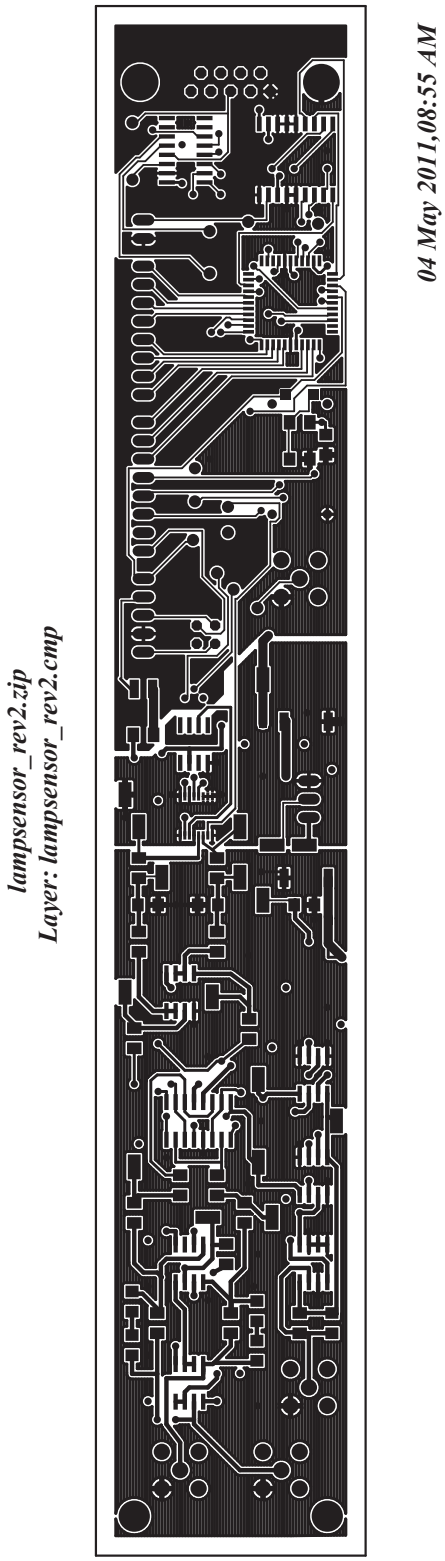


Figure A-4: Top copper layer.

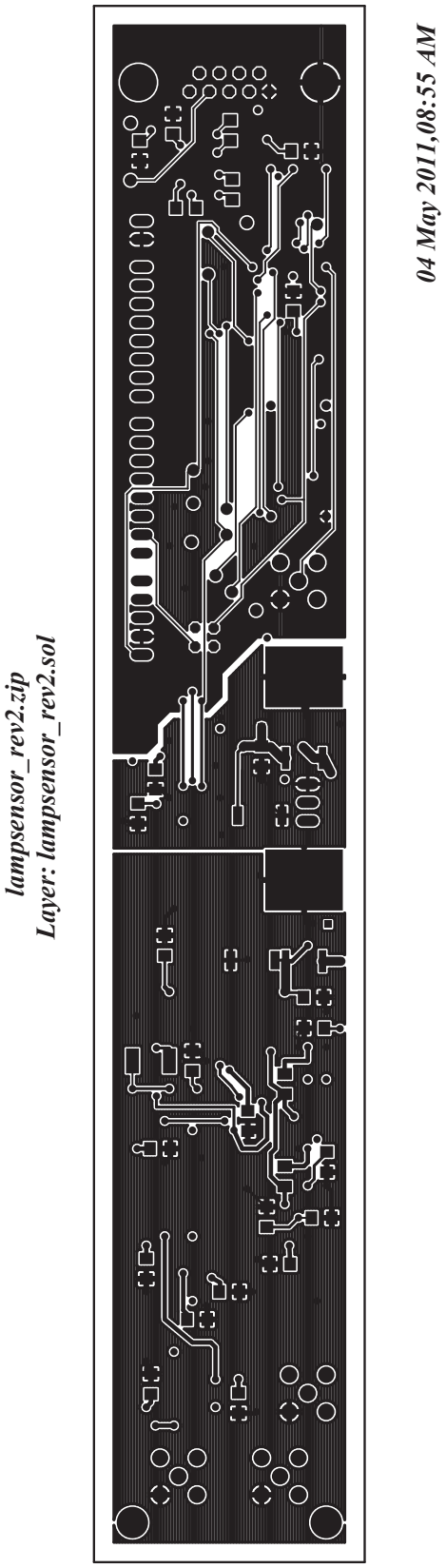


Figure A-5: Bottom copper layer.

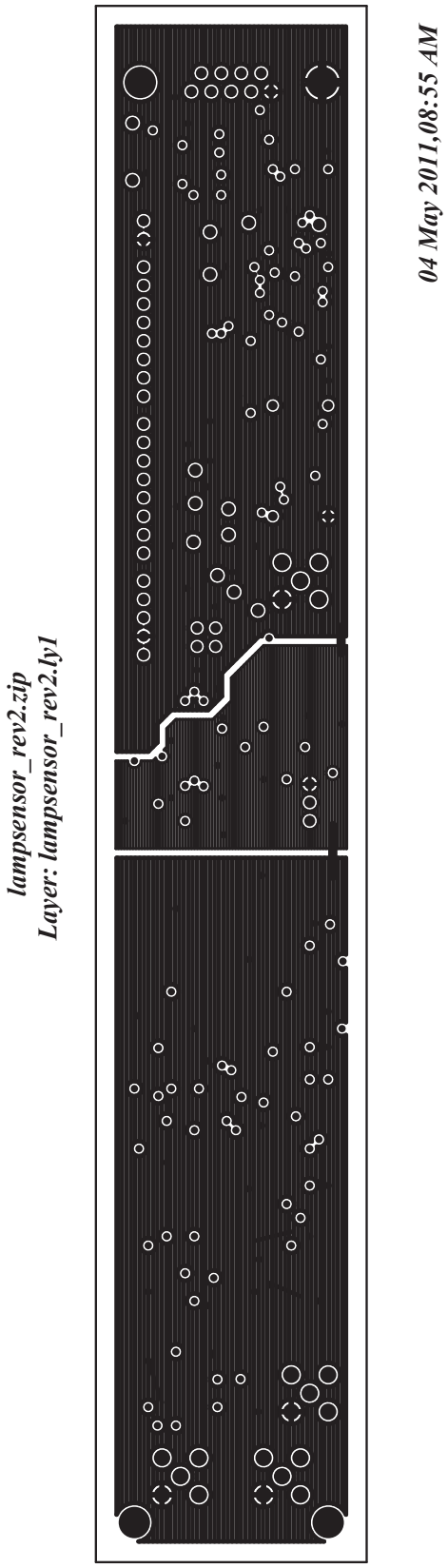


Figure A-6: Inner copper layer 1.

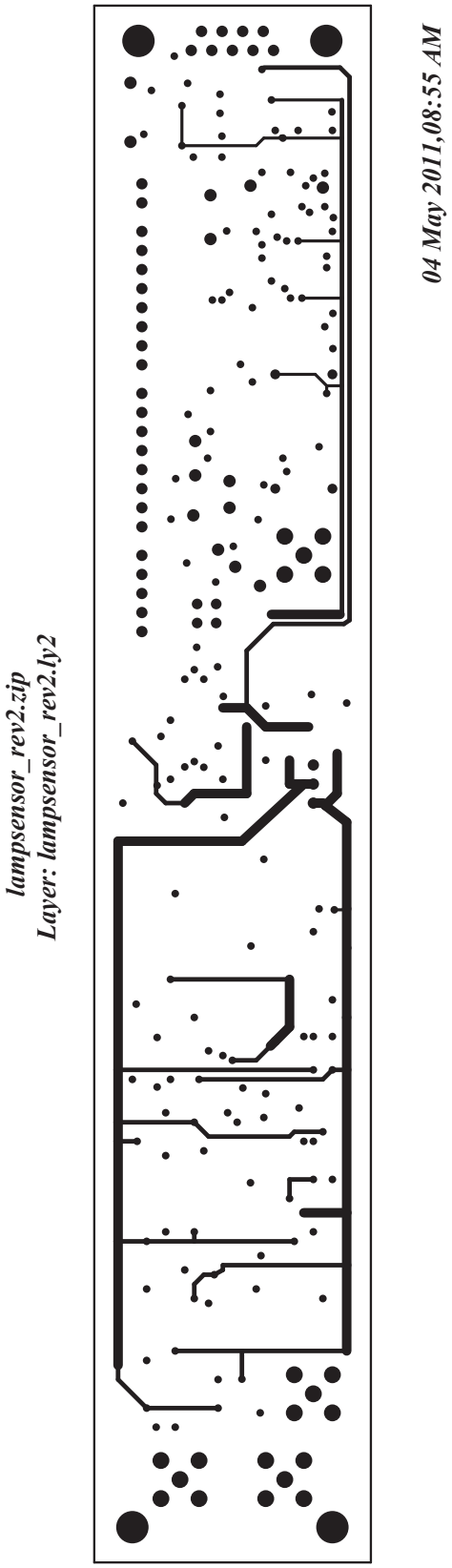


Figure A-7: Inner copper layer 2.

A.1.3 Schematic Drawings

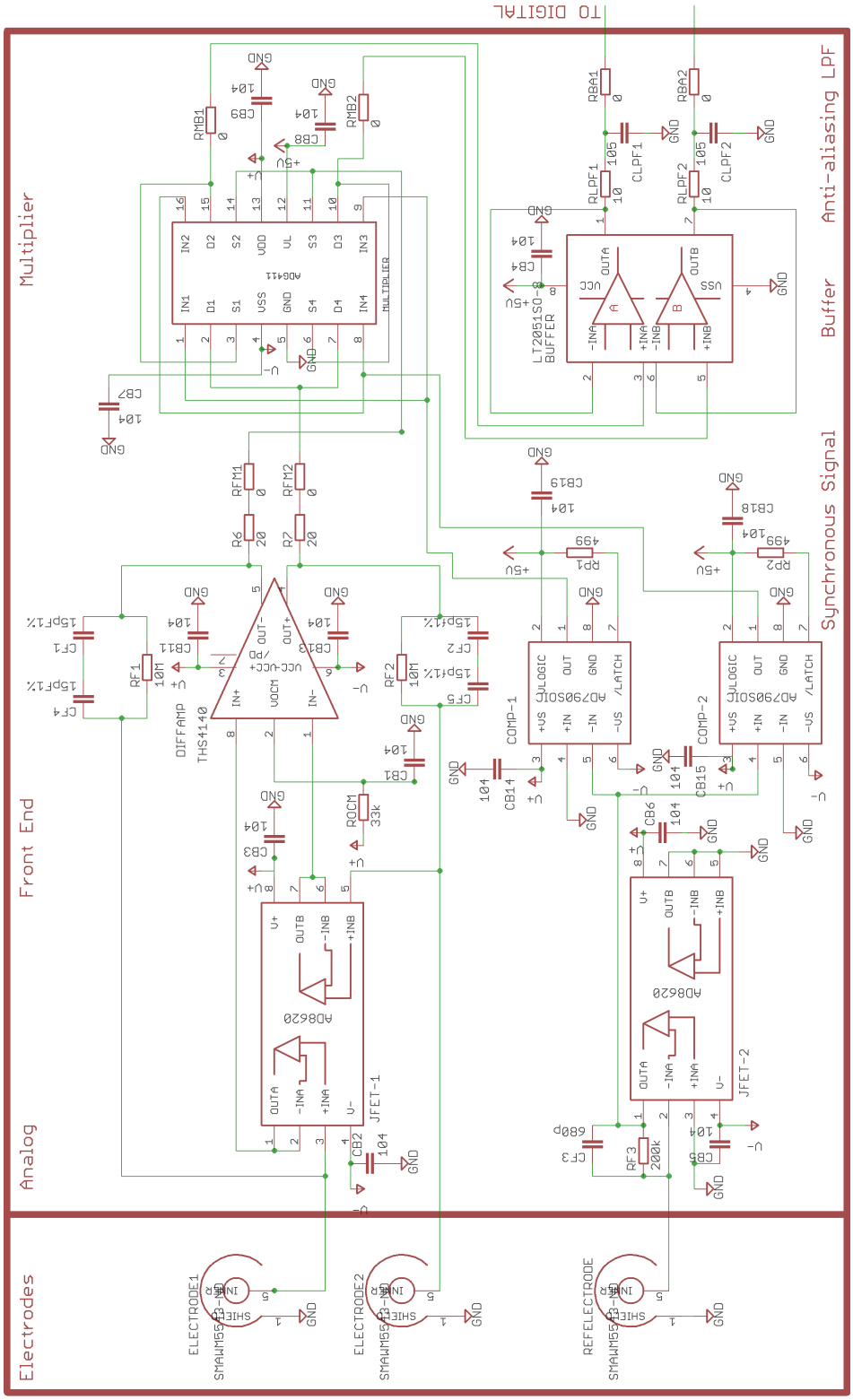


Figure A-8: The analog section of the Eagle Cad® schematic of the lamp sensor, Rev 2.

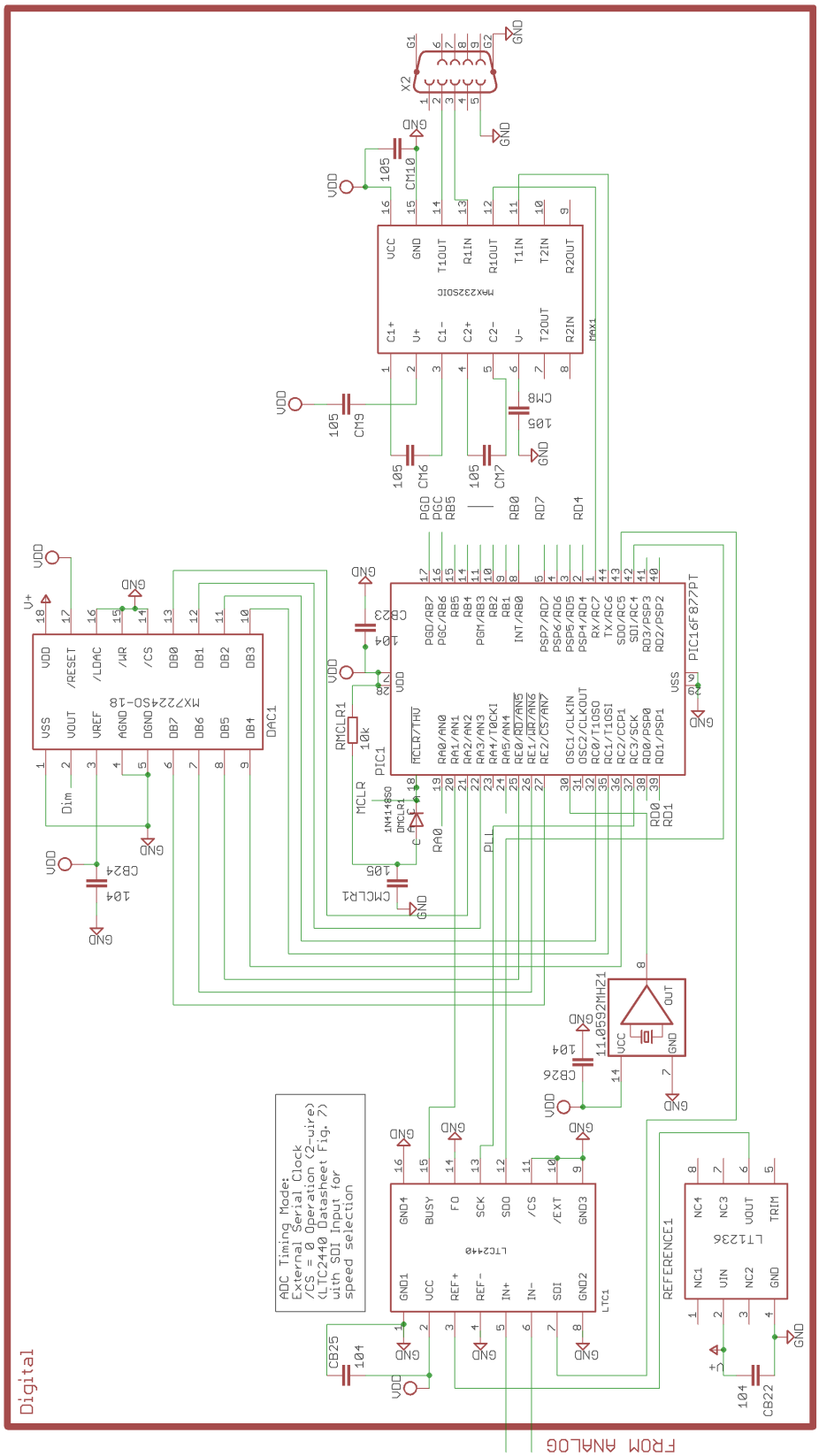


Figure A-9: The digital section of the Eagle Cad® schematic of the lamp sensor, Rev 2.

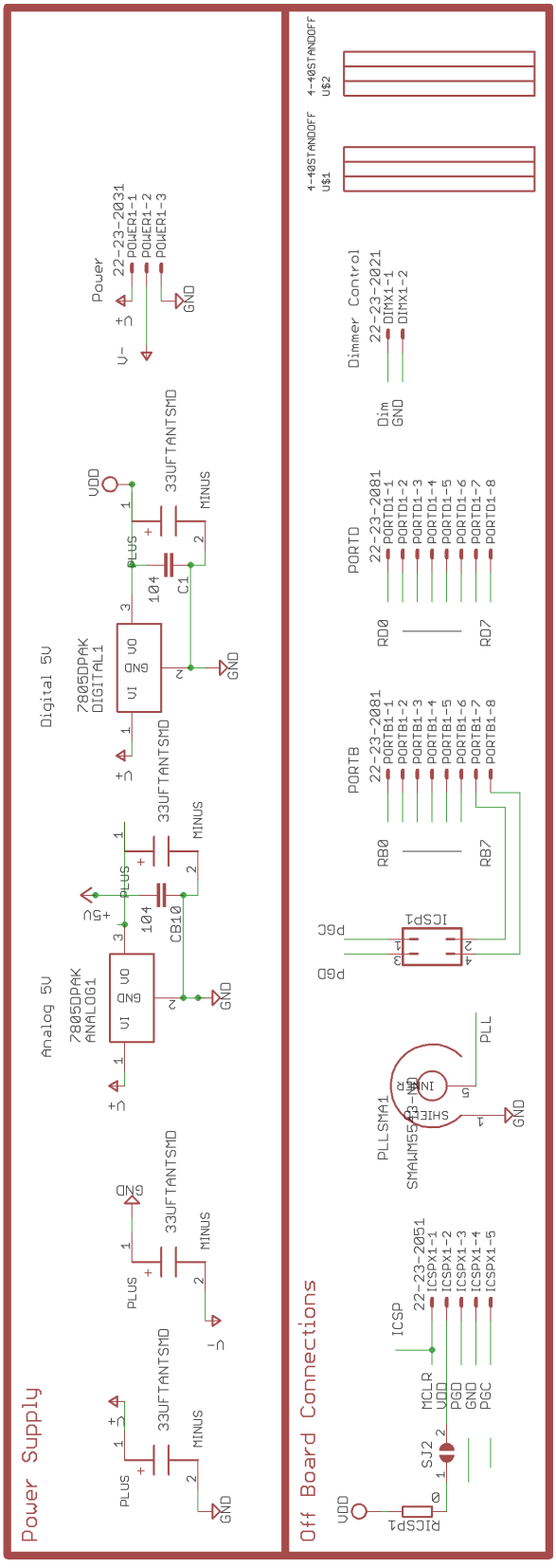


Figure A-10: The ancillary sections of the Eagle Cad® schematic of the lamp sensor, Rev 2.

A.1.4 Build Notes

- Move the LPF to before the buffer and and change it to 10k and 1nF. Use the 0 ohm pads for RMB1 and RMB2 as the 10k and a through hole cap for the 1nF.
- Do solder the solder bridge SJ1 between VDD Molex pin and RICSP=0Ohm.
- CMCLR should not be populated.

A.1.5 BOM

The lamp sensor, Rev. 2, bill of materials is shown in the table below. Refer to Chapter 3 for changes.

Qty	Value	Device	Parts
1		F09HP	X1
1		JP2Q	ICSP
1		QG5860	11.0592MHZ
1		SJW	SJ1
7		0	R-EUM1206 RBA1-2, RFM1-2, RICSP, RMB1-2
1	1N4148SO	1N4148SO	DMCLR
2	4-40STANDOFF	4-40STANDOFF	U3, $U4$
2	10	R-EUM1206	RLPF1, RLPF2
2	10M	R-EUM1206	RF1, RF2
1	10k	R-EUM1206	RMCLR
2	15pF1%	C-EUC1206	CF1, CF4
2	15pf1%	C-EUC1206	CF2, CF5
2	20	R-EUM1206	R6, R7
1	22-23-2021	22-23-2021	DIMX
1	22-23-2031	22-23-2031	POWER
1	22-23-2051	22-23-2051	ICSPX
2	22-23-2081	22-23-2081	PORTB, PORTD
4	33UFTANTSMD	33UFTANTSMD	ANA5CAP, DIG5CAP, V+CAP, V-CAP
1	33k	R-EUM1206	ROCM
22	104	C-EUC1206	C6, CB1-21
8	105	C-EUC1206	CLPF1-2, CM1-52, CMCLR
1	200k	R-EUM1206	RF3
2	499	R-EUM1206	RP1, RP2
1	680p	C-EUC1206	CF3
2	7805DPAK	7805DPAK	ANALOG7805, DIGITAL7805
2	AD790SOIC	AD790SOIC	COMP-1, COMP-2
2	AD8620	AD8620	JFET-1, JFET-2
1	ADG411	ADG411	MULTIPLIER
1	LT1236	LT1236	REFERENCE
1	LT2051SO-8	LT2051SO-8	BUFFER
1	LTC2440	LTC2440	LTC2440
1	MAX232SOIC	MAX232SOIC	MAX232
1	MX7224SO-18	MX7224SO-18	DAC
1	PIC16F877PT	PIC16F877PT	PIC
4	SMAWM5543-ND	SMAWM5543-ND	ELECTRODE1-2, PLLSMA, REFELECTRODE
14	TESTPOINT5000K-ND	TESTPOINT5000K-ND	BUSY-SCK
19	ESTPOINTSO5015KCT	TESTPOINTSO5015KCT	ADC+ - VOCM
1	THS4140	THS4140	DIFFAMP

Table A.1: Lamp sensor, Rev.2 bill of materials.

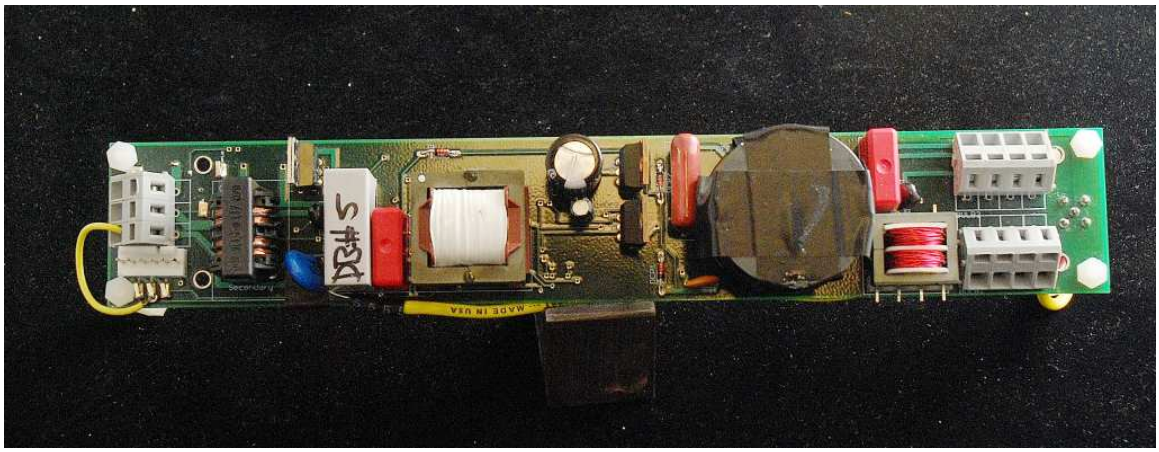
A.2 Dimming Ballast Hardware

- Photographs
- PCB layout
- Schematic drawings
- Build notes
- Bill of materials
- Inductor specifications.

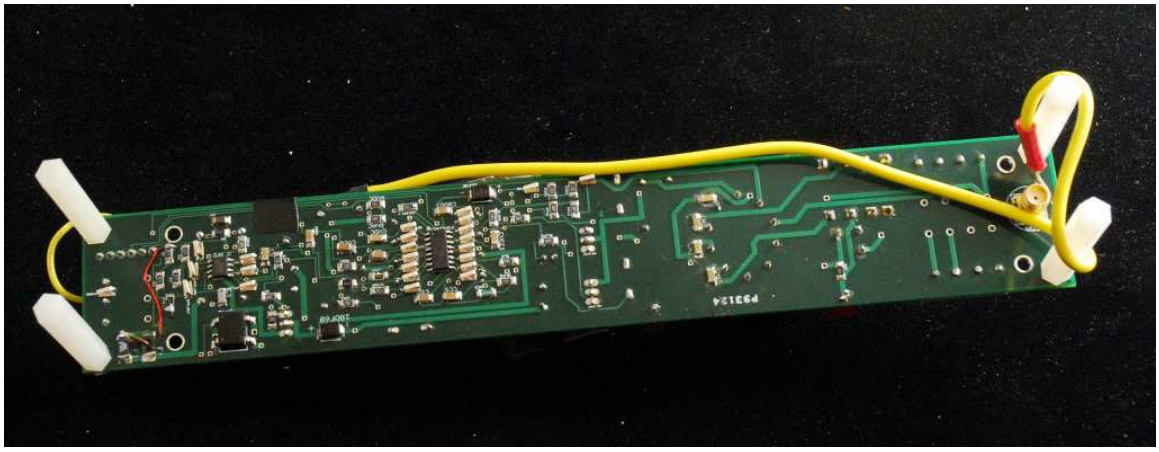
The dimming ballast is a frequency-controlled dimming ballast built around the International Rectifier IR21592 ballast IC. It drives two 32 W bulbs in a balanced configuration and takes a DC input voltage between 0 and 5 V as a control input for the lamp power (brightness). Design software provided by International Rectifier was used to aid the implementation of this ballast. The outputs from that design software are included in this Appendix. Some modifications were made to the resulting design. Those modifications are also described in this Appendix.

A.2.1 Photographs

Photographs of the dimming ballast, Rev. 2 PCB are shown in the Figure below.



(a) Top



(b) Bottom

Figure A-11: Photographs of the dimming ballast, Rev. 2 PCB.

A.2.2 PCB Layout

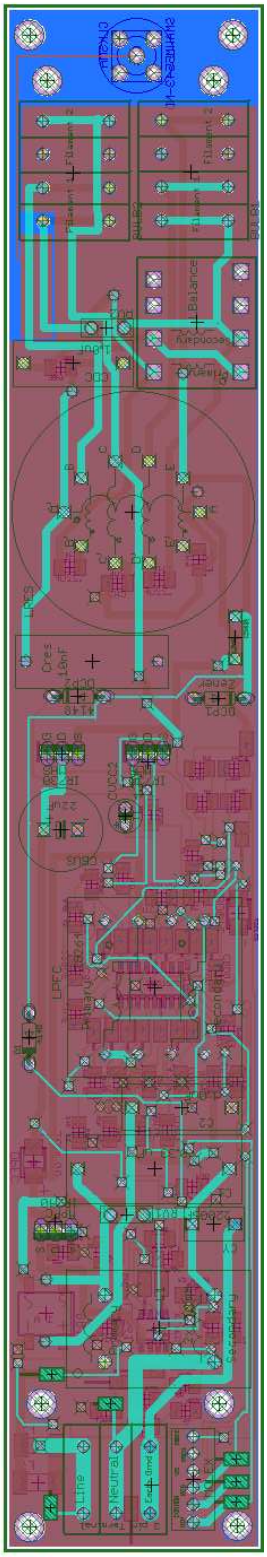


Figure A-12: The Eagle Cad® PCB layout of the dimming ballast, Rev 2.

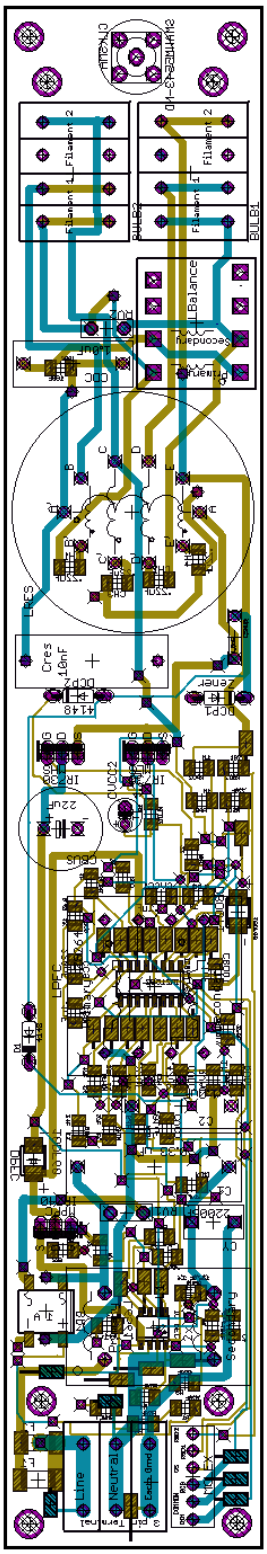


Figure A-13: The Eagle Cad® PCB layout of the dimming ballast, Rev 2 without ground and power planes drawn.

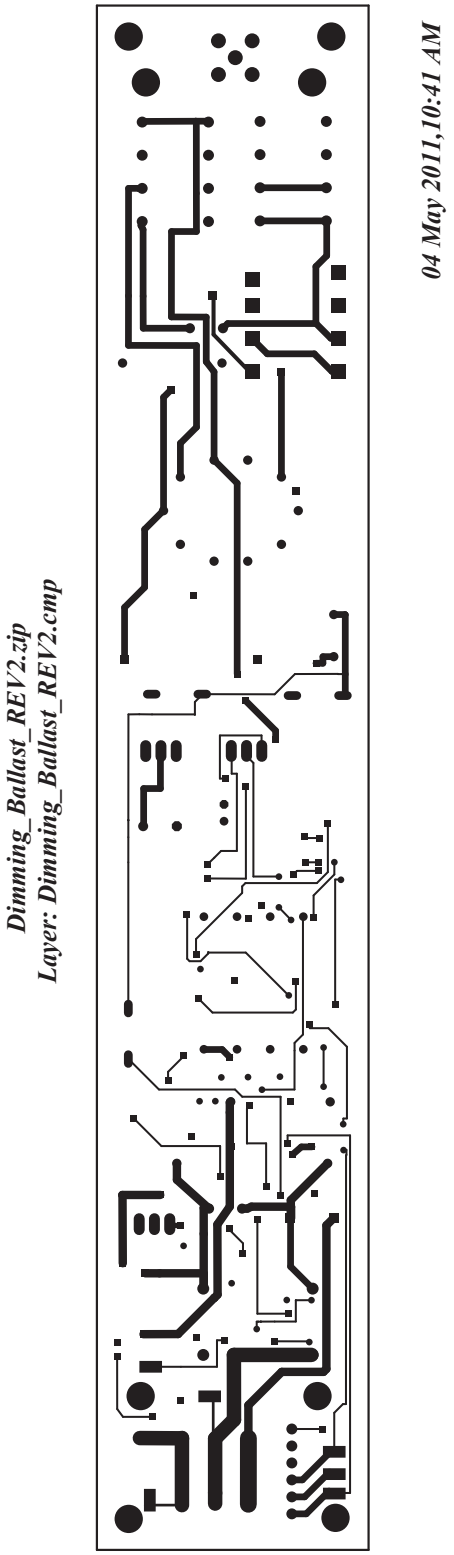


Figure A-14: Top copper layer.

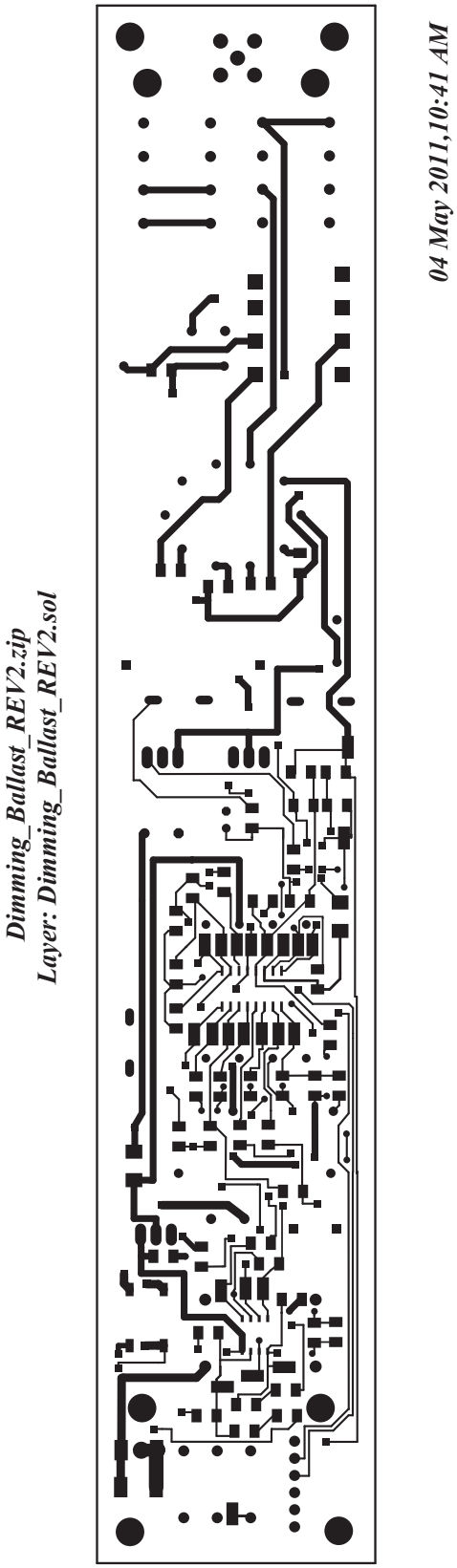


Figure A-15: Bottom copper layer.

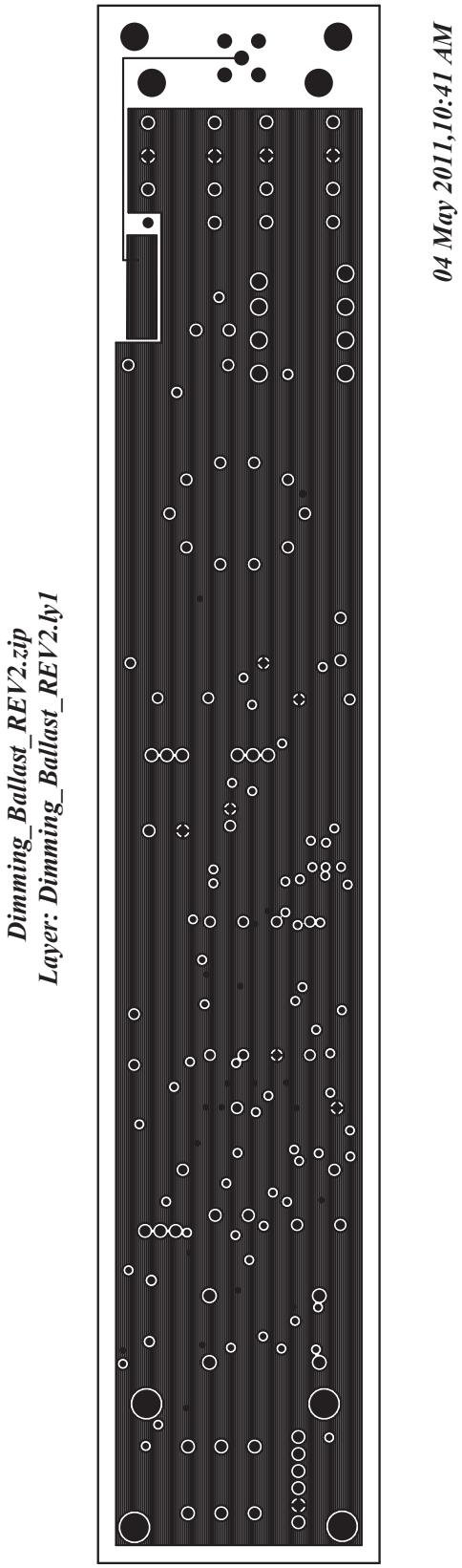


Figure A-16: Inner copper layer 1.

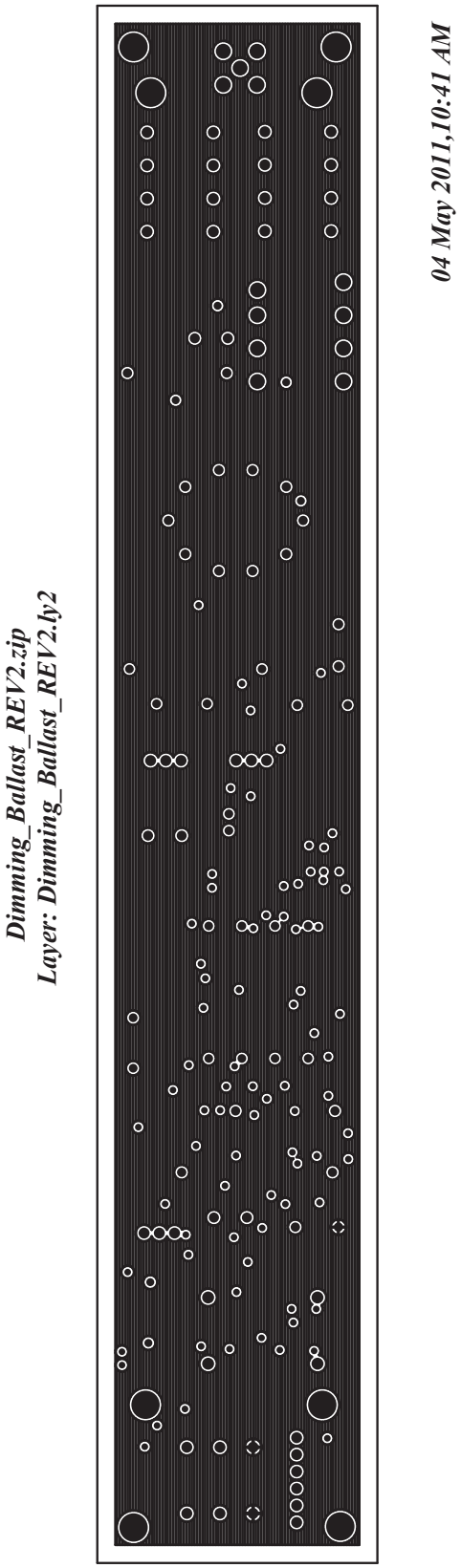


Figure A-17: Inner copper layer 2.

A.2.3 Schematic Drawings

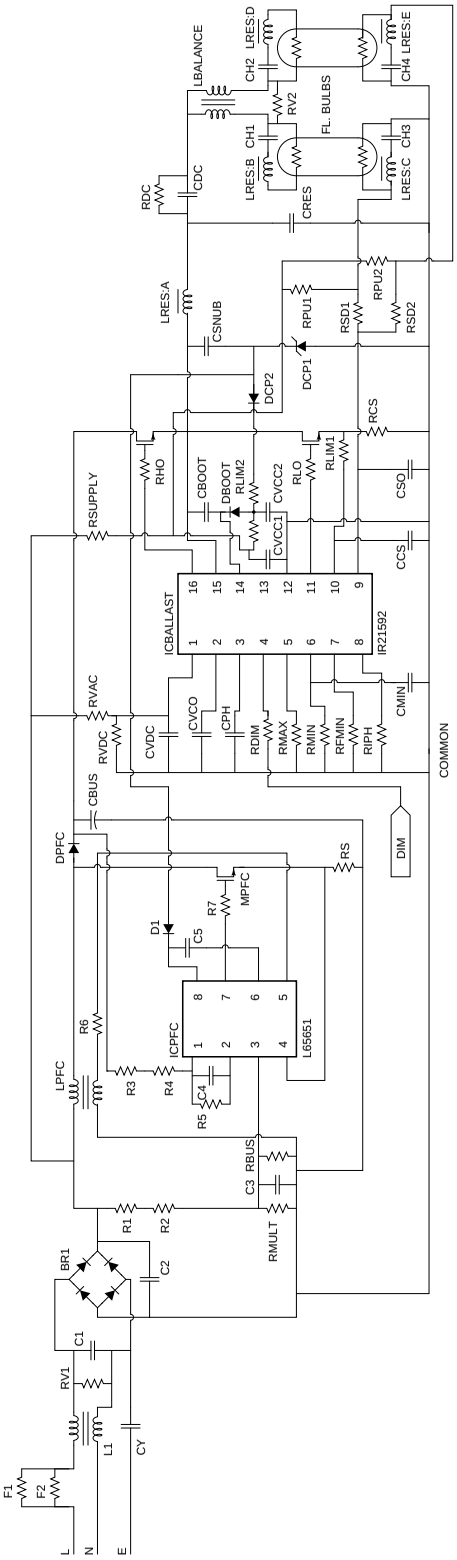


Figure A-18: Dimming ballast, Rev. 2 schematic

A.2.4 Build Notes

Layout notes:

- Wind Lres to inductance value not to turns count. 48 instead of 54 is about right for 1.2mH. This is because the gap length of the actual core is .5mm while the design calls for .6mm yielding a higher AL value in the actual core set than in the designed core set.
- Eliminate buzz and flicker: Short Earth plane to common plane at terminal block (earth plane) and molex near terminal block (common) to eliminate buzz and flicker. For EMI filtering, lift Cy outside leg and connect to Earth gnd from wall and backplane. In next rev, eliminate earth plane, or make both planes common planes.

Filament heating notes - Daniel Vickery, optimized the component values to reduce unneeded filament heating - Last updated 2010.09.21:

- Chx: 0.22uF $\rightarrow$ 0.12uF - This increases the impedance of each heating capacitor, reducing the voltage across the filaments.
- Cph: 0.27uF $\rightarrow$ 0.56uF - Doubles the pre-heating time (before ignition).
- Cvco: 0.01uF $\rightarrow$ 0.022uF - Decreases the slope of the ignition frequency ramp by a factor of two. This fixes our original striking problems.
- Riph: 24k $\rightarrow$ 26.1k - Slightly increase the pre-heat filament current.
- Rmin: 27k $\rightarrow$ 27.4k - Slightly increase the phase shift at minimum power.
- Rmax: 30k $\rightarrow$ 24k - Slightly decrease the phase shift at maximum power.

A.2.5 BOM

The dimming ballast, Rev. 2, bill of materials is shown in the table below. Refer to Chapter 3 and to the layout and filament heating notes for changes.

International
IOR Rectifier
7/23/2008, 4:35:05 PM Page 1

IR21592 Bill Of Materials (74 items)
Lamp Type 'T8 32W'
Line Input '80 to 140VAC/300VDC'
Configuration 'Dual lamp parallel/Balance transformer'
Target IC 'IR21592 discrete dimming ballast'

Type	Value	Rating	Tolerance	Reference
Bridge Rectifier	1 A	1000V		BR1
Capacitor	0.33 uF	275VAC		C1
Capacitor	0.1 uF	400V		C2,CDC
Capacitor	0.01 uF	25V		C3,CVCO
Capacitor	0.68 uF	25V		C4
Capacitor	0.47 uF	25V		C5,CVDC
Capacitor	0.1 uF	25V		CBOOT,CMIN,CSD,CVCC1
DC Bus Capacitor	22 uF	350V		CBUS
Capacitor	220 pF	25V		CCS
Capacitor	0.22 uF	100V		CH1,CH2,CH3,CH4
Preheat Time Capacitor	0.27 uF	25V		CPH
Resonant Capacitor	0.01 uF	1500V	5%	CRES
Capacitor	1.5 nF	630V		CSNUB
Capacitor	4.7 uF	25V		CVCC2
Y Capacitor	2.2 nF	250VAC		CY
Diode	1N4148			D1,DCP2
Fast Recovery Diode	600 V	1A		DBOOT
Diode	17 V			DCP1
PFC Diode	600 V	1A		DPFC
Fuse	2 A	250VAC		F1
Ballast Control IC	IR21592			IC BALLAST
PFC IC	L6561			IC PFC
Common-mode Line Filter	2x5.1mH	0.8A		L1
Balance Transformer	2x10mH			LBALANCE
PFC Inductor	400 uH	2.9 Apk	5%	LPFC:A
Secondary Winding	10 Turns			LPFC:B
Resonant Inductor	1.2 mH	3.0 Apk	5%	LRES:A
Secondary Windings	5 Turns			LRES1:B,LRES1:C,LRES2:B,LRES2:C
Half-Bridge MOSFET	IRF730			MHS,MLS
PFC MOSFET	IRF740			MPFC
Resistor	820 KOhm	200V		R1,R2,R3,R4
Resistor	100 KOhm			R5,RDC
Resistor	22 KOhm			R6
Resistor	20 Ohm			R7
Resistor	13.78 KOhm		1%	RBUS
Current Sense Resistor	0.62 Ohm		1%	RCS
Resistor	5.1 KOhm			RDIM
Resistor	47 KOhm		1%	RFMIN
Resistor	20 Ohm		5%	RHO,RLO
Resistor	24 KOhm		1%	RIPH
Resistor	1 KOhm			RLIM1
Resistor	10 Ohm			RLIM2,RLIM3
Resistor	30 KOhm		1%	RMAX
Resistor	18 KOhm		1%	RMIN
Resistor	9.1 KOhm			RMULT
Resistor	1 M Ohm			RPU1,RPU2
Resistor	0.2 Ohm		1%	RS
Resistor	220 KOhm			RSD1,RSD2
Resistor	270 KOhm	400V		RSUPPLY
Varistor	470 V			RV1
Resistor	1 M Ohm	400V		RVAC
Resistor	130 KOhm			RVDC

Figure A-19: Dimming ballast, Rev.2 bill of materials.

A.2.6 Inductor Specifications

International
IOR Rectifier
7/23/2008, 4:33:59 PM Page 1

LRES Inductor (50%)
Lamp Type 'T8 32W'
Line Input '80 to 140VAC/300VDC'
Configuration 'Dual lamp parallel/Balance transformer'
Target IC 'IR21592 discrete dimming ballast'

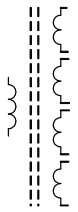
International
IOR Rectifier

INDUCTOR SPECIFICATION
TYPE : LRES(VOLTAGE MODE)

CORE SIZE	P36/22	GAP LENGTH 0.6	mm
BOBBIN	HORIZONTAL		
CORE MATERIAL	Philips 3C85, Siemens N27 or equivalent		
NOMINAL INDUCTANCE	1.2	mH	
MAXIMUM CURRENT	2.6	Apk	
MAXIMUM CORE TEMPERATURE	100	ºC	

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN			54	0.3
CATHODE (1)			5	0.2
CATHODE (2)			5	0.2
CATHODE (3)			5	0.2
CATHODE (4)			5	0.2

ELECTRICAL LAYOUT



PHYSICAL LAYOUT

TEST (TEST FREQUENCY = 50kHz)

MAIN WINDING INDUCTANCE	MIN	mH	MAX	mH
MAIN WINDING RESISTANCE	MIN	Ohms		

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency.

Figure A-20: Dimming ballast, Rev.2 resonant inductor specification.

International
IOR Rectifier
7/23/2008, 4:37:01 PM Page 1

Balance Transformer (50%)
Lamp Type 'T8 32W'
Line Input '80 to 140VAC/300VDC'
Configuration 'Dual lamp parallel/Balance transformer'
Target IC 'IR21592 discrete dimming ballast'

International
IOR Rectifier

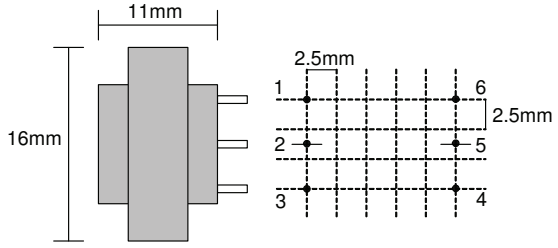
INDUCTOR SPECIFICATION
TYPE : LRES (CURRENT MODE)

CORE SIZE	E16/8/5	GAP LENGTH 0	mm
BOBBIN	HORIZONTAL		
CORE MATERIAL	Philips 3C85, Siemens N27 or equivalent		
MINIMUM INDUCTANCE	1		mH
MAXIMUM CURRENT	0.5		Apk
MAXIMUM CORE TEMPERATURE	100		ºC

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
PRIMARY	1	3	100	0.25
SECONDARY	6	4	100	0.25

ELECTRICAL LAYOUT

PHYSICAL LAYOUT



TEST (TEST FREQUENCY = 50kHz)

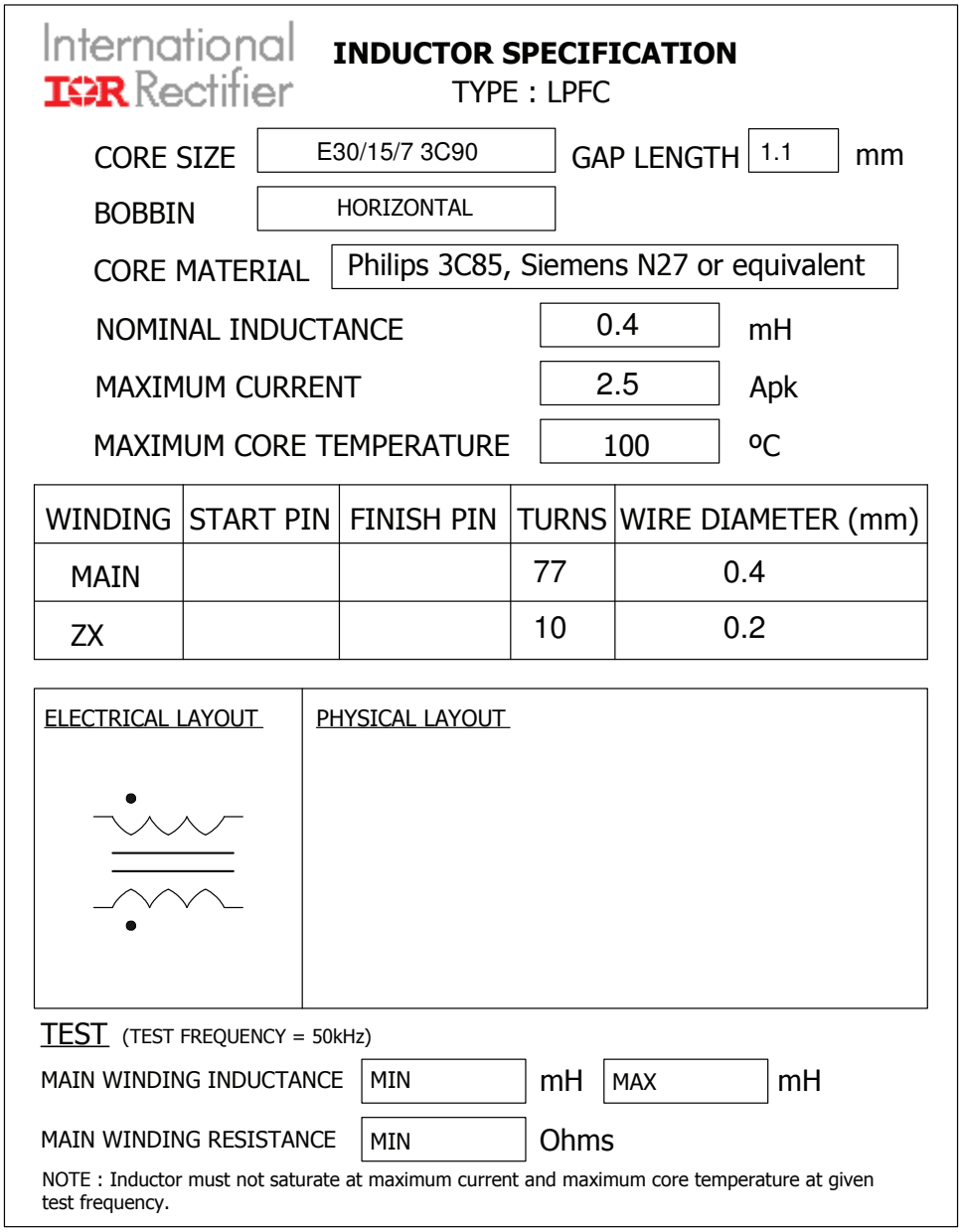
MAIN WINDING INDUCTANCE	MIN	1	mH
MAIN WINDING RESISTANCE	MIN	0.5	Ohms

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency.

Figure A-21: Dimming ballast, Rev.2 current share (balance) transformer specification.

International
IOR Rectifier
7/23/2008, 4:34:35 PM Page 1

LPFC Inductor (50%)
Lamp Type 'T8 32W'
Line Input '80 to 140VAC/300VDC'
Configuration 'Dual lamp parallel/Balance transformer'
Target IC 'IR21592 discrete dimming ballast'



International
IOR Rectifier

INDUCTOR SPECIFICATION

TYPE : LPFC

CORE SIZE	E30/15/7 3C90	GAP LENGTH 1.1	mm
BOBBIN	HORIZONTAL		
CORE MATERIAL	Philips 3C85, Siemens N27 or equivalent		
NOMINAL INDUCTANCE	0.4	mH	
MAXIMUM CURRENT	2.5	Apk	
MAXIMUM CORE TEMPERATURE	100	ºC	

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN			77	0.4
ZX			10	0.2

ELECTRICAL LAYOUT

PHYSICAL LAYOUT

TEST (TEST FREQUENCY = 50kHz)

MAIN WINDING INDUCTANCE	MIN	mH	MAX	mH
MAIN WINDING RESISTANCE	MIN	Ohms		

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency.

Figure A-22: Dimming ballast, Rev.2 power factor correction (pfc) transformer specification.

A.3 Lamp Sensor Software

The PIC microcontroller runs the c program ("operating system") listed in Section A.3.1. The operating system interfaces with MATLAB® through an RS-232 serial connection. An illustrative flow diagram for the operating system is shown in Figure A-23. The flow diagram highlights the handshaking operation of the PIC-MATLAB® interface. Handshaking before each event improves the reliability of the software. The c program is listed in A.3.1. Various "apps" were written as MATLAB® scripts to interface with the lamp sensor. Some useful apps are also listed in this Appendix.

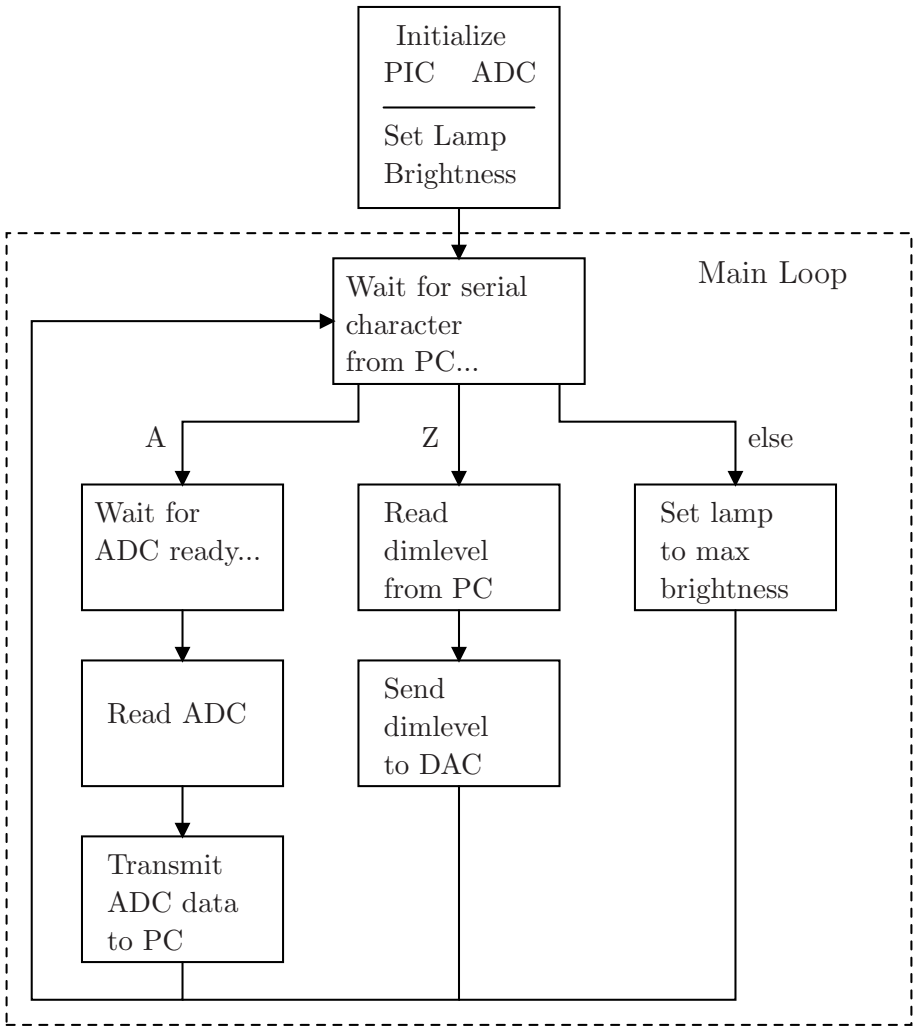


Figure A-23: Flow chart of PIC microcontroller "operating system" listed in A.3.1.

A.3.1 PIC Microcontroller Operating System

`handshakedimmer2.c`

This is the "PIC Operating System." It is programmed into the PIC onboard the lampsensor PCB and interfaces with a PC over a serial (RS-232) port. It also employs some of its output pins with a DAC to control the dimming level of a dimming fluorescent lamp ballast using a signal voltage between 0 and 5 V. The operating system can interface with a PC using simple ASCII character handshaking.

```
#include <pic.h>

//Make sure to change pcc.bat to reflect the correct PIC or you will
//have problems up here!

//Program as regular 8 bit hex or Intel

//ADC Timing Mode is: External Serial Clock, /CS = 0 Operation (2-wire), with SDI
//input speed selection from the PIC on each conversion cycle.  See Fig. 7 in the
//LTC2440 Datasheet.  The PIC shifts in the speed resolution byte on the ADC SDI
//pin while it supplies the serial clock to the SCK pin on the ADC and while it
//shifts in the ADC output data from the ADC SDO pin. See Fig. 4 in the LTC2440
//Datasheet.

__CONFIG(0x3F72);               //No code prot., no debugger, FLASH prog. memory write enabled
                                //no LVP, yes Brown Out Reset, no Watchdog, yes Power up timer
                                //High Speed Oscillator

unsigned char MMSB;
unsigned char NNSB;
unsigned char LLSB;
unsigned char JJSB;
unsigned char MSB;
unsigned char NSB;
unsigned char LSB;
unsigned char SIGN;
unsigned char trash;
unsigned char incoming;
unsigned char status;
int newlinecount;
int i;
int j;
int datapoint;
int dimlevel;

void ReadADC(void);
void WriteUART(unsigned char);
void WriteHex(unsigned char);
void getdatabytes(void);
void transmit(void);
void ftransmit(void);
void delay(void);
void dim5(void);
void dim4(void);
void dim3(void);
void dim2(void);
```

```
void dim1(void);
void getdatapoint(void);
void handshake(void);
void getdimlevel(void);
void setDAC(int);


void Linit(void) {      //Linit just initializes everything and chooses
                        //all of the appropriate options in the mess of
                        //Special Registers.


        TRISA = 0b11110011;     //Use Port A to control and pole ADC,
                                //ADC Busy -> RA1 (input)
                                //Slave Enable -> RA0 (input)
                                //A3 and A2 -> Lsb's for DAC input (outputs)
                                //Watch ADCON registers here and for every
                                //port which has AD input channels!!

        ADCON1 = 0b00000110;    //ADC pins: 00000110 sets all RA's and RE's digital.
                                //Analog input pins must be TRIS = 1.  Also see ADCON0.



        TRISB = 0x00;           //Use Port B on Harsha's Board to control
                                //dimming DAC.


                                //Configure SPI
        TRISC = 0xD0;           //Configure port C: Rx and Tx set (UART);
                                //SDO Output; SDI configured by control reg
                                //as input;
                                //SCK output (Master); RC<2:0> don't care.

        TRISE = 0x00;           //Port E[2:0] is 3 Msb's for DAC input (outputs)


        SSPCON = 0x20;  //Configure Synchronous Serial Port Control Register:
                                //SSPCON<7:6> don't care;
                                //Enable Serial Port mode for SCK, SDO, SDI (and SS);
                                //Idle State for clock is Low;
                                //SPI Master Mode, clock = Fosc/4.

        SSPSTAT = 0x40; //Configure Synchronous Serial Port Status Register:
                                //SMP Sample at middle of data output time
                                //Data transmit on rising edge of SCK.
                                //SSPSTAT<5:0> don't care.

                                //Configure UART
        RCSTA = 0x90;   //Set bit SPEN to configure RX and TX as UART pins.
                                //RCSTA for Async continuos receive enable

        TXSTA = 0x24;   //Configure Transmit register:
                                //Bit 7 don't care (Async); 8-bit transmission;
                                //Transmit enabled; Asynchronous Mode; bit 3 unimp.
                                //High Baud Rate; TXSTA<1:0> don't care.

        SPBRG =71;              //Baud Rate Generator Value = 5 for 115.2kbps
                                //with (11.0592MHz Clock). 71 for 9600

        trash = RCREG;          //Clear Serial Recv interrupt flag
```

```
        RCIF = 0;



}


void main(void) {



        Linit();                        //Initialize PIC and ADC
        dim5();                         //Brighten lamp



while(1){
        handshake();
        if (incoming == 'A')

                {
                while (RA1 == 1)        //Wait for ADC to finish converting
                        continue;
                ReadADC();              //Get the conversion result
                getdatabytes();         //Isolate 24 data bits out of 32
                ftransmit();            //Send the result to serial port
                }

                else if (incoming == 'Z') //If incoming == 'Z' we are going to get
                {                               //a dimming level next.
                getdimlevel();                  //Read the binary dimlevel value
                setDAC(dimlevel);               //Set the DAC input pins
                }

                else                    //If the incoming char was != 'A' or 'Z'
                {
                trash = RCREG;                  //Clear the RCREG
                RCIF = 0;                       //and the interrupt flag
                dim5();                         //brighten lamp to 100%
                }

}



}


////////////////////////////////////////////////////////////////
//subroutines
////////////////////////////////////////////////////////////////

void setDAC(int DAC) {                  //Sets the leftover PIC pins
                RE2 = (DAC >> 7) &0x01; //to correctly control the DAC
                RE1 = (DAC >> 6) &0x01;
                RE0 = (DAC >> 5) &0x01;
                RC2 = (DAC >> 4) &0x01;
                RC1 = (DAC >> 3) &0x01;
                RC0 = (DAC >> 2) &0x01;
                RA3 = (DAC >> 1) &0x01;
                RA2 = DAC &0x01;
```

```
                        }

void getdimlevel(void) {                //Reads a binary value from the serial port
        while (RCIF == 0)
                continue;
        dimlevel = RCREG;
}

void handshake(void) {                  //Reads a character from the serial port
        while (RCIF == 0)
                continue;
        incoming = RCREG;
}

void dim5(void) {               //saw Ballast dim 4.98V 3/13/08

                PORTE = 0x07;
                RC2 = 0;

                RC1 = 1;
                RC0 = 1;
                RA3 = 1;
                RA2 = 1;
                }

void dim4(void) {
                PORTE = 0x06;   //Saw Ballast dim 3.97 3/13/08
                RC2 = 0;

                RC1 = 0;
                RC0 = 1;
                RA3 = 0;
                RA2 = 0;
                }

void dim3(void) {               //Saw Ballast dim 3.02 3/13/08
                PORTE = 0x04;
                RC2 = 1;

                RC1 = 0;
                RC0 = 1;
                RA3 = 1;
                RA2 = 0;
                }

void dim2(void) {
                PORTE = 0x03;   //Saw Ballast dim 2.02 3/13/08
                RC2 = 0;

                RC1 = 0;
                RC0 = 1;
                RA3 = 0;
                RA2 = 0;
                }

void dim1(void) {               //Saw Ballast dim 1.26V 3/13/08
                                //Desire > 1V

                PORTE = 0x01;
                RC2 = 1;
```

```
                RC1 = 1;
                RC0 = 1;
                RA3 = 0;
                RA2 = 0;
                }


void delay(void) {

        i = 0;
        while(i<500)    {

                j = 0;
                while (j<1000) {
                        j = j+1;
                        continue;
                                }
        i = i+1;
        continue;
                        }
}




void transmit(void) {           //Transmit MSB, then NSB, then LSB

                                                //Play with delimiting characters here
                WriteUART(MSB);
                WriteUART(NSB);
                WriteUART(LSB);
                WriteUART(SIGN);
                WriteUART(0);           //Delimit with a zero.

}

void ftransmit(void) {          //Transmit MSB, then NSB, then LSB
                                        //Play with delimiting characters here
                WriteHex(MSB);
                WriteUART('\n');
                WriteHex(NSB);
                WriteUART('\n');
                WriteHex(LSB);
                WriteUART('\n');
                WriteHex(SIGN);
                WriteUART('\n');

}

//////////////

void ReadADC(void) {
        int SampRateByte = 0x48; //This is the value we will write to SSPBUF to initiate
                                        //transmission and also to send to the SDI pin on the ADC
                                        //in order to program the sampling rate as follows:
                                        //0x08 = 3.52kHz, 0x10 = 1.76kHz, 0x00 = 880Hz, 0x18 = 880Hz
                                        //0x20 = 440Hz, 0x28 = 220Hz, 0x30 = 110Hz, 0x38 = 55Hz
                                        //0x40 = 27.5Hz, 0x48 = 13.75Hz, 0x78 = 6.875Hz

        SSPBUF = SampRateByte;  //Write to SSPBUF to initiate transmission.
                                        //The Value written to SSPBUF outputs to the ADC's SDI pin
```

```
                                        //and programs the sample rate.
                                        //SCK is output to ADC

        while (STAT_BF == 0)    //Wait till Buffer is full
                continue;

        MMSB = SSPBUF;          //8 of 32 in MSB


        SSPBUF = SampRateByte;          //next byte
        while (STAT_BF == 0)
                continue;
        NNSB = SSPBUF;          //9-16 in NSB


        SSPBUF = SampRateByte;          //next byte
        while (STAT_BF == 0)
                continue;
        LLSB = SSPBUF;          //17-24 in LSB


        SSPBUF = SampRateByte;          //Let the ADC finish so it can
        while (STAT_BF == 0)    //start the next cycle.
                continue;
        JJSB = SSPBUF;

                                        //I leave it as an exercise to the reader to figure out why
//      SSPBUF = SampRateByte;          //I needed this extra one in order to
//      while (STAT_BF == 0)    //get it working.
//              continue;
}                                       //back to main with MMSB, NNSB and LLSB

//////////////////////

const char hexlookup[] = "0123456789ABCDEF";    //Array for bin to hex conversion

void WriteHex(unsigned char x)                  //Convert from bin to hex and write
{                                                       //to the UART
        WriteUART(hexlookup[x >> 4]);
        WriteUART(hexlookup[x & 0x0f]);
}

//////////////////////

void WriteUART(unsigned char transmitchar) {    //Just write to the UART.
        while(!TXIF)                                    //Wait until last transmit is done
                continue;
        TXREG = transmitchar;                           //Write to TXREG which initiates
}                                                       //transmission

//////////////////////

void getdatabytes(void) {               //Get 24 data bits amongst the 32 transmitted bits:
                MSB = (((MMSB << 3) & 0b11111000) + ((NNSB >> 5) & 0b00000111));
                NSB = (((NNSB << 3) & 0b11111000) + ((LLSB >> 5) & 0b00000111));
                LSB = (((LLSB << 3) & 0b11111000) + ((JJSB >> 5) & 0b00000111));
                SIGN = ((MMSB >> 5) & 0b00000001);
}
```

A.3.2 Matlab® Sensing and Real-time Measurements

`dimmerdemo2.m`

This script oversees a demonstration of occupancy sensing for a system that can also control the lamp power level (dimming level).

```
o%% A lamp sensor demo.  You can specify a dimming level with a
%% continuous value between 1 and 5.  Uses plotdimmer.m.  Works with
%% handshakedimmer2.c.

function y = dimmerdemo2(ref,points,dimlevel)
clear figure

%% Check the arguments
if (nargin ~=3)
    disp('Usage: dimmerdemo2(reference voltage, points per frame, ...
    dim level (1-5))')
    return
else

    %% Define Globals
    gomaster = 'A';
    stopmaster = 'B';
    dimcommand = 'Z';
    linewidth = 2;
    figure(2);
    format long;
    printbuf = zeros(1,points);     %Initialize the prinbuffer to zeros.
    event = ([]);                   %Initialize the event buffer
    STATUS = 0;LAST_EVENT = 0;      %Some variables
    calibrate = ([]);               %Autocalibrate the output plot scale
    collected = [];
    matrix = [];
    ports=instrfind;

%% Initialize some things
    event = ([]);                   %Initialize the event buffer
    STATUS = 0;
    LAST_EVENT = 0;
    calibrate = ([]);               %Autocalibrate the output plot scale

%% Check the serial ports and cleanup if needed
    if size(ports,1) > 0
        stopasync(instrfind);
        fclose(instrfind);
        delete(instrfind);
    end

%% Create a serial port object
    s=serial('COM4', 'BaudRate', 9600, 'DataBits', 8, 'Parity', 'none', ...
        'StopBits', 1, 'terminator', 'LF','timeout',2);
    fopen(s);  %Open serial port defined above

%% Adjust dimgain and dimoffset iteratively to calibrate for the gain and
%% offset in order to achieve dimlevel[1:5] corresponding to DAC output
%% [1:5]V.
    dimgain = 0.745;
    dimoffset = 255*(1-0.058)/5;
```

```
    %Map 1-5 value onto 0-255 binary output value:
    dimlevel = dimlevel - 1;         %1-5 -> 0-4
    dimlevel = (dimlevel/4)*255;     %0-4 -> 0-255
    dimlevel = dimlevel*dimgain;     %correct gain error
    dimlevel = dimlevel+dimoffset;   %correct offset (error)

    %% Set the initial dimming level
    fprintf(s,'%c',dimcommand);
    fwrite(s,dimlevel);

    %% Measure the noise-floor to calibrate plot scales, event detection
    while(length(calibrate))<50
        collected = [];
        matrix = [];
        fprintf(s,'%c',gomaster);
        for i=1:4                %Collect 4 bytes from the ADC
            collected = (fscanf(s,'%x'));
            matrix = horzcat(matrix, collected);
        end
        MSB = (2^16)*matrix(1);NSB = (2^8)*matrix(2);LSB = ...
            matrix(3);SIGN = matrix(4);
        if SIGN==0
            datapoint = -(16777215-(MSB+NSB+LSB));
        else
            datapoint = MSB+NSB+LSB;
        end
        calibrate = horzcat(calibrate, datapoint*(1/16777215));
        STATUS = 'Calibrating'
    end
    calibrate = calibrate(35:length(calibrate));
    minscale = 1.8*(max(calibrate)-min(calibrate))*ref;

%% The Main Loop
    while(1)
        %Stop the loop if you press q
        if strcmp(get(2,'currentcharacter'),'q')
            % Close and wrap up the serial port
            close(2)
            stopasync(s);
            fclose(s);
            delete(s);
            clear s;
            save printbuf;
            break
        end
        % The "Plot Helper" script
        plotdimmer
    end
end
```

`plotdimmer.m`

This script "helps" the demonstration script, `dimmerdemo2.m`, by plotting a single data point and also computing signal characteristics, e.g. time-domain windowed noise, and identifying events in the sensor output e.g. movement of an occupant into or out of the detection field.

```
%% A sub-script that collects data from the lamp sensor, plots it,
%% interprets it as events, etc.

%% Initialize some variables
collected = [];
matrix = [];

%% Collect the data point!
fprintf(s,'%c',gomaster);
for i=1:4               %Collect 4 bytes from the ADC
    collected = (fscanf(s,'%x'));
    matrix = horzcat(matrix, collected);
end

%% Translate the 4 data bytes into a signed integer
MSB = (2^16)*matrix(1);NSB = (2^8)*matrix(2);LSB = matrix(3);...
    SIGN = matrix(4);

if SIGN==0
    datapoint = -(16777215-(MSB+NSB+LSB));
else
    datapoint = MSB+NSB+LSB;
end
%Output datapoint has units Volts
datapoint = ref*datapoint/16777215;

%% Shift the new data pt. in, the last data pt. out for a "rolling plot"
printbuf = horzcat(printbuf(2:points), datapoint);

%% Real-time Signal Characteristics, e.g. Noise
format short
% Compute the total deviation in a window of data
VRANGE = (max(printbuf)-min(printbuf));
% Compute the average in the same window of data
AVG = sum(printbuf)/(points);
% Compute the rms voltage about the average: This is a useful indication of
% noise in the time-domain when there is NO detection
VACrms_uV = (((1/points)*sum((printbuf-AVG).*(printbuf-AVG)))^0.5)/(1e-6)

%% Plotting
% Upper plot: auto-zooming, centered on the data
subplot(3,1,1)          %This window will auto scale unless the deviations
%are less than some value "minscale"

fixedscale = 2*ref*1e-2;      %Set up the fixed scale window
% Middle plot: Fixed Scale, centered on zero
subplot(3,1,2)
plot(printbuf, 'Linewidth', linewidth)
axis ([1 points -fixedscale fixedscale ]);
ylabel('Volts')
```

```
%% Event Detection:
%% For the final plot, we will need to know if there is currently an "Event"
%Use the total deviation in the window to indicate an "Event"
%If there is no event, zoom in to the minimum scale on the upper plot
if VRANGE < minscale
    plot(printbuf, 'Linewidth', linewidth)
    axis([1 points (min(printbuf) - minscale) (max(printbuf) + minscale)]);
    ylabel('Volts')
    STATUS = 'Quiet "shhhhhh"';
    %Event display starts here:
    %If Vrange is small and the length of the event is small, there is no
    %event ongoing and any event that happened was insignificant: reset the
    %event vector
    if length(event) < 6
        %If the window is not auto scaled
        event = ([]);
    else
        %If there has been an event long enough in duration then plot it
        subplot(3,1,3)          %In the bottom plot
        %Get some values to help plot the event history
        length_event = length(event);
         %These 4 values can be used to determine direction of travel
        event_left = event(1:floor(0.5*length_event));
        avg_event_left = (sum(event_left))/length(event_left);
        event_right = event(ceil(0.5*length_event):length_event);
        avg_event_right = (sum(event_right))/length(event_right);
        %Make bookends for the plot history
        bookend_length = floor(0.3*length_event);
        avgevent = (sum(event(1:length_event)))/(length_event);
        %Glue the bookends onto the event
        event = horzcat((ones(1,bookend_length)).*avgevent,...
            event,(ones(1,bookend_length)).*avgevent);
        %Plot the whole event in red in the last window
        plot(event, 'r', 'linewidth', linewidth)
        %Identify direction of travel
        if avg_event_left < avg_event_right,
            LAST_EVENT = 'Left to Right';
        else
            LAST_EVENT = 'Right to Left';
        end
        axis auto;              %Auto scale the event window
        ylabel('Volts')
        event = ([]);           %reset the event vector
    %Event display ends here
    end
else
    %If there is an event on-going, autoscale the upper plot and continue.
    plot(printbuf, 'linewidth', linewidth)
    axis auto;
    ylabel('Volts')
    %And collect the event data points
    event = horzcat(event(1:(length(event))), datapoint);
    %Also print 'Event'
    STATUS = 'Event';
end
% Drawnow
drawnow
```

A.3.3 Matlab® Time-domain Windowed Noise Measurements

`noisedatplot.m`

This script takes time-domain data from the lamp sensor and computes a windowed noise measurement. It averages the rms noise levels from several finite-length windows to get an estimate of the noise floor.

```
%% This script measure and computes time-domain windowed noise data.
%% Each window (frame) is a fixed number of points long.
function y = noisedataplot2(frames, points, datarate, dimlevel)
clear figure

%% Check the arguments
if (nargin ~=4)
    disp('Usage: dataplot(no. of frames, points per frame, datarate ...
    (points per second)), dim level 1-5')
    return
else

    %% Initialize some variables
    gomaster = 'A';
    stopmaster = 'B';
    dimcommand = 'Z';
    ref = 5;
    linewidth = 2;
    figure(2);
    format long;
    printbuf = zeros(1,points);     %Initialize the prinbuffer to zeros.
    calibrate = ([]);               %Autocalibrate the output plot scale
    collected = [];
    matrix = [];
    Vacrms = [];
    event = ([]);                   %Initialize the event buffer
    calibrate = ([]);               %Autocalibrate the output plot scale
    STATUS = 0;
    LAST_EVENT = 0;

    %% Check the serial ports and cleanup if needed
    ports=instrfind;
    if size(ports,1) > 0
        stopasync(instrfind);
        fclose(instrfind);
        delete(instrfind);
    end

    %% Open a serial port
    s=serial('COM6', 'BaudRate', 9600, 'DataBits', 8, 'Parity', 'none', ...
        'StopBits', 1, 'terminator', 'LF','timeout',2);
    fopen(s);  %Open serial port defined above

    %Adjust dimgain and dimoffset iteratively to calibrate for the gain and
    %offset in order to achieve dimlevel[1:5] corresponding to
    %DAC output [1:5]V.
    dimgain = 0.76;
    dimoffset = 255*(0.96)/5;
    %Map 1-5 value onto 0-255 binary output value:
    dimlevel = dimlevel - 1;        %1-5 -> 0-4
```

```
dimlevel = (dimlevel/4)*255;     %0-4 -> 0-255
dimlevel = dimlevel*dimgain;     %correct gain error
dimlevel = dimlevel+dimoffset;   %correct offset (error)

%% Set the intial dim level
fprintf(s,'%c',dimcommand);
fwrite(s,dimlevel);

%% Measure the noise floor for calibrating the plot window
while(length(calibrate)<40)
    collected = [];
    matrix = [];
    fprintf(s,'%c',gomaster);    %Tell Master PIC to go
    for i=1:4                %Collect 4 bytes from the ADC
        collected = (fscanf(s,'%x'));
        matrix = horzcat(matrix, collected);
    end
    MSB = (2^16)*matrix(1);NSB = (2^8)*matrix(2);LSB = matrix(3);...
        SIGN = matrix(4);
    if SIGN==0
        datapoint = -(16777215-(MSB+NSB+LSB));
    else
        datapoint = MSB+NSB+LSB;
    end
    calibrate = horzcat(calibrate, datapoint*(1/16777215));
    STATUS = 'Calibrating'
end
calibrate = calibrate(20:length(calibrate));
minscale = 1.8*(max(calibrate)-min(calibrate))*ref;
printbuf = ref*calibrate(length(calibrate))*ones(1,points);
pointcount = 0;
framecount = 0;
printbufhistory = [];

%% The Main Loop
while(1)
    if pointcount == points
        printbufhistory = horzcat(printbufhistory, printbuf);
        printbuf = ref*calibrate(length(calibrate))*ones(1,points);
        Vacrms = horzcat(Vacrms,VACrms_uV)
        pointcount = 0;
        framecount = framecount + 1;
    end
    %Stop the loop if data collection is done OR if you press q
    if framecount==frames|strcmp(get(2,'currentcharacter'),'q')
        % Close and wrap up the serial port
        close(2)
        stopasync(s);
        fclose(s);
        delete(s);
        clear s;
    %Save all the data
        Length_of_window_sec = points/(datarate)
        save Length_of_window_sec;
        no_of_windows = frames
        save no_of_windows;
        Dim_level = dimlevel
        save Dim_level;
        Data_rate_Hz = datarate
        save Data_rate_Hz;
        Window_VACrms_uV = Vacrms
```

```
            save Window_VACrms_uV;
            End_to_end_dev_mV = ...
                (printbufhistory(length(printbufhistory))...
                -printbufhistory(1))*1000
            save End_to_end_dev_mV;
            Max_dev_mV = (max(printbufhistory)-min(printbufhistory))*1000
            save Max_dev_mV;
            Avg_Window_VACrms_uV = sum(Vacrms)/length(Vacrms)
            save Avg_Window_VACrms_uV;
            Avg_output_mV =...
                sum(printbufhistory)/length(printbufhistory)*1000
            save Avg_output_mV;
            save Vacrms;
            save printbufhistory;
            save points;
            save frames;

            % Glue all of the frames together into one plot vector
            frameend = [];
            for i = 1:(frames-1)
                frameend = horzcat(length(printbufhistory)...
                    -i*points, frameend);
            end
            save frameend;


            break
        end
        % Plot the data as we go
        noisedataplotroll
        pointcount = pointcount+1;
    end
end
```

A.4 Lamp Sensor Full System Simulation

This appendix presents code and example simulation parameters for the full system simulation of the lamp sensor system.

A.4.1 SPICE Model Output Voltage Extraction

`bash command for extracting data from log files.txt`

This command can be used in a unix command line interface to extract data points from several .log files resulting from several different SPICE simulations. This is useful when performing a SPICE simulation for several discrete occupant positions in the lamp sensor simulation. The simulated output voltage among the SPICE simulations can be tabulated. The result can be plotted as a simulated lamp sensor output voltage.

```
Having saved the unix command extratlogs.sh as an executable in the
directory with the log files do:
>> chmod +x extractlogs.sh
which makes the .sh file executable
then
>> ./extractlogs.sh
and simulatedoutput.txt appears in the directory where the log files are.

then MATLAB:
>> generateplot2

*****************
Unix command in extractlogs.sh:
for i in *log; do echo -n ${i/.log}" "; awk -F '[ =]' '/voutfda/{print $3}'...
$i ; done | tee simulatedoutput.txt
```

Capacitive Model Validation Plotting

`generateplot2.m`

This script generates a model validation plot to compare simulated and measured lamp sensor data.

```
%% This script plots simulated data overlayed on exptal data.  It extracts
%% simulated data from simulatedoutput.txt which is generated by running
%% the following BASH command in the simulation directory having the .log
%% files from the LTSPICE simulations: for i in *log; do echo -n ${i/.log}"
%% "; awk -F '[ =]' '/voutfda/{print $3}' $i ; done | tee
%% simulatedoutput.txt It extracts exptal data from printbuf.mat which is
```

```
%% the output buffer from the dataplot2.m script run with using a lamp
%% sensor.


%% Simulated Data
load simulatedoutput.txt;
simulatedvod = vertcat(flipud(simulatedoutput(1:15,2)),...
    simulatedoutput(16:length(simulatedoutput),2));

%% Experimental Data
load printbuf.mat;
exptalvod = printbuf;

%% Simulated and exptal offsets
simulatedbias = simulatedvod(1);
exptalbias = exptalvod(1);

%% Subtract the offsets
simulatedvod = simulatedvod-simulatedbias;
exptalvod = exptalvod - exptalbias;

%% Initialize horizontal axis vector
x = -3.6:0.2:3.6;

%% Trim the exptal data and x vector so they are the same length as the
%% simulated data.
exptalvod = exptalvod(1:length(simulatedvod));
x = x(1:length(simulatedvod));

%% Plot the data
figure(1)
plot(x,1e3*simulatedvod,'x')
xlim([min(x) max(x)])
hold on; plot(x,1e3*exptalvod,'-.');
legend('Simulated','Measured','Location','Best')
title({'Lampsensor Response to a Passing 1.83 m-tall Occupant';...
    'Lamp Height = 2.58 m, Electrode Spacing = 98 cm, Depth = 14.5 cm';...
    'Simulated floor height (below tile) = -2.5 cm, V_s = 200 V,...
    f_c = 50 kHz';'Floor Earthed, Gnd Earthed'})
xlabel('Occupant distance from center of lamp (m)')
ylabel('Lamp sensor output (mV)')
hold off
```

FastCap® Example list File

`model.lst`

This is an example input (.lst) or "list" file for generating a 3D physical model useful in extracting lumped capacitances to describe the lamp sensor or other capacitive system. The .qui files are each data files (input surfaces) that describe a 3D object. The .lst file determines their geometric position in the 3D space. '+' signs indicate that adjacent conductors are to be lumped as one conductor, i.e. capacitances coupling to the conductors are lumped into one capacitance. The result of this particular .lst file is pictorially depicted in Figure 3-20.

```
*G model.lst
*Syntax is "C objectfile.qui rel.perm xorigin yorigin zorigin"

*Group1
*Upper Left
C halfbulb.qui 1 0.007 0.0575 0

*Group2
*Lower Right
C halfbulb.qui 1 0.612 -0.0825 0

*Group3
*Lower Left
C halfbulb.qui 1 0.007 -0.0825 0

*Group4
*Upper Right
C halfbulb.qui 1 0.612 0.0575 0

*Group5
*Left Electrode .0762 = 3in. 0.1524 = 6 in.
C electrode.qui 1 0.12 -0.127 0.1524
*Group6
*Right Electrode
C electrode.qui 1 1.10 -0.127 0.1524

*Group7: Lamp Case and other conductors that will be earthed
C backplane.qui 1 0 -0.127 -0.07+
C sideplane.qui 1 -0.011 -0.127 -0.07+
C sideplane.qui 1 1.221 -0.127 -0.07+
C middlepart.qui 1 0.03 -0.05 -0.05+
C middlepart.qui 1 0.23 -0.05 -0.05+
C middlepart.qui 1 0.43 -0.05 -0.05+
C middlepart.qui 1 0.63 -0.05 -0.05+
C middlepart.qui 1 0.83 -0.05 -0.05+
C middlepart.qui 1 1.03 -0.05 -0.05+

C fixedlamps.qui 1 -0.47 -1 -0.22+
C fixedlamps.qui 1 1.85 -1 -0.22+
C powerstrip.qui 1 0 -1.2 1.5+
C pipe.qui 1 -2.5 -0.1 -0.45+
C duct.qui 1 1.25 -4.0 -1
```

```
*Group8
*Human Centered when x = 0.61-0.1 = 0.51
*C target.qui 1 0 0 1
C head.qui 1              -1.4              -0.050 0.625+
C torso.qui  1            -1.4              -0.225 0.90+
C legs.qui 1              -1.4              0.024 1.56+
C legs.qui 1              -1.4              -0.15 1.56

*Group9
*Unmovable floating conducting objects: "cabinet" for short
C cabinet.qui 1 -2.1 -1.7 0.4

*Group 10
*Floor or whatever is under the floor
C bigfloorpart.qui 1 -3.5 -0.5 2.48+
C bigfloorpart.qui 1 -3.5 0.0 2.48+
C bigfloorpart.qui 1 -3.0 -0.5 2.48+
C bigfloorpart.qui 1 -3.0 0.0 2.48+

C bigfloorpart.qui 1 3.5 -0.5 2.48+
C bigfloorpart.qui 1 3.5 0.0 2.48+

C bigfloorpart.qui 1 4.0 -0.5 2.48+
C bigfloorpart.qui 1 4.0 0.0 2.48+

C bigfloorpart.qui 1 -2.0 -1.0 2.48+
C bigfloorpart.qui 1 -1.5 -1.0 2.48+
C bigfloorpart.qui 1 -1.0 -1.0 2.48+
C bigfloorpart.qui 1 -0.5 -1.0 2.48+
C bigfloorpart.qui 1 0.0 -1.0 2.48+
C bigfloorpart.qui 1 0.5 -1.0 2.48+
C bigfloorpart.qui 1 1.0 -1.0 2.48+
C bigfloorpart.qui 1 1.5 -1.0 2.48+
C bigfloorpart.qui 1 2.0 -1.0 2.48+

C bigfloorpart.qui 1 -2.5 -1.0 2.48+
C bigfloorpart.qui 1 -2.5 -0.5 2.48+
C bigfloorpart.qui 1 -2.5 0.0 2.48+
C bigfloorpart.qui 1 -2.5 0.5 2.48+

C bigfloorpart.qui 1 2.5 -1.0 2.48+
C bigfloorpart.qui 1 2.5 -0.5 2.48+
C bigfloorpart.qui 1 2.5 0.0 2.48+
C bigfloorpart.qui 1 2.5 0.5 2.48+
C bigfloorpart.qui 1 3.0 -1.0 2.48+
C bigfloorpart.qui 1 3.0 -0.5 2.48+
C bigfloorpart.qui 1 3.0 0.0 2.48+
C bigfloorpart.qui 1 3.0 0.5 2.48+

C bigfloorpart.qui 1 -1.0 -0.5 2.48+
C bigfloorpart.qui 1 -2.0 -0.5 2.48+
C bigfloorpart.qui 1 -1.5 -0.5 2.48+
C bigfloorpart.qui 1 -2.0 0 2.48+
C bigfloorpart.qui 1 -1.5 0 2.48+
C bigfloorpart.qui 1 -1.0 0 2.48+
C bigfloorpart.qui 1 -1.0 0.5 2.48+
C bigfloorpart.qui 1 -1.5 0.5 2.48+
C bigfloorpart.qui 1 -2.0 0.5 2.48+

C bigfloorpart.qui 1 0.5 -0.5 2.48+
```

```
C bigfloorpart.qui 1 -0.5 -0.5 2.48+
C bigfloorpart.qui 1 0 -0.5 2.48+
C bigfloorpart.qui 1 -0.5 0 2.48+
C bigfloorpart.qui 1 0 0 2.48+
C bigfloorpart.qui 1 0.5 0 2.48+
C bigfloorpart.qui 1 0.5 0.5 2.48+
C bigfloorpart.qui 1 0 0.5 2.48+
C bigfloorpart.qui 1 -0.5 0.5 2.48+

C bigfloorpart.qui 1 1.0 -0.5 2.48+
C bigfloorpart.qui 1 1.5 -0.5 2.48+
C bigfloorpart.qui 1 1.0 0 2.48+
C bigfloorpart.qui 1 1.5 0 2.48+
C bigfloorpart.qui 1 2.0 0 2.48+
C bigfloorpart.qui 1 2.0 0.5 2.48+
C bigfloorpart.qui 1 1.5 0.5 2.48+
C bigfloorpart.qui 1 1.0 0.5 2.48+
C bigfloorpart.qui 1 2.0 -0.5 2.48+


C bigfloorpart.qui 1 -2.0 -1.5 2.48+
C bigfloorpart.qui 1 -2.5 -1.5 2.48+
C bigfloorpart.qui 1 -1.5 -1.5 2.48+
C bigfloorpart.qui 1 -2.0 -2.0 2.48+
```

FastCap® Example Input Surfaces

`Input Surfaces.txt`

This is an output screen from a FastCap® simulation summarizing the input surfaces' dimensions and physical placement in the model. It shows distinct groups of conductors. Multiple conductors are combined into one group using the '+' sign notation.

```
Running fastcap 2.0 (18Sep92)
  Input: C:\Documents and Settings\John Cooley\
SPICE Cap Model Simulations Jan and Feb 2010\FastCap
Working Files\temp.lst
  Input surfaces:
   GROUP1
    halfbulb.qui, conductor
      title: '0.6mX0.025mX0.025m cube (n=1 e=0.1)
'
      outer permittivity: 1
      number of panels: 98
      number of extra evaluation points: 0
      translation: (0.007 0.0575 0)
   GROUP2
    electrode.qui, conductor
      title: '0.0254mX0.254mX0.001m cube (n=1 e=0.1)
'
      outer permittivity: 1
      number of panels: 578
      number of extra evaluation points: 0
      translation: (0.127 -0.127 0.1524)
   GROUP3
    backplane.qui, conductor
      title: '1.22mX0.254mX0.01m cube (n=1 e=0.1)
'
      outer permittivity: 1
      number of panels: 302
      number of extra evaluation points: 0
      translation: (0 -0.127 -0.07)
    sideplane.qui, conductor
      title: '0.01mX0.254mX0.1m cube (n=1 e=0.1)
'
      outer permittivity: 1
      number of panels: 74
      number of extra evaluation points: 0
      translation: (-0.011 -0.127 -0.07)
    middlepart.qui, conductor
      title: '0.19mX0.1mX0.08m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 66
      number of extra evaluation points: 0
      translation: (0.03 -0.05 -0.05)
    fixedlamps.qui, conductor
      title: '0.254mX2mX0.05m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 402
      number of extra evaluation points: 0
      translation: (-0.47 -1 -0.22)
```

```
    powerstrip.qui, conductor
      title: '5mX0.05mX0.05m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 1470
      number of extra evaluation points: 0
      translation: (0 -1.2 1.5)
    pipe.qui, conductor
      title: '5mX0.1mX0.1m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 750
      number of extra evaluation points: 0
      translation: (-2.5 -0.1 -0.45)
    duct.qui, conductor
      title: '0.6mX5mX0.5m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 162
      number of extra evaluation points: 0
      translation: (1.25 -4 -1)
  GROUP4
    head.qui, conductor
      title: '0.1mX0.1mX0.2m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 66
      number of extra evaluation points: 0
      translation: (0 -0.05 0.61)
    torso.qui, conductor
      title: '0.1mX0.45mX0.55m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 108
      number of extra evaluation points: 0
      translation: (0 -0.225 0.9)
    legs.qui, conductor
      title: '0.1mX0.127mX0.9m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 150
      number of extra evaluation points: 0
      translation: (0 0.024 1.52)
  GROUP5
    cabinet.qui, conductor
      title: '0.6mX0.5mX2m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 84
      number of extra evaluation points: 0
      translation: (-2.1 -1.7 0.4)
  GROUP6
    bigfloorpart.qui, conductor
      title: '0.48mX0.48mX0.05m cube (n=3 e=0.1)
'
      outer permittivity: 1
      number of panels: 174
      number of extra evaluation points: 0
      translation: (-3.5 -0.5 2.46)
Date: Thu Feb 11 15:28:54 2010
```

A.4.2 Fully Differential Amplifier Circuit Model Netlist

`FDAnetlist.ls`

The following netlist was used in the SPICE simulations to capture the linearized circuit model of the fully-differential front-end amplifier. Refer to Figure 3-25.

```
.param ad = 2.794e6
.param ac = 8771.5
.param Zf = 423e3
.param deltaZf = 0.0
.param delZf = {deltaZf*Zf}
.param Zf1 = {Zf + 0.5*delZf}
.param Zf2 = {Zf - 0.5*delZf}
.param nomZf = {(Zf1+Zf2)/2}
.param Zind = {(2*nomZf/(1+ad))+(ac*delZf/(2*(1+ad)))}
.param Zinc = {0.5*nomZf}

R3FDA N001FDA edp {0.5*Zind}
R4FDA edm N002FDA {0.5*Zind}
R5FDA ecsource ec {Zinc}
Vpdummy + N001FDA 0
Vmdummy - N002FDA 0

Bedp edp ec V = 0.5*(i(vpdummy)+i(vmdummy))*(1/(1+{ad}))*(-0.5*{delZf}
-0.5*{nomZf}*{ac})
Bedm ec edm V = 0.5*(i(vpdummy)+i(vmdummy))*(1/(1+{ad}))*(-0.5*{delZf}
-0.5*{nomZf}*{ac})

Bec ecsource gnd V= -0.5*{delZf}*(i(vpdummy)-i(vmdummy))*0.5

Bvodp vopfda vocfda V = 0.5*(i(vpdummy)+i(vmdummy))*0.5*(-{ad}*{delZf}
+{ac}*{nomZf})/(1+{ad})+(i(vpdummy)-i(vmdummy))*0.5*(2*({ad}/(1+{ad})
)*{nomZf}-{ac}*{delZf}/(2*(1+{ad})))

Bvodm vocfda vomfda V = -0.5*(i(vpdummy)+i(vmdummy))*0.5*(-{ad}*{delZf}
+{ac}*{nomZf})/(1+{ad})+(i(vpdummy)-i(vmdummy))*0.5*(2*({ad}/(1+{ad}))
*{nomZf}-{ac}*{delZf}/(2*(1+{ad})))
Bvoc vocfda gnd V = {Vocm}
```

A.4.3 Full System Simulation SPICE Parameters

`model.ls`

The following SPICE directives and parameters were used in the full system SPICE model of the lamp sensor system. Refer to Figure 3-25.

```
***General Parameters***
.param Vs = 200
.param fcarr = 50e3
.param stoptime = 10/{fcarr}

 ***Signal Source Model****
.param Vstrong = {Vs/2}
.param Vweak = {Vs/4}
.param Vend = {Vweak}
*******************************
.param Vsupp = 6
.param RLP = 10
.param CLP = 1e-6
**********************Results********************
***********************************************
.measure Vout RESULT = avg(V(voutp,voutm)) from 150u to 200u
```

A.4.4 Example Capacitances

capacitances.ls

The following SPICE directives show a tabulation of example capacitances used in the full systems simulation of the lamp sensor. Refer to Figure 3-25.

```
**********Capacitances**********
*****************************************************
**********Vary With target**********
*Left strong to target: 1-8
.param C3 = 300e-15
 *Right strong to target: 2-8
.param C5 = 167e-15
*Left electrode to target: 5-8
.param C9 = 534e-15
 *Right electrode to target: 6-8
.param C10 = 187e-15
*Target to backplane: 7-8
.param C27 = 14300e-15
*Target to cabinet: 9-8
.param C37 = 2511e-15
 *****************************************************
*****************************************************
**********Fixed**********
*Left source to left electrode: 1-5
.param C1 = 477e-15
*Left strong to left weak: 1-3
.param C11 = 126e-15
*Left strong to right strong: 1-2
.param C13 =41e-15
*Left strong to cabinet: 1-9
.param C35 = 56e-15
*Right strong to cabinet: 2-9
.param C39 = 62e-15
*Left weak to cabinet: 3-9
.param C41 = 81e-15
*Right weak to cabinet: 4-9
.param C40 = 53e-15
*Left electrode to cabinet: 5-9
.param C36 = 102e-15
*Right electrode to cabinet: 6-9
.param C38 = 52e-15
*Backplane to cabinet:7-9
.param C42 = 19030e-15
*Left strong to right electrode: 1-6
.param C23 = 27e-15
*Left strong to backplane: 1-7
.param C25 = 30050e-15
*Left electrode to backplane: 5-7
.param C26 = 3086e-15
*Left strong to Right weak: 1-4
.param C33 = 1625e-15
*************************************************
*floor to backplane: 7-10
.param C43 = 79720e-15
*floor to cabinet: 9-10
.param C44 = 121300e-15
*Left strong to floor: 1-10
```

```
.param C14 = 321e-15
*Left electrode to floor: 5-10
.param C15 = 401e-15
*Target to floor: (shoe) 8-10
.param C16 = 42400e-15
**********************************************
*Input Node Capacitance: Measured
.param Cstray = 159e-12
**************************************************

*****************Set by symmetry****************
.param C2 = {C1}
.param C4 = {C3}
.param C6 = {C5}
.param C7 = {C1}
.param C8 = {C7}
.param C12 = {C11}
.param C17 = {C15}
.param C18 = {C14}
.param C19 = {C14}
.param C20 = {C19}
.param C24 = {C23}
.param C28 = {C26}
.param C29 = {C25}
.param C30 = {C25}
.param C31 = {C30}
.param C32 = {C13}
.param C34 = {C33}
**************************************************
```

A.5 Lamp Sensor Practice

This Appendix describes the setup, operation and some practical considerations useful for a working demonstration of the lamp sensor system.

A.5.1 Matlab® Interface and Demonstration

Refer to the code in Appendix A.3.

The PIC microcontroller onboard the lamp sensor is typically programmed with an "Operating System" (see Appendix A.3.1) that will interface with MATLAB® over an RS-232 (serial) connection. Various MATLAB® "applications" were written. Some examples are included in Appendix A.3. A basic demonstration of the behavior of the lamp sensor using one of these apps interfaced with the lamp sensor is depicted in Figure A-24. The plot in Figure A-24 shows data taken from the lamp sensor. The upper two plots show the same real-time data; the top window auto-zooms, while the middle window shows the data in a fixed-scale window. The bottom window shows a history of data corresponding to what MATLAB® thought was a detection or an "event." The data shown in the upper two windows corresponds to an occupant passing from one end to the other of the detection field below the lamp. The event history in the bottom window corresponds to an occupant walking through the detection field in one direction, then immediately reversing and walking back through the detection field in the opposite direction.

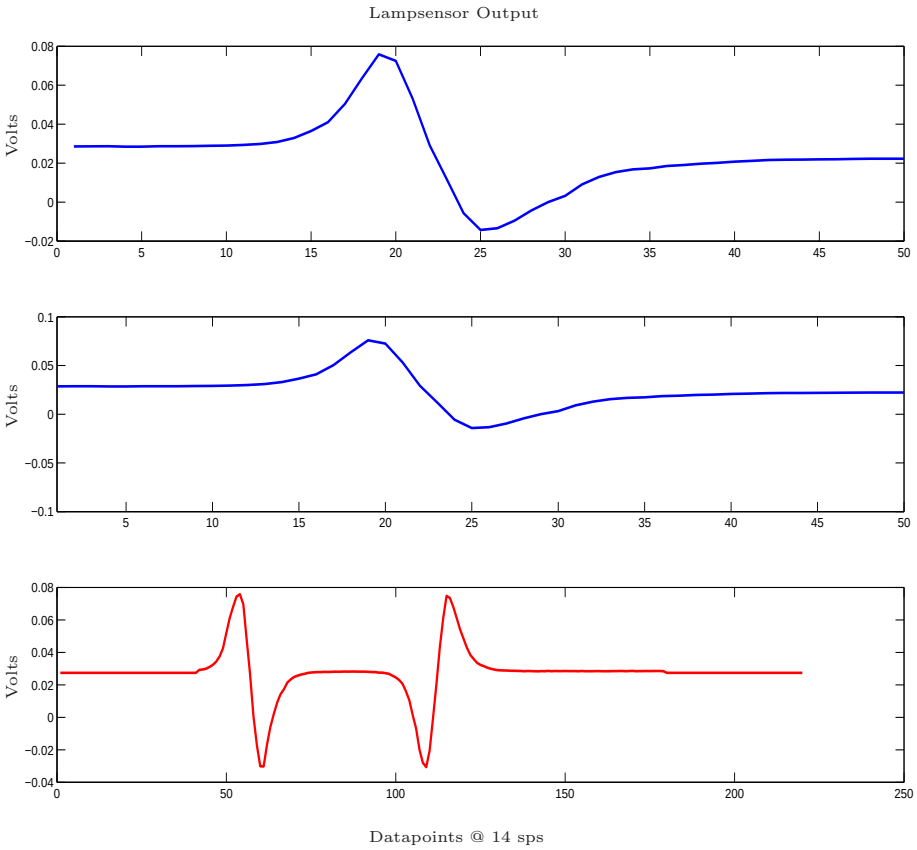


Figure A-24: A screenshot of a MATLAB® demonstration output window showing the lampsensor output voltage. **Top**: auto-zooming window, **Middle**: fixed-scale window, **Bottom**: Event history window

A.5.2 Nulling

The lamp sensor relies on a balanced measurement of the electric fields below the lamp. When there is no detection, the output of the sensor should be approximately "nulled" or zero volts. Imbalances in the system either desired (detections of occupants) or undesired cause the lamp sensor output to deviate from that "null-point."

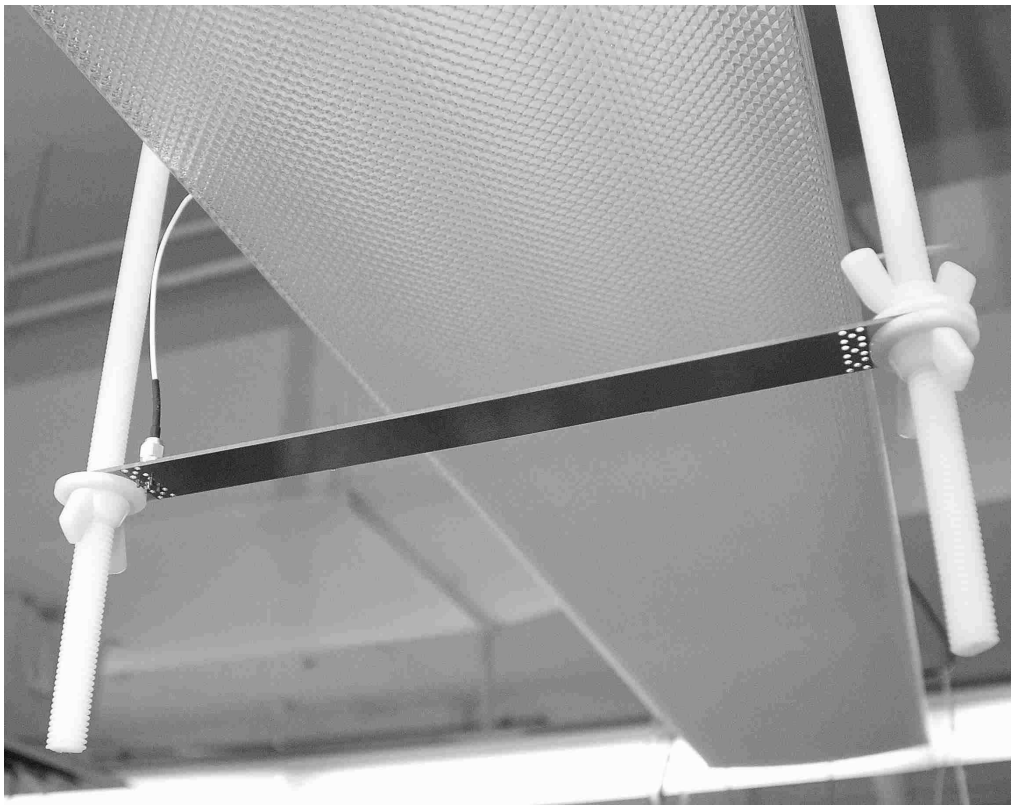


Figure A-25: A photograph of an adjustable electrode

In practice, it is necessary to null the lamp sensor output by adjusting the relative depth of the two electrodes. The adjustable electrode shown in Figure A-25 allows for manual adjustment of the electrode's depth from the lamp. The depth of the electrode in Figure A-25 may be adjusted by turning the nylon wing nuts. Nulling is most easily accomplished by watching the lamp sensor output, e.g. the middle plot of Figure A-24, while adjusting the depth of one of the electrodes. This process is iterative, because the adjuster's hand near the electrode will constitute a strong detection. Therefore, the adjuster should note the offset while out of the detection

field, adjust the electrode depth in one direction and then leave the detection field again to note the change in offset. The electrode depth can then be adjusted in the appropriate direction to reduce the offset toward zero volts.

A.5.3 Grounding, Stray Current Return Paths, and Safety Isolation

The lamp sensor is a quasistatic electric field system. Therefore it relies on closed circuit paths for measurement of the electric fields below the lamp. In general, there may not be explicit return paths between the sensing electronics and the signal source (the lamp). When there is no explicit path, the sensor relies on stray coupling for signal currents to return to the signal source. From experience and observation of the lamp sensor behavior both with and without explicit return paths in place, the stray coupling appears to be both strong and unavoidable. Most notably, the phase reference amplifier is SE, so that currents must return via the sensor power supply ground for that measurement to take place. The phase reference signal is largely unaffected by the presence or lack of an explicit return path.

For experimental or other purposes, it may be necessary to provide an explicit current return path from the sensor electronics to the signal source. Ultimately, this requires the direct connection (short circuit or jumper wire) between the sensor power supply ground ("gnd") and the lamp ballast ground ("common"). Care must be taken however, because gnd will typically also be connected to earth ground ("earth"). Because earth is normally tied directly to the utility neutral wire, that earth connection also comprises a neutral connection. Therefore, tying gnd to common also ties earth and therefore neutral to those references. This is a problem when the power supply for either the sensor electronics or the ballast is not isolated from the utility. In that case, the ground derived from the utility will be driven to neutral and to line with a duty cycle determined by the rectifier between the utility and power supply DC bus. Therefore, unisolated grounds are directly connected to line with some duty cycle. Connecting them directly to earth and therefore to neutral effectively shorts

the utility voltage and will draw damaging levels of current through the intervening electronics (usually the rectifier for the unisolated power supply). Even without an explicit earth connection to either power supply, the ground for the serial port is typically earthed at the PC itself. Therefore, this situation is typical and largely unavoidable.

The solution is to ensure that all of the power supplies derived from the utility are isolated with isolation transformers. At the time of this writing, the lamp sensor was typically powered from an isolated commercial power supply, but some revisions of the custom lamp ballast were powered directly from the utility. An off-the-shelf 1:1 60 Hz isolation transformer was typically used to isolate the ballast from the utility in order to accommodate the short circuit between gnd and common. Practical configurations of the lamp sensor should ultimately include power supplies that are all isolated.

It is also the case that oscilloscope probe grounds are typically earthed. Therefore, if a ground-referenced scope measurement is to be made on, for instance, an unisolated ballast, that ballast must first be isolated from the utility with an isolation transformer.

A.5.4 Modifying Off-the-shelf Fluorescent Lamps

The lamp sensor is made from a commercially available F32T8 fixture designed for 48-inch T8 bulbs. Phillips Alto-series bulbs are typical in our experimental setups. The original fixture will have a plastic light diffuser panel covering the bulbs. After this is removed, a long metal ballast cover should be visible in the center of the fixture. The bulbs should be seated in plastic connectors known as "Tombstones" at each end of the fixture.

Many modern ballasts are designed for cold-cathode striking, wherein the bulbs are struck without preheating the filaments. In those cases the filaments are heated by the bulb current during normal operation. These sorts of fixtures will have "shunted" tombstones, usually marked with a capital "S" on the back of the package. Each shunted tombstone shorts together the two connections two each filament. In some revisions of the custom lamp ballast, filament heating is necessary for proper op-

eration. For those ballasts, shunted tombstones must be replaced with standard un-shunted tombstones.

To install the lamp sensor electronics, remove the metal ballast cover and the ballast beneath it. In most cases, new holes will need to be drilled in the fixture to properly mount the dimming ballast. An unpopulated ballast PCB can be used as a template for drilling. Once holes have been drilled, the dimming ballast can be mounted using nylon standoffs and screws. Most fixtures will have many knockouts in the backplane and ends of the fixture for running electrical connections between the ballast and other boards. If the necessary electronics for the lamp sensor cannot fit beneath the ballast cover, an electrical project box can be bolted onto the opposite side of the backplane. Alternatively, electronics can simply rest outside the fixture if the fixture is mounted on a workbench for experimental purposes. In either case, it is recommended that the electronics be enclosed in a metal box and that the enclosure be connected to the power supply ground for the electronics.

A.5.5 Programming the PIC Microcontroller

Programming the lamp sensor board PIC microcontroller can be accomplished with the MICROCHIP®'s MPLAB software. A photograph of the lamp sensor board connected to the MPLAB programmer is shown in Figure A-26. A photograph showing the MPLab connector for the lamp sensor is shown in Figure A-27.

Programming Notes:

- **The MPLab in-circuit programmer pin-out for the lamp sensor PCB through Rev 2 is different from the standard pin-out for MPLab in-circuit programmers. Two lines must be crossed from the modular connector to the PCB's Molex connector. Refer to the MPLab connector pinout and the lamp sensor PCB and schematics in this Appendix.**
- Do power board during in circuit programming.
- Use Hi-Tech PICC to compile pic code. (.c→.hex)

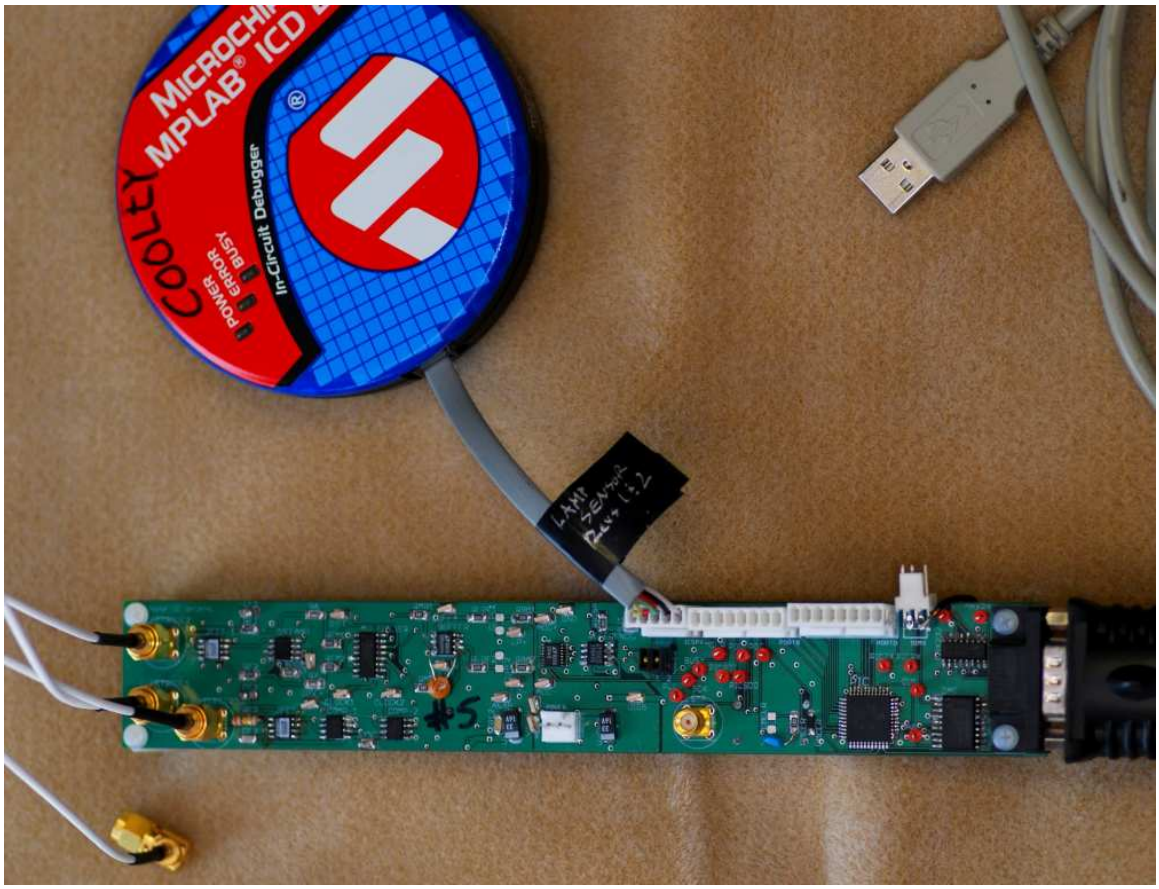


Figure A-26: A photograph of the MPLab ICD 2 programmer puck connected to the lamp sensor board

- Use MPlab software to program pic. (.hex→onto PIC)
- Jumpers on ICSP jumper headers should be in place so that the pins are shorted together top to bottom in two columns. These jumpers allow port pins B7 and B8 to be disconnected from the ICSP Molex if desired in the future.
- The color code for the MPLab connector pin-out is shown in the Table below.
- Note that the blue line is not connected to anything inside the programmer so it is not used.

With MPLAB and the proper USB drivers for the MPLAB ICD 2 programmer puck installed, the programming procedure is as follows:

1. Connect the ICD 2 programmer puck to the PC USB port.

Signal	Color
VPP/MCLR	white
VDD	black
PGD	green
GND	red
PGC	yellow

Table A.2: MPLab connector pin-out color code.

2. Connect the programmer dongle (molex) to the five-pin programming header on the senor board.

3. Open MPLAB and the source code file or hex file.

4. Under the "Programmer" menu, go to "Programmer" and select MPLAB ICD 2.

5. Under the "Configure" menu, click "Select Device..." and select the PIC16F877PT.

6. If necessary, click the "BUILD" button to compile the code to generate a .hex file from the .c file. This .hex file is what is actually copied into the program memory of the PIC.

7. Under the "Programmer" menu, click "Connect to Programmer"

8. Under the "Programmer" menu, click "Program"

A.5.6 Required PCB Cleaning

If the sensor output appears unusually noisy, then noise or unwanted signals are likely coupling from the power supply to the input nodes before the front-end amplifier through flux residue and other oils on the PCB surface. This problem results from the fact that the front-end amplifier is specifically designed to measure very small currents, which is an otherwise desirable and intentional design feature. A good scrubbing with isopropanol followed by a rinse in distilled water (available on tap in building 13, 2nd floor) has been shown to consistently and significantly resolve this

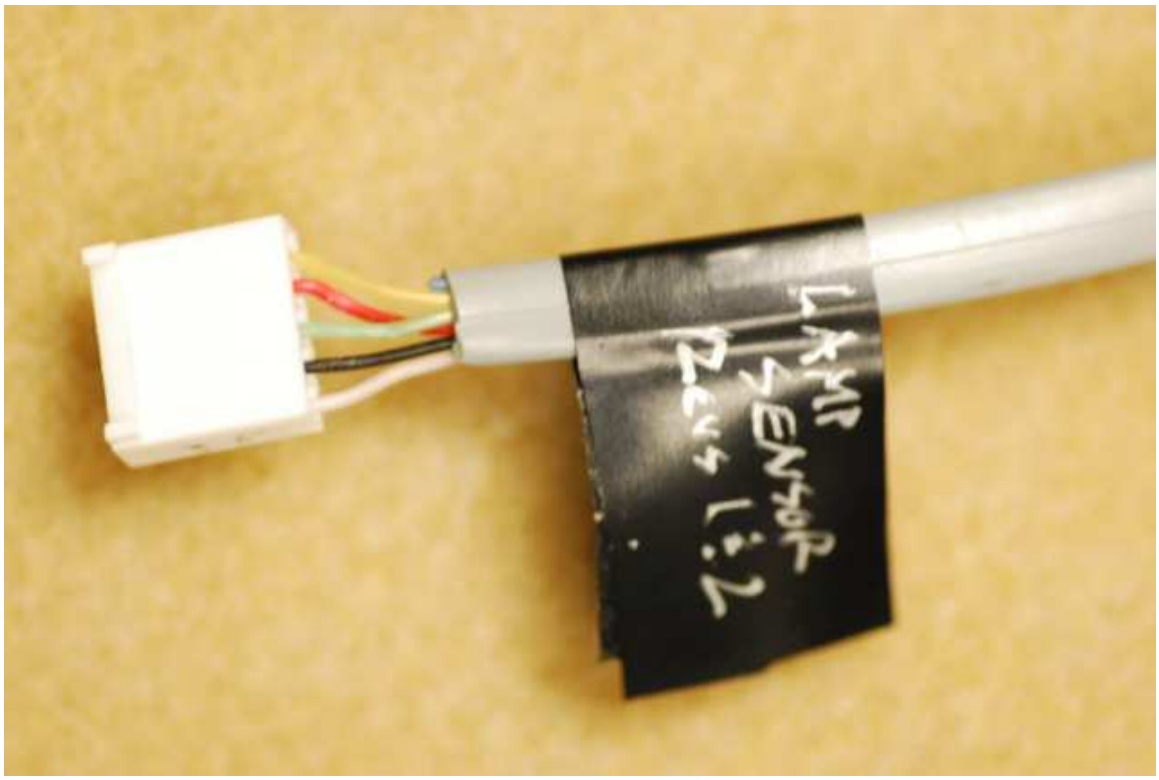


Figure A-27: A photograph of the MPLab ICD 2 connector used for the lamp sensor revisions 1 and 2.

issue. You can either bake the PCB at low temperature, or use a heat gun to dry it.

- Dan Vickery

A.6 Standalone Sensor Software

This appendix includes MATLAB® code for operating the standalone sensor system. The scripts and functions are largely adapted from similar code that was previously developed for operating the lamp sensor.

A.6.1 Matlab® Detection Pattern Data Collection

`sensormatrix.m`

This script is an augmented version of `dimmerdemo2.m`. It has an option to collect a grid of data from the lamp sensor. `sensormatrix.m` requires functions:

- `collectgrid.m`
- `getdatapoint.m`
- `plothelper.m`

```
%% Sensormatrix.m is pretty much the same as standalone, except pressing
%% "m" having selected the plot window will start the grid data collection
%% mode.
function y = sensormatrix(points,port,grid_dimensionx, grid_dimensiony)
%% Clear environment
close all
clc

%% Check arguments
if (nargin ~=4)
    disp('Usage: sensormatrix(points per frame, COM port, grid x dim., grid y dim.)')
    return
end

%% Initialize some global variables
ref = 5;
figure(2);
linewidth = 2;
format long;
printbuf = zeros(1,points);     %Initialize the prinbuffer to zeros.
STATUS = 0;LAST_EVENT = 0;
gomaster = 'A';
stopmaster = 'B';
calibrationlength = 20;

%% Initialize some arrays
event = ([]);                   %Initialize the event buffer
calibrate = ([]);               %Autocalibrate the output plot scale
collected = [];
matrix = [];
```

```
%% COM Port Handling
portstr = int2str(port);        %Convert COM Port arg to string
ports=instrfind;

% Close all open serial ports
if size(ports,1) > 0
    stopasync(instrfind);
    fclose(instrfind);
    delete(instrfind);
end

% Determine Serial Port Path (Platform-Specific):
if ismac == 1
    serial_path = '/dev/tty.usbserial';
elseif isunix == 1
    serial_path = '/dev/TTYUSB0';
elseif ispc == 1
    %Create proper serial path with port arg
    serial_path = strcat('COM',portstr);
else
    disp('Cannot figure out serial port path.  ...Plese edit the .m file manually.');
    return;
end

% Define the serial port
s=serial(serial_path, 'BaudRate', 9600, 'DataBits', ...
    8, 'Parity', 'none', 'StopBits', 1, 'terminator', 'LF',...
    'timeout',2); % create a serial port object
%Open serial port defined above
fopen(s);

%% Calibration to determine noise floor
while(length(calibrate)) < calibrationlength
    datapoint = getdatapoint(s, gomaster, ref);
    calibrate = horzcat(calibrate, datapoint);
    STATUS = 'Calibrating'
end

calibrate = calibrate(35:length(calibrate));
minscale = 1.8*(max(calibrate)-min(calibrate))*ref;

%% The Main Loop
while(1)

    % if m is pressed, enter data matrix collection mode
    %Enter matrix mode if you press m
    if strcmp(get(2,'currentcharacter'),'m')
        clc
         % The function that prints a grid of deteciton data
        collectgrid(grid_dimensionx, grid_dimensiony, s, gomaster, ref);
        stopasync(s);
        fclose(s);
        delete(s);
        clear s;
        break

    % if q is pressed, quit
    %Stop the loop if you press q
    elseif strcmp(get(2,'currentcharacter'),'q')
        close(2);    % Clean up
```

```
        stopasync(s);
        fclose(s);
        delete(s);
        clear s;
        save printbuf;
        break
    end

    % Otherwise continue to generate the scrolling plot window
    plothelper

end
```

`collectgrid.m`

This function collects sensor data corresponding to a grid of points in the detection field. It displays visual cues on the monitor so that the occupant can operate the experiment alone. Each data point is the time-averaged sensor output voltage for a window that is typically a few seconds in duration.

```
%% Collectgrid.m is the script that gets the grid data.
%% Recall and plot data as follows
%% In the directory where the data is saved:
%% >> load grid_result; surf(X,Y,Z);

function y = collectgrid(grid_dimensionx, grid_dimensiony, s, gomaster, ref)

%% Close the display figure
close all

%% Initialize some arrays
gridlvl = [];
datapts=[];

%% Intialize some variables
dataptlength = 30;
x_scale = 9/12; % feet per step
y_scale = 9/12; % feet per step

%% Display Start
f1 = figure(1);
display('Move to first point on grid.')
uicontrol(f1,'Style','Text','String','1','FontSize',94,'units',...
    'Normalized','Position',[0 .5 1 .4])
uicontrol(f1,'backgroundcolor',[0 1 0],'units','Normalized',...
    'Position',[0 0 1 .2])
pause(2);

%% The data collection loop
%iterate for all points on a grid x grid matrix
while(length(gridlvl)) < grid_dimensionx*grid_dimensiony
    % Display instruction to user
    display(['Stand Still! point: ', num2str(length(gridlvl)+1), '/', ...
        num2str(grid_dimensionx*grid_dimensiony)])
    uicontrol(f1,'Style','Text','String',num2str(length(gridlvl)+1),...
        'FontSize',94,'units','Normalized','Position',[0 .5 1 .4])
    uicontrol(f1,'Style','Text','String','Stand Still','FontSize',60...
    ,'units','Normalized','Position',[0 .25 1 .2])
    uicontrol(f1,'backgroundcolor',[1 0 0],'units','Normalized',...
        'Position',[0 0 1 .2])
    pause(1);

    %collect dataptlength samples of data at one point on grid
    for j=1:dataptlength
        j
        %collect data point from the sensor
        datapoint = getdatapoint(s, gomaster, ref);
        datapts = horzcat(datapts, datapoint);
    end

    meanvalue = mean(datapts); % time average the data at one point on grid
```

```
    display(['I recorded ', num2str(1000*meanvalue) ' mV']);
    display('');
    beep()
    gridlvl = horzcat(gridlvl, meanvalue); % Concatenate onto the results array
    if length(gridlvl) < grid_dimensionx*grid_dimensiony
        display('Move to next point on grid') % Display instruction to user
        uicontrol(f1,'Style','Text','String','Move.','FontSize',60,...
            'units','Normalized','Position',[0 .25 1 .2])
        uicontrol(f1,'backgroundcolor',[0 1 0],'units','Normalized',...
            'Position',[0 0 1 .2])
        if mod((length(gridlvl)),grid_dimensionx) == 0  % Time delay
            pause(4); % Greater time delay if at the end of a grid row.
        else
            pause(2); % Short time delay between points.
        end
    end
%     clc
    datapts = [];   % reset the results array
end

%% Display Done
display('Data collection done.')
close(f1)

%% Center the results
gridlvl = gridlvl-1.00001*max(gridlvl);

%% Format vector into matrix
grid_result = [];
for i = 1:grid_dimensiony
    x_result = [];
    for j = 1:grid_dimensionx
        x_result = horzcat(x_result, gridlvl(1));
        gridlvl = gridlvl(2:length(gridlvl));
    end
    grid_result = vertcat(grid_result, x_result);
end

%% Plotting
figure(3)
[X,Y] = meshgrid(1:grid_dimensionx, 1:grid_dimensiony);
X = X.*x_scale;
Y = Y.*y_scale;
Z = grid_result;
surf(X,Y,Z);
% surf(X,Y,20*log10(abs(Z)));

%% Plot Formatting
title('');
xlabel('x Position (ft.)');
ylabel('y Position (ft.)');
% zlabel('Response (db mV)');
zlabel('Response (V)');
box

%% Save data
save grid_result

end
```

`getdatapoint.m`

This function polls the lampsensor for a single data point (4 bytes). The same code is incorporated directly in other scripts, for instance, `plotdimmer.m`.

```
%% This function collects one data byte from the sensor board
function datapoint = getdatapoint(s, gomaster, ref)

%% Initialize some arrays
collected = [];
matrix = [];

%% Send the command to the sensor
fprintf(s,'%c',gomaster);

%% Read the serial port recv buffer four times for four bytes
for k=1:4       %Collect 4 bytes from the ADC
    collected = (fscanf(s,'%x'));
    matrix = horzcat(matrix, collected);
end

%% Translate the 4 data bytes into a signed integer
MSB = (2^16)*matrix(1);NSB = (2^8)*matrix(2);LSB = matrix(3);SIGN = ...
    matrix(4);
if SIGN==0
    datapoint = -(16777215-(MSB+NSB+LSB));
else
    datapoint = MSB+NSB+LSB;
end

%% Return the value of the datapoint in Volts
datapoint = ref*datapoint/16777215;

end
```

`plothelper.m`

This script is similar to `plotdimmer.m`. It calls the `getdatapoint.m` function to poll the lampsensor for a data point instead of incorporating that code directly in the script.

```
%% A sub-script that collects data from the lamp sensor and plots it.

%% Collect the next data point
datapoint = getdatapoint(s, gomaster, ref);

%% Scroll the print buffer
printbuf = horzcat(printbuf(2:points), datapoint);

%% Plotting

%% Fixed Scale (Middle) Window
fixedscale = 2*ref*1e-2;      %Set up the fixed scale window
subplot(3,1,2)          %for the middle plot
plot(printbuf, 'Linewidth', linewidth)
axis ([1 points -fixedscale fixedscale ]);
ylabel('Volts')

%% Auto scale (Top) Window
subplot(3,1,1)
%% Event Detection
format short
VRANGE = (max(printbuf)-min(printbuf));
AVG = sum(printbuf)/(points);
VACrms_uV = (((1/points)*sum((printbuf-AVG).*(printbuf-AVG)))^0.5)/(1e-6)

if VRANGE<minscale   %If there is no event, zoom in to the minimum scale
    plot(printbuf, 'Linewidth', linewidth)
    axis([1 points (min(printbuf) - minscale) (max(printbuf) + minscale)]);
    ylabel('Volts')
    STATUS = 'Quiet "shhhhhh"';
    if length(event) < 6            %%%Event display starts here:
        %If the window is not auto scaled
        event = ([]);               %assume the event is over and print it.
        %But if it's too short don't actually print it (goto end)
    else

        %% Event History (Bottom) Window
        subplot(3,1,3)          %In the bottom plot
        %Get some values to help plot it in a cool way.
        length_event = length(event);
         %These 4 values are for the direction detection
        event_left = event(1:floor(0.5*length_event));
        avg_event_left = (sum(event_left))/length(event_left);
        event_right = event(ceil(0.5*length_event):length_event);
        avg_event_right = (sum(event_right))/length(event_right);
        %Make a bookend for the plot so it looks better
        bookend_length = floor(0.3*length_event);
        avgevent = (sum(event(1:length_event)))/(length_event);
        %Glue the bookends onto the event
        event = horzcat((ones(1,bookend_length)).*avgevent, ...
            event,(ones(1,bookend_length)).*avgevent);

        %plot the whole event in red in the last window
```

```
        plot(event, 'r', 'linewidth', linewidth)
        axis auto;              %Auto scale the event window
        ylabel('Volts')
        event = ([]);           %reset the event vector
    end                             %%%Event display ends here
else
    plot(printbuf, 'linewidth', linewidth)
    axis auto;
    ylabel('Volts')
    %And collect the event data points
    event = horzcat(event(1:(length(event))), datapoint);
    STATUS = 'Event';                                   %Also print 'Event'
end
drawnow
```

A.7 Fully-Differential Amplifier Detailed Derivations

A.7.1 Derivation of Transconductances using the Virtual Short-ckt. Approximation

Refer to Figure 2-6(c).

Definitions:

$$i_{id} \equiv \frac{i_+ - i_-}{2} \qquad i_{ic} \equiv i_+ + i_- \tag{A.1}$$

$$e_d \equiv -i_{ic}\frac{\Delta Z_f + \overline{Z_f}a_c}{2(1+a_d)} \qquad e_c \equiv -i_{id}\frac{\Delta Z_f}{2} \tag{A.2}$$

$$Z_{dm} \equiv Z_1 + Z_2 \qquad Z_{cm} \equiv Z_1||Z_2 + Z_c \tag{A.3}$$

$$Z_d \equiv \left(\frac{2\overline{Z_f} + \frac{1}{2}\Delta Z_f a_c}{(1+a_d)}\right) \qquad Z_c \equiv \left(\frac{\overline{Z_f}}{2}\right) \tag{A.4}$$

$$\Delta Z \equiv Z_1 - Z_2 \qquad \overline{Z} \equiv \frac{(Z_1 + Z_2)}{2} \tag{A.5}$$

$$\Delta Z_f \equiv Z_{f1} - Z_{f2} \qquad \overline{Z_f} \equiv \frac{(Z_{f1} + Z_{f2})}{2} \tag{A.6}$$

$$v'_{sd} \equiv \frac{1}{2}v_{sd} \tag{A.7}$$

Circuit constraints:

$$i_+ = \frac{(v_{sc} + \frac{1}{2}v_{sd} - e_{cc})}{Z_1} \tag{A.8}$$

$$i_- = \frac{(v_{sc} - \frac{1}{2}v_{sd} - e_{cc})}{Z_2} \tag{A.9}$$

$$e_{cc} = e_c + (i_+ i_-)Z_c \tag{A.10}$$

Y_{dd} Derivation:

$$Y_{dd} \equiv \left.\frac{i_{id}}{v_{sd}}\right|_{v_{sc}=0}. \tag{A.11}$$

$$i_+ = \frac{(\frac{1}{2}v_{sd} - e_{cc})}{Z_1} \tag{A.12}$$

$$i_- = \frac{(\frac{1}{2}v_{sd} - e_{cc})}{Z_2}. \tag{A.13}$$

$$\begin{aligned} 2i_{id} &= v'_{sd}\left(\frac{1}{Z_1}+\frac{1}{Z_2}\right) + e_{cc}\left(-\frac{1}{Z_1}+\frac{1}{Z_2}\right) \\ &= v'_{sd}\left(\frac{1}{Z_1||Z_2}\right) + e_{cc}\left(\frac{\Delta Z}{Z_1 Z_2}\right). \end{aligned} \tag{A.14}$$

Also,

$$\begin{aligned} e_{cc} &= e_c + (i_+ + i_-)Z_c \\ &= e_c + \left(\frac{v'_{sd} - e_{cc}}{Z_1} + \frac{-v'_{sd} - e_{cc}}{Z_2}\right) Z_c. \end{aligned} \tag{A.15}$$

so that,

$$e_{cc}\left(1 + \frac{Z_c}{Z_1||Z_2}\right) = -\left(\frac{\Delta Z_f}{2}\right) i_{id} - v'_{sd}\left(\frac{\Delta Z Z_c}{Z_1 Z_2}\right). \tag{A.16}$$

$$e_{cc} = -\left(\frac{\Delta Z_f}{2} i_{id} + v'_{sd}\left(\frac{\Delta Z Z_c}{Z_1 Z_2}\right)\right)\left(\frac{Z_1||Z_2}{Z_1||Z_2 + Z_c}\right). \tag{A.17}$$

Combining (A.14) and (A.17)

$$2i_{id} = v'_{sd}\left(\frac{1}{Z_1||Z_2} - \frac{\Delta Z}{Z_1 Z_2}\frac{\Delta Z Z_c}{Z_1 Z_2}\frac{Z_1||Z_2}{(Z_1||Z_2 + Z_c)}\right) - i_{id}\left(\frac{\Delta Z}{Z_1 Z_2}\frac{\Delta Z_f}{2}\frac{Z_1||Z_2}{(Z_1||Z_2 + Z_c)}\right) \tag{A.18}$$

Collecting terms

$$i_{id}\left(2 + \frac{\Delta Z \Delta Z_f Z_1||Z_2}{2Z_1 Z_2(Z_1||Z_2 + Z_c)}\right) = v'_{sd}\left(\frac{1}{Z_1||Z_2} - \frac{\Delta Z}{Z_1 Z_2}\frac{\Delta Z Z_c Z_1||Z_2}{Z_1 Z_2(Z_1||Z_2 + Z_c)}\right) \tag{A.19}$$

Recall that $v'_{sd} = \frac{1}{2}v_{sd}$. This leads to a numerator:

$$Y_{dd,num} = \frac{1}{Z_1||Z_2} - \frac{\Delta Z^2 Z_c Z_1||Z_2}{Z_1^2 Z_2^2 (Z_1||Z_2 + Z_c)}$$

and a denominator

$$Y_{dd,den} = 4 + \frac{\Delta Z \Delta Z_f Z_1||Z_2}{Z_1 Z_2 (Z_1||Z_2 + Z_c)}.$$

We recognize the quantity $(Z_1||Z_2+Z_c)$ as the impedance seen by a purely CM voltage driving a purely CM input current and rename it Z_{cm}. Then, aiming to eliminate second-order terms from the numerator, we decompose $Z_1||Z_2$ and simplify:

$$Y_{dd,num} = \frac{Z_1 + Z_2}{Z_1 Z_2} - \frac{\Delta Z^2 Z_c}{Z_1 Z_2 (Z_1 + Z_2) Z_{cm}}.$$

Now, recognizing the term $(Z_1 + Z_2)$ as the impedance seen by a purely DM voltage driving a purely DM input current, we rename it Z_{dm}. Identifying Z_{dm} and combining terms in the numerator leads to

$$Y_{dd,num} = \frac{(Z_1 + Z_2) Z_{dm} Z_{cm} - \Delta Z^2 Z_c}{Z_1 Z_2 Z_{dm} Z_{cm}}.$$

Identifying Z_{cm} in the denominator leads to

$$Y_{dd,den} = 4 + \frac{\Delta Z \Delta Z_f Z_1||Z_2}{Z_1 Z_2 Z_{cm}}.$$

Moving $Z_{dm} Z_{cm} Z_1 Z_2$ from the numerator to the denominator leads to

$$\begin{aligned} Y_{dd,num} &= (Z_1 + Z_2) Z_{dm} Z_{cm} - \Delta Z^2 Z_c \\ Y_{dd,den} &= \left(4 + \frac{\Delta Z \Delta Z_f Z_1||Z_2}{Z_1 Z_2 Z_{cm}}\right) Z_{dm} Z_{cm} Z_1 Z_2. \end{aligned}$$

Identifying $Z_1||Z_2/Z_1 Z_2$ as $1/Z_{dm}$ and multiplying the denominator through gives

$$Y_{dd,den} = 4 Z_{dm} Z_{cm} Z_1 Z_2 + Z_1 Z_2 \Delta Z \Delta Z_f.$$

Collecting terms,

$$Y_{dd,den} = Z_1 Z_2 (4 Z_{dm} Z_{cm} + \Delta Z \Delta Z_f).$$

Suspecting a more simple result, we expand the Z_{dm} and Z_{cm} terms in the numerator, temporarily increasing the expression's entropy:

$$Y_{dd,num} = Z_1 Z_1 || Z_2 + 2 Z_1 Z_2 Z_1 || Z_2 + 4 Z_1 Z_2 Z_c + Z_2 Z_1 || Z_2.$$

Dividing common factors and collecting terms leads to

$$\begin{aligned} Y_{dd,num} &= Z_1 + 2 Z_1 Z_2 + Z_2 + 4 Z_c (Z_1 + Z_2) \\ Y_{dd,den} &= (4 Z_{dm} Z_{cm} + \Delta Z \Delta Z_f)(Z_1 + Z_2). \end{aligned}$$

Factoring the numerator and identifying Z_{dm} and Z_{cm} effectively "applies mental energy" to the expression and reduces its entropy [31]:

$$Y_{dd} = \frac{Z_{dm}^2 + 4 Z_c Z_{dm}}{(4 Z_{dm} Z_{cm} + \Delta Z \Delta Z_f)(Z_1 + Z_2)}.$$

Dividing out the common factor of $Z_{dm} = Z_1 + Z_2$ in the numerator and denominator gives

$$Y_{dd} = \frac{Z_{dm} + 4 Z_c}{4 Z_{dm} Z_{cm} + \Delta Z \Delta Z_f},$$

which can be rewritten to match the result in (2.85) using the definitions of Z_{dm} and Z_c in (2.65),

$$\boxed{Y_{dd} = 2 \frac{\overline{Z} + \overline{Z_f}}{4 Z_{dm} Z_{cm} + \Delta Z \Delta Z_f}}.$$

Y_{dc} Derivation:

$$Y_{dc} \equiv \left. \frac{i_{ic}}{v_{sd}} \right|_{v_{sc}=0}. \tag{A.20}$$

$$i_+ = \frac{(\frac{1}{2}v_{sd} - e_{cc})}{Z_1} \tag{A.21}$$

$$i_- = \frac{(\frac{1}{2}v_{sd} - e_{cc})}{Z_2}. \tag{A.22}$$

$$\begin{aligned} i_{ic} &= \left(\frac{v'_{sd} - e_{cc}}{Z_1}\right) - \left(\frac{v'_{sd} - e_{cc}}{Z_2}\right) \\ &= v'_{sd}\left(\frac{1}{Z_1} - \frac{1}{Z_2}\right) - e_{cc}\left(\frac{1}{Z_1} + \frac{1}{Z_2}\right) \\ &= v'_{sd}\left(\frac{-\Delta Z_f}{Z_1 Z_2}\right) - e_{cc}\left(\frac{1}{Z_1||Z_2}\right) \end{aligned} \tag{A.23}$$

Also,

$$\begin{aligned} e_{cc} &= e_c + i_{ic}Z_c \\ &= -\frac{\Delta Z_f}{2}\left(\frac{i_+ - i_-}{2}\right) + i_{ic}Z_c \\ &= -\frac{\Delta Z_f}{2}\frac{1}{2}\left(\frac{v'_{sd} - e_{cc}}{Z_1} + \frac{v'_{sd} + e_{cc}}{Z_2}\right) + i_{ic}Z_c \end{aligned} \tag{A.24}$$

so that,

$$e_{cc}\left(1 - \frac{\Delta Z_f}{4}\frac{1}{Z_1} + \frac{\Delta Z_f}{4}\frac{1}{Z_2}\right) = i_{ic}Z_c - v'_{sd}\frac{\Delta Z_f}{4}\left(\frac{1}{Z_1} + \frac{1}{Z_2}\right) \tag{A.25}$$

and

$$\begin{aligned} e_{cc} &= \left(i_{ic}Z_c - v'_{sd}\frac{\Delta Z_f}{4}\frac{1}{Z_1||Z_2}\right)\left(1 + \frac{\Delta Z_f}{4}\left(\frac{1}{Z_2} - \frac{1}{Z_1}\right)\right)^{-1} \\ &= \left(i_{ic}Z_c - v'_{sd}\frac{\Delta Z_f}{4Z_1||Z_2}\right)\left(\frac{4Z_1Z_2}{4Z_1Z_2 + \Delta Z_f \Delta Z}\right) \end{aligned} \tag{A.26}$$

Combining,

$$\begin{aligned} i_{ic} = v'_{sd}&\left(\frac{-\Delta Z}{Z_1Z_2} + \frac{1}{Z_1||Z_2}\frac{\Delta Z_f}{Z_1||Z_2}\frac{Z_1Z_2}{(4Z_1Z_2 + \Delta Z_f\Delta Z)}\right) \\ &+ i_{ic}\left(\frac{-Z_c}{Z_1||Z_2}\right)\left(\frac{4Z_1Z_2}{4Z_1Z_2 + \Delta Z_f\Delta Z}\right) \end{aligned} \tag{A.27}$$

$$i_{ic}\left(1+\frac{4Z_cZ_1Z_2}{Z_1||Z_2(4Z_1Z_2+\Delta Z_f\Delta Z)}\right)=v'_{sd}\left(-\frac{\Delta Z}{Z_1Z_2}+\frac{\Delta Z_fZ_1Z_2}{(Z_1||Z_2)^2(4Z_1Z_2+\Delta Z_f\Delta Z)}\right) \tag{A.28}$$

Leading to a numerator:

$$Y_{dc,num}=\frac{1}{2}\left(\frac{-\Delta Z}{Z_1Z_2}+\frac{\Delta Z_fZ_1Z_2}{(Z_1||Z_2)^2(4Z_1Z_2+\Delta Z_f\Delta Z)}\right) \tag{A.29}$$

and a denominator:

$$Y_{dc,den}=1+\frac{4Z_cZ_1Z_2}{Z_1||Z_2(4Z_1Z_2+\Delta Z_f\Delta Z)} \tag{A.30}$$

Expanding $Z_1||Z_2$ once, Z_1Z_2 divides out,

$$Y_{dc,num}=\frac{1}{2}\left(\frac{-\Delta Z}{Z_1Z_2}+\frac{\Delta Z_f(Z_1+Z_2)}{(Z_1||Z_2)(4Z_1Z_2+\Delta Z_f\Delta Z)}\right) \tag{A.31}$$

Expanding $Z_1||Z_2$ again in the numerator

$$Y_{dc,num}=\frac{1}{2}\left(\frac{-\Delta Z}{Z_1Z_2}+\frac{\Delta Z_f(Z_1+Z_2)^2}{(Z_1Z_2)(4Z_1Z_2+\Delta Z_f\Delta Z)}\right) \tag{A.32}$$

Expanding $Z_1||Z_2$ once, Z_1Z_2 divides out of the denominator,

$$Y_{dc,den}=1+\frac{4Z_c(Z_1+Z_2)}{(4Z_1Z_2+\Delta Z_f\Delta Z)} \tag{A.33}$$

Combining fractions in the numerator

$$Y_{dc,num}=\frac{1}{2}\left(\frac{\frac{-\Delta Z}{Z_1Z_2}(Z_1Z_2)(4Z_1Z_2+\Delta Z_f\Delta Z)+\Delta Z_f(Z_1+Z_2)^2}{(Z_1Z_2)(4Z_1Z_2+\Delta Z_f\Delta Z)}\right) \tag{A.34}$$

and the denominator

$$Y_{dc,den}=\frac{(4Z_1Z_2+\Delta Z_f\Delta Z)+4Z_c(Z_1+Z_2)}{(4Z_1Z_2+\Delta Z_f\Delta Z)} \tag{A.35}$$

$(4Z_1Z_2 + \Delta Z_f \Delta Z)$ divides out yielding

$$Y_{dc,num} = \frac{1}{2}\left(\frac{\frac{-\Delta Z}{Z_1 Z_2}(Z_1 Z_2)(4Z_1 Z_2 + \Delta Z_f \Delta Z) + \Delta Z_f (Z_1 + Z_2)^2}{(Z_1 Z_2)}\right) \tag{A.36}$$

and

$$Y_{dc,den} = (4Z_1 Z_2 + \Delta Z_f \Delta Z) + 4Z_c(Z_1 + Z_2) \tag{A.37}$$

Replacing $Z_1 Z_2$ with $Z_1||Z_2(Z_1 + Z_2)$ and recognizing $Z_1 + Z_2$ as Z_{dm}, in the denominator yields

$$\begin{aligned} Y_{dc,den} &= 4Z_1||Z_2 Z_{dm} + \Delta Z_f \Delta Z + 4Z_c Z_{dm} \\ &= 4Z_{dm}(Z_1||Z_2 + Z_c) + \Delta Z_f \Delta Z \end{aligned} \tag{A.38}$$

and recognizing $(Z_1||Z_2 + Z_c)$ as Z_{cm} yields

$$Y_{dc,den} = 4Z_{dm} Z_{cm} + \Delta Z_f \Delta Z \tag{A.39}$$

Expanding ΔZ and ΔZ_f in the numerator temporarily increases the expressions entropy

$$Y_{dc,num} = \frac{1}{2}\left(\frac{\frac{Z_2 - Z_1}{Z_1 Z_2}(Z_1 Z_2)(4Z_1 Z_2 + (Z_{f1} - Z_{f2})(Z_1 - Z_2)) + (Z_{f1} - Z_{f2})(Z_1 + Z_2)^2}{(Z_1 Z_2)}\right) \tag{A.40}$$

Expansion and canceling of terms leads to

$$Y_{dc,num} = 2(-\Delta Z + \Delta Z_f) \tag{A.41}$$

and

$$\boxed{Y_{dc} = 2\frac{-\Delta Z + \Delta Z_f}{4Z_{dm} Z_{cm} + \Delta Z_f \Delta Z}} \tag{A.42}$$

Y_{cd} Derivation:

$$Y_{cd} \equiv \left.\frac{i_{id}}{v_{sc}}\right|_{v_{sd}=0}. \tag{A.43}$$

$$i_+ = \frac{(v_{sc} - e_{cc})}{Z_1} \tag{A.44}$$

$$i_- = \frac{(v_{sc} - e_{cc})}{Z_2}. \tag{A.45}$$

$$\begin{aligned} 2i_{id} &= \left(\frac{v_{sc} - e_{cc}}{Z_1}\right) - \left(\frac{v_{sc} - e_{cc}}{Z_2}\right) \\ &= v_{sc}\left(\frac{-\Delta Z_f}{Z_1 Z_2}\right) + e_{cc}\left(\frac{\Delta Z}{Z_1 Z_2}\right) \end{aligned} \tag{A.46}$$

Also,

$$\begin{aligned} e_{cc} &= e_c + (i_+ + i_-)Z_c \\ &= -\left(\frac{\Delta Z_f}{2}\right) i_{id} + (i_+ + i_-)Z_c \\ &= -\left(\frac{\Delta Z_f}{2}\right) i_{id} + \left(\frac{(v_{sc} - e_{cc})}{Z_1} + \frac{(v_{sc} - e_{cc})}{Z_2}\right) Z_c \end{aligned} \tag{A.47}$$

so that,

$$e_{cc}\left(1 + \frac{Z_c}{Z_1||Z_2}\right) = -\left(\frac{\Delta Z_f}{2}\right) i_{id} + v_{sc}\left(\frac{Z_c}{Z_1||Z_2}\right) \tag{A.48}$$

$$e_{cc} = \left(-\frac{\Delta Z_f}{2} i_{id} + v_{sc}\frac{Z_c}{Z_1||Z_2}\right)\left(\frac{Z_1||Z_2}{Z_1||Z_2 + Z_c}\right) \tag{A.49}$$

Combining

$$2i_{id} = v_{sc}\left(-\frac{\Delta Z}{Z_1 Z_2} + \frac{\Delta Z}{Z_1 Z_2}\frac{Z_c}{(Z_1||Z_2 + Z_c)}\right) + i_{id}\left(-\frac{\Delta Z_f}{2}\frac{Z_1||Z_2}{(Z_1||Z_2 + Z_c)}\right)\frac{\Delta Z}{Z_1 Z_2} \tag{A.50}$$

$$i_{id}\left(2 + \frac{\Delta Z_f \Delta Z Z_1||Z_2}{2Z_1 Z_2(Z_1||Z_2 + Z_c)}\right) = v_{sc}\left(\frac{\Delta Z}{Z_1 Z_2}\right)\left(\frac{Z_c}{(Z_1||Z_2 + Z_c)} - 1\right). \tag{A.51}$$

Leading to a numerator:

$$Y_{cd,num} = \frac{\Delta Z}{Z_1 Z_2}\left(\frac{Z_c}{Z_1||Z_2 + Z_c} - 1\right) \tag{A.52}$$

$$Y_{cd,den} = 2 + \frac{\Delta Z_f \Delta Z Z_1||Z_2}{2Z_1 Z_2(Z_1||Z_2 + Z_c)} \tag{A.53}$$

Expanding $Z_1||Z_2$, $(Z_1 Z_2)$ divides out of the denominator

$$Y_{cd,den} = 2 + \frac{\Delta Z \Delta Z_f}{2(Z_1 + Z_2)(Z_1||Z_2 + Z_c)}. \tag{A.54}$$

Recognizing $(Z_1 + Z_2)$ as Z_{dm} and $(Z_1||Z_2 + Z_c)$ as Z_{cm},

$$Y_{cd,den} = 2 + \frac{\Delta Z \Delta Z_f}{2Z_{dm} Z_{cm}}. \tag{A.55}$$

Combining fractions

$$Y_{cd,den} = \frac{2Z_{dm} Z_{cm} + \frac{1}{2}\Delta Z \Delta Z_f}{Z_{dm} Z_{cm}}. \tag{A.56}$$

and multiplying the denominator by 2/2 reveals the common denominator term from the other transconductances

$$Y_{cd,den} = \frac{4Z_{dm} Z_{cm} + \Delta Z \Delta Z_f}{2Z_{dm} Z_{cm}}. \tag{A.57}$$

Combining fractions in the numerator leads to

$$\begin{aligned} Y_{cd,num} &= \frac{\Delta Z}{Z_1 Z_2}\left(\frac{Z_c - Z_1||Z_2 - Z_c}{Z_{cm}}\right) \\ &= -\frac{\Delta Z}{Z_1 Z_2}\left(\frac{Z_1||Z_2}{Z_{cm}}\right) \end{aligned} \tag{A.58}$$

Expanding $Z_1||Z_2$, $Z_1 Z_2$ divides out

$$\begin{aligned} Y_{cd,num} &= -\frac{\Delta Z}{(Z_1 + Z_2)Z_{cm}} \\ &= -\frac{\Delta Z}{Z_{dm} Z_{cm}} \end{aligned} \tag{A.59}$$

so that the final result is

$$\boxed{Y_{cd} = -2\frac{\Delta Z}{4Z_{dm}Z_{cm} + \Delta Z \Delta Z_f}} \tag{A.60}$$

Y_{cc} Derivation:

$$Y_{cc} \equiv \left.\frac{i_{ic}}{v_{sc}}\right|_{v_{sd}=0}. \tag{A.61}$$

$$i_+ = \frac{(v_{sc} - e_{cc})}{Z_1} \tag{A.62}$$

$$i_- = \frac{(v_{sc} - e_{cc})}{Z_2}. \tag{A.63}$$

$$\begin{aligned} i_{ic} &= \frac{v_{sc} - e_{cc}}{Z_1} + \frac{v_{sc} - e_{cc}}{Z_2} \\ &= v_{sc}\left(\frac{1}{Z_1} + \frac{1}{Z_2}\right) - e_{cc}\left(\frac{1}{Z_1} + \frac{1}{Z_2}\right) \\ &= v_{sc}\left(\frac{1}{Z_1||Z_2}\right) - e_{cc}\left(\frac{1}{Z_1||Z_2}\right) \end{aligned} \tag{A.64}$$

Also,

$$\begin{aligned} e_{cc} &= e_c + i_{ic}Z_c \\ &= -\left(\frac{\Delta Z_f}{2}\right)\left(\frac{i_+ - i_-}{2}\right) + i_{ic}Z_c \\ &= -\left(\frac{\Delta Z_f}{4}\right)\left(\frac{v_{sc} - e_{cc}}{Z_1} - \frac{v_{sc} - e_{cc}}{Z_2}\right) + i_{ic}Z_c \end{aligned} \tag{A.65}$$

so that,

$$e_{cc}\left(1 - \frac{\Delta Z_f}{4Z_1} + \frac{\Delta Z_f}{4Z_2}\right) = v_{sc}\left(\frac{-\Delta Z_f}{4}\right)\left(\frac{1}{Z_1} - \frac{1}{Z_2}\right) + i_{ic}Z_c \tag{A.66}$$

and,

$$e_{cc} = \left(v_{sc}\frac{\Delta Z_f}{4}\frac{\Delta Z}{Z_1 Z_2} + i_{ic}Z_c\right)\left(\frac{4Z_1Z_2}{4Z_1Z_2 + \Delta Z_f \Delta Z}\right) \tag{A.67}$$

Combining,

$$\begin{aligned} i_{ic} = v_{sc}\left(\frac{1}{Z_1||Z_1} - \frac{1}{Z_1||Z_2}\frac{\Delta Z_f \Delta Z}{4Z_1Z_2 + \Delta Z_f \Delta Z}\right) \\ + i_{ic}\left(-\frac{Z_c}{Z_1||Z_2}\frac{4Z_1Z_2}{4Z_1Z_2 + \Delta Z_f \Delta Z}\right) \end{aligned} \tag{A.68}$$

$$i_{ic}\left(1 + \frac{4Z_cZ_1Z_2}{Z_1||Z_2(4Z_1Z_2 + \Delta Z_f \Delta Z)}\right) = v_{sc}\left(\frac{1}{Z_1||Z_2} - \frac{1}{Z_1||Z_2}\frac{\Delta Z_f \Delta Z}{(4Z_1Z_2 + \Delta Z_f \Delta Z)}\right) \tag{A.69}$$

Leading to a numerator:

$$Y_{cc,num} = \frac{1}{Z_1||Z_2} - \frac{1}{Z_1||Z_2}\frac{\Delta Z_f \Delta Z}{4Z_1Z_2 + \Delta Z_f \Delta Z} \tag{A.70}$$

and a denominator:

$$Y_{cc,den} = 1 + \frac{4Z_cZ_1Z_2}{Z_1||Z_2(4Z_1Z_2 + \Delta Z_f \Delta Z)} \tag{A.71}$$

Combining fractions in the denominator

$$Y_{cc,den} = \frac{Z_1||Z_2(4Z_1Z_2 + \Delta Z_f \Delta Z) + 4Z_cZ_1Z_2}{Z_1||Z_2(4Z_1Z_2 + \Delta Z_f \Delta Z)} \tag{A.72}$$

$Z_1||Z_2$ divides out between the numerator and denominator.

$$Y_{cc,num} = 1 - \frac{\Delta Z_f \Delta Z}{4Z_1Z_2 + \Delta Z_f \Delta Z} \tag{A.73}$$

$$Y_{cc,den} = \frac{Z_1||Z_2(4Z_1Z_2 + \Delta Z_f \Delta Z) + 4Z_cZ_1Z_2}{(4Z_1Z_2 + \Delta Z_f \Delta Z)} \tag{A.74}$$

Then, combining fractions in the numerator yields

$$\begin{aligned} Y_{cc,num} &= \frac{4Z_1Z_2 + \Delta Z_f \Delta Z - \Delta Z_f \Delta Z}{4Z_1Z_2 + \Delta Z_f \Delta Z} \\ &= \frac{4Z_1Z_2}{4Z_1Z_2 + \Delta Z_f \Delta Z} \end{aligned} \tag{A.75}$$

so that $(4Z_1Z + \Delta Z_f \Delta Z)$ divides out between the numerator and denominator

$$Y_{cc,num} = 4Z_1Z_2 \tag{A.76}$$

$$Y_{cc,den} = Z_1||Z_2(4Z_1Z_2 + \Delta Z_f \Delta Z) + 4Z_cZ_1Z_2 \tag{A.77}$$

Expanding $Z_1||Z_2$ in the denominator,

$$Y_{cc,den} = \frac{Z_1Z_2}{Z_1 + Z_2}(4Z_1Z_2 + \Delta Z_f \Delta Z) + 4Z_cZ_1Z_2 \tag{A.78}$$

Z_1Z_2 divides out between the numerator and denominator

$$Y_{cc,num} = 4 \tag{A.79}$$

$$Y_{cc,den} = \frac{1}{Z_1 + Z_2}(4Z_1Z_2 + \Delta Z_f \Delta Z) + 4Z_c \tag{A.80}$$

Combining fractions in the denominator

$$\begin{aligned} Y_{cc,den} &= \frac{1}{Z_1 + Z_2}(4Z_1Z_2 + \Delta Z_f \Delta Z + 4Z_c(Z_1 + Z_2)) \\ &= \frac{1}{Z_{dm}}(4Z_1Z_2 + \Delta Z_f \Delta Z + 4Z_c(Z_1 + Z_2)) \end{aligned} \tag{A.81}$$

so that

$$Y_{cc,num} = 4Z_{dm} \tag{A.82}$$

$$Y_{cc,den} = (4Z_1Z_2 + \Delta Z_f \Delta Z) + 4Z_c(Z_1 + Z_2) \tag{A.83}$$

Rearranging the denominator

$$\begin{aligned} Y_{cc,den} &= 4(Z_1Z_2 + Z_c(Z_1 + Z_2)) + \Delta Z \Delta Z_f \\ &= 4(\frac{Z_1Z_2}{Z_1 + Z_2} + Z_c)(Z_1 + Z_2) + \Delta Z \Delta Z_f \\ &= 4(Z_1||Z_2 + Z_c)(Z_1 + Z_2) + \Delta Z \Delta Z_f \\ &= 4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f \end{aligned} \tag{A.84}$$

and recognizing $4Z_{dm}$ in the numerator as $8\overline{Z}$, yields the final result

$$\boxed{Y_{cc} = 8\frac{\overline{Z}}{4Z_{cm}Z_{dm} + \Delta Z \Delta Z_f}} \tag{A.85}$$

A.7.2 Derivation of Y'_{cd} using the corrected circuit model

Refer to Figure 2-6(d)

Definitions:

$$e_d = Z_{ed} Y_{cc} v_{sc} \qquad e_c = Z_{ec} Y_{cd} v_{sc} \tag{A.86}$$

$$Z_{ed} \equiv -\frac{\Delta Z_f + \overline{Z_f} a_c}{2(1+a_d)} \qquad Z_{ec} \equiv -\frac{\Delta Z_f}{2} \tag{A.87}$$

Circuit constraints:

$$\begin{aligned} i_{id} &= i_{ed} + \frac{e_d}{4Z_c} \\ &= i_{ed} + i'_{id} \\ i_{ic} &= i_+ + i_- = i'_{ic} \end{aligned} \tag{A.88}$$

where

$$i'_{id} \equiv \frac{1}{2}(i'_+ - i'_-) \tag{A.89}$$

$$i'_{ic} \equiv i'_+ + i'_- = i_{ic} \tag{A.90}$$

and the current through the added DM voltage element is

$$\begin{aligned} i_{ed} &= i_+ - i'_+ \\ &= i'_- - i_-. \end{aligned} \tag{A.91}$$

Applying KVL results in two equations:

$$v_{sc} - i_+ Z_1 - e_d - i'_- 2Z_c - e_c = 0 \tag{A.92}$$

$$v_{sc} - i_- Z_2 + e_d - i'_+ 2Z_c - e_c = 0. \tag{A.93}$$

Y'_{cd} Derivation:

Adding (A.92) and (A.93) leads to:

$$\begin{aligned} 0 &= 2v_{sc} - i_+Z_1 - i_-Z_2 - 2Z_c i_{ic} - 2e_c \\ &= 2v_{sc} - i_+Z_1 + Z_2(2i_{id} - i_+) - 2Z_c i_{ic} - 2e_c \\ &= 2v_{sc} - i_+Z_1 + Z_2(2Y'_{cd}v_{sc} - i_+) - 2Z_c Y_{cc} v_{sc} - 2Z_{ec}Y'_{cd}v_{sc} \end{aligned} \tag{A.94}$$

so that

$$2v_{sc}(1 + Z_2Y'_{cd} - Z_cY_{cc} - Z_{ec}Y'_{cd}) = i_+(Z_1 + Z_2), \tag{A.95}$$

while subtracting the two leads to:

$$\begin{aligned} 0 &= -i_+Z_1 + i_-Z_2 - 2e_d + 2Z_c(-i'_- + i'_+) \\ &= -i_+Z_1 + i_-Z_2 - e_d \\ &= -i_+Z_1 + i_-Z_2 - Z_{ed}Y_{cc}v_{sc} \end{aligned} \tag{A.96}$$

so that

$$i_- = \frac{i_+Z_1 + Z_{ed}Y_{cc}v_{sc}}{Z_2}. \tag{A.97}$$

Eliminating i_- and i_+ in favor of i_{id}:

$$\begin{aligned} i_{id} &= \frac{i_+ - i_-}{2} \\ &= \frac{1}{2}\left(i_+ - \frac{i_+Z_1 + Z_{ed}Y_{cc}v_{sc}}{Z_2}\right) \\ &= \frac{1}{2}i_+\left(1 - \frac{Z_1}{Z_2}\right) - \frac{1}{2}\frac{Z_{ed}Y_{cc}v_{sc}}{Z_2} \\ &= -\frac{1}{2}i_+\left(\frac{\Delta Z}{Z_2}\right) - \frac{Z_{ed}Y_{cc}v_{sc}}{2Z_2} \end{aligned} \tag{A.98}$$

so that

$$i_+ = \left(i_{id} + \frac{Z_{ed}Y_{cc}v_{sc}}{2Z_2}\right)\left(-\frac{2Z_2}{\Delta Z}\right). \tag{A.99}$$

Plugging i_+ into (A.95) yields

$$\begin{aligned} 2v_{sc}(1 + Z_2Y'_{cd} - Z_cY_{cc} - Z_{ec}Y'_{cd}) &= 2\overline{Z}\left(-\frac{2Z_2}{\Delta Z}\right)\left(i_{id} + \frac{Z_{ed}Y_{cc}v_{sc}}{2Z_2}\right) \\ &= 2\overline{Z}\left(-\frac{2Z_2}{\Delta Z}\right)\left(Y'_{cd}v_{sc} + \frac{Z_{ed}Y_{cc}v_{sc}}{2Z_2}\right) \\ 2(1 + Z_2Y'_{cd} - Z_cY_{cc} - Z_{ec}Y'_{cd}) &= 2\overline{Z}\left(-\frac{2Z_2}{\Delta Z}\right)\left(Y'_{cd} + \frac{Z_{ed}Y_{cc}}{2Z_2}\right). \end{aligned} \tag{A.100}$$

Collecting terms,

$$Y'_{cd}\left(2Z_2 - 2Z_{ec} + \frac{4\overline{Z}Z_2}{\Delta Z}\right) = Y_{cc}\left(-Z_{ed}\frac{2\overline{Z}}{\Delta Z} + 2Z_c\right) - 2 \tag{A.101}$$

and solving,

$$\begin{aligned} Y'_{cd} &= \frac{Y_{cc}(-Z_{ed}\frac{2\overline{Z}}{\Delta Z} + 2Z_c) - 2}{2Z_2 - 2Z_{ec} + \frac{4\overline{Z}Z_2}{\Delta Z}} \\ &= \frac{Y_{cc}(-Z_{ed}2\overline{Z} + 2Z_c\Delta Z) - 2\Delta Z}{2Z_2\Delta Z - 2Z_{ec}\Delta Z + 4\overline{Z}Z_2}. \end{aligned} \tag{A.102}$$

The denominator of Y'_{cd} can be made symmetric by expanding $Z_{ec} = -\frac{\Delta Z_f}{2}$, $\Delta Z = Z_1 - Z_2$ and $\Delta Z_f = Z_{f1} - Z_{f2}$. The denominator becomes

$$\begin{aligned} Y'_{cd,den} &= 2Z_2(Z_1 - Z_2) + \frac{1}{2}(Z_{f1} - Z_{f2})(Z_1 - Z_2) + 4\frac{Z_1 + Z_2}{2}Z_2 \\ &= 4Z_1Z_2 + \frac{1}{2}Z_{f1}Z_1 - \frac{1}{2}Z_{f1}Z_2 - \frac{1}{2}Z_1Z_{f2} + \frac{1}{2}Z_2Z_{f2} \\ &= 4Z_1Z_2 + \frac{1}{2}\Delta Z\Delta Z_f \end{aligned} \tag{A.103}$$

and Y'_{cd} becomes

$$Y'_{cd} = \frac{Y_{cc}(-Z_{ed}2\overline{Z} + 2Z_c\Delta Z) - 2\Delta Z}{4Z_1Z_2 + \frac{1}{2}\Delta Z\Delta Z_f}. \tag{A.104}$$

Expanding Z_{ed} and Z_c in the numerator leads to

$$Y'_{cd} = \frac{Y_{cc}(\overline{Z}\frac{\Delta Z_f + a_c\overline{Z_f}}{1+a_d} + \overline{Z_f}\Delta Z) - 2\Delta Z}{4Z_1Z_2 + \frac{1}{2}\Delta Z\Delta Z_f} \tag{A.105}$$

Which can be rewritten

$$\boxed{Y'_{cd} = \frac{Y_{cc}(\overline{Z}\frac{\Delta Z_f + a_c\overline{Z_f}}{1+a_d} + \overline{Z_f}\Delta Z) - 2\Delta Z}{4Z_1Z_2 + \frac{1}{2}\Delta Z_f \Delta Z}}. \tag{A.106}$$

Y'_{cds} Derivation:

With the small-mismatch approximations,

$$\Delta Z_f << Z_{f1}, Z_{f2}, \overline{Z_f} \tag{A.107}$$

$$\Delta Z << Z_1, Z_2, \overline{Z}. \tag{A.108}$$

$$Y_{cc} \approx \frac{1}{Z_{cm}}. \tag{A.109}$$

From (A.106), Y'_{cds} can be simplified with the approximations in (A.107)-(A.109) as follows:

$$Y'_{cd} \approx \frac{\frac{1}{Z_{cm}}(\overline{Z}\frac{a_c\overline{Z_f}}{1+a_d} + \overline{Z_f}\Delta Z) - 2\Delta Z}{4Z_1Z_2}. \tag{A.110}$$

Combining fractions

$$\begin{aligned} Y'_{cd} &\approx \frac{(\overline{Z}\frac{a_c\overline{Z_f}}{1+a_d} + \overline{Z_f}\Delta Z) - 2\Delta Z Z_{cm}}{4Z_1Z_2Z_{cm}} \\ &= \frac{(\overline{Z}\frac{a_c\overline{Z_f}}{1+a_d} + \overline{Z_f}\Delta Z) - 2\Delta Z(Z_1||Z_2 + \frac{Z_f}{2})}{4Z_1Z_2Z_{cm}}. \end{aligned} \tag{A.111}$$

Canceling terms in the numerator leads to

$$\begin{aligned} Y'_{cd} &\approx \frac{\left(\overline{Z}\frac{a_c\overline{Z_f}}{1+a_d}\right) - 2\Delta Z Z_1||Z_2}{4Z_1Z_2Z_{cm}} \\ &= \frac{\left(\overline{Z}\frac{a_c\overline{Z_f}}{1+a_d}\right) - \Delta Z\overline{Z}}{4Z_1Z_2Z_{cm}} \\ &= \frac{\left(\overline{Z}\frac{a_c\overline{Z_f}}{1+a_d}\right) - \Delta Z\overline{Z}}{4Z_1Z_2Z_{cm}}. \end{aligned} \tag{A.112}$$

Using the small mismatch approximations $Z_1 Z_2 \approx \overline{Z}^2$ so that $\overline{Z}$ divides out leaving

$$\begin{aligned} Y'_{cd} &\approx \frac{\left(\frac{a_c \overline{Z_f}}{1+a_d}\right) - \Delta Z}{4\overline{Z} Z_{cm}} \\ &= \frac{\left(\frac{a_c \overline{Z_f}}{1+a_d}\right) - \Delta Z}{4(\frac{Z_1+Z_2}{2}) Z_{cm}} \end{aligned} \tag{A.113}$$

So that

$$\boxed{Y'_{cds} = \frac{\left(\frac{a_c \overline{Z_f}}{1+a_d}\right) - \Delta Z}{2 Z_{cm} Z_{dm}}}. \tag{A.114}$$

Appendix B

Multi-converter Systems

- Master-slacve current-voltage regulator hardware
- MATLAB® scripts for multi-converter system modeling
- Derivation of special-case impedances for $\hat{i}_{o1}/\hat{d}_1$
- Derivation of special-case impedances for $\hat{i}_{o1}/\hat{d}_2$

B.1 Master-Slave Current-Voltage Regulator Hardware

- Photograph
- Schematic drawings

B.1.1 Photograph

A photograph of the master-slave regulator system deployed in an experimental setting is shown in the Figure below.

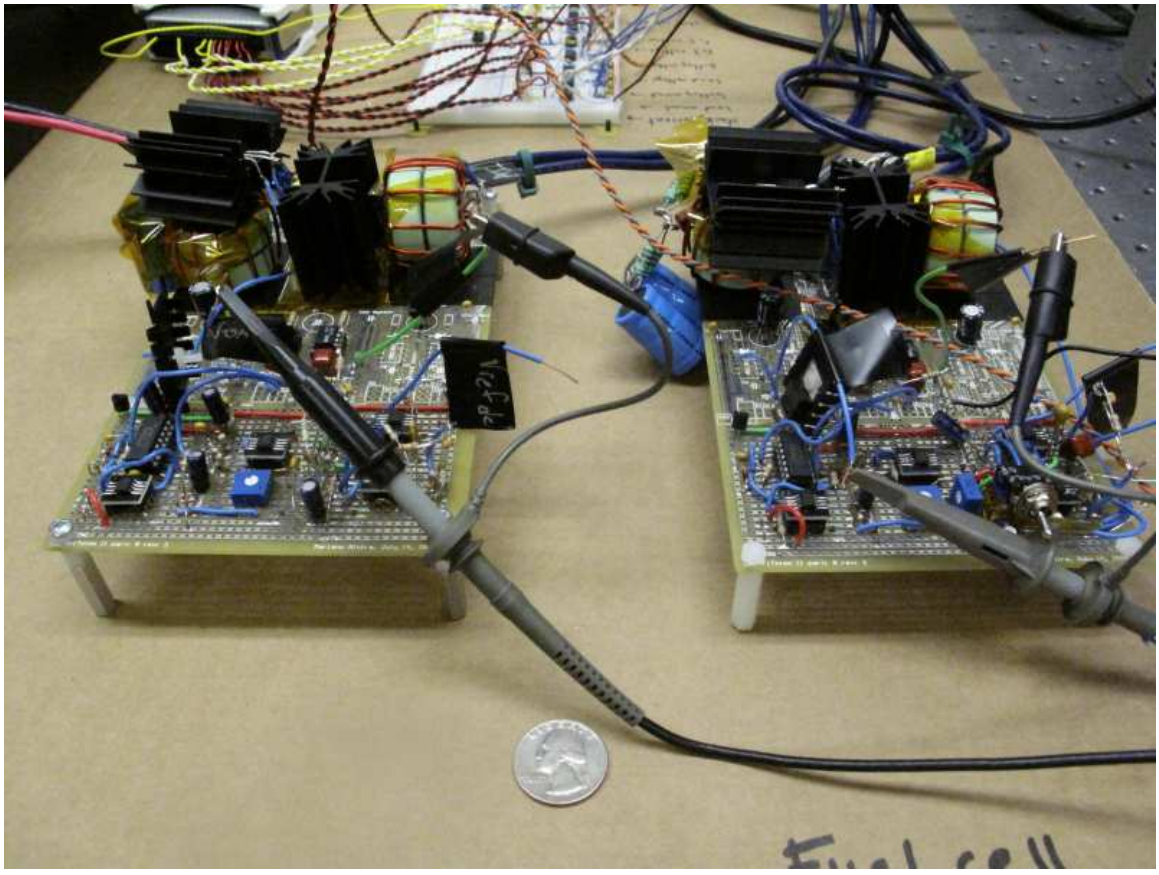


Figure B-1: A closeup photograph of the two-converter current-voltage regulated power system deployed in the fuel cell experimental setup.

B.1.2 Schematic Drawings

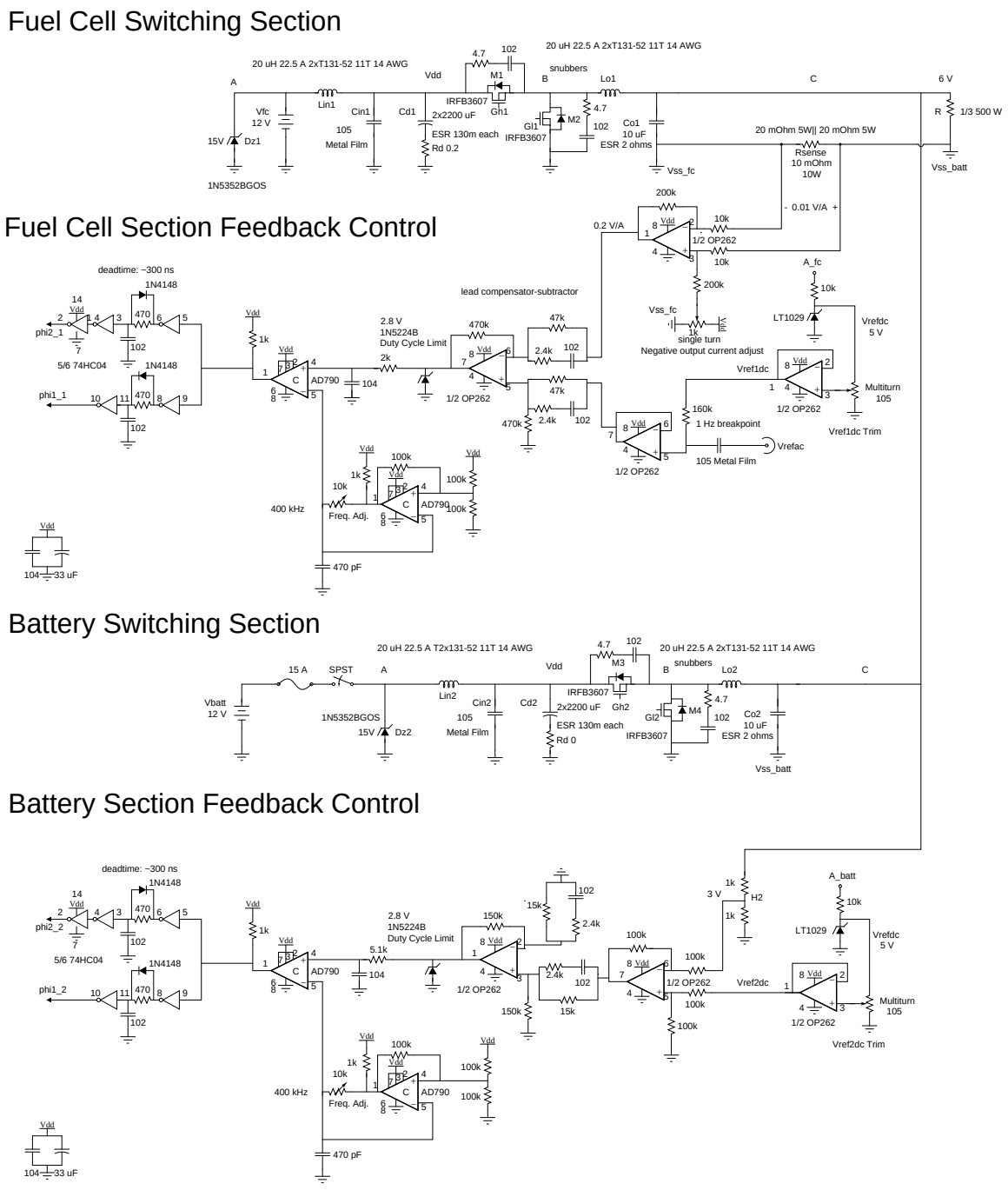


Figure B-2: Switching sections and feedback control circuits. ‘A’, ‘B’, ‘C’, ‘Vdd’, ‘Vss’, labels above switching section nodes correspond to edge connectors on the Totem Cards for the respective converters (fuel cell and battery).

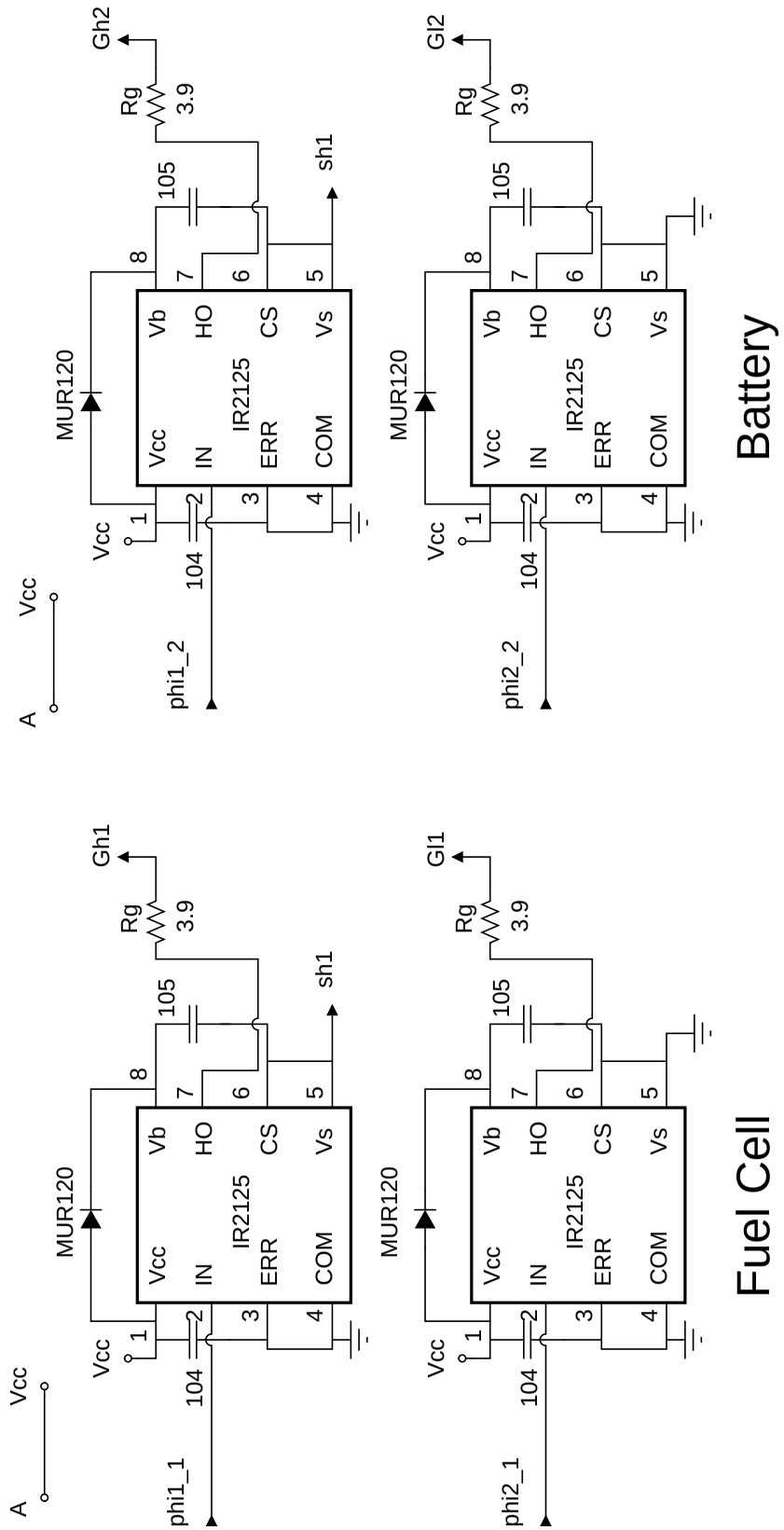


Figure B-3: Gate drives

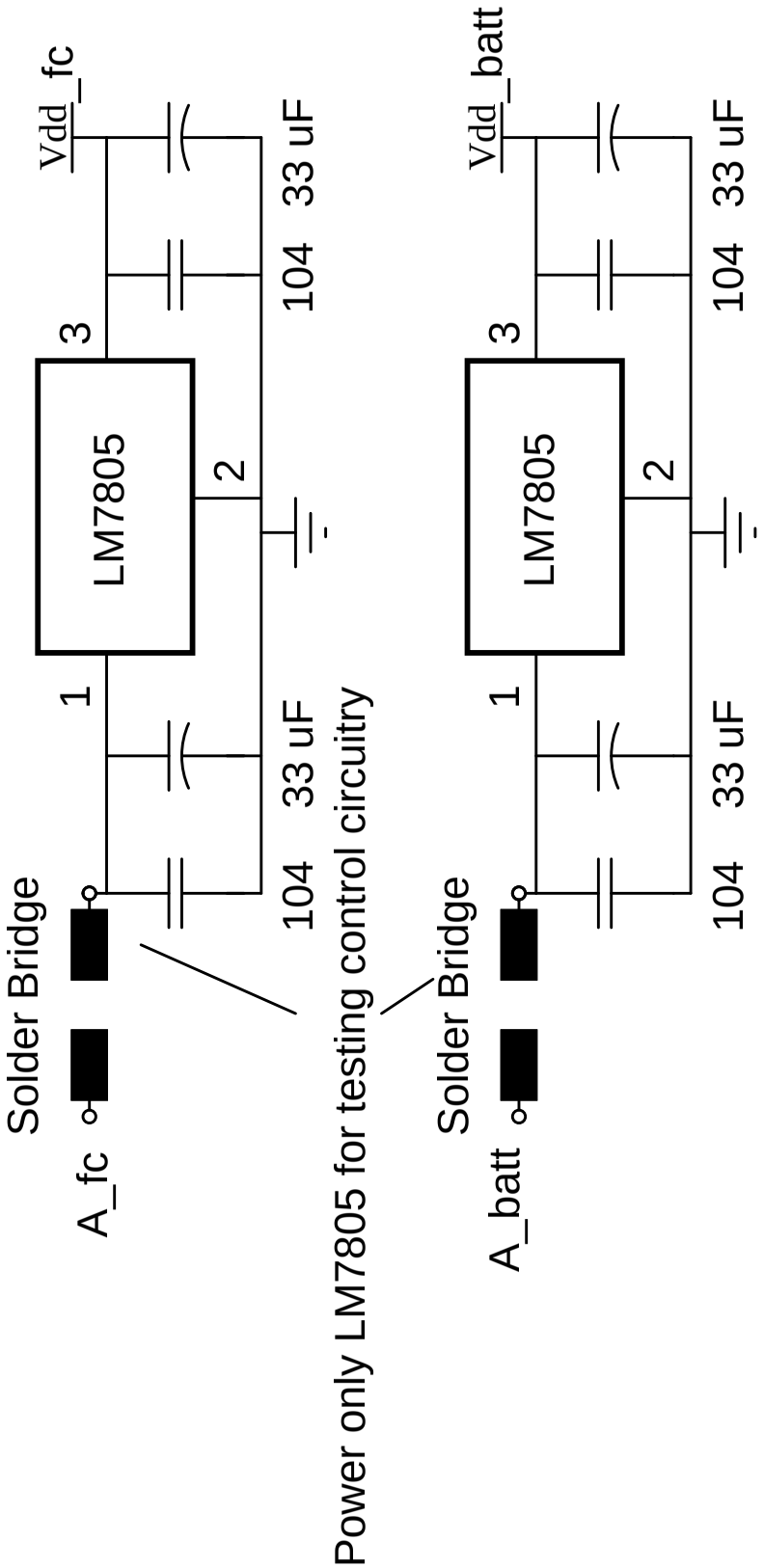


Figure B-4: Linear regulators

B.2 Matlab® Scripts for Multi-converter System Modeling

This Appendix presents a MATLAB® platform for evaluating the performance and stability of a dual converter power system. The computation of numerical values for complex high order rational transfer functions is demonstrated in the example functions. Algebraic manipulation or reduction of low entropy transfer functions by hand is avoided using the quasi-symbolic method also demonstrated in the example functions.

B.2.1 Master-slave Current-voltage Regulated Power System Evaluation

`MSRM.m`

This script is a platform for evaluating the performance and stability of the "master-slave" current-voltage regulated dual converter fuel cell power system. Supporting functions include functions that report magnitude and phase vectors for closed-loop transfer functions derived in Chapter 6 and also 2EET correction factors.

```
%% AC AND DC Analysis
clc
clear
close all
s = tf('s');

%% Inputs
%Choose plots
DC = 0;
CL = 1;
OL = 0;
OutputFilter = 0;
InputFilter = 0;
CorrectionFactors = 0;
Uncorrectedvoverd1 = 0;
Correctedvoverd1 = 0;
Uncorrectedvoverd2 = 0;
Correctedvoverd2 = 0;
FilteredInput = 0;
Single = 0;
Printdata = 0;

%Feedback loop parameters
H1 = 20;
```

```
Rsense = 10e-3;
H2 = 1/2;
Fm1 = 1/1.7;
Fm2 = 1/1.7;
% Lead Lag compensator Current Feedback Loop G1 = 10; wlagp1 = 6e4; wlagz1
% = 2e6; wleadp1 = 1e6; wleadz1 = 1e6; % Voltage Feedback Loop G2 = 10;
% wlagp2 = 2e6; wlagz2 = 2e6; wleadp2 = 1e6; wleadz2 = 1e6;
%
% Gc1 = G1*(1+s/wlagz1)*(1+s/wleadz1)/((1+s/wlagp1)*(1+s/wleadp1)); Gc2 =
% G2*(1+s/wlagz2)*(1+s/wleadz2)/((1+s/wlagp2)*(1+s/wleadp2));

% Third order compensator Current Feedback Loop
G1 = 10;
wp1 = 4e5;
wz1 = 2e4;
wf1 = 5e3;
% Voltage Feedback Loop
G2 = 10;
wp2 = 4e5;
wz2 = 6e4;
wf2 = 2e3;
Gc1 = G1*(1/(1+s/wf1))*(1+s/wz1)/(1+s/wp1);
Gc2 = G2*(1/(1+s/wf2))*(1+s/wz2)/(1+s/wp2);
% Gc1 = 1; Gc2 = 1;

% Output Filters
Rwire = 0.02;
lo1 = 20e-6;
ESRlo1 = 0.01;
ESRlo1 = 0.5+0.01+Rsense+Rwire;
Co1 = 10e-6;
ESRco1 = 2;
lo2 = lo1;
ESRlo2 = 0.01;
Co2 = Co1;
ESRco2 = ESRco1;
Rdiode1 = 0.0;
Rdiode2 = 0.0;

% Input Filters
Lin1 = 20e-6;
Cin1 = 1e-6;
Cd1 = 2*2200e-6;
Rd1 = 0.2+0.5*0.130; % = Rd + ESRc
ESRlin1 = 0.01;
ESRcin1 = 0.01;
Lin2 = Lin1;
Cin2= Cin1;
Cd2 = Cd1;
Rd2 = 0.2*0.130;
ESRlin2 = ESRlin1;
ESRcin2 = ESRcin1;

%Set points
Vfc = 12;
Vbatt = 12;
Vout_Command = 6;
Io1_Command = 8;
V = Vout_Command;
Io1 = Io1_Command;
Io2 = 8;
```

```
D1 = V/Vfc;
D2 = V/Vbatt;
I = Io1+Io2;

% Load Resistive: R = V/I; Current Source:
R = 1e9;

% Simulation and Swept Parameters Vref1min = 0; Vref1res = 0.001; Vref1max
% = 9;
fsim = logspace(1,9);

%% Linear Model: Buck
Le1 = lo1;
Le2 = lo2;
ESRle1 = ESRlo1;
ESRle2 = ESRlo2;
Ce1 = Co1;
Ce2 = Co2;
ESRce1 = ESRco1;
ESRce2 = ESRco2;
zce1 = ESRce1+1/(s*Ce1);
zce2 = ESRce2+1/(s*Ce2);
zc = zce1*zce2/(zce1+zce2);
zl = reduce_sys(zc*R/(zc+R));
zlsingle1 = reduce_sys(zc*R/(zc+R));
zlsingle2 = reduce_sys(zc*R/(zc+R));
zle1 = s*lo1+ESRlo1;
zle2 = s*lo2+ESRlo2;
zlpzle1 = (zl*zle1/(zl+zle1));
zlpzle2 = (zl*zle2/(zl+zle2));
ze1 = zle1*zce1/(zle1+zce1);
ze2 = zle2*zce2/(zle2+zce2);
M1 = D1;
M2 = D2;
e1 = V/(D1^2);
e2 = V/(D2^2);
j1 = Io1;
j2 = Io2;
Rp = R/(1+R/ESRle1+R/ESRle2);
lambdaprime1 = zle1+(zle2*zl/(zle2+zl));
lambda1 = (zle2*zl/(zle2+zl))/lambdaprime1;
lambdaprime2 = zle2+(zle1*zl/(zle1+zl));
lambda2 = (zle1*zl/(zle1+zl))/lambdaprime2;

%% Open-loop transfer functions

%Pre-evaluated voverd and io1overd
[v1mag,v1phase] = voverd1(H1,H2,Gc1,Gc2,M1,M2,e1,e2,j1,j2,Fm1,Fm2,Le1,...
    Le2,ESRle1,ESRle2,Ce1,Ce2,ESRce1, ESRce2, R,fsim);
[v2mag,v2phase] = voverd2(H1,H2,Gc1,Gc2,M1,M2,e1,e2,j1,j2,Fm1,Fm2,Le1,...
    Le2,ESRle1,ESRle2,Ce1,Ce2,ESRce1, ESRce2, R,fsim);
[i1mag,i1phase] = io1overd1(H1,H2,Gc1,Gc2,M1,M2,e1,e2,j1,j2,Fm1,Fm2,Le1,...
    Le2,ESRle1,ESRle2,Ce1,Ce2,ESRce1, ESRce2, R,fsim);
[i2mag,i2phase] = io1overd2(H1,H2,Gc1,Gc2,M1,M2,e1,e2,j1,j2,Fm1,Fm2,Le1,...
    Le2,ESRle1,ESRle2,Ce1,Ce2,ESRce1, ESRce2, R,fsim);

%Unevaluated voverd for computation of loop transfer functions
voverd1_uneval = e1*M1*lambda1;
voverd2_uneval = e2*M2*lambda2;

%Unevaluated io1overd for computation of loop transfer functions
```

```
io1overd1_uneval = (M1*e1/zle1-voverd1_uneval/ze1);
io1overd2_uneval = -voverd2_uneval/ze1;

%Unevaluated doverx for computation of loop transfer functions
d1overx_uneval = -io1overd2_uneval*Fm1*Gc1*H1*Rsense*Gc2*Fm2/(1+Fm1*Gc1...
    *H1*Rsense*io1overd1_uneval);
d2overx_uneval = Gc2*Fm2;

%Unevaluated doverq for computation of loop transfer functions
d1overq_uneval = Gc1*Fm1;
d2overq_uneval = -H2*Gc2*Fm2*voverd1_uneval*Gc1*Fm1/(1+H2*Gc2*Fm2*...
    voverd2_uneval);

%Loop transfer functions with minor loops
T1 = H1*Rsense*(d1overq_uneval*io1overd1_uneval+d2overq_uneval*...
    io1overd2_uneval);
T2 = H2*(d1overx_uneval*voverd1_uneval+d2overx_uneval*voverd2_uneval);


% Single converter for debugging while building
%zlpzle2 -> zlsingle1
% voverd1_uneval_single = e1*M1*zlsingle1/(zle1+zlsingle1); Tsingle1 =
% voverd1_uneval_single*Fm1*Gc1*H1;
%zlpzle1 -> zlsingle2
% voverd2_uneval_single = e2*M2*zlsingle2/(zle2+zlsingle2); Tsingle2 =
% voverd2_uneval_single*Fm2*Gc2*H2;

%% Closed-loop transfer functions
d2overd1_uneval = -(H2*Fm2*Gc2*M1*e1*zlpzle2/(zle1+zlpzle2))/...
    (1+H2*Fm2*Gc2*M2*e2*zlpzle1/(zle2+zlpzle1));
den_uneval = 1+Fm1*Gc1*H1*Rsense*M1*e1*(1/zle1-zlpzle2/...
    ((zle1+zlpzle2)*ze1));
d1overvref1_uneval = (Fm1*Gc1/den_uneval)/(1-Fm1*Gc1*H1*Rsense*M2*...
    (zlpzle1/(zle2+zlpzle1))*(e2/zle1)*d2overd1_uneval/(den_uneval));
d2overvref1_uneval = d1overvref1_uneval*d2overd1_uneval;

[vmag,vphase] = vovervref1(M1,M2,e1,e2,j1,j2,Le1,Le2,ESRle1,ESRle2,Ce1,...
    Ce2,ESRce1,ESRce2,Fm1,Fm2,Gc1,Gc2,H1,H2,R, d1overvref1_uneval,...
    d2overvref1_uneval, fsim);
[io1mag,io1phase] = io1overvref1(M1,M2,e1,e2,j1,j2,Le1,Le2,ESRle1,...
    ESRle2,Ce1,Ce2,ESRce1,ESRce2,Fm1,Fm2,Gc1,Gc2,H1,H2,R, ...
    d1overvref1_uneval, d2overvref1_uneval, fsim);
[iin1mag,iin1phase] = iin1overvref1(M1,M2,e1,e2,j1,j2,Le1,Le2,...
    ESRle1,ESRle2,Ce1,Ce2,ESRce1,ESRce2,Fm1,Fm2,Gc1,Gc2,H1,H2,R, ...
    d1overvref1_uneval, d2overvref1_uneval, fsim);
[iin1overiloadmag,iin1overiloadphase] = iin1overiload(M1,M2,e1,e2,j1,...
    j2,Le1,Le2,ESRle1,ESRle2,Ce1,Ce2,ESRce1,ESRce2,Fm1,Fm2,Gc1,Gc2,H1,...
    H2,R, Rsense, fsim);

%% Output Filter Transfer function
Q1 = zlpzle2/(zlpzle2+zle1);
Q2 = zlpzle1/(zlpzle1+zle2);

%% Input Filter Transfer Function
Zlin1 = ESRlin1+s*Lin1;
Zlin2 = ESRlin2+s*Lin2;
Zcin1 = ESRcin1+1/(s*Cin1);
Zcin2 = ESRcin2+1/(s*Cin2);
Zd1 = Rd1+1/(s*Cd1);
Zd2 = Rd2+1/(s*Cd2);
Qin1 = Zcin1*Zd1/(Zcin1+Zd1)/(Zcin1*Zd1/(Zcin1+Zd1)+Zlin1);
```

```
Qin2 = Zcin2*Zd2/(Zcin2+Zd2)/(Zcin2*Zd2/(Zcin2+Zd2)+Zlin2);
[Qin1mag, Qin1phase] = bode(Qin1, fsim);
Qin1mag = 20*log10(Qin1mag(:));
Qin1phase = (180/pi)*(unwrap((pi/180)*Qin1phase(:)));

%% Correction Factors for Input Filters
[CF1mag,CF1phase] = CFactor1(e1,e2,j1,j2,Le1,Le2,ESRle1,ESRle2,Ce1,Ce2,...
    ESRce1,ESRce2,M1,M2,R,Lin1,Cin1,ESRlin1, ESRcin1, Cd1, Rd1,Lin2,...
    Cin2,ESRlin2, ESRcin2, Cd2, Rd2,fsim);
[CF2mag,CF2phase] = CFactor2(e1,e2,j1,j2,Le1,Le2,ESRle1,ESRle2,Ce1,Ce2,...
    ESRce1,ESRce2,M1,M2,R,Lin1,Cin1,ESRlin1, ESRcin1, Cd1, Rd1,Lin2,...
    Cin2,ESRlin2, ESRcin2, Cd2, Rd2,fsim);
[CF3mag,CF3phase] = CFactor3(e1,e2,j1,j2,Le1,Le2,ESRle1,ESRle2,Ce1,Ce2,...
    ESRce1,ESRce2,M1,M2,R,Lin1,Cin1,ESRlin1, ESRcin1, Cd1, Rd1,Lin2,...
    Cin2,ESRlin2, ESRcin2, Cd2, Rd2,fsim);
[CF4mag,CF4phase] = CFactor4(e1,e2,j1,j2,Le1,Le2,ESRle1,ESRle2,Ce1,Ce2,...
    ESRce1,ESRce2,M1,M2,R,Lin1,Cin1,ESRlin1, ESRcin1, Cd1, Rd1,Lin2,...
    Cin2,ESRlin2, ESRcin2, Cd2, Rd2,fsim);

%% Plotting %%

%% Plotting C-L transfer functions
while CL == 1
    % V
    %vmag
    figure
    subplot(2,1,1)
    % calculated
    semilogx(fsim,vmag); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,vovervref1acmagdata,'x')
        %          semilogx(fsim,vovervref1acmagdata_droop,'+')
    end
    %     h_legend = legend('Calculated','Simulated');
    %     set(h_legend,'FontSize',8);
    title('V/V_{ref1}')
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('|v/v_{ref1}| (db)','Fontsize',8,'Color','k');
    hold off
    grid on
    box on

    %vphase
    subplot(2,1,2)
    % calculated
    semilogx(fsim,vphase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,vovervref1acphasedata,'x')
        %          semilogx(fsim,vovervref1acphasedata_droop,'+')
    end
    %     h_legend = legend('Calculated','Simulated');
    %     set(h_legend,'FontSize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('\angle v/v_{ref1} (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
```

```
hold off
grid on
box on

% IO1
%io1mag
figure
subplot(2,1,1)
% calculated
semilogx(fsim,io1mag); hold on
% simulated
if Printdata == 1
    semilogx(fsim,io1overvref1acmagdata,'x')
    %         semilogx(fsim,io1overvref1acmagdata_droop,'+')
end
%     h_legend = legend('Calculated','Simulated');
%     set(h_legend,'FontSize',8);
title('I_{o1}/V_{ref1}')
h = gca;
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
%     set(h_legend,'Location','best')
ylabel('|i_{o1}/v_{ref1}| (db)','Fontsize',8,'Color','k');
hold off
grid on
box on


%io1phase
subplot(2,1,2)
% calculated
semilogx(fsim,io1phase); hold on
% simulated
if Printdata == 1
    semilogx(fsim,io1overvref1acphasedata,'x')
    %         semilogx(fsim,io1overvref1acphasedata_droop,'+')
end
%     h_legend = legend('Calculated','Simulated');
%     set(h_legend,'FontSize',8);
h = gca;
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
%     set(h_legend,'Location','best')
ylabel('\angle i_{o1}/v_{ref1} (deg)','Fontsize',8,'Color','k');
xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
hold off
grid on
box on

% IIN1
%iin1mag
figure
subplot(2,1,1)
% calculated
semilogx(fsim,iin1mag); hold on
% simulated
if Printdata == 1
    semilogx(fsim,iin1overvref1acmagdata,'x')
    %         semilogx(fsim,iin1overvref1acmagdata_droop,'+')
end
%     h_legend = legend('Calculated','Simulated');
%     set(h_legend,'FontSize',8);
title('I_{in1}/V_{ref1}')
```

```
h = gca;
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
%     set(h_legend,'Location','best')
ylabel('|i_{in1}/v_{ref1}| (db)','Fontsize',8,'Color','k');
hold off
grid on
box on

%iin1phase
subplot(2,1,2)
% calculated
semilogx(fsim,iin1phase); hold on
% simulated
if Printdata == 1
    semilogx(fsim,iin1overvref1acphasedata,'x')
    %         semilogx(fsim,iin1overvref1acphasedata_droop,'+')
end
%     h_legend = legend('Calculated','Simulated');
%     set(h_legend,'FontSize',8);
h = gca;
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
%     set(h_legend,'Location','best')
ylabel('\angle i_{in1}/v_{ref1} (deg)','Fontsize',8,'Color','k');
xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
hold off
grid on
box on


% IIN1overiload
%iin1overiloadmag
figure
subplot(2,1,1)
% calculated
semilogx(fsim,iin1overiloadmag); hold on
% simulated
if Printdata == 1
    semilogx(fsim,iin1overvref1acmagdata,'x')
    %         semilogx(fsim,iin1overvref1acmagdata_droop,'+')
end
%     h_legend = legend('Calculated','Simulated');
%     set(h_legend,'FontSize',8);
title('I_{in1}/I_{load}')
h = gca;
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
%     set(h_legend,'Location','best')
ylabel('|i_{in1}/i_{load}| (db)','Fontsize',8,'Color','k');
hold off
grid on
box on

%iin1overiloadphase
subplot(2,1,2)
% calculated
semilogx(fsim,iin1overiloadphase); hold on
% simulated
if Printdata == 1
    semilogx(fsim,iin1overvref1acphasedata,'x')
    %         semilogx(fsim,iin1overvref1acphasedata_droop,'+')
end
%     h_legend = legend('Calculated','Simulated');
```

```
    %     set(h_legend,'FontSize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('\angle i_{in1}/i_{load} (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
    hold off
    grid on
    box on
    CL = 0;
end

%% Plotting O-L transfer functions
while OL == 1
    figure
    %     subplot(1,2,1)
    margin(T1)
    % grid on
    box on
    figure
    %     subplot(1,2,2)
    margin(T2)
    box on
    OL = 0;
end

%% Plotting Correction Factors
while CorrectionFactors == 1,
    figure
    % Magnitude
    subplot(2,1,1)
    % calculated
    semilogx(fsim,CF1mag); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd1correctedacmagdata -...
            voverd1uncorrectedacmagdata,'x')
        % semilogx(fsim,voverd1correctedacmagdata_droop-voverd1uncorrecteda
        % cmagdata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    h = gca;
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('|CF_1| (db)','Fontsize',8,'Color','k');
    title('Extra Element Correction Factor CF_1 for v/d_1')
    grid on
    box on
    hold off

    % Phase
    subplot(2,1,2)
    % calculated
    semilogx(fsim,CF1phase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd1correctedacphasedata -...
            voverd1uncorrectedacphasedata,'x')
```

```
    % semilogx(fsim,voverd1correctedacphasedata_droop-voverd1uncorrecte
    % dacphasedata_droop,'o')
end

% Plot Formatting
%     h_legend = legend('Calculated','Simulated');
h = gca;
%     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
ylabel('\angle CF_1 (deg)','Fontsize',8,'Color','k');
xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
grid on
box on
hold off

%% Plotting Correction Factor 2
figure
% Magnitude
subplot(2,1,1)
% calculated
semilogx(fsim,CF2mag); hold on
% simulated
if Printdata == 1
    semilogx(fsim,voverd2correctedacmagdata -...
        voverd2uncorrectedacmagdata,'x')
    % semilogx(fsim,voverd2correctedacmagdata_droop-voverd2uncorrectedacmagdata_droop,'o')
end

% Plot Formatting
%     h_legend = legend('Calculated','Simulated');
h = gca;
%     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
ylabel('|CF_2| (db)','Fontsize',8,'Color','k');
title('Extra Element Correction Factor CF_2 for v/d_2')
grid on
box on
hold off

% Phase
subplot(2,1,2)
% calculated
semilogx(fsim,CF2phase); hold on
% simulated
if Printdata == 1
    semilogx(fsim,voverd2correctedacphasedata -...
        voverd2uncorrectedacphasedata,'x')
    %semilogx(fsim,voverd2correctedacphasedata_droop-
    %voverd2uncorrectedacphasedata_droop,'o')
end

% Plot Formatting
%     h_legend = legend('Calculated','Simulated');
h = gca;
%     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
ylabel('\angle CF_2 (deg)','Fontsize',8,'Color','k');
xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
```

```
grid on
box on
hold off

%% Plotting Correction Factor 3 for io1/d1
figure
% Magnitude
subplot(2,1,1)
% calculated
semilogx(fsim,CF3mag); hold on
% simulated
if Printdata == 1
    semilogx(fsim,io1overd1correctedacmagdata-...
        io1overd1uncorrectedacmagdata,'x')
    % semilogx(fsim,voverd2correctedacmagdata_droop-
    % voverd2uncorrectedacmagdata_droop,'o')
end

% Plot Formatting
%     h_legend = legend('Calculated','Simulated');
h = gca;
%     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
ylabel('|CF_3| (db)','Fontsize',8,'Color','k');
title('Extra Element Correction Factor CF_3 for i_{o1}/d_1')
grid on
box on
hold off

% Phase
subplot(2,1,2)
% calculated
semilogx(fsim,CF3phase); hold on
% simulated
if Printdata == 1
    semilogx(fsim,io1overd1correctedacphasedata-...
        io1overd1uncorrectedacphasedata,'x')
    % semilogx(fsim,voverd2correctedacphasedata_droop-
    % voverd2uncorrectedacphasedata_droop,'o')
end

% Plot Formatting
%     h_legend = legend('Calculated','Simulated');
h = gca;
%     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
ylabel('\angle CF_3 (deg)','Fontsize',8,'Color','k');
xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
grid on
box on
hold off


%% Plotting Correction Factor 4 for io1/d2
figure
% Magnitude
subplot(2,1,1)
% calculated
semilogx(fsim,CF4mag); hold on
```

```
    % simulated
    if Printdata == 1
        semilogx(fsim,io1overd2correctedacmagdata-...
            io1overd2uncorrectedacmagdata,'x')
        % semilogx(fsim,voverd2correctedacmagdata_droop-
        % voverd2uncorrectedacmagdata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    h = gca;
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('|CF_4| (db)','Fontsize',8,'Color','k');
    title('Extra Element Correction Factor CF_4 for i_{o1}/d_2')
    grid on
    box on
    hold off

    % Phase
    subplot(2,1,2)
    % calculated
    semilogx(fsim,CF4phase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,io1overd2correctedacphasedata-...
            io1overd2uncorrectedacphasedata,'x')
        % semilogx(fsim,voverd2correctedacphasedata_droop-
        % voverd2uncorrectedacphasedata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    h = gca;
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('\angle CF_4 (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off


    CorrectionFactors = 0;
end

%% Plotting Uncorrected voverd1
while Uncorrectedvoverd1 == 1,
    figure
    % Magnitude
    subplot(2,1,1)
    % calculated
    semilogx(fsim,v1mag); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd1uncorrectedacmagdata,'x')
        %         semilogx(fsim,voverd1uncorrectedacmagdata_droop,'o')
    end
```

```
    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    %     set(h_legend,'FontSize',8);
    title('v/d_1','Fontsize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('|v/d_1| (db)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off

    % Phase
    subplot(2,1,2)
    % calculated
    semilogx(fsim,v1phase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd1uncorrectedacphasedata,'x')
        %         semilogx(fsim,voverd1uncorrectedacphasedata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('\angle v/d_1 (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off

    Uncorrectedvoverd1 = 0;
end

%% Plotting Corrected voverd1
while Correctedvoverd1 == 1,
    figure
    % Magnitude
    subplot(2,1,1)
    % calculated
    c1mag = v1mag+CF1mag;
    semilogx(fsim,c1mag); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd1correctedacmagdata,'x');
        %         semilogx(fsim,voverd1correctedacmagdata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    title('Corrected v/d_1','Fontsize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('|v/d_1| (db)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off
```

```
    % Phase
    subplot(2,1,2)
    %calculated
    c1phase = v1phase+CF1phase;
    semilogx(fsim,c1phase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd1correctedacphasedata,'x')
        %         semilogx(fsim,voverd1correctedacphasedata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    h = gca;
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('\angle v/d_1 (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off
    Correctedvoverd1 = 0;
end

%% Plotting Uncorrected voverd2
while Uncorrectedvoverd2 == 1,
    figure
    % Magnitude
    subplot(2,1,1)
    % calculated
    semilogx(fsim,v2mag); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd2uncorrectedacmagdata,'x')
        %         semilogx(fsim,voverd2uncorrectedacmagdata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    %     set(h_legend,'FontSize',8);
    title('v/d_2','Fontsize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    set(h_legend,'Location','best')
    ylabel('|v/d_2| (db)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off

    % Phase
    subplot(2,1,2)
    % calculated
    semilogx(fsim,v2phase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd2uncorrectedacphasedata,'x')
        %         semilogx(fsim,voverd2uncorrectedacphasedata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
```

```
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('\angle v/d_2 (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off

    Uncorrectedvoverd2 = 0;
end

%% Plotting Corrected voverd2
while Correctedvoverd2 == 1,
    figure
    % Magnitude
    subplot(2,1,1)
    % calculated
    c2mag = v2mag+CF2mag;
    semilogx(fsim,c2mag); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd2correctedacmagdata,'x')
        %         semilogx(fsim,voverd2correctedacmagdata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    title('Corrected v/d_2','Fontsize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('|v/d_2| (db)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off

    % Phase
    subplot(2,1,2)
    %calculated
    c2phase = v2phase+CF2phase;
    semilogx(fsim,c2phase); hold on
    % simulated
    if Printdata == 1
        semilogx(fsim,voverd2correctedacphasedata,'x')
        %         semilogx(fsim,voverd2correctedacphasedata_droop,'o')
    end

    % Plot Formatting
    %     h_legend = legend('Calculated','Simulated');
    h = gca;
    %     set(h_legend,'FontSize',8); set(h_legend,'Location','best')
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    ylabel('\angle v/d_2 (deg)','Fontsize',8,'Color','k');
    xlabel('Frequency (rad/sec)','Fontsize',8,'Color','k');
    grid on
    box on
    hold off
    Correctedvoverd2 = 0;
end
```

```
%% Plotting Input Filter transfer functions
while InputFilter == 1,
    figure
    bode(Qin1)
    legend('Input Filter 1 TF')
    grid on
    box on
    figure
    bode(Qin2)
    legend('Input Filter 2 TF')
    grid on
    box on
    InputFilter = 0;
end

%% Plotting Output filter transfer functions
while OutputFilter == 1
    figure
    bode(Q1)
    legend('Output Filter 1 TF')
    grid on
    box on
    figure
    bode(Q2)
    legend('Output Filter 2 TF')
    grid on
    box on

    OutputFilter = 0;
end

%% Plotting Filtered Input Current transfer function
while FilteredInput == 1,
    figure
    subplot(2,1,1)
    % calculated
    semilogx(fsim,iin1mag+Qin1mag); hold on
    % simulated
    %     if Printdata == 1
    %         semilogx(fsim,iin1overvref1acmagdata,'x')
    %         semilogx(fsim,iin1overvref1acmagdata_droop,'+')
    %     end h_legend = legend('Calculated','Simulated R_{droop} =
    %     0','Simulated R_{droop} \neq 0'); set(h_legend,'FontSize',8);
    title('Filtered I_{in1}/V_{ref1}')
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('|i_{in1}/v_{ref1}| (db)','Fontsize',8,'Color','k');
    hold off
    grid on
    box on

    %iin1phase
    subplot(2,1,2)
    % calculated
    semilogx(fsim,iin1phase+Qin1phase); hold on
    % simulated
    %     if Printdata == 1
    %         semilogx(fsim,iin1overvref1acphasedata,'x')
    %         semilogx(fsim,iin1overvref1acphasedata_droop,'+')
    %     end h_legend = legend('Calculated','Simulated R_{droop} =
```

```
    %     0','Simulated R_{droop} \neq 0'); set(h_legend,'FontSize',8);
    h = gca;
    set(h,'Fontsize',8,'Ycolor',[0.4,0.4,0.4],'Xcolor',[0.4,0.4,0.4])
    %     set(h_legend,'Location','best')
    ylabel('\angle i_{in1}/v_{ref1} (deg)','Fontsize',8,'Color','k');
    hold off
    grid on
    box on

    FilteredInput = 0;
end

%% Plotting Loop transfer for single converter for debugging while building
while Single == 1,
    figure
    margin(Tsingle1)
    box on
    grid on
    figure
    margin(Tsingle2)
    box on
    grid on

    Single = 0;
end
```

`vovervref1.m`

This script reports the magnitude and phase of the closed-loop transfer function from the first converter's control voltage perturbation to the load voltage perturbation.

```
function [mag,phase] = vovervref1(M1,M2,e1,e2,j1,j2,Le1,Le2,ESRle1,...
    ESRle2,Ce1,Ce2,ESRce1,ESRce2,Fm1,Fm2,Gc1,Gc2,H1,H2,R, ...
    d1overvref1_uneval, d2overvref1_uneval, eval_vector);
s = tf('s');
zle1 = ESRle1+s*Le1;
zle2 = ESRle2+s*Le2;
zce1 = ESRce1+1/(s*Ce1);
zce2 = ESRce2+1/(s*Ce2);
ze1 = zle1*zce1/(zle1+zce1);
ze2 = zle2*zce2/(zle2+zce2);
zc = zce1*zce2/(zce1+zce2);
zl = zc*R/(zc+R);
zlpzle1 = (zl*zle1/(zl+zle1));
zlpzle2 = (zl*zle2/(zl+zle2));

d1overvref1 = freqresp(d1overvref1_uneval, eval_vector);
d2overvref1 = freqresp(d2overvref1_uneval, eval_vector);

term1 = d1overvref1.*freqresp(M1*zlpzle2*e1,eval_vector)./...
    freqresp((zle1+zlpzle2), eval_vector);
term2 = d2overvref1.*freqresp(M2*zlpzle1*e2,eval_vector)./...
    freqresp((zle2+zlpzle1), eval_vector);
result= term1+term2;

%% Results
mag = 20*log10(abs(result(:)));
phase = 180/pi*(angle(result(:)));

end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

`CFactor1.m`

This script reports the magnitude and phase of the 2EET correction factor for the converter transfer function from the first converter's duty ratio perturbation to the first converter's output voltage perturbation (the load voltage).

```
%% Correction factor for v/d1 for TWO input filters with Output
%% Capacitances

function [mag,phase] = CFactor1(e1,e2,j1,j2,Le1,Le2,ESRle1,ESRle2,Ce1,...
    Ce2,ESRce1, ESRce2,M1,M2,R,Lin1,Cin1,ESRlin1, ESRcin1, Cd1, ...
    Rd1,Lin2,Cin2,ESRlin2, ESRcin2, Cd2, Rd2, eval_vector)
s = tf('s');

%% Total Shunt Impedance at Load (ZL) Due to addition of output
%% capacitances
Zce1 = ESRce1+1/(s*Ce1);
Zce2 = ESRce2+1/(s*Ce2);
Zc = Zce1*Zce2/(Zce1+Zce2);
Zle1 = ESRle1+s*Le1;
Zle2 = ESRle2+s*Le2;
ZL = Zc*R/(Zc+R);

%% Special-case impedances
Zs1 = tf(-e1/j1);
Zs2 = tf(Zle2/(M2*M2));
Zs3 = tf((Zle1+(Zle2*ZL/(ZL+Zle2)))/(M1*M1));     %(R->ZL)
Zs4 = tf((Zle2+(Zle1*ZL/(ZL+Zle1)))/(M2*M2));     %(R->ZL)
Zs5 = tf(-e1/j1);
Zs6 = (ZL+Zle1)/(M1*M1);                           %(R->ZL)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Filter Output Impedances
% Z1 = reduce_sys(FilterZo1(Lin1,Cin1,ESRlin1, ESRcin1, Cd1, Rd1));
% Z2 = reduce_sys(FilterZo2(Lin2,Cin2,ESRlin2, ESRcin2, Cd2, Rd2));
Z1 = FilterZo1(Lin1,Cin1,ESRlin1, ESRcin1, Cd1, Rd1);
Z2 = FilterZo2(Lin2,Cin2,ESRlin2, ESRcin2, Cd2, Rd2);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Interaction Parameters
Kn = Zs1/Zs5;
Kd = Zs3/Zs6;

 %if interaction factor=1 can factor exactly.  more numerically robust
 if freqresp(Kn, 1) == 1,
    CF1num = (1+Z1/Zs1)*(1+Z2/Zs2);
else
    CF1num = (1+Z1/Zs1+Z2/Zs2+Kn*(Z1*Z2/(Zs1*Zs2)));
end

%if interaction factor=1 can factor exactly.  more numerically robust
if freqresp(Kd, 1) == 1,
    CF1den = (1+Z1/Zs3)*(1+Z2/Zs4);
else
    CF1den = (1+Z1/Zs3+Z2/Zs4+Kd*(Z1*Z2/(Zs3*Zs4)));
end

%% Compute CF1 in steps
% CF1num = CF1num1*CF1num2:
```

```
CF1num1 = (1+Z1/Zs1);
CF1num2 = (1+Z2/Zs2);

% CF1den = CF1den1+CF1den2:
CF1den1 = 1+Z1/Zs3+Z2/Zs4;
CF1den2 = Kd*(Z1*Z2/(Zs3*Zs4));

%% Evaluate CF1 numerator and denominator numerically
CF1num = freqresp(CF1num1,eval_vector).*freqresp(CF1num2,eval_vector);
CF1den = freqresp(CF1den1,eval_vector)+freqresp(CF1den2,eval_vector);

%% Divide the numerical results to get the numerical Transfer function
%% result
CF1 = CF1num./CF1den;

%% Converter to db magnitude and unwrapped degrees phase
CF1mag = 20*log10(abs(CF1(:)));
CF1phase = (180/pi)*unwrap(angle(CF1(:)));

%% Reporting
mag = CF1mag;
phase = CF1phase;
end
```

B.3 Derivation of Special-case Impedances for $\hat{i}_{o1}/\hat{d}_1$

Designating $\hat{i}_{o1}/\hat{d}_1$ as the 3^{rd} transfer function, the superscripts for the six special-case impedances are all (3). The other independent inputs, $\hat{d}_2(s)$, $\hat{v}_{gth1}(s)$ and $\hat{v}_{gth2}(s)$, are all deactivated leading to some simplification of the circuit in Figure 7-5.

The first special-case impedance, $Z_{N1}|^{(3)}_{Z_2=0}$, is the null-condition impedance at the first extra element port with the second extra element port shorted. Because it is a null-condition impedance, analysis of the circuit should address the fact that the independent input in this transfer function, $\hat{d}_1$ will be directed such that the first converter's output current, $\hat{i}_{o1}$, is nulled. With this condition, and with the other independent inputs deactivated, the voltage drop across the first converter's total output impedance is zero and the second converter output current must also be zero since the second duty ratio has been deactivated. The output voltage must be zero since both converter output currents are zero and that voltage appears at the secondary of the first ideal transformer. The primary voltage of the first ideal transformer must also be zero. Therefore, the voltage across the extra element port is simply $\hat{v}_{in} = -e_1\hat{d}_1(s)$ and the current through the extra element port must be $\hat{i}_{in} = j_1\hat{d}_1(s)$ so that their ratio, the impedance seen at the extra element port is

$$\boxed{Z_{N1}|^{(3)}_{Z_2=0} = -\frac{e_1}{j_1}}. \tag{B.1}$$

The second special-case impedance, $Z_{N2}|^{(3)}_{Z_1=0}$, is the null-condition impedance at the second extra element port with the first extra element port shorted. Because the first converter's output current is zero, the load voltage is simply, $e_1\hat{d}_1M_1$ and the second converter's output current must be $\hat{i}_{o2} = \frac{e_1\hat{d}_1M_1}{R}$. Solving the circuit in Figure 7-5 leads to

$$\hat{i}_{in} = M_2\left(\frac{M_1e_1\hat{d}_1}{R}\frac{Z_{ce2}}{Z_{ce2}+Z_{le2}}\right) \tag{B.2}$$

$$\hat{v}_{in} = \frac{1}{M_2}\left(e_1\hat{d}_1M_1 + \frac{1}{M_2}\hat{i}_{in}Z_{le2}\right). \tag{B.3}$$

Dividing these two leads to

$$\boxed{Z_{N2}|_{Z_1=0}^{(3)} = \frac{1}{M_2^2}\left(R\left(\frac{Z_{ce2}+Z_{le2}}{Z_{ce2}}+Z_{le2}\right)\right)}. \tag{B.4}$$

The third special-case impedance, $Z_{D1}|_{Z_2=0}^{(1)}$, is the open-loop impedance at the first extra element port with the second extra element port shorted. Now the independent input in the transfer function of interest is deactivated leaving all of the independent inputs deactivated. This condition is identical to that for the open-loop impedance found for correcting any other transfer function. The result can be taken directly from the correction factor derivation for $\hat{v}/\hat{d}_1$, for instance:

$$\boxed{Z_{D1}|_{Z_2=0}^{(3)} = \frac{Z_{le1}+Z_L||Z_{le2}}{M_1^2}}. \tag{B.5}$$

The fourth special-case impedance can be taken from the third from symmetry arguments:

$$\boxed{Z_{D2}|_{Z_1=0}^{(3)} = \frac{Z_{le2}+Z_L||Z_{le1}}{M_2^2}}. \tag{B.6}$$

The remaining two special-case impedances are needed to determine the interaction parameters in the correction factor. Note that from (7.31), there is some redundancy in the choice of these final special-case impedances. Here we derive, $Z_{N1}|_{Z_2=\infty}^{(3)}$ and $Z_{D1}|_{Z_2=\infty}^{(3)}$. The fifth special-case impedance, $Z_{N1}|_{Z_2=\infty}^{(3)}$, is the null-condition impedance at the first extra element port with the second extra element port open-circuited. Because the second port is open-circuited, the current through the second primary must be zero, $\hat{i}_{pri2} = 0$ and so must the current through the second inductor, $\hat{i}_{le2} = 0$. Since the first converter's output current is nulled, $\hat{i}_{o1} = 0$, the voltage drop across the first converter's total output impedance is zero, so that by KVL, the voltage across the first secondary and therefore its primary is zero, $\hat{v}_{pri1} = 0$. Therefore, the voltage across the extra element port is simply $\hat{v}_{in} = -e_1\hat{d}_1(s)$ and the current through the extra element port must be $\hat{i}_{in} = j_1\hat{d}_1(s)$ so that their ratio, the

impedance seen at the extra element port is

$$\boxed{Z_{N1}|_{Z_2=\infty}^{(3)} = -\frac{e_1}{j_1}}. \tag{B.7}$$

This result is identical to the result for the first special-case impedance. This fact leads to a numerator interaction parameter that of unity and an interesting simplification of the resulting correction factor.

The sixth and final special-case impedance, $Z_{D1}|_{Z_2=\infty}^{(3)}$, is the open-loop impedance at the first extra element port with the second extra element port open-circuited. The result can be taken directly from the correction factor derivation for $\hat{v}/\hat{d}_1$, for instance:

$$\boxed{Z_{D1}|_{Z_2=\infty}^{(3)} = \frac{Z_{le1} + Z_L}{M_1^2}}. \tag{B.8}$$

B.4 Derivation of Special-case Impedances for $\hat{i}_{o1}/\hat{d}_2$

Designating $\hat{i}_{o1}/\hat{d}_2$ as the 4^{th} transfer function, the superscripts for the six special-case impedances are all (4). The other independent inputs, $\hat{d}_1(s)$, $\hat{v}_{gth1}(s)$ and $\hat{v}_{gth2}(s)$, are all deactivated leading to some simplification of the circuit in Figure 7-5.

The first special-case impedance, $Z_{N1}|_{Z_2=0}^{(4)}$, is the null-condition impedance at the first extra element port with the second extra element port shorted. Because it is a null-condition impedance, analysis of the circuit should address the fact that the independent input in this transfer function, $\hat{d}_2$ will be directed such that the first converter's output current, $\hat{i}_{o1}$, is nulled. With this condition, and with the other independent inputs deactivated, the input voltage can be written in terms of the nonzero load voltage as

$$\hat{v}_{in} = \frac{1}{M_1}\hat{v}\left(\frac{Z_{ce1} + Z_{le1}}{Z_{ce1}}\right) \tag{B.9}$$

and the input current is the transformed current through C_{e1} also written in terms of the load voltage as

$$\hat{i}_{in} = M_1\frac{\hat{v}}{Z_{ce1}} \tag{B.10}$$

and dividing the two yields the result

$$\boxed{Z_{N1}|_{Z_2=0}^{(4)} = \frac{Z_{ce1} + Z_{le1}}{M_1^2(D_1)}}. \tag{B.11}$$

The second special-case impedance, $Z_{N2}|_{Z_1=0}^{(4)}$, is the null-condition impedance at the second extra element port with the first extra element port shorted. The voltage drop across the second converter's total output impedance is zero and the first converter output current must also be zero since the first duty ratio has been deactivated. The output voltage must be zero since both converter output currents are zero and that voltage appears at the secondary of the second ideal transformer. The primary voltage of the second ideal transformer must also be zero. Therefore, the voltage across the extra element port is simply $\hat{v}_{in} = -e_2\hat{d}_2(s)$ and the current through the extra element port must be $\hat{i}_{in} = j_2\hat{d}_2(s)$ so that their ratio, the impedance seen at the extra element port is

$$\boxed{Z_{N2}|_{Z_1=0}^{(4)} = -\frac{e_2}{j_2}}. \tag{B.12}$$

The third special-case impedance, $Z_{D1}|_{Z_2=0}^{(4)}$, is the open-loop impedance at the first extra element port with the second extra element port shorted. Now the independent input in the transfer function of interest is deactivated leaving all of the independent inputs deactivated. This condition is identical to that for the open-loop impedance found for correcting any other transfer function. The result can be taken directly from the correction factor derivation for $\hat{v}/\hat{d}_1$, for instance:

$$\boxed{Z_{D1}|_{Z_2=0}^{(4)} = \frac{Z_{le1} + Z_L||Z_{le2}}{M_1^2}}. \tag{B.13}$$

The fourth special-case impedance can be taken from the third from symmetry arguments:

$$\boxed{Z_{D2}|_{Z_1=0}^{(4)} = \frac{Z_{le2} + Z_L||Z_{le1}}{M_2^2}}. \tag{B.14}$$

The remaining two special-case impedances are needed to determine the interaction parameters in the correction factor. Note that from (7.31), there is some redun-

dancy in the choice of these final special-case impedances. Here we derive, $Z_{N1}|^{(4)}_{Z_2=\infty}$ and $Z_{D1}|^{(4)}_{Z_2=\infty}$. The fifth special-case impedance, $Z_{N1}|^{(4)}_{Z_2=\infty}$, is the null-condition impedance at the first extra element port with the second extra element port open-circuited. With this condition, and with the other independent inputs deactivated, the input voltage can be written in terms of the nonzero load voltage as

$$\hat{v}_{in} = \frac{1}{M_1}\hat{v}\left(\frac{Z_{ce1} + Z_{le1}}{Z_{ce1}}\right) \tag{B.15}$$

and the input current is the transformed current through C_{e1} also written in terms of the load voltage as

$$\hat{i}_{in} = M_1\frac{\hat{v}}{Z_{ce1}} \tag{B.16}$$

and dividing the two yields the result

$$\boxed{Z_{N1}|^{(4)}_{Z_2=\infty} = \frac{Z_{ce1} + Z_{le1}}{M_1^2(D_1)}}. \tag{B.17}$$

This result is identical to the result for the first special-case impedance. This fact leads to a numerator interaction parameter that of unity and an interesting simplification of the resulting correction factor.

The sixth and final special-case impedance, $Z_{D1}|^{(4)}_{Z_2=\infty}$, is the open-loop impedance at the first extra element port with the second extra element port open-circuited. The result can be taken directly from the correction factor derivation for $\hat{v}/\hat{d}_1$, for instance:

$$\boxed{Z_{D1}|^{(4)}_{Z_2=\infty} = \frac{Z_{le1} + Z_L}{M_1^2}}. \tag{B.18}$$

Appendix C

Switched-capacitor Multilevel Output DC/DC Converters

- Hardware
- MATLAB® scripts for switched-capacitor system modeling

C.1 Hardware

- Photograph
- PCB layout
- Schematic drawings
- Build notes
- Bill of materials

C.1.1 Photograph

A photograph of the marx converters in the two-converter photovoltaic experimental setup is shown in the Figure below.

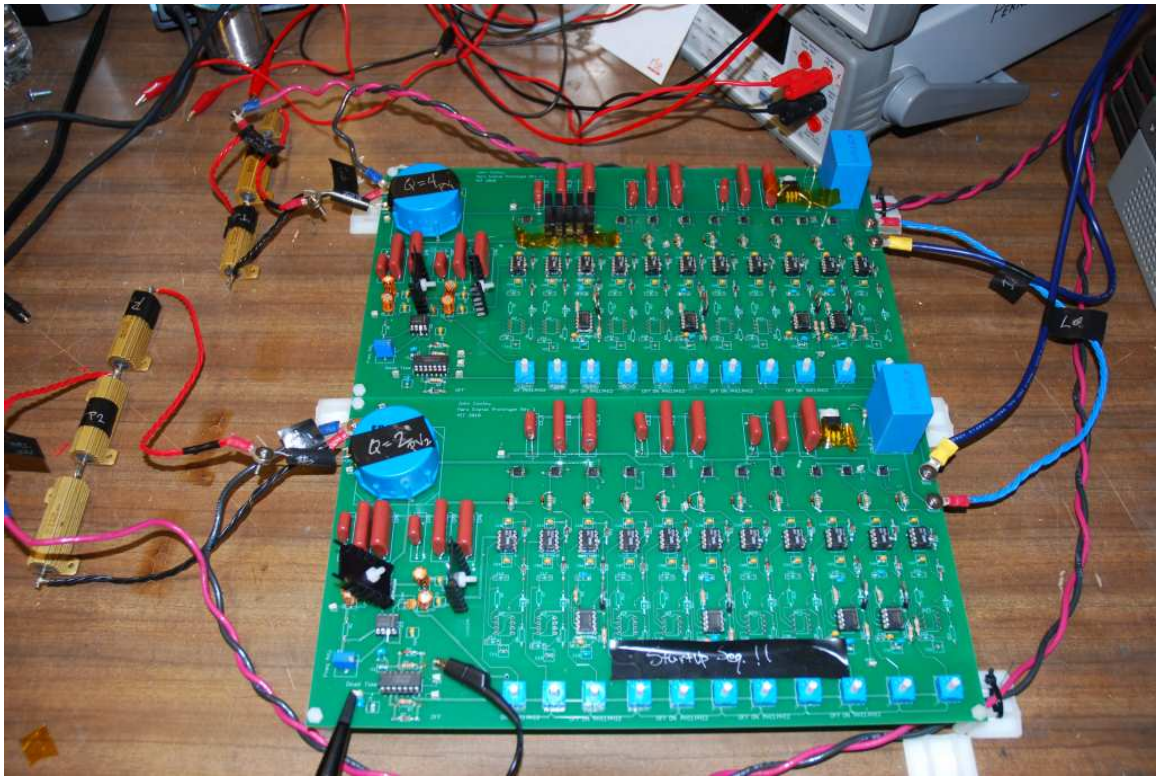


Figure C-1: A closeup photograph of the two marx converters in the experimental setup.

C.1.2 PCB Layout

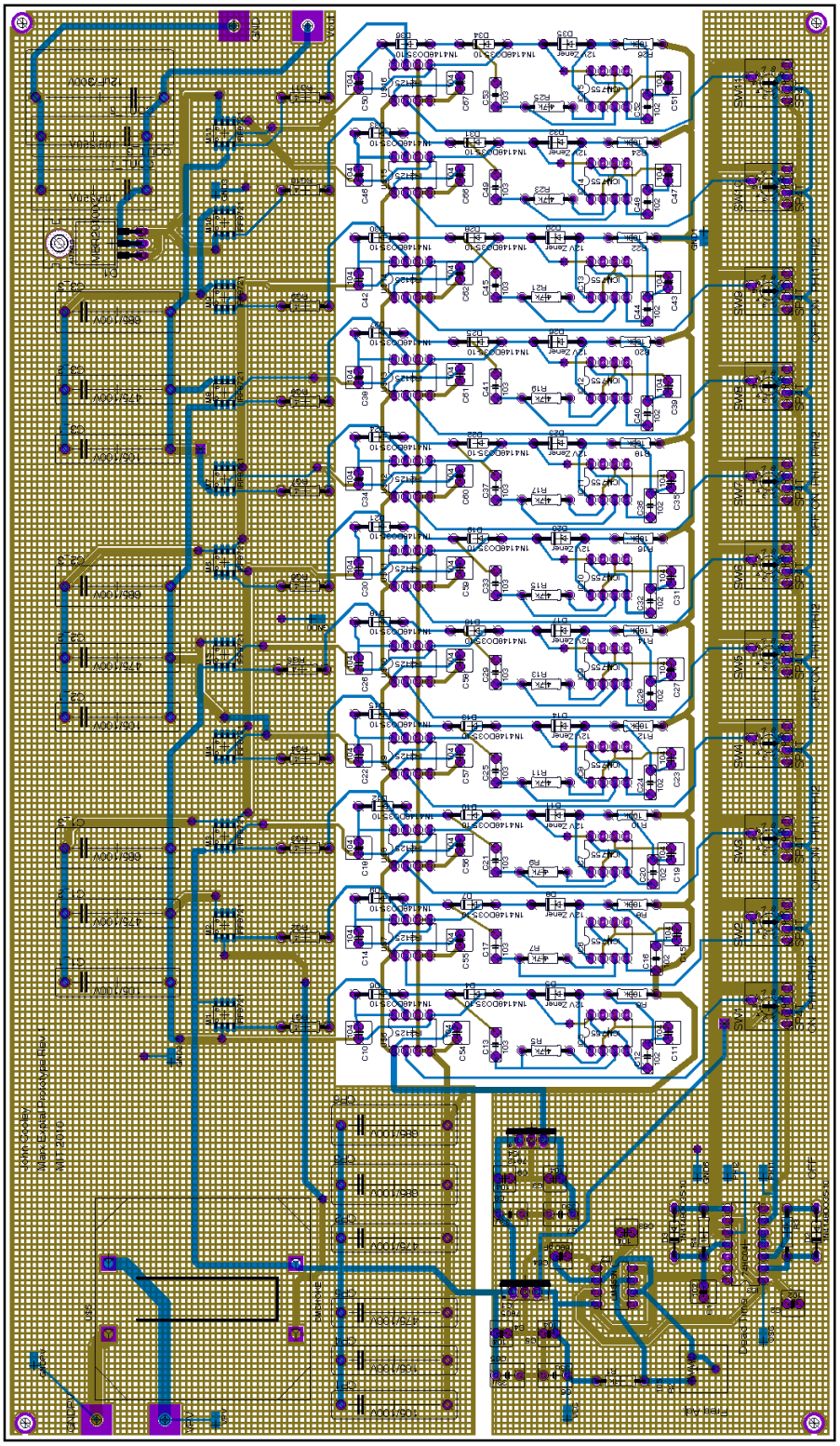


Figure C-2: The Eagle Cad® PCB layout of the marx converter.

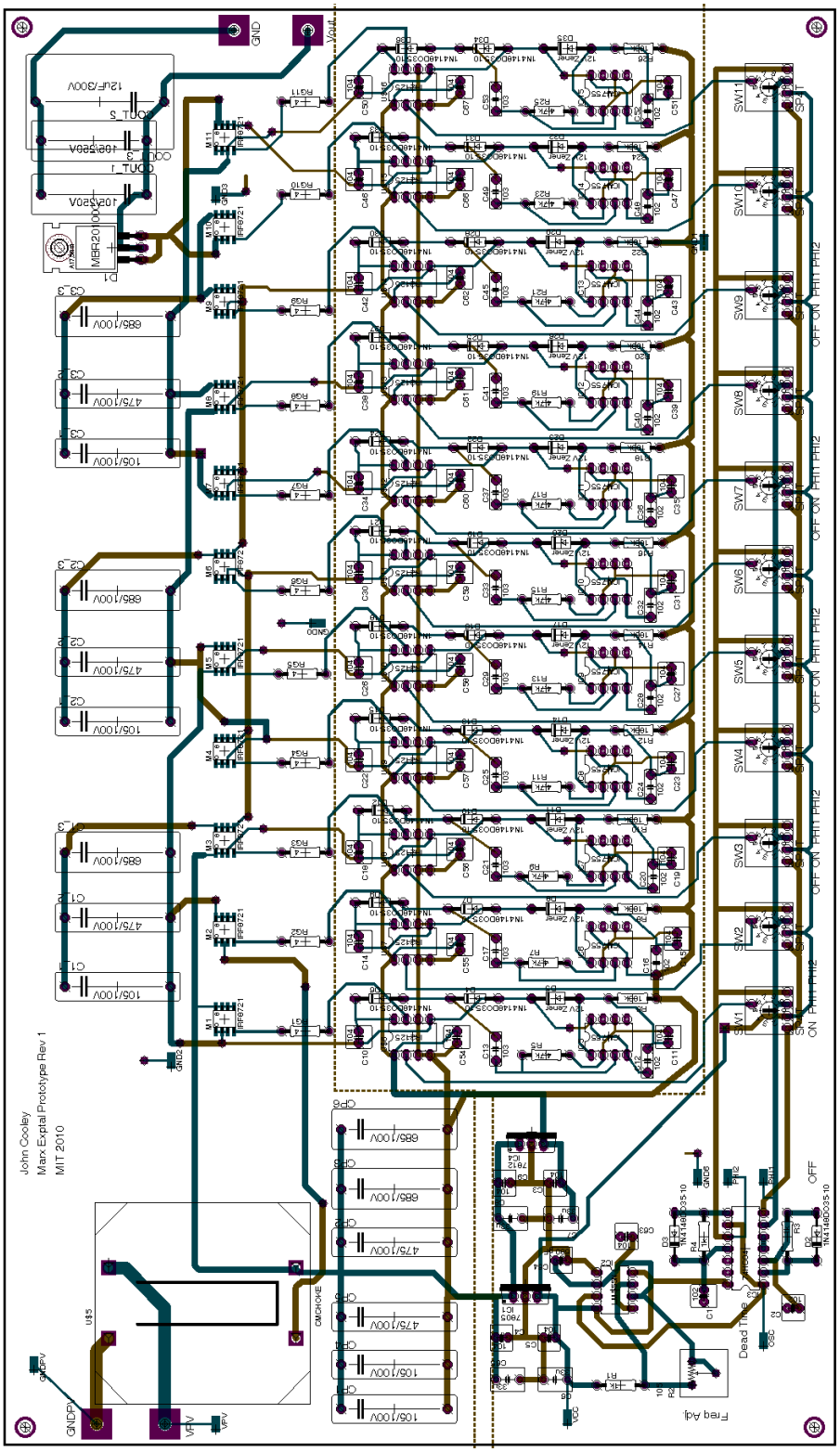


Figure C-3: The Eagle Cad® PCB layout of the marx converter without ground and power planes drawn.

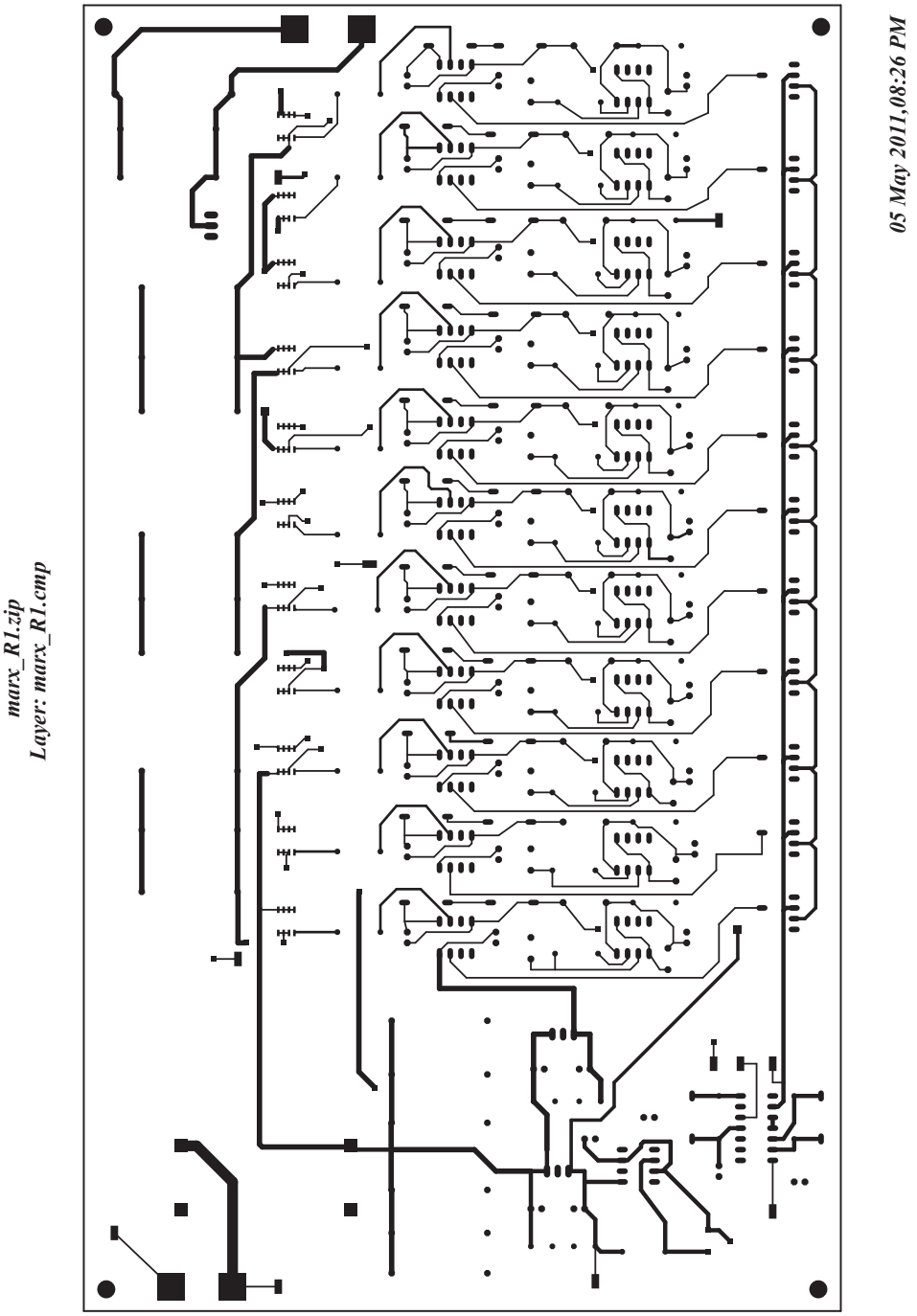


Figure C-4: Top copper layer

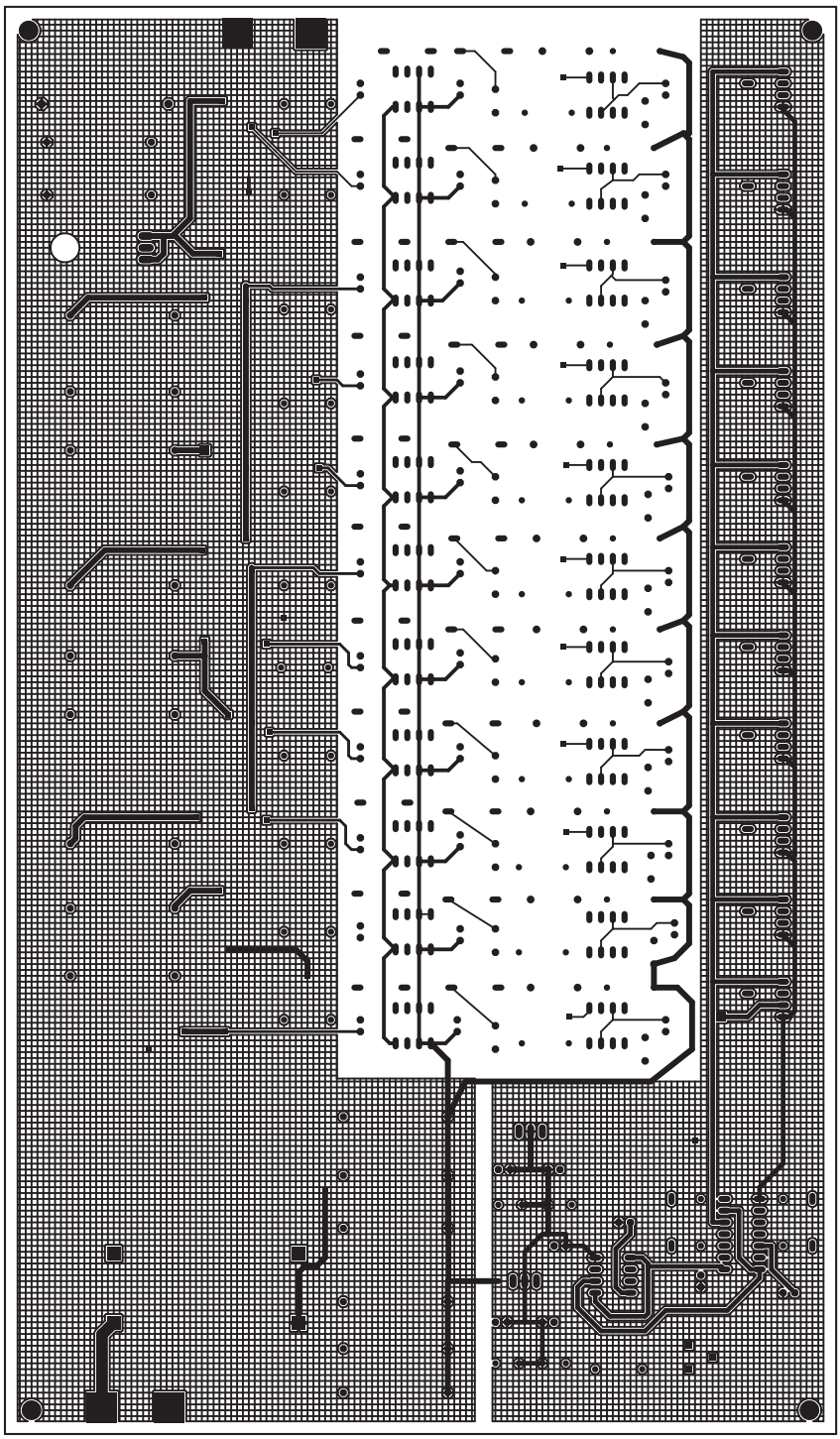


Figure C-5: Bottom copper layer

C.1.3 Schematic Drawings

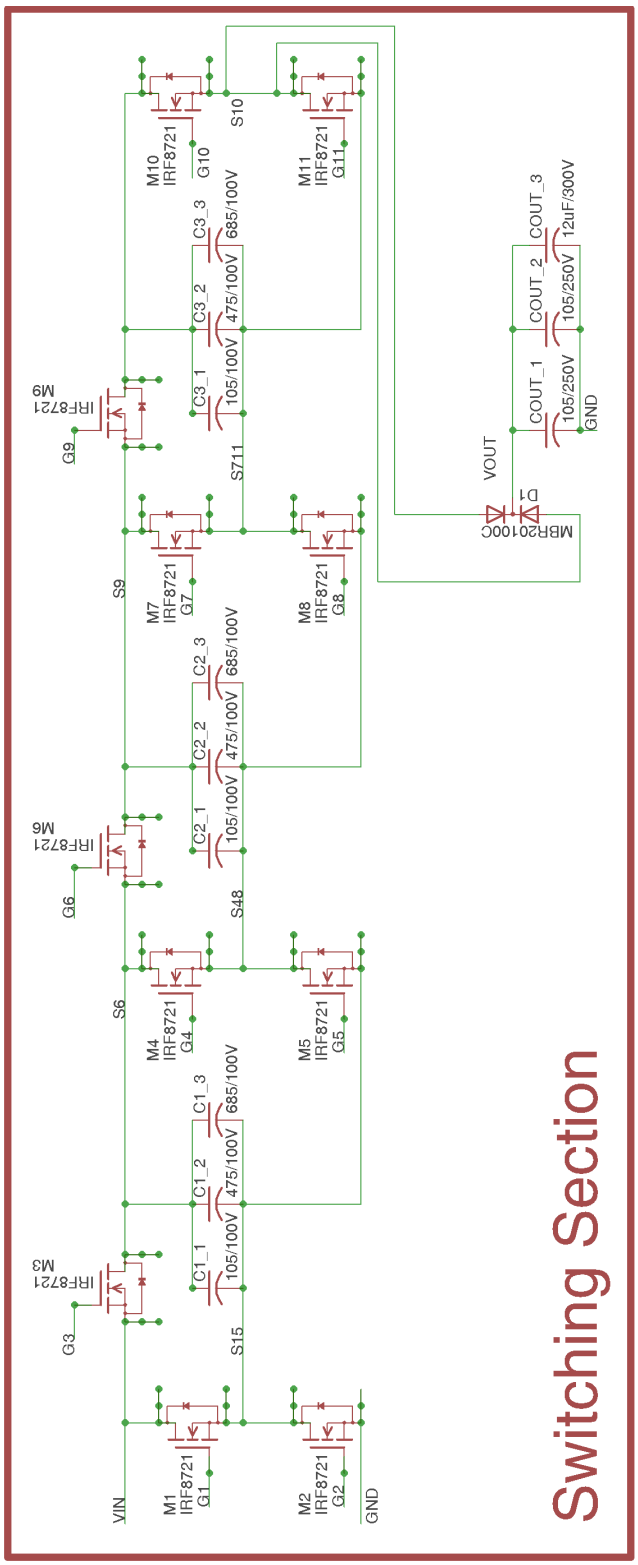


Figure C-6: Switching section

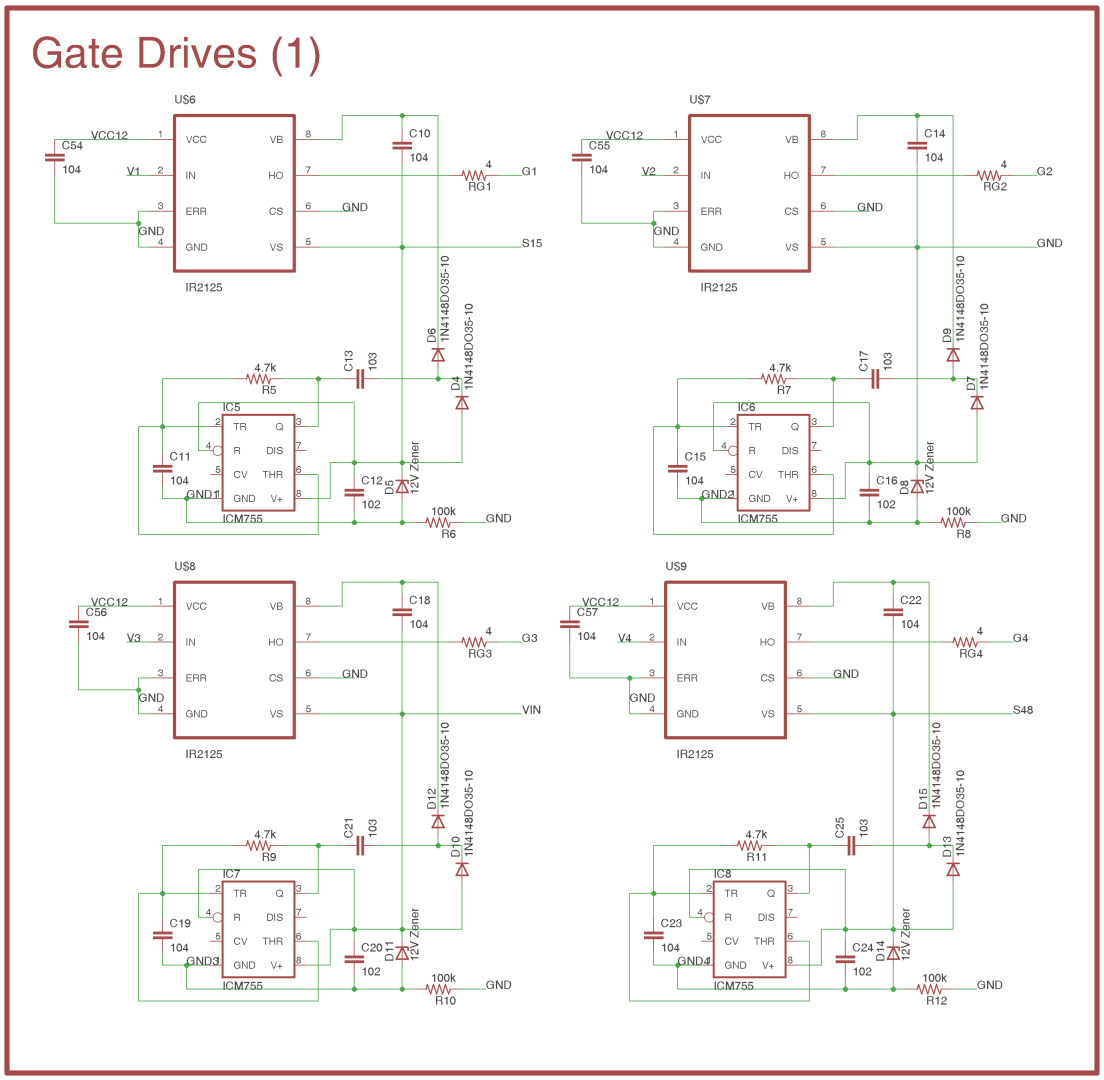


Figure C-7: Gate drives, sheet 1

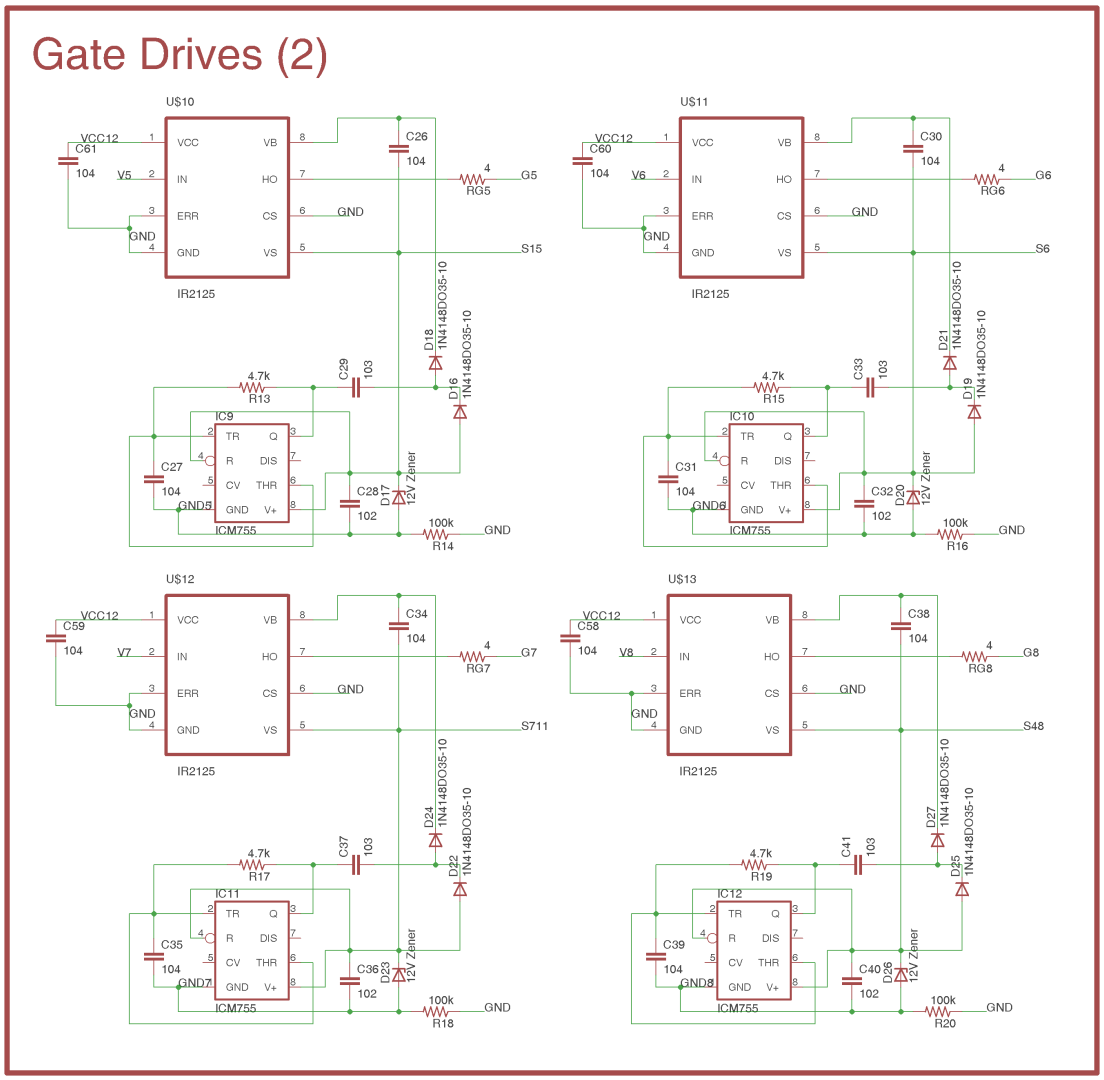


Figure C-8: Gate drives, sheet 2

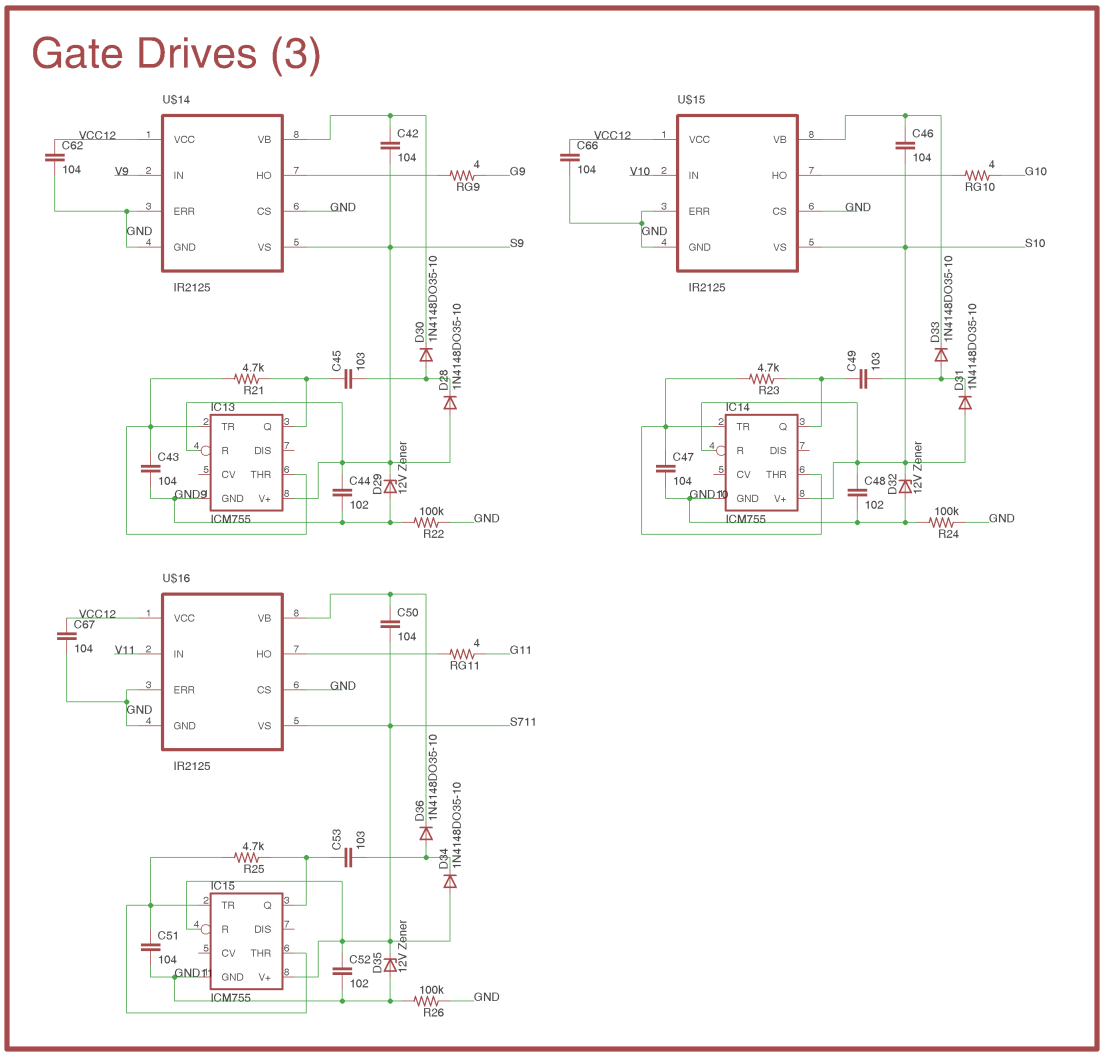


Figure C-9: Gate drives, sheet 3

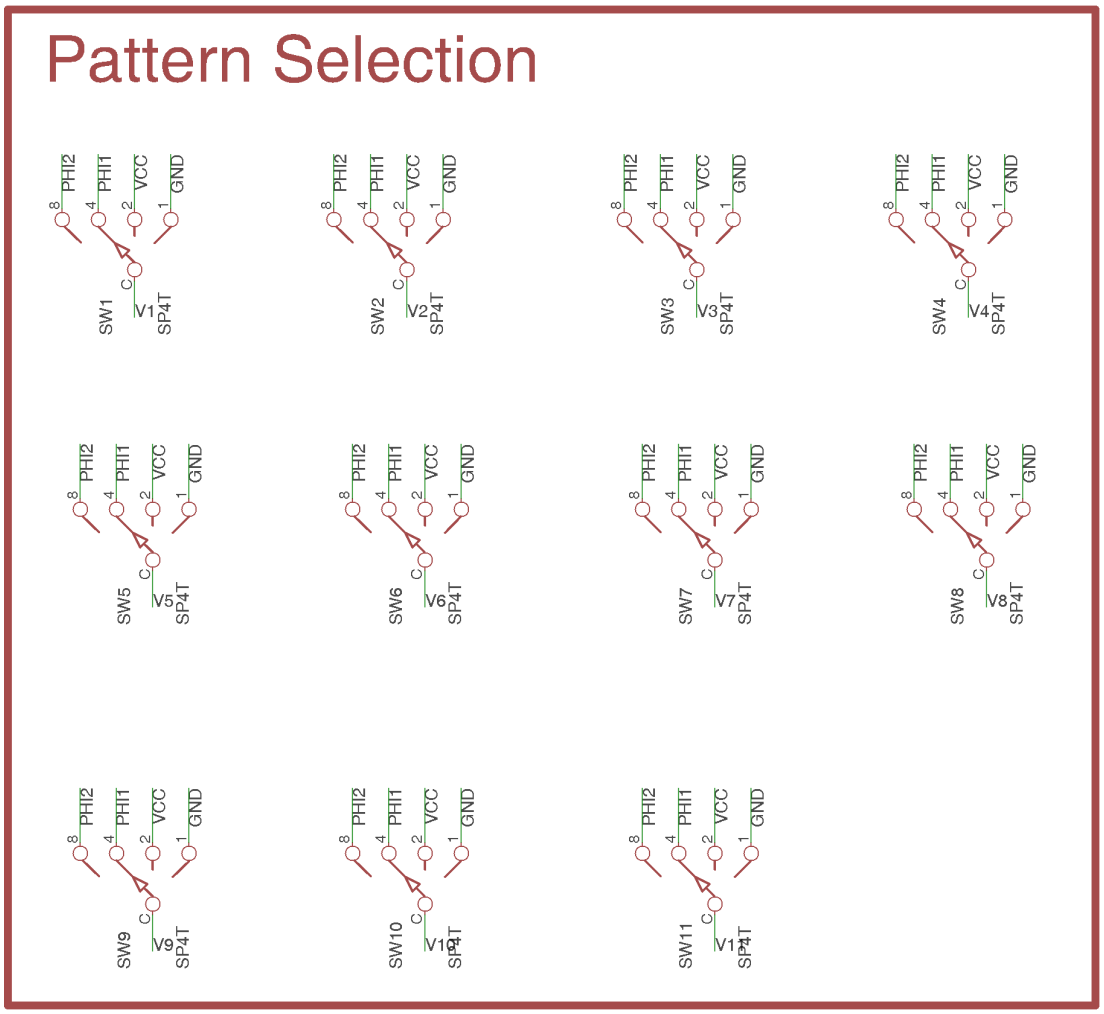


Figure C-10: Switching pattern selection switches

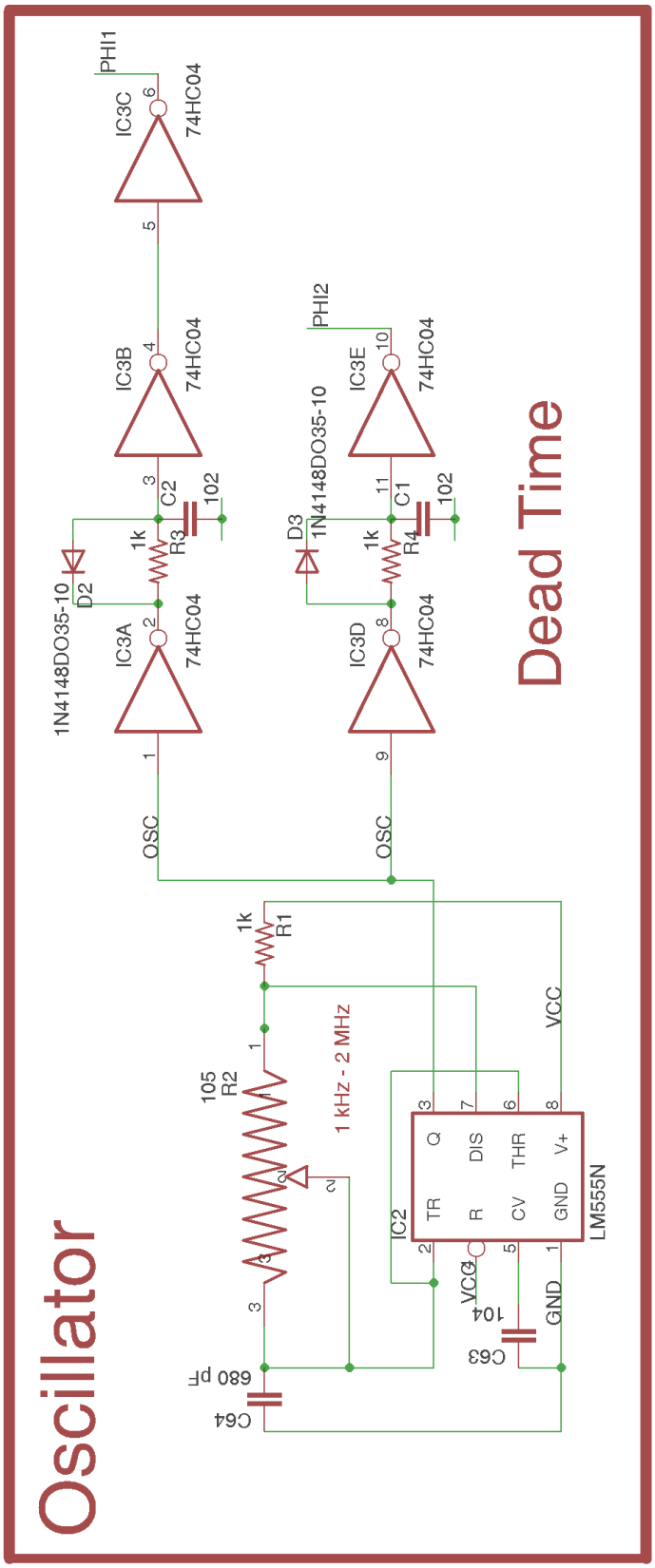


Figure C-11: Oscillator

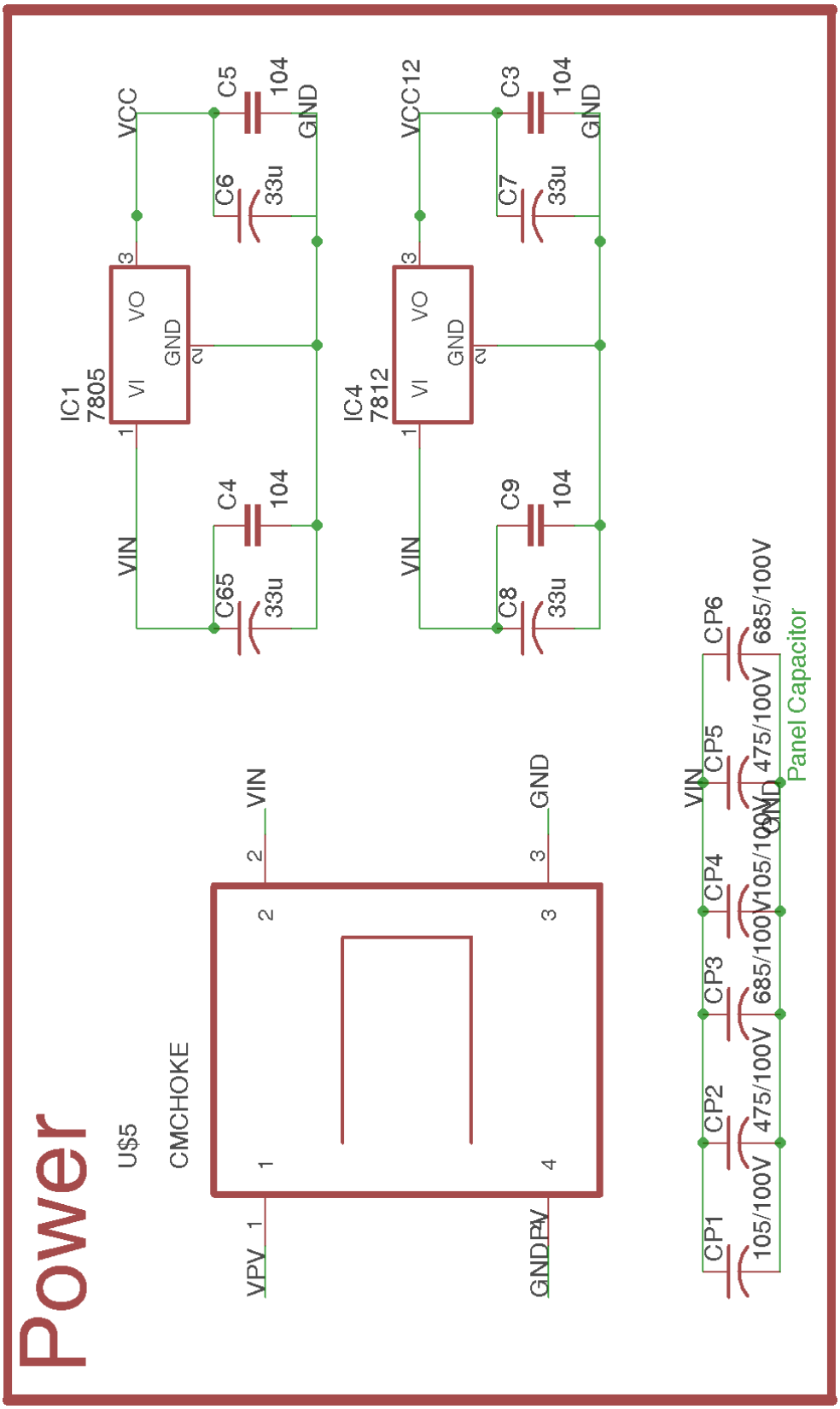


Figure C-12: Power

C.1.4 Build Notes

- Note that not all charge pumps need to be populated. Generally, for this experiment only the charge pumps for M3, M6, M9, and M10 need to be populated.
- CS pins on IR2125 are grounded; should be connected to Vs...will need to hack a fix on this rev of the PCB; and include it in any future revs..also see absolute max ratings in 2125 Datasheet Cs must be within Vs and Vb Gnd will destroy it
- Adjust deadtime timing resistor empirically
- Adjust zener bias diodes empirically or per time averaged source node voltage calculation
- Adjust Rg empirically
- Adjust Zener empirically
- Add antiparallel diodes to Rg (1N4148) with anode at gate.
- Missing Vcc diodes on IR2125's (1N4148 or MUR120)
- Oscillator is connected in such a way that D is not generally 50%. Remove 1k resistor, NC pin 7 on the 555 and connect the 1k resistor end of the pot to pin 3.
- The values of capacitors C11 and C12 and all analogous pairs are switched in the Eagle schematic. C11 should be 102, C12 should be 104

C.1.5 BOM

The Marx converter bill of materials is shown in the table below. Refer to Section 10.5 for changes.

Table C.1: Marx converter bill of materials.

Qty	Value	Device	Parts
24	1N4148DO35-10	1N4148DO35-10	D2, D3, D4, D6, D7, D9, D10, D12, D13, D15, D16, D18, D19, D21, D22, D24, D25, D27, D28, D30, D31, D33, D34, D36
3	1k	R-US-0207/10	R1, R3, R4
11	4	R-US-0207/10	RG1-11
11	4.7k	R-US-0207/10	R5, R7, R9, R11, R13, R15, R17, R19, R21, R23, R25
11	12V Zener	ZENER-DIODEDO41Z10	D5, D8, D11, D14, D17, D20, D23, D26, D29, D32, D35
1	12uF/300V	C-US275-205X316	COUT-3
4	33u	C-US050-050X075	C6, C7, C8, C65
1	74HC04	74ALS04N	IC3
11	100k	R-US-0207/10	R6, R8, R10, R12, R14, R16, R18, R20, R22, R24, R26
2	102	C2.5/6	C1, C2
11	102	C5/2.5	C12, C16, C20, C24, C28, C32, C36, C40, C44, C48, C52
11	103	C5/2.5	C13, C17, C21, C25, C29, C33, C37, C41, C45, C49, C53
38	104	C2.5/6	C3-5, C9, C10, C11, C14, C15, C18, C19, C22, C23, C26, C27, C30, C31, C34, C35, C38, C39, C42, C43, C46, C47, C50, C51, C54-63, C66, C67
1	105	BOURNEPOT3310Y001	R2
5	105/100V	C-US225-062X268	C1-1, C2-1, C3-1, CP1, CP4
2	105/250V	C-US225-087X268	COUT-1, COUT-2
5	475/100V	C-US225-062X268	C1-2, C2-2, C3-2, CP2, CP5
1	680 pF	C2.5/6	C64
5	685/100V	C-US225-087X268	C1-3, C2-3, C3-3, CP3, CP6
1	7805	7805TV	IC1
1	7812	7805TV	IC4
1	CMCHOKE	B82725A-CMCHOKE	U5
11	ICM755	LM555N	IC5, IC6, IC7, IC8, IC9, IC10, IC11-15
11	IR2125	IR2125	U6-16
11	IRF8721	FDS5680	M1-11
1	LM555N	LM555N	IC2
1	MBR20100C	MUR620CT	D1
11	SP4T	SW-C10	SW1-11
4	STANDOFF4-40	STANDOFF4-40	U17, U18, U19, U20

C.2 Matlab® Scripts for Switched-capacitor System Modeling

This Appendix includes MATLAB® scripts and functions for modeling the performance of a Marx converter system for distributed solar power processing.

C.2.1 Monte Carlo Performance Prediction

`montecarlo_Io_stepping.m`

This script iterates computations of the Marx converter performance through randomized panel lighting levels. It records the maximum efficiency for each iteration and averages the results among all of the iterations. The result is a statistical performance prediction of the Marx converter system. This script requires functions:

- `Io_sweep.m`
- `single_sim_single_Io.m`
- `etapsim_single_Io.m`
- `Qsim_single_Io.m`
- `Rout_lookup.m`
- `varycolor.m`

```
%% Perform many repeated simulations of the PV system having selected a
%% random distribution of normalized insolation levels across all of the
%% panels each time.  Avg the results to get a prediction of real avg
%% performance. (Montecarlo simulation)

%% Clear environment
clear
close all

%% Clear screen
clc

%% Inputs
% Figure
fig_no = 10;
```

```
Plotonly = 0;
Plot2D = 0;
Plot3D = 0;

Single_system = 1;
Diode_loss = 1;

%Load Data if Plotonly
if Plotonly == 1
    load matlab.mat
    Plotonly = 1;
end

% Circuit Elements
%C per level per module (i.e. the actual value of the capacitor C)
C = 12.5e-6;
Ron = 8.5e-3;          %FET Ron
Qg = 8.3e-9;           %Gate Charge (C)
Qoss = 5e-9;          %Qoss (C)
Qrr = 15e-9;          %Reverse recovery charge (C)
Vg = 10;              %Gate Drive Voltage (V)
fsw = 360e3;

% PV Parameters
Voc_nom = 29;
Vmp_nom = 24.6;
Isc_nom = 7.38;
Imp_nom = 6.93;

%Simulation Controls Converter Loss 1: ON or 0: OFF -> implemented in
%etapsim_single_Io based on Q, C, fsw, Ron
Ro = 1;
montecarlo_length  = 100;
Iomin = 0.01;
Iorescoarse = 20e-3;
Ioresfine = 20e-3;
Iorescoarse = Ioresfine;
Iomax = 6.93;
Qmin = 0;
Qres = 1;
Qmaxmax = 4;
min_number_of_sources = 3;
max_number_of_sources = 3;
Compress_range = 0.5;
 % Make 0 for Iosweep to select random Isc's or select a vector
 Isc_vec_norm = 0;

%% Check to make sure we can compute Ro for all switching patterns and stop if not
if Qmaxmax > 7 && Ro == 1
    disp('Dont have Ro values for Qmax > 7!!')
    return
end

%% Create simulation vectors
montecarlo_vec = 1:montecarlo_length;
Number_of_sources_vec = min_number_of_sources:max_number_of_sources;
if Single_system == 1
    Qmax_vec = Qmaxmax;
else
    Qmax_vec = 1:1:Qmaxmax;
end
```

```
if Plotonly == 0
    montecarlo_avg_etap_array = [];
    montecarlo_avg_etac_array = [];
    montecarlo_avg_eta_array = [];
    for Qmax = Qmax_vec
        %% Check Rout Lookup getting etc = 100% for Qmax = 1 case not right
        Q_avail = Qmin:Qres:Qmax;   %Varying Q_avail (reset Qmax each time)
        montecarlo_avg_etap_vec = [];
        montecarlo_avg_etac_vec = [];
        montecarlo_avg_eta_vec = [];
        for Number_of_sources = Number_of_sources_vec
            etap_vec = [];
            etac_vec = [];
            eta_vec = [];
            for i = montecarlo_vec
                Qmax
                Q_avail;
                Number_of_sources
                Montecarlo_N = i
                results_array = Io_sweep(Iomin, Ioresfine, Iorescoarse, ...
                    Iomax, Q_avail, Number_of_sources, Voc_nom, Vmp_nom, ...
                    Isc_nom, Imp_nom, Ro, C, fsw, Ron, Qg, Qoss, Qrr, Vg, ...
                    Compress_range, Isc_vec_norm, Diode_loss);
                etap = results_array(:,1);
                etac = results_array(:,2);
                eta = results_array(:,3);
                % Find etamax index
                etamax = max(eta);
                etamax_index = find(etamax == eta);
                if length(etamax_index) > 1  % only want one
                    etamax_index = etamax_index(1);
                end
                % Find etap etac and eta at etamax index
                etapmax = etap(etamax_index);
                etacmax = etac(etamax_index);
                % Concatenate onto results vectors
                etap_vec = horzcat(etap_vec, etapmax);
                etac_vec = horzcat(etac_vec, etacmax);
                eta_vec = horzcat(eta_vec, etamax);
            end
            montecarlo_avg_etap_vec = horzcat(montecarlo_avg_etap_vec, ...
                mean(etap_vec));
            montecarlo_avg_etac_vec = horzcat(montecarlo_avg_etac_vec, ...
                mean(etac_vec));
            montecarlo_avg_eta_vec = horzcat(montecarlo_avg_eta_vec, ...
                mean(eta_vec));
        end
        montecarlo_avg_etap_array = vertcat(montecarlo_avg_etap_array, ...
            montecarlo_avg_etap_vec)
        montecarlo_avg_etac_array = vertcat(montecarlo_avg_etac_array, ...
            montecarlo_avg_etac_vec)
        montecarlo_avg_eta_array = vertcat(montecarlo_avg_eta_array, ...
            montecarlo_avg_eta_vec)
    end
end

%% Extract converter efficiency from etap and eta: eta = etap*etac
% montecarlo_avg_etac_array =
% 100*montecarlo_avg_eta_array./montecarlo_avg_etap_array;
```

```
%% Data Plotting
Iores = Ioresfine;
if Ro == 0
    Rout = sprintf('Off');
else
    Rout = sprintf('On');
end

% 2D
if Plot2D == 1
    %etap
    figure
%     title_array = {['Tracking Efficiency vs. Number of Sources across
%     Q_{max}'];['Q_{avail} = [' num2str(Qmin) ':' num2str(Qres)
%     ':Q_{max}], Montecarlo Length = '
%     num2str(montecarlo_length)];['I_{o,sweep} = [' num2str(Iomin) ':'
%     num2str(Iores) ':' num2str(Iomax) '] A, Conv. Loss = [' Rout ']'];['C
%     = ' num2str(1e6*C) ' \muF, f_{sw} = ' num2str(fsw/1000) ' kHz,
%     R_{dson} = ' num2str(Ron*1000) ' m\Omega, Q_{g} =  ' num2str(Qg*1e9)
%     ' nC,  Q_{oss} = ' num2str(Qoss*1e9) ' nC, Q_{rr} = '
%     num2str(1e9*Qrr) ' nC, V_g = ' num2str(Vg) ' V'];['V_{oc} = '
%     num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) ' V, I_{sc} = '
%     num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Distribution Compression  = ' num2str(100*Compress_range)
%     '%']};
    legend_vec = [];
    legend_vec = Qmax_vec';
    ColorSet = varycolor(length(legend_vec));
    set(gca, 'ColorOrder', ColorSet);
    hold all;
    plot(Number_of_sources_vec,montecarlo_avg_etap_array');
    %% Plot Formatting
    ylabel('\eta_p (%)')
    xlabel('Number of Sources')
    title(title_array);
    grid on
    box on
    drawnow
    legend(num2str(legend_vec),'Location','Best');

    %etac
    figure
%     title_array = {['Converter Efficiency vs. Number of Sources across
%     Q_{max}'];['Q_{avail} = [' num2str(Qmin) ':' num2str(Qres)
%     ':Q_{max}], Montecarlo Length = '
%     num2str(montecarlo_length)];['I_{o,sweep} = [' num2str(Iomin) ':'
%     num2str(Iores) ':' num2str(Iomax) '] A, Conv. Loss = [' Rout ']'];['C
%     = ' num2str(1e6*C) ' \muF, f_{sw} = ' num2str(fsw/1000) ' kHz,
%     R_{dson} = ' num2str(Ron*1000) ' m\Omega, Q_{g} =  ' num2str(Qg*1e9)
%     ' nC,  Q_{oss} = ' num2str(Qoss*1e9) ' nC, Q_{rr} = '
%     num2str(1e9*Qrr) ' nC, V_g = ' num2str(Vg) ' V'];['V_{oc} = '
%     num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) ' V, I_{sc} = '
%     num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Distribution Compression  = ' num2str(100*Compress_range)
%     '%']};
    legend_vec = [];
    legend_vec = Qmax_vec';
    ColorSet = varycolor(length(legend_vec));
    set(gca, 'ColorOrder', ColorSet);
    hold all;
    plot(Number_of_sources_vec,montecarlo_avg_etac_array');
```

```
    %% Plot Formatting
    ylabel('\eta_c (%)')
    xlabel('Number of Sources')
    title(title_array);
    grid on
    box on
    drawnow
    legend(num2str(legend_vec),'Location','Best');

    %eta
    figure
%     title_array = {['Total Efficiency vs. Number of Sources across
%     Q_{max}']};['Q_{avail} = [' num2str(Qmin) ':' num2str(Qres)
%     ':Q_{max}], Montecarlo Length = '
%     num2str(montecarlo_length)];['I_{o,sweep} = [' num2str(Iomin) ':'
%     num2str(Iores) ':' num2str(Iomax) '] A, Conv. Loss = [' Rout ']'];['C
%     = ' num2str(1e6*C) ' \muF, f_{sw} = ' num2str(fsw/1000) ' kHz,
%     R_{dson} = ' num2str(Ron*1000) ' m\Omega, Q_{g} =  ' num2str(Qg*1e9)
%     ' nC,  Q_{oss} = ' num2str(Qoss*1e9) ' nC, Q_{rr} = '
%     num2str(1e9*Qrr) ' nC, V_g = ' num2str(Vg) ' V'];['V_{oc} = '
%     num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) ' V, I_{sc} = '
%     num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Distribution Compression  = ' num2str(100*Compress_range)
%     '%']};
    legend_vec = [];
    legend_vec = Qmax_vec';
    ColorSet = varycolor(length(legend_vec));
    set(gca, 'ColorOrder', ColorSet);
    hold all;
    plot(Number_of_sources_vec,montecarlo_avg_eta_array');
    %% Plot Formatting
    ylabel('\eta (%)')
    xlabel('Number of Sources')
    title(title_array);
    grid on
    box on
    drawnow
    legend(num2str(legend_vec),'Location','Best');
end

%3D
if Plot3D == 1

    % etap
    figure
%     title_array = {['Tracking Efficiency vs. Number of Sources across
%     Q_{max}']};['Q_{avail} = [' num2str(Qmin) ':' num2str(Qres)
%     ':Q_{max}], Montecarlo Length = '
%     num2str(montecarlo_length)];['I_{o,sweep} = [' num2str(Iomin) ':'
%     num2str(Iores) ':' num2str(Iomax) '] A, Conv. Loss = [' Rout ']'];['C
%     = ' num2str(1e6*C) ' \muF, f_{sw} = ' num2str(fsw/1000) ' kHz,
%     R_{dson} = ' num2str(Ron*1000) ' m\Omega, Q_{g} =  ' num2str(Qg*1e9)
%     ' nC,  Q_{oss} = ' num2str(Qoss*1e9) ' nC, Q_{rr} = '
%     num2str(1e9*Qrr) ' nC, V_g = ' num2str(Vg) ' V'];['V_{oc} = '
%     num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) ' V, I_{sc} = '
%     num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Distribution Compression  = ' num2str(100*Compress_range)
%     '%']};
    surf(Number_of_sources_vec, Qmax_vec, montecarlo_avg_etap_array);
    %% Plot Formatting
    zlabel('\eta_p (%)')
```

```
    ylabel('Q_{max}')
    xlabel('Number of Sources')
    title(title_array);
    grid on
    box on
    drawnow

    % etac
    figure
%     title_array = {['Converter Efficiency vs. Number of Sources across
%     Q_{max}'];['Q_{avail} = [' num2str(Qmin) ':' num2str(Qres)
%     ':Q_{max}], Montecarlo Length = '
%     num2str(montecarlo_length)];['I_{o,sweep} = [' num2str(Iomin) ':'
%     num2str(Iores) ':' num2str(Iomax) '] A, Conv. Loss = [' Rout ']'];['C
%     = ' num2str(1e6*C) ' \muF, f_{sw} = ' num2str(fsw/1000) ' kHz,
%     R_{dson} = ' num2str(Ron*1000) ' m\Omega, Q_{g} =  ' num2str(Qg*1e9)
%     ' nC,  Q_{oss} = ' num2str(Qoss*1e9) ' nC, Q_{rr} = '
%     num2str(1e9*Qrr) ' nC, V_g = ' num2str(Vg) ' V'];['V_{oc} = '
%     num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) ' V, I_{sc} = '
%     num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Distribution Compression  = ' num2str(100*Compress_range)
%     '%']};
    surf(Number_of_sources_vec, Qmax_vec, montecarlo_avg_etac_array);
    %% Plot Formatting
    zlabel('\eta_c (%)')
    ylabel('Q_{max}')
    xlabel('Number of Sources')
    title(title_array);
    grid on
    box on
    drawnow

    % eta
    figure
%     title_array = {['Total Efficiency vs. Number of Sources across
%     Q_{max}'];['Q_{avail} = [' num2str(Qmin) ':' num2str(Qres)
%     ':Q_{max}], Montecarlo Length = '
%     num2str(montecarlo_length)];['I_{o,sweep} = [' num2str(Iomin) ':'
%     num2str(Iores) ':' num2str(Iomax) '] A, Conv. Loss = [' Rout ']'];['C
%     = ' num2str(1e6*C) ' \muF, f_{sw} = ' num2str(fsw/1000) ' kHz,
%     R_{dson} = ' num2str(Ron*1000) ' m\Omega, Q_{g} =  ' num2str(Qg*1e9)
%     ' nC,  Q_{oss} = ' num2str(Qoss*1e9) ' nC, Q_{rr} = '
%     num2str(1e9*Qrr) ' nC, V_g = ' num2str(Vg) ' V'];['V_{oc} = '
%     num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) ' V, I_{sc} = '
%     num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Distribution Compression  = ' num2str(100*Compress_range)
%     '%']};
    surf(Number_of_sources_vec, Qmax_vec, montecarlo_avg_eta_array);
    %% Plot Formatting
    zlabel('\eta (%)')
    ylabel('Q_{max}')
    xlabel('Number of Sources')
    title(title_array);
    grid on
    box on
    drawnow

end
```

Io_sweep.m

This function returns all of the results for a single string current sweep.

```
%% Sweep Io to find global MPPT in Io stepping system
function results_array = Io_sweep(Iomin, Ioresfine, Iorescoarse, ...
    Iomax, Q_avail, Number_of_sources, Voc_nom, Vmp_nom, Isc_nom, ...
    Imp_nom, Ro, C, fsw, Ron, Qg, Qoss, Qrr, Vg, Compress_range, ...
    Isc_vec_norm, Diode_loss)

%% Clear screen
% clc

%% Plot?
Plot_on = 0;

%% Choose Isc's: If Isc_vec_norm = 0, choose random Isc's else use the
%% given Isc_vec_norm.
if Isc_vec_norm == 0
    Isc_vec_norm = [];
    for i = 1:Number_of_sources
        Isc_vec_norm = horzcat(Isc_vec_norm, (1-Compress_range+...
            Compress_range*rand));
    end
end

%% Coarse Sweep to localize MPP: results = [etap eta and Q]
if Ioresfine ~= Iorescoarse
    Io_vec_coarse = Iomin:Iorescoarse:Iomax;
    results_array_coarse = [];
    for Io = Io_vec_coarse
        Io;
        results = single_sim_single_Io(Q_avail, Isc_vec_norm, ...
            Voc_nom, Vmp_nom, Isc_nom, Imp_nom, Ro, C, fsw, Ron,...
            Qg, Qoss, Qrr, Vg, Io);
        results = horzcat(results, Io, Isc_vec_norm);
        results_array_coarse = vertcat(results_array_coarse, results);
    end

    %% Determine ballpark max Io
    Ballparkmax_Io = Io_vec_coarse(find(max(results_array_coarse(:,1))...
        == results_array_coarse(:,1)));
    Iominfine = Ballparkmax_Io-Iorescoarse;
    Iomaxfine = Ballparkmax_Io+Iorescoarse;
else
    Iominfine = Iomin;
    Iomaxfine = Iomax;
end

%% Fine Sweep: results = [etap eta and Q]
% Bound Io sweep
Io_vec_fine = Iominfine:Ioresfine:Iomaxfine;
results_array_fine = [];
for Io = Io_vec_fine
    Io;
    [etap etac eta Q] = single_sim_single_Io(Q_avail, Isc_vec_norm, ...
        Voc_nom, Vmp_nom, Isc_nom, Imp_nom, Ro, C, fsw, Ron, Qg, Qoss, ...
        Qrr, Vg, Io, Diode_loss);
    results_array_fine = vertcat(results_array_fine, ...
        [etap etac eta Q Io Isc_vec_norm]);
end
```

```
%% Reporting
results_array = results_array_fine;

%% Data Plotting if Plot_on == 1
if Plot_on == 1
    MPP_etap = max(results_array_fine(:,1));
    if Ro == 0
        Rout = sprintf('Off');
    else
        Rout = sprintf('On');
    end
    figure
    plot(Io_vec_fine, results_array_fine(:,1))
%     title({['Tracking Efficiency vs. Output
%     Current'];[num2str(Number_of_sources) ' sources'];['Q_{avail} = ['
%     num2str(Q_avail) '], Coarse \Delta I_o = ' num2str(1000*Iorescoarse)
%     ' mA, Fine \Delta I_o = ' num2str(1000*Ioresfine) ' mA, Conv. Loss =
%     [' Rout ']'];['Imp_{vec} = [' num2str(Imp_nom*Isc_vec_norm) ']
%     A'];['V_{oc} = ' num2str(Voc_nom) ' V, V_{mp} = ' num2str(Vmp_nom) '
%     V, I_{sc} = ' num2str(Isc_nom) ' A, I_{mp} = ' num2str(Imp_nom) '
%     A'];['Max Power \eta_p = ' num2str(MPP_etap) '%']})
    xlabel('I_o (A)')
    ylabel('\eta_p (%)')
    grid
    box on

    if Ioresfine ~= Iorescoarse
        plot(Io_vec_coarse, results_array_coarse(:,1))
        xlabel('I_o (A)')
        ylabel('\eta_p (%)')
        grid
        box on
    end
end
% Isc_vec_norm

end
```

`single_sim_single_Io.m`

This function returns the efficiencies and conversion ratios for a single string current value.

```
function [etap etac eta Q] = single_sim_single_Io(Q_avail, Isc_vec_norm, ...
    Voc_nom, Vmp_nom, Isc_nom, Imp_nom, Ro, C, fsw, Ron,  Qg, Qoss, Qrr, ...
    Vg, Io, Diode_loss)
%% A single Marx PV system simulation returning a set of Qs and etap

%% Clear screen
% clc

%% Determine number of sources from length of Isc vector
Number_of_sources = length(Isc_vec_norm);

%% Define Panels
Voc_vec = [];
Isc_vec = [];
Vmp_vec = [];
Imp_vec = [];

% This assumes Imp_nom is given (known to the manufacturer) and that Imp is
% linearly proporitional to Isc which is measured in runtime.  Vmp can be
% arbitrary since we are matching Iin to Imp which is unique to the
% maximum power point and thus to the correct Vmp.
% For simplicity and without significant loss of generality we can assume
% that Vmp is fixed.
for j = 1:Number_of_sources
    Isc_norm = Isc_vec_norm(j);
    Imp = Isc_norm*Imp_nom;
    Isc = Isc_norm*Isc_nom;
    Vmp = Vmp_nom;
    Voc = Voc_nom;
    Imp_vec = horzcat(Imp_vec, Imp);
    Isc_vec = horzcat(Isc_vec, Isc);
    Vmp_vec = horzcat(Vmp_vec, Vmp);
    Voc_vec = horzcat(Voc_vec, Voc);
end

%% Calculate PV model parameters as on P. 14 of book 9/10-
Rs_vec = [];
Rp_vec = [];
for j = 1:Number_of_sources
    Rs_vec = horzcat(Rs_vec, (Voc_vec(j)-Vmp_vec(j))./Imp_vec(j));
    Rp_vec = horzcat(Rp_vec, (Isc_vec(j)*Rs_vec(j)-Voc_vec(j))/(Imp_vec(j)...
        -Isc_vec(j)));
end

%% Determine actual Photovoltaic Currents as on P.14 of book 9/10-
Iph_vec = [];
for j = 1:Number_of_sources
    Iph_vec = horzcat(Iph_vec,Imp_vec(j)+Voc_vec(j)/Rp_vec(j));
end

%% Define MP's
MP_vec = [];
for j = 1:Number_of_sources
    MP_vec = horzcat(MP_vec, Imp_vec(j)*Vmp_vec(j));
end
```

```
%% Find Q
Q = Qsim_single_Io(Imp_vec, Io, Q_avail);

%% Compute etap etac and eta
[etap etac eta] =  etapsim_single_Io(Number_of_sources, Iph_vec, ...
    Imp_vec, Voc_vec, Rs_vec, Rp_vec, Q, MP_vec, Ro, C, fsw, Ron, ...
    Qg, Qoss, Qrr, Vg, Q_avail, Io, Diode_loss);

return
```

`etapsim_single_Io.m`

This function returns the efficiencies achieved for a single string current.

```
function [etap etac eta] = etapsim_single_Io(Number_of_sources, ...
    Iph_vec, Imp_vec, Voc_vec, Rs_vec, Rp_vec, Q, MP_vec, Ro, C, ...
    fsw, Ron, Qg, Qoss, Qrr, Vg, Q_avail, Io, Diode_loss)
%% Compute the tracking efficiency given a set of Qs

%% Calculate Pin of each panel as on P. 2 attachment book 9/10-
Pin_vec = [];
Iin_vec = [];
Vin_vec = [];
Vo_vec = [];
Rout_vec = [];
Pswloss_vec = [];
Vdrev_vec = [];

% Ouput Diode
Cd = 10e-12;    % Output Diode Capacitance
Is = 159e-6;    % Output Diode Is
n = 1.76;       % Output Diode Quality factor
ESRd = 0.02;      % Output Diode ESR
kTonq = 25e-3;
Vd = log(Io/Is+1)*n*kTonq+ESRd*Io;  % Output Diode ideal voltage

for j = 1:Number_of_sources
    Iin = Q(j)*Io;

    % Nonlinear equations for Vin depend on state of PV Diode
    if Iin < Imp_vec(j)  %%Diode on
        Vin = Voc_vec(j)-Iin*Rs_vec(j);
    elseif Iin >= Imp_vec(j)  %% Diode off
        Vin = Rp_vec(j)*Iph_vec(j)-(Rs_vec(j)+Rp_vec(j))*Iin;
    end

    % Handle the Q = 0 Case: Load is open not shorted (Vin = Voc not 0 V)
    if Q(j) == 0
        Vin = Voc_vec(j);
        Iin = 0;        % Redundant to Iin = Q(j)*Io
    end

    % Compute Pin
    Pin = Iin*Vin;

    % Nan Checking
    if isnan(Vin)       % if Vin = 0/0 set it to 0
        Vin = 0;
    end
    if isnan(Iin)       % if Iin = 0/0 set it to 0
        Iin = 0;
    end
    if isnan(Pin)       % if Pin = 0/0 set it to 0
        Pin = 0;
    end

    % Lossless or not
    if Ro ~= 0
        Rout = Rout_lookup(Q_avail, Q(j), C, fsw, Ron);
    else
        Rout = 0;
```

```
        Qg = 0;
        Qoss = 0;
        Qrr = 0;
    end

    % Find switching loss as a function of Vin
    % Number of active switches
    if Q(j) ~= 0
        N = 3*Q(j)-2;
    elseif Q(j) == 0
        N = 1;
    end
    Pswloss = N*(Qg*Vg*fsw+0.5*Qoss*abs(Vin)*fsw+Qrr*abs(Vin)*fsw);

    % Enumerate the results
    Rout_vec = horzcat(Rout_vec, Rout);
    Pswloss_vec = horzcat(Pswloss_vec, Pswloss);
    Vin_vec = horzcat(Vin_vec, Vin);
    Iin_vec = horzcat(Iin_vec, Iin);
    Pin_vec = horzcat(Pin_vec, Pin);
    Vo_vec = horzcat(Vo_vec,Q(j)*Vin);
    Vdrev_vec = horzcat(Vdrev_vec,Q(j)*Vin-Vin);
end
% Debugging and Op. Pt reporting
% Vin_vec
% Iin_vec
% Vo_vec
% Pin_vec
% Print initial conditions referenced to gnd to help with LTSPICE
% Vin1 = Vin_vec(1)
% Vin2 = Vo_vec(1)+Vin_vec(2)
% Vin3 = Vo_vec(1)+Vo_vec(2)+Vin_vec(3)
% Vo1 = Vo_vec(1)
% Vo2 = Vo_vec(1)+Vo_vec(2)
% Vo = sum(Vo_vec)

%% Calculate tracking efficiency etap
Pin = sum(Pin_vec);
MPtot = sum(MP_vec);
Rout_tot = sum(Rout_vec);

% Pdiodeloss_tot = Io*Vd+ESRd*Io^2;
if Diode_loss == 1
    Pdiodeloss_tot = Number_of_sources*Io*Vd+...
        fsw*Cd*sum(Vdrev_vec.*Vdrev_vec);
else
    Pdiodeloss_tot = 0;
end
Pswloss_tot = sum(Pswloss_vec);
Prloss_tot = Rout_tot*Io^2;
Ploss = Pswloss_tot + Prloss_tot + Pdiodeloss_tot;
Pout = Pin-Ploss;
% Not interested in Negative Power conditions
if Pout < 0
    Pin = 0;
    Pout = 0;
end

%% Reporting: report the maximum etap found
etap = 100*Pin/MPtot;
etac = 100*Pout/Pin;
```

```
eta = 100*Pout/MPtot;

% NaN checking Pin = 0 -> all Q = 0
if isnan(etac)        % if etac = 0/0 set it to 0
    etac = 100;
end

return
```

`Qsim_single_Io.m`

This function returns the conversion ratios for a set of Marx converters for a single string current based on the local maximum power point tracking algorithm.

```
function Q_vec = Qsim_single_Io(Imp_vec, Io, Q_avail)
%% A simulation of the set of Q's determined by each module independently
%% of the others having a fixed Io and set of available Q's.
% clc

%% Beginialize the variables
Q_vec = [];
Iin_avail = [];
Number_of_sources = length(Imp_vec);

%% Determine the set of available input currents given this Io
Iin_avail = Q_avail*Io;

%% Distribute panels into their appropriate Q's
for j = 1:Number_of_sources
    Source = j;
    Iin_error = Imp_vec(j)-Iin_avail;
    neg_indices = find(sign(Iin_error) == -1);
    pos_indices = find(sign(Iin_error) == 1);
    zer_indices = find(sign(Iin_error) == 0);
    Iin_error_neg = Iin_error(neg_indices);
    Iin_error_pos = Iin_error(pos_indices);
    Iin_error_zer = Iin_error(zer_indices);

    % Would like Iin = Imp, Iin < Imp, Iin > Imp in that order of
    % preference.  Pin diminishes slowly as Iin decreases beyond Imp but
    % decreases abruptly as Iin increases beyond Imp.
    if length(Iin_error_zer ~= 0)
        Q_index = zer_indices(1);
    elseif length(Iin_error_pos ~=0)
        pos_index = find(abs(Iin_error_pos) == min(abs(Iin_error_pos)));
        Q_index = pos_indices(pos_index);
    elseif length(Iin_error_neg ~= 0)
        neg_index = find(abs(Iin_error_neg) == min(abs(Iin_error_neg)));
        Q_index = neg_indices(neg_index);
    end
        %also only want one index not a whole bunch
    if length(Q_index > 1)
        Q_index = Q_index(1);
    end
        Q = Q_avail(Q_index);
        Q_vec = horzcat(Q_vec, Q);
end

%% Reporting
return
```

`Rout_lookup.m`

This function returns the effective output resistance value for a Marx converter given the switched-capacitor value, the switching frequency and the MOSFET on resistance value.

```
function result = Rout_lookup(Q_avail, Q, C, fsw, Ron)

%% Multiplier arrays
%Check these arrays for accuracy especially regarding Q = 0 cases, then go
%back and make sure FET selection script is also accurate
     %Qmax = 1   2   3   4   5   6   7
Rssl_mult = [0   0   0   0   0   0   0;     % Q = 0
             0   0   0   0   0   0   0;     % Q = 1
             0   1   1/2 1/3 1/4 1/5 1;     % Q = 2
             0   0   2   3/2 1   5/6 2/3;   % Q = 3
             0   0   0   3   5/2 2   3/2;   % Q = 4
             0   0   0   0   4   7/2 3;     % Q = 5
             0   0   0   0   0   5   9/2;   % Q = 6
             0   0   0   0   0   0   6      % Q = 7
            ];

    %Qmax = 1       2       3       4       5       6       7
Rfsl_mult = [2      4       6       8       10      12      14;     % Q = 0
             2      4       6       8       10      12      14;     % Q = 1
             0      8       10      12.444  8.2     17.6    32.39;  % Q = 2
             0      0       26      24      38      48.4    50.8;   % Q = 3
             0      0       0       64      90      100     100;    % Q = 4
             0      0       0       0       130     180     206;    % Q = 5
             0      0       0       0       0       232     307;    % Q = 6
             0      0       0       0       0       0       378     % Q = 7
            ];

%% Compute absolute SSL and FSL Rout values
Rssl = Rssl_mult(Q+1,max(Q_avail))*1/(C*fsw);
Rfsl = Rfsl_mult(Q+1,max(Q_avail))*Ron;

%% FSL or SSL
Rout = max(Rssl,Rfsl);

%% Reporting
result = Rout;

end
```

varycolor.m

This function was written by Daniel Helmick and was found at MATLAB Central online. It was used to control the 3D mesh color gradient in the output plots from the Monte Carlo simulations.

```
function ColorSet=varycolor(NumberOfPlots)
% VARYCOLOR Produces colors with maximum variation on plots with multiple
% lines.
%
%     VARYCOLOR(X) returns a matrix of dimension X by 3.  The matrix may be
%     used in conjunction with the plot command option 'color' to vary the
%     color of lines.
%
%     Yellow and White colors were not used because of their poor
%     translation to presentations.
%
%     Example Usage:
%          NumberOfPlots=50;
%
%          ColorSet=varycolor(NumberOfPlots);
%
%          figure
%          hold on;
%
%          for m=1:NumberOfPlots
%              plot(ones(20,1)*m,'Color',ColorSet(m,:))
%          end

%Created by Daniel Helmick 8/12/2008

error(nargchk(1,1,nargin))%correct number of input arguements??
error(nargoutchk(0, 1, nargout))%correct number of output arguements??

%Take care of the anomolies
if NumberOfPlots<1
    ColorSet=[];
elseif NumberOfPlots==1
    ColorSet=[0 1 0];
elseif NumberOfPlots==2
    ColorSet=[0 1 0; 0 1 1];
elseif NumberOfPlots==3
    ColorSet=[0 1 0; 0 1 1; 0 0 1];
elseif NumberOfPlots==4
    ColorSet=[0 1 0; 0 1 1; 0 0 1; 1 0 1];
elseif NumberOfPlots==5
    ColorSet=[0 1 0; 0 1 1; 0 0 1; 1 0 1; 1 0 0];
elseif NumberOfPlots==6
    ColorSet=[0 1 0; 0 1 1; 0 0 1; 1 0 1; 1 0 0; 0 0 0];

else %default and where this function has an actual advantage

    %we have 5 segments to distribute the plots
    EachSec=floor(NumberOfPlots/5);

    %how many extra lines are there?
    ExtraPlots=mod(NumberOfPlots,5);

    %initialize our vector
```

```
    ColorSet=zeros(NumberOfPlots,3);

    %This is to deal with the extra plots that don't fit nicely into the
    %segments
    Adjust=zeros(1,5);
    for m=1:ExtraPlots
        Adjust(m)=1;
    end

    SecOne   =EachSec+Adjust(1);
    SecTwo   =EachSec+Adjust(2);
    SecThree =EachSec+Adjust(3);
    SecFour  =EachSec+Adjust(4);
    SecFive  =EachSec;

    for m=1:SecOne
        ColorSet(m,:)=[0 1 (m-1)/(SecOne-1)];
    end

    for m=1:SecTwo
        ColorSet(m+SecOne,:)=[0 (SecTwo-m)/(SecTwo) 1];
    end

    for m=1:SecThree
        ColorSet(m+SecOne+SecTwo,:)=[(m)/(SecThree) 0 1];
    end

    for m=1:SecFour
        ColorSet(m+SecOne+SecTwo+SecThree,:)=[1 0 (SecFour-m)/(SecFour)];
    end

    for m=1:SecFive
        ColorSet(m+SecOne+SecTwo+SecThree+SecFour,:)=[(SecFive-m)/(SecFive) 0 0];
    end

end
```

Appendix D

Switched-capacitor DC/DC Marx Converter Loss Models

D.1 Introduction

The primary goal of this work was to develop a starting point for generalizations in loss modeling of DC/DC switched-capacitor marx converters, building from the work in [30] by Seemen et. al. This work generally attempts to treat the marx converter as a specific type of switched-capacitor converter. However, we will study how the marx converter fundamentally compares and contrasts to other types of switched-capacitor converters based on the choice of switching pattern. The result of that discussion will be a proposed classification of marx converter configurations based on switching patterns.

We can recognize the marx converter as both a switched-capacitor and a multilevel output converter. The motivation here is to exploit the marx converter as an inductor-less boosting multilevel DC/DC converter (it may be used, although under-utilized, as a bucking DC/DC converter as well). Specifying the DC/DC case as opposed to the DC/AC case basically indicates a load with a large enough capacitance to maintain a fixed steady state output voltage over the timescale of one switching period. One example will show how the efficiency and load regulation behavior of the converter is fundamentally altered when leaving the big load capacitance limit. The implica-

tions of switch implementation and its effect on the fundamental operation of these converters will also be discussed later.

D.1.1 Literature Review

This work builds from the work by Seeman in [30]. Seeman describes a new framework for analyzing switched-capacitor circuits that results in simple-to-understand two-port models like that shown in Figure D-1. In Figure D-1, the ideal transformer models the conversion from input to open-circuit output voltage and the output resistance R_O, captures both load regulation and loss in the circuit. The intent of this work was to apply Seeman's framework to the marx converter.

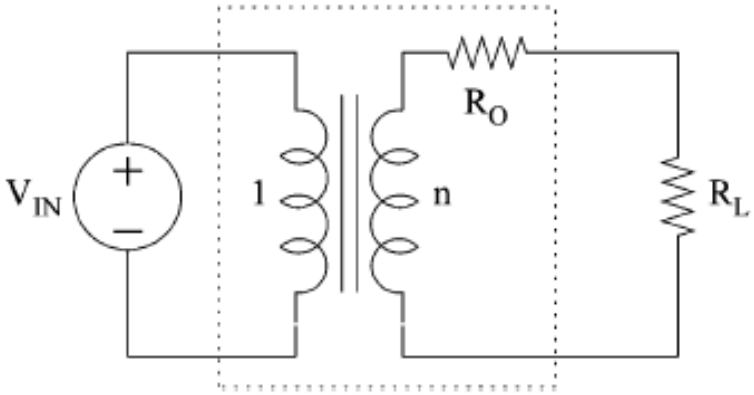


Figure D-1: The simple two-port model of switched-capacitor DC/DC converters proposed by Seeman. The model captures open-circuit voltage, load regulation and loss with one ideal transformer and one resistor [30].

Reference [184] by Maksimovic:PESC95 and Makowski provides analyses and modeling of switched-capacitor converters that motivated Seeman to develop his new straight forward abstractions. References [185–189] describe analyses of specific types of switched-capacitor converters including so-called "voltage-multiplier" converters and multilevel DC/DC converters. The principle result in reference [186] is a generalized two-port model of the AC/DC voltage multiplier circuit in what amounts to the slow-switching-limit (SSL). In reference [185], a similar analysis is carried for AC/DC voltage multiplier circuits in what amounts to the fast-switching-limit (FSL). Reference [190] presents the two-port model from Figure D-1 for an FSL step-down

switched-capacitor converter. Reference [187] details the losses in a multilevel flying capacitor DC/DC converter using both energy methods for capacitor balancing and enumerating power dissipated in conducting interconnects.

The main difference between the previous work and the work of Seemen et. al. is in the simplified abstractions that he presents for both the switching speed limits. These abstractions are drawn from a fundamental understanding of the loss mechanisms. This work uses Seeman's framework when it is applicable, but also uses straight forward circuit analysis similar to that in the references described above, when the framework is not applicable. Seemen's framework is reviewed in Section D.6.

Reference [190] provides references for review and examples of control techniques for multilevel output converters. In particular, it focuses on the modulation technique for DC output multi-level converters that is the crux of the switching pattern described in Section D.7. In this modulation technique, the output is modulated between the two levels that span the desired steady-state output voltage.

D.1.2 Analytical and Model Validation Approaches in this Work

The analysis of marx converters here focuses on load regulation and loss modeling. For now, each switching pattern studied is assumed to be implemented with finite on-resistance switches that can block voltage and carry current in both directions. Practical switch implementations must be carefully chosen to actually achieve the behaviors developed here. That being said, switch implementations might also be chosen to fundamentally alter the behaviors developed here. This will be discussed further in Section D.8.

While the marx converter may be extended to an arbitrary number of output voltage levels, the analysis here attempts to understand its load regulation and loss behavior across the fundamental types of switching patterns by first focusing only on the three-level cases (the simplest form of the marx converter). Section D.6 contains an example in which the model is extended to four levels.

Model validation was carried out in simulation with LTSPICE. I found it easier to model converter behavior across effective switching frequency regimes by varying the switched-capacitor and output capacitor values, rather than actually varying the switching frequency. By varying these capacitor values, I was able to model the transition between the slow-switching-limit (SSL) and the fast-switching-limit (FSL) behaviors without adjusting switching frequency and all of the ancillary values that would require. Therefore, capacitor values that seem impractically large in simulation, are only that way to demonstrate relative switching speed. In those cases, a practical implementation of the converter could just as easily contain more reasonable capacitor values but with an increased switching frequency instead.

Switch on-resistances are often assumed to be equal in the analyses and are always held at $R_{on} = 10m\Omega$ in the simulations here.

D.2 Switching Speed Limit Definitions

As described by Seeman et. al., in the slow-switching-limit (SSL), the switched-capacitors fully equilibrate so that capacitor currents can be modeled as impulsive, reaching nearly zero Amps in a time that is very small compared to the switching period [30]. On the other hand, in the fast-switching-limit (FSL), the switched-capacitors maintain fixed voltages and capacitor currents during each switching state are constant [30]. The plots of capacitor voltage and current in both switching limits shown in Figure D-2 demonstrate these points for a simulated 3-level marx converter.

The two switching speed limits can be understood by considering the classic capacitor charging loss problem depicted in Figure D-3. The loss associated with charging the capacitor from $V_C(0)$ for a time, t, can be found as follows. The total energy lost is

$$E_{tot} = \int_{t=o}^{\infty} I_C(\tau)^2 R d\tau \tag{D.1}$$

where, by inspection the capacitor voltage is

$$V_C(t) = (V_{in} - V_C(0))(1 - e^{-t/RC}) + V_C(0) \tag{D.2}$$

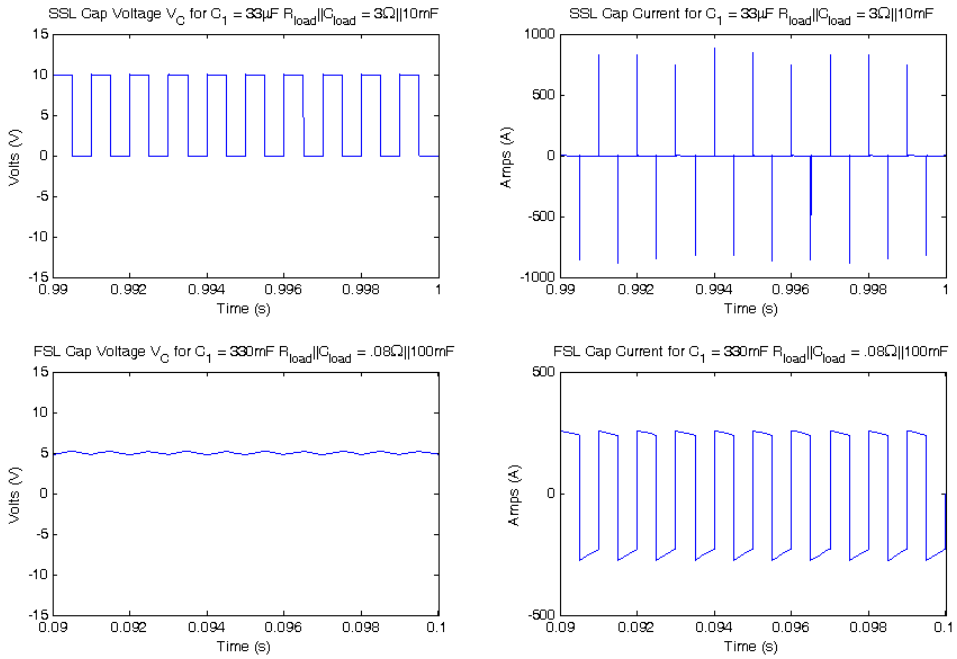


Figure D-2: In the SSL, capacitor voltages equilibrate each half-cycle and currents are impulsive. In the FSL, capacitor voltages are constant and capacitor currents are fixed during each half cycle in the big capacitance limit.

and the capacitor current, $CdV_c(t)/dt = \frac{V_{in}-V_C(0)}{R}e^{-t/RC}$. Plugging this into the integral above leads to

$$E_{tot} = -\frac{(V_{in}-V_C(0))^2}{2R}RC\left(e^{-2t/RC}\right)_0^t. \tag{D.3}$$

At this point, we see that the value of R to the left of the exponential is about to cancel. What is left only depends on R in the exponential term. In the slow-switching-limit, this exponential term is allowed to collapse to (-1) because the final time, t, is very long compared to the RC time-constants in the circuit. In that case, the energy lost becomes

$$E_{tot,SSL} = \frac{1}{2}(V_{in}-V_C(0))^2C \tag{D.4}$$

or

$$\boxed{E_{tot,SSL} = \frac{1}{2}C\Delta V_C^2}, \tag{D.5}$$

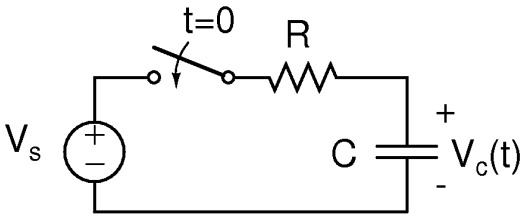


Figure D-3: The canonical circuit for studying the fundamental loss associated with charging a capacitor.

a result that is useful in calculating loss whenever a capacitor is allowed to charge to its resting value (until no current flows). The result in eqn. (D.5) is independent of the resistance, R, mathematically, because the exponential term containing it was allowed to collapse in the slow-switching-limit. If, however, the exponential is not allowed to collapse, the total energy lost becomes

$$E_{tot}(t) = \frac{1}{2}(V_{in} - V_C(0))^2 C(1 - e^{-2t/RC}), \tag{D.6}$$

which does depend on R and, in the fast-switching-limit, can be viewed near t=0 with the Taylor series approximation to the exponential term so that

$$E_{tot,FSL}(t) = \frac{1}{2}(V_{in} - V_C(0))^2 C(1 - (e^0 - \frac{2t}{RC}e^0 t)). \tag{D.7}$$

Finally, the total loss reduces to that which we would expect for two fixed voltages connected across the resistor:

$$\boxed{E_{tot,FSL}(t) = \frac{(V_{in} - V_C(0))^2 t}{R}}. \tag{D.8}$$

The result in eqn. (D.8) does depend on R because, mathematically, the exponential term was not allowed to collapse. When the exponential term was allowed to collapse, the total loss necessarily simplified to a quantity fundamentally independent of R. On the other hand, when the exponential term was *not* allowed to collapse, the total loss was fundamentally dependent on the value of R. While these results apply neatly to SSL and FSL, we will generally use this understanding to differentiate fundamental

loss mechanisms in the marx converter based on the instantaneous conditions imposed on the circuit by the input source and the load.

D.2.1 Generalization of SSL to Finite R-C Loads

As stated above, in the slow-switching limit, the switched-capacitor voltages equilibrate to the voltages connected across them each half cycle. However, when a switched-capacitor is connected to a non-ideal voltage source, such as a finite R-C load, during one of its phases, this statement needs to be generalized. In the SSL, the switched-capacitor voltages equilibrate during cycles when they are connected to the ideal input voltage source, and nearly equilibrate otherwise. Figure D-4 shows the SSL capacitor voltage for a 3-level marx converter with a large load capacitance and a smaller load capacitance. In these cases, SSL may be identified by the equilibration of the switched-capacitor voltage for the phase during which it is connected to the ideal input voltage source.

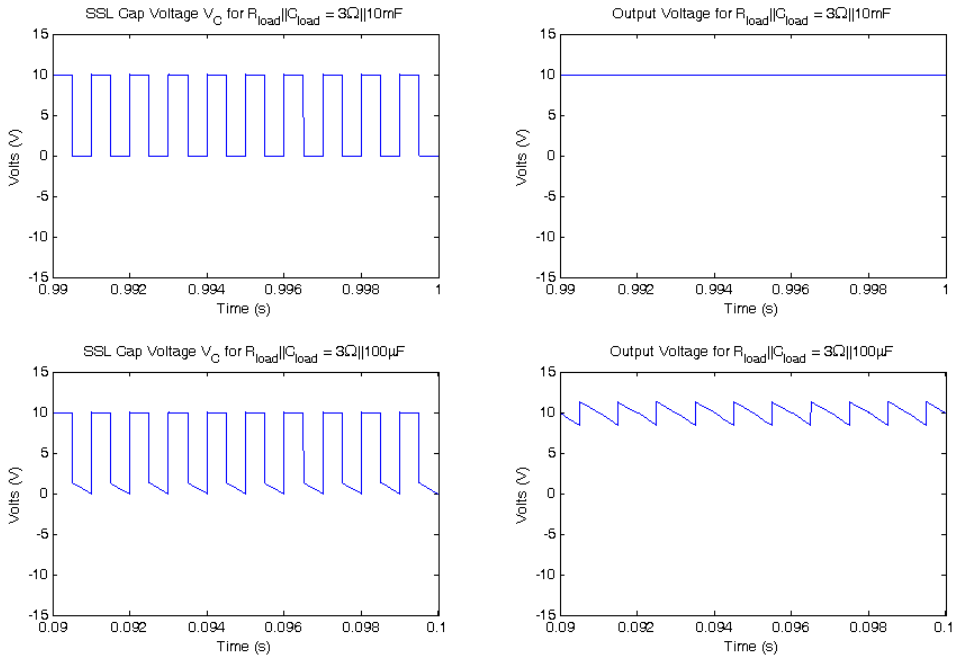


Figure D-4: In the SSL, the capacitors have time to fully equilibrate. With a finite R-C load, the output voltage ripple allows for a time-varying equilibration point during some phases.

D.3 Switching Pattern Classification of Marx Converters

This section describes a classification of marx converters switching patterns that differentiates the types of converters analyzed here. The switched-capacitor converters studied in Seeman et. al. [30], largely fall into one class described here. In [30], the author points out how the switching patterns may lead to constrained or under-constrained charge-balance problems:

> "[T]ypical of most step-down converters, the input source is connected to the circuit during only one phase (phase 2 in this case). As no charge flows from the input source during phase 1 (in this example), the phase-2 input-source charge flow is identified as q_{in}. Likewise, for most step-up converters, the output source is connected to the converter during only one phase. For the few converters where both sources are connected to the converter during both phases, it may be possible to determine a starting constraint by inspection. If such a constraint does not exist, one can fall back to the matrix-based methods [184] for determining the a_c vector." [30]

In the marx converter, it is possible to connect both sources to the circuit during both (or all if more than two) phases. It is also possible to connect the load directly to the input source or directly to ground. In this work, I consider "single-phase" patterns that drive the load during one phase, leaving it disconnected during the other phase, and also "multi-phase" patterns that drive the load during more than one phase. I also consider "non-isolated" switching patterns which include a phase that connects the load directly to the input source (or ground) and "isolated" patterns which only drive the load with switched-capacitors.

For this work, I organized the types of converters (switching patterns) analyzed into the chart shown in Table D.1. In Section D.8, I suggest how a more complete classification might be made. For now, the classification proposed here separates my analyses into demonstrative examples. For instance, the "Class-II" switching

patterns are similar to those analyzed by Seeman et. al. and the Class-III patterns are similar to multilevel output DC/DC converters. The Class-0, single-phase non-isolated pattern is not useful for boosting DC/DC converters because it requires that the load be connected directly to ground or the input during one phase and disconnected during the other. Therefore, I analyzed only Class-I,II, and III types from Table D.1.

Table D.1: Classification of Switching Patterns Analyzed

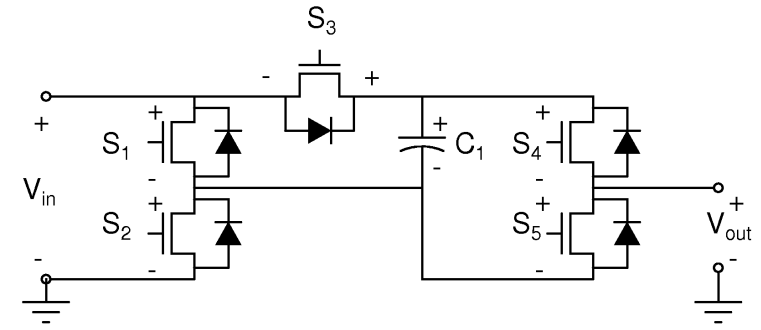
	non-isolated	isolated
single-phase	0	II
multi-phase	I	III

D.4 3-Level Marx Switch States

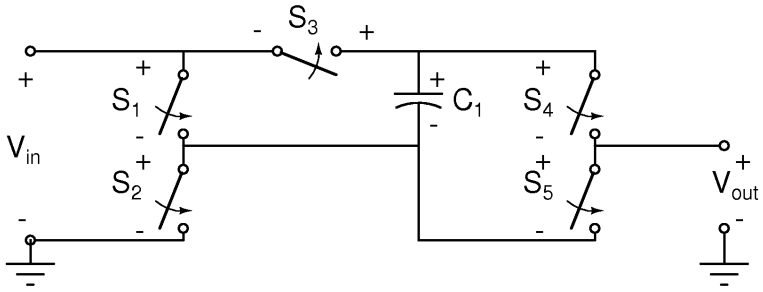
An example FET implementation of a three-level marx converter and the idealized switch implementation are shown in Figure D-5. The ideal implementation is the one analyzed in this work.

The three-level marx converter is capable of driving its output to 0,1, or 2 times its input voltage. For each case, there are generally redundant switching states that produce the same desired output voltage. Here, I considered only non-destructive switch states, i.e. ones that did not short the input source directly to ground. Non-destructive "Zero-states" (meaning states that drive the output to 0V) for the 3-level marx converter are depicted in Figures D-6. Non-destructive "one-states" and "two-states" are shown in Figures D-7 and D-8 respectively.

In this work, I am mostly concerned with one and two-states to produce a step-up in voltage from input to output. Within the one-states, states $1 - 1^{v\prime}$ drive the output directly from the input source. State $1^{v\prime\prime}$ drives the output with the switched-capacitor, C_1. Also, states $1'', 1'^{v}, 1^{v}$ and $1^{v\prime}$ discharge C_1, while state $1'$ recharges C_1 and states 1 and $1'''$ do not charge or discharge C_1.



(a) An FET implementation of a 3-level marx converter.



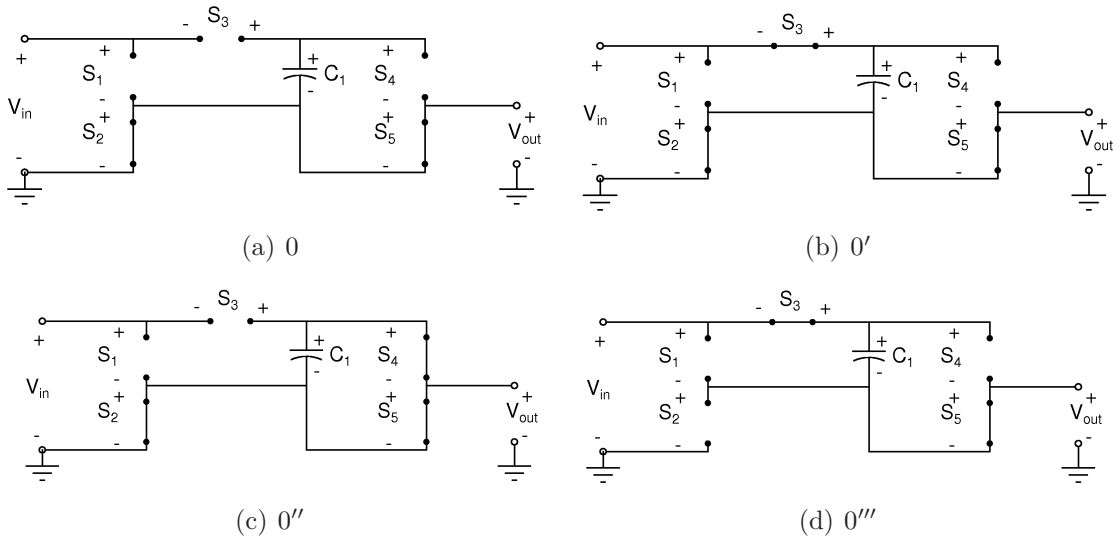
(b) Ideal switch representation of a 3-level marx converter.

Figure D-5: 3-level marx converter example FET implementation and the ideal switch implementation used for the analysis here.

There is only one two-state for the three-level marx and it is shown in Figure D-8. In the two-state, the output is driven by the series combination of the input source and the switched-capacitor.

One can already understand that the degree to which the switched-capacitor can hold up the output voltage during states $1^{v\prime\prime}$ and 2 is related to both loss and load regulation. A heavier load will draw more charge per unit time from the capacitor in these states leading to a drop in the capacitor voltage and a corresponding drop in the average output voltage of the converter. Furthermore, this same drop in the capacitor voltage leads to a loss proportional to $1/2(\Delta V_C)^2 f_{sw}$, so the same mechanism that accounted for output voltage droop or load regulation also accounts for loss.

Reducing the effective output resistance can be accomplished by increasing the capacitance value or by increasing the switching frequency. Either approach reduces the total change in voltage on the capacitor for a given load current. Increasing the switching frequency or the capacitor value enough causes the voltage on the capacitor



(a) 0 (b) 0′

(c) 0″ (d) 0‴

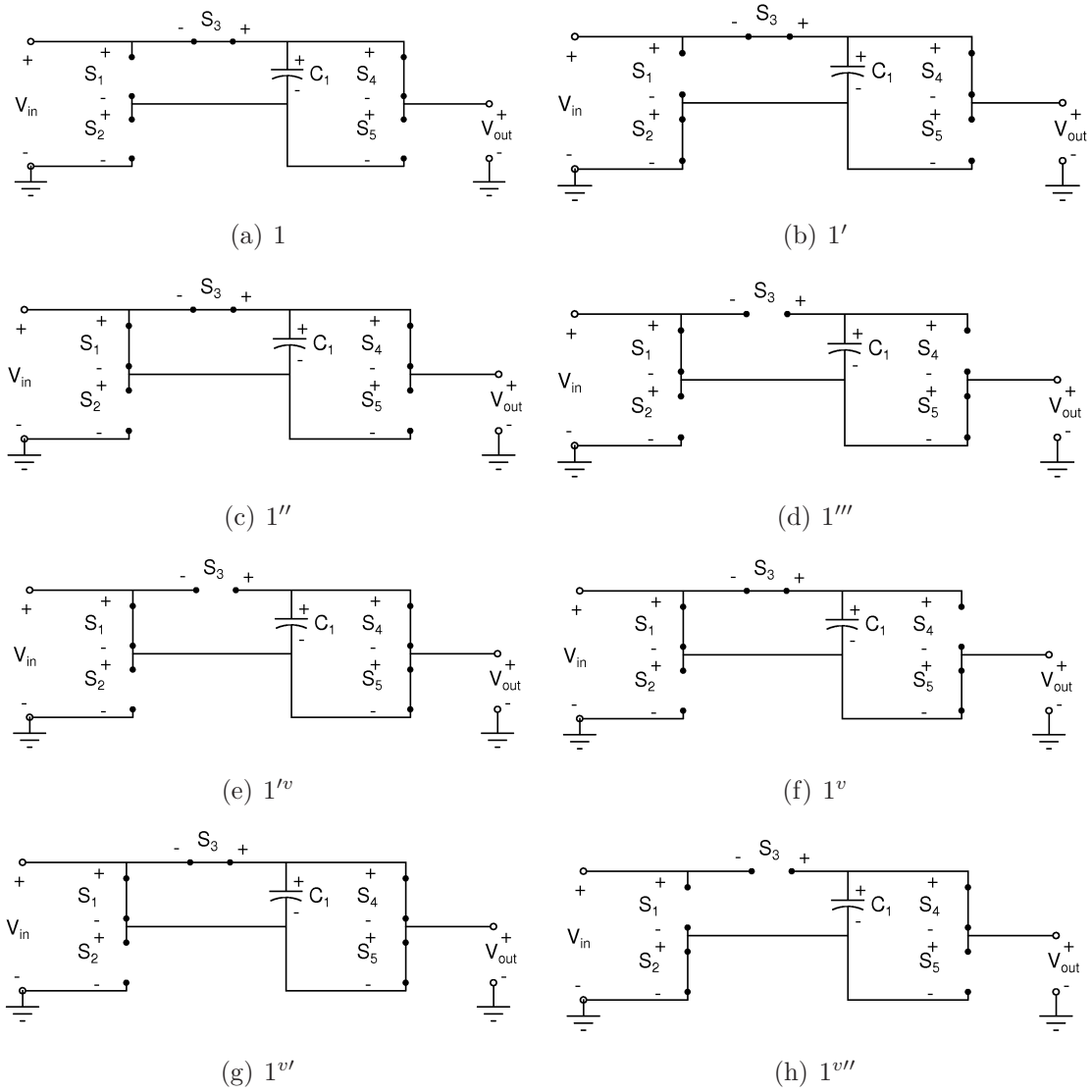
Figure D-6: 0-output switch states.

to remain fixed and yields the fast-switching-limit. In the FSL, the output resistance is lower-bound by the resistances of the interconnects in the circuit, which are usually dominated by the on-state resistances of the switches. Therefore, we expect to see effective resistances in the SSL like $1/C_1 f_{sw}$ and in the FSL like R_{on}.

D.5 Class-I Marx

The first type of switching pattern that I studied was the Class-I marx. This class is fundamentally different from the switched-capacitor circuits considered in [30]. Here, the input source is connected directly to the output during one phase (phase 1) while the switched-capacitor drives the output toward twice the input voltage during a second phase (phase 2). Because charge is transferred, during phase 1, directly between the input source and load, the periodic steady state charge balance constraint on the switched-capacitor is not sufficient to constrain the total charge to the output. This means that the charge-balance analysis used by Seeman does not apply well to this class of switching patterns. The need for an additional constraint will be evident in the analysis below.

In the case of the three-level class-I marx, phase 1 must be switching state 1′ drawn



(a) 1 (b) $1'$

(c) $1''$ (d) $1'''$

(e) $1'^{v}$ (f) 1^{v}

(g) $1^{v\prime}$ (h) $1^{v\prime\prime}$

Figure D-7: 1-states.

in Figure D-7 because phase 2 must be switching state 2 and the switched-capacitor must be recharged during each cycle. The two states are shown simplified in Figure D-9.

This converter can be solved for output voltage, V_{out}, in the slow switching limit as follows. We first assume that the output voltage is fixed at some steady-state value, V_{out}, because it contains a sufficiently large capacitance C_{out}. We also assume that the switched-capacitor equilibrates quickly during each half cycle as defined by the

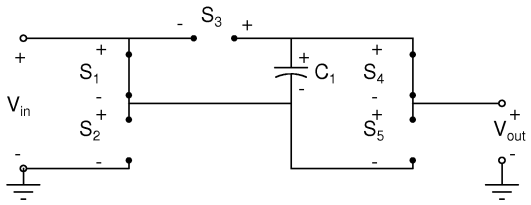
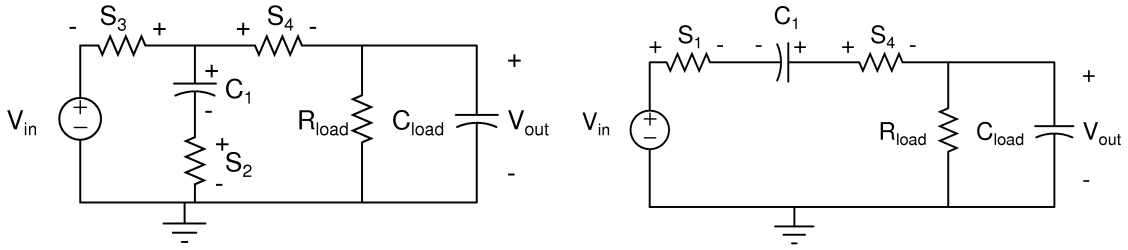


Figure D-8: The only 2-state (2).



(a) Phase 1 (b) Phase 2

Figure D-9: The two simplified switching states of the class-1 converter.

SSL. Since we are looking for the average output voltage, we can write

$$< V_{out} >=< I_{out} > R_{load} \tag{D.9}$$

where $< I_{out} >$ is the average current into the load:

$$< I_{out} >= f_{sw}(\Delta q_{out}^{(1)} + \Delta q_{out}^{(2)}) = f_{sw}(\Delta q_{out}) \tag{D.10}$$

and the superscripts denote phases. Now, the charge delivered to the load in phase 1 is

$$\Delta q_{out}^{(1)} = -\Delta q_{in}^{(1)} - \Delta q_{C}^{(1)}, \tag{D.11}$$

where Δq_c is the charge delivered to C_1. From Figure D-9, the charge delivered to the load in phase 2 all comes from the capacitor. In periodic steady state, the charge off the capacitor in phase 2 must equal the charge onto it in phase 1, so $\Delta q_{out}^{(2)} = -\Delta q_c^{(2)} = +\Delta q_c^{(1)}$. This is the charge-balance constraint. Therefore, the total output charge over one full cycle is

$$\Delta q_{out} = \Delta q_{out}^{(1)} + \Delta q_{out}^{(2)} = -\Delta q_{in}^{(1)}. \tag{D.12}$$

To find $\Delta q_{in}^{(1)}$, in this case, we can integrate the input current during phase 1 as follows.

$$-\Delta q_{in}^{(1)} = \int_0^{t_1} \left(\frac{V_{in} - V_c^{(1)}(\tau)}{R_{sw3}} \right) d\tau, \tag{D.13}$$

where t_1 is the time spent in phase 1. The capacitor voltage during phase 1 can be shown to be

$$V_c^{(1)}(t) = \left(V_c(0) - \frac{V_{in} + V_{out}}{2} \right) e^{-t/\tau_1} + \frac{V_{in} + V_{out}}{2}, \tag{D.14}$$

where we have assumed, in calculating the capacitor voltage, that $R_{sw3} = R_{sw4} = R_{on}$ and also $\tau_1 = R_{on}C_1/2$. Carrying out the integral in eqn. (D.13) leads to

$$-\Delta q_{in}^{(1)} = \frac{1}{R_{on}} \left(\frac{1}{2} t_1 (V_{in} - V_{out}) + (\frac{1}{2} V_{out} - \frac{3}{2} V_{in}) \tau_1 (e^{-t1/\tau 1} - 1) \right), \tag{D.15}$$

which, in the SSL reduces to

$$-\Delta q_{in}^{(1)} = \frac{1}{2R_{on}} (V_{in} - V_{out}) t_1 = \Delta q_{out}, \tag{D.16}$$

meaning that the short charge time of the switched-capacitor could have been ignored and only the current transferred directly from the input to the load considered. The expression in (D.16) can be identified as the necessary additional constraint that charge-balance analysis alone would not have provided in the class-1 converter. It captures the energy lost when the input source is connected directly to the load and depends on R_{on} and t_1, fundamentally different from the losses associated with SSL charging and discharging of the switched-capacitor.

Now, the average output current becomes

$$< I_{out} >= \frac{f_{sw}}{2R_{on}} t_1 (V_{in} - V_{out}). \tag{D.17}$$

Combining this with eqn. (D.9) and assuming a 50% duty ratio, so that $t_1 = T_{sw}/2$ the output voltage becomes

$$\boxed{V_{out} = V_{in} \left(\frac{R_{load}}{4R_{on} + R_{load}} \right)}. \tag{D.18}$$

The result in eqn. (D.18) is just an expression of the fact that the switched-capacitor really does nothing in the slow-switching limit. Connecting the input source to load "D" of the time leads to $(1/D)$ times the series resistance between the input source and the output during phase 1. Therefore, we can see that this switching pattern will not allow a step-up in voltage for a DC output voltage in the SSL. Varying the duty ratio will vary the coefficient that appears in front of the R_{on} term in the denominator of eqn. (D.18), changing the effective output resistance of the converter but still not allowing a step-up in voltage.

A plot of the result from eqn. (D.18) is shown compared to simulated data for a three-level class-I marx converter. Note that as the load capacitance is increased in simulation the load regulation curve approaches that of the model which assumes a fixed DC output voltage corresponding to $C_{out} = \infty$.

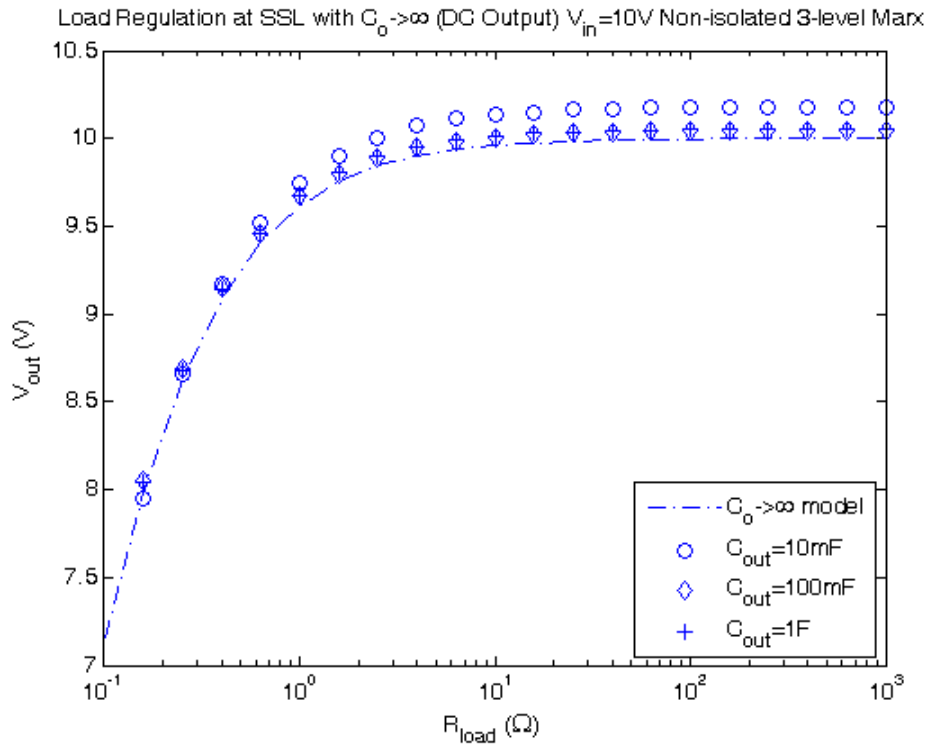
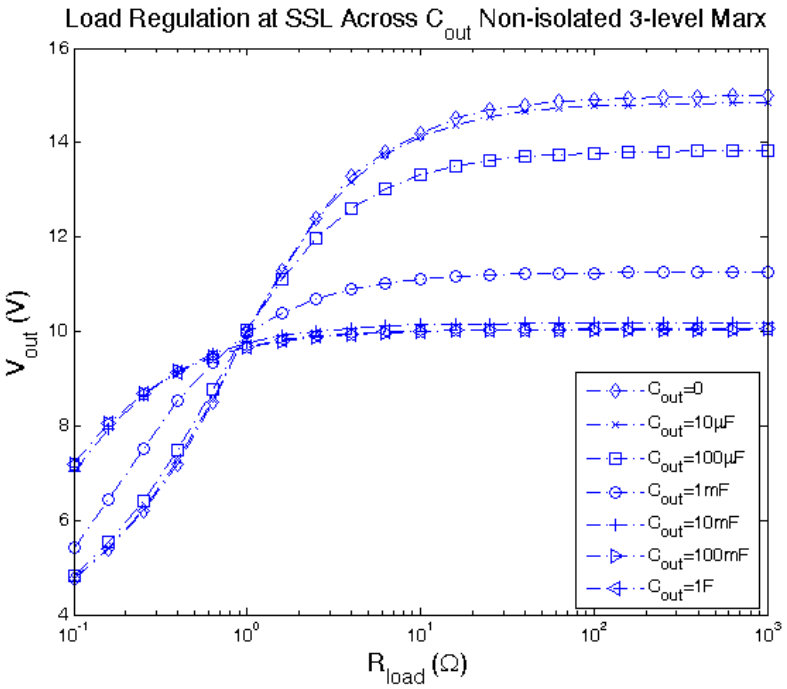


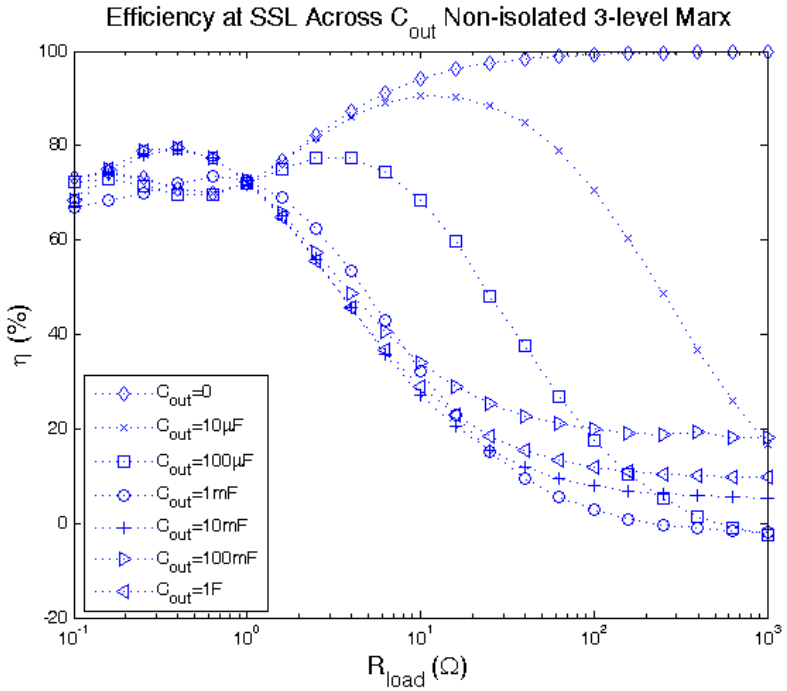
Figure D-10: Load regulation in the SSL class-I three-level marx for D=0.5.

Because the SSL class-I marx behaves like a resistor, it is not useful as a boosting DC/DC converter. However, it is interesting to point out at this point how the behavior of this converter changes as the load capacitance varies. That is to say, the

converter's "load regulation" and efficiency depend on how fixed the output voltage is. Plots of simulated data for load regulation and efficiency across values of the load capacitance are shown in Figures D-11(a) and D-11(b) respectively. As the load capacitance decreases, the converter starts to behave like a DC/AC converter or a DC/DC converter with increasing output voltage ripple. It should be clear from the plots of Figure D-11 that if the load were not treated correctly, i.e. in the big load capacitance limit, the wrong behavior could be inferred.



(a) Simulated load-regulation across load capacitance.



(b) Simulated efficiency across load capacitance.

Figure D-11: SSL Class-I simulated load regulation and η: the fundamental behavior of the marx converter changes between DC/DC mode (big C_{load}) and DC/AC mode (small C_{load}).

Although the class-I converter in SSL was not useful as a boosting DC/DC converter, we can also consider the fast-switching-limit. In the FSL, the capacitor voltage is fixed. Again, referring to Figure D-9, the output voltage can be solved for as follows.

Starting from the constraint that

$$V_{out} = I_{out} R_{load}, \tag{D.19}$$

where average quantities V_{out} and I_{out} are now assume without the carats. The time-averaged output current is

$$I_{out} = (1-D) I_{out}^{(1)} + D I_{out}^{(2)}. \tag{D.20}$$

Solving the two states for their output currents yields

$$I_{out}^{(1)} = \frac{V_c - V_{out}(1+\frac{R_{sw2}}{R_{sw3}}) + \frac{R_{sw2}}{R_{sw3}} V_{in}}{R_{sw4} + \frac{R_{sw2}}{R_{sw3}}(R_{sw3}+R_{sw4})} \tag{D.21}$$

$$I_{out}^{(2)} = \frac{V_{in} + V_c - V_{out}}{R_{sw1} + R_{sw4}} \tag{D.22}$$

where R_{swi} is the on-resistance of the i^{th} switch (all assumed to be R_{on} previously). The second constraint is that the average capacitor current is zero (charge balance) and can be written:

$$(1-D) I_c^{(1)} + D I_c^{(2)} = 0. \tag{D.23}$$

Solving the capacitor current in the two states yields

$$I_c^{(1)} = \frac{1}{R_{sw3}} \frac{V_{out}(1 - \frac{R_{sw3}+R_{sw4}}{R_{sw4}}) + V_c \frac{R_{sw3}+R_{sw4}}{R_{sw4}} - V_{in}}{1 + \frac{R_{sw2}}{R_{sw4}}(R_{sw3}+R_{sw4})\frac{1}{R_{sw3}}} \tag{D.24}$$

$$I_c^{(2)} = \frac{V_{in} + V_c - V_{out}}{R_{sw1} + R_{sw4}} \tag{D.25}$$

Combining these two independent equations yields the capacitor voltage, V_c and the output voltage, V_{out}, in terms of $D's$ and $R'_{sw}s$ in closed form. After simplification

and assuming that all switches have on-resistance R_{on}, the output voltage becomes

$$\boxed{V_{out} = \frac{V_{in}D'R_{load}(2D' + 3D)}{2(D')^2R_{load} + 2D'R_{load}D + 4D'R_{on} + 3DR_{on}}} \tag{D.26}$$

and the capacitor voltage becomes

$$V_c = \frac{-(-2D'R_{on} - D'R_{load}D - 2(D')^2R_{load} + 3DR_{on})V_{in}}{2(D')^2R_{load} + 2D'R_{load}D + 4D'R_{on} + 3DR_{on}} \tag{D.27}$$

The loss can be derived by adding up the losses in the switches as follows. The losses in the two phases are

$$P_{loss}^{(1)} = (I_c^{(1)})^2R_{sw2} + (I_{out}^{(1)})^2R_{sw4} + (I_c^{(1)} - I_{out}^{(1)})^2R_{sw3} \tag{D.28}$$

$$P_{loss}^{(2)} = \frac{(V_{in} + V_c - V_{out})^2}{R_{sw1} + R_{sw4}}, \tag{D.29}$$

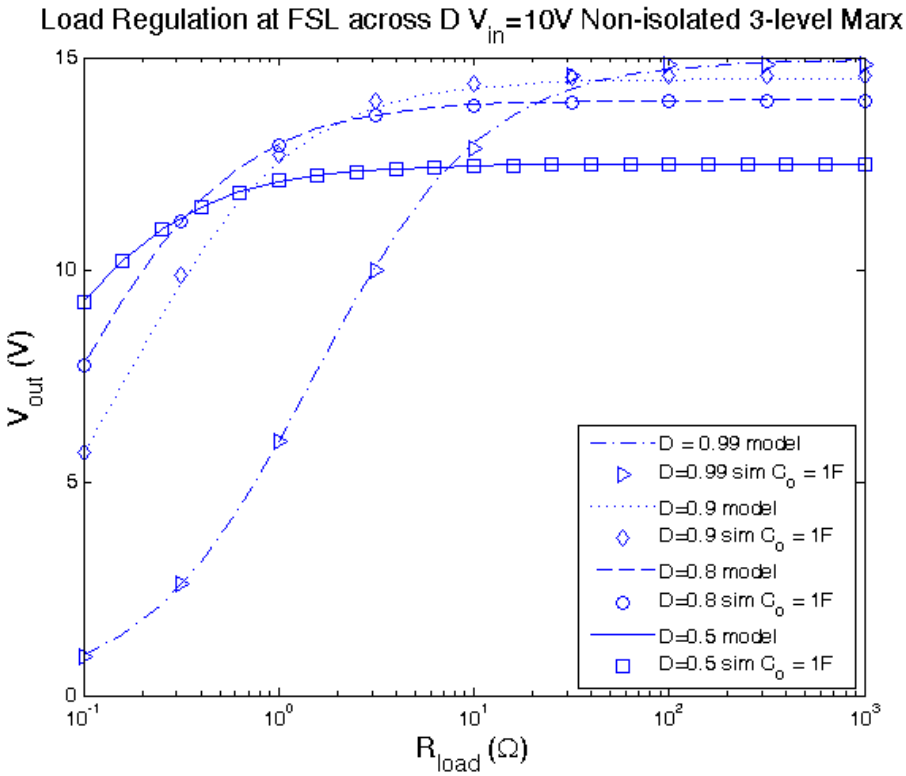
where $I_c^{(1)}$ and $I_{out}^{(1)}$ were solved for above. The time-averaged loss is

$$P_{loss,tot} = D'P_{loss}^{(1)} + DP_{loss}^{(2)}. \tag{D.30}$$

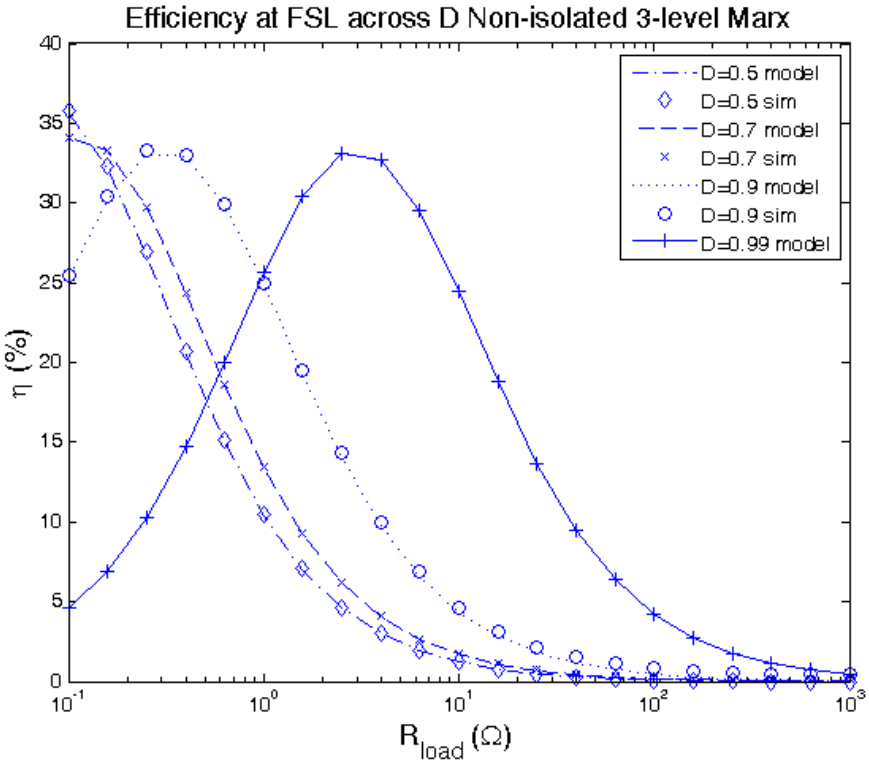
Combining eqns. (D.29) with eqns. (D.25), (D.22), (D.26)and (D.27) yields the power loss in closed form. Finally, efficiency can be calculated as

$$\eta = (1 + \frac{P_{loss}}{V_{out}^2/R_{load}})^{-1}. \tag{D.31}$$

Model validation plots of load regulation and efficiency for the FSL class-1 marx are shown in Figure D-12.



(a) Load-regulation



(b) Efficiency

Figure D-12: Model and simulation of load regulation and efficiency plots at FSL for the Class-I marx converter.

These results show that the FSL class-I marx may produce a step-up in voltage. However, efficiencies are generally poor and are at a maximum for a narrow load range. The control approach here would perhaps be to adjust the duty ratio in order to optimize efficiency as the load varies.

D.6 Class-II Marx

The framework developed by Seemen et. al. can be directly applied to the class-II marx switching patterns. These consist of one phase in which the switched-capacitors are connected to the input source and one phase when they are connected to the output. In neither phase, is there a direct connection between the input and output source so all of the loss and load regulation is the result of capacitor charging and discharging. Therefore, charge-balance analysis can fully constrain the analysis of these switching patterns. Starting with the three-level marx, we can build the loss model shown in Figure D-1 for both switching speed limits.

Here, we choose the switching state shown in Figure D-13 as the phase 1 state to recharge the capacitor while the load is disconnected. The other state is chosen

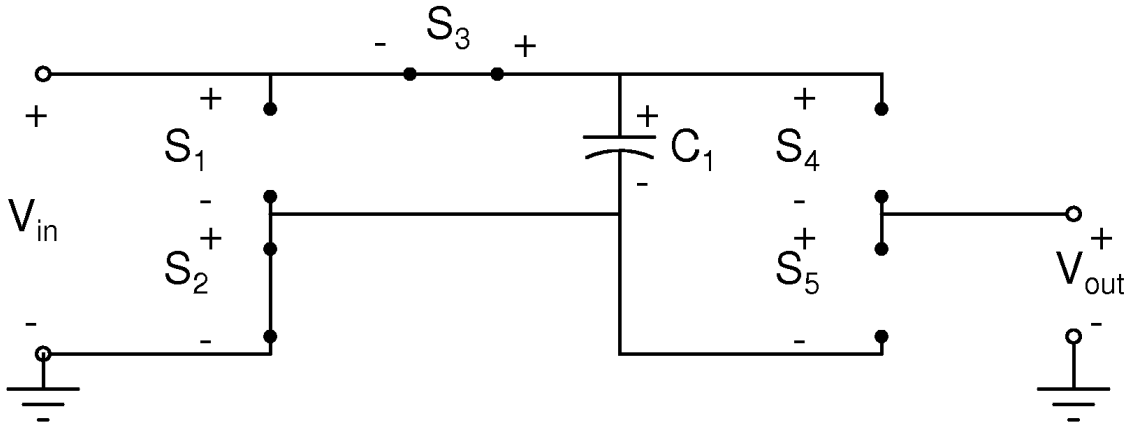
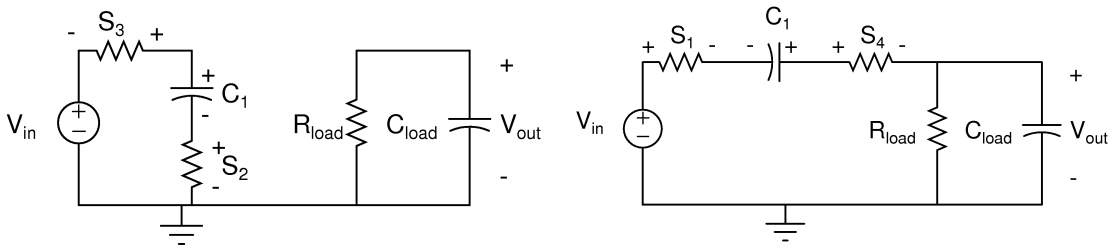


Figure D-13: The recharging state.

to achieve a step-up in voltage using state 2. The two states are shown simplified in Figure D-14. The charge-balance analysis here is well-constrained enough that the open-circuit voltage transfer and the output resistance can be found simultaneously.



(a) Phase 1 (b) Phase 2

Figure D-14: The two simplified switching states of the class-1 converter.

In the SSL, the charge-balance analysis goes as follows.

Phase 1	Phase 2
$\Delta q_c^{(1)} = q_A$	$\Delta q_c^{(2)} = -q_{out}$
$\Delta q_{in}^{(1)} = -q_A$	$\Delta q_{in}^{(2)} = -q_{out}$
$\Delta q_{out}^{(1)} = 0$	$\Delta q_{out}^{(2)} = q_{out}$

From the charge balance constraint imposed on the capacitor in periodic steady state, $q_A = -q_{out}$. The charge multiplier vectors are

$$a_c^{(1)} = [\Delta q_{out}^{(1)}/q_{out}, \Delta q_c^{(1)}/q_{out}, \Delta q_{in}^{(1)}/q_{out}] \quad (D.32)$$

$$a_c^{(2)} = [\Delta q_{out}^{(2)}/q_{out}, \Delta q_c^{(2)}/q_{out}, \Delta q_{in}^{(2)}/q_{out}], \quad (D.33)$$

where q_{out} is the total charge into the load. These vectors become

$$a_c^{(1)} = [0, 1, -1] \quad (D.34)$$

$$a_c^{(2)} = [1, -1, -1], \quad (D.35)$$

and the sum of the two, a_c, is

$$a_c = [1, 0, -2] \quad (D.36)$$

which says that $q_{in}/q_{out} = -2$ so that the open-circuit voltage transfer ratio is

$$\boxed{M = -\frac{q_{in}}{q_{out}} = 2} \quad (D.37)$$

because the open-circuit voltage indicates the no-loss case. (The vector a_c should also

have zero values for all entries other than the ends). From Seeman et. al. [30], the slow-switching-limit output resistance is

$$R_{SSL} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \tag{D.38}$$

which can be evaluated for either charge multiplier vector and becomes

$$\boxed{R_{SSL} = \frac{1}{f_{sw} C_1}} \tag{D.39}$$

for this three-level marx. The FSL output resistance can be taken from the switch multiplier vector, which keeps track of the charge through each interconnect in order to maintain the same charge-balance constraint above. Using the reference polarities on the switches, the switch multiplier vector consists of the charge through each interconnect, when it is on, normalized by the total output charge, q_{out}.

$$a_r = [a_{r1}^{(2)}, a_{r2}^{(1)}, a_{r3}^{(1)}, a_{r4}^{(2)}, a_{r5}^{(1)}] = [-1, 1, 1, 1, 0]. \tag{D.40}$$

From Seeman et. al., the FSL output resistance can be found as

$$R_{FSL} = \sum_i \frac{R_i (a_{r,i})^2}{D_i} \tag{D.41}$$

where R_i is the i^{th} switch on-resistance, and D_i is the duty ratio corresponding to the phases during which the respective switches are on. Defining DT_{sw} as the time spent in phase 2, the FSL output resistance becomes

$$R_{FSL} = \frac{R_{sw1}}{D} + \frac{R_{sw2}}{1-D} + \frac{R_{sw3}}{1-D} + \frac{R_{sw4}}{D}. \tag{D.42}$$

If we assume that all switch resistances are R_{on}, this results simplifies to

$$\boxed{R_{FSL} = \frac{2R_{on}}{D(1-D)}}, \tag{D.43}$$

while the open-circuit voltage above applies here as well. Finally, efficiency can be taken directly from the model proposed by Seeman in Figure D-1 as

$$\eta = 1 - \frac{R_{eq}}{R_{eq} + R_{load}}. \tag{D.44}$$

These results were compared to simulated data. First, the simulated output resistance, calculated as $P_{loss,meas}/I^2_{out,meas}$ was plotted against the SSL and FSL output resistance asymptotes in Figure D-15, showing good agreement.

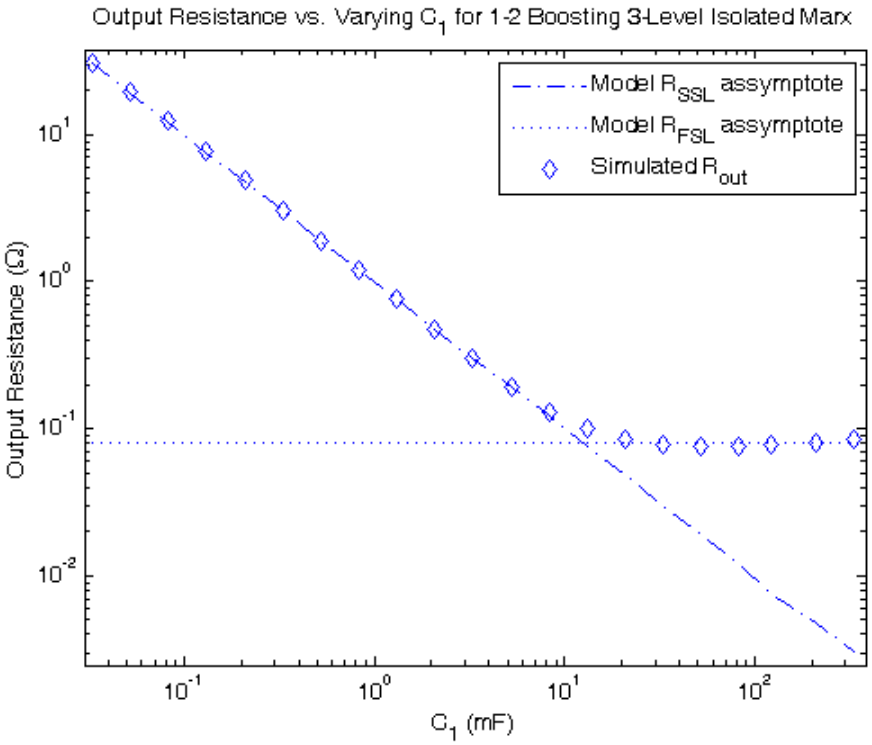
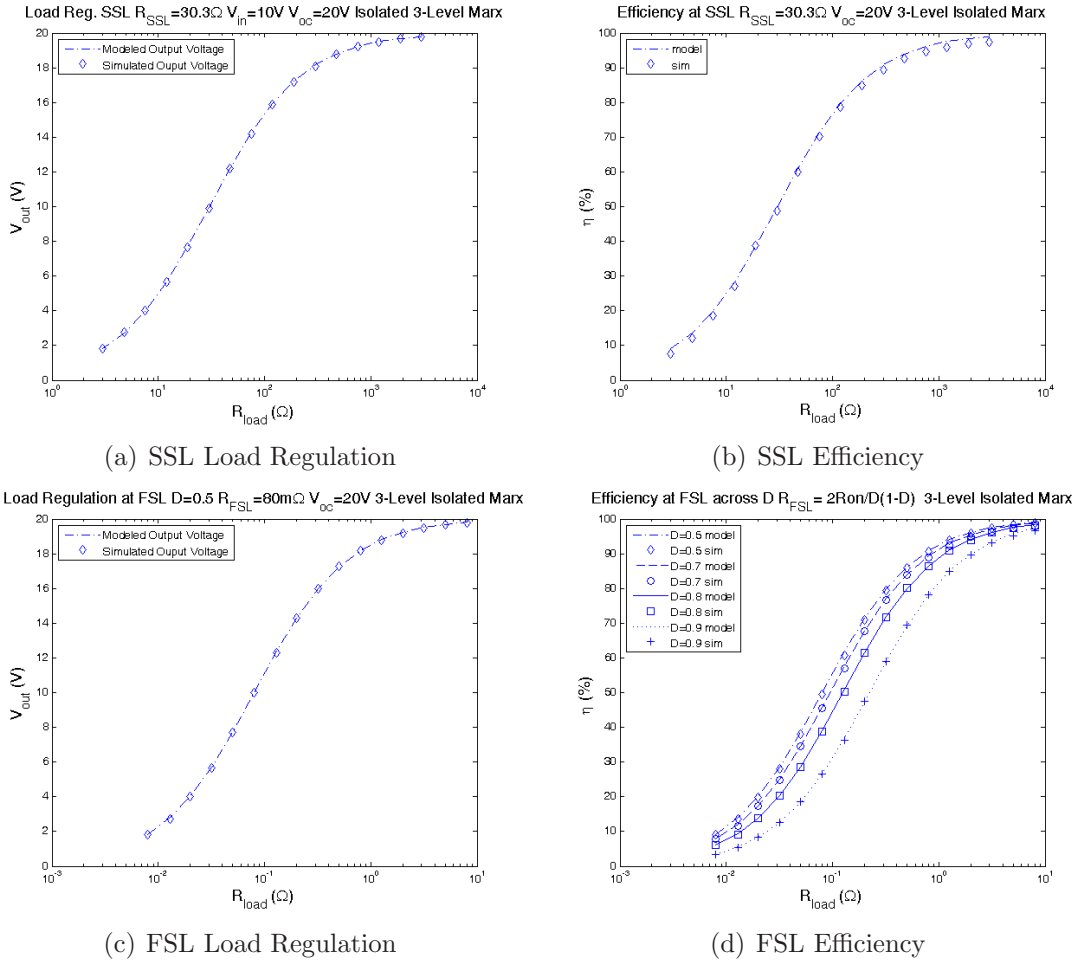


Figure D-15: Simulated and modeled output resistance across switching speed limits.

Model validation plots of load regulation and efficiency for both switching speed limits are shown in Figure D-16. These plots show that as the load becomes heavier, the converter's efficiency decreases. That is, the class-II converter is very efficient when the load voltage is close to the open-circuit voltage of the converter. One can think of this behavior as that of a linear regulator. Therefore, we could regulate the output voltage by varying the output resistance using the switching frequency of the class-II converter.



(a) SSL Load Regulation

(b) SSL Efficiency

(c) FSL Load Regulation

(d) FSL Efficiency

Figure D-16: Model and simulation of load regulation and efficiency plots at SSL and FSL.

The FSL model also shows that efficiency gets worse as we depart from a 50% duty ratio. In the FSL, the optimal duty ratio for efficiency can be calculated as follows.

$$\frac{dR_{FSL}}{dD} = R_{on}\left(\frac{-D^{-2}}{(1-D)} + \frac{1}{D(1-D)^2}\right) \tag{D.45}$$

and setting this derivative equal to zero leads to the expression

$$D_{opt} = 1 - D_{opt} \tag{D.46}$$

which is only satisfied for

$$\boxed{D_{opt} = 0.5} \tag{D.47}$$

as confirmed by the plot in Figure D-17.

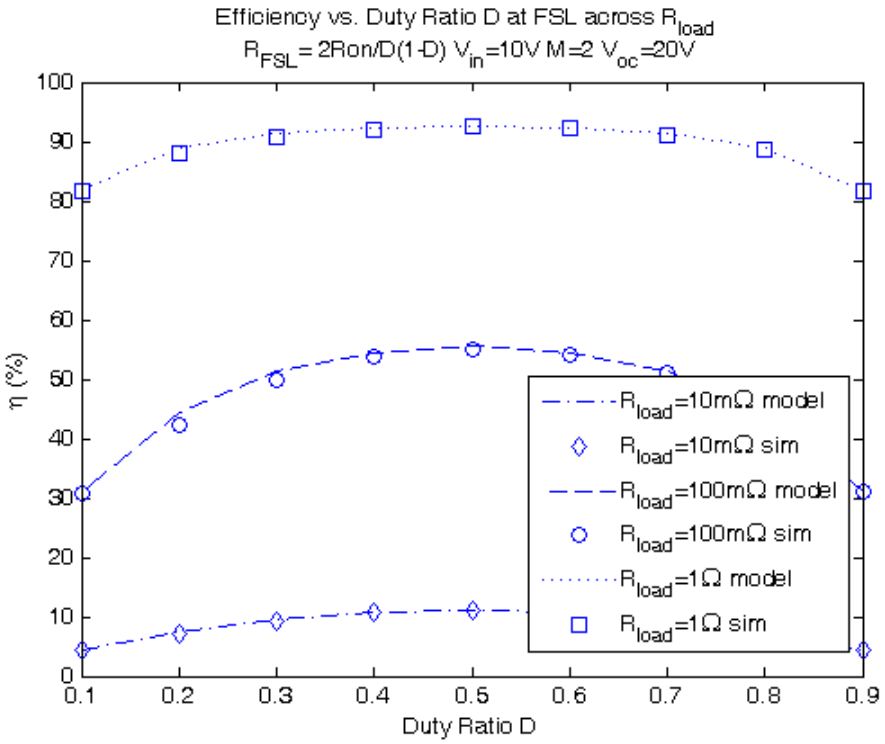


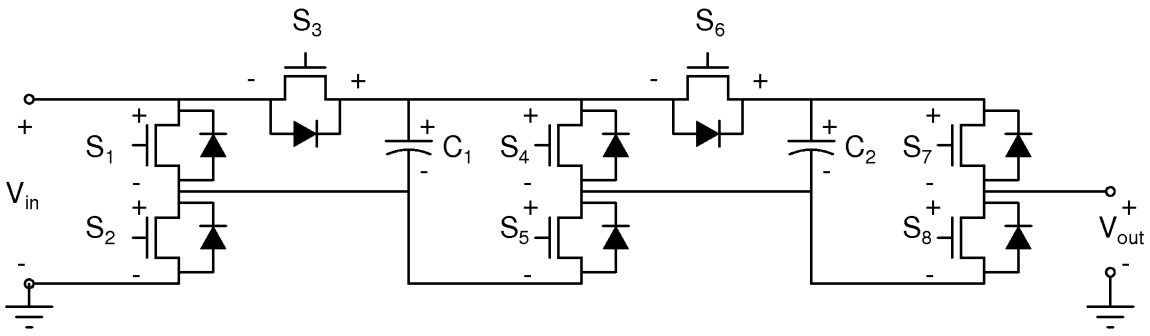
Figure D-17: Simulated and modeled efficiency, η, vs. R_{load} across duty ratio, D.

D.6.1 Extension to 4-Level Example

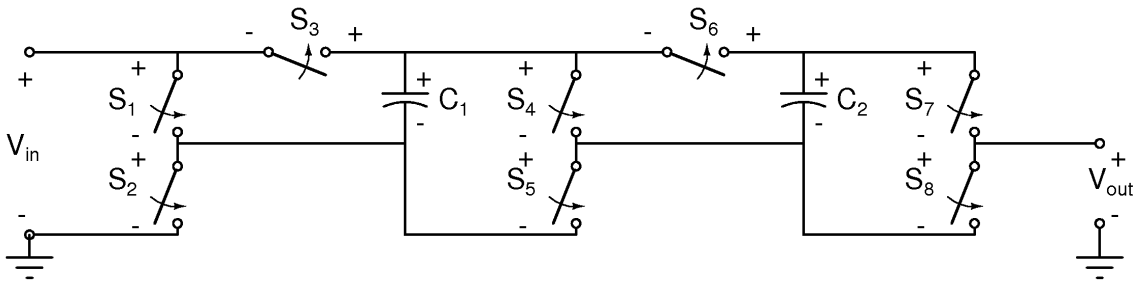
The charge balance analysis above can be easily extended to more than three levels. A four-level marx converter is depicted in Figure D-18. First, we consider briefly the converter's behavior when boosting to two times the input voltage.

The switching states that allow boosting to twice the input voltage are shown in Figure D-19. There are three redundant 2-states and one useful recharge state that recharges both switched-capacitors, C_1 and C_2, which we will call the $\star$-state.

This example highlights a subtlety in the calculation of R_{FSL}. In Seeman [30], only switches that are on during one phase and off during the other are ever considered. This is because if a switch is on in both phases, the converter could presumably be implemented without it. However, when using a marx converter in the way that I am proposing, we may want to keep those switches around to, for instance, "reconfigure"



(a) An FET implementation of a 4-level marx converter.



(b) Ideal switch representation of a 4-level marx converter.

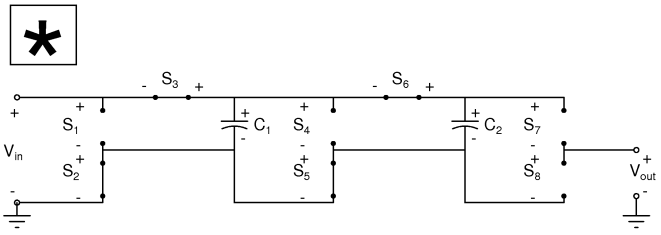
Figure D-18: 4-level marx converter example FET implementation and the ideal switch implementation used for the analysis here.

the converter between the 1-2 boosting mode here and the 1-3 boosting mode that I analyze later. For now, I analyze the FSL case assuming that "always-on" switches are ideal because they could be eliminated. However, to analyze the so-called reconfigurable converter that includes those switches' on-resistances, I will show how the effect of their losses can be added back into the final result.

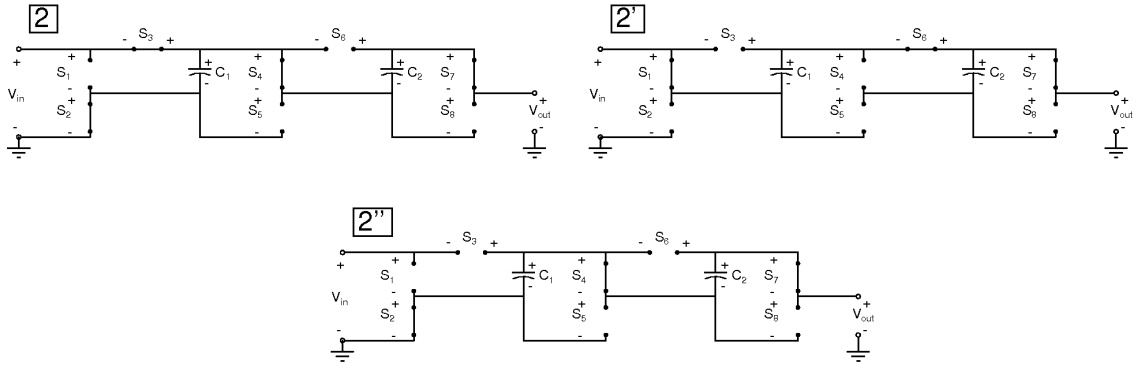
Charge balance analysis for the three possible switching patterns in the SSL yields the following results. For each converter the open-circuit voltage gain in both the SSL and FSL is always

$$\boxed{M = 2}. \tag{D.48}$$

The output resistances are,



(a) Phase 1



(b) Phase 2 choices

Figure D-19: The simplified switching states of the four-level class-2 converter for boosting to twice the input voltage.

Pattern	R_{SSL}	R_{FSL}
$\star - 2$	$\frac{1}{C_2 f_{sw}}$	$\frac{2R_{on}}{D(1-D)}$
$\star - 2'$	$\frac{1}{C_1 f_{sw}}$	$\frac{2R_{on}}{D(1-D)}$
$\star - 2''$	$\frac{C_1+C_2}{C_1 C_2 f_{sw}}$	$\frac{8(D-2)}{D(1-D)}$

where we have assumed that all switches have on-state resistance R_{on} and D corresponds to the time spent in phase 2. From this analysis, either of the first two switching patterns wins over the third in both switching speed limits based on output resistance.

In order to add back in the effect of the always-on switches in a reconfigurable marx converter the R_{FSL} results would be modified as follows. Now, the switch multiplier vector a_r cannot generally be written as a the superposition of the two switch multiplier vectors. Instead, we would keep track of the switch multiplier vectors for each phase $a_r^{(1)}$ and $a_r^{(2)}$ since the always-on switches will have non-zero entries in

both. The current in each switch during each phase is

$$i_{r,i}^{(j)} = \frac{q_{r,i}^{(j)} f_{sw}}{D_i^{(j)}} \tag{D.49}$$

so that we can write the currents in terms of the switch multiplier vector entries in each phase:

$$i_{r,i}^{(j)} = \frac{a_{r,i}^{(j)} q_{out} f_{sw}}{D_i^{(j)}} = \frac{a_{r,i}^{(j)} i_{out}}{D_i^{(j)}}. \tag{D.50}$$

Now, the time-averaged power loss in general is the sum of each $i^2 R_{on}$ loss for all switches:

$$P_{loss} = \frac{1}{T_{sw}} \left(D_i^{(j)} T_{sw} R_i \left(\frac{a_{r,i}^{(j)} i_{out}}{D_i^{(j)}} \right)^2 \right) \tag{D.51}$$

over all i switches and over all j phases. Then, the loss in the always-on switches is

$$P_{loss,alwayson} = \sum_{i,j} R_i \frac{(a_{r,i}^{(j)})^2 i_{out}^2}{D_i^{(j)}} \tag{D.52}$$

and the total loss is the sum of the losses in the always-on switches and the normal switches:

$$P_{loss,tot} = P_{loss,alwayson} + P_{normal}. \tag{D.53}$$

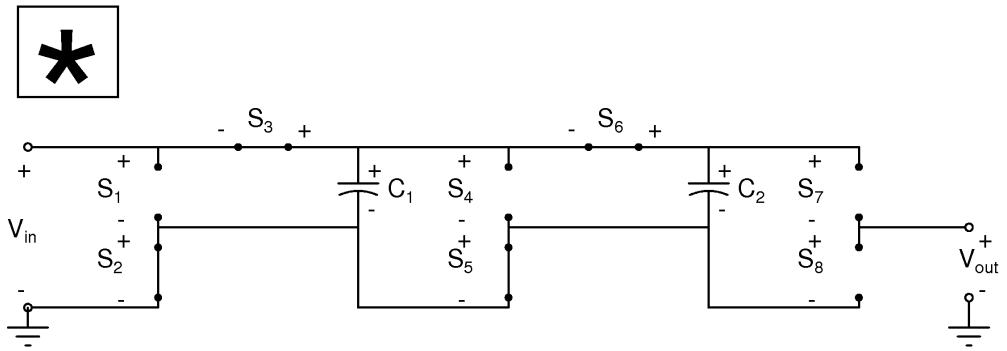
Because all charge is still transferred through capacitor charging and discharging, we can assume a loss model like the one shown in Figure D-1 so that the equivalent output resistance is just $R_{FSL} = P_{loss,tot}/i_{out}^2$. Now, the new output resistance becomes

$$R_{FSL,new} = \sum_{i-alwayson,j} R_i \frac{(a_{r,i}^{(j)})^2}{D_i^{(j)}} + \sum_{i-normal} R_i \frac{(a_{r,i})^2}{D_i} \tag{D.54}$$

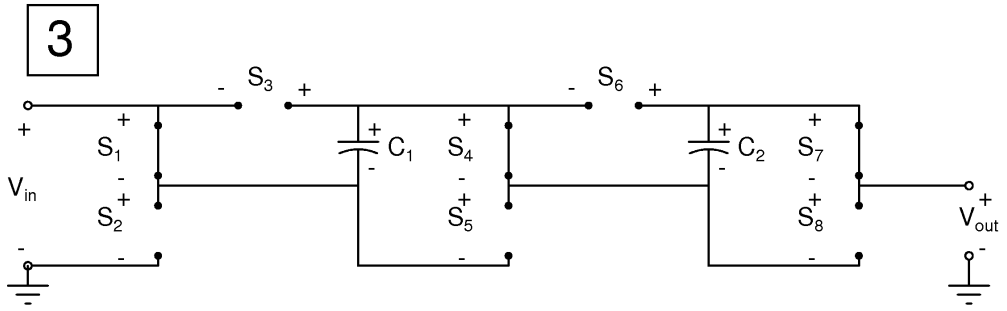
where the first term is new and the second term is the old expression for R_{FSL}.

Finally, we can study the four-level marx boosting to three times the input voltage. The switching states for this case are shown in Figure D-20.

The charge balance analysis goes as follows.



(a) Phase 1



(b) Phase 2

Figure D-20: The simplified switching states of the four-level class-2 converter for boosting to three times the input voltage.

Phase 1	Phase 2
$\Delta q_{in}^{(1)} = -q_A$	$\Delta q_{c}^{(2)} = -q_{out}$
$\Delta q_{c1}^{(1)} = q_A - q_B$	$\Delta q_{in}^{(2)} = -q_{out}$
$\Delta q_{c2}^{(1)} = q_B$	$\Delta q_{in}^{(2)} = -q_{out}$
$\Delta q_{out}^{(1)} = 0$	$\Delta q_{out}^{(2)} = q_{out}$

and the periodic state charge balance conditions on the switched-capacitors yields

$$q_A - q_B = q_{out} \tag{D.55}$$

$$q_B = q_{out} \tag{D.56}$$

so that the charge multiplier vectors become

$$a_c^{(1)} = [0, 1, 1, -2] \tag{D.57}$$

$$a_c^{(2)} = [1, -1, -1, -1] \tag{D.58}$$

$$a_c = [1, 0, 0, -3] \tag{D.59}$$

implying the open circuit voltage transfer ratio of

$$\boxed{M = 3} \tag{D.60}$$

and the SSL output resistance

$$\boxed{R_{SSL} = \frac{1}{C_1 f_{sw}} + \frac{1}{C_2 f_{sw}}}. \tag{D.61}$$

Inspecting the circuits in Figure D-20 with the charge multiplier vectors above yields the switch multiplier vector

$$a_r = [1, -2, -2, 1, 1, -1, 1, 0] \tag{D.62}$$

and noting that the duty ratio D corresponds to the time spent in state-3, the FSL output resistance becomes

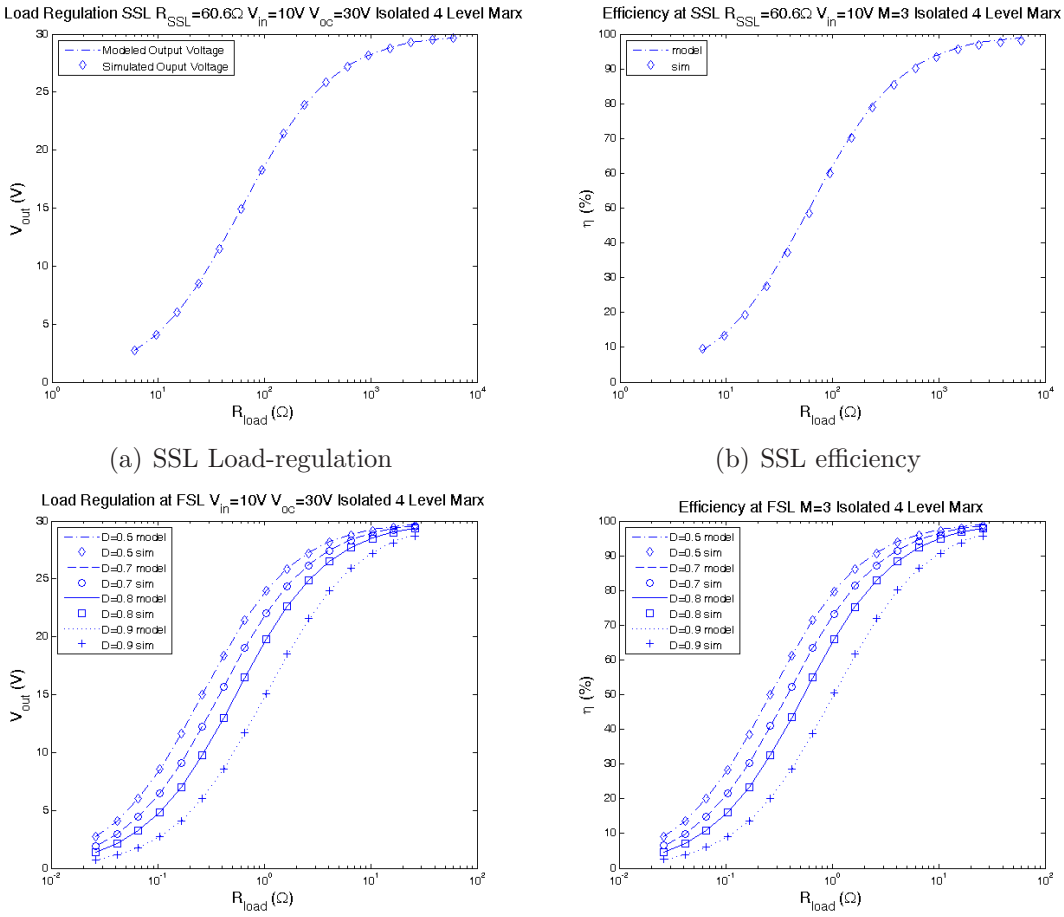
$$R_{FSL} = \frac{1}{D}(R_{sw1} + R_{sw4} + R_{sw7}) + \frac{1}{1-D}(4R_{sw2} + 4R_{sw3} + R_{sw5} + R_{sw6}). \tag{D.63}$$

If we assume that all switches have the same on-resistance,

$$\boxed{R_{FSL} = \frac{3R_{on}}{D} + \frac{10R_{on}}{1-D}}. \tag{D.64}$$

Model validation plots of load regulation and efficiency for both switching speed limits are shown in Figure D-21. These plots, like the ones for the three-level class-II marx, show that efficiency is best when the output voltage equals the open-circuit output voltage. They also show that both load regulation and efficiency are best at a

50% duty ratio as derived above. Because the class-II marx operates most efficiently when the open-circuit output voltage equals the load voltage (light loads), it may be advantageous to use a so-called reconfigurable class-II marx converter that can switch between boosting modes. For instance, this four-level converter might boost to three times the input voltage under some conditions but if the load becomes heavier or if the input voltage increases, it might be reconfigured in real-time to boost only to twice the input voltage. Both of these modes can be achieved with the switching patterns described and analyzed in this section. This real-time reconfiguring approach may be one way that the marx converter could be controlled to efficiently regulate the output voltage amidst load and input voltage variations.



(a) SSL Load-regulation

(b) SSL efficiency

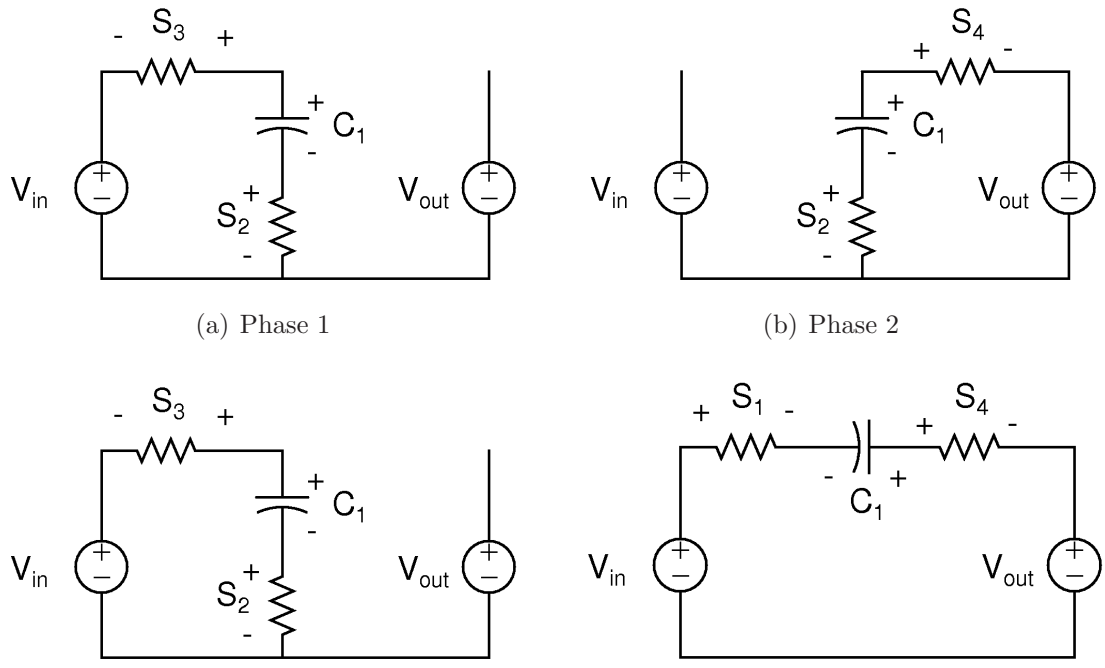
(c) FSL Load-regulation

(d) FSL efficiency

Figure D-21: Model and simulation agreement of load regulation and efficiency for the four-level marx boosting to three times the input voltage.

D.7 Class-III Marx

The class-III marx is similar to multi-level DC/DC converters because it drives the output to two different voltage levels. In order to balance the switched-capacitors, recharge phases must be included between states that drive the output to the two levels. Therefore, for the three-level marx, the switching pattern ends up being that shown in Figure D-22. Phases 1 and 3 are both the recharge switch state from the class-II three-level marx and are the three-level equivalent of the $\star$-state from the four-level class-II marx. Phases 2 and 4 come from the marx switch states presented in the beginning of this work.



(a) Phase 1

(b) Phase 2

(c) Phase 3

(d) Phase 4

Figure D-22: The four simplified switching states of the class-III converter. Phases 1 and 3 are the same recharging switch state.

I approached the analysis of the class-III marx in the SSL as follows. Using the

fact that the switched-capacitor equilibrates during each phase to

$$V_c^{(1)} = V_{in} \tag{D.65}$$
$$V_c^{(2)} = V_{out} \tag{D.66}$$
$$V_c^{(3)} = V_{in} \tag{D.67}$$
$$V_c^{(4)} = V_{out} - V_{in}, \tag{D.68}$$

so that the changes in capacitor voltage from cycle-to-cycle are

$$\Delta V_c^{(1-2)} = V_{out} - V_{in} \tag{D.69}$$
$$\Delta V_c^{(2-3)} = V_{in} - V_{out} \tag{D.70}$$
$$\Delta V_c^{(3-4)} = 2V_{in} - V_{out} \tag{D.71}$$
$$\Delta V_c^{(4-1)} = V_{out} - 2V_{in} \tag{D.72}$$

and adding up the $1/2C\Delta V_C^2$ losses per cycle the time averaged power loss is

$$P_{loss} = C_1 f_{sw}((V_{out} - 2V_{in})^2 + (V_{out} - V_{in})^2). \tag{D.73}$$

From here, we can recognize the loss terms and try to form a loss model of this converter. The proposed loss model, shown in Figure D-23, includes a resistance that bridges the ideal transformer as well as one that looks like the output resistance in the original loss model of Figure D-1.

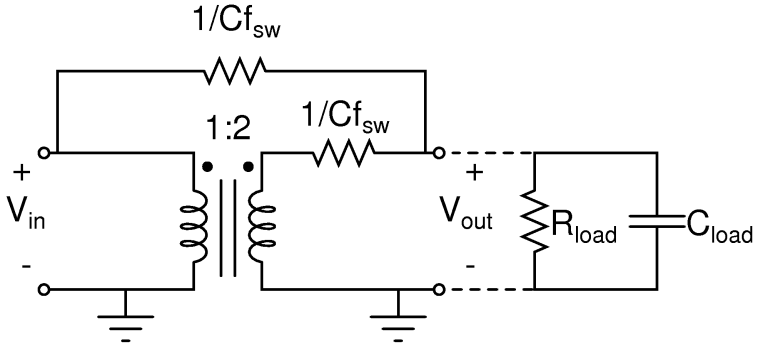


Figure D-23: The loss and load regulation model for the class-III marx.

From the proposed loss model in Figure D-23, the open circuit voltage can be found using KCL and taking into account the ideal transformation of the input voltage to the secondary:

$$\frac{V_{in} - V_{oc}}{R_{eq1}} = \frac{V_{oc} - 2V_{in}}{R_{eq2}}, \tag{D.74}$$

where $R_{eq1} = R_{eq2} = 1/f_{sw}C_1$. Now the open circuit voltage can be solved as

$$\boxed{V_{oc} = \frac{3}{2}V_{in}} \tag{D.75}$$

as we'd expect from the action of the converter. By applying the load to the loss model, the load regulation of the output voltage can be found again with KCL,

$$\frac{V_{in} - V_{oc}}{R_{eq1}} = \frac{V_{oc} - 2V_{in}}{R_{eq2}} + I_{out}, \tag{D.76}$$

where we can substitute $I_{out} = V_{out}/R_{load}$ (time-averaged quantities) and collect terms to get

$$\boxed{V_{out} = 3V_{in}\left(\frac{R_{load}}{2R_{load} + R_{eq}}\right)} \tag{D.77}$$

where $R_{eq} = 1/f_{sw}C_1$.

Now, efficiency can be calculated as

$$\eta = 1 - \frac{P_{loss}}{P_{in}}, \tag{D.78}$$

where P_{loss} can be found by plugging the output voltage from eqn. (D.77) into eqn. (D.73) to get a closed-form expression of P_{loss}.

P_{in} can be calculated by finding I_{in} from the loss model as

$$I_{in} = \frac{5V_{in} - 3V_{out}}{R_{eq}} \tag{D.79}$$

into which we can plug V_{out} from eqn. (D.77) to get a closed-form expression of $P_{in} = V_{in}I_{in}$ and the efficiency in the slow-switching-limit.

In the FSL, we treat the capacitor voltage as fixed. Adding up the switch losses

in each phase leads to the time-averaged power loss:

$$P_{loss} = \frac{(V_c - V_{in})^2}{2R_{on}} 2D^{(1)} + \frac{(V_c - V_{out})^2}{2R_{on}} D^{(2)} + \frac{(V_{in} + V_c - V_{out})^2}{2R_{on}} D^{(4)}, \tag{D.80}$$

where we have assumed that all switches have on-resistance R_{on} and that the time spent in phases 1 and 3 are the same and represented by $D^{(1)} = D^{(3)}$. Note that $D^{(1)} + D^{(2)} + D^{(3)} + D^{(4)} = 1$.

The capacitor voltage can be found from the charge-balance constraint

$$R_{on} \sum_j i_c^{(j)} = 0 = \frac{V_{in} - V_c}{2} 2D^{(1)} + \frac{V_{out} - V_c}{2} D^{(2)} + \frac{V_{out} - V_c - V_{in}}{2} D^{(4)} \tag{D.81}$$

which leads to

$$V_c = \frac{V_{in}(D^{(1)} - \frac{1}{2}D^{(4)}) + V_{out}(\frac{D^{(2)}+D^{(4)}}{2})}{D^{(1)} + \frac{D^{(2)}+D^{(4)}}{2}}. \tag{D.82}$$

The output voltage can be found from $V_{out} = I_{out} R_{load}$:

$$V_{out} = \frac{R_{load}}{2R_{on}} \left(D^{(2)}(V_c - V_{out}) + D^{(4)}(V_{in} + V_c - V_{out}) \right). \tag{D.83}$$

Plugging V_c into this expression for V_{out} leads to the closed-form solution. Finally, efficiency here can be calculated as

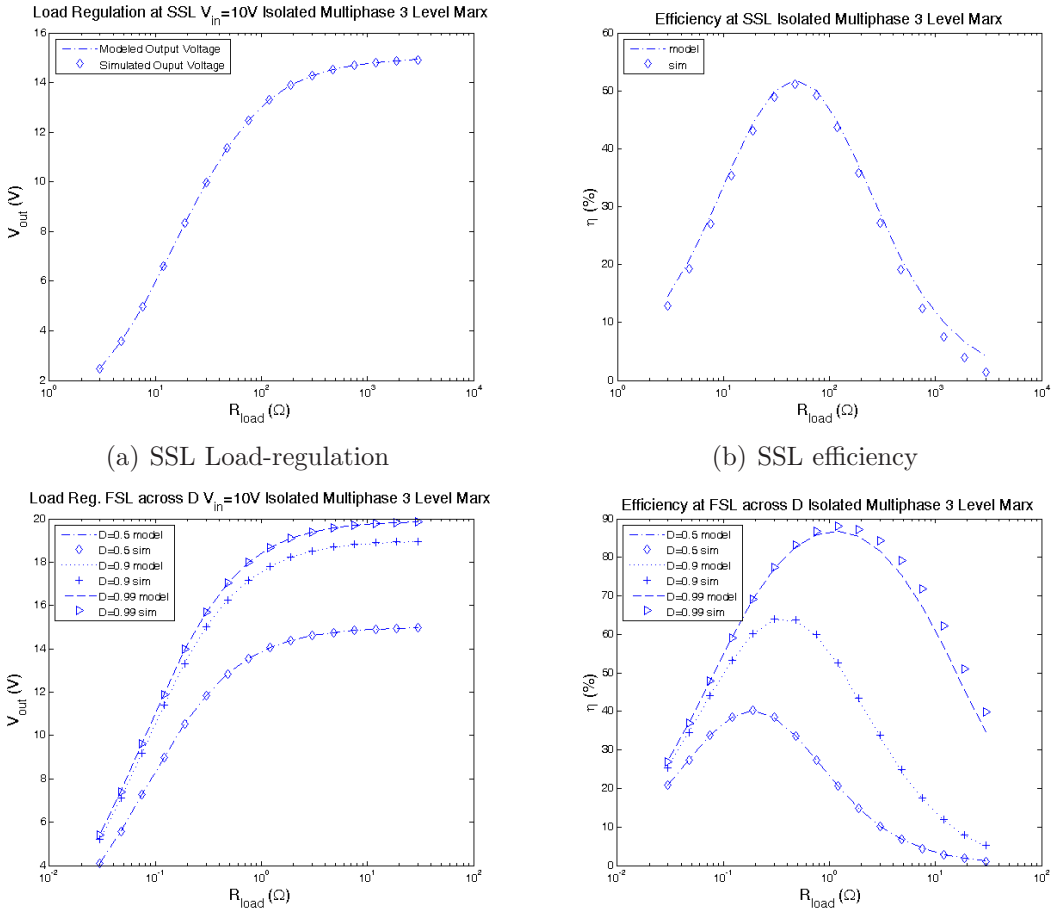
$$\eta = (1 + \frac{P_{loss}}{V_{out}^2 / R_{load}})^{-1} \tag{D.84}$$

using the expression for P_{loss} in eqn. (D.80) with the expressions for capacitor voltage in eqn. (D.82) and output voltage in eqn. (D.83). Model validation plots of load regulation and efficiency for the class-III marx in both switching speed limits are shown in Figure D-24. In the FSL plots, the duty ratio is the time spent in phase 2 with respect to phase 4 holding the total $D^{(2)} + D^{(4)} = 0.5$.

From the plots, we see that in the SSL, this converter can achieve a step-up in voltage but suffers from poor efficiency. On the other hand, in the FSL, the converter can achieve both a variable step-up in voltage and good efficiency for extreme duty

ratios as defined above. In the class-III marx, efficiency is best at some optimum load point as opposed to the class-II marx, for which the lightest load is optimum.

From these observations, we can conclude that the class-II converter is best suited for light loads or situations in which the open-circuit output voltage of the converter can be adjusted to suit the load. On the other hand, the class-III converter may achieve better efficiencies at medium loads. Further work might investigate how the converter behaves in FSL when varying all four duty ratios $D^{(1)}, D^{(2)}, D^{(3)}$ and $D^{(4)}$ for the four phases in the class-III switching pattern.



(a) SSL Load-regulation

(b) SSL efficiency

(c) FSL Load-regulation

(d) FSL efficiency

Figure D-24: Model and simulation agreement of load regulation and efficiency for the three-level class-III marx.

D.8 Discussion, Conclusion, and Further Work

This work should serve as a vantage point from which further work could investigate how to effectively utilize the marx converter as a DC/DC converter. The analysis and model validation of the types of converters here are intended to serve as demonstrative examples of how one could treat the converter under different switching patterns.

The results show that the class-I converter generally yields poor efficiency and can only provide a step-up in voltage in the fast-switching-limit. However, the class-II converter yields excellent efficiency at light loads, similar to the switched-capacitor converters analyzed by Seeman et. al. in [30], and may be reconfigured on the fly to match the load voltage to the convert's open-circuit output voltage in order to regulate efficiently despite load and input variations. Furthermore, the class-III converter shows good efficiency especially at extreme duty ratios and medium loads. Therefore, sophisticated control approaches could reconfigure the marx converter between classes of switching patterns to achieve good efficiency across a wide range of loads.

In the analyses provided here, the switches were assumed to be able to block voltage and carry current in both directions. This assumption directly impacts the analysis of the converters. Figure D-25 shows one example of a switch implementation that enables bidirectional carrying and blocking. Further work might investigate optimal switch implementations for each class of switching pattern or for converters that are intended to be reconfigured between switching patterns. Further work might also show how the converter might be fundamentally altered by changing the switch implementation characteristics. It may be that there are switching pattern-switch implementation combinations that lead to very advantageous converter characteristics.

The switching pattern classification proposed here is not intended to be complete. It is only intended to organize the converters analyzed. Therefore, further work could generalize the switching pattern classification. For instance, a complete switching pattern classification could capture patterns in which the input and output are connected to the circuit an arbitrary number of times per full cycle and how these intersect with

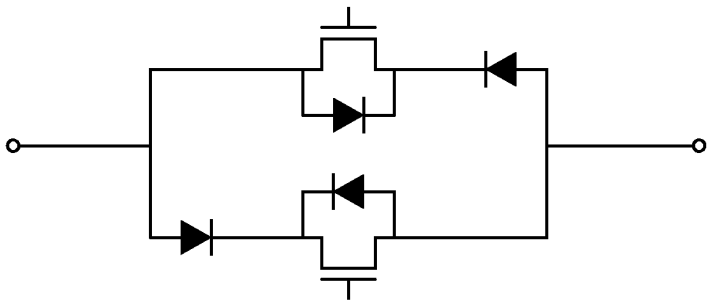


Figure D-25: A "fully-capable" switch implementation.

the isolated and non-isolated cases. Ultimately, such classifications along with their loss models could be generalized to an arbitrary number of levels. Also, there are several loss mechanisms not considered here such as gate loss. Study of these loss mechanisms could ultimately lead to preference of one redundant switching pattern over another or even one switching pattern classification over another.

Finally, the effect of adding the loss due to always-on switches back into the class-II reconfigurable converter could be validated against simulation. Also, all of the results could also be generalized to capture differences in on-state switch resistances, whereas in these analyses, I generally assumed that they were all the same for simplicity.

Bibliography

[1] J. J. Cooley, A.-T. Avestruz, and S. B. Leeb, "A retrofit capacitive sensing occupancy detector using fluorescent lamps." Accepted for publication IEEE Transactions on Industrial Electronics, Special Issue on Modern Ballast Technology, March 2011.

[2] J. Smith, "Field mice: Extracting hand geometry from electric field measurements," *IBM Systems Journal*, vol. 35, 1996.

[3] Y. Ahmed and S. Rowland, "Modelling linesmen's potentials in proximity to overhead lines," *Power Delivery, IEEE Transactions on*, vol. 24, pp. 2270 –2275, Oct. 2009.

[4] W. Buller and B. Wilson, "Measurement and modeling mutual capacitance of electrical wiring and humans," *Instrumentation and Measurement, IEEE Transactions on*, vol. 55, pp. 1519 –1522, Oct. 2006.

[5] O. Fujiwara and T. Ikawa, "Numerical calculation of human-body capacitance by surface charge method," *Electronics and Communications in Japan*, vol. 85, no. 12, 2002.

[6] B. George, H. Zangl, T. Bretterklieber, and G. Brasseur, "A novel seat occupancy detection system based on capacitive sensing," in *Instrumentation and Measurement Technology Conference Proceedings, 2008. IMTC 2008. IEEE*, pp. 1515 –1519, May 2008.

[7] N. Karlsson and J.-O. Jarrhed, "A capacitive sensor for the detection of humans in a robot cell," in *Instrumentation and Measurement Technology Conference, 1993. IMTC/93. Conference Record., IEEE*, pp. 164 –166, May 1993.

[8] A. Shahidi and P. Savard, "A volume conductor model of the human thorax for field calculations," in *Engineering in Medicine and Biology Society, 1990., Proceedings of the Twelfth Annual International Conference of the IEEE*, pp. 615 –616, Nov 1990.

[9] A. Ueno, Y. Akabane, T. Kato, H. Hoshino, S. Kataoka, and Y. Ishiyama, "Capacitive sensing of electrocardiographic potential through cloth from the dorsal surface of the body in a supine position: A preliminary study," *Biomedical Engineering, IEEE Transactions on*, vol. 54, pp. 759 –766, April 2007.

[10] D. H. Wolaver, *Phase-Locked Loop Circuit Design*. P T R Prentice Hall, Englewood Cliffs, NJ 07632, 1991.

[11] C. International Rectifier, El Segundo, "Ir21592 datasheet." Datasheet, Sept. 2005.

[12] R. Middlebrook and S. Cuk, "A general unified approach to modeling switching-converter power stages," *International Journal of Electronics*, vol. 42, pp. 521–550, June 1977.

[13] R. Middlebrook, "Input filter considerations in design and application of switching regulators," *IEEE Industry Applications Society Annual Meeting*, vol. 1, no. 76CH1122-1-IA, p. 366382, 1976.

[14] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics, Second Edition*. Springer Science+Business Media, LLC., 2001.

[15] C. Wang and M. Nehrir, "Dynamic modeling and simulation of solid oxide fuel cells," in *Modelling and Control of Fuel Cells; Distributed Generation Applications*, pp. 85 –115, 2009.

[16] L. Linares, R. Erickson, S. MacAlpine, and M. Brandemuehl, "Improved energy capture in series string photovoltaics via smart distributed power electronics," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pp. 904 –910, Feb 2009.

[17] G. Walker and P. Sernia, "Cascaded dc-dc converter connection of photovoltaic modules," *Power Electronics, IEEE Transactions on*, vol. 19, pp. 1130 – 1139, July 2004.

[18] E. Roman, R. Alonso, P. Ibanez, S. Elorduizapatarietxe, and D. Goitia, "Intelligent pv module for grid-connected pv systems," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 1066 –1073, June 2006.

[19] G. Walker and J. Pierce, "Photovoltaic dc-dc module integrated converter for novel cascaded and bypass grid connection topologies 8212; design and optimisation," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1 – 7, June 2006.

[20] W.-Y. Choi, S.-M. Kim, S.-J. Park, K.-H. Kim, and Y.-C. Lim, "High step-up dc-dc converter with high efficiency for photovoltaic module integrated converter systems," in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*, pp. 1 –4, Oct 2009.

[21] B. Yuan, X. Yang, and D. Li, "Analysis and design of a high efficiency current fed multi-resonant converter for high step-up power conversion in renewable energy harvesting," in *Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium on*, pp. 138 –143, June 2010.

[22] J. Enslin, M. Wolf, D. Snyman, and W. Swiegers, "Integrated photovoltaic maximum power point tracking converter," *Industrial Electronics, IEEE Transactions on*, vol. 44, pp. 769 –773, Dec. 1997.

[23] J.-M. Kwon, B.-H. Kwon, and K.-H. Nam, "Three-phase photovoltaic system with three-level boosting mppt control," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 2319 –2327, Sept 2008.

[24] R. Faranda, S. Leva, and V. Maugeri, "Mppt techniques for pv systems: Energetic and cost comparison," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, pp. 1 –6, July 2008.

[25] D. Hohm and M. Ropp, "Comparative study of maximum power point tracking algorithms using an experimental, programmable, maximum power point tracking test bed," in *Photovoltaic Specialists Conference, 2000. Conference Record of the Twenty-Eighth IEEE*, pp. 1699 –1702, Jan. 2000.

[26] Y. Bo, Y. Xu, and L. Donghao, "Application of power compensating concept for high efficiency maximum power point tracking in grid-connected photovoltaic system," in *Power Electronics Conference (IPEC), 2010 International*, pp. 938 –941, June 2010.

[27] C. Sullivan and M. Powers, "A high-efficiency maximum power point tracker for photovoltaic arrays in a solar-powered race vehicle," in *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, pp. 574 –580, June 1993.

[28] J. Lopez-Seguel, S. Seleme, P. Donoso-Garcia, L. Morais, P. Cortizo, and M. Mendes, "Comparison of mppt approaches in autonomous photovoltaic energy supply system using dsp," in *Industrial Technology (ICIT), 2010 IEEE International Conference on*, pp. 1149 –1154, March 2010.

[29] I. Rectifier, "An-978 hv floating mos-gate driver ics." Application Note.

[30] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc x2013;dc converters," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 841 –851, March 2008.

[31] R. D. Middlebrook, "Low-entropy expressions: the key to design-oriented analysis," in *IEEE Frontiers in Education, Twenty-First Annual Conference*, pp. 399–403, September 1991.

[32] M. Arsalan, A. Shamim, L. Roy, and M. Shams, "A fully differential monolithic lna with on-chip antenna for a short range wireless receiver," *Microwave and Wireless Components Letters, IEEE*, vol. 19, pp. 674 –676, Oct. 2009.

[33] B. Sewiolo, G. Fischer, and R. Weigel, "A 30 ghz variable gain amplifier with high output voltage swing for ultra-wideband radar," *Microwave and Wireless Components Letters, IEEE*, vol. 19, pp. 590 –592, Sept. 2009.

[34] S. Chattier, B. Schleicher, T. Feger, T. Purtova, and H. Schumacher, "79 ghz fully integrated fully differential si/sige hbt amplifier for automotive radar applications," in *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, pp. 1011 –1014, Dec. 2006.

[35] K. Cornett, G. Fu, I. Escorcia, and H. Mantooth, "Sige bicmos fully differential amplifier for extreme temperature range applications," in *Aerospace conference, 2009 IEEE*, pp. 1 –10, March 2009.

[36] X.-Y. He, K.-P. Pun, and P. Kinget, "A 0.5-v wideband amplifier for a 1-mhz ct complex delta-sigma modulator," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTESM-I: REGULAR PAPERS*, vol. 56, November 2009.

[37] E. M. Spinelli, P. A. Garcia, and D. O. Guaraglia, "A dual-mode conditioning circuit for differential analog-to-digital converters," *IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT*, vol. 59, January 2010.

[38] J. Weiss, B. Majoux, and G. Bouvier, "A very high gain bandwidth product fully differential amplifier," in *VLSI Design, 1996. Proceedings., Ninth International Conference on*, pp. 99 –102, Jan. 1996.

[39] A. Pletersek, D. Strle, and J. Trontelj, "Low supply voltage, low noise fully differential programmable gain amplifiers," in *European Design and Test Conference, 1995. ED TC 1995, Proceedings.*, pp. 105 –112, Mar. 1995.

[40] J. Karki, "Fully-differential amplifiers; texas instruments application report," August 2000.

[41] J. Karki, "Analysis of fully-differential amplifiers; texas instruments application report," 2005.

[42] A. D. Inc., "Differential drivers for high speed adcs overview," 2009. Analog Devices Tutorial MT-075.

[43] A. Nordeng, "Fully differential amplifier with rail-to-rail outputs offers 16-bit performance at 1mhz on a single 2.5v supply," December 2005. Linear Technology Magazine.

[44] L. T. Coporation, "Lt6404 datasheet." Milipitas, CA 95035.

[45] J. Haspeslagh and W. Sansen, "Design techniques for fully differential amplifiers," in *Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988*, pp. 12.2/1 –12.2/4, May 1988.

[46] T.-S. Lee, H.-Y. Chung, and S.-M. Cai, "Design techniques for low-voltage fully differential cmos switched-capacitor amplifiers," in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, p. 4 pp., 2006.

[47] S.-W. Sin, S.-P. U, and R. Martins, "Generalized circuit techniques for low-voltage high-speed reset- and switched-opamps," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTESM-I: REGULAR PAPERS*, vol. 55, September 2008.

[48] M. Dessouky and A. Kaiser, "Very low-voltage fully differential amplifier for switched-capacitor applications," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 5, pp. 441 –444 vol.5, 2000.

[49] E. Peeters, M. Steyaert, and W. Sansen, "Hf measurement procedure for fully differential building blocks," in *Instrumentation and Measurement Technology Conference*, 1996.

[50] G. Xu and S. Embabi, "A systematic approach in constructing fully differential amplifiers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 1343–1347, November 2000.

[51] O. J. Hurst and S. H. Lewis, "Determination of stability using return ratios in balanced fully differential feedback circuits," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 42, December 1995.

[52] P. Crovetti and F. Fiori, "Finite common-mode rejection in fully differential operational amplifiers," *Electronics Letters*, vol. 42, May 2006.

[53] R. Wu, K. Makinwa, and J. Huijsing, "The design of a chopped current-feedback instrumentation amplifier," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, pp. 2466 –2469, May 2008.

[54] H. Xie and G. Fedder, "A cmos z-axis capacitive accelerometer with comb-finger sensing," in *Micro Electro Mechanical Systems, 2000. MEMS 2000. The Thirteenth Annual International Conference on*, pp. 496 –501, Jan 2000.

[55] G. Zhang, H. Xie, L. de Rosset, and G. Fedder, "A lateral capacitive cmos accelerometer with structural curl compensation," in *Micro Electro Mechanical Systems, 1999. MEMS '99. Twelfth IEEE International Conference on*, pp. 606 –611, Jan 1999.

[56] R. D. Middlebrook, *Differential Amplifiers*. John Wiley and Sons, Inc., 1963.

[57] L. J. Giacoletto, *Differential Amplifiers*. Wiley-Interscience, 1970.

[58] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. John Wiley and Sons, Inc., 2001.

[59] U. S. D. of Energy, "The smart grid: An introduction," August 2009.

[60] U. D. of Energy, "Annual energy outlook 2010 tables a4 and a5." Energy Information Administration, February 2010.

[61] W. Yan, S. Hui, and H.-H. Chung, "Energy saving of large-scale high-intensity-discharge lamp lighting networks using a central reactive power control system," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 3069 –3078, Aug. 2009.

[62] E. Bueno, A. Hernandez, F. Rodriguez, C. Giron, R. Mateos, and S. Cobreces, "A dsp- and fpga-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 654 –669, March 2009.

[63] A. Timbus, M. Larsson, and C. Yuen, "Active management of distributed energy resources using standardized communications and modern information technologies," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 4029 –4037, Oct. 2009.

[64] J. Cooley, A.-T. Avestruz, and S. Leeb, "An autonomous distributed demand-side energy management network using fluorescent lamp sensors," in *PESC 2008. IEEE*, June 2008.

[65] C. S. Moo, K. H. Lee, H. L. Cheng, and W. M. Chen, "A single-stage high-power-factor electronic ballast with zvs buck x2013;boost conversion," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 1136 –1146, April 2009.

[66] R. Orletti, M. Co, D. Simonetti, and J. de Freitas Vieira, "Hid lamp electronic ballast with reduced component number," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 718 –725, March 2009.

[67] T.-E. Jang, H.-J. Kim, and H. Kim, "Dimming control characteristics of electrodeless fluorescent lamps," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 93 –100, Jan. 2009.

[68] L. R. Center, "Investigation of the effects of dimming on fluorescent lamp life," tech. rep., Rensselaer Polytechnic Institute, 2010.

[69] P. Zappi, E. Farella, and L. Benini, "Enhancing the spatial resolution of presence detection in a pir based wireless surveillance network," in *Advanced Video and Signal Based Surveillance, 2007. AVSS 2007. IEEE Conference on*, pp. 295 –300, Sept. 2007.

[70] Z. Zhang, X. Gao, J. Biswas, and J. K. Wu, "Moving targets detection and localization in passive infrared sensor networks," in *Information Fusion, 2007 10th International Conference on*, pp. 1 –6, July 2007.

[71] H. H. Kim, K. N. Ha, S. Lee, and K. C. Lee, "Resident location-recognition algorithm using a bayesian classifier in the pir sensor-based indoor location-aware system," *Systems, Man, and Cybernetics, Part C: Applications and Reviews, IEEE Transactions on*, vol. 39, pp. 240 –245, March 2009.

[72] T. Lim and M. Moghavvemi, "Capacitive fingerprint sensor chip for automatic matching," in *TENCON 2000. Proceedings*, vol. 2, pp. 442 –446 vol.2, 2000.

[73] T. Shimamura, H. Morimura, N. Shimoyama, T. Sakata, S. Shigematsu, K. Machida, and M. Nakanishi, "A fingerprint sensor with impedance sensing for fraud detection," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 170 –604, Feb. 2008.

[74] M.-L. Sheu, C.-K. Lai, W.-H. Hsu, and H.-M. Yang, "A novel capacitive sensing scheme for fingerprint acquisition," in *Electron Devices and Solid-State Circuits, 2005 IEEE Conference on*, pp. 627 – 630, Dec. 2005.

[75] M. Tartagni and R. Guerrieri, "A fingerprint sensor based on the feedback capacitive sensing scheme," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 133 –142, Jan 1998.

[76] H. Chu, J. Mills, and W. Cleghorn, "Design of a high sensitivity capacitive force sensor," in *Nanotechnology, 2007. IEEE-NANO 2007. 7th IEEE Conference on*, pp. 29 –33, Aug. 2007.

[77] F. Han, Q. Wu, R. Zhang, and J. Dong, "Capacitive sensor interface for an electrostatically levitated micromotor," *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, pp. 3519 –3526, Oct. 2009.

[78] S. Jawed, D. Cattin, N. Massari, M. Gottardi, B. Margesin, and A. Baschirotto, "A simplified modeling approach for a mems capacitive sensor," in *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, pp. 112 –115, Aug. 2007.

[79] A. Kuijpers, R. Wiegerink, G. Krijnen, T. Lammerink, and M. Elwenspoek, "Capacitive long-range position sensor for microactuators," in *Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS)*, pp. 544 – 547, 2004.

[80] J.-I. Lee, X. Huang, and P. Chu, "Nanoprecision mems capacitive sensor for linear and rotational positioning," *Microelectromechanical Systems, Journal of*, vol. 18, pp. 660 –670, June 2009.

[81] S. Chatzandroulis, D. Tsoukalas, and P. Neukomm, "A miniature pressure system with a capacitive sensor and a passive telemetry link for use in implantable applications," *Microelectromechanical Systems, Journal of*, vol. 9, pp. 18 –23, Mar 2000.

[82] M. Dokmeci and K. Najafi, "A high-sensitivity polyimide capacitive relative humidity sensor for monitoring anodically bonded hermetic micropackages," *Microelectromechanical Systems, Journal of*, vol. 10, pp. 197 –204, June 2001.

[83] T. Fabian and G. Brasseur, "A robust capacitive angular speed sensor," *Instrumentation and Measurement, IEEE Transactions on*, vol. 47, pp. 280 –284, Feb 1998.

[84] C.-Y. Lee, S.-H. Nam, S.-G. Lee, D.-W. Kim, and M.-K. Choi, "High frequency partial discharge measurement by capacitive sensor for underground power cable system," in *Power System Technology, 2000. Proceedings. PowerCon 2000. International Conference on*, vol. 3, pp. 1517 –1520 vol.3, 2000.

[85] E. Ghafar-Zadeh and M. Sawan, "A hybrid microfluidic/cmos capacitive sensor dedicated to lab-on-chip applications," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 1, pp. 270 –277, Dec. 2007.

[86] C. Merritt, H. Nagle, and E. Grant, "Textile-based capacitive sensors for respiration monitoring," *Sensors Journal, IEEE*, vol. 9, pp. 71 –78, Jan. 2009.

[87] T. Salpavaara, J. Verho, and J. Lekkala, "Capacitive insole sensor for hip surgery rehabilitation," in *Pervasive Computing Technologies for Healthcare, 2008. PervasiveHealth 2008. Second International Conference on*, pp. 311 –314, 30 2008-feb. 1 2008.

[88] Y.-J. Wen, J. Granderson, and A. Agogino, "Towards embedded wireless-networked intelligent daylighting systems for commercial buildings," in *Sensor Networks, Ubiquitous, and Trustworthy Computing, 2006. IEEE International Conference on*, vol. 1, p. 6 pp., June 2006.

[89] E. Deng and S. Cuk, "Negative incremental impedance and stability of fluorescent lamps," in *Applied Power Electronics Conference and Exposition, 1997. APEC '97 Conference Proceedings 1997., Twelfth Annual*, vol. 2, pp. 1050 –1056 vol.2, Feb 1997.

[90] A. D. Inc., "Ad8620 datasheet," 2008.

[91] T. I. Inc., "Ths4140 datasheet," 2004.

[92] J. K. Roberge, *Operational Amplifiers: Theory and Practice*. John Wiley and Sons, Inc., 1975.

[93] L. T. Corp., "Ltc2440 datasheet," 2002.

[94] L. T. Corp., "Ltc2051 datasheet," 2000.

[95] K. Nabors and J. White, "Multipole-accelerated capacitance extraction algorithms for 3-d structures with multiple dielectrics," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 39, pp. 946 –954, Nov 1992.

[96] J. Cooley, A.-T. Avestruz, and S. Leeb, "Proximity detection and ranging using a modified fluorescent lamp for security applications," in *Carnahan Conferences Security Technology, Proceedings 2006 40th Annual IEEE International*, pp. 1 –8, Oct. 2006.

[97] J. Cooley, A.-T. Avestruz, and S. Leeb, "A modified fluorescent lamp for discreet biometric surveillance," in *Technologies for Homeland Security, 2007 IEEE Conference on*, pp. 227 –233, May 2007.

[98] J. J. Cooley, "Capacitive sensing with a fluorescent lamp," Master's thesis, Massachusetts Institute of Technology, Cambridge, Massachusetts, 2007.

[99] J. Cooley, A.-T. Avestruz, S. Leeb, and L. Norford, "A fluorescent lamp with integral proximity sensor for building energy management," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, pp. 1157 –1163, June 2007.

[100] S. Ben-Yaakov, M. Shvartas, and S. Glozman, "Statics and dynamics of fluorescent lamps operating at high frequency: Modeling and simulation," *IEEE Transactions On Industry Applications*, vol. 38, Dec. 2002.

[101] R. E. Best., *Phase-Locked Loops: Design, Simulation, And Applications*. McGraw-Hill, New York, 1999.

[102] "Annual energy outlook 2009." Energy Information Administration: United States Department of Energy, March 2009.

[103] D. Steigerwald, J. Bhat, D. Collins, R. Fletcher, M. Holcomb, M. Ludowise, P. Martin, and S. Rudaz, "Illumination with solid state lighting technology," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 8, pp. 310–320, Mar/Apr 2002.

[104] I.-H. Oh, "A soft-switching synchronous buck converter for zero voltage switching (zvs) in light and full load conditions," in *Proc. Twenty-Third Annual IEEE Applied Power Electronics Conf. and Exposition APEC 2008*, pp. 1460–1464, 2008.

[105] K. I. Hwu and Y. T. Yau, "Simple design of a soft-switching buck converter," in *Proc. IEEE Int. Conf. Sustainable Energy Technologies ICSET 2008*, pp. 410–414, 2008.

[106] J.-H. Park and B.-H. Cho, "Nonisolation soft-switching buck converter with tapped-inductor for wide-input extreme step-down applications," *IEEE J CASI RP*, vol. 54, no. 8, pp. 1809–1818, 2007.

[107] M. Dyble, N. Narendran, A. Bierman, and T. Klein, "Impact of dimming white leds: Chromacity shifts due to different dimming methods," in *Fifth International Conference on Solid State Lighting, Proceedings of SPIE 5941*, (Bellingham, WA), pp. 291–299, International Society of Optical Engineers, 2005.

[108] Y. Gu, N. Narendran, T. Dong, and H. Wu, "Spectral and luminous efficacy change of high-power leds under different dimming methods," in *Sixth International Conference on Solid State Lighting, Proceedings of SPIE 6337, 63370J*, 2006.

[109] S. Muthu, F. J. Schuurmans, and M. D. Pashley, "Red, green, and blue led based white light generation: issues and control," in *Proc. 37th IAS Annual Meeting Industry Applications Conf. Conf. Record of the*, vol. 1, pp. 327–333, 2002.

[110] C. M.-S. Fu and D. D.-C. Lu, "Shorting-inductor approach for dimming high power light-emitting diodes," in *Proc. Int. Conf. Power Electronics and Drive Systems PEDS 2009*, pp. 417–422, 2009.

[111] K. H. Loo, W.-K. Lun, S.-C. Tan, Y. M. Lai, and C. K. Tse, "On driving techniques for leds: Toward a generalized methodology," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2967–2976, 2009.

[112] W.-K. Lun, K. H. Loo, S.-C. Tan, Y. M. Lai, and C. K. Tse, "Bilevel current driving technique for leds," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2920–2932, 2009.

[113] S. Beczkowski and S. Munk-Nielsen, "Led spectral and power characteristics under hybrid pwm/am dimming strategy," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 731–735, 2010.

[114] Y.-K. Lo, K.-H. Wu, K.-J. Pai, and H.-J. Chiu, "Design and implementation of rgb led drivers for lcd backlight modules," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 12, pp. 4862–4871, 2009.

[115] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin, and S.-C. Mou, "A high-efficiency dimmable led driver for low-power lighting applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 2, pp. 735–743, 2010.

[116] K. I. Hwu and Y. T. Yau, "Powering led using high-efficiency sr flyback converter," *IEEE Transactions on Industry Applications*, no. 99, 2011. Early Access.

[117] G. C. V. John G. Kassakian, Martin F. Schlect, *Principles of Power Electronics*. Addison-Wesley, 1991.

[118] J. Cooley, D. Vickery, A.-T. Avestruz, A. Englehart, J. Paris, and S. Leeb, "Solid-state lamp with integral occupancy sensor," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 2305 –2313, 21-25 2010.

[119] K. Taylor, J. Ward, V. Gerasimov, and G. James, "Sensor actuator networks supporting agents for distributed energy management," in *29th Annual IEEE*

International Conference on Local Computer Networks, (Bellingham, WA), pp. 463 – 470, November 2004.

[120] E. I. A. U. S. D. of Energy, "Annual energy outlook 2007," February 2007.

[121] A. Emadi and M. Ehsani, "Multi-converter power electronic systems: definition and applications," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 2, pp. 1230 –1236 vol.2, 2001.

[122] A. Emadi and A. Ehsani, "Dynamics and control of multi-converter dc power electronic systems," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 1, pp. 248 –253 vol. 1, 2001.

[123] A. Khaligh, "Realization of parasitics in stability of dc x2013;dc converters loaded by constant power loads in advanced multiconverter automotive systems," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 2295 –2305, June 2008.

[124] A. Emadi, "Modeling and analysis of multiconverter dc power electronic systems using the generalized state-space averaging method," *Industrial Electronics, IEEE Transactions on*, vol. 51, pp. 661 – 668, June 2004.

[125] L. Del Ferraro and F. Capponi, "Stability conditions for multi-converter power systems," in *Vehicle Power and Propulsion, 2005 IEEE Conference*, p. 6 pp., 2005.

[126] Y. Zhang and Z. Jiang, "Dynamic power sharing strategy for active hybrid energy storage systems," in *Vehicle Power and Propulsion Conference, 2009. VPPC '09. IEEE*, pp. 558 –563, Sept. 2009.

[127] R. Nilsen and I. Sorfonn, "Hybrid power generation systems," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, pp. 1 –9, Sept. 2009.

[128] Z. Jiang, "Power management of hybrid photovoltaic - fuel cell power systems," in *Power Engineering Society General Meeting, 2006. IEEE*, p. 6 pp., 2006.

[129] F. Musavi, K. Al-Haddad, and H. Kanaan, "A novel large signal modelling and dynamic analysis of paralleled dc/dc converters with automatic load sharing control," in *Industrial Technology, 2004. IEEE ICIT '04. 2004 IEEE International Conference on*, vol. 1, pp. 536 – 541 Vol. 1, Dec. 2004.

[130] V. Thottuvelil and G. Verghese, "Analysis and control design of paralleled dc/dc converters with current sharing," *Power Electronics, IEEE Transactions on*, vol. 13, pp. 635 –644, Jul 1998.

[131] J. Rajagopalan, K. Xing, Y. Guo, F. Lee, and B. Manners, "Modeling and dynamic analysis of paralleled dc/dc converters with master-slave current sharing control," in *Applied Power Electronics Conference and Exposition, 1996. APEC*

'96. Conference Proceedings 1996., Eleventh Annual, vol. 2, pp. 678 –684 vol.2, Mar 1996.

[132] I. Zafrany and S. Ben-Yaakov, "Average modeling, analysis and simulation of current shared dc-dc converters," in *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE*, vol. 1, pp. 640 –646 vol.1, May 1998.

[133] Y. Panov and M. Jovanovic, "Stability and dynamic performance of current-sharing control for paralleled voltage regulator modules," in *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, vol. 2, pp. 765 –771 vol.2, 2001.

[134] A. Garg, D. Perreault, and G. Verghese, "Feedback control of paralleled symmetric systems, with applications to nonlinear dynamics of paralleled power converters," in *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, vol. 5, pp. 192 –197 vol.5, 1999.

[135] V. Vorperian, "Simplified analysis of pwm converters using model of pwm switch. continuous conduction mode," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 26, pp. 490 –496, May 1990.

[136] B. Choi, B. Cho, R. Ridley, and F. Lee, "Control strategy for multi-module parallel converter system," in *Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE*, pp. 225 –234, June 1990.

[137] R. Ridley, B. Cho, and F. Lee, "Analysis and interpretation of loop gains of multiloop-controlled switching regulators [power supply circuits]," *Power Electronics, IEEE Transactions on*, vol. 3, pp. 489 –498, Oct 1988.

[138] D. Garabandic and T. Petrovic, "Modeling parallel operating pwm dc/dc power supplies," *Industrial Electronics, IEEE Transactions on*, vol. 42, pp. 545 –551, Oct 1995.

[139] R. Middlebrook, "Modelling and analysis methods for dc-to-dc switching converters," *IEEE International Semiconductor Power Converter Conference*, pp. 90–111, 1977.

[140] R. Middlebrook, "A general unified approach to modelling switching dctodc converters in discontinuous conduction mode," *IEEE Power Electronics Specialists Conference*, vol. 32, no. 3, pp. 36–57, 1977.

[141] S. K. Mazumder, K. Acharya, C. L. Haynes, R. Williams, M. R. v. S. Jr., D. J. Nelson, D. F. Rancruel, J. Hartvigsen, and R. S. Gemmen, "Solide-oxide-fuel-cell performance and durability: Resolution of the effects of power-conditioning systems and application loads," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1263–1278, September 2004.

[142] B. W. Q. Huang, R. Hui and J. Zhang, "A review of ac impedance modeling and validation in sofc diagnosis," *Electrochimica Acta*, vol. 52, pp. 8144–8164, November 2007.

[143] E. Ramschak, V. Peinecke, P. Prenninger, T. Schaffer, and V. Hacker, "Detection of fuel cell critical status by stack voltage analysis," *Journal of Power Sources*, vol. 2006, pp. 837–840, October 2006.

[144] R. S. Gemmen, "Analysis for the effect of inverter ripple current on fuel cell operating condition," *Transactions of the ASME*, vol. 125, pp. 576–585, May 2003.

[145] J. Ren, S. Gamble, A. Roscoe, and G. Burt, "Modelling interaction between solid oxide fuel cell, inverters and ac power networks," in *Universities Power Engineering Conference (UPEC), 2009 Proceedings of the 44th International*, pp. 1 –5, Sept. 2009.

[146] J. Ren, A. J. Roscoe, S. Gamble, and G. Burt, "Modelling a reversible solid oxide fuel cell to be used as a storage device within ac power networks," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, pp. 1 –6, April 2010.

[147] C. Gabrielli, "Use and application of electrochemical impedance techniques." Solarton Analytical Technical Report 24, April 1997.

[148] N. Wagner, W. Schnurnberger, B. Müller, and M. Lang, "Electrochemical impedance spectra of solid-oxide fuel cells and polymer membrane fuel cells," *Electrochimica Acta*, vol. 43, no. 24, pp. 3785–3793, 1998.

[149] L. G. A. T. Romero-Castañón and U. Cano-Castillo, "Impedance spectroscopy as a tool in the evaluation of mea's," *Journal of Power Sources*, vol. 118, pp. 179–182, May 2003.

[150] E. Barsoukov and J. R. MacDonald, *Impedance Spectroscopy Theory, Experiment, and Applications*. John Wiley and Sons, Inc., 2005.

[151] R. Middlebrook, "Null double injection and the extra element theorem," *IEEE Trans. on Education*, vol. 32, pp. 90–111, August 1989.

[152] R. Middlebrook, "The two extra element theorem," *Proc. IEEE Frontiers in Education*, pp. 702–708, Sept. 1992.

[153] E. Seger and S. R. Shaw, "In-situ electrical terminal characterization of a 5 kw solid oxide fuel cell stack," *Submitted for publication in the IEEE Transactions on Energy Conversion*, 2010.

[154] R. Johansson, *System Modeling and Identification*. Prentice-Hall, Inc., 1993.

[155] D. J. Hall and R. G. Colclaser, "Transient modeling and simulation of a tubular solid oxide fuel cell," *IEEE Transactions on Energy Conversion*, vol. 14, pp. 749–753, September 1999.

[156] M. H. N. C. Wang and S. R. Shaw, "Dynamic models and model validation for pem fuel cells using electrical circuits," *IEEE Transactions on Energy Conversion*, vol. 20, pp. 442–451, June 2005.

[157] S. Pasricha and S. R. Shaw, "A dynamic pem fuel cell model," *IEEE Transactions on Energy Conversion*, vol. 21, pp. 484–490, June 2006.

[158] P. Krein and R. Balog, "Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and led lighting applications based on minimum capacitance requirements and a ripple power port," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pp. 620 –625, Feb 2009.

[159] P. T. Krein, "Power electronics needs and performance analysis for achieving grid parity solar energy costs." power point presentation.

[160] R. W. Erickson, "Future of power electronics for photovoltaics." power point presentation.

[161] J. K. Mapel, *Organic Photovoltaics and Concentrators*. PhD thesis, Massachusetts Institute of Technology,, 2006.

[162] T. Esram, J. Kimball, P. Krein, P. Chapman, and P. Midya, "Dynamic maximum power point tracking of photovoltaic arrays using ripple correlation control," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 1282 –1291, Sept 2006.

[163] H. Patel and V. Agarwal, "Mppt scheme for a pv-fed single-phase single-stage grid-connected inverter operating in ccm with only one current sensor," *Energy Conversion, IEEE Transactions on*, vol. 24, pp. 256 –263, March 2009.

[164] B. Sahan, A. Vergara, N. Henze, A. Engler, and P. Zacharias, "A single-stage pv module integrated converter based on a low-power current-source inverter," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 2602 –2609, July 2008.

[165] W. Xiao, N. Ozog, and W. Dunford, "Topology study of photovoltaic interface for maximum power point tracking," *Industrial Electronics, IEEE Transactions on*, vol. 54, pp. 1696 –1704, June 2007.

[166] F. Filho, Y. Cao, and L. Tolbert, "11-level cascaded h-bridge grid-tied inverter interface with solar panels," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 968 –972, Feb 2010.

[167] S. Kouro, B. Wu, A. Moya, E. Villanueva, P. Correa, and J. Rodriguez, "Control of a cascaded h-bridge multilevel converter for grid connection of photovoltaic systems," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, pp. 3976 –3982, Nov 2009.

[168] E. Ozdemir, S. Ozdemir, and L. Tolbert, "Fundamental-frequency-modulated six-level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 4407 –4415, Nov 2009.

[169] M. Mousa, M. Ahmed, and M. Orabi, "New converter circuitry for pv applications using multilevel converters," in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*, pp. 1 –6, Oct 2009.

[170] P. Krein and Kim, "Pv converter module configurations for mppt operation," *PECI*, 2010.

[171] M. Seeman, V. Ng, H.-P. Le, M. John, E. Alon, and S. Sanders, "A comparative analysis of switched-capacitor and inductor-based dc-dc conversion technologies," in *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*, pp. 1 –7, June 2010.

[172] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc-dc power conversion," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 380 – 393, March 2006.

[173] M. E. Corp., "Mitsubishi electric photovoltaic module pv-mf170eb4 170wp." Datasheet, June 2006.

[174] J. Martynaitis, "Discussion of "theoretical and experimental analyses of photovoltaic systems with voltage and current-based maximum power point tracking"," *Energy Conversion, IEEE Transactions on*, vol. 19, p. 652, Sept. 2004.

[175] H. Matsuo and F. Kurokawa, "New solar cell power supply system using a boost type bidirectinal dc-dc converter," *Industrial Electronics, IEEE Transactions on*, vol. IE-31, pp. 51 –55, Feb. 1984.

[176] T. Noguchi, S. Togashi, and R. Nakamoto, "Short-current pulse based adaptive maximum-power-point tracking for photovoltaic power generation system," in *Industrial Electronics, 2000. ISIE 2000. Proceedings of the 2000 IEEE International Symposium on*, vol. 1, pp. 157 –162 vol.1, Jan 2000.

[177] C. Yu-yun and M. Yong-kui, "Constant current-based maximum-power-point tracking for photovoltaic power systems," in *Control and Decision Conference, 2009. CCDC '09. Chinese*, pp. 3422 –3425, June 2009.

[178] S. Yuvarajan and J. Shoeb, "A fast and accurate maximum power point tracker for pv systems," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, pp. 167 –172, Feb. 2008.

[179] I. Rectifier, "Irl3714z hexfet power mosfet." Datasheet, 2004.

[180] R. Ram, "Power electronics." ARPA-E Pre Summit Seminar, March 2010.

[181] P. Krein and T. Esram, "Admittance control for anti-islanding protection in modular grid-connected inverters," in *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*, pp. 1 –5, June 2010.

[182] M. S. Inc., "Switchmode power rectifiers mbr20100c." Datasheet, 1996.

[183] J. Kassakian, M. Schlecht, and G. Verghese, *Principles of Power Electronics*. Adison-Wesley Publishing Co., 1992.

[184] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, pp. 1215 –1221 vol.2, June 1995.

[185] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," *Circuits and Systems, IEEE Transactions on*, vol. 24, pp. 517 – 530, Oct 1977.

[186] J. Brugler, "Theoretical performance of voltage multiplier circuits," *Solid-State Circuits, IEEE Journal of*, vol. 6, pp. 132 – 135, June 1971.

[187] Z. Pan, F. Zhang, and F. Peng, "Power losses and efficiency analysis of multilevel dc-dc converters," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, vol. 3, pp. 1393 –1398 Vol. 3, March 2005.

[188] I. Oota, N. Hara, and F. Ueno, "A general method for deriving output resistances of serial fixed type switched-capacitor power supplies," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 3, pp. 503 –506 vol.3, 2000.

[189] G. Zhu and A. Ioinovici, "Switched-capacitor power supplies: Dc voltage ratio, efficiency, ripple, regulation," in *Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE International Symposium on*, vol. 1, pp. 553 –556 vol.1, May 1996.

[190] J. Leon, R. Portillo, S. Vazquez, J. Padilla, L. Franquelo, and J. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 3239 –3248, Sept. 2008.