Feature Scaling of Large, Ballasted, Field Emission Arrays

by

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Abstract

Field emitters are an exciting technology for high-frequency, high-power applications because of their excellent free space electron transport, and their potential for high current density and high current, especially when they are used in an array format. However, a major challenge preventing the widespread use of this technology are the spatial and temporal variations that arise from non-uniformity in emitter tip radius and work function, respectively. To address the problems, various methods of controlling the supply of electrons to the emitter have been developed. One method of current limiting is the vertical ungated field effect transistor (FET), which uses the channel pinch-off and velocity saturation of carriers in silicon combined with a high aspect ratio to provide an effective method of controlling current.

To reduce the operating voltage, and likewise the energy spread of the emitted electrons, we created vertical ungated FET current limiters that were 100 nm in diameter, 8 µm tall, and had a pitch of 1 µm that were patterned using optical lithography. These devices demonstrated excellent current saturation, with output conductances lower than $10^{-11}$ S. In addition, a fabrication process for building nano-sharp emitters on these high aspect ratio pillars was developed. Using this process tip radii of less than 6 nm were obtained on top of the pillars. Process and device simulations were performed that indicate it will be possible to integrate extraction gates with small apertures into this structure, allowing for stable, uniform emission at gate voltages under 20 V in future work.

Thesis Supervisor: Akintunde Ibitayo (Tayo) Akinwande
Title: Professor of Electrical Engineering and Computer Science
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There have been so many people have contributed to my completing this thesis that I’m sure I’ll forget some. Please forgive me.

First and foremost, I must thank my advisor, Professor Tayo Akinwande. I have learned so much from his guidance and his advice, both professionally and personally. His high scientific standard has resulted in my growth as a researcher. It seems that no matter how murky your understanding of a topic may be, after a brief conversation, he can make it seem as clear as a bright summer day. His enthusiasm, support, and, when needed, the occasional push, have been instrumental in the quality of this work.

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The entire Akinwande group, but particularly Melissa Smith, Michael Swanwick, and Annie Wang, has been extremely useful to bounce ideas off of, provided assistance with testing, and occasionally gave a much needed place to vent or a welcome source of distraction. If I were to enumerate all of the ways my group-mates have helped me, there would be little room for much else. The amount of intellectual insight I have gleaned from them is second only to amount of the fun they are.

My friends, who have managed to put up with me, and even offer support, as I go through the many ups and downs of graduate school. You guys are the best. I would like to single out Dave, Chuck, Josh, Zach, Jamie, Nicole, Eva, Arturo, J-Rod, Glen, and, of course, mANiS, for pretty much keeping me sane through this roller coaster ride.

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Thank you, all.
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Chapter 1

Introduction: Vacuum Microelectronics

Electron sources play a vital role in a wide variety of applications ranging from displays to thrusters for spacecraft. The best known application for electron sources is the cathode ray tube (CRT) which was present inside almost every television and computer monitor until the recent explosion of liquid crystal displays (LCDs). For these applications, the main methods of extracting electrons from a material into vacuum are thermionic emission, photo-electron emission, and field emission. In thermionic cathodes, a filament is heated such that the thermal energy imparted to the electrons is sufficient to overcome the work function barrier and escape into vacuum. The work function is the energy difference between the Fermi energy (the equilibrium energy for electrons in a material), and the vacuum energy. In photocathodes, the electrons instead receive the energy from a beam of photons, rather than temperature.

Field emission, the ejection of electrons from a material through the application of an external electrostatic field, has been widely researched since it was first suspected to be a physical effect, distinct from photo or thermal emission, in the early 1900s [6]. This cold-cathode electron source has a range of applications that include imaging and microscopy [7], miniaturized x-ray tubes [8], vacuum sources [9], high frequency amplifiers [10], and display applications [11] [12].

While only two terminals are required for a field emission device, an anode and a
cathode, the field emitter is typically constructed as at least a three terminal device, comprised of an emitter (or tip), an extraction gate (or grid), and a collector (or anode). Additional electrodes may be added to provide electrostatic focusing or lensing action for emitted electrons. Typically, the gate voltage is set to intermediate value between the emitter voltage and the anode voltage, $0 < V_G < V_A$. The gate serves to extract electrons from emitter, and the electrons are subsequently accelerated to the anode by the anode electrostatic field.

To ensure that few collisions occur before the electrons arrive at the anode, a mean free path longer than the distance from the emitter to the anode is required. Consequently, operation in high vacuum (pressure $< 10^{-5}$ Torr) is often needed, since typically the distance from the cathode to the anode is at least several millimeters. With the large electric fields that are present, the ambient gas may experience electron

![Figure 1-1: General structure of a microfabricated field emitter, showing all of the major components of a three-terminal device.](image-url)
impact ionization if the surrounding medium is not vacuum, resulting in plasma
discharge and arcing. This discharge can damage the sharp emitters. In addition,
the gas may adsorb and desorb at the surface of the emitter, changing the local work
function of the material and leading to temporal instabilities in the emission current.

Originally, studies examined a single field emitter with a tip radius of 100nm
to 1 $\mu$m [13]. With the rise of batch fabricated microelectronics, at first interest
in vacuum tubes and vacuum electronics as a whole declined. However, beginning
with the development of the microfabricated Spindt tip at SRI in the 1960s, [14],
research in vacuum microelectronics began to steadily rise. Current state-of-the-art
microfabricated field emitters can have a tip radius that is as small as several atomic
diameters [15].

While circuits utilizing complementary metal-oxide-semiconductor (CMOS) tran-
sistors moved from the integrated circuit to very large scale integration, so has the
field emitter moved into the realm of large field emission arrays (FEAs). These large
FEAs are required to obtain substantial current. Indeed, state of the art field emission
arrays can contain upwards of one billion individual emitters per cm$^2$ with emission
currents as high as 10 $\mu$A / emitter [3] [16].

Because of the ubiquity and rapid commodification of solid-state electronics, the
most appropriate applications for FEAs lie in areas where there are no competing
CMOS electronics. Table 1.1 shows a side-by-side comparison of the main features
of both conventional solid-state electronic devices and vacuum microelectronic de-
vices. The main advantages that vacuum microelectronic devices have over solid-
state devices arise from the excellent transport properties of vacuum when compared
to transport in semiconducting materials at room temperature. While the saturation
velocity in semiconductors at 300 K is limited by scattering events with impurities
and phonons to about $1 \times 10^7$ cm/s in both silicon and gallium arsenide, the electron
velocity in free space can approach the speed of light ($3 \times 10^{10}$ cm/s).

In addition, Semiconductor devices are only able to tolerate limited voltages at
their drain or collector due to the breakdown of semiconductor devices at high electric
fields. The breakdown field is determined by the bandgap of the semiconductor.
Vacuum devices, on the other hand, have much higher breakdown fields. Thus, in any device in which significant power is required, semiconductor devices must resort to techniques that use arrays of devices, whereas with vacuum electronics, a single device is capable of providing significant power.

The frequency performance of standard electronics is poor, with very little gain extending into the upper mm-wave spectral range, which is required for applications such as radar sources. However, compact and efficient electron sources for these devices still do not exist, with many vacuum microwave amplifiers still using thermionic cathodes. Thermionic cathodes are inefficient, requiring filament temperatures greater than 1200 K to operate. In addition, the cathode will degrade with time and need to be replaced. The goal for this project is to create an efficient high current, stable cold cathode emission source that can be used in a variety of applications where high stability, reliability, and uniformity are critical, including high frequency amplifiers, compact x-ray sources, gas ionizers, and multi-electron beam lithography. While the field emission cathode is a platform that could allow for great advancement in all of these areas, in this thesis, the focus will be on field emission cathodes for high frequency amplifiers, in particular those that operate at terahertz (THz) frequencies.

1.1 Motivation: An Integrated THz Amplifier

Terahertz radiation is considered the sub-mm frequency band between 300 GHz and 10.0 THz [17]. The energy of a 1 THz photon is 4 meV, which is near the energy gap between molecular bands [18]. For this reason, THz is particularly exciting for applications investigating the structure and composition of materials, include medical imaging (tomography), biological and chemical sensing, and spectroscopy. In addition, while the atmosphere absorbs radiation in the THz regime quite readily, the bandwidth available is enormous, making it a promising band for high-bandwidth satellite-satellite or satellite-aircraft communications [19].

Despite the wide range of potential applications requiring amplification in the
Table 1.1: Comparison of Vacuum Microelectronic Devices to Conventional Electronics [5]

<table>
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<tr>
<th>Properties</th>
<th>Solid-State Devices</th>
<th>Vacuum Microelectronics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Density</td>
<td>$10^4 - 10^5$ A/cm$^2$</td>
<td>$\approx 2 \times 10^5$ A/cm$^2$</td>
</tr>
<tr>
<td>Bandgap</td>
<td>Structure</td>
<td>Solid/vacuum</td>
</tr>
<tr>
<td>Solid/solid interface</td>
<td></td>
<td>Solid/vacuum</td>
</tr>
<tr>
<td>Injecting Barrier Height</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Structure</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electron Transport Medium</td>
<td>Solid</td>
<td>Vacuum</td>
</tr>
<tr>
<td>Ballistic</td>
<td>$&lt; 0.1 \mu$m, Low temp.</td>
<td>100% ballistic</td>
</tr>
<tr>
<td>Coherence</td>
<td>Length $&lt; 0.1 \mu$m</td>
<td>Length $\gg 0.1 \mu$m</td>
</tr>
<tr>
<td>$t &lt; 10^{-13}$ s at 300 K</td>
<td>$t \gg 10^{-13}$ s</td>
<td></td>
</tr>
<tr>
<td>Lens effect</td>
<td>Difficult</td>
<td>Easy</td>
</tr>
<tr>
<td>Noise</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal noise</td>
<td>Random motion of carriers</td>
<td>Comparable</td>
</tr>
<tr>
<td>Flicker noise</td>
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<td>Worse</td>
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<tr>
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<td>$&lt; 0.3$ eV</td>
<td>Several to 1000+ eV</td>
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<td>500 – 1000+ GHz</td>
</tr>
<tr>
<td></td>
<td>600 GHz (InGaAs)</td>
<td></td>
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<tr>
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<td>Large</td>
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<tr>
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<td>Poor</td>
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<tr>
<td>Temperature Sensitivity</td>
<td>$-30$ – $+50^\circ$C</td>
<td>$&lt; 500^\circ$C</td>
</tr>
<tr>
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<td>Well established (Si)</td>
<td>Not well established</td>
</tr>
<tr>
<td></td>
<td>established (GaAs)</td>
<td></td>
</tr>
<tr>
<td>Applications</td>
<td>Microprocessors, memory devices, optoelectronic devices, rf devices</td>
<td>Flat panel displays, microwave power tubes, electron/ion e-beam lithography, e-beam memories, and excitation devices</td>
</tr>
</tbody>
</table>
There is a gap around 1 THz where neither electronics nor photonics can efficiently work [1].

In the THz regime, there is a lack of commercially available products. This is largely due to the difficulty of reaching THz using both photonics and electronics. Figure 1-2 illustrates the electromagnetic spectrum, highlighting the so-called “THz Gap.”

Conventional electronics cannot efficiently operate in the THz regime. In order to operate at high frequency, a device needs to be scaled to shorter dimensions in order to have higher unity gain cut-off frequency, $f_T$ and it is proportional to the saturation velocity, $v_s$ of the semiconductor channel. However, a decrease in gate length also means a decrease in the breakdown voltage and consequently the maximum voltage at which the transistor can be operated and the power gain. The breakdown voltage is proportional to the critical field, $E_c$. The Johnson figure of merit [20] for high-power, high-frequency applications is defined as the product of the critical field, $E_c$, and the saturation velocity, $v_s$. Typically an $f_T$ at least 2 times larger than the frequency to be amplified is required in order to get significant gain at that frequency. While it is only a matter of time before semiconductor devices attain an $f_T$ of 1 THz, it will be quite a bit longer before they can operate at frequencies of 1.5-2 THz. A “back-of-the-envelope” calculation indicates that a gate length between 10 and 20 nm is required to obtain an $f_T$ of 1 THz.

Quantum cascade lasers (QCLs) show promise as THz sources, achieving 50 mW of...
power at 4.3 THz [21]. It cannot be neglected that QCLs are the brightest continuous-wave sources in the 1.2-5 THz bandwidth [22]. However, the main disadvantage of QCL THz sources is that they require cryogenic cooling, limiting their utility for many applications, particularly those that require low-power or portable designs, and whether or not they can be used as an amplifier for electronic signals. It is not clear whether the epitaxial growth or device design can improve enough to allow room temperature operation, particularly to reach the lower THz regime.

A potential way to build a THz amplifier is to use a semiconductor device to modulate a cold-cathode electron source, and take advantage of the superlative transport properties of vacuum electronics. By removing the semiconductor device from the power loop and instead putting it in the control loop, it may be possible to create a high-power amplifier for THz signals.

1.2 Thesis Outline

The remainder of this thesis is organized as follows:

- In chapter two, the physics of field emission is explained. This physics is used to drive the design of the chosen field-emitter structure: a nanofabricated silicon emitter tip ballasted by a vertical ungated FET. Also, chapter two covers current state-of-the-art microfabricated field emitter structures as well as their advantages and disadvantages.

- Chapter three covers the device design and simulation of vertical ungated FETs, quantum simulations of the accumulation layer, and device simulations of individual vertical ungated FET ballasting elements (FEA-FETs).

- Chapter four discusses the fabrication of arrays of vertical ungated FETs, and FEA-FETs.

- Chapter five provides data analysis and discussion of the testing results of vertical ungated FETs.
• Finally, chapter six provides a summary of the thesis, as well as possible directions for future work.
Chapter 2

Background

The work function, \( \phi \), of a metal or semiconductor is defined as the difference between the Fermi energy and the vacuum energy, and forms a potential barrier which keeps electrons bound to the material. Electrons can overcome this barrier and be ejected from the metal or semiconductor into vacuum by two different methods - they can jump over the barrier, as in thermionic emission or photoemission, or they can tunnel through the barrier as in field emission. In the case of thermionic emission or photoemission, the electrons are either imparted with thermal energy or energy from photons so they can overcome the potential barrier into vacuum as illustrated in

![Figure 2-1](image)

**Figure 2-1:** Two methods of emission of electrons from a metal. (a) Thermionic or photo emission. (b) Field emission.
Figure 2-1a. In the case of field emission, however, the potential barrier is deformed by an applied electric field such that electrons can tunnel through this barrier into vacuum as in Figure 2-1b. To first order, this tunneling process can be modeled as a one-dimensional problem of an electron transmitting through a triangular barrier to give insight into the key dependencies of the physics involved. In this section, the vacuum level at the metal-vacuum interface ($x = 0$) is used as the energy reference.

### 2.1 Tunneling Through a Triangular Barrier

Because the barrier potential is slowly varying on the scale of the electron wavelength inside the material, the transmission probability, $T(E_x)$, through the barrier can be estimated by applying the Wentzel-Kramers-Brillouin (WKB) approximation to the work function barrier [23]. The WKB approximation allows for the description of the wavefunction away from the classical turning points, and gives reasonable results in the forbidden region. For a single electron with energy in the direction of the barrier $E_x$, the one-dimensional time-independent Schrödinger equation is:

$$E_x \psi(x) = -\frac{\hbar^2}{2m^*} \frac{d^2}{dx^2} \psi(x) + V(x) \psi(x) \quad (2.1)$$

Where $V(x)$ is the potential, and $\psi$ is the wavefunction of the electron. The tunneling distance, $W$, depends on both the energy of the electron as well as the applied electric field, $F$.

$$W(E_x) = \frac{\phi + E_F - E_x}{qF} \quad (2.2)$$

The electron traveling in the $+x$ direction can be modeled as an evanescent wave and the wave function inside of the barrier can be approximated as decaying as $\psi_0 e^{-\alpha x}$, where $\alpha$ is the decay coefficient. From this model, an expression for the fraction of the wave that is transmitted through the barrier is obtained:

$$\frac{\psi(W)}{\psi(0)} \approx e^{-\alpha W} \quad (2.3)$$
This means that the transmission probability is

\[ T(E_x) = \left| \frac{\psi(W)}{\psi(0)} \right|^2 \approx e^{-2\alpha W} \quad (2.4) \]

The WKB approximation states:

\[ T(E_x) \approx e^{-2 \int_{x_1}^{x_2} \kappa(x) \, dx} \quad (2.5) \]

Where \( x_1 \) and \( x_2 \) are the classical turning points, and \( W = x_2 - x_1 \). The \( x \)-directed wave vector inside the classically forbidden region, \( \kappa(x) \), from the Shrödinger equation, is

\[ \kappa(x) = \sqrt{2m^* [V(x) - E_x]/\hbar^2} \quad (2.6) \]

From this equation, the relation between \( \alpha \) and \( \kappa \) can be found.

\[ \alpha W = \int_{x_1}^{x_2} \kappa(x) \, dx \quad (2.7) \]

Applying the WKB approximation, then, yields

\[ T(E_x) \approx \exp \left[ -2 \int_{x_1}^{x_2} \sqrt{2m^* [V(x) - E_x]/\hbar^2} \, dx \right] \quad (2.8) \]

Where the potential difference \( V(x) - E_x = -qFx + \phi + EF - E_x \). From the potential \( V(x) = -qFx \), the limits of the classically forbidden region are \( 0 \leq x \leq \frac{\phi + EF - E_x}{qF} \), giving the limits of the integration. The resulting equation is:

\[ T(E_x) \approx \exp \left[ -2 \int_0^W \sqrt{\frac{2m^*}{\hbar^2}} \sqrt{-qFx + \phi + EF - E_x} \, dx \right] \quad (2.9) \]

The equation can be readily integrated to find:

\[ T(E_x) \approx \exp \left[ -\frac{4}{3} \sqrt{\frac{2m^*}{\hbar^2}} \frac{(\phi + EF - E_x)^{3/2}}{qF} \right] \quad (2.10) \]

Alternatively, by noting that apart from the factor of \( \sqrt{2m^*/\hbar} \), this area resembles
a triangle with base \((\phi + E_F - E_x)/qF\) and height of \(\sqrt{\phi + E_F - E_x}\), the same result can be obtained.

If the assumption that \(E_x = E_F\) is made, equation 2.10 simplifies to:

\[
T(E_x) \approx \exp \left[ -\frac{4}{3} \sqrt{\frac{2m^* \phi^{3/2}}{\hbar^2 qF}} \right]
\]  

(2.11)

Of course, electrons will be arriving at the surface at a range of different energies, so why is it valid to consider only electrons at the Fermi level? The physics of the tunneling in equation give insight into why this is valid. As the energy of the electrons is increased, the tunneling probability increases exponentially and the electrons are much more likely to participate in transmission. However, the number of electrons that are available falls off very rapidly at energies above \(E_F\), particularly at low temperatures. In metals, due to the extremely large density of states effective mass, there are effectively no electrons at energies above \(E_F\). Energies much below the Fermi level are not likely to participate in transmission until high fields are applied,

![Figure 2-2: Tunneling probability through a triangular barrier shows an exponential dependence on electric field. For this calculation, the electron has energy normal to the surface \(E_x = E_F\).](image)

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thus energies below $E_F$ may be neglected under sufficiently low electric fields.

From the above, the tunneling probability has exponential dependence on the applied electric field, $F$, as well as the barrier height, $\phi$. Assuming that the electron with $x$-directed energy $E_x$ equal to the Fermi energy, the height of the barrier is the work function, $\phi$, for n-type Si ($\sim 4.04$ eV). A simple calculation can be performed to understand the field required for significant electron emission to occur. Figure 2-2 shows the relationship of the tunneling probability to the electric field. There begins to be significant tunneling probability at roughly $2 \text{ V/nm}$ ($2 \times 10^7 \text{ V/cm}$), indicating that the width of the potential barrier must be less than approximately $2 \text{ nm}$.

A more careful calculation of the tunneling probability was performed by Fowler and Nordheim [24] with the result:

$$T = \frac{4\sqrt{E_x(\phi + E_F - E_x)}}{\phi + E_F} \exp \left[-\frac{4}{3} \sqrt{\frac{2m^*}{\hbar^2}} \frac{(\phi + E_F - E_x)^{3/2}}{qF}\right]$$ (2.12)

When considering many electrons, it is more appropriate to consider tunneling current density rather than tunneling probabilities. The tunneling current density can be expressed as the tunneling probability multiplied by the differential arrival rate (flux of electrons per unit energy) $N(E_x)$, called the supply function, and then integrated from $-\infty$ to $E_F$:

$$J_{\text{tun}} = q \int_{-\infty}^{E_F} T(F, E) \cdot N(E) \, dE$$ (2.13)

Where:

$$N(E_x) = \int v(E_x) g(E) f(E_x)$$ (2.14)

Here, $v(E_x)$ is the $x$-velocity of the electrons, $g(E)$ is the density of states (in p-space), and $f(E_x)$ is the Fermi-Dirac distribution. For a 3-D electron gas, the density of states will be:

$$g(E) = \frac{2}{\hbar^3} dp_x dp_y dp_z$$ (2.15)
and the supply function integral is:

\[
N(E_x) = \int_{p_y, p_z} \frac{p_x}{m^*} \cdot \frac{2}{\hbar^3} dp_x dp_y dp_z \cdot \frac{1}{1 + \exp\left(\frac{E_x - E_F}{k_B T}\right)} \tag{2.16}
\]

Performing a change of variables and evaluating this integral in cylindrical coordinates results in:

\[
N(E_x) = \frac{4\pi m^* k_B T}{\hbar^3} \ln \left(1 + e^{\frac{E_F - E_x}{k_B T}}\right) \tag{2.17}
\]

Putting equations 2.17 and 2.12 together into 2.13 yields an approximate expression for the tunneling current.

\[
J_{\text{tun}}(E_x) dE_x = \frac{16\pi m^* k_B T}{q} \frac{\sqrt{E_x(\phi + E_F - E_x)}}{\hbar^3(\phi + E_F)} \ln \left(1 + e^{\frac{E_F - E_x}{k_B T}}\right) \tag{2.18}
\]

\[
\cdot \exp \left[-B \frac{(\phi + E_F - E_x)^{3/2}}{qF}\right] dE_x
\]

Where

\[
B = \frac{8\pi \sqrt{2m^*}}{3h} = 6.83 \times 10^7 \text{ cm}^{-1} \cdot \text{eV}^{-1/2} \tag{2.19}
\]

At moderate temperatures, the following simplification can be made in the calculation of the supply function:

\[
k_B T \ln \left(1 + e^{\frac{E_F - E_x}{k_B T}}\right) \approx \begin{cases} 
    k_B T e^{\frac{E_F - E_x}{k_B T}}, & \text{for } E_x > E_F \\
    E_F - E_x, & \text{for } E_x \leq E_F
\end{cases} \tag{2.20a}
\]

The simplification results in the tunneling current becoming:
\[ J_{ntl}(E_x) \, dE_x = \]
\[ \frac{16\pi m^*(E_F - E_x) \sqrt{E_x(\phi + E_F - E_x)}}{h^3(\phi + E_F)} \exp \left[ -\frac{B(\phi + E_F - E_x)^{3/2}}{qF} \right] \, dE_x \]  
\[(2.21)\]

for \( E_x > E_F \), and:

\[ J_{ntl}(E_x) \, dE_x = \]
\[ \frac{16\pi m^* k_B T \sqrt{E_x(\phi + E_F - E_x)e^{(E-E_F)/k_B T}}}{h^3(\phi + E_F)} \exp \left[ -\frac{B(\phi + E_F - E_x)^{3/2}}{qF} \right] \, dE_x \]

\[(2.22)\]

for \( E_x \leq E_F \). Because this function is peaking at \( E_x = E_F \), the approximation that \( E_F - E_x \ll \phi \) may be made. In addition, by using the approximation:

\[(B/F)(\phi + E_F - E_x)^{3/2} = (B/F)\phi^{3/2}(1 + (E_F - E_x)/\phi)^{3/2} \cong (B/F)^{3/2}\phi^{1/2}(E_F - E_x)\]

\[(2.23)\]

which is valid because \((E_F - E_x)/\phi \ll 1\) and results in an integral of the form

\[-\int ye^{cy}dy.\]

The modified version of equation 2.21 shown below:

\[ J_{ntl} = q \frac{16\pi m^* \sqrt{\phi E_F}}{h^3(\phi + E_F)} \exp \left[ -\frac{\phi^{3/2}}{qF} \right] \int_{-\infty}^{E_F} \exp \left[ \frac{3}{2} B\phi^{1/2}(E_F - E_x)/qF \right] (E_F - E_x) \, dE_x \]

\[(2.24)\]

Performing the integration, we finally arrive at the Fowler-Nordheim model without image correction in 3-D:

\[ J_{ntl} = q \frac{4}{3} \frac{16\pi m^* \sqrt{\phi E_F}}{h^3 B^2(\phi + E_F)} F^2 \exp \left[ -\frac{\phi^{3/2}}{qF} \right] \]

\[(2.25)\]
2.2 Fowler-Nordheim Model

While the above sections give a simple quantum mechanical model for the tunneling current seen in a field emitter, additional considerations must be taken into account [7] for a more accurate model of field emission from a metal, degenerate semiconductor or other free electron gas.

First, the above section assumes that the charge cloud terminates abruptly at the surface of the emitter. Instead, the electron cloud extends part way into vacuum. Because of this, the potential step is not as abrupt as depicted, and a “double layer” forms, as the positively charged nuclei must stop abruptly at the surface. In addition, near the surface the electrons see an image potential due to their proximity to the conducting surface, given classically by \( V_{im} = -q^2/4x \) [25]. This modifies the potential barrier to give a total potential term of:

\[
V = -q \left[ Fx + \frac{q}{4x} \right]
\]  

Recall from Section 2.1 that the transmission coefficient, \( T(E_x) \), is dependent on the integral of the imaginary wave vector, \( \kappa = \sqrt{2m^*[V(x) - E_x]/\hbar^2} \) in the potential barrier. This new potential, while rounded at the top, is still almost triangular, with a maximum height given by \( \sqrt{\phi - yF^{1/2}} \) and a tunneling width of \( \phi/qF \). The image potential term, \( y \) can be modeled by

\[
y = \sqrt{\frac{q^3}{4\pi\epsilon_0\phi^2}} F = 3.79 \times 10^{-4} F^{1/2}/\phi
\]

for \( F \) in V/cm and \( \phi \) in eV. This corrected barrier is slightly smaller than the barrier that does not include the image potential. The ratio of the area under the original barrier to the area under the corrected barrier is close to one, and given by

\( \alpha = \sqrt{1 - y} \).

The corrected potential term is inserted into the tunneling probability expression and the integral in eq. 2.13 is computed following a similar method as was performed for the uncorrected barrier. The result is the Fowler-Nordheim equation with image
Figure 2-3: Comparison of the barrier with image charge correction (solid line) to the uncorrected barrier (dashed line)

correction [25].

\[
J = \frac{AF^2}{\phi t^2(y)} \exp \left[ -\frac{B\phi^{3/2}}{F} v(y) \right]
\] (2.28)

Where \( t^2(y) \) and \( v(y) \) are special elliptic integral functions that take into account the image charge barrier rounding effects, \( A = 1.54 \times 10^{-6} \), \( B = 6.8 \times 10^7 \) and \( y = 3.79 \times 10^{-4} F^{1/2}/\phi \) [26].

Several approximations can be made to make the problem analytically solvable. First, because the elliptical functions are slowly varying, they can be approximated as \( t^2(y) = 1.1 \) and \( v(y) = 0.95 - y^2 \) [27]. The substitutions \( J = I/\alpha \) and \( F = \beta V_G \) can also be made, where \( \alpha \) is the area of emission, \( \beta \) is the field factor, and \( V_G \) is the extraction gate voltage. With a large \( \beta \), the effective electric field will be much larger than the macroscopic electric field, and the operating voltage can be significantly reduced. With these simplifications, equation 2.28 becomes:

\[
I = \frac{\alpha A \beta^2}{1.1 \phi} \exp \left[ \frac{B(1.44 \times 10^{-7})}{\phi^{1/2}} \right] V_G^2 \exp \left[ -\frac{0.95B\phi^{3/2}}{\beta V_G} \right]
\] (2.29)

This equation can be further simplified by the introduction of the FN coefficients commonly seen in the literature [27], \( a_{FN} \) and \( b_{FN} \).
\[ a_{FN} = \frac{\alpha A \beta^2}{1.1 \phi} \exp \left[ \frac{B(1.44 \times 10^{-7})}{\phi^{1/2}} \right] \]

\[ b_{FN} = \frac{0.95 B \phi^{3/2}}{\beta} \]  

(2.30)

Making the appropriate substitutions results in a simplified version of the FN equation:

\[
I = a_{FN} V_G^2 \exp \left[ -\frac{b_{FN}}{V_G} \right]
\]

(2.31)

### 2.3 Tunneling From a Reduced-States Accumulation Layer

Depending on the geometry of the emitter and the material used to fabricate it, the assumption that the electrons are in a 3-dimensional electron gas (3DEG) may not be valid. In a non-degenerate n-type semiconductor, a sheet charge, a line charge, or a point charge may form at the field emitter, resulting in a 2-D, 1-D, or 0-D electron gas. This tight confinement of the electrons in the accumulation layer causes discrete

\[
E_c, E_f, E_x, E
\]

Figure 2-4: The formation of an accumulation layer at the semiconductor-vacuum interface leads to the creation of quantized energy levels for the quasi-bound electrons

38
Figure 2-5: Density of states in a semiconductor as a function of dimension. A “OD” system is a quantum dot, where although it is truly a three-dimensional object, there is confinement in all three dimensions. From [2]

allowed states for electrons to form, and these states do not necessarily need to be at the Fermi energy.

In this section, a tunneling model for electrons trapped in a 2DEG will be developed, though a similar method can be employed for the description of tunneling from quantum wires and quantum dots into vacuum. The main difference in the physics between all of these lower-dimensional structures is the differences that arise in the density of states calculations. Figure 2-5 shows a comparison in the density of states for a bulk material versus 2-D, 1-D, and 0-D confinement.

2.3.1 General Theory

When tunneling calculations through thin oxides are performed in standard MOS-FETs, only bound states in the resulting inversion layer need be considered due to the separation that arises from the depletion layer that forms. This separation keeps extended states from contributing to tunneling current. In an accumulation layer, however, the bulk states must be considered in addition to the quasibound states, as this separation does not exist. Thus, the total current density, $J_{tot}$ is the equal combination of the current from both the extended states and the bound states.
\[ J_{\text{tot}} = J_{\text{extended}} + J_{\text{bound}} \]  

(2.32)

Where \( J_{\text{extended}} \) is the same as \( J_{\text{tnl}} \) calculated in the previous section, with the integral taken over all of the extended states in the accumulation layer. For the calculation of \( J_{\text{bound}} \), a different approach must be taken.

From Fig. 2-6, it can be seen that there is a different curvature in the \( k_x \) direction for the electrons sitting in the valleys in the \( k_x \) direction, than those electrons in the \( k_y \) or \( k_z \) valleys. This difference in curvature can be interpreted as the electrons having different effective masses, giving rise to two “ladders” of subbands, depending on which valley the electrons reside in. The first set has a two-fold degeneracy, and a density-of-states effective mass parallel to the surface of \( m^* = m_t \). The second set has a four-fold degeneracy, and an effective mass parallel to the surface of \( m^* = \sqrt{m_tm_l} \).

To find the energy eigenvalues, the 1-D Schrödinger equation must be solved and shown to be consistent with the solutions to the Poisson equation. The Poisson equation is a boundary-value problem that relates potential, \( \phi \), to charge density and is given by:

\[
\nabla^2 \phi = -\frac{q}{\epsilon} (N_D^+ - N_A^- + p - n) \]

(2.33)

Where \( \epsilon \) is the dielectric constant, \( N_D^+ \) and \( N_A^- \) are respectively the ionized donor and acceptor concentrations, \( n \) and \( p \) are the electron and hole concentrations. Once the eigenenergies are known, using the effective masses along with the the degeneracy in the accumulation layer, the density of states in the accumulation layer can be calculated, similarly to the calculation performed in [28].

\[
\rho(E) = (\pi \hbar^2) \sum \delta_n m_{dn} H(E - E_n) \]

(2.34)

Where \( E_n \) are the various eigenenergies, \( \delta_n \) is the degeneracy of the subband, and \( m_{dn} \) is the density-of-states effective mass in each ellipse. \( H \) is the Heaviside step function (\( H(x) = 1 \) for \( x > 0 \), \( H(x) = 0 \) otherwise). Once the density of states is
Figure 2-6: The first Brillouin zone of silicon, showing the six constant-energy surfaces of the conduction band in the $<$100$>$ direction. These ellipsoidal valleys give rise to different effective masses in the direction towards the surface depending on which valley the electrons reside in. The longitudinal axis of the ellipsoid corresponds to an effective mass $m_l$, and the transverse axis corresponds to $m_t$. 
known, the number of electrons in the accumulation layer can be found by multiplying
with the Fermi-Dirac function

$$N_{inv} = \left( \frac{KT}{\pi \hbar^2} \right) \times \sum_n \delta_n m_{dn} \ln \left[ 1 + \exp \left( \frac{E_F - E_n}{KT} \right) \right] \quad (2.35)$$

When describing the tunneling current from quasibound states, it is no longer ap-
propriate to consider the flux of electrons to the surface. Instead, a better approach is
to calculate $\nu_n(E_n)$, the tunneling attempt frequency, or the number of tunneling at-
ttempts per second in the $n^{th}$ quasibound state. There are several different approaches
that may be taken, however, we will follow the approach of Rana et. al. [29], though
other methods of calculating it exist [30] [31]. This approach finds the frequency at
which electrons interact with the tunneling barrier, by finding the approximate time
for a round trip for quasi-bound electrons to travel between the two classical turning
points.

$$\nu_n(E_n) = \frac{1}{\int_0^{x_n} \sqrt{2m_x/[E_n - E_c(x)]} dx} \quad (2.36)$$

$E_n$ is the eigenenergy of the $n^{th}$ quasibound state. $x_n$ is the classical turning point
of the $n$th quasibound state, and $m_x$ is the effective mass of the valley perpendicular
to the surface. Because the rate of tunneling through the barrier is much faster than
the energy relaxation time of the quasibound state [32], the state lifetime $\tau_n(E)$ is
approximately given by the transmission rate through the barrier: $\nu_n(E_n) T(E) =
1/\tau_n(E)$. The state lifetime (half-life / ln 2) is similar to that of alpha emission from
a radioactive nucleus [33]. While these two phenomena appear quite dissimilar at
first glance, in both cases particles are trapped in a well with a single penetrable
barrier and an impenetrable barrier. In the case of Gamow decay, to model the radial
symmetry of the nucleus, the center is considered an impenetrable barrier, and the
well is modeled from 0 to the radius, $R$, with the penetrable barrier at $r = R$.

Note that in equation 2.36 $E$, rather than $E_n$ is used for the energy to calculate
the tunneling probability, to keep the equation general.

Putting this all together yields an expression for $J_{\text{bound}}$:
$J_{\text{bound}} = q \left( \frac{KT}{\pi \hbar^2} \right) \sum_n \frac{1}{\tau_n(E)} \delta_n m_{dn} \ln \left[ 1 + \exp \left( \frac{E_F - E_n}{KT} \right) \right] \quad (2.37)$

2.3.2 Linearly Varying Potential Well Approximation

As mentioned above, in order to accurately calculate the quasi-bound eigenstates of the electrons, the Schrödinger equation must be solved consistently with the Poisson Equation. This calculation is not possible to carry out analytically (numerical simulations of the eigenstates are discussed in Section ). Typically, these types of problems are solved using a variational method, however, by making several reasonable approximations, an analytical solution for a very similar quantum problem may be obtained.

To carry out this calculation, the accumulation layer is approximated as a linear potential well, and the vacuum-semiconductor interface as an infinite potential. This approximation is acceptable for regimes with a moderate applied electric field, so that significant quantum confinement occurs in the accumulation layer, and the tunneling current is small enough to be considered a perturbation. A schematic illustration of the model is shown in Figure 2-7.

To first order, the electric field inside the semiconductor under applied field $F$ in
vacuum will be $(\epsilon_{Si}/\epsilon_0)F + \rho_s$, where $\rho_s$ is any fixed charge at the surface. By defining the bottom of the potential well to be the energy reference, the potential is:

\[
V(x) = q(\epsilon_{si}/\epsilon_0)Fx \quad \text{for} \quad x \geq 0 \quad (2.38)
\]

\[
= \infty \quad \text{for} \quad x < 0 \quad (2.39)
\]

The Schrödinger equation with this potential results in an Airy equation of the form

\[
\frac{d^2\psi}{d\eta^2} - \eta \psi(\eta) = 0 \quad (2.40)
\]

where

\[
\eta = x \left( \frac{2m^*q(\epsilon_{si}/\epsilon_0)F}{\hbar^2} \right)^{1/3} - \frac{2m^*E}{\hbar^2} \left( \frac{\hbar^2}{2m^*q(\epsilon_{si}/\epsilon_0)F} \right)^{2/3} \quad (2.41)
\]

Here, the effective mass is the effective mass perpendicular to the surface ($m_\perp$). This means for the band with a degeneracy of 2, $m^* = m_l$. Conversely, for the band with a degeneracy of 4, $m^* = m_t$. The solutions to this equation are the Airy Functions $Ai(\eta)$. The zeros of the Airy function occur at $x = 0$ for $\eta_n$ approximately given by:

\[
\eta_n \approx - \left[ \frac{3\pi}{2} \left( n - \frac{1}{4} \right) \right]^{2/3}, n = 1, 2, 3, ...
\quad (2.42)
\]

The energy levels can then be calculated from:

\[
E_n \approx \left( \frac{\hbar^2}{2m^*} \right)^{1/3} \left[ \frac{3\pi q(\epsilon_{si}/\epsilon_0)F}{2} \left( n - \frac{1}{4} \right) \right]^{2/3}, n = 1, 2, 3, ...
\quad (2.43)
\]

The first zero of the Airy function is $\eta_1 = 2.338$ (exact), simplifying the equation for the first energy eigenvalues to:

\[
E_1 = 2.338 \left( \frac{(q(\epsilon_{si}/\epsilon_0)F\hbar)^2}{2m^*} \right)^{1/3}
\quad (2.44)
\]
Note that this energy calculation has to be repeated for each of the different subband “ladders”, using their different effective masses. However, only the first several energy eigenvalues need to be considered, as beyond that the energy levels are large enough that the Fermi-Dirac integral is vanishingly small.

### 2.4 Emitter Geometry and the Problem of Nano-Sharp Emitters

A very rough model for describing the geometry of a typical micro-structure field emitter is the ball in a sphere model as illustrated in Figure 2-8. While the tip is not truly a spherical ball, and the gate is not a sphere, it allows for a simple solution to the Laplace equation that allows for the electrostatics of the problem to be readily solvable in a spherical coordinate system. This gives the result of for the field enhancement factor $\beta$, whose units are typically given in cm$^{-1}$:

$$\beta \approx \frac{1}{r} \frac{d}{(d-r)} \quad (2.45)$$

Typically, $r$ is several orders of magnitude smaller than $d$ ($\sim 5$ nm compared to $\sim 200$-300 nm for an integrated gate electrode. If not integrated, $d$ may be many orders of magnitude larger), so the approximation that $d \gg r$ is valid, resulting in $\beta \sim 1/r$. This introduces an exponential dependence on tip radius into the equation, which means that without some form of negative feedback, small variations in tip radius will result in large variations in output current. It further shows that to reduce the operation voltage of the structure, tip radius should be engineered to be as small as possible.

More careful modeling of the electrostatics of microfabricated conical emitters with a proximal gate [34] [35], including finite element analysis and a semi-analytical model that places a small sphere on top of an infinite cone (the bowling pin model), suggests that $\beta$ varies with tip radius $r$ as $\beta \approx \frac{k}{r^n}$, where $k$ and $n$ are geometry dependent. Typically, $n$ is close to 0.7 and $k$ is approximately $2.5 \times 10^6$ [36], for $r$
Figure 2-8: Ball-in-sphere model for emitter structure. $d$ is the gate aperture, and $r$ is the emitter radius. Figure from [3]

given in nm, and $\beta$ in cm$^{-1}$ (and $k$ includes a conversion from nm to cm).

Examining the geometry of field emission tips fabricated out of silicon using transmission electron microscopy (TEM) imaging, as performed by Pflug [3] in Fig. 2-9, shows that the radius of the field emitters that were fabricated followed log-normal distribution, with radii ranging from 1.4-14nm. Nilsson et. al. have suggested that the field enhancement factor, $\beta$ follows a Poisson distribution [37], and through implication, that a similar distribution can be deduced for tip radius.

Because of the limits of fabrication at these small scales, it is currently impossible for a FEA to be completely uniform even across a single die, and large spatial distributions may exist across a wafer. This distribution of tip radius will result in an even larger distribution of emission currents, due to the exponential dependence on tip radius that exists in the FN tunneling model. Thus, even while some tips do have enough electric field to turn on, other tips may have enough electric field that the joule heating could lead to tip destruction [Fig. 2-10].
Field emission can be thought of as a three-step transport process, shown in figure 2-11. First, there needs to be a supply of electrons to the surface of the emitter (1). Next, the electron must tunnel through the potential barrier into vacuum (2). Finally, the electrons must be accelerated to the anode (3). For metals and n-type semiconductors, the field emitter is limited by the probability of tunneling into vacuum (2). Because the emission current has an exponential relationship to the emitter radius and there may large temporal fluctuations due to random adsorption processes, it is advantageous instead to shift the limiting process to the supply of electrons to the emitter (1). Indeed, historically, most of the research that is aimed at developing spatially and temporally uniform emitter arrays have focused on limiting the supply of electrons to the surface.

The first efforts to control the number of available carriers were to build field emitters on high-resistivity substrates [38]. The effect of adding a large resistance in series with the emission can be modeled by the load line shown in fig 2-12. Increasing
Figure 2-10: Field emitters require a certain voltage range to operate. If the voltage is too high, the tip will be destroyed by Joule heating. If the voltage is too low, no significant current will be seen.

Figure 2-11: Block diagram of the factors involved with field emission. A field emitter may be limited by either the transmission at the surface, or the flux to the surface.
emission current results in a lower voltage drop across the emitter and a lower emission current, giving rise to a negative feedback effect. This negative feedback is what is needed to give stable and uniform current emission.

Figure 2-12: Load lines of different devices connected in series with the emitters, showing the variation of emission current for different tip radii. The dashed blue line shows that even if the output resistance of the FET equaled the that of the resistor, the FET would provide more emission current.

While adding this resistance improves emitter performance, it is at the cost of operating voltage and power. A large resistor is needed to have a uniform emission current, driving up the operating voltage and resulting in a large amount of wasted power.

To address the non-idealities of the resistive element in series with the FEAs, MOSFET structures have been integrated into FEAs to control individual [39] or small groups of emitters [4] [40]. The variation of emission current is much less when a saturated MOSFET is used as a ballasting element compared to when limited by
a resistor provided that the FET output conductance \( G_{out} \ll 1/R \) as illustrated in figure 2-12. The output characteristics of a MOSFET is best modeled as a voltage controlled current source. Since the output conductance (or resistance) is essentially independent of the current value, it is possible to obtain much higher current using the MOSFET as a feedback element than when using a resistor as a feedback element. Therefore, the ballasting is more efficient when a FET is used. Figure 2-13 shows a schematic cross-section of an FEA element ballasted by a planar mosfet.

![Cross-section of an FEA with MOSFET ballasting.](image)

**Figure 2-13:** Cross-section of an FEA with MOSFET ballasting. After [4]

The drawback of using a planar MOSFET to ballast field emission arrays is that emission non-uniformity will still occur in the smaller set of emitters controlled by the same transistor. To control each individual emitter with a conventional lateral MOSFET is not advantageous because the relatively large area of the MOSFET will result in a greatly reduced packing density. Figure 2-14 gives a schematic cross-section of an emitter ballasted by a vertical ungated FET.

While it may be possible to use a vertical MOSFET [41] or JFET [42] to control the electron supply to the field emitter, ultimately these are not attractive options as
both require additional lithography steps, and the fabrication of these structures is not straight-forward.

![Diagram of field emission array](image)

**Figure 2.14:** Cross-section (a) and equivalent circuit model (b) for a field emitter ballasted by an ungated FET pillar, with voltage naming and sign conventions used throughout the remainder of this thesis. ($V_G = V_{GS} = V_{GE} + V_{DS}$)

## 2.6 Objective and Technical Approach

The objective of this work is to make a uniform and stable field emission array that does not have the drawbacks of the resistor or traditional MOSFET ballasting elements. To ensure spatial uniformity, each emitter must be individually ballasted, and the tight packing density will ensure that large emission currents can be achieved at low operating voltages.
A suitable current limiter has been recently proposed: the vertical ungated FET. This two-terminal device utilizes the fact that the velocity of carriers in silicon saturates at sufficiently high fields. Early work [43] used two contacts spaced very closely together to generate the required field for velocity saturation. In the planned devices, the contacts are spaced much further apart while the cross-sectional area remains constant, resulting in a high aspect ratio. The silicon pillars are embedded in an oxide, which passivates the surface. When a voltage is applied to the drain end, the drain electric field creates a channel electric field (longitudinal). The drain potential also depletes the surface of the silicon column at the drain end, narrowing the channel width. The channel becomes narrower as the drain potential increases, eventually resulting in pinch-off. The current saturates due to a combination of the pinch-off and the saturation of electron velocity under large electric fields. If a lower aspect ratio were used, a higher drain voltage required to pinch off the channel.

Dr. L.F. Velásquez-García recently fabricated a device consisting of an array of 1000 × 1000 emitters in 1 cm², where each field emitter is ballasted by an ungated FET with dimensions of 1 µm × 1 µm × 100 µm with tip radius of approximately 33 nm that demonstrated current saturation. The tip to tip pitch was 10 µm.

While these devices show very good stability, uniformity and prevent the destructive heating of the sharpest tips, better performance would be obtained if the emitters were spaced closer together and the tips sharper. Due to a combination of large pillar size, relatively dull tips, and lack of a proximal extraction gate, Dr. Velásquez-García’s devices required several hundred volts to operate, and over 1000 V to exhibit current saturation. By decreasing the size of the pillar, the emitters can be made nano-sharp, resulting in a large $\beta$ and low-voltage operation, combining the stability and uniformity of the devices reported in [4] with the low-voltage and high-current performance of devices reported in [3].

There are many possible advantages to scaling, including:

1. Low voltage operation (sharp emitter gives a large $\beta$)

2. Uniform current emission (both temporally and spatially)
Figure 2-15: Plot of a device that shows full ballasting. Due to the dependencies of the FN equation, if \( \ln\left(\frac{I}{V^2}\right) \) is plotted against \( V^{-1} \), the graph should be a straight line if the emission mechanism is field emission. This is known as a Fowler-Nordheim plot. This device clearly shows ballasting at large voltages.
3. Lower energy distribution (from low-voltage operation)
4. Higher current density (from higher packing density)

2.7 Vertical Ungated FET Model

The carrier flow in electronics is most generally described by the Boltzmann Transport Equation (BTE). However, for the purpose of developing a simple analytical model for the description of the operation of the ungated FET, beginning with drift-diffusion equation will suffice (although, it is important to note that the drift-diffusion equation can be derived from the BTE). For this discussion, the hole current will be neglected, as the substrate used to fabricate the ungated FET pillars is n-type, and the device is operated in the dark, so that there are no photo-generated minority carriers. The substrate is uniformly doped so that there are neither junctions nor large electron concentration gradients, so the diffusion term may also be safely neglected. The problem may be even further reduced by noting that all of the carrier flow will be along the axial direction of the pillar, resulting in a one-dimensional problem.

\[ J \approx -qn v_e \text{drift}(E) \]  
(2.46)

At low fields, the current density is proportional to the electric field through the electron mobility, \( \mu_e \).

\[ J = -qn \mu_e E \]  
(2.47)

Assuming that the pillar has a cross-sectional area, \( A \), and a length, \( L \), the total current supplied to the field-emitter may be obtained. At low voltages, the voltage drop is expected to be linear along the length of the pillar, that is \( E = -\nabla V = -dV(x)/dx \) is a constant, yielding the following expressions for the drain current, \( I_D \) and the linear resistance, \( G_{LIN} \) [Ω]:

\[ I_D = qAn \mu_e \frac{dV(x)}{dx} \approx \frac{qAn \mu_e V_{DS}}{L} \]  
(2.48)
$G_{LIN} = \frac{qA_n\mu_e}{L}$

However, at higher electric fields, the velocity of electrons begins to saturate. In silicon, the saturation velocity, $v_{sat}$ is $\approx 1 \times 10^7$ cm/s. To describe the saturation effect, no longer can a linear relationship between current density and electric field be assumed. The drift velocity must now be replaced by the following simple analytic expression:

$$v_e^{drift} = \frac{\mu_e \mathcal{E}}{\sqrt{1 + \left(\frac{\mu_e \mathcal{E}}{v_{sat}}\right)^2}}$$

(2.50)

In addition to the field-dependent mobility, the source depletion layer increases from the source to the drain end of the ungated FET, resulting in a cross-sectional area, $A(x)$, that decreases along the length of the channel. The full drain current expression is:

$$I_D = \frac{qA(x)n\mu_e}{\sqrt{1 + \left(\frac{\mu_e}{v_{sat}}\right)^2 \left(\frac{dV(x)}{dx}\right)^2}} dV(x) dx$$

(2.51)

Above a certain $V_{DS}$, the velocity of the electrons reaches $v_{sat}$, and the electron concentration in the drain end of the channel drops off substantially. Defined as $V_{DSS}$, it is at this voltage that the channel is pinched off and the current reaches its saturation value, $I_{DSS}$. Increasing $V_{DS}$ beyond this value causes the excess voltage $\Delta V_{DS} = V_{DS} - V_{DSS}$ to be dropped across the depletion region. As $\Delta V_{DS}$ is further increased, the depletion region widens, effectively shortening the length of the channel by an amount, $\Delta L$. This effect, known as channel length modulation, can be modeled as a linear increase in the drain current for $V_{DS} > V_{DSS}$. Figure 2-16 illustrates the effect of increasing $V_{DS}$ beyond $V_{DSS}$. The current in the saturation regime is thus:

$$I_D \cong I_{DSS}[1 + \lambda V_{DS}] = I_{DSS} + G_{OUT} \Delta V_{DS}$$

(2.52)

where $\lambda [V^{-1}]$ is the channel length modulation parameter and $G_{OUT} = \lambda I_{DSS}$ [6]
is the resulting output conductance. While the behavior of channel length modulation in ungated FETs is largely analogous to its behavior in standard planar MOSFETs, the channel pinch-off in the ungated vertical FET is a 3-D effect, as the extension of the depletion region varies in both orthogonal directions perpendicular to the axial direction.

![Diagram of device cross-section](image)

**Figure 2-16:** Schematic device cross-section showing the evolution of the equipotential lines and depletion width.

### 2.8 Chapter Summary

In this chapter, an analytical model for tunneling through a triangular barrier was described, giving insight into the key features that govern the operation of field emission cathodes. Then, a model to describe the effect of the semiconductor accumulation layer on the tunneling current was presented, along with several approximations to make the problem of calculating the energy eigenvalues in the accumulation layer analytically solvable. The Fowler-Nordheim model of field-emission was then explained.
Following that, the effect of the tip radius distribution was presented, highlighting the need for a compact method of controlling the supply of electrons to the emitter. Next, the state-of-the-art in methods of ballasting field emitters was detailed, along with their strengths and weaknesses.

After the discussion of current technology, the approach that was used in this thesis was explained. In general, three conditions must be met to achieve current-source behavior. These are:

- High aspect ratio
- Velocity saturation
- Channel Pinch-off

The vertical ungated FET pillar allows a passive current source to be integrated directly under each emitter, allowing for a high emitter density while still permitting large currents to be emitted. Scaling the vertical ungated FET to smaller dimensions has been shown to work via device simulations, and offers the advantage of low-voltage operation and small energy distribution while providing high current density and spatially and temporally uniform emission.
Chapter 3

Device Design and Modeling

3.1 Ungated FET Pillar Geometry Considerations

When choosing the specifications for designing the ungated FET pillar, several important figures of merit needed to be characterized: the linear conductance, $G_{LIN}$, the output conductance, $G_{OUT}$, the saturation voltage, $V_{DSS}$, and the saturation current, $I_{DSS}$.

The important performance specifications are as follows:

- To obtain large emission currents and saturate at low voltages, $G_{LIN}$ needs to be maximized.

- To minimize the variations in current density across the array in the saturation regime, $G_{OUT}$ must be as small as possible. A large output resistance also ensures good current-source behavior.

- To ensure that the emitter does not burn out, $I_{DSS}$ must be below the emitter burn-out limit. This limit is at roughly 1 µA for very sharp tips. However, $I_{DSS}$ must also not be too small, as to cause inconsequential emission current.

- Finally, for low voltage operation, $V_{DSS}$ should be minimized.

It is clear from Section 2.7 that the main controllable physical parameters are the channel length $L$, the cross-sectional area of the pillar $A$, and the doping $N_D$. 
Intuitively, it is clear that increasing the carrier concentration or the cross-sectional area of the pillar will increase the drain current, resulting in a larger $I_{DSS}$. To explore the effect that these parameters have on the performance metrics of ungated FET pillars in detail, device and process simulations were carried out for micron-sized vertical ungated FETs [44].

The simulations indicate that the main driving force for controlling the output conductance was the aspect ratio of the pillar. To illustrate this fact, the ungated FET cross-section was set at 100 nm × 100 nm, while the channel length, $L$ was varied between 1 µm and 10 µm, and the doping concentration, $N_D$ was varied between $10^{13}$ and $10^{16}$ cm$^{-3}$. Then, the output conductance, the linear conductance, the output current, and the maximum current at $V_{DS} = 10$ V were extracted. Figure 3-1 shows $I_{DSS}$, $I_{DMAX}$, $G_{LIN}$ and $G_{OUT}$ as a function of doping concentration, with the pillar dimensions held constant at 100 nm × 100 nm × 10 µm.

Next, the doping was held constant at $2 \times 10^{15}$ cm$^{-3}$, and the channel length was varied from 1 µm to 10 µm while still keeping the cross-section at 100 nm times 100 nm. The results are plotted in Figure 3-2.

From these results, it is apparent that increasing the length parameter of the FET has the effect of increasing the output resistance, preferentially to the drain resistance.

**Figure 3-1:** Drain saturation current $I_{DSS}$ and maximum current $I_{DMAX}$ (at 10 V) *(left)*. Linear conductance $G_{LIN}$ and output conductance $G_{OUT}$ *(right)* vs. doping concentration for an ungated FET with a cross-section of 100 nm × 100 nm and a length of 10 µm.
Figure 3-2: Linear conductance $G_{LIN}$ and output conductance $G_{OUT}$ (left), and saturation current $I_{DSS}$ and maximum current $I_{DMAX}$ (at 10V) (right) vs. channel length for an ungated FET with a cross-section of 100 nm $\times$ 100 nm and $N_D = 2 \times 10^{14}$.

Since they are not linear to each other, they have different functional dependancies. In addition, one can conclude that a high aspect ratio, of roughly greater than 50:1, is needed to get satisfactory current limiter operation, and that structures such as [45] most likely do not have the aspect ratio needed to effectively control the supply of electrons to the emitter.

3.2 Numerical Simulations of a Nano-Scaled Un-gated FET Pillar

Following the results of the previous section, simulations were carried out in SILVACO [46], a technology cad (TCAD) software package consisting of ATHENA, a microfabrication process simulator, and ATLAS, the semiconductor device physics simulator. The purpose of these simulations was to ensure that reducing the pillar geometry still resulted in a device that saturated. An ideal process flow was developed and run in ATHENA. The completed structure is plotted in Figure 3-3.

The structure is a 10 $\mu$m tall pillar that has a cross-sectional area of 0.01 $\mu$m$^2$ (for an aspect ratio of 100:1) was etched into an n-type silicon substrate. The donor concentration in the substrate was $5 \times 10^{15}$ cm$^{-3}$. The pillar was originally 0.32 $\mu$m
Figure 3-3: The two-dimensional structure generated in the process simulator Athena to extract the figures of merit for the nano-scale pillar wide, so to thin it to 0.1 µm, a wet thermal oxidation was performed. After the oxidation, the remaining gap between the pillars was filled with an low pressure chemical vapor deposition (LPCVD) oxide, and the surface was planarized in a polishing step. An ion implantation (dose=2.5e12 @ 50kV of phosphorus) step was performed to create an ohmic contact, and following dopant activation, a contact hole to the top of the pillar was opened and the structure was metallized with a titanium silicide and aluminum. For the input deck to generate this structure, please see Appendix C.

Once the structure was created, ATLAS was used to apply a drain to source bias and simulate the current density, among other parameters. Several interesting results
Figure 3-4: ATLAS simulation at $V_{DS} = 1$ V. In the low-field regime, the potential drop is linear along the length of the pillar. *Left*: Equipotential lines near the onset of saturation. *Right*: Potential drop along the length of the pillar. In this figure, 0 Microns is the drain end of the pillar and 10 Microns is the source end of the pillar. The average vertically-directed electric field along the length of the pillar is approximately 1000 V/cm.

are summarized in the following pages.

In Figure 3-4, the equipotential lines are plotted for $V_{DS} = 1$ V. Along side the equipotential lines, a cutline of the potential along the middle of the pillar is plotted. As was expected for a pillar with $V_{DS} < V_{DSS}$, the potential varies nearly linearly along the length of the channel. Examining the electron velocity at the drain end of the channel found that the electrons were reaching $3 \times 10^6$ cm/s, well below the saturation velocity in silicon. While this velocity is not yet saturated, between 0.5 and 10 µm the electron velocity is a factor of two lower.

As the drain to source bias is further increased, the velocity of the electrons in the drain end of the pillar will reach saturation, causing the carriers to be swept away towards the drain and forming a depletion region along the surface of the pillar, eventually pinching off the drain end of the channel. Increasing the bias beyond this point will cause the size of the depletion region to increase, shortening the length of the channel. Figure 3-5 depicts the ATLAS result for the electron velocity and
depletion region boundary for $V_{DS} = 10$ V. At this potential, the effective channel is nearly 2 $\mu$m shorter than the true pillar length, and velocity saturation is clearly occurring near the drain.

Finally, the current-voltage characteristic of the pillar was obtained, shown in figure 3-6. Raw results from ATHENA are obtained in units of A/µm, so in order to plot the data correctly, the data was multiplied by the cross-section width, 0.1 µm. From the IV characteristic, the performance metrics were extracted.

**Figure 3-5:** Electron velocity and depletion region boundary (thick red line) for a nanoscaled FET pillar with $V_{DS} = 10$ V. At this potential, the drain end of the channel is clearly pinched off, and the effective channel length is roughly 2 $\mu$m shorter than the true pillar height.
**Figure 3-6:** Simulated I-V characteristic of the nanopillar with doping $N_D = 5 \times 10^{15}$ cm$^{-3}$. Extracted parameters: $G_{LIN} = 0.212 \, \mu\Omega$, $G_{OUT} = 2.714 \, n\Omega$, $V_{DSS} = 1.42 \, V$, $I_{DSS} = 0.327 \, \mu\text{A}$

**Figure 3-7:** Simulated I-V characteristic of the nanopillar with doping $N_D = 2 \times 10^{14}$ cm$^{-3}$. Extracted parameters: $G_{LIN} = 0.011 \, \mu\Omega$, $G_{OUT} = 0.01 \, n\Omega$, $V_{DSS} = 0.11 \, V$, $I_{DSS} = 1.148 \, \text{nA}$. 

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Table 3.1 tabulates these simulation results and compares them to the $1 \, \mu m \times 1 \, \mu m \times 100 \, \mu m$ pillar to those obtained with a $100 \, nm \times 100 \, nm \times 10 \, \mu m$ pillar. These results indicate that the performance of a scaled version of the pillar can perform comparably to a pillar that takes up $100 \times$ the area and is ten times as long.

**Table 3.1:** Summary table of the comparison of micro vs. nanoscale pillar operation, at two different doping densities

<table>
<thead>
<tr>
<th></th>
<th>Micropillar</th>
<th>Nanopillar (1)</th>
<th>Nanopillar (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cross-sectional area</td>
<td>1 $\mu m^2$</td>
<td>0.01 $\mu m^2$</td>
<td>0.01 $\mu m^2$</td>
</tr>
<tr>
<td>Length</td>
<td>100 $\mu m$</td>
<td>10 $\mu m$</td>
<td>10 $\mu m$</td>
</tr>
<tr>
<td>$N_D$</td>
<td>$2.0 \times 10^{14}$ cm$^{-3}$</td>
<td>$2.0 \times 10^{14}$ cm$^{-3}$</td>
<td>$5 \times 10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>$G_{LIN}$</td>
<td>0.121 $\mu \Omega$</td>
<td>0.011 $\mu \Omega$</td>
<td>0.212 $\mu \Omega$</td>
</tr>
<tr>
<td>$G_{OUT}$</td>
<td>0.72 n$\Omega$</td>
<td>0.01 n$\Omega$</td>
<td>2.714 n$\Omega$</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>0.818 $\mu A$</td>
<td>1.148 nA</td>
<td>0.327 $\mu A$</td>
</tr>
<tr>
<td>$V_{DSS}$</td>
<td>6.75 V</td>
<td>0.11 V</td>
<td>1.42 V</td>
</tr>
<tr>
<td>$I_{DMAX}$</td>
<td>0.89 $\mu A$ @ 100 V</td>
<td>1.20 nA @ 10 V</td>
<td>0.35 $\mu A$ @ 10 V</td>
</tr>
</tbody>
</table>

### 3.3 Numerical Simulations of the FET-FEA

While the previous section detailed the use of ATLAS as a useful framework for the investigation of the device physics of the ungated FET pillar, and used ATHENA to gain some insight into the processing required to create real structures, a truly interesting use of these simulation packages is to build and simulate a coupled FET-FEA structure. If it is possible to model the classical device physics, the quantum tunneling, and the complex electrostatics (particularly field enhancement) at the same time, great insight into the interactions between the field emitter and the vertical ungated FET can be gained.

As a first step, a simple FET/FEA process flow was created and simulated in ATHENA, resulting in the structure shown in Figure 3-8. In this simulation the donor concentration was $5 \times 10^{15}$ cm$^{-3}$. to create a sharp tip ($r \approx 2$ nm) on top of the silicon pillar, a short isotropic etch to begin rough tip formation was performed continuing with the deep anisotropic etch to form the pillar. When performing the
oxidation, the time was carefully controlled to produce a sharp emitter. After the oxidation, the gaps were filled in with LPCVD oxide, and aluminum was deposited. to create a self-aligned gate, a polishing step was used to pattern the gate aperture, stopping just before the emitter tip was damaged. Finally, the oxide encasing the emitter was removed with a wet etch step.

In this process, the self-aligned aperture size is defined by the amount of oxide deposited. The structure simulated had an aperture of 240 nm, slightly larger than the width of the silicon pillar. The aperture is in plane with the emitter tip, as detailed electrostatics simulations have shown that this is the most efficient structure for emission [34].

In figure 3-9, the simulated I-V characteristic of this structure for gate voltage, $V_{GS}$, between 0 and 100 V is plotted on both a linear and semilog scale. ATLAS gives current results in units of A/micron, so to convert this to a current, the result was multiplied by the width of a pillar, 100nm. As a result of this normalization, the structure simulated is a ridge type emitter, sharp in one axis and long in the other. Because of this, The field enhancement is lower than it would be for a conical emitter. From the graphs, it is clear that at low gate voltages, the current is limited by the
tunneling through the barrier.

Figure 3-10 is a Fowler-Nordheim plot of the IV characteristic of the simulated structure. Pure Fowler-Nordheim emission is characterized by a straight line with a negative slope, as seen at voltages below 66 V $1/V = 0.015$ V$^{-1}$. Above this voltage, the curve begins to bend, with the slope eventually becoming positive. This bending over is an indication that the supply of electrons is being controlled from an external source.

From the slope and intercept of the plot, the Fowler-Nordheim parameters discussed in section 2.2 can be extracted. The slope of the curve gives a $b_{FN}$ value of 325.33, and the natural log of the intercept gives an $a_{FN}$ value of $2.73 \times 10^{-8}$. From the extracted $b_{FN}$, $\beta$ was calculated to be $1.63 \times 10^6$. Using the values of $a_{FN}$ and $\beta$, an $\alpha$ of $2.16 \times 10^{-16}$ is obtained.

To judge this simulation’s performance, a comparison to a similar, but unballasted, structure reported in [3] was conducted. While both structures were n-type silicon emitters with tip radii < 5 nm, Pflug’s structures were silicon emitters with a gate
Figure 3-10: Fowler-Nordheim plot of the simulation of the structure in Figure 3-8. Extracted parameters: $a_{FN} = 2.73 \times 10^{-8}$, $b_{FN} = 325.33$, $\alpha = 2.16 \times 10^{-16}$, $\beta = 1.63 \times 10^{6}$
Table 3.2: Device characteristics from various Silicon arrays fabricated by Pflug of size 100 μm × 100 μm[3]

<table>
<thead>
<tr>
<th>a_{FN}</th>
<th>b_{FN}</th>
<th>α</th>
<th>β</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.9 × 10^{-3}</td>
<td>203</td>
<td>1.9 × 10^{-14}</td>
<td>2.6 × 10^{6}</td>
</tr>
<tr>
<td>1.5 × 10^{-2}</td>
<td>204</td>
<td>6.2 × 10^{-11}</td>
<td>2.6 × 10^{6}</td>
</tr>
<tr>
<td>3.9 × 10^{-1}</td>
<td>228</td>
<td>1.9 × 10^{-9}</td>
<td>2.3 × 10^{6}</td>
</tr>
<tr>
<td>4.3 × 10^{-1}</td>
<td>235</td>
<td>2.3 × 10^{-9}</td>
<td>2.3 × 10^{6}</td>
</tr>
<tr>
<td>7.4 × 10^{-4}</td>
<td>193</td>
<td>2.7 × 10^{-11}</td>
<td>2.7 × 10^{6}</td>
</tr>
</tbody>
</table>

aperture of approximately 70 nm. Table 3.2 tabulates the extracted parameters from Pflug. Pflug also was testing 100 μm × 100 μm arrays of field emitters, while this simulation considered only a single emitter.

It can be seen that the β value of the simulation compares well to the experimental data presented by Pflug. The lower β value is indicative of a larger tip radius than what Pflug obtained in his experimental work. This makes some sense, as it has been shown that emission can result from roughness on the emitter surface from as few as several lattice sites. Initially surprising was the disparity in a_{FN} and α between the experimental results and the simulated structure. The difference in α can be mostly explained by the fact that the α Plug reports is not normalized by the array size. Normalizing by the array size yields an effective area of between 1.9 × 10^{-15} and 2.3 × 10^{-13}.

The difference explained by errors in the simulation, such as the quantization of the finite element mesh, as well as from the uncertainties and errors in the extraction of α from the experimental data, as averaging in the array will occur. Effective emission areas as small as 1.3 × 10^{-16} have been reported from the Fowler-Nordheim plots of single microfabricated Spindt tips [26], so the value of α obtained from the simulation is not unreasonable.

While the results presented above are promising, this work is currently ongoing. There are many places where the simulation can be improved. Because of the high doping density in the channel and large width of the FET pillar, the saturation voltage of the FET is quite large. In addition, the meshing at the tip should be finer. However,
when simulating the process flow, the meshing is at the mercy of the finite element oxidation solver. Finally, the $a_{FN}$ and $b_{FN}$ coefficients in the Fowler-Nordheim model that ATLAS uses should be modified to match experimental data.

3.4 Numerical Simulations of Accumulation Layer States and Tunneling

As explained in Section 2.3, the Schrödinger and Poisson equations must be solved numerically and self-consistently to calculate the energy eigenvalues of quasi-bound states in the accumulation layer of an n-type semiconductor under an externally applied electric field, $F$. ATLAS contains a self-consistent coupled Schrödinger-Poisson module that is able to simultaneously solve the Poisson equation for potential, and the Schrödinger equation for the electron wavefunctions and energy levels for a configurable number of eigen values. Typically in device physics modeling, this simulation module is used for the calculation of quantum effects in the channels of FETs and HEMTs (high electron mobility transistors), so its applicability to the surface of a field emitter was poorly understood.

To investigate the use of these models for the calculation of the accumulation layer states in a semiconducting field emitter, a planar metal-insulator-semiconductor (MIS) stack consisting of an n-type semiconductor substrate with doping concentration $N_D = 10^{15}$ cm$^{-3}$, a 100 μm thick vacuum layer, and an aluminum anode was created. To ensure reasonable answers, special care was taken to make sure that the finite element mesh at the vacuum-semiconductor interface was extremely dense (spacing < 1 Å). Simulations were then carried out for a series of anode-semiconductor voltages. For these simulations, all tunneling models were turned off.

Figure 3-11 shows the band structure of the conduction band, with the three lowest energy eigenvalues, for an applied electric field of $2 \times 10^7$ V/cm, typically considered the “turn-on” field for field emission. Valley #1 corresponds to the ellipsoidal conduction band minima in the $k_x$ direction ($k$-vector towards the surface) of the
**Figure 3-11:** *Left:* The lowest three energy eigenvalues for an applied field $F = 2 \times 10^7$ V/cm;  

*Right:* Band structure at the surface for an applied field $F = 2 \times 10^7$ V/cm

First Brillouin zone, whereas Valley #2 is the degenerate four valleys in the $k_y$ and $k_z$ direction, with $k$-vectors orthogonal to the surface.

Figure 3-12 plots the wavefunctions, the probability density function (PDF) of one of the wavefunctions, and the electron concentration at the surface, for the same field. The peak of the electron concentration is away from the surface of the semiconductor, as the electron concentration is being skewed by the bound states whose expected value is, as evidenced by the PDF, is shifted away from the surface by approximately 8 Å, for the first bound state. Higher order states are shifted even further away from the surface, but due to their higher energy (and thus, lower electron populations), impact the electron concentration less.

Note also that the PDF and the electron concentration are allowed to extend into the forbidden region, rather than treating the boundary as an infinite barrier. In the forbidden region, they begin to decay following a single exponential extinction curve. There is an end the simulation with a boundary placed 1.5 nm into the tunneling barrier. This boundary condition results in the probability density function to begin to roll off faster at $x = -1$ nm. At that point, however, the PDF is already eight
Figure 3-12: (a) The normalized lowest three wavefunctions for an applied field of $2 \times 10^7$ V/cm, superimposed on the band structure and offset by the energy eigenvalues. (b) The normalized probability density function of the lowest state. Note that the solver allows the wavefunction to extend into the classically forbidden region, giving more accurate results for the energy levels.
Figure 3-13: A comparison of the linear potential well model to the numerical simulations. While the lowest energy is reasonably approximated by the analytical model, quickly, the linear potential well becomes too confining compared to reality due to the conduction band bending over away from the surface.
orders of magnitude down from the peak, so that its impact on the energy level calculation is minimal.

A comparison between the first two energy eigenvalues obtained using the analytical model presented in Section 2.3.2 is compared to those obtained through the numerical simulation in Figure 3-13 for an electric field of $2 \times 10^7$ V/cm. For the purpose of this calculation, the energy reference was taken to be the bottom of the conduction band well at the surface of the semiconductor, -0.228 eV below $E_F$. For the linear potential well, the field inside the semiconductor was estimated to be $1.71 \times 10^6$ V/cm.

$E_1$ was numerically calculated to be 0.201 eV, where as the linear potential approximation estimated its energy level to be 0.258 eV. For $E_2$, simulation found a value of 0.2639 eV, and the linear potential approximation gave a value of 0.4456 eV. The main source of error for this calculation is that in an accumulation layer, the conduction band begins to bend over quite quickly, as there are many mobile carriers to compensate for the applied electric field, and the field does not penetrate very deeply into the semiconductor. In an inversion layer, however, a much larger field arises in the semiconductor, causing the linear potential approximation to fit the simulated data much better.

The results of the bound state simulations are tabulated in Table 3.3. With the energy values known, it is now possible to calculate the tunneling current contributions from the quasibound states. For this calculation, the quasibound tunneling model developed in Section 2.3 will be used. Only the first two states will be considered, as above the second state, because the 3rd state is nearly $3k_BT$ above the Fermi level and thus its population can be considered negligible. The first step to finding the tunneling current is to calculate the state lifetime $1/\tau$. Using equation 2.36, the state lifetime of the first bound state was found to be $1/\tau_1 = 4.177 \times 10^7$ s$^{-1}$. $1/\tau_2 = 1.808 \times 10^8$ s$^{-1}$. Because the lack of a closed form to describe the conduction band, the integral in equation 2.36 was performed numerically.

These results can then be plugged into the expression for $J_{\text{bound}}$ (equation 2.37), and the tunneling current density can now be obtained. $J_{\text{bound},1} = 194.1$ A/cm$^2$ and
\[ J_{\text{bound},2} = 124.3 \, \text{A/cm}^2, \text{ for } J_{\text{bound}} = 318.4 \, \text{A/cm}^2. \]

The current obtained from the Fowler-Nordheim equation with image correction is 0.78 A/cm². The reason the current from the bound states is so much larger can be attributed to the attempt frequency \( \times \) the density of states is much larger than the supply function calculated for the Fowler-Nordheim equation.

### 3.5 Chapter Summary

In this chapter, modeling of key parts of the integrated FEA-FET structure was presented. First, the dependancies of the figures-of-merit for ungated FET pillars were explored through the simulation of larger, micron-sized structures. Next, numerical simulations of a scaled version of the ungated FET pillar were carried out, and the performance of the ungated FET pillar was analyzed. Device simulations of an integrated FEA-FET showed field emission results comparable to previously recorded experimental data, opening up a new avenue with which to explore the interactions between the FEA and ballasting devices such as the ungated FET. Lastly, numerical simulations of the accumulation layer were performed to find the energy levels of quasibound states in the accumulation layer of semiconducting FEAs, and the energy levels were compared to those found using a simple analytical model. Using these quasibound energy levels, correction factors to tunneling currents were computed.
Table 3.3: Summary of bound state tunneling simulation results for different applied electric fields

<table>
<thead>
<tr>
<th>$F_{\text{vac}}$ [V/cm]</th>
<th>$6.62 \times 10^4$</th>
<th>$1.63 \times 10^6$</th>
<th>$9.94 \times 10^6$</th>
<th>$1.99 \times 10^7$</th>
<th>$4.99 \times 10^7$</th>
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</thead>
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<tr>
<td>$F_{\text{surf}}$ [V/cm]</td>
<td>$5.61 \times 10^3$</td>
<td>$1.38 \times 10^4$</td>
<td>$8.42 \times 10^5$</td>
<td>$1.69 \times 10^6$</td>
<td>$4.22 \times 10^6$</td>
</tr>
<tr>
<td>$F_{\text{vac}}/F_{\text{surf}}$</td>
<td>11.80</td>
<td>11.80</td>
<td>11.81</td>
<td>11.82</td>
<td>11.85</td>
</tr>
<tr>
<td>$\rho_{\text{interface}}$</td>
<td>$4.91 \times 10^{-11}$</td>
<td>$1.21 \times 10^{-10}$</td>
<td>$8.23 \times 10^{-9}$</td>
<td>$1.77 \times 10^{-8}$</td>
<td>$5.44 \times 10^{-8}$</td>
</tr>
<tr>
<td>$n_{\text{interface}}$</td>
<td>$3.11 \times 10^{8}$</td>
<td>$7.58 \times 10^{8}$</td>
<td>$5.14 \times 10^{10}$</td>
<td>$1.11 \times 10^{11}$</td>
<td>$3.40 \times 10^{11}$</td>
</tr>
<tr>
<td>Bottom of Well ($E_C - E_F$)</td>
<td>0.213 eV</td>
<td>0.176 eV</td>
<td>-0.124 eV</td>
<td>0.229 eV</td>
<td>-0.446 eV</td>
</tr>
<tr>
<td>Valley 1 (V1):</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td>1st bound energy</td>
<td>0.219 eV</td>
<td>0.185 eV</td>
<td>0.007 eV</td>
<td>-0.028 eV</td>
<td>-0.092 eV</td>
</tr>
<tr>
<td>2nd bound energy</td>
<td>-</td>
<td>-</td>
<td>0.069 eV</td>
<td>0.059 eV</td>
<td>0.051 eV</td>
</tr>
<tr>
<td>Valley 2 (V2):</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1st bound energy</td>
<td>-</td>
<td>-</td>
<td>0.054 eV</td>
<td>0.035 eV</td>
<td>0.003 eV</td>
</tr>
<tr>
<td>Barrier Width:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_F$</td>
<td>-</td>
<td>-</td>
<td>4.11 nm</td>
<td>1.97 nm</td>
<td>0.75 nm</td>
</tr>
<tr>
<td>1st bound state</td>
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<td>-</td>
<td>4.11 nm</td>
<td>2.02 nm</td>
<td>0.77 nm</td>
</tr>
<tr>
<td>$T(E)$:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_F$</td>
<td>-</td>
<td>-</td>
<td>$3.9 \times 10^{-14}$</td>
<td>$1.37 \times 10^{-6}$</td>
<td>$6.8 \times 10^{-3}$</td>
</tr>
<tr>
<td>1st state (V1)</td>
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<td>-</td>
<td>$4.23 \times 10^{-14}$</td>
<td>$1.18 \times 10^{-6}$</td>
<td>$6.0 \times 10^{-3}$</td>
</tr>
<tr>
<td>1st state (V2)</td>
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<td>-</td>
<td>$7.06 \times 10^{-14}$</td>
<td>$5.09 \times 10^{-6}$</td>
<td>$7.2 \times 10^{-3}$</td>
</tr>
</tbody>
</table>
Chapter 4

Fabrication of Ungated FET Pillars and FEA-FETs

In this chapter, the fabrication of large arrays of vertical ungated FET pillars is described. Large arrays are required to obtain substantial emission currents when building field emission cathodes. After initial experiments to test the limits of MTL’s processing capabilities, a feature size of 500 nm was chosen, with a pillar-to-pillar pitch of 1 µm. Each 10 mm × 10 mm die contains 9 arrays of 4 M pillars each, for a total of 36 M pillars per die.

Vias were designed to make contact to individual pillars, with different metallizations to provide a wide range of array sizes to test, from a single pillar to a full-scale 4M pillar array.

4.1 Wafer Lot One Fabrication

This section presents the fabrication of the first batch of wafers for the characterization of ungated FETs. The starting wafers were n-type phosphorus doped. Two resistivities were chosen to test the performance of the pillars at different doping concentrations: one set of wafers had a resistivity of 3-9 Ω·cm, and the other had a resistivity of 100-150 Ω·cm.

Figure 4-1 gives a schematic fabrication process flow depiction of the formation of
Figure 4-1: Process flow for the fabrication of 100 nm diameter pillars.
pillars with a diameter of 100 nm. A detailed process flow with recipes can be found in Appendix D.1.

4.1.1 Photomask Definition

The first step to creating the silicon pillars is to define a mask for the etching of the silicon. To etch 10 µm anisotropically is a challenge, when the critical feature size is as small as 500 nm. If only photoresist were used as the masking material, during the deep reactive ion etching (DRIE) step, the photoresist would completely erode, causing the mask to change shape and altering the profile as the etch advances down into the silicon. Thus, to ensure a uniform etching mask for DRIE, a thermal oxide of 3000 Å was grown to serve as a hardmask layer. The oxide was grown at 1000°C using a mixture of pyrogenic hydrogen and dry oxygen, which combine to form water vapor which increases the oxidation rate. This process is known as “wet” oxide growth. SiO₂ can also be grown using only dry oxygen, known as a “dry” oxide. Dry oxides form better Si-SiO₂ interfaces, however, the growth rate is much slower and the thickness is limited.

Figure 4-2: Patterned Photoresist dots. These dots have a diameter of 550 nm before descum.
The performance of two different photoresists were compared, Megaposit SPR 700 [47] and Shipley Ultra-i 123 [48] with an antireflective coating, Brewer Science XHRiC-16. It was found that the SPR 700 gave more consistent results, though this may in large part be due to the fact that the SPR 700 photoresist is coated and developed on an automatic wafer coating track, and the Ultra-i 123 was deposited manually on a spin coater.

Exposure was performed in a Nikon i-line stepper with a 365 nm wavelength mercury source, and the resist development was performed using LDD-26W positive resist developer. Initial resolution experiments showed that the stepper is able to resolve down to 0.4 µm features, but the repeatability was poor, and the structure was very rough.

Still, due to the dense, small feature size, the pattern was found to be very sensitive to environmental and exposure conditions. Care had to be taken to ensure that the humidity when doing photolithography was not above 40%. Every time new wafers were fabricated, it was imperative to check the structure of the resist after development. If the dots were too overexposed, during column formation the pillars would be destroyed. Conversely, if the dots were underexposed, the etch would terminate before reaching the desired depth.

4.1.2 Hard Mask Etching

Once the photoresist was patterned with the dots to define the columns, the next step was to pattern the SiO$_2$ hard mask. The reactive ion etching (RIE) was performed using an Applied Materials P5000 etcher using CF$_4$/CHF$_3$/Ar chemistry. The CF$_4$ is the primary reacting species, decomposing to create F$^-$ ions which attack the SiO$_2$. The CHF$_3$ content forms a polymer on the sidewalls of the oxide as it is being etched, improving the anisotropy.

Before the etching began, a 15 second O$_2$ plasma etch was performed. This etch, called a “descum” etch, helps with the uniformity of the photoresist dots and ensures that any remaining thin layers of resist are gone before the oxide etch begins. While this step does erode the resist, the benefits gained by smoothing out the resist features
To further help with the uniformity of the etch mask, a 50% over-etch of the oxide was performed. This over-etch, while it slightly decreased the diameter of the oxide dots, helped to make them more round. Experiments showed that etching reduced the diameter of the dots from 540 nm to 518 nm.

### 4.1.3 Deep Reactive Ion Etching

After the hard mask was patterned, a deep reactive ion etch (DRIE) was performed in a Surface Technology Systems (STS) etcher. Etches to create pillars 8-10 µm were performed. To attain high etch aspect ratios (20:1), DRIE uses a method known as the Bosch process to etch into the silicon. In the Bosch process, two etching steps are time-multiplexed. The first step consists of a nearly isotropic etch using SF\(_6\). The second step uses C\(_4\)F\(_8\), which form a passivation layer on the surface of the sidewalls, with similar characteristics to Teflon. Because of this multiplexing, sidewalls that have been etched with DRIE have a characteristic “scalloped” shape.

The etch rate is extremely sensitive the amount of area on the wafer to etch. The original mask to decide on which feature sizes to build the device mask was
a clearfield mask, meaning the majority of the wafer was etched during this step resulting in exposed pillars. The final mask design used a darkfield mask, where the majority of the wafer was protected by photoresist and oxide, and only areas in between pillars were etched because a planar substrate is necessary for the testing of the ungated FETs. This had the effect of increasing the etch rate, so new recipes needed to be developed in order to form pillars with desirable characteristics.

To develop the recipe, a design of experiments (DOE) approach was taken, looking at variable parameters with three possible choices. The three things to change were the passivation time, the etch:passivation time ratio, and the pressure at which the etch was performed. To judge the performance of the etch, the diameter of the pillars at the top and bottom where characterized, as well as the height and depth of the scalloping at the top of the pillar, where it is most severe. It was found that

![Figure 4-4](image-url)

Figure 4-4: Cross-section of DRIE etch to form the pillars. The scalloping of the walls of the pillars is a characteristic of the Bosch process used in DRIE. The height of these pillars shown is 10 µm with a width of 380 nm. The actual height of the pillars used for devices was approximately 8 µm.
Figure 4-5: Cross-section detail of the top of the pillars after DRIE. Etch Parameters: 6s C$_4$F$_8$ passivation cycle @ 40 sccm, 5s SF$_6$ etch cycle @ 105 sccm, 600 Watts RF (passivation), 800 Watts RF (etch), 120 Watts bias power, passivate first. Constant pressure 25 mTorr

by decreasing the etch:passivation time to less than one, using short cycle times, and keeping the pressure during the etch near the middle of the range at 25 mTorr resulted in the best etch characteristics. Figures 4-4 and 4-5 show the pillar structure after this etch.

Original experiments to test the feasibility of the structure were performed creating pillars with a depth of 8 µm, without issue. When fabricating the wafers to build testable FETs, a 10 µm etch with very good characteristics was performed. Subsequent processing require an RCA clean, a wet processing step. After the RCA clean, it was discovered that the pillars were pliable enough that during the wet processing, they were able to bend the 0.5 µm between them and static friction would hold them together. To prevent this problem, a series of experiments varying the pillar length was performed to find the longest length where this would not occur. It was found pillars that are 8 µm tall have a very low incidence rate of pillars touching, so we decided to use 8µm tall pillars to for vertical ungated FETs. In order to attain an aspect ratio of 50:1, a pillar diameter of 160 nm is needed.
4.1.4 Oxidation Thinning

The etched pillars were then stripped of their photoresist in an O\textsubscript{2} plasma, and a dip in concentrated hydrofluoric acid (50\% HF) was performed to strip the hardmask. After an RCA clean, the wafers underwent dry oxidation to remove between 150 and 200 nm of material. In addition to reducing the diameter of the pillars and decreasing the gap between them, the oxidation passivates the surface of the pillar, resulting in low interfacial charge density, and the slower oxidation rate was beneficial to control the amount of silicon consumed during the oxidation.

Process simulations in ATHENA were performed to guide the oxidation process to ensure that the correct amount of oxide was grown. Too little oxidation, and the pillars would be too large to effectively limit current. If they were over-oxidized, part of the pillars could be completely consumed, resulting in no connection between the source and the drain of the FET. Simulations indicated that an oxidation time of 5 hours and 30 minutes at 1000° C to grow 1500 Å of oxide and result in a pillar with the thinnest point 100 nm in diameter.

After the oxidation, one wafer had its oxide stripped to examine the diameter of the pillars. It was found that the pillars were intact, with a minimum dimension at

![Figure 4-6: Pillars after oxidation.](image)

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4.1.5 Gap Filling

First, a coating of low temperate oxide (LTO) was deposited to further decrease the gap between the pillars. LTO is an LPCVD deposited oxide film with good conformality, deposited at 530°C. 350 nm of LTO was deposited, and verified using ellipsometry on a dummy wafer. However, upon inspection in the SEM, it was found that only 100 nm of oxide was on the sidewalls.

After the LTO deposition, the remaining gaps between the pillars needed to be filled to make top contact to the devices. Several different materials were explored:

- Filling the remaining gaps with LTO.
- Filling the remaining gaps with low-stress vertical tube reactor (VTR) silicon nitride.
- Filling the remaining gaps with undoped polycrystalline silicon (poly-Si).

Figure 4-7: Cross-section of pillars after oxidation with oxide stripped. The diameter at the thinnest part of the scallop is just under 100 nm. The pillar widened to 150 nm at the base.

the top of the pillar of 93 nm. The pillars tapered out to 150 nm at the base.
Figure 4-8: After 350nm of LTO was deposited. Large gaps are visible between the pillars, indicating that the sidewall coverage rate was much lower than the planar coverage rate.

Figure 4-9: The different methods explored for filling the remaining gaps
LTO is a good dielectric, but the deposition did not have the conformality required. After depositing another 650 nm of LTO the wafer was cross-sectioned. Upon examination, it was found that there were large voids just underneath the surface. During via opening, these voids could be exposed, possibly resulting in metallization along the length of the column and negatively impacting performance.

Low-stress silicon-rich nitride deposited in a vertical tube reactor (VTR nitride) showed good, conformal coverage, but proved difficult to process afterwards. Several planar dummy wafers that accompanied the pillar-bearing wafers and were used for experiments in opening vias. These experiments used several different recipes in two different etch tools, the LAM 490b and the AME P5000, and none of the tools were able to effectively open vias before the resist eroded. A final attempt was made to thin the VTR nitride using a hot phosphoric acid bath, but that was found to make the wafer surface too rough to do photolithography on afterwards.

LPCVD deposition of 1 µm of undoped polycrystalline silicon (poly-Si) gave good coverage, and was able to be planarized after, making it the best choice of

**Figure 4-10:** Cross-section SEM after the poly-Si fill revealed conformal coverage.
the materials available at MTL. Ellipsometry was performed on dummy wafers to ensure the correct thickness. Cross-sectioning SEMs made it clear that the filling was complete to the bottom of the pillar. There was a small region where the deposition between two adjacent pillars meets diagonally that did not fuse, but there was no obvious cracking present.

4.1.6 Planarization

To planarize the structure and remove all of the poly-Si on the surface to ensure that the pillars were not shorted together, a three-step process was performed:

- oxidation of part of the thickness of the poly-Si on the surface
- removal of the grown oxide in HF
- oxidation to consume the remainder of the poly-Si

The reason for the multiple steps is three-fold. It would be a high temperature, long oxidation process to consume all of the poly-Si in one step. By breaking it up into two steps, the time required for the oxidation is decreased. Secondly, by removing a portion of the oxide, the aspect ratio required for the via is decreased. Finally, These steps result in a surface smoother than if the poly-Si was just oxidized.

The first oxidation was a growth of 1.36 $\mu$m performed at 1000$^\circ$ C, consuming 0.75 $\mu$m of the poly-Si. After the first oxidation, a dip in HF was performed to strip the oxide grown and expose the remaining poly-Si on the surface. Then, a second oxidation was performed at 1000$^\circ$ C that would consume 0.5 $\mu$m of poly-Si. This is enough to consume the remaining poly, plus an extra 50% to make sure that there was no remaining film at the surface to join pillars together.

Figure 4-11 shows atomic force microscope images of the surface in the four different states: the poly-Si as deposited, after the first oxidation, after the first oxide was stripped, and after the final oxidation. After each step, the roughness of the film decreased. The film began with an RMS roughness of 60 nm, and ended with an RMS roughness of 32 nm.
Figure 4-11: AFM analysis of the surface after each step of the planarization process.
4.1.7 Via Opening

With all of the polysilicon on the surface consumed, the next step was to open contact windows to the pillars. First, 1 µm of resist was spun on the wafer and patterned to define the areas that would be opened. Care was taken to perform precise alignment of the via openings to the pillars, however, there still may be up to 100 nm of error in the alignment process. To ensure that the contacts opened up to pillars, the via windows were exposed so that they were 0.6 µm in diameter.

The contact windows were then etched in the AME P5000 RIE, using the same chemistry that was used to pattern the hard mask. Figure 4-12 shows a cross-sectional SEM of the columns after the via windows were opened. It is clear from the SEM that while there was a slight misalignment, the pillar is clearly visible in the via. An unfortunate consequence of the misalignment is that the undoped poly-Si is no longer protected by oxide.

![Figure 4-12: SEM cross-section to verify that vias open to columns](image)

Figure 4-12: SEM cross-section to verify that vias open to columns
4.1.8 Metallization and Contact Formation

After the via windows were opened, a metal stack of 2000Å n$^+$ poly-Si / 1000Å TiN / 10kÅ Al was deposited to connect to the pillars and would form the basis for metal pads for probing and testing arrays of pillars in parallel. The purpose of the n$^+$ poly-Si is to increase the doping density at the drain end of the channel in order to make good contact to the metallization. Four-point probe measurements on the poly yielded a doping density of $N_D$ cm$^{-3}$. After the poly-Si deposition, a dopant activation anneal was performed at 950$^\circ$ C under a nitrogen ambient. The rest of the metal stack was then deposited using a physical vapor deposition (PVD) process. The TiN is there to act as a barrier metal for the aluminum, which when annealed could “spike” into the pillar and cause it to not operate as intended.

The metal was then patterned using contact photolithography and the Rainbow, a metal etcher in ICL. Following the metal etching, the resist was stripped through ashing. The final step of processing the wafers was to sinter the metallization. Sintering took place at 400$^\circ$ C under forming gas, a 20:1 mixture of N$_2$ and H$_2$. The

Figure 4-13: Optical micrograph of a completed array with different sized sub-arrays for testing.
reducing atmosphere prevents further oxidation of the aluminum during heating, and could help reduce any interfacial oxide between the metal and the semiconductor. In addition, the partial pressure of hydrogen passivates interfacial trap states [49].

A micrograph of a completed array is shown in Figure 4-13. The testing results from this run can be found in section 5.2.1

4.2 Wafer Lot Two Fabrication

The characterization of the first lot of wafers with FET pillars revealed several non-idealities that needed to be addressed. First, contact to the poly-Si around the pillar led to some anomalous effects that were unexpected. Second, after testing the wafer, the contacts were found to have Schottky barrier behavior, most likely due to the fact that the n\(^+\) poly was not doped enough. To address these problems, a second lot of wafers were fabricated with the following changes.

![Process flow for the fabrication of the second lot of pillars.]

**Figure 4-14:** Process flow for the fabrication of the second lot of pillars.

The differences in the processing of the second lot of wafers includes thicker LTO
so that the undoped poly-Si was not contacted and ion implantation was used to create ohmic contacts, and is highlighted in Figure 4-14. A detailed process flow can be found in Appendix D.2.

4.2.1 Gap Filling

In this batch, the amount of LTO used was doubled to close the gaps between the pillars in the orthogonal directions, resulting in a much smaller chance to contact the undoped poly-Si filling material. Nominally, 650 nm of LTO was deposited. As can be seen in figure 4-15, the remaining gaps between the pillars is approximately a 390 nm circle in the center of four neighboring pillars.

Figure 4-15: In the second batch of wafers, enough LTO was deposited to fill the orthogonal gaps between pillars, allows for contact to be made to the pillars while avoiding the poly-Si.
4.2.2 Ion Implantation Contact Formation

After the via windows were opened, the wafers were sent for ion implantation at Innovion [50], an external vendor based in San Jose, CA. The implant was a $3 \times 10^{15}$ cm$^{-2}$ does of arsenic with an energy of 30 kV and a 7$^\circ$ tilt from normal. Simulation of the implant in ATHENA indicated a doping concentration at the surface after annealing of $3 \times 10^{19}$ cm$^{-3}$, more than enough to create an ohmic contact. By tilting the angle at which the ions arrive limits the range that they travel in the silicon, due to the anisotropy of silicon’s crystal lattice. Following the implant, an anneal was performed to activate the dopants for 12 minutes at 950$^\circ$ C in an N$_2$ ambient.

The implantation made it so there was no need to deposit poly-Si, so just the TiN barrier metal and the Al metal were deposited after wafer cleaning and HF dip to remove any native oxide that had formed. As before, the metallization was patterned using contact lithography and dry etching, then sintered at 400$^\circ$ C under forming gas to reduce the contact.

4.3 FEA-FET fabrication

FEA-FET fabrication processing steps are almost identical to the beginning of the vertical ungated FET processing steps, with a couple of modifications. Before the pillars are etched in DRIE, a tip must begin to be formed at the top of the pillar, and during the oxidation to reduce the width of the pillar, the oxidation must be precisely controlled to sharpen the tip at the same time.

4.3.1 Rough Tip Formation

The first place that the fabrication of FEA-FETs differs from the fabrication of vertical ungated FETs is the need to form silicon emitter tips on the top of each pillar. To begin this process, an isotropic plasma etch was performed using the LAM 490B plasma etcher. SF$_6$ was used as the etching gas, with a partial pressure of O$_2$, which is used to control the horizontal etch rate using the process developed by Chen [51].
The etch parameters used were a pressure of 300 mTorr, an RF power of 130 Watts, and gas flow rates of 190 sccm SF$_6$ and 10 sccm O$_2$.

In the rough tip formation process, the goal is to get an isotropic undercut etch with a long neck. This long neck, when sharpened yields a high aspect ratio cone, and will give better field enhancement performance than a cone that has a larger vertex angle and lower aspect ratio.

![Figure 4-16: Cross-section of rough tip formation using a plasma etcher.](image)

When designing this process, process simulations guided the requirement on the rough tip diameter to ensure it was compatible with the diameter of the FET pillar. If the rough tip were too sharp, the pillar would be too large a diameter and would not effectively limit current. If the neck of the etch were too large, it would be difficult to oxidize it completely without destroying the pillar. It was found that with a pillar diameter of 400 nm, obtained from previous DRIE experiments, the rough tip would have to be between 150 nm and 300 nm to get a pillar aspect ratio of higher than 50:1, and still have at least 100 nm diameter pillar left after the oxidation. Figure 4-16 shows a cross-sectional SEM after rough tip formation.

After the rough tip formation, the wafers then went through the DRIE step detailed in section 4.1.3.
4.3.2 Oxidation Sharpening and Removal

To create nano-sharp tips, the oxidation is the most critical step in the process. Both over-oxidation and under-oxidation will cause a tip to blunt.

![Post-DRIE](image1)

![Post-oxidation](image2)

**Figure 4-17:** SEM cross sections of the array post-DRIE, and the structure after oxidation sharpening

The final step to preparing the FEA-FET device for testing is to perform an HF dip to remove the grown oxide and examine the sharpness of the tips.

4.4 Chapter Summary

In this chapter, the fabrication of vertical ungated FETs and FEA-FETs without proximal gates was shown, however, there are still many ways that they can be improved. Here are several of them:

- It is likely that the DRIE step can be further optimized to obtain sidewalls with less roughness. Particularly in the SEM taken of the pillars after the oxide was stripped, it is apparent that there is significant sidewall roughness.

- While the poly-Si filling process was shown to work, not having a real dielectric to fill the voids is a definite area that needs to be addressed. It may be that processes such as atomic layer deposition (ALD) or novel next-generation processes [52] may hold the key to address this issue.
• For the planarization, rather than the double oxidations, chemical-mechanical polishing (CMP) of the filled layers should be explored. Initial experiments with the new G&P Poli-400L installed in ICL have shown promise, both in terms of uniformity and repeatability.

• During ion implantation, a thin screen oxide should have been used. It would have protected the silicon surface from any sputtering damage that may have occurred from the high energy ion bombardment. In addition, during the anneal step, it would have prevented dopant species from out-diffusing into the environment. While As atoms are relatively slow diffusers, it is still a concern. Instead of using a screen oxide, it may be possible to implant before opening the via windows.
Chapter 5

IV Characterization

5.1 Measurement Setup

Once the samples were prepared, current-voltage characterization (IV) were performed on the Ungated FETs. Measurement took place in the dark using an Agilent 4156C precision semiconductor parameter analyzer. Different sizes of arrays were measured, and the figures of merit, $I_{DSS}$, $V_{DSS}$, $G_{LIN}$, and $G_{OUT}$ were extracted from the output characteristics.

To extract the linear conductance $G_{LIN}$, the slope of the first few data points of the output characteristic in the linear regime was taken. Likewise, to extract the output conductance $G_{OUT}$, a line was fit to output characteristic in the saturation regime. The intersection of these two curves gave an approximate value for $V_{DSS}$ and $I_{DSS}$.

5.2 Lot One Data

5.2.1 Testing of Arrays

Figure 5-1 shows a typical output characteristic of a single FET pillar from the first lot. When a $V_{DS}$ greater than 1 V is applied, the I-V characteristic begins to bend upwards. To approximate the output conductance for these characteristics, where
there is no clear linear trend, the slope of the output was taken from $V_{DS} \approx V_{DSS}$ to $V_{DS} = 1$ V.

![Graph showing drain voltage vs. drain current](image)

**Figure 5-1**: A single FET from a wafer with resistivity 3-9 Ω-cm. The current never shows saturation.

It is believed that the inadvertent contact made between the doped poly-silicon deposited in the via and the undoped poly-silicon deposited earlier to fill the gap between the pillars led to the formation of an effective metal-oxide-semiconductor (MOS) structure, which resulted in a parasitic MOSFET that is in parallel with the ungated FET. This poly-Si acts as a gate, forming an accumulation region at the surface of the FET. The gate effect is verified by plotting the $\sqrt{I_D}$ vs. $V_{DS}$, which forms a straight line beyond the linear regime ($V_{DS} > V_{DSS}$), showing that this output follows a square-law dependence. Gate modulation in a planar MOSFET follows the same dependence, with $I_D \sim V_{GS}^2$. 

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In larger arrays, such as the array of 2500 pillars shown in 5-2, the current does show some saturation, with an output conductance of $2.95 \times 10^{-8}$ S, nearly an order of magnitude lower than the conductance in the linear regime.

![Figure 5-2: 2500 Pillars](image)

The even larger arrays, such as the in the output characteristics shown in Figures 5-3 and 5-4 show poor current saturation.

A different way of visualizing the variation in devices is to plot the I-V characteristics normalized by the number of pillars, shown in Figure 5-5. Here, huge variation on how the pillars behave when in the linear regime can be seen. Possible because of the poor contact, the larger arrays have a much smaller normalized linear conductance around $V_{DS} = 0$ V than the single devices and small arrays. Then, several of the arrays, particularly those with 20,000 and 40,000 elements have currents much higher than just simple scaling of single devices.

A summary of these results is shown in table 5.1. In general, there was wide variation in the device parameters, with $V_{DSS}$ ranging from 0.076 V to over 4 V.
Figure 5-3: 14,400 Pillars

Figure 5-4: 40,000 Pillars
Figure 5-5: IV characteristics of lot 1 normalized by the number of pillars

Table 5.1: Summary of representative data taken from lot 1.

<table>
<thead>
<tr>
<th>Device Designation</th>
<th># Cols</th>
<th>$I_{DSS}$ [A]</th>
<th>$V_{DSS}$ [V]</th>
<th>$G_{LIN}$ [S]</th>
<th>$G_{OUT}$ [S]</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1_W1_D54_1_2</td>
<td>1</td>
<td>5.02E-11</td>
<td>0.076</td>
<td>6.71E-10</td>
<td>1.25E-10</td>
</tr>
<tr>
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<td>0.11</td>
<td>2.08E-10</td>
<td>5.97E-11</td>
</tr>
<tr>
<td>L1_W1_D54_1_4</td>
<td>2</td>
<td>8.10E-11</td>
<td>0.13</td>
<td>7.00E-10</td>
<td>2.14E-10</td>
</tr>
<tr>
<td>L1_W1_D45_1_24</td>
<td>2500</td>
<td>1.10E-07</td>
<td>0.78</td>
<td>1.56E-07</td>
<td>2.95E-08</td>
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<tr>
<td>L1_W1_D46_3_46</td>
<td>14,400</td>
<td>8.24E-06</td>
<td>4.82</td>
<td>1.94E-06</td>
<td>5.79E-07</td>
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<tr>
<td>L1_W1_D46_3_31</td>
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<td>2.66E-05</td>
<td>3.32</td>
<td>8.54E-06</td>
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<td>L1_W1_D54_1_1</td>
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<td>4.41E-05</td>
<td>5.79</td>
<td>8.09E-06</td>
<td>2.39E-06</td>
</tr>
</tbody>
</table>
5.2.2 Process Characterization

To extract the contact resistance, transfer length method (TLM) structures were included on the wafers. TLM is a widely implemented method for determining the contact resistance to semiconductors, and has been extensively studied [53]. These structures consist of long contacts of different spacings. The spacing between the contacts must be much less than their width, so that the charge spreading in the semiconductor does not occur. It is also possible to perform a mesa etch to limit carrier flow in one direction, but that would have involved additional masks and processing steps.

By plotting the resistance versus length, the resistance can be interpolated back to the resistance at a length of 0. This resistance is twice the contact resistance, $2R_c$. To then convert this number to the specific contact resistance $\rho_c$, the contact resistance is divided by the contact area $\rho_c = R_c/A_c$.

Figure 5-6 shows the raw TLM I-V characteristics for a wafer with resistivity 100-150 Ω·cm. From this data, it can be seen that there I-V characteristics are very non-linear. In addition, there is some current rectification. The non-linearity is indicative of poor contact, and the rectification indicates that the metal-semiconductor interface is forming a Schottky junction.

The TLM data of a wafer with a resistivity of 3-9 Ω·cm showed slightly improved performance. While there was more symmetry in the IV characteristics, they were still very non-linear.

From these results, it was clear that better contact to the semiconductor needed to be made. Thus, for the second lot of devices, ion implantation was explored.

5.3 Lot Two Data

5.3.1 Testing of Arrays

After the second lot of wafers were completed, I-V characterization was conducted. It was clear that these devices showed better saturation performance than the previous
Figure 5-6: Raw TLM data showing asymmetric Schottky barrier operation.

Figure 5-7: Raw TLM data showing better symmetry, but still large amounts of non-linearity

Figure 5-8 shows a comparison of the output characteristics of three different single vertical ungated FETs.
Figure 5-8: Various Single FETs across the wafer showing process non-uniformity. Most of this non-uniformity can be attributed to pillar diameter variation.

There is nearly a factor of 2 variation in the saturation current of these devices. This can be explained by non-uniformities in the processing, particularly by variations in the pillar diameter.

There were some ungated FETs that displayed different I-V characteristics. Figure 5-9 is a representative example of these devices, with a shifted I-V characteristic. In this characteristic, the FET does not begin to turn on until 0.3 V, with saturation occurring at approximate $V_{DS} = 0.85$ V.

As $V_{DS}$ was taken to higher voltages, the ungated FETs began to show signs of breaking down at approximately 4.5 V. The I-V characteristic shown in figure 5-10 illustrates this effect. While the exact breakdown mechanism is unknown, it is expected that either band-to-band tunneling (where electrons in the valence band can tunnel to the conduction band) or electron impact ionization (where collisions with phonons cause carrier multiplication) is occurring. Simulations of impact ionization show it beginning to occur at $V_{DS} = 7$ V.
**Figure 5-9:** Shifted I-V characteristic of a single FET.

**Figure 5-10:** 4 Pillars
Larger arrays, such as the one whose I-V characteristic is shown in Figure 5-11, show a "double-humped" output characteristic, with the current beginning to saturate, then going to a higher current at higher $V_{DS}$. This can be explained by looking at Figures 5-8 and 5-9. If some percentage of the pillars have an output characteristic similar to one shown in Figure 5-8, and some have output characteristics like one shown in Figure 5-9, when examining the entire array, an output characteristic resembling 5-11 results.

![Graph showing I-V characteristic](image)

**Figure 5-11:** 125k Pillars

Another interesting aspect of the output characteristic seen in figure 5-11 is the negative resistance in the saturation regime. This may be due to joule heating changing the mobility at higher voltages. These larger arrays also show increased resilience to breakdown, being able to be biased at over 20 V before a rapid increase in current is seen.

Surprisingly, as the arrays get larger, the "double hump" characteristic becomes less pronounced, and arrays larger than 1 million pillars do not show the effect at all. We speculate that the shifted I-V characteristic is also due to a contact issue.
As the arrays of pillars get larger, the via pattern gets denser. The denser via pattern may have resulted in slightly larger vias due to standing wave effects during photolithography to pattern the contact windows.

Figure 5-12 shows a typical output characteristic for an array of 4 million FETs.

![Figure 5-12: 4M Pillars](image)

### 5.3.2 Process Characterization

Again with these wafers, TLM measurements were performed. It was found that the IV characteristics of the TLM structures were linear. In this plot, only the smallest four lengths are shown. For lengths beyond $L = 60 \ \mu\text{m}$, the resistance began to asymptotically approach a value. This behavior is indicative of current spreading in the semiconductor becoming significant and effecting the resistance measurement.

Four different TLM structures on adjacent dies were measured. Plotting the resistance vs. length results in the plot shown in Figure 5-13. By following the previous method outlined, a specific contact resistance of $3.31 \times 10^{-3} \ \Omega \cdot \text{cm}^2$ is obtained. Typ-
ically, for “good” contacts, a specific contact resistance of less than $10^{-5} \ \Omega \cdot \text{cm}^2$ is required. There are several possible reasons for the high specific contact resistance. Particularly, during ion implantation, a screen oxide was not used. The screen oxide protects the silicon surface from sputter damage from the high-energy ions that are incident on the surface. In addition, during the annealing step, it is possible for dopants to out-diffuse into the ambient, lowering the doping and increasing the contact resistance. The screen oxide would have acted as a diffusion barrier to prevent this out-diffusion.

Next, the resistivity (and through inference, the doping density) was extracted. From the TLM measurements, the sheet resistance, $R_{\text{sh}}$, can be estimated as $R_{\text{sh}} = \rho_c / L_T^2 = 122 \ \Omega / \square$, or a resistivity of $7.93 \ \Omega \cdot \text{cm}$. The doping concentration is found to be $N_D = 5.6 \times 10^{14} \ \text{cm}^{-3}$. This agrees quite well to the doping concentration obtained from 4-point probe measurements. the doping density of this wafer was found to be $6.5 \times 10^{14} \ \text{cm}^{-3}$ was obtained.

Figure 5-13: TLM data used to extract specific contact resistance $\rho_c$ and transfer length $L_T$.
5.3.3 Analysis of Data

A summary of the device parameters for representative devices of this lot is shown in table 5.2. To compare the performance of the different arrays, $I_{DSS}$, $G_{LIN}$, and $G_{OUT}$ were normalized by the number of pillars, and are tabulated in Table 5.3.

In general, these devices behaved quite differently from what simulation predicted. Table 5.4 compares the simulated results to the measured results. Two different simulations are reported. The Sim (rectangular) result is device parameters from a 2-D device cross-section simulation. The Sim (cylindrical) is from a device simulation where half of a FET is simulated using cylindrical symmetry. The cylindrically symmetric simulation saturates at a lower $V_{DS}$ and has an $I_{DSS}$ that is almost an order of magnitude lower than the 2-D cross-section simulation. This makes intuitive sense, as the cylindrically symmetric simulation pinches off from all directions, whereas the 2-D cross-section simulation only pinches off from the left and the right sides.

The most striking difference is that the output current of the measured devices is orders of magnitude lower than the simulation results. There are several causes for this effect. Table 5.3 includes the calculation of effective mobility $\mu_{eff}$, calculated

<table>
<thead>
<tr>
<th>Device Designation</th>
<th># Cols</th>
<th>$I_{DSS}$ [A]</th>
<th>$V_{DSS}$ [V]</th>
<th>$G_{LIN}$ [S]</th>
<th>$G_{OUT}$ [S]</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2_W1_D6_3_52</td>
<td>1</td>
<td>7.50E-13</td>
<td>0.08</td>
<td>9.42E-12</td>
<td>2.47E-12</td>
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<tr>
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Table 5.3: Data from table 5.2, normalized by the number of pillars in the array. In addition, the effective mobility $\mu_{eff}$ was calculated from the linear conductance. Dash indicates there was a negative saturation resistance.

<table>
<thead>
<tr>
<th>Device</th>
<th># Cols</th>
<th>$I_{DSS}$ [A]</th>
<th>$G_{LIN}$ [S]</th>
<th>$G_{OUT}$ [S]</th>
<th>$\mu_{eff}$ [cm$^2$/V·s]</th>
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<td>9.98E-11</td>
<td>6.50E-15</td>
<td>39.64</td>
</tr>
</tbody>
</table>

from:

$$\mu_{eff} = \frac{G_{LIN}L}{qAN_D}$$ (5.1)

Where, a length of 10 μm, a cross-sectional area of $\pi(50\text{nm})^2$, and a doping density of $2 \times 10^{14}$ was assumed. The extremely low effective mobility indicates that it is likely that the effective doping density in the pillars is much lower than expected, or that the cross-sectional area is smaller than expected. This could be a result of non-uniformities in the oxidation thinning process, resulting in a pillar with a smaller cross-sectional area.

Assuming a pillar area of $7.85 \times 10^{-11}$ cm$^2$, (that is, $\pi \cdot (50\text{ nm})^2$) a contact resistance $R_c$ to the pillar of 42.1 MΩ is obtained. While this contact resistance is quite large, this number is orders of magnitude lower than the linear resistance $R_{LIN} = 1/G_{LIN}$. However, the pillar contacts are much smaller than the contacts in TLM structure used to extract the contact resistance. For example, due to the tilt of the ion implantation, a fraction of the dose may have been screened by the
sidewalls of the vias, causing the doping density at the drain end of the channel to be lower than the doping density of the larger contacts. If this is the case, the pillar contact resistance may be even larger, but it is impossible to measure this resistance directly with the current structures. This may cause $R_c$ to dominate over $R_{LIN}$, and an inaccurate measurement of $G_{LIN}$.

In addition, to the difference in saturation current, the saturation conductance was much lower than the simulations predicted. While in general this indicates better performance as a current limiter, the lower saturation current creates somewhat of a trade-off between the two.

**Table 5.4:** Comparison between simulation results to measured data

<table>
<thead>
<tr>
<th></th>
<th>Measured</th>
<th>Sim (rectangular)</th>
<th>Sim (cylindrical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_D$</td>
<td>$5 \times 10^{14}$ cm$^{-3}$</td>
<td>$2 \times 10^{14}$ cm$^{-3}$</td>
<td>$2 \times 10^{14}$ cm$^{-3}$</td>
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<td>$A$</td>
<td>$\sim 7.85 \times 10^{-11}$ cm$^2$</td>
<td>100 nm $\times$ 100 nm</td>
<td>7.85 $\times 10^{-11}$ cm$^2$</td>
</tr>
<tr>
<td>$G_{LIN}$</td>
<td>0.012 n$\Omega$</td>
<td>11 n$\Omega$</td>
<td>7.93 n$\Omega$</td>
</tr>
<tr>
<td>$G_{OUT}$</td>
<td>29.9 p$\Omega$</td>
<td>0.1 n$\Omega$</td>
<td>2.58 p$\Omega$</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>1.25 pA</td>
<td>1.148 nA</td>
<td>0.291 nA</td>
</tr>
<tr>
<td>$V_{DSS}$</td>
<td>0.1 V</td>
<td>0.11 V</td>
<td>0.036 V</td>
</tr>
</tbody>
</table>

**Figure 5-14:** $G_{LIN}$ vs. Number of Columns
Figure 5-14 plots the linear conductance versus the number of pillars. As can be seen from the plot, there is a nearly linear trend relating the number of pillars to the linear conductance. This shows that the devices are working as intended, and that their characteristics are adding linearly.

Further analysis comparing simulations to the actual devices needs to be conducted. Simulation needs to be made to match the performance of actual devices. This may mean advanced modeling of the sidewall roughness and more sophisticated models for mobility.

5.3.4 Characterization of FET-FEAs

![Diagram](image)

**Figure 5-15:** The experimental setup for testing FET-FEA structures without integrated extraction gates. This testing takes place in an ultra-high vacuum testing chamber to prevent arcing and interactions with gas molecules.

After the FEA devices were fabricated, without a proximal gate the only way to test them would be using using a suspended MEMS extraction gate. The concept for the gate was developed by Dr. Velásquez-García, and consists of a grid made of a silicon wafer that has been through-etched in many places with holes to create a perforated grid. A 25 µm thick polyester gasket is then placed on the surface of the device under test. The MEMS gate is placed on top of that gasket, directly over the
device that is to be tested. The gasket acts as an insulator, so that the gate does not short to the substrate. Alumina spacers are used to clamp the assembled structure together. The assembly is performed manually, and requires a steady hand and careful handling. Figure 5-15 illustrates the test setup for the FET-FEA structure.

Attempts to perform IV characterization of the FET-FEA structure failed, with devices either short-circuiting immediately, or showing no current for large $V_{GS}$. To examine why this was the case, simulations were performed using COMSOL Multiphysics software, which is able to solve Laplace’s equation for a set of boundary conditions. Several different scenarios were simulated: A single exposed tip, a single tip recessed into the substrate, an array of tips exposed, and an array of tips recessed as illustrated in Figure 5-16.

In each case, the emitter consisted of a 10 µm tall pillar with an emitter on top. The emitter had a 5 nm tip radius and a cone-base angle was 45°. An anode was placed 25 µm away, and the electric field in the bulk region was normalized to 1 V/µm. The electric field right at the tip was measured. Table 5.5 summarizes the

![Figure 5-16: The various structures simulated in COMSOL Multiphysics.](image)

(a) (b) (c) (d)
simulation results. While the electric field is over 50 times higher for an isolated tip, when an array of tips is recessed into the substrate, such as in the structure that was fabricated, the field enhancement ratio drops to 8.7.

The structure presented above and simulated has several issues that preclude it from being operated with an external gate. The first is that the neighboring pillars are probably too close to each other, leading to electrostatic field screening. In addition, the fact that they are recessed into the substrate prevents each tip to see the full extent of field enhancement than the tip would if it were alone. This problem could be mitigated if there were a way to bring the gate closer to the tips, but there are no polymer spacers that are thin enough and have the dielectric strength to withstand the voltages that will be applied.

![Simulation Results](image)

**Figure 5-17**: *A*: an example of the 2-D electrostatics simulations performed. Here is shown the simulation for multiple tips that are recessed. *B*: the meshing used at each emitter tip
Table 5.5: Summary of different electrostatic simulations performed for a separation of 25 µm. The local electric field of the multiple tips was measured in the center of the array. Here, the turn on voltage is defined as an electric field of $2 \times 10^3$ V/µm.

<table>
<thead>
<tr>
<th>Description</th>
<th>$E_{bulk}$ [V/µm]</th>
<th>$E_{tip}$ [V/µm]</th>
<th>$\beta$ [cm$^{-1}$]</th>
<th>$V_{turn\ on}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Exposed Tip</td>
<td>1</td>
<td>53.1</td>
<td>$2.12 \times 10^4$</td>
<td>943</td>
</tr>
<tr>
<td>Single Recessed Tip</td>
<td>1</td>
<td>7.6</td>
<td>$3.04 \times 10^3$</td>
<td>6580</td>
</tr>
<tr>
<td>Multiple Exposed Tips</td>
<td>1</td>
<td>22.0</td>
<td>$8.80 \times 10^3$</td>
<td>2270</td>
</tr>
<tr>
<td>Multiple Recessed Tips</td>
<td>1</td>
<td>8.7</td>
<td>$3.48 \times 10^3$</td>
<td>5750</td>
</tr>
</tbody>
</table>

To examine the effect of lowering the substrate in relation to the tips, a series of simulations were performed where the substrate was lowered and the the field enhancement was measured. A 15 µm gap between the substrate and the extraction gate was used, as this is the thinnest polymer spacer commercially available. The structure of the emitters is identical as what was previous simulated.

From these simulations, the field factor $\beta$ and the turn on voltage $V_{turn\ on}$ (defined here as a local electrostatic field of 2 V/nm) were extracted. Figure 5-18 shows the

![Graph showing $\beta$ and $V_{turn\ on}$ vs. Distance Above Substrate](image)

Figure 5-18: The effect of exposing the tips above the substrate on $\beta$ and $V_{turn\ on}$.
results. As expected, bringing the extraction gate close to the emitters reduces the voltage required for field emission. The Keithley 237 precision source measure units that are available to test have a maximum output voltage of 1100 V, so the turn on voltage must be under this voltage to emit.

To test these field emission devices with an external gate will require a mask that has the emitters completely exposed, so that the extraction gate is only 5 $\mu$m away from the emitter tips. While it is possible to fabricate this structure, a new set of photomasks will need to be fabricated. Thus, the structure that was fabricated was not testable.

5.4 Chapter Summary

This chapter presents the I-V characterization of two different lots of ungated FET pillars. First, the measurement set-up and methods were described. Then, from the I-V characteristics, the device parameters for ungated FETs, $G_{LIN}$, $G_{OUT}$, $I_{DSS}$, and $V_{DSS}$, were extracted. Process characterization was performed to extract the resistivity of the substrate, and the specific resistance of the contacts. Finally, a comparison between simulation results and measured results was performed.

The biggest shortcoming of this work is the lack of experimental field emission data to accompany the ungated FET experiments. Future work should focus on building structures with testable FEA-FETs.
Chapter 6

Thesis Summary and Future Work

6.1 Thesis Summary

Field emitters are an exciting technology for high-frequency, high-power applications because of their excellent free space electron transport and their potential for high current density and high current especially when used in an array format. However, a major challenge preventing their widespread use are the spatial and temporal variations that arise from emitter tip radius variations and work function variations, respectively. Both of these issues are a direct result of the tip fabrication process. These non-uniformities cause sharper emitters to burn out before duller emitters turn on, reducing the current density attainable from field emission arrays.

To combat these variations, groups have attempted to incorporate active ballasting elements such as planar MOSFETs and reverse biased diodes and passive, large resistors, but neither of these approaches are optimal. MOSFETs greatly increase the complexity and difficulty of the fabrication, and because they take up a large amount of area reducing the emitter density, they cannot be used to ballast individual emitters without the penalty of adversely reducing the array density. With reverse-biased diodes and resistors, it is impossible to get a high current.

In our prior efforts to solve the problem, we developed the vertical ungated FET structure which addresses these issues. The vertical ungated FET uses the channel pinch-off and velocity saturation of carriers in silicon combined with a high aspect
ratio to provide an effective method of controlling current. Originally the structure was developed as a 1 µm × 1 µm × 100 µm pillar with 10 µm pitch, but this structure limits the possible emitter density. Furthermore, the turn-on and operating voltages of the device is relatively high because the gate aperture is usually at the minimum the same diameter as the pillar diameter. A consequence of the high operating voltage is that when each emitter is biased with a current limiter, the observed variation in the tip current when their is no ballasting element biasing the tip is translated to a variation in the voltage drop across the tip. The variation in the voltage drop across the tip translates to a variation in the energy distribution of the electrons emitted from the array of tips. This large operating voltage results in a large energy distribution in the emitted electrons, which makes electron optics challenging. An approach for reducing the energy spread when field emitters are biased with current limiters would be to redesign the cathode to operate at lower voltages. If the operating voltages are lower, the energy spread would also be lower.

Thus, to reduce the operating voltage, and likewise the energy spread of the emitted electrons, we developed current limiters that were 100 nm in diameter, with a pitch of 1 µm. These devices demonstrated excellent current saturation, with output conductances lower than 10^{-11} S. In addition, a fabrication process for building nano-sharp emitters on these pillars is described. Tip radii of less than 6 nm were obtained, on top of the pillars. It will be possible to integrate extraction gates with small apertures into this structure, allowing for stable, uniform emission at gate voltages under 20 V.

Simulations and numerical modeling of FEA-FET devices was performed, to verify low-voltage operation and current control. Through comparison with experimental data, these simulations indicate that the integrated structure behaves largely like the individual structures connected in series, and provides a clear path going forward for the fabrication of these structures and expectations for their performance.

Finally, an extended model of tunneling from accumulation layers in semiconductors was developed. By considering the changes to the electron number density at the surface, as well as the quantized energy bands that arise inside the accumulation
layer, a new expression for the emitted current density is described.

Altogether, this thesis brings the field of vacuum microelectronics one step closer to achieving the stable and uniform currents with low electron energy distribution required for many applications, and incrementally advances the theory of emission from semiconducting materials.

6.2 Future work

Unfortunately, the line has to be drawn somewhere, so there are some things which this work has not addressed to the degree at which they deserve. These include:

- An analysis of the pillar diameter distribution should be conducted. The pillar diameter is a largely a function of the original photomask pattern. The photomask itself showed some variation across the arrays contributing to variations even before taking into account variations in the etching. Because the deep reactive ion etching step is very sensitive to the initial conditions of the mask, these small variations in the photomask may have resulted in larger variations of the pillar diameter, but a systematic study of the variation has not been performed.

- Completely exposed field emission arrays should be fabricated. These exposed arrays will allow for field emission testing with our current measurement system, providing insight into the field emitter performance, even without integrated extraction gates.

- The process should be modified to incorporate integrated, self-aligned gates for each individual field emitter to allow for low voltage operation to realize the main benefits of scaling the voltage: low energy distribution of the emitted electrons. Optimally, this structure will include an integrated electrostatic focusing electrode. Obviously, the performance will need to be characterized with IV characterization, showing both three- and four-terminal operation.
• Finally, the model of tunneling from bound states should be applied to experimental field emission data from semiconductors.
Appendix A

Table of Fundamental Physical Constants

<table>
<thead>
<tr>
<th>Physical Constant</th>
<th>Symbol</th>
<th>SI units</th>
<th>“microelectronic” units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boltzmann constant</td>
<td>$k_B$</td>
<td>$1.38 \times 10^{-23}$ J/K</td>
<td>$8.62 \times 10^{-5}$ eV/K</td>
</tr>
<tr>
<td>Electron charge</td>
<td>$q$</td>
<td>$1.60 \times 10^{-19}$ C</td>
<td>$1.60 \times 10^{-19} = 1 , e$</td>
</tr>
<tr>
<td>Electron rest mass</td>
<td>$m_0$</td>
<td>$9.11 \times 10^{-31}$ kg</td>
<td>$5.69 \times 10^{-16}$ eV·s²/cm²</td>
</tr>
<tr>
<td>Planck constant</td>
<td>$h$</td>
<td>$6.63 \times 10^{-34}$ J·s</td>
<td>$4.14 \times 10^{-15}$ eV·s</td>
</tr>
<tr>
<td></td>
<td>$\hbar$</td>
<td>$1.05 \times 10^{-34}$ J·s</td>
<td>$6.58 \times 10^{-16}$ eV·s</td>
</tr>
<tr>
<td>Speed of light in vacuum</td>
<td>$c$</td>
<td>$3.00 \times 10^8$ m/s</td>
<td>$3.00 \times 10^{10}$ cm/s</td>
</tr>
<tr>
<td>Permittivity of vacuum</td>
<td>$\epsilon_0$</td>
<td>$8.85 \times 10^{-12}$ F/m</td>
<td>$8.85 \times 10^{-14}$ F/cm</td>
</tr>
</tbody>
</table>

Conversion between both systems:

$$1 \, \text{eV} = 1.60 \times 10^{-19} \, \text{J}$$

$$1 \, \text{kg} = 6.24 \times 10^{14} \, \text{eV} \cdot \text{s}^2/\text{cm}^2$$

From [54]
## Appendix B

### Table of Important Material

#### Parameters of Si and GaAs at 300 K

<table>
<thead>
<tr>
<th>Physical Parameter</th>
<th>Sym</th>
<th>Si Value</th>
<th>GaAs Value</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>lattice constant</td>
<td>a</td>
<td>0.543</td>
<td>0.565</td>
<td>nm</td>
</tr>
<tr>
<td>interatomic distance</td>
<td>Na</td>
<td>0.235</td>
<td>0.245</td>
<td>nm</td>
</tr>
<tr>
<td>atomic density</td>
<td>d</td>
<td>5.0 × 10^{22}</td>
<td>4.4 × 10^{22}</td>
<td>g</td>
</tr>
<tr>
<td>density</td>
<td></td>
<td>2.33</td>
<td>5.32</td>
<td>g·cm^{-3}</td>
</tr>
<tr>
<td>linear thermal expansion coefficient</td>
<td>α</td>
<td>2.59 × 10^{-6}</td>
<td>5.73 × 10^{-6}</td>
<td>K^{-1}</td>
</tr>
<tr>
<td>relative dielectric constant</td>
<td>εr</td>
<td>11.7</td>
<td>12.9</td>
<td>-</td>
</tr>
<tr>
<td>electron affinity</td>
<td>χ</td>
<td>4.04</td>
<td>1.422</td>
<td>eV</td>
</tr>
<tr>
<td>bandgap energy</td>
<td>Eg</td>
<td>1.124</td>
<td>1.422</td>
<td>eV</td>
</tr>
<tr>
<td>DOS electron effective mass</td>
<td>m_{de}^*</td>
<td>1.09 m_0</td>
<td>0.066 m_0</td>
<td>eV·s^2/cm^2</td>
</tr>
<tr>
<td>DOS hole effective mass</td>
<td>m_{dh}^*</td>
<td>1.15 m_0</td>
<td>0.52 m_0</td>
<td>eV·s^2/cm^2</td>
</tr>
<tr>
<td>conduction band effective DOS</td>
<td>N_c</td>
<td>2.86 × 10^{19}</td>
<td>4.21 × 10^{17}</td>
<td>cm^{-3}</td>
</tr>
<tr>
<td>valence band effective DOS</td>
<td>N_v</td>
<td>3.10 × 10^{19}</td>
<td>9.51 × 10^{18}</td>
<td>cm^{-3}</td>
</tr>
<tr>
<td>intrinsic carrier concentration</td>
<td>n_i</td>
<td>1.07 × 10^{10}</td>
<td>2.25 × 10^{6}</td>
<td>cm^{-3}</td>
</tr>
<tr>
<td>optical phonon energy</td>
<td>E_{opt}</td>
<td>0.063</td>
<td>0.035</td>
<td>eV</td>
</tr>
<tr>
<td>conductivity electron effective mass</td>
<td>m_{ce}^*</td>
<td>0.28 m_0</td>
<td>0.070 m_0</td>
<td>eV·s^2/cm^2</td>
</tr>
<tr>
<td>conductivity hole effective mass</td>
<td>m_{he}^*</td>
<td>0.41 m_0</td>
<td>0.44 m_0</td>
<td>eV·s^2/cm^2</td>
</tr>
<tr>
<td>phonon-limited electron mobility</td>
<td>μ_e</td>
<td>1430</td>
<td>8000</td>
<td>cm^2/V·s</td>
</tr>
<tr>
<td>phonon-limited hole mobility</td>
<td>μ_h</td>
<td>480</td>
<td>320</td>
<td>cm^2/V·s</td>
</tr>
<tr>
<td>electron saturation velocity</td>
<td>ν_{sat}</td>
<td>1.0 × 10^7</td>
<td>1.0-1.5×10^7</td>
<td>cm/s</td>
</tr>
<tr>
<td>hole saturation velocity</td>
<td>ν_{hoat}</td>
<td>6.0 × 10^6</td>
<td></td>
<td>cm/s</td>
</tr>
<tr>
<td>optical G/R rate coefficient</td>
<td>r_{rad}</td>
<td>2.0 × 10^{-15}</td>
<td>7.2 × 10^{-10}</td>
<td>cm^3/s</td>
</tr>
<tr>
<td>electron-electron Auger coefficient</td>
<td>r_{eeh}</td>
<td>1.8 × 10^{-31}</td>
<td>1.8 × 10^{-31}</td>
<td>cm^6/s</td>
</tr>
<tr>
<td>hole-hole Auger coefficient</td>
<td>r_{ehh}</td>
<td>9.5 × 10^{-32}</td>
<td>4.0 × 10^{-30}</td>
<td>cm^6/s</td>
</tr>
<tr>
<td>impact ionization threshold energy</td>
<td>E_{ii}</td>
<td>1.12</td>
<td>1.72</td>
<td>eV</td>
</tr>
</tbody>
</table>

From [54]
Appendix C

SILVACO Deck for Fabrication Process and Device Simulations

C.1 Process Simulation - ssc01.in

```plaintext
go athena
# Si Current Limiter for CNT FEA Process Simulation
# File Name : ssc01.in
# Author Tayo Akinwande and Stephen Guerrera
# Written: June 15, 2008
# Last modified: March 9, 2011
# Objective is to simulate the scaled vertical Si Current Limiter
# Channel Length =10 um, x-sectional =100x100 nm^2, Nd=2e14
#
#
# Initial Grid
line x loc=0.00 spac=0.030
line x loc=0.10 spac=0.030
line x loc=0.50 spac=0.050
line x loc=1.00 spac=0.025
#
line y loc=0.00 spac=0.050
line y loc=0.10 spac=0.10
line y loc=0.50 spac=0.20
line y loc=1.00 spac=0.50
line y loc=9.50 spac=0.20
line y loc=9.75 spac=0.10
line y loc=10.00 spac=0.050
line y loc=10.25 spac=0.10
line y loc=10.50 spac=0.20
line y loc=12.00 spac=0.50
```
# Initial Silicon Structure
init silicon c.phosphor=2.0e14 orientation=100 two.d
#
# Pad Oxide
deposit oxide thick=.20 divisions=10
#
# Etch Oxide Mask
#
etch oxide start x=0.16 y=0.00
etch cont x=0.70 y=0.00
etch cont x=0.70 y=-0.20
etch done x=0.16 y=-0.20
#
# save file
struct outfile=ssc01_0.str
tonyplot ssc01_0.str
#
# Directional Silicon Etch Rate in STS
rate.etch machine=STS silicon a.s rie isotropic=0.00 dir=20 chem=0.00 \ div=0.001
#
# Silicon Anisotropic Etch
etch machine=STS time=5000 seconds dx.mult=1.0
#
# save file
struct outfile=ssc01_1.str
tonyplot ssc01_1.str
#
# Trench Wall Oxidation
diffus time=40 temp=950 weto2 press=1.00 hcl.pc=0
#
# Trench Wall Re-Oxidation
diffus time=200 temp=1050 weto2 press=1.00 hcl.pc=0
#
# Trench Wall Re-Oxidation
diffus time=200 temp=1050 weto2 press=1.00 hcl.pc=0
#
# Trench Wall Re-Oxidation
diffus time=200 temp=1050 weto2 press=1.00 hcl.pc=0
#
# save file
struct outfile=ssc01_2.str
tonyplot ssc01_2.str
#
# LPCVD of LTO
deposit oxide thick=0.18 dy=0.02
#
struct outfile=ssc01_3.str
tonyplot ssc01_3.str
#
# Polish rate of polysilicon in CMP
rate.polish machine=CMP poly a.m max.hard=150 min.hard=30 isotropical=10
# Polish rate of oxide in CMP
rate.polish machine=CMP oxide a.m  max.hard=150 min.hard=30 isotropical=10
#
# Polish oxide and poly
polish machine=CMP time=110.0 minutes dx.mult=0.5
#
struct outfile=ssc01_4.str
tonyplot ssc01_4.str
#
# Implant Contact Region
implant phosphor dose=2.5e12 energy=50 rotation=45 crystal
#
# Implant Anneal / Oxidation
diffus time=10 temp=800 dryo2
##
struct outfile=ssc01_5.str
tonyplot ssc01_5.str
#
# Contact Hole Etch
etch oxide start x=0.05 y=0.11
etch cont x=0.05 y=0
etch cont x=0.00 y=0
etch done x=0.00 y=0.11
#
# Titanium Silcide Contact Formation
deposit tisix thick=0.05
#
# Aluminun Metal Deposition
deposit aluminum thick=0.2
#
# Aluminum Etch
etch aluminum right p1.x=0.1
#
# Titanium Silicide Etch
etch tisix right p1.x=0.1
#
struct outfile=ssc01_6.str
tonyplot ssc01_6.str
#
# 2D Mirror
#struct mirror left
#
electrode name=Anode x=0.01 y=0.00
#
electrode name=Cathode backside
#
#
struct outfile=ssc01_7.str
tonyplot ssc01_7.str
#
#
quit
C.2 Device Simulation - sscdev01.in

go atlas
# Current limiter simulations
# Vertical Sicon Current Limiter Device Simulation
# File Name : cylsscdev01.in
# Authors: Tayo Akinwande and Stephen Guerrera
# This simulation deck tested anode voltage 0<Va<10 V
# Device parameters L = 10 micron A= 100 nm x 100 nm Nd = 2x10^14 cm^-3
#
mesh   infile=ssc01_7.str
#
# Electrode Definitions
#
# #1=anode #2=cathode
electrode name=anode number=1
electrode name=cathode number=2
#
# contact name=source neutral
# contact name=drain neutral
#
# Device Models
#
models srh conmob fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \ 
boltzman print numcarr=2 temperature=300
#
# mobility 
bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200 \ 
taun.cvt=0.125 taup.cvt=0.0317 gamm.cvt=2.5 gamp.cvt=2.2 \ 
mun.cvt=52.2 munp.cvt=44.9 muin.cvt=43.4 muip.cvt=29 mumaxn.cvt=1417 \ 
mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 csn.cvt=3.43e+20 \ 
csp.cvt=6.1e+20 alphan.cvt=0.68 alphap.cvt=0.71 betan.cvt=2 betap.cvt=2 \ 
pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 delp.cvt=2.0546e+14
#
#
# Numerical Simulation Methods
#
method   newton itlimit=25 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1 \ 
tol.time=0.005 dt.min=1e-25
#
#
# Output Electron and Hole velocities
#
output flowlines e.velocity h.velocity ex.velocity ey.velocity hx.velocity \ 
hy.velocity
#
#
# Initial Solutions
#
solve init
#
# save output structure and plot
save   outf=sscdev01_00.str
tonyplot sscdev01_00.str
# Solution for low anode bias
#
solve vanode=0.001
# solve vanode=0.05
# solve vanode=0.1
# solve vanode=0.5
# solve vanode=1.0
#
# save output structure and plot
save outf=sscdev01_01.str
tonyplot sscdev01_01.str
#
# Calculate transfer characteristics
log outf=sscdev01_0.log
solve vanode=0.0 vstep=0.0005 vfinal=0.1 name=anode
solve vanode=0.11 vstep=0.01 vfinal=0.5 name=anode
solve vanode=0.52 vstep=0.02 vfinal=1.00 name=anode
#
# save output structure and plot
save outf=sscdev01_02.str
tonyplot sscdev01_02.str
#
solve vanode=1.05 vstep=0.05 vfinal=3.0 name=anode
#
# save output structure and plot
save outf=sscdev01_03.str
tonyplot sscdev01_03.str
#
solve vanode=3.05 vstep=0.05 vfinal=7.0 name=anode
#
# save output structure and plot
save outf=sscdev01_04.str
tonyplot sscdev01_04.str
#
solve vanode=7.1 vstep=0.1 vfinal=10.0 name=anode
#
# save output structure and plot
save outf=sscdev01_05.str
tonyplot sscdev01_05.str
#
# Plot current voltage characteristics
#
quit
Appendix D

Process Flows

The procedures outlined below are for the fabrication of vertical ungated FETs. The machines utilized for the fabrication of these structures are located in MIT’s Microsystems Technology Laboratories (MTL). While these processing steps and conditions could be used as a guideline, results may vary greatly depending on feature density, and from run to run.

D.1 Fabrication of Vertical Ungated FETs - Lot1

<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alignment Marks Definition</td>
<td></td>
<td></td>
<td>Standard RCA clean prior to tube run</td>
</tr>
<tr>
<td>1</td>
<td>ICL</td>
<td>RCA-ICL</td>
<td>1. 10 min SC-1 (5:1:1 DI water:H₂O₃:NH₃ at 80°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. 1 min HF dip (50:1 DI water:HF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3. 15 min SC-2 (6:1:1 DI water:H₂O₂:HCl at 80°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4. SRD</td>
</tr>
<tr>
<td>2</td>
<td>ICL</td>
<td>Tube-5D</td>
<td>Hard mask formation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Wet oxidation at 1000°C. Target thickness: 3 kÅ. Following growth, thickness characterization was performed using the UV1280 ellipsometer.</td>
</tr>
</tbody>
</table>

cont’d
<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
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<th>Description / Processing Conditions</th>
</tr>
</thead>
</table>
| 3    | ICL      | Coater6  | Coat with standard photoresist  
Recipe: T1HMDS                                                                                                                                      |
| 4    | ICL      | i-Stepper| Expose level 0: Alignment Marks  
Exposure: 165 ms                                                                                                                                         |
| 5    | ICL      | Coater6  | Develop photoresist on developer track  
Recipe: Dev6                                                                                                                                         |
| 6    | ICL      | AME5000  | Etch alignment marks through the oxide and into the silicon substrate. A 10 s descum etch was first performed, then the oxide etch was performed in chamber A using recipe baseline.ox_new for 120 s. The silicon etch was performed in chamber B using recipe 5000:STI for a 15 seconds. |
| 7    | ICL      | Asher-ICL| Remove resist in oxygen plasma for 3 minutes and 15 seconds                                                                                                                                                                       |

**Column Etching**

<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
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</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>ICL</td>
<td>Coater6</td>
<td>Coat with standard resist using recipe T1HMDS</td>
</tr>
<tr>
<td>9</td>
<td>ICL</td>
<td>i-Stepper</td>
<td>Expose level 1: Columns. Exposure: 100 ms at optimal focus position</td>
</tr>
<tr>
<td>10</td>
<td>ICL</td>
<td>Coater6</td>
<td>Develop columns layer on developer track using recipe PUD3SG, modified to be slightly shorter than the original PUDDLE3 recipe. Total develop time is 26s. Verify exposure quality in optical microscope and SEM.</td>
</tr>
<tr>
<td>11</td>
<td>ICL</td>
<td>AME5000</td>
<td>Etch hardmask. Prior to etching, perform an O₂ descum for 15 s to clean up resist profile. Etch oxide using recipe baseline.ox_new for 130 s. Verify hard mask profile in SEM.</td>
</tr>
</tbody>
</table>

cont’d
<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>TRL</td>
<td>STS2</td>
<td>Etch pillars using recipe GUERRER2. Etch conditions: 6s C₄F₈ passivation cycle @ 40 sccm, 5s SF₆ etch cycle @ 105 sccm, 600 Watts RF (passivation), 800 Watts RF (etch), 120 Watts bias power, passivate first. Constant pressure 25 mTorr. Total etch time was 8 minutes. End on etch step to minimize polymer contamination.</td>
</tr>
<tr>
<td>13</td>
<td>ICL</td>
<td>SEM-Zeiss</td>
<td>Examine etch profile using SEM. This step guides the oxidation in step 20.</td>
</tr>
<tr>
<td>14</td>
<td>TRL</td>
<td>Asher-TRL</td>
<td>Remove photoresist in O₂ plasma.</td>
</tr>
<tr>
<td>15</td>
<td>TRL</td>
<td>Acidhood</td>
<td>Strip hardmask in pure (50%) HF.</td>
</tr>
<tr>
<td>16</td>
<td>TRL</td>
<td>Acidhood</td>
<td>Pirahna clean (3:1 H₂SO₄:H₂O₂). SRD.</td>
</tr>
<tr>
<td>17</td>
<td>TRL</td>
<td>Asher-TRL</td>
<td>Ash 1.5 hours</td>
</tr>
<tr>
<td>18</td>
<td>TRL</td>
<td>Acidhood</td>
<td>Pirahna clean</td>
</tr>
</tbody>
</table>

**DRIE Polymer Removal**

<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>TRL</td>
<td>RCA-TRL</td>
<td>RCA cleaning prior to tube run</td>
</tr>
<tr>
<td>20</td>
<td>TRL</td>
<td>Tube-A2</td>
<td>Dry thermal oxidation at 1000°C. Oxidation time 5 hours 30 minutes so that the resultant pillar diameter is approximately 100 nm. Numerical simulations of the oxidation performed to guide this oxidation</td>
</tr>
</tbody>
</table>

**Surface Passivation / Oxidation thinning**

<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>TRL</td>
<td>RCA-TRL</td>
<td>RCA clean</td>
</tr>
<tr>
<td>22</td>
<td>ICL</td>
<td>LTO</td>
<td>LTO deposition using the Akinwande group’s special dedicated quartzware. Recipe 53ASPK. Target thickness: 3000 Å. To characterize deposition, include a dummy wafer and measure using ellipsometry. Characterize LTO conformality using SEM.</td>
</tr>
</tbody>
</table>

cont’d
<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>TRL</td>
<td>RCA-TRL</td>
<td>RCA clean (omitted if wafers coming directly from LTO deposition)</td>
</tr>
<tr>
<td>24</td>
<td>TRL</td>
<td>Tube-B4</td>
<td>Poly-Si deposition to fill voids. Target thickness 8 kÅ. To characterize deposition, include a dummy wafer with 1 kÅ oxide and measure using ellipsometry.</td>
</tr>
<tr>
<td>25</td>
<td>TRL</td>
<td>RCA-TRL</td>
<td>RCA clean (omitted if wafers are coming directly from Tube-B4.</td>
</tr>
<tr>
<td>26</td>
<td>TRL</td>
<td>Tube-A2</td>
<td>Wet oxidation of poly-Si on surface at 1000°C (consume 550 nm of poly-Si)</td>
</tr>
<tr>
<td>27</td>
<td>ICL</td>
<td>oxEtch-BOE</td>
<td>Strip oxidized poly in buffered oxide etchant (BOE - 7:1 NH₄F:HF). Etch time is 15 minutes, or until wafer de-wets when removed from the etching solution. Dump rinse, then SRD.</td>
</tr>
<tr>
<td>28</td>
<td>TRL</td>
<td>RCA-TRL</td>
<td>RCA clean</td>
</tr>
<tr>
<td>29</td>
<td>TRL</td>
<td>Tube-A2</td>
<td>Wet Oxidation of remaining poly-Si on surface of wafer at 1000°C (consume 250nm poly + 50% over-oxidation)</td>
</tr>
</tbody>
</table>

**Back End Processing**

<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>TRL</td>
<td>TRL-HMDS</td>
<td>15s HMDS treatment of wafers in vacuum oven.</td>
</tr>
<tr>
<td>31</td>
<td>TRL</td>
<td>Coater</td>
<td>Coat wafers with one micron OCG 825 positive resist</td>
</tr>
<tr>
<td>32</td>
<td>TRL</td>
<td>Pre-bake</td>
<td>Bake in prebake oven 95°C 30 minutes.</td>
</tr>
<tr>
<td>33</td>
<td>TRL</td>
<td>EV-1</td>
<td>Expose level 2A: Large Vias. 2s exposure with hard contact.</td>
</tr>
<tr>
<td>34</td>
<td>TRL</td>
<td>Photo-Wet</td>
<td>Develop 1 minute in OCG 934 positive resist developer. SRD</td>
</tr>
<tr>
<td>35</td>
<td>TRL</td>
<td>Post-bake</td>
<td>Bake in postbake at 120°C for 30 minutes.</td>
</tr>
<tr>
<td>36</td>
<td>ICL</td>
<td>AME5000</td>
<td>Etch vias through the oxide, stopping on silicon. Using recipe baseline_ox_new, etch time is 200s, including overetch.</td>
</tr>
</tbody>
</table>

cont’d
<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>ICL</td>
<td>Asher-ICL</td>
<td>Remove resist in oxygen plasma for 3 minutes and 15 seconds</td>
</tr>
<tr>
<td>38</td>
<td>ICL</td>
<td>Coater6</td>
<td>Coat with standard photoresist Recipe: T1HMDS</td>
</tr>
<tr>
<td>39</td>
<td>ICL</td>
<td>i-Stepper</td>
<td>Expose level 2b: Fine Alignment Marks Exposure: 290 ms at optimal focus</td>
</tr>
<tr>
<td>40</td>
<td>ICL</td>
<td>Coater6</td>
<td>Develop using PUDDLE3 recipe. Verify resist structure is acceptable using SEM.</td>
</tr>
<tr>
<td>41</td>
<td>ICL</td>
<td>AME5000</td>
<td>Etch vias through the oxide, stopping on silicon. Using recipe baseline_ox_new, etch time is 220s, including overetch. Verify vias in SEM.</td>
</tr>
<tr>
<td>42</td>
<td>ICL</td>
<td>Asher-ICL</td>
<td>Remove resist in oxygen plasma for 3 minutes and 15 seconds</td>
</tr>
<tr>
<td>43</td>
<td>TRL</td>
<td>RCA-TRL</td>
<td>RCA clean</td>
</tr>
<tr>
<td>44¹</td>
<td>ICL</td>
<td>Tube-6A</td>
<td>Deposit 2000 Å n⁺ poly-Si to form contacts. Include a dummy wafer with 1000 Å oxide to measure sheet resistance and thickness.</td>
</tr>
<tr>
<td>45</td>
<td>TRL</td>
<td>Tube-B3</td>
<td>Immediate transfer wafers to tube to anneal and activate dopants at 950°C for 30 minutes under N₂ ambient</td>
</tr>
<tr>
<td>46</td>
<td>ICL</td>
<td>Premetal-Piranha</td>
<td>10 mins Piranha + 15 seconds HF dip to expose a clean silicon surface immediately prior to metallization.</td>
</tr>
<tr>
<td>47</td>
<td>ICL</td>
<td>Endura</td>
<td>Physical vapor deposition (PVD) of a 1 kÅ TiN diffusion barrier and 10 kÅ Al contact metal.</td>
</tr>
<tr>
<td>48</td>
<td>TRL</td>
<td>TRL-HMDS</td>
<td>15s HMDS treatment of wafers in vacuum oven.</td>
</tr>
<tr>
<td>49</td>
<td>TRL</td>
<td>Coater</td>
<td>Coat wafers with two microns OCG 825 positive resist</td>
</tr>
<tr>
<td>50</td>
<td>TRL</td>
<td>Pre-bake</td>
<td>Bake in prebake oven 95°C 30 minutes.</td>
</tr>
</tbody>
</table>

¹This step was approved as a one time exception, and to be used again requires PTC approval.
<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>51</td>
<td>TRL</td>
<td>EV-1</td>
<td>Expose level 3: Metal1. 2s exposure with hard contact.</td>
</tr>
<tr>
<td>52</td>
<td>TRL</td>
<td>Photo-Wet</td>
<td>Develop 1 minute in OCG 934 positive resist developer. SRD</td>
</tr>
<tr>
<td>53</td>
<td>TRL</td>
<td>Post-bake</td>
<td>Bake in postbake at 120°C for 30 minutes.</td>
</tr>
<tr>
<td>54</td>
<td>ICL</td>
<td>Rainbow</td>
<td>Etch Al / TiN / Poly-Si stack using standard Cl₂ chemistry for etching aluminum. Total etch time was 150 s.</td>
</tr>
<tr>
<td>55</td>
<td>ICL</td>
<td>Asher-ICL</td>
<td>Remove resist in oxygen plasma for 3 minutes and 15 seconds</td>
</tr>
<tr>
<td>56</td>
<td>TRL</td>
<td>Tube-A3</td>
<td>Contact formation at 390°C-410°C under forming gas</td>
</tr>
</tbody>
</table>
D.2 Fabrication of Vertical Ungated FETs - Lot2

This process continues exactly as the process shown in the previous section until step 44, with one exception. During the LTO deposition in step 22, the target thickness was 600 nm, twice the target thickness in the first process flow. This fabrication procedure will detail the steps taken from step 44 and beyond.

<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>44</td>
<td>Innovion</td>
<td>Ion implantation</td>
<td>Implant parameters: Energy: 30 keV; Dose $3 \times 10^{15}$ As; Tilt: $7^\circ$</td>
</tr>
<tr>
<td>45</td>
<td>ICL</td>
<td>Premetal</td>
<td>Post implant clean: double piranha (blue, then green)</td>
</tr>
<tr>
<td>46</td>
<td>TRL</td>
<td>Tube-B3</td>
<td>Immediately transfer wafers to tube to anneal and activate dopants at temperature above 950°C for 15 minutes under N$_2$ ambient</td>
</tr>
<tr>
<td>47</td>
<td>ICL</td>
<td>Premetal-Piranha</td>
<td>10 mins Piranha + 15 seconds HF dip to expose a clean silicon surface immediately prior to metallization.</td>
</tr>
<tr>
<td>48</td>
<td>ICL</td>
<td>Endura</td>
<td>Physical vapor deposition (PVD) of a 1 kÅ TiN diffusion barrier and 10 kÅ Al contact metal.</td>
</tr>
<tr>
<td>49</td>
<td>TRL</td>
<td>TRL-HMDS</td>
<td>15s HMDS treatment of wafers in vacuum oven.</td>
</tr>
<tr>
<td>50</td>
<td>TRL</td>
<td>Coater</td>
<td>Coat wafers with two microns OCG 825 positive resist</td>
</tr>
<tr>
<td>51</td>
<td>TRL</td>
<td>Pre-bake</td>
<td>Bake in prebake oven 95°C 30 minutes.</td>
</tr>
<tr>
<td>52</td>
<td>TRL</td>
<td>EV-1</td>
<td>Expose level 3: Metal1. 2s exposure with hard contact.</td>
</tr>
<tr>
<td>53</td>
<td>TRL</td>
<td>Photo-Wet</td>
<td>Develop 1 minute in OCG 934 positive resist developer. SRD</td>
</tr>
<tr>
<td>54</td>
<td>TRL</td>
<td>Post-bake</td>
<td>Bake in postbake at 120°C for 30 minutes.</td>
</tr>
</tbody>
</table>

cont’d
<table>
<thead>
<tr>
<th>Step</th>
<th>Location</th>
<th>Tool</th>
<th>Description / Processing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>55</td>
<td>ICL</td>
<td>Rainbow</td>
<td>Etch Al / TiN stack using standard Cl₂ chemistry for etching aluminum. Total etch time was 100 s.</td>
</tr>
<tr>
<td>56</td>
<td>ICL</td>
<td>Asher-ICL</td>
<td>Remove resist in oxygen plasma for 3 minutes and 15 seconds</td>
</tr>
<tr>
<td>57</td>
<td>TRL</td>
<td>Tube-A3</td>
<td>Contact formation at 390°C-410°C under forming gas</td>
</tr>
</tbody>
</table>


