Design Port and Optimization of a High-Speed SAR ADC Comparator from 65nm to 0.11μm

by

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B.S. Electrical Engineering and Computer Science, MIT, 2010

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of Master of Engineering in Electrical Engineering and Computer Science at the Massachusetts Institute of Technology

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DESIGN PORT AND OPTIMIZATION OF A HIGH-SPEED SAR ADC COMPARATOR FROM 65NM TO 0.11μM

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ABSTRACT

As the world continues to do more and more of its signal processing digitally, there is an ever increasing need for high speed high precision signal processors in consumer applications such as digital photography. Technological progress in CMOS fabrication has allowed chips to be made on nano scale processes, but this still comes at a steep price. Especially in chips for which analog components are a priority over digital components, some of the benefits of using nano scale processes diminish, such as smaller area. In these cases, it is worth investigating whether the same performance can be achieved with larger feature size, and therefore, cheaper processes.

To that end, a three-stage comparator circuit for use in a digital camera SAR ADC has been ported from its original 65nm process to a 0.11µm process. Its design has been analyzed and performance presented here. Additionally, an alternative latch-only architecture for the comparator has been designed and analyzed. In 0.11µm the three-stage comparator operates at the same speed, 13% lower RMS noise contributing 0.9 bits difference, and 11% higher power than the original in 65nm. More noteworthy, the 0.11µm latch-only comparator operates at 40% higher speed, equivalent noise, and 72% lower power.

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CHAPTER 1: INTRODUCTION

1.1 MOTIVATION

Nano scale CMOS technologies provide many benefits in the implementation of today's highly digital circuits, especially in consumer electronics. Digital circuitry follows Moore's law [1] in that moving to a smaller feature size process means more digital components can fit in the same area. Also, smaller devices offer higher gate speed at lower power dissipation digital circuitry. Analog circuits, however, do not necessarily shrink as many designs do not use or allow for minimum length devices. Therefore, in chips in which analog components are more emphasized, some of the benefits of smaller scale technologies such as a reduced chip area are no longer as relevant, and are therefore offset by drawbacks such as higher expense. This makes it worthwhile to investigate implementation of the circuits in larger feature size processes.

The setting of this thesis is the field of high-speed high-precision signal processors for digital camera and camcorder applications. One of the major components of these signal processors is the high-speed ADC (analog-to-digital converter, see star outline in Fig. 1). Several different types of ADC's are commonly used in signal processing applications including flash, pipeline, and Successive Approximation Register (SAR) [2]. Flash ADCs are fast parallel

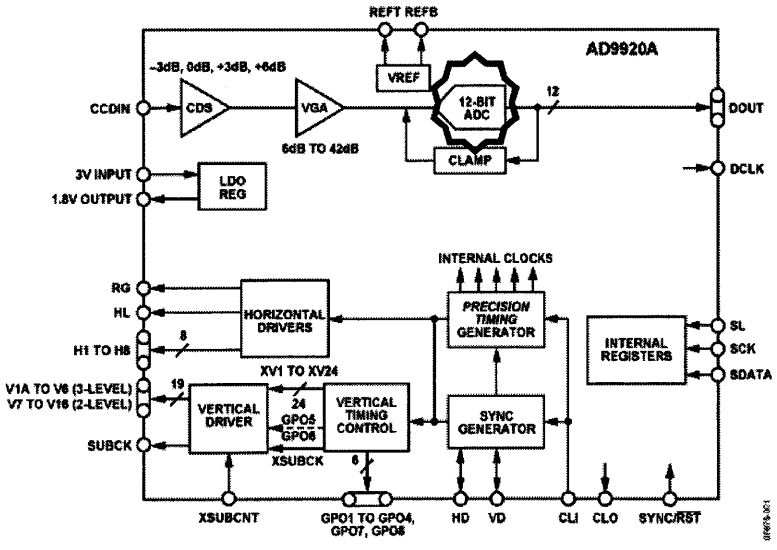


Figure 1: Example of a current 12-bit CCD Signal Processor [3] on the market by Analog Devices. The ADC is highlighted in with a star.

converters but they have a drawback in that for an N-bit flash ADC, 2^N-1 comparators are necessary, thus power and area becomes an issue. Pipeline ADCs are very good for high-speed applications, but their power consumption is often an issue [2]. While the high-speed ADC of choice for the Digital Imaging Group has traditionally been a pipeline ADC, with its transition from 0.18μm to a 65nm CMOS fabrication process, the group began investigating the use of SAR ADCs instead. SAR ADCs tend to consume less power than pipelined ADCs at the cost of speed, but due to the inherent increase in gate speed of the 65nm process node, this trade-off of speed for power was able to be circumvented, and the same spec was achieved by the group. Also, unlike pipeline ADCs, SAR ADCs do not require an amplifier and are thus better suited for smaller process devices with intrinsically lower gain. For this reason, the group decided to use the SAR architecture for its 65nm ADC.

This thesis describes the design port of a comparator for a SAR ADC in digital still camera and camcorder applications, from the 65nm to 0.11μm process node. The two processes have similar characteristics and both operate off a 1.2V supply. Hence, 0.11μm seems like a cheaper alternative to 65nm for chips in which there is less emphasis on digital circuitry, because the area taken by the analog components will be roughly the same. For this reason, porting strategies that maintain the 65nm comparator's performance while moving to the 0.11μm process are investigated here. Furthermore, a different architecture from the one used in 65nm is explored and its relative performance is presented.

The group has never utilized a 0.11μm process before, so this will be the company's first investigation to transition the design of their high speed SAR ADC comparator from 65nm to 0.11μm. The SAR ADC is a 14-bit converter with two redundant bit decisions, for a total of 16 bit decisions. The first 5 MSBs (most significant bits) are decided by an auxiliary flash ADC, leaving 11 decisions for the comparator to arbitrate.

The comparator designed by Analog Devices comprised of three stages: two preamplifier stages, followed by a dynamic latch. While the dynamic latch can make comparator decisions on its own, the preamplifiers increase the signal to overcome offset in the comparator. The preamplifiers also shield the input signal from charge kickback in the latch, defined the charge that is "kicked back" to the inputs through C_{gd} of the input pairs when the latch regenerates. While this doesn't have negative repercussions for all input signals, the inputs in this case come from a capacitive DAC used for sampling that is sensitive to this charge kickback.

1.2 Fundamentals and Basics of Operation

1.2.1 A peek into SAR ADCs

A SAR ADC uses a successive approximation binary search algorithm to get a digital representation of an analog input signal. Fig. 2 shows a simplified representation of a SAR ADC, whose main components are a Track/Hold stage, a SAR logic/register stage, an N-bit digital to analog converter (DAC), and a comparator.

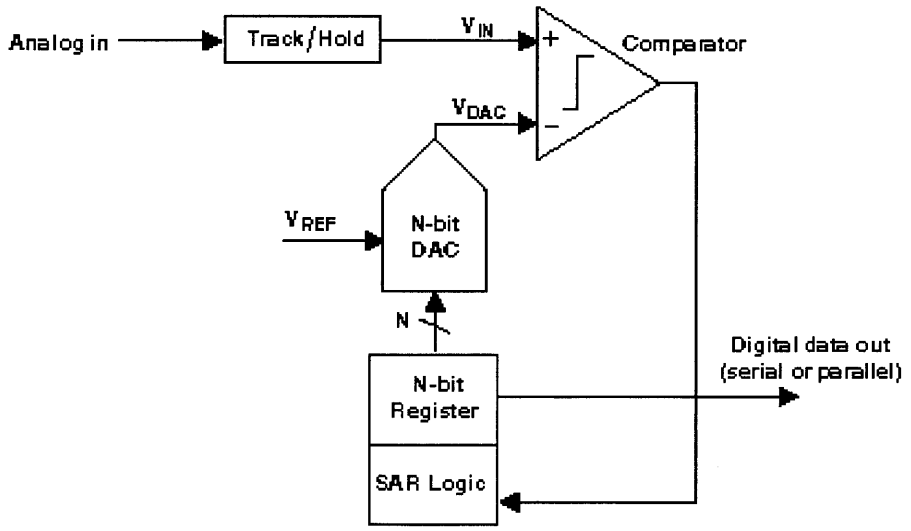


Figure 2: SAR ADC Architecture [2]

Each conversion period consists of two phases: in the first one, the analog signal is tracked and held, and in the second one, the digital output bits are resolved by the SAR logic. Fig. 3 is an example diagram of a four bit SAR ADC using a feedback capacitive DAC.

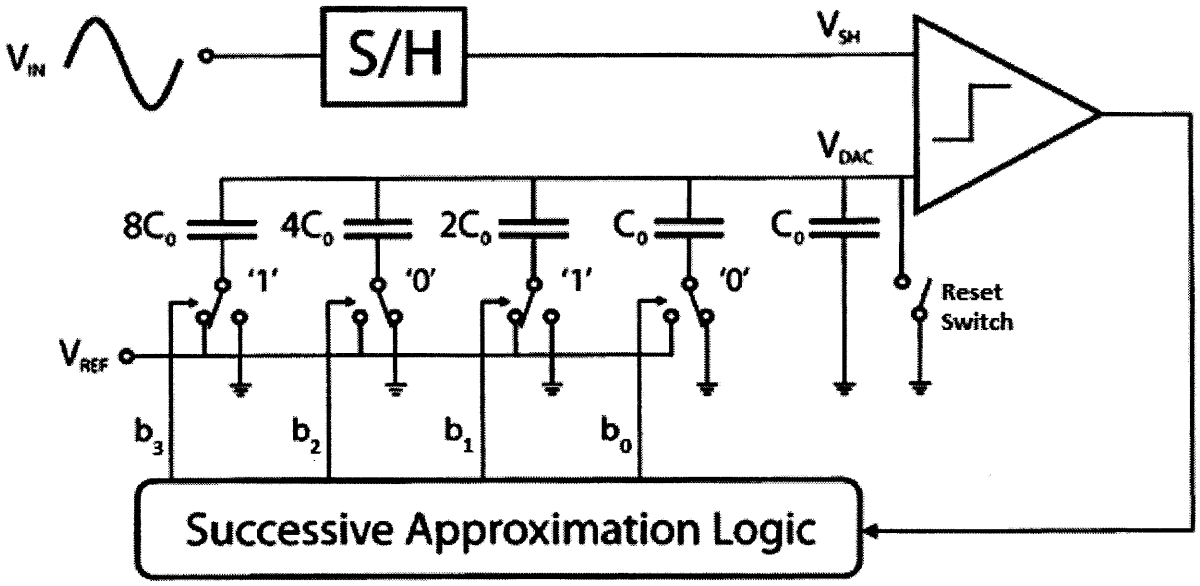


Figure 3: A representative 4-bit SAR ADC Architecture (adapted from [2])

Let us take an example with the held value being V_{SH}=0.6V and V_{REF}=1V. After resetting the DAC voltage V_{DAC}=0V, the most significant bit (MSB), b3, is instantiated as 1. This connects the capacitor for the MSB to V_{REF} and makes the DAC voltage to be fed into the comparator to become 0.5*V_{REF}, or 0.5V. At the comparator level, this is compared to 0.6V and since it is higher, the comparator outputs a logic '1', which is translated through the successive approximation logic to set b3 to 1 for the remainder of the translation. If the sampled voltage were lower than 0.5V, the Reset Switch would be used to reset the capacitors and turn b3 to 0 for the remainder of the cycle. A similar process is used for the remainder of the bits, eventually converging V_{DAC} to V_{SH}. The figure below shows this process in terms of the successive approximation to V_{SH}.

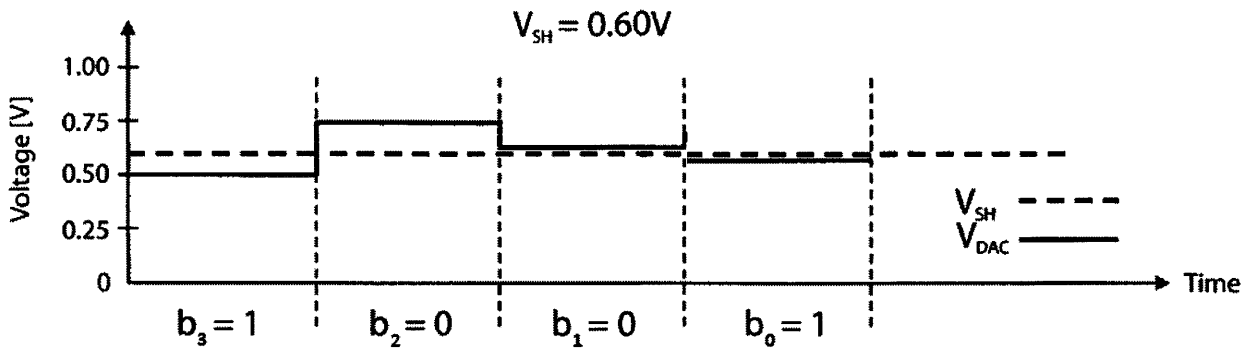


Figure 4: Close-up of 4-bit SAR function given VSH=0.6V

1.2.2 Comparator Design Fundamentals

High speed comparators are critical in making a high speed SAR ADC, because they are one of the main bottlenecks in the overall speed of the ADC. The comparators used in this application take the difference between V+ and V- and if it is positive (i.e. V+ is larger) they output a logic '1', otherwise they output a logic '0'. The speed, or a response time in a comparator is defined as the delay between the time the differential input passes the comparator threshold voltage and the time the output exceeds the input logic level of the subsequent stage [4].

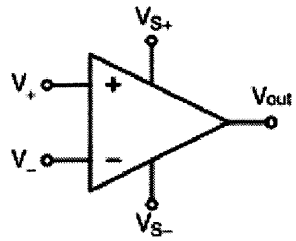


Figure 5: Comparator

One of the simplest forms of a comparator is a two stage compensated op-amp. Compensation of an op-amp often involves the separation of the poles of an op-amp by lowering one pole through the addition of a large capacitor at the output [4]. This form of compensation greatly decreases the speed of op-amps and makes them undesirable for high-speed applications. Even in the uncompensated case, however, the response time is still significantly slow due to other parasitic capacitances, and making this type of comparator inadequate for most high speed applications.

A significantly more popular approach to making a high speed comparator involves multiple stages: one or more high-speed differential pre-amplifier stages often followed by a dynamic latch stage [4]. The purpose of the pre-amplifier stages is to cancel offset and amplify the input voltages to an extent that the input offset voltage becomes negligible. The dynamic latch (shown in Fig. 6) in turn uses strong positive feedback when the clock is high and the input is being sampled to obtain high gain (albeit non-linear) and output a logic '1' or '0' very quickly.

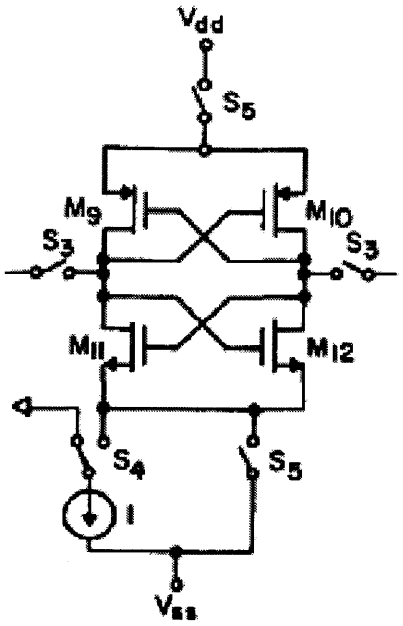


Figure 6: Dynamic Latch [7]

Another design technique to make the comparator even faster involves replacing the active loads (e.g. diode connected loads) in the pre-amplifier stages with resistive loads [4]. This speed increase is due to the limit on the response time by the parasitic capacitances of the load devices. One drawback to this resistive load (other than more power being consumed), however, is that the voltage drop across the resistors can vary significantly with process variations, such as resistor mismatch.

While the SAR ADC to be investigated is 14-bit, 5 of those bits will go through a flash ADC, leaving only 9 bits (plus the two redundant bits mentioned in the previous chapter) to the SAR ADC. The SAR ADC therefore only needs to be mid resolution, and design techniques similar to those described here will be useful.

1.3 STATE OF THE ART

One of the earlier comparator architectures was designed by McCarroll, Sodini, and Lee in 1988 [7]. Pre-amplifier stages were used on V_{in} (which is to be compared to V_{ref}), after which the amplified ($V_{in} - V_{ref}$) was put through a dynamic latch. For the pre-amplifier stages, three configurations were investigated depending on the required output voltage (that would be the input to the dynamic latch): a single stage amplifier, a single stage amplifier with a source follower, and a two stage amplifier with a source follower. The response time was calculated for each and was plotted as a function of the output voltage. For an 8 bit ADC it was found that the one stage pre-amplifier plus a source follower was the optimum configuration. Architectures similar to this one are investigated in detail in this thesis.

More recent papers on SAR ADCs exhibit successful implementations of comparators using only the latch stage [8], or using a single preamp stage and latch stage [9]. An alternative implementation of the 65nm design based on one of these papers will be discussed further in the thesis. It is also useful to take a step back and compare resolution and speed specifications achieved in recent literature, along with the choice of process to be used. The table below compares resolution, speed, and process used in seven recent (2007 on) publications of SAR ADCs. They are organized in order of increasing resolution. Several trends can be seen from these papers. First, speed decreases significantly when the resolution transitions from mid-range (10 bit) to high-range (12 bit and beyond). This follows intuitively because it takes longer to achieve higher-resolution conversion. Another trend can be seen when comparing the two 10 bit SAR ADCs: higher speed can be obtained by using a smaller feature size process such as the one we see below from 90nm to 65nm, something we are trying to circumvent in this thesis (i.e. getting same speed even with a larger process size).

Reference	Resolution (bits)	Speed	Process Size
[16], 2009	4	700 MS/s	0.18μm
[17], 2009	7	2.5 GS/s	45nm
[8], 2009	9	100MS/s	65nm
[18], 2010	10	100MS/s	90nm
[19], 2010	10	204MS/s	65nm
[20], 2009	12	50KS/s	0.14μm
[21], 2007	14	40KS/s	0.13μm

1.4 Specifications of Interest

The three main specifications that this thesis will focus on are speed, noise, and power. The area of the comparator is only about 4% of the total ADC area, and a small area increase from going to 0.11μm will be negligible. Therefore, it wasn't a specification of focus in the thesis (through hand-calculations the 0.11μm comparator area was later estimated to be minimally different from the 65nm comparator area). Also, while it is not of special focus in this thesis, it should be noted that offset must be overcome to get the right bit decision.

The speed, or sample clock rate specification of the 65nm ADC is 80MHz at peak performance, allowing for integration with the 74.24MHz standard for high definition digital video (includes resolutions such as 720p60 and 1080i60) [14]. However, because this particular SAR was designed by the group to be self-timed, there isn't a specific time set for the comparator to finish making a decision, as long as the overall SAR clock rate is met.

Thus in this thesis, instead of keeping to a specific value the 65nm comparator's decision time will be used as a speed benchmark.

In order to match the 65nm comparator noise, the specification here has been set to 71uV rms of input referred noise. Noise in a comparator is not as straightforward to model and quantify as in most linear circuits because of the transient nature of a comparator's operation, and thus periodic noise has been measured using the "Spectre RF" simulation program [15].

The power dissipation specification is also determined by comparison to the one consumed in 65nm, and has been set to 5.4mW. Power is calculated by measuring the average current during operation and multiplying by rail-to-rail voltage, in this case 1.2V.

CHAPTER 2: CHARACTERIZATION OF 65NM VERSUS 0.11μM PROCESS

If certain trends in the MOS devices in 65 nm and 0.11 μm processes are known, we can exploit any benefits of 0.11 μm to obtain better performance when moving to this new process. If there are no benefits, we can at least be aware of the challenges to come. This thesis focuses on the following MOS parameters: transconductance (g_m), switch on-resistance (Ron), and parasitic capacitance (C_{gs},C_{gd}).

The transconductance is closely related to the small signal gain of an amplifier: g_m*r_{out} (shown in Fig. 7). Therefore, higher g_m tends to point to a steady-state higher gain in an amplifier of the same dimensions. Of course, in applications involving reset switches, speed (versus gain) is of greater importance, and in this case a low on-resistance is desired. Parasitic capacitances can limit the speed at which a decision is made (due to 1/RC time constants) so the smaller they are the better.

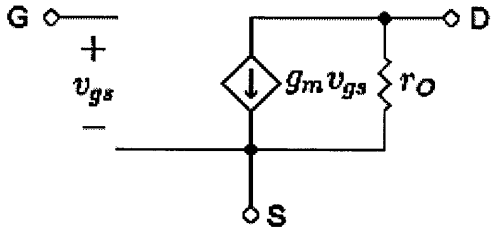


Figure 7: Small-signal MOSFET model

2.1 TRANSCONDUCTANCE

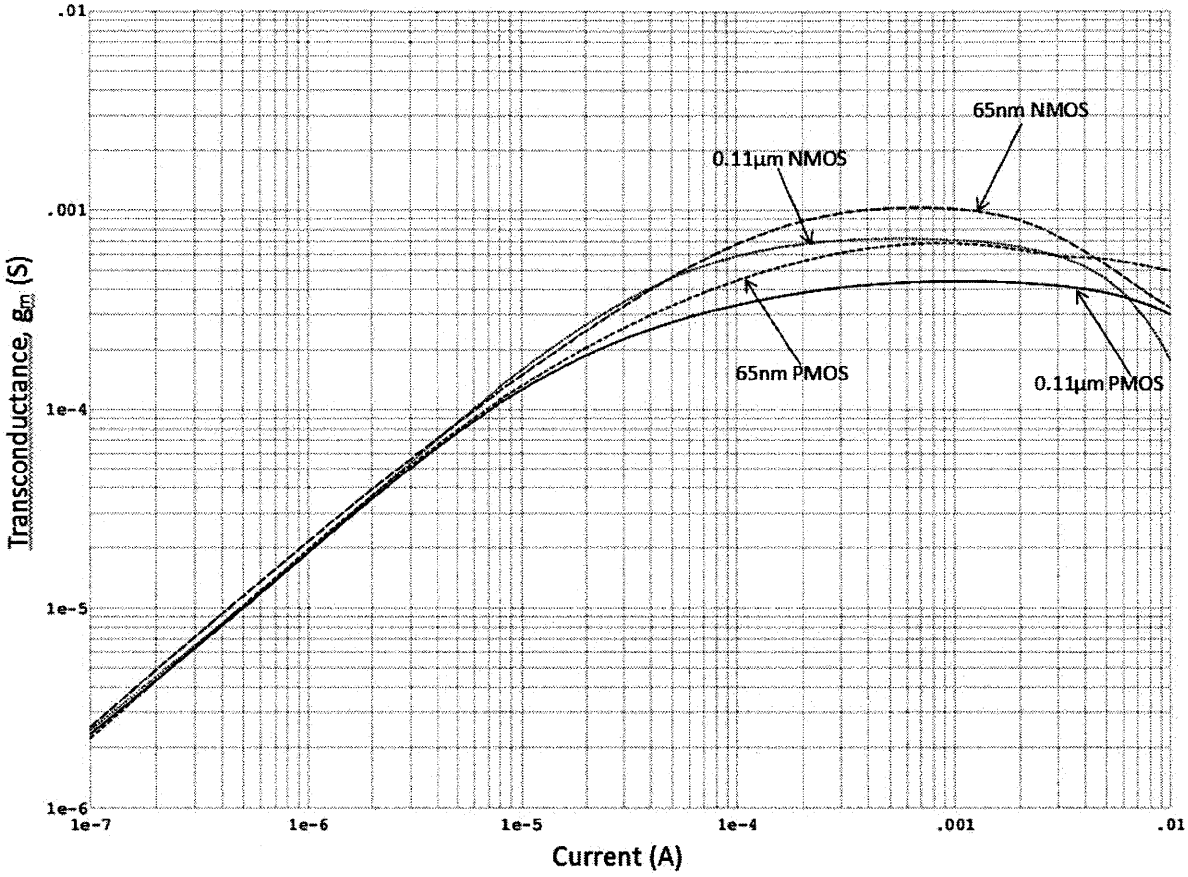


Figure 8: Transconductance versus current for the four devices; W=1µm for all, L= minimum length;

Above is a plot of g_m per width versus drain current per width of four transistors: 65nm NMOS, 65nm PMOS, 0.11µm NMOS, and 0.11µm PMOS. The length is the minimum allowed by each process (0.06µm for 65nm and 0.12µm for 0.11µm). There are two regions to be noted in the plot: weak and strong inversion. Weak inversion corresponds to the region with lower current (roughly less than 2e-5A), in which the MOSFET acts much like a BJT in that its transconductance varies linearly with current ($g_m \sim I/V_{th}$). During the period of weak inversion, the 65nm NMOS has the highest transconductance, although they are all quite similar. Later, once the slope of g_m becomes quadratic instead of linear (varies as the square root of current here), the transistor is operating in strong inversion. At currents

above 1mA, the transistor comes out of saturation and the transconductance can no longer keep increasing due to velocity saturation (however, we are not operating in this region so it is of no concern here). In the region of strong inversion, two trends can be seen:

a) 65nm devices on average have a higher transconductance given a certain drain current than 0.11μm devices (e.g. for 100μA drain current, 65nm NMOS g_m is 17% higher than 0.11μm NMOS g_m).

b) PMOS devices tend to have a lower transconductance than NMOS devices.

However, due to higher g_m for a given current, some of the transistors in the comparator, such as the input pair in stage 1, were biased in weak inversion. Therefore it is useful to see what the transconductance is in weak inversion (zooming into the above plot into g_m for smaller bias currents) in each of the four devices. The table below shows g_m/W for a 1 μA bias current (region of weak inversion).

Device	Transconductance per Width
65nm NMOS	0.022 mS
65nm PMOS	0.02 mS
0.11μm NMOS	0.02 mS
0.11μm NMOS	0.019 mS

These results have several implications for the comparator design port. First, the general trends are the same as in strong inversion, i.e. 65nm has higher trasconductance than 0.11μm, and PMOS has lower transconductance than NMOS. Why is this important? When ported to 0.11μm, the g_m will decrease (given the same W), and a higher width will be necessary to keep it the same. For instance, stage 1 of the comparator has PMOS input transistors, so the g_m of the input pair will decrease. Taking a look at the table above, we see

that g_m for 65nm PMOS is actually equal (in this case, otherwise very similar) to that of 0.11μm NMOS. This means that if we were to change the inputs to NMOS, this problem would be alleviated. The architecture in this case required a common-mode voltage of 0.25V for the inputs and thus PMOS inputs were required, but this may be something that can be changed in the future to provide a higher g_m. While this difference doesn't seem so great in the table above (0.02 mS versus 0.019 mS), these values correspond to a transconductance for a unit width, so with input devices of width 576 μm biased at 3 μA, the difference in g_m becomes 1.2 mS (23 mS versus 21.8 mS). While this is still a small difference, it may prove important in certain applications.

2.2 On-Resistance

The original comparator contains several reset switches and it is critical that these switches fully turn on to properly reset the comparator after each decision. Hence another parameter to consider when moving to 0.11 μm is the on-resistance of a MOS device. The smaller the on-resistance (Ron) of switch is, the closer to ideal that switch is considered to be.

In general, as W increases Ron decreases, while as L increases Ron increases. This trend can be seen by taking the case where W or L is doubled. When W is doubled, the transistor can be thought to be in parallel with itself (while it is in series with itself when L is doubled). This means that Ron is also in parallel with itself (R = 0.5Ron) in the case of 2W, and in series with itself (R=2Ron). Fig. 9 gives one example of this trend: Ron versus width for an NMOS device in 0.11 μm, confirming the trend that Ron decreases with increased width.

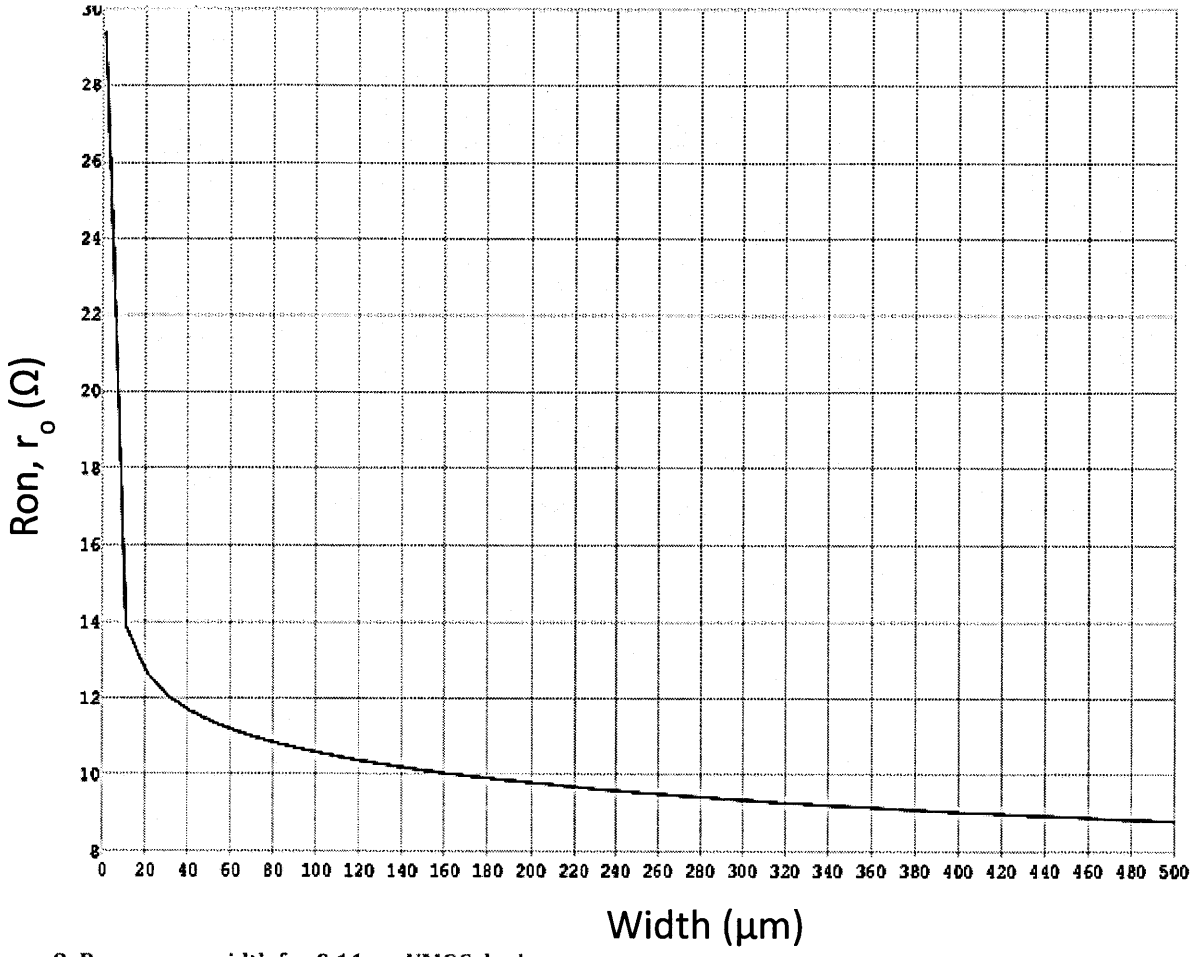


Figure 9: Ron versus width for 0.11μm NMOS device

The 0.11μm process switches have higher Ron resistance because minimum L was now increased (keeping W the same). While the case more often involves changing both W and L so these results cannot be used directly, we will be able to calculate the width required in 0.11μm to achieve the same Ron. This comes out to keeping the W/L ratio roughly the same: at W= 1μm, Ron was 0.7MΩ for 65nm NMOS (L=60nm), while it was 1.6 MΩ for 0.11 μm (L=0.12μm). This corresponds to a factor of 2.2 increase in Ron for a factor of 2 decrease in W/L.

2.3 PARASITIC CAPACITANCES

In MOSFETs, parasitic capacitances exist between the gate, source, drain, and bulk terminals. The ones of highest magnitude are most often Cgs and Cgd, and they will be of focus here. The reason for concern when dealing with high speed circuits is that these capacitances introduce more RC time constants (see equation) and slow the circuits down.

$$\tau = RC = \frac{1}{2\pi f_c}$$

The following table shows Cgs and Cgd for the four types of devices in saturation, each with W=1μm and minimum length (0.06μm or 0.12μm):

	65nm NMOS	65nm PMOS	0.11μm NMOS	0.11μm PMOS
Cgs	0.78fF	1.4fF	1fF	1.5fF
Cgd	0.32fF	0.34fF	0.32fF	0.25fF

While the parasitic capacitances are almost identical for W=1μm, it is important to note the percentage difference in Cgs: 28% increase for NMOS and 7% for PMOS. This means that especially for NMOS devices, the change in gate capacitance will be significant. For the purposes of the thesis, this implies that we will need to be aware of this difference and make sure the NMOS devices (such as the reset switches) are as small as possible to limit speed decrease in the comparator.

CHAPTER 3: 65NM COMPARATOR TOPOLOGY ANALYSIS

This chapter will analyze the comparator design provided by Analog Devices in 65nm. The comparator has three stages. The first two stages serve as preamplifiers and the final stage is a latch. Once basic operation and the limiting factors to speed, power and noise are known, they can be used in optimizing the design port to 0.11µm for maximum performance.

3.1 STAGE 1: INTEGRATOR

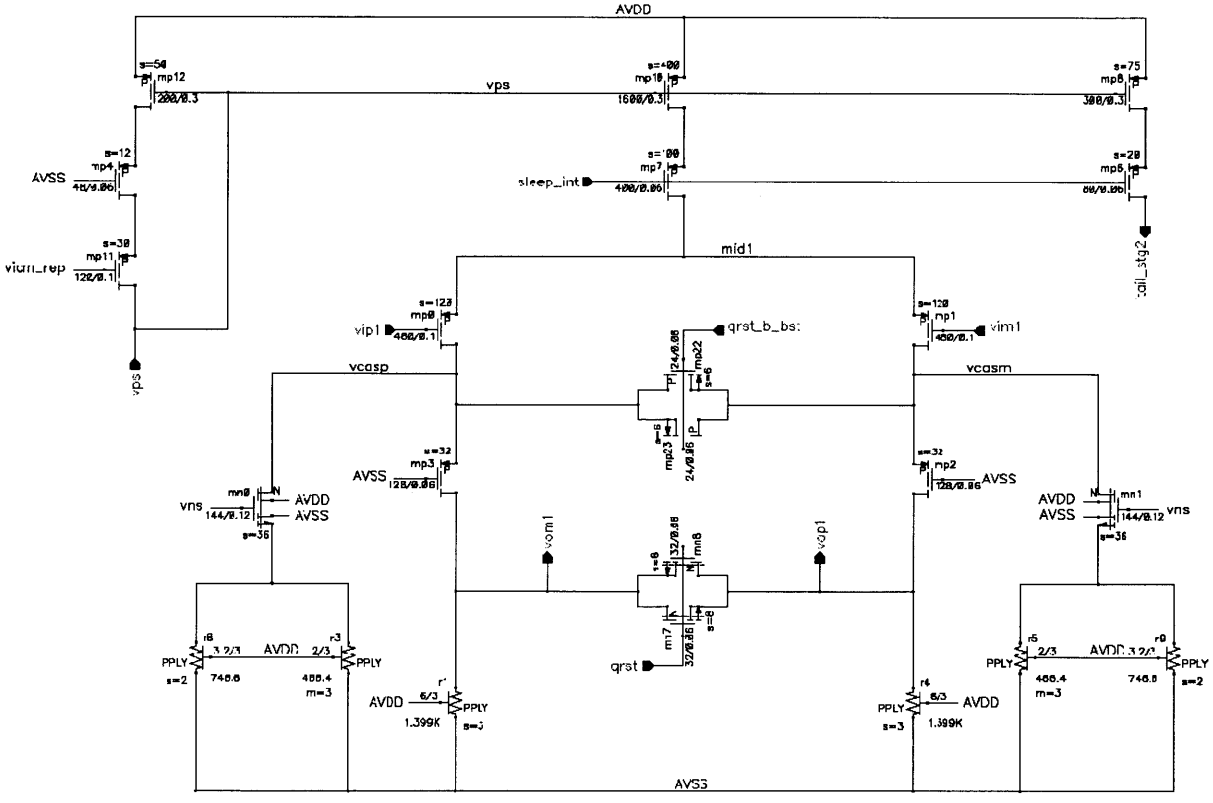


Figure 10: 65nm Stage 1

Basic Topology and Function

The first stage of the comparator is a differential amplifier that can be seen as acting as an integrator because the settling time period is significantly less than the load time constant ($t_{int} << r_{out} * C_{int}$). It was chosen to work as an integrator because of its higher power efficiency in achieving the same gain target within a limited time, compared to a traditional wide-band amplifier. While the circuit does not contain an explicit capacitor on which to integrate, the input capacitance of the next stage acts as this capacitor. A cascode stage is added in to increase the output resistance of the amplifier, and therefore the DC small-signal gain $g_m * r_{out}$. In addition to this, a current stealing technique is applied at the source nodes of the cascode devices. This allows for less current to flow through the load, decreasing the headroom required and thereby decreasing the noise of the load. Current stealing allows for only ~1/8 of the bias current to flow through the loads, and a large resistor could be used instead of active one to achieve the same gain.

Speed – gain in a given amount of time

The voltage gain was approximated to be

$$\text{Gain} \approx \frac{g_{m,input}}{c_{int}} \circ t_{int}.$$

To figure out why this is so, let us first look at the current flowing out of stage 1. The output current of stage 1 is determined by the transconductance of the input pair, g_m, times the differential input voltage:

$$i_c = C\frac{dv_{out}}{dt} = g_m v_{in}$$

Taking the integral on both sides:

$$Cv_{out} + C_o = \int g_m v_{in} dt$$

C_o is 0 because the capacitor is initially discharged and v_{in} is a constant input in this case, therefore:

$$g_m v_{in} t_{int} = Cv_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{C} t_{int}$$

Because the amplifier needs to achieve a certain amount of gain to overcome offset in the latch, in order to achieve high gain for a given capacitance, we must increase either g_m or t_{int}. In order words, the larger the capacitance on the output, the larger either the input pair transconductance or the integration time needs to be to achieve a certain gain.

Noise Analysis

The noise in the first stage integrator can be separated as coming from discrete noise sources such as the input pair, cascode devices, and resistors. The noise contribution of the input pair is greater than that of the load resistors [2], and as will be shown below, the cascode devices also contribute negligible noise. The input pair noise of an integrator is derived to be the following:

$$\boldsymbol{E[v_{n,}^2] = \frac{16}{3}\frac{kT}{g_{m,in}}\frac{1}{2}t_{int} = \frac{4kT\gamma}{g_{m,in}t_{int}}}$$

where $\gamma = \left(\frac{2}{3}\right)$ is the noise factor [2]

The derivation of this noise voltage comes from realizing that the input pair of the integrator provides noise according to the noise voltage model of a MOSFET times the noise bandwidth (NBW). The noise current of an integrator is defined as:

$$\boldsymbol{E[i_{n,MOSFET}^2] = 4kT\gamma g_{m,in}}$$

In order to obtain noise voltage from this current, we divide by $\boldsymbol{g_{m,in}}^2$ (since $v^2 = i^2 * R^2 = \frac{i^2}{g_{m,in}{}^2}$) in order to obtain:

$$E[v_{n,MOSFET}^2] = \frac{4kT\gamma}{g_{m,in}}$$

Next, the noise bandwidth in an integrator has been shown to be:

$$NBW = \frac{1}{2 \cdot t_{int}} \; (NBW = noise\ bandwidth, t_{int} = integration\ time)\ [12]$$

And therefore, the total noise voltage in the integrator (with a factor of 2 to take into account the differential nature of the input) becomes:

$$E[v_n^2] = \left(4kT\gamma \frac{1}{g_m}\right)(2) \cdot NBW$$

$$\therefore \boldsymbol{E\left[v_n^2(t_1)\right] = \frac{4kT\gamma}{g_m t_{int}}}$$

What design intuition does this noise equation give us? The first point to note is that the noise voltage does not depend on the integrator's capacitance. Therefore, to get maximum speed, it makes sense to use as small a capacitor as possible (thus it makes sense that no external integrating capacitor is added to the output). Second, the higher the transconductance, the lower the noise voltage power will be. Finally, integration time is inversely proportional to noise voltage, but since we have a limited total integration time t_{int} (not to be confused with the time constant) we don't have much room to alter this value.

Therefore, the trade-off presented by this equation is between power and speed: how much input pair transconductance is required to achieve a certain noise given an allowed time specification.

Moving onto the cascode devices, their noise is negligible because the noise currents in these devices cycle through them instead of flowing out to the resistor to contribute to the total noise voltage (see Fig. 11).

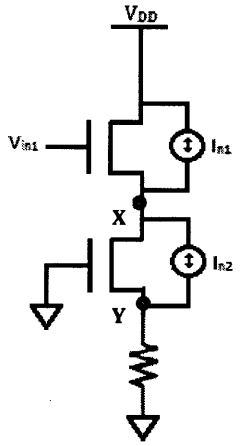


Figure 11: Model of input and cascode transistor on one side of the first stage, including each noise current

From between the two transistors at node X, $r_{out}=1/g_{ds}$ can be seen looking up, and $1/ g_m$ can be seen looking down. Because, $r_{out}=1/g_{ds}$ is on average much larger than $1/ g_m$, the noise current of the input transistor, I_{n1}, travels down through the cascode transistor, finally to go through the transistor and contribute to the overall noise voltage. I_{n2} however, makes the same choice and travels up to the midpoint and back down into itself. Once it travels back down through the cascode device, I_{n2} can't go down through the load resistor because of KCL at node Y: if there is a current source I_{n2} going up, none of it can travel through R. Instead it must instead keep cycling around itself, and because of this, I_{n2}'s effect can be considered negligible.

To summarize, the key factors to look out for in the design port of stage 1 are transconductance (maximizing it in order to minimize noise) and parasitic capacitances on the output.

3.2 STAGE 2: PREAMPLIFIER

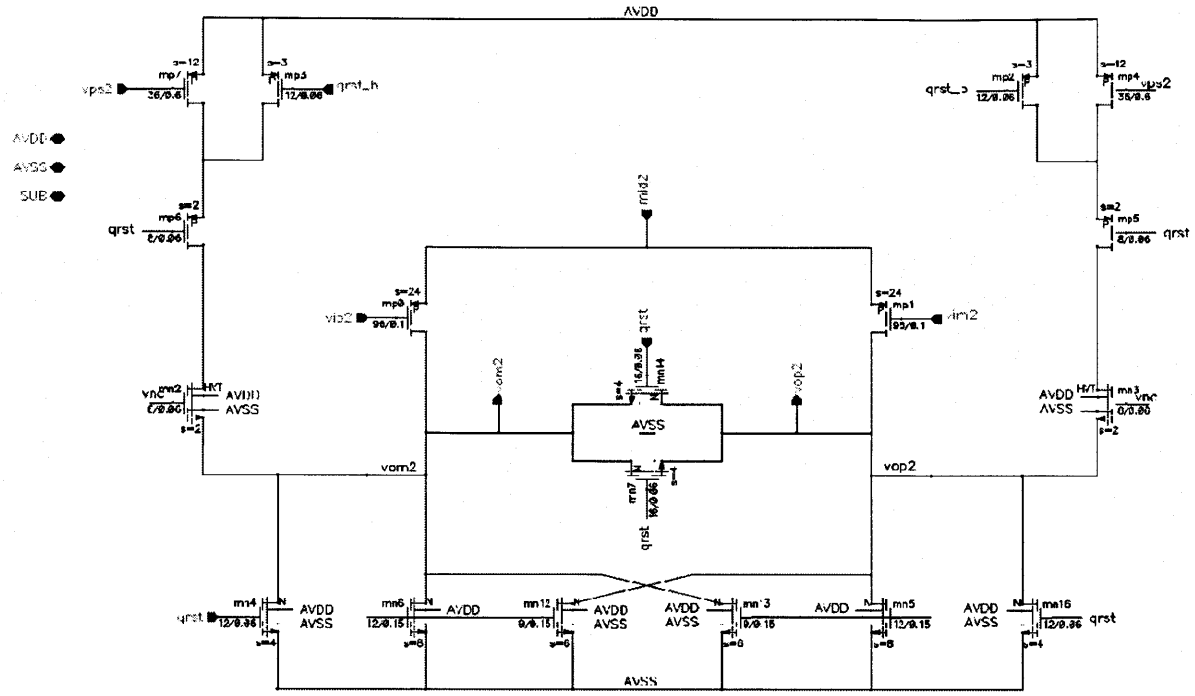


Figure 12: 65nm Stage 2

Basic Topology and Function

The second stage in this comparator is a more traditional amplifier, whose function is to provide a bit more gain and to set up the bias voltage for the inputs to the 3rd stage. Because the majority of gain is provided by the first stage, this stage does not require a cascode device. The loads are realized through cross-coupled diode loads. At the beginning of the amplification phase, the cross-coupled loads are off, because they have to be charged up to V_{gs} before they can turn on and provide a load impedance.

Gain

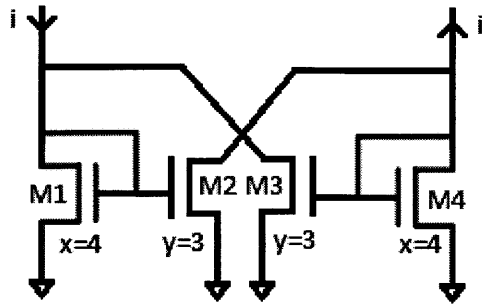


Figure 13: Model of Stage 2's cross-coupled devices

The approach taken here to derive gain in the second stage involves analyzing the current gain provided by the cross-coupled devices (shown in Fig. 13). X and Y correspond to the relative multiplicative factors of W in each transistor. For instance, if M2 and M3 had W=9=3*3, in order to fulfill the X/Y ratio in the figure, M1 and M4 would have to have W=12=4*3.

Taking a step back to calculate current gain given any X and Y:

KCL applied:

$$i = i_1 + i_3 \qquad \boldsymbol{-i = i_2 + i_4}$$

$$\boldsymbol{i_1 = \frac{x}{y} i_2} \qquad i_4 = \frac{x}{y} i_3$$

$$\boldsymbol{i_1 = -i_4} \qquad i_2 = -i_3$$

Using the bolded equations above:

$$i = -i_2 - i_4$$

$$i = -\frac{y}{x} i_1 + i_1$$

$$i = i_1 \left(\frac{x-y}{x}\right) \rightarrow \boldsymbol{\frac{i_1}{i} = \frac{x}{x-y}}$$

For the X/Y dimensions in the figure above (dimensions in original design) the current gain is 4, and therefore the overall gain of the stage is 4x the gain from the input devices ($g_m/C*t_{int}$).

Noise Analysis

Noise in the second stage can be divided into that coming from the input pair, and that coming from the loads.

The noise analysis for the input pair can be found similarly to that of the one in stage 1. The only difference from the one found in stage 1 is that now the noise voltage is referred to the input and therefore we divide $E[v_n^2(t_1)]$ by the gain squared (since we are dealing with powers).

Therefore, dividing by $(\text{Gain}_{Stage\ 1})^2$ we get:

$$\therefore E[v_n^2(t_1)] = \frac{4kT\gamma}{g_m t_{int}} \frac{1}{(\text{Gain}_{Stage\ 1})^2}$$

Intuitively, this means that the noise voltage coming from the input pair will be significantly lower than it was in the first stage. With the DC gain in the first stage designed to be around 20, the noise voltage power of the input pair is $1/400^{th}$ of that in the first stage.

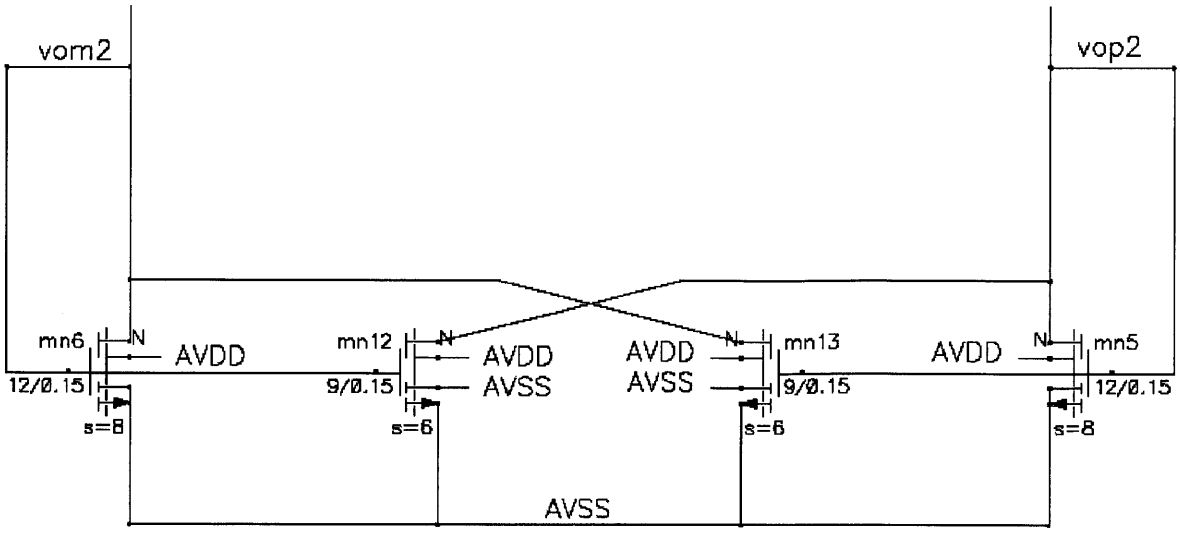
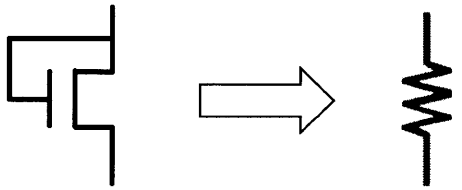


Figure 14: Stage 2 Close-up of Cross-coupled loads

The noise coming from the loads can analyzed by first expressing a diode connected transistor as a $1/g_m$ resistor (in this case mn6 and mn5), and amplifying its noise current by the current gain provided by the cross-coupled devices (mn12, mn13), 4x in this case.



$$v_R^2(f) = 4kTR \approx \frac{4kT}{g_m}$$

$$I_R^2(f) = 4kTg_m$$

Therefore the total noise in this stage is this noise current multiplied by the current gain:

$$I^2 = 16kTg_m$$

Because the loads are not on at the beginning of the amplification phase, not all of the noise calculated above is actually seen by the comparator.

3.3 STAGE 3: LATCH

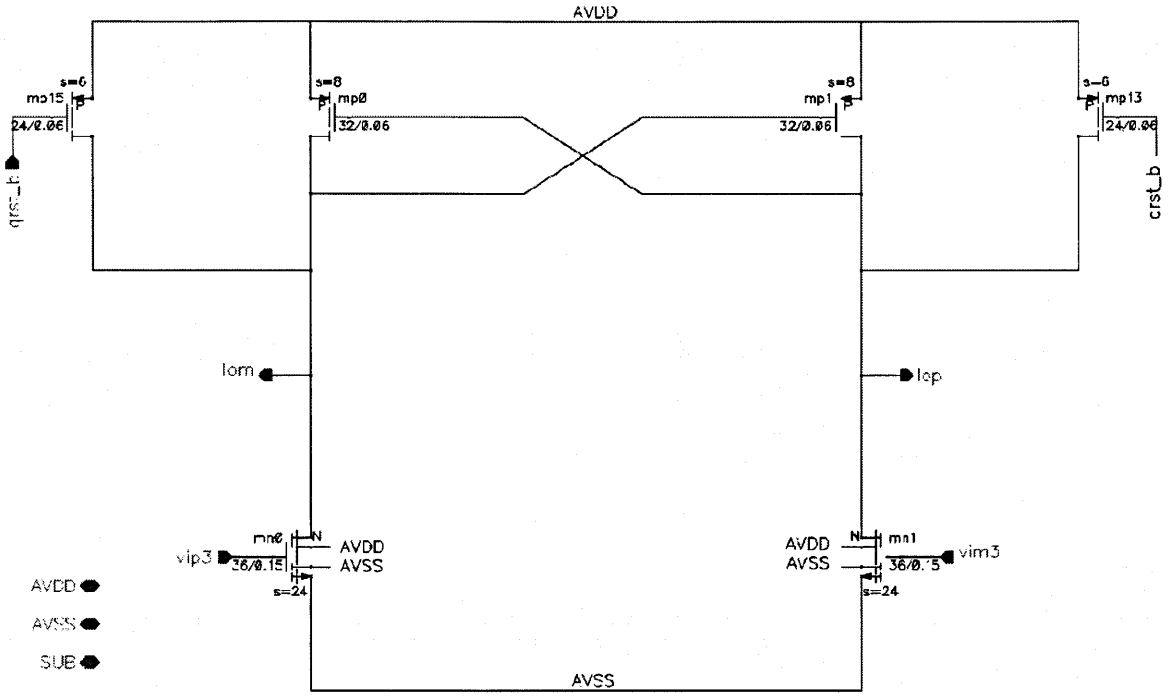


Figure 15: 65nm Stage 3

Basic Topology and Function

The regenerative latch represents the third stage of the comparator. It includes a grounded source NMOS input pair, and cross-coupled PMOS loads. During reset, the outputs are tied to V_{DD}, while the gates of the input pair are tied to ground (from the previous stage), allowing no current to flow through the stage at this time. During the decision phase, as the inputs of the latch increase to above V_{TH} (of the NMOS input pair), the input pair devices turn on, discharge the output nodes, and turn on the PMOS loads, beginning regeneration.

Offset is one of the biggest limiting factors in the latch. It can be on the order of 1-5 mV, which is larger than RMS noise in most designs. In addition to this, the latch needs to be run in over-drive by a certain amount, or else it will take a very long time to achieve a certain logic level. The topology of the latch is largely limited by the 65nm process. Due to the high V_{TH} (higher than in 0.11μm) of the devices and the low 1.2 V +/-10% supply, back to back inverters seen in many conventional latches [source] are not feasible because there is not enough headroom and the devices will go out of saturation.

Noise Analysis

Noise in a typical regenerative latch has been derived to be the following using stochastic differential equations [3]:

$$E[v_n^2] = \left(\frac{4kT\gamma g_m t_{int}}{C^2}\right)\left(e^{\frac{2t_{int}}{\tau}}\right) \text{ where } \tau = \frac{C}{g_m}$$

While this equation is quite complex, intuitively there are two reasons why the latch contributes very little noise to the comparator. First, by the time the noise is referred back to the input, the gain in the first two stages is high enough that it diminishes its magnitude. Second, since the load devices of the second stage feed directly into the latch and they are shorted to ground during the reset period, the input pair of the latch isn't on during this time so its noise contribution is cut down even further.

It is important to note that offset is also an issue in comparators, and especially the latch. For applications such as this one, however, the DC offset was considered to be able to calibrated for afterwards, and was thus not a design consideration in this thesis.

CHAPTER 4: DESIGN PORT

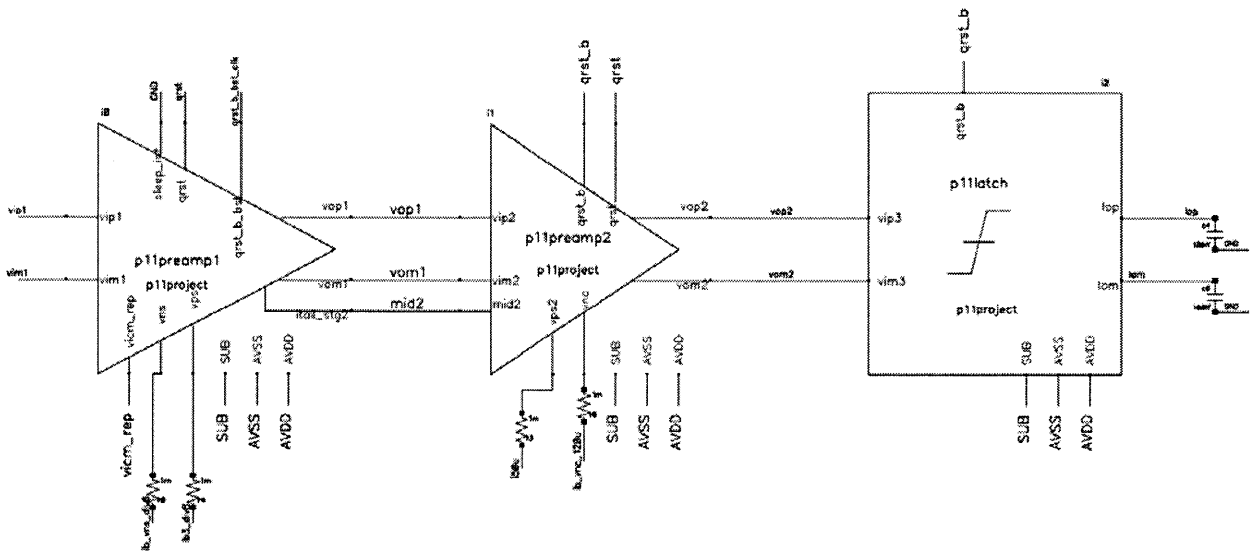


Figure 16: 0.11µm Comparator

In considering how to port the design of this comparator from 65nm to 0.11µm, a general methodology is first introduced. When deciding how to size a transistor from the 65nm comparator to 0.11µm, the following three steps were attempted in order:

1. **Keep W/L ratio the same**
2. **Without changing current –**
    1. *If speed is too low* –
        1. Decrease load capacitances by making switches smaller
    2. *If speed is high enough, but not resetting properly* –
        1. Make reset switches larger at cost of speed

3. *If gain is too low or noise too high –*

    1. Increase g_m of input pairs by increasing the size of devices

3. **If performance still sub-par to 65nm –**

    1. Consider increasing the current, and therefore the power of the circuit

The port was done stage by stage, at each checkpoint measuring performance by comparing to that of the 65nm synonymous circuits. Each stage was optimized first for speed, then for noise and power. Speed was measured as gain observed given a certain amount of time to settle. The input of choice here is 640 μV, determined to be one of the hardest inputs for the comparator to decide on. "DC gain" means the maximum gain achieved given unlimited time allowed for settling. In the charts to follow, "W/L same" corresponds to leaving the ratio of W/L of all transistors in the stage equal to that of their 65nm counterparts, and Switches/In_pair "#W" correspond to increasing the width in the specified transistors by a factor of #. Results are grouped as follows: stage 1 alone, stage 1 and 2 together, and finally all three stages together. Therefore, each builds on the achieved performance of the last.

4.1 Design Port + Performance of Stage 1

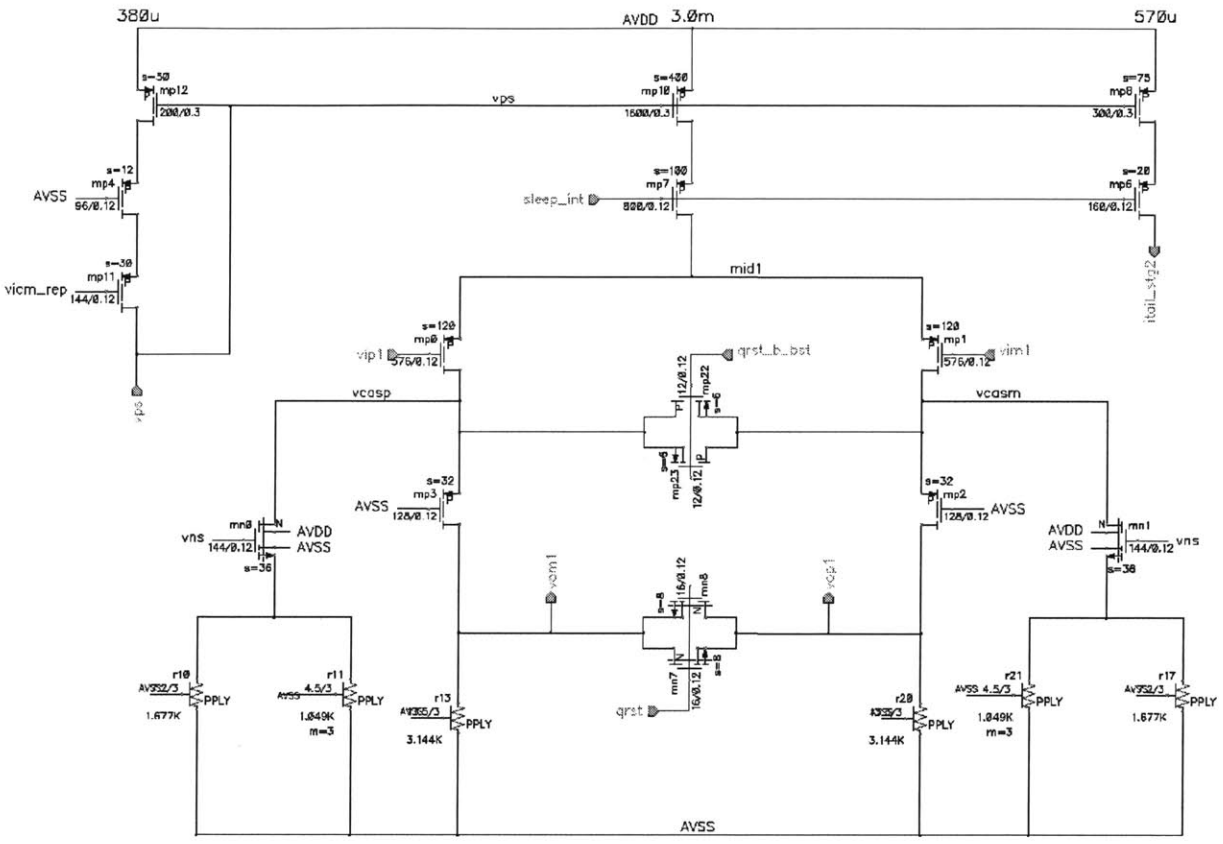


Figure 17: Final Dimensions of 0.11µm Stage 1

Changes	Gain in 300ps	~DC gain
65nm Control	12.99	20
W/L same	6.43	21
Switches 1/4W	**9.36**	**23**
In_pair 2W	8.79	24
In_pair 1/2W	8.95	21
Cascode_pair 1/3W	**13.26**	**22**

As seen in the chart above, Stage 1 in 65nm achieves a gain of nearly 13 in 300ps, while the ported stage 1 when W/L is kept the same is only 6.43 (~50% slower). In order to increase the speed, the reset switch Width was quartered, bringing the gain to 9.36. The change of input pair width did not affect the gain significantly, so it was left the same. Finally, decreasing the cascode pair width by a factor of 1/3 increased the gain to 13.26, higher than stage 1 in 65nm.

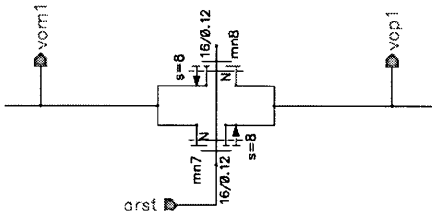


Figure 18: Close-up of Switches in 0.11µm Stage 1

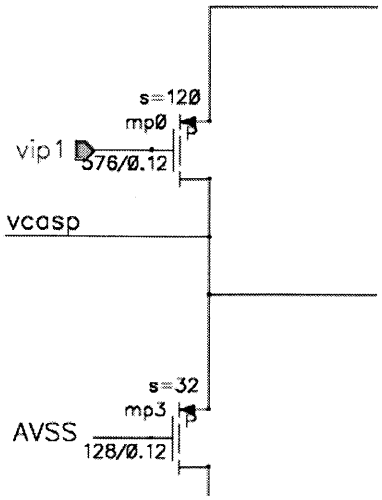


Figure 19: Close-up of Stage 1 input-pair in 0.11µm

First, running through a few hand-calculations it makes sense that quartering the reset switches had the effect of increasing speed, because the reset switches' Cgs and Cgd capacitances have gone down by a factor of 4, bringing the overall parasitic capacitances down by a factor of approximately 20%. Taking the slope or gm/C to be the speed of the decision with $g_m \approx 20mS$, the speed increased roughly 30%. The actual % increase in speed from 6.43 to 9.36 is ~45%, and while the hand-calculated capacitances do not give the whole picture of the speed increase, they begin to give us a clue.

Next, let us investigate why the speed did not increase when the input pair width was doubled. One of the hypotheses from the design of the stage was that if g_m was increased, the speed would also increase (slope is g_m/C). The first observation is that doubling the width of a device does not double its g_m (as would be expected given the formula for g_m in saturation is proportional to the square root of width). In fact, g_m only increased from 25.9 to 28.8 mS, an increase of roughly 10%. Despite this, given our

integrator model of speed as g_m/C, the speed should have increased at least a bit. The most probable reason this didn't occur involves the size of the switches. As we saw in the process characterization chapter, as the width of a transistor increases, the output resistance decreases. Doubling the width to 1152 must have dropped the input pair's output resistance, R_{DS} to a level comparable to the $1/ g_m$ that can be seen looking down into the source of the cascode pair (see Fig. 20). At this point, some of the drain current of the input transistor goes back into itself as opposed to traveling down through the cascode. This means that not all of the g_m is seen at the output, and the benefit of speed increase is no longer seen. As a quick math check, g_m of the cascode device is roughly 19.2mS, meaning $1/ g_m \sim 52\Omega$. In comparison, R_{DS} for W=1152 is projected to be less than 5kΩ. While this is still much higher, it is much closer to $1/ g_m$ than at W=576, where $R_{DS} \sim 10k\Omega$.

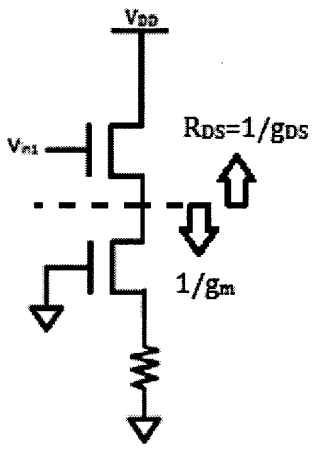


Figure 20: Resistances looking up and down between the input and cascode devices of Stage 1

Finally, the fact that decreasing cascode width by 1/3 gave a 40% speed increase should come as no surprise, because the cascode capacitance Cgd can be seen at the output. Running the same hand-calculations as above for the case of the switches, this decrease in cascode width corresponds to about a 30% decrease in capacitance on the output. Checking speed as g_m/C with $g_m \sim 19.2$mS (assuming that the change in g_m was not large, based on the small change in g_m for input pair width change), the theoretical speed increase is approximately 38%, confirming the trend.

In terms of minimizing noise, the strategy was to keep the input pair g_m as large as possible.

The first stage's static current is set by a current source to be 1.5mA, and therefore changes to the device sizes did not change the overall current running through them. Because the aim in this project was not to optimize power but to match the previous spec, this was a satisfactory result.

4.2 Design Port of Stage 2, Performance of Stages 1 + 2

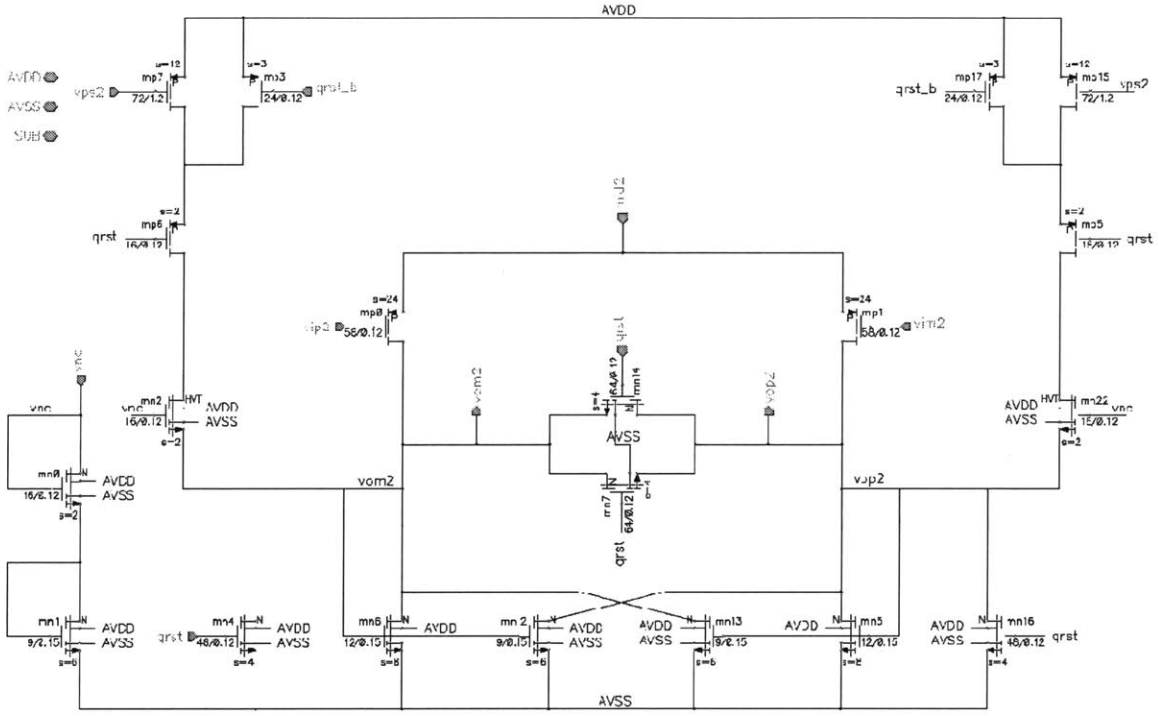


Figure 21: Final Dimensions of Stage 2 in 0.11um

Changes	Gain in 400ps	~DC gain
65nm Control	26.2	66
W/L same	16.7	66
In_pair 1/2W	**19.6**	**64**
Switch to gnd 2W	**19.6**	**64**

In 400ps, the 65nm stages 1 and 2 simulated together achieved a gain of roughly 26. At the same W/L ratio, the 0.11um stages could only reach a gain of roughly 17. Similarly to

stage 1's input pair the original strategy for the input pair was to keep it as large as possible (maximizing g_m achieved was 18, in comparison to 23 seen in 65nm). However, since it is directly connected to the output of stage 1, the input pair of stage 2 now added significant parasitic capacitance of about 300fF slowing down the circuit. In order to alleviate the parasitic capacitance, the in_pair width of stage 2 was cut in half, increasing speed by 17%. The switches to ground were made twice as wide as their 65nm counterparts in order to ensure proper resetting. This did not contribute to a loss in speed because these switches were smaller to begin with, and did not contribute as much to the overall capacitance on the output.

4.3 Design Port of Stage 3 and Performance of All Stages Together

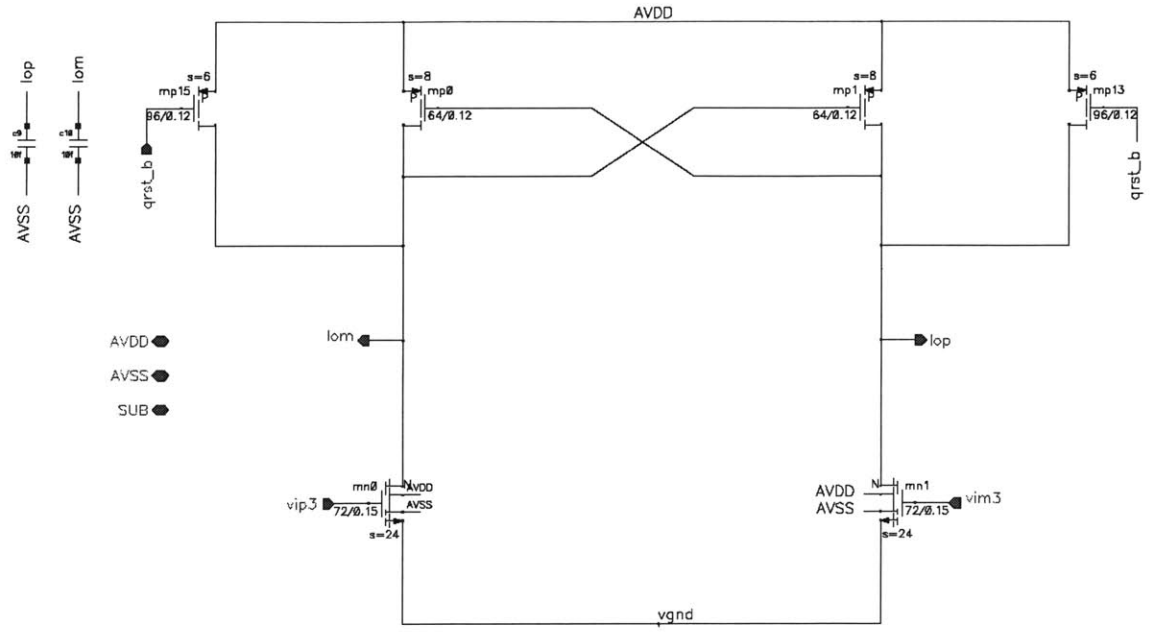


Figure 22: Stage 3

With equal W/L ratio as the 65nm comparator, the speed of the 0.11μm comparator was 20% lower, while the noise and power were within 2% of each other. In order to match speed the current in the latch was increased by doubling the width of the input pair. This increased the overall power in the system by 11%.

4.4 Results

	Speed	Noise	Power
65nm	510ns	70.7uV rms	**5.4mW**
0.11um	510ns	**61.6 uV rms**	6mW

"Speed" here is defined as the time it took for the output of each comparator to reach 0.6V, or the middle of the voltage range. It shows that the speed being the same, the noise in

the 0.11um comparator was 12.8% lower while the power was 11.1% higher. Given this trade-off between noise and power, a choice of process can be made depending on the application involved.

Another trade-off seen is the one between speed and power as well, but given the overall SAR system, speed was a limiting factor in the group's design whereas power ended up less than budgeted for (10mW spec), so the increase in power was acceptable.

The following chart describes the major noise sources of the system:

Noise Source	% of total (0.11μm)	% of total (65nm)
Preamp1 in-pair	45.4%	44.6%
Preamp1 resistors	12%	13.6%
Preamp1 switches	11.6%	12.4%
Preamp1 cascode	9.8%	8%
Preamp2 in-pair	4.8%	7.8%
Preamp2 switches	3.2%	0.06%

As expected, the majority of noise came from the first stage's input pair, followed by the other major components in that stage. It can also be seen that the noise contributions by component are similar between the processes.

CHAPTER 5: NEW ARCHITECTURE

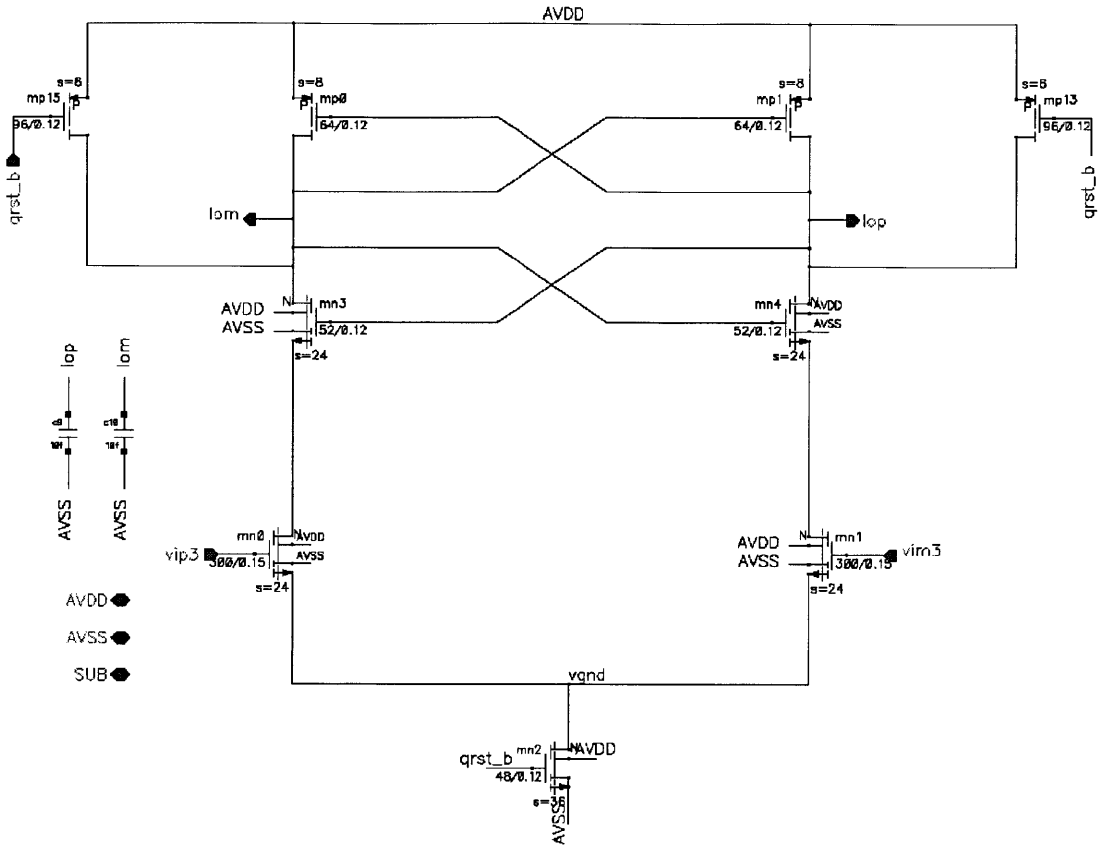


Figure 23: New Latch-only Architecture

Recent common comparator implementations for SAR ADCs in literature involve only one stage: the latch. This served as motivation in this thesis to implement the comparator in 0.11µm as only one latch stage. Fig. 24 shows an implementation from a 2009 paper [8], which was followed in this thesis.

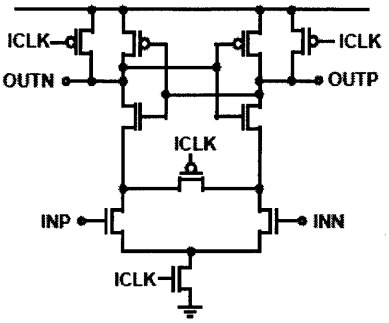


Figure 24: Implementation of Latch-Only Architecture [8]

There are benefits as well as drawbacks to using a single latch stage as opposed to three stages. Because there are fewer components, a latch only comparator will be significantly lower in power and faster in making its decisions. However, the latch also expects

to be of higher noise and offset (no preamplifier stages to reduce input-referred noise), and the input is not protected from kickback charge. Offset compensation will definitely be necessary if a latch-only architecture is used, because the amplifiers that were previously used to amplify the input signal to beyond the offset are no longer present.

One difference in the processes that allowed for the above implementation of the latch (as opposed to the 65nm latch) was the lower V_{th} in 0.11µm. Lower V_{th} allowed for the stacking of an extra pair of transistors in the latch, making it a true coupled-inverter system.

OVERALL RESULTS

	Speed	Noise	Power
65nm	510ns	70.7uV rms	5.4mW
0.11um	510ns	**61.6 uV rms**	6mW
0.11um latch only	**300ns**	70.8uV rms	**1.49mW**

As the table above shows, the new latch only comparator achieves 40% higher speed, approximately equal input referred noise as the 65nm comparator, and 72% lower power than the 65nm comparator. As mentioned before, however, offset in the latch will be the limiting factor when deciding which topology to use.

CHAPTER 6: CONCLUSION AND FUTURE WORK

This thesis presents the design port of a three stage SAR ADC comparator from 65nm to 0.11μm, as well as a new comparator architecture in 0.11μm. The performance of the comparator in 0.11μm (especially the latch-only architecture) shows promise that the 0.11μm process is one worth going to for this specific application. The 0.11μm design port confirmed a trade-off between noise and power, i.e. the correlation between more power (e.g. higher g_m) and lower overall noise, due to the noise voltage power's inverse relationship with g_m. Another trade-off was the one between power and speed – in order to achieve the same speed at the larger process node, the comparator (latch stage) needed to burn more power.

The decision to move to the 0.11μm node will most probably stem from a business perspective more than a technological limitation – whether other parts of the chip in question also benefit from being in 0.11μm.

There are many questions left to answer in future work. What happens with different process skews? Does the system still meet specs? Why is the noise in the latch-only comparator not significantly higher than the one in 65nm? Is there a hidden trade-off that has not been looked at in this thesis? In addition, mismatches in devices were not taken into account here, so a further look into the offset of the comparator would be useful to decide whether or not it is tolerable or requires background calibration.

CHAPTER 7: APPENDIX

Simulations were separated into three main areas: testing for speed/accuracy, testing for noise, and testing for power. Testing for power consumption involved taking time averages of the instantaneous currents flowing through the devices and due to its calculation-based nature is not featured here.

7.1 TESTING FOR SPEED/ACCURACY: HYSTERESIS ANALYSIS

The hysteresis test seen below served as the major examination tool in this thesis, which involves switching between two inputs at a certain period (2ns here for convenience) and taking a look at the output. This test provides dual benefit in that it checks whether the switches in the comparator allow it to reset properly, and also lets us compare the slope (aka speed) of the decisions.

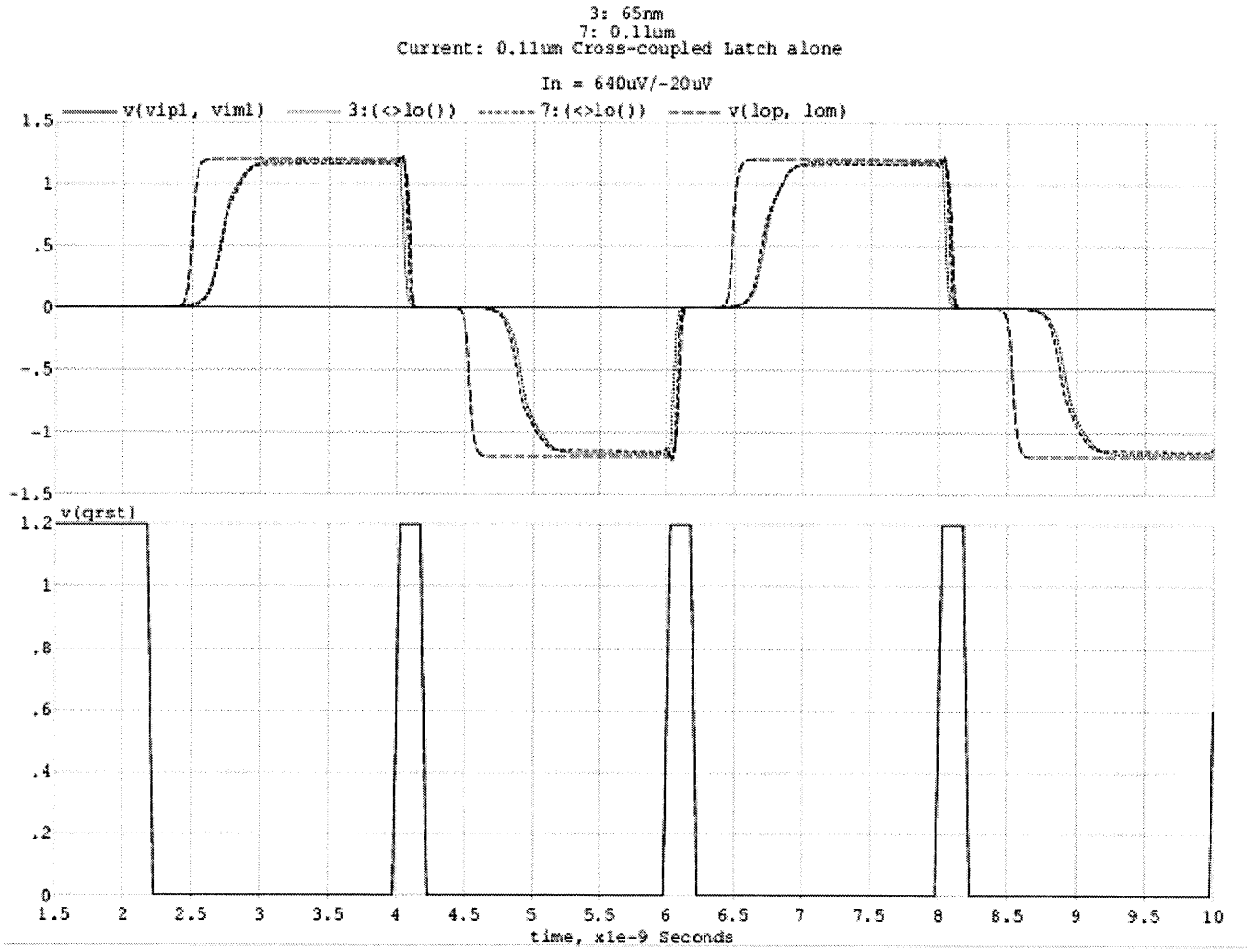


Figure 25: 640μV/-20μV Hysteresis test for three comparator types

The two figures here compare the performance of the original 65nm comparator, the direct design port in 0.11μm, and the new simplified architecture in 0.11μm. The two sets of inputs, 640μV/-20μV and 20mV/-160μV were chosen to simulate the hardest sequence of decisions the comparator would have to make, in order to test whether it resets properly and there is no memory from the previous decision to affect the new one. For example, with an input as high as 20mV, the comparator would regenerate very quickly to 1.2V, and so the next input of -160μV would seem like a very subtle difference from 0 compared to 20mV. As can be seen in both figures, the new architecture employing only a latch clearly made a decision (increased to 1.2V or -1.2V) much more quickly than both of the other comparators.

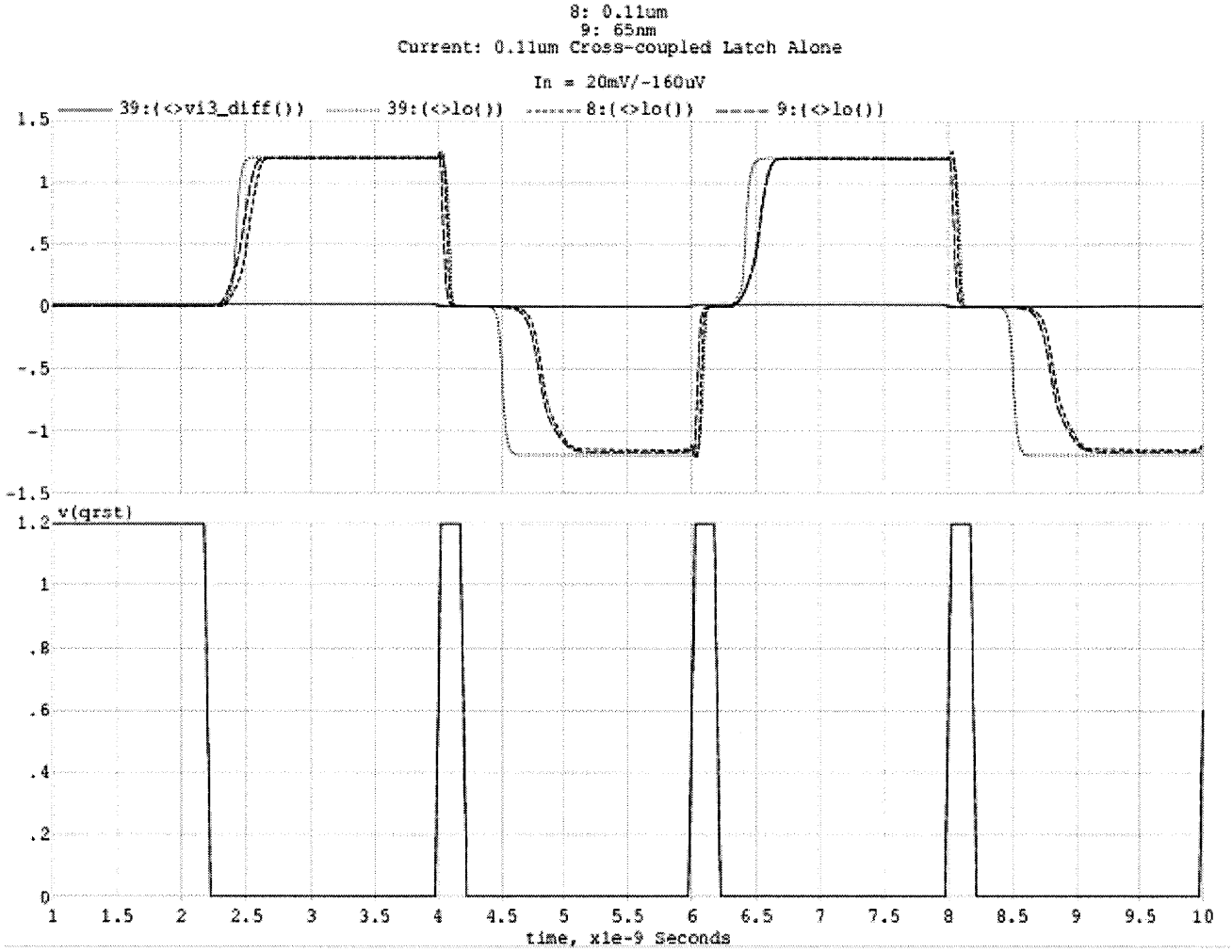


Figure 26: 20mV/-160µV Hysteresis test for three comparator types

7.2 Noise Analysis: Spectre RF

As mentioned before, noise in the comparator is different from steady-state noise in most circuits due to its transient nature. Instead of linearizing a circuit about a single operating point, comparators require a whole period to be taken into account. For this reason, SpectreRF software was used because of its ability to provide periodic steady state (pss) and periodic noise (pnoise) analysis. Essentially SpectreRF linearized the comparator circuit around a period and used this period as a periodically time-varying operating point.

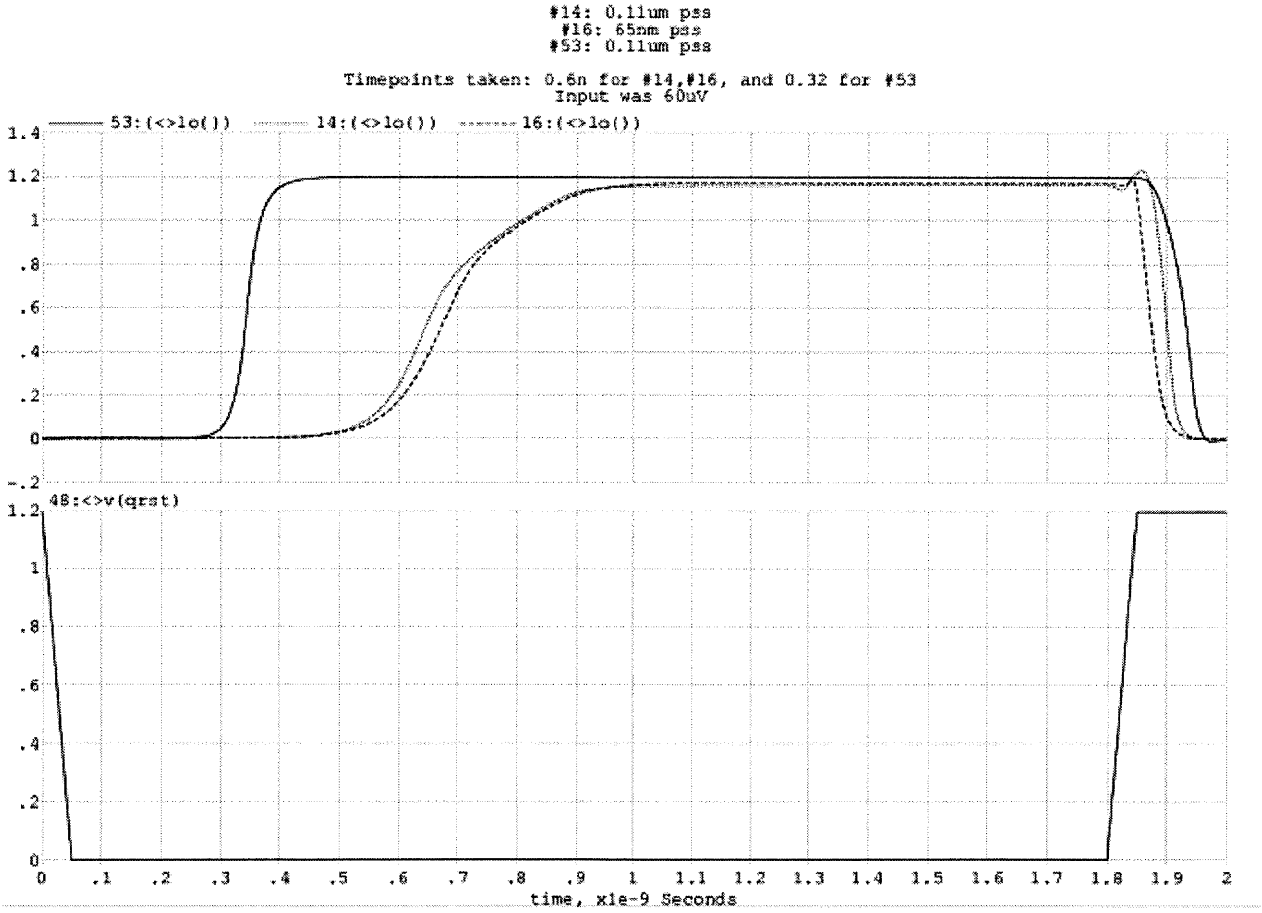


Figure 27: SpectreRF pss analysis

Fig, 27 shows the pss analysis run in order to find one period within the comparator's run time. The original 65nm comparator, the direct design port in 0.11μm, and the new simplified architecture in 0.11μm are again compared here for one period, and it is easy to

see how much faster the simplified architecture in 0.11μm is. Fig. 29 shows the noise power of the three circuits. The noise is being integrated with frequency, so the last point of each plot is the actual noise power. The plots are misleading because in order to find input referred noise we must divide the values we see in the figure by each comparator's gain. The table on the next page shows the noise power (as read from Fig. 28), each circuit's gain, and the ratio of noise power/gain, or input-referred noise. We see that the circuit with lowest input-referred noise actually comes out to be the 0.11μm design port, even though in the figure it is the highest curve.

	Noise power	Gain	Input-referred noise
0.11um comp	245.6mV rms	4000	**61.6uV rms**
65nm comp	201.5mV rms	2840	70.7uV rms
0.11um latch	177.73mV rms	2500	70.8uV rms

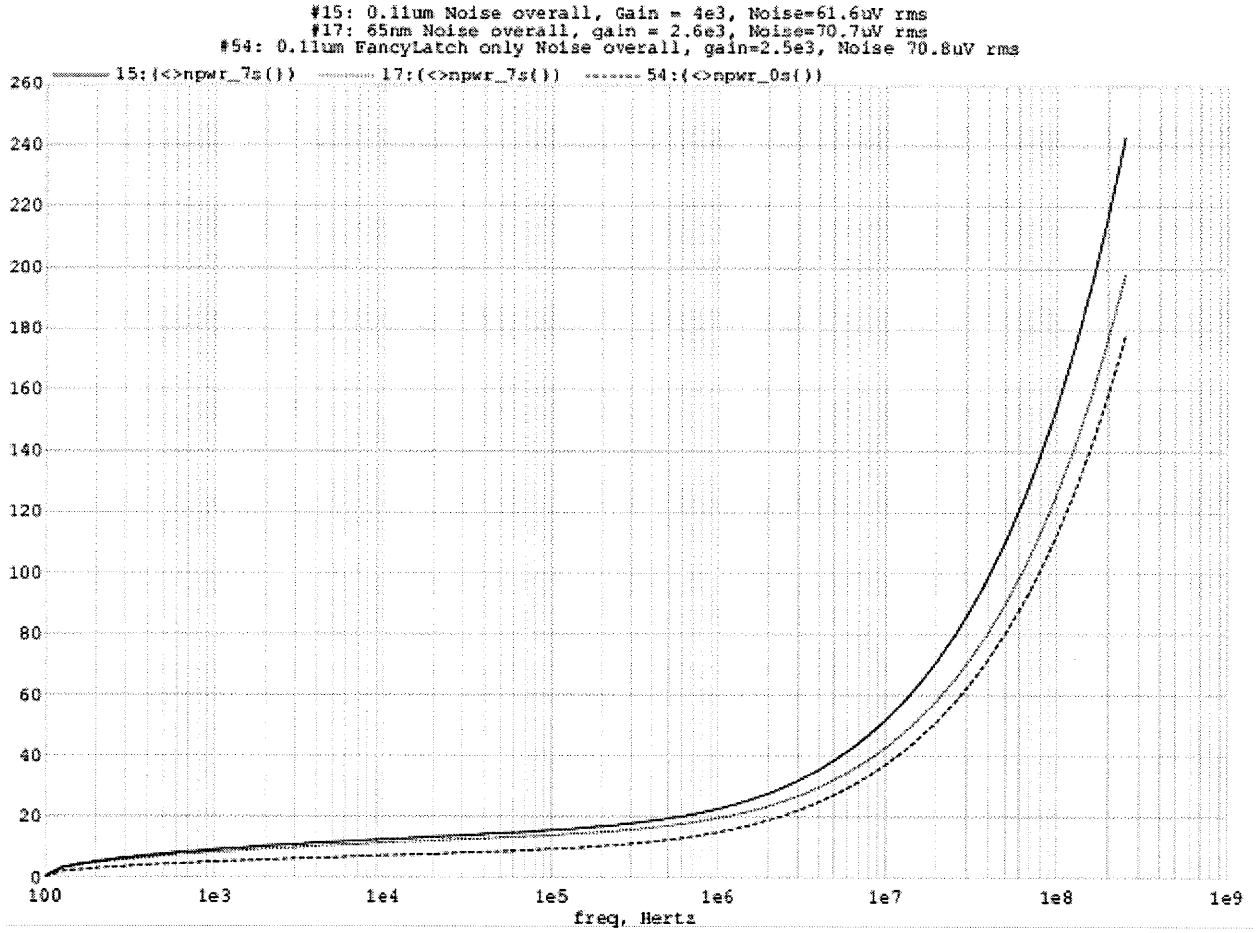


Figure 28: SpectreRF pnoise analysis

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