Thermally Actuated MEMS Seal for Vacuum Applications

by
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Abstract

This thesis presents the design, fabrication and testing of a new, leak-free, permanently sealable MEMS valve for use in vacuum applications. This device is different from existing MEMS valves in that it is leak-free in the closed state and has a relatively high flow rate in the open state.

This device relies on the surface tension of a molten seal material to establish a permanent seal over its initially-open port upon heating. The sealable port is a through via located in the center of an isolated silicon island supported on a thermally-insulating silicon nitride membrane in the center of a die. The through via is surrounded by a moderately high aspect ratio ring of indium solder. To seal the solder over the through via, the island and solder are heated by passing a current through a resistive heater on the back side of the device. Upon thermal actuation, the hollow cylinder of solder reflows into a toroid due to surface tension. For sufficiently high solder aspect ratios, the inner edges of the toroid meet in the center, thereby plugging the via. The heater is then turned off, solidifying the solder and forming a permanent seal.

Individual subsystems of the device were first analytically modeled using structural, thermal, electrical and geometrical models to optimize the device features. The sealing and thermal isolation subsystems were then separately fabricated and tested to verify the analytical models and key fabrication processes. The individual subsystems were then combined into the final device. Tests on the final device indicate an open state flow rate of 60 to 400 standard cm$^3$ per minute (sccm), a closed state leak rate not detectable above that of the test jig used ($10^{-4}$ sccm), and an open-to-closed flow rate ratio of greater than $10^5$ to $10^6$. 

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Chapter 1

Introduction and Background

1.1 Context

Chip-scale vacuum pumping is important for a range of MEMS applications such as high-Q resonators, chemical analysis systems and chip-scale atomic clocks. High-Q resonators achieve their highest Q factors when operated at pressures in the microTorr to milliTorr range, by avoiding the viscous damping effects that result from operating at higher pressures. Gavan et al. have demonstrated that the Q-factor for silicon nitride cantilevers follows a sigmoidal-shaped curve with the highest values occurring below a pressure of $10^{-4}$ Torr [1]. Fong et al. have reported Q-factors on the order of $10^5$ for a pressure of $6 \times 10^{-4}$ Torr [2], whereas Khine et al. have demonstrated Q-factors on the order of $10^6$ for a pressure of $3.6 \times 10^{-5}$ Torr [3]. In comparison, typical Q-factors for resonators at atmospheric pressure are limited to the 10 to 1000 [1, 2, 4]. Similarly, micro chemical analysis systems such as the one reported by Zellers et al. [5] operate under a pressure of a few milliTorr because higher pressures can lead to sample dilution and prevent the successful detection of the target species. Chip-scale atomic clocks also require
vacuum on the order of $10^{-7}$ Torr [6] since the isolation of the reference isotope atoms is essential for the operation of such devices.

These are just a few examples of the MEMS devices that require high vacuum to function effectively. Vacuum pumping in these devices is currently achieved using macroscale vacuum systems, as the state of the art for MEMS vacuum pumping is limited to hundreds of Torr [7]. The necessity for macroscale auxiliary devices for such MEMS systems nullifies many of the benefits of size reduction for these MEMS systems. Consequently, there has been a considerable push for the development of MEMS pumps. While a huge amount of this work has focused on liquid pumping [8-10], the development of MEMS vacuum pumps has been slower. Some of the challenges for MEMS vacuum pumps include valve leakage, dead volume and the lack of actuators that have enough force to act against any the necessary pressure differences and enough stroke to evacuate the pump chambers fully. The first MEMS vacuum pumps that were reported were only capable of achieving a pressure differential of few tens of Torr from atmosphere[11]. Since then, there has been significant progress in micropumping. Recently, Zhou et al. [12] demonstrated a single-stage MEMS displacement pump that achieved a base pressure of 164 Torr, the lowest reported base pressure to date. While this is a huge improvement over the earliest MEMS vacuum pumps, it still does not approach the micro or even milliTorr range that is required for many MEMS systems. One important reason for this is valve leakage; Zhou et al. use valves that consist of pneumatically actuated diaphragms that are pushed onto a flow port to seal it. However, as will be described in Section 1.3, such MEMS valves leak due to surface roughness, thereby limiting the base pressure that can be achieved by the MEMS pump.

1.2 Project Overview – Chip-Scale Vacuum Micro Pump (CSVMP)

The Chip-Scale Vacuum Micro Pump (CSVMP) project aims to develop the first chip-scale MEMS vacuum pump (to-date) capable of reaching high vacuum.

Ultimate specifications for the project, as specified by DARPA, are as follows:

- Ultimate pressure – $10^{-6}$ Torr
Specifications for Phase 1 of the project are listed below:

- **Ultimate pressure** - $10^{-2}$ Torr
- **Volume** - 2 cm$^3$
- **Power** - 1 W

The team working on this wider CSVMP project consisted of Prof. Carol Livermore, Prof. Martin Schmidt, Prof. Akintunde Akinwande, Dr. Luis Velasquez-Garcia, Dr. Hanqing Li, Dr. Hui Zhou, Dr. Xiaozhi Wang, Daniel Jang, Vivi Jayanty, Eric Newton and the author. The solution proposed involves a three stage pump shown schematically below, with the first stage consisting of a mechanical flow-through pump and the second and third stages consisting of sealed ion pumps. The mechanical pump is designed to reduce the chamber pressure from atmosphere (760 Torr) to 30 Torr, at which point the ion pumps are turned on and reduce the pressure from 30 Torr to approximately $10^{-2}$ Torr. The ion pumps serve to ionize the remaining molecules in the chamber and capture them with a “getter”, a material held at an opposite potential compared to the ionized molecules. One of the ion pumps uses electron emitters to produce electrons to ionize the residual species, while the other uses field ionizers to ionize the residual species directly. The captured ions then diffuse out from the getter surface into its interior. Because the getters have only a finite surface area for capturing ions as well as a finite volume for storing these ions, they have a finite capacity and lifetime. This lifetime is adversely affected by any leakage into the pressure chamber, as leakage increases the number of ions that must be captured by the getters in order to maintain a low pressure. Models indicate that a leakage of $10^{-9}$ sccm (standard cm$^3$ per minute) would allow the ion pumps to run continuously for approximately one year before the getters are saturated. This leakage is much lower than the leakage of the pneumatic valves used in the mechanical pump. This necessitates a separate valve between the mechanical pump and the ion pumps that is closed immediately before the ion pumps are turned on, and that has a leakage of less than $10^{-9}$ sccm. An extensive literature review was done to identify any MEMS valves already designed that could be adopted for this purpose.
1.3 State-of-the-art for MEMS valves

The idea of a microvalve is not new. Some of the earliest MEMS valves were reported around 1978 [13]. Since then, a host of MEMS valves have been designed and fabricated [10, 14-18]. Most MEMS valves consist of a boss that is actuated to cover or uncover a flow port.
The generic microvalve shown in Figure 1-2 can be designed to be normally-open or normally-closed. The boss is either actuated to push against the valve seat to close the valve, or it is actuated to pull away from the seat to open the valve. The actuation mechanism used to do this can be electrostatic [14, 16, 17, 19-21], magnetic [22-25], piezoelectric [26, 27] or pneumatic [28-30], or a combination of some of these [31]. The highest flow rates reported in these valves have been on the order of 50 sccm, while the lowest leak rates have been on the order of $10^{-3}$ sccm. One exception is the valve reported by Hirano et al. which employs electromagnetic actuation and has a leakage of $10^{-7}$ sccm [32]. However, the flow rate for this valve is only 0.189 sccm, therefore it is not representative of the higher flow rate valves described above.

Although valves in which a moveable boss seals a flow path are most common, other sealing methodologies have been demonstrated as well. One type of microvalve demonstrated to work recently utilizes the manipulation of ferrofluidic liquids to open or close the fluid flow path [33]. A schematic of such a valve is shown in Figure 1-3 below.

![Ferrofluidic Valve Schematic](image_url)

**Figure 1-3:** Schematic of a ferrofluidic valve, in the open (left) and closed (right) configuration.

While this valve was reported to be capable of withstanding a 12kPa ($\approx 100$ Torr) pressure differential, the exact leakage was not quantified. Moreover, the external electromagnets required to manipulate the ferrofluid are large, and difficult to integrate into a size-limited MEMS system, such as the Chip-Scale Micro Vacuum Pump. However, this type of valve does introduce a novel approach to overcome the roughness issue that plagues the other valves described above by utilizing a liquid that wets the channel in which it resides.
In a different valve designed for sealing applications, Stenmark et al. [34] use the properties of a liquid (such as molten solder) to get leak-free initial sealing, after which the liquid is solidified. This initially-closed device is permanently opened by melting and reflowing the solid seal. The resulting liquid then drains away from the seal interface and is captured in a reservoir. Although the valve in [34] provides the leak free sealing that is required for the CSVMP application, it starts closed and can be opened once rather than starting open and being closed as is required for the present application.

Thus, it can be seen that no currently existing valves offer the functionality required by the CSVMP system. A big problem with the conventional valves described above is that the lowest reported leak rates for high flow valves (> 50sccm) are on the order of $10^{-3}$ sccm, whereas the leak rate specification for the valve being designed is $10^{-9}$ sccm. Each of the other valves described above also lacks a key characteristic, such as open flow rate [32], small system size [33], or ability to be sealed during operation [34]. For this reason, none of the MEMS valves described in literature can be used for our purposes. They either need to be modified in some way, or an entirely new valve needs to be designed.

**Table 1-1:** Leak rates and flow rates for some MEMS valves.

<table>
<thead>
<tr>
<th>VALVE</th>
<th>LEAK/FLOW RATES (IN SCCM)</th>
<th>OPEN TO CLOSED FLOW RATE RATIOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OPEN</td>
<td>CLOSED</td>
</tr>
<tr>
<td>Yang et al. [35]</td>
<td>45</td>
<td>$6 \times 10^{-3}$</td>
</tr>
<tr>
<td>Yang et al. [36]</td>
<td>52</td>
<td>$5 \times 10^{-3}$</td>
</tr>
<tr>
<td>Robertson et al. [19]</td>
<td>1</td>
<td>0.1</td>
</tr>
<tr>
<td>Potkay et al. [31]</td>
<td>3.3</td>
<td>0.02</td>
</tr>
<tr>
<td>Design specs for our valve</td>
<td>$&gt;&gt;50$</td>
<td>$&lt;10^{-9}$</td>
</tr>
</tbody>
</table>
1.4 Permanently Sealable Valve

In the Chip Scale Vacuum Micro Pump system, the permanently sealable valve is located between the mechanical pump and the ion pumps. Once the mechanical pumps reduce the chamber pressure down to 30 Torr, the initially-open valve is actuated, providing a leak-free seal for the ion pumps to start pumping. This thesis will focus on the design and fabrication of this permanently sealable valve (also referred to as a “Thermally Actuated MEMS Seal”). The design specifications for this valve are as follows:

1. Leakage \( < 10^{-9} \) standard cm\(^3\) per minute (sccm)
2. Volume \(< 0.3 \) cm\(^3\)
3. Power consumed \(< 1 \) W
4. Must be MEMS-compatible

Based on these requirements, a structure like the one shown in Figure 1-4 is proposed. This design relies on the surface tension of a molten seal material to establish a permanent seal over its initially-open port upon heating. The sealable port is a through via located in the center of an isolated silicon island supported on a thermally-insulating membrane in the center of a die. The through via is surrounded by a moderately high aspect ratio ring of solder sealing material. To seal the solder over the through via, the island and solder are heated by passing a current through a resistive heater on the back side of the device. Upon thermal actuation, the cylindrically-shaped solder reflows into a toroid due to surface tension and the lyophobic interaction with its substrate. With a sufficiently high solder aspect ratio and a sufficiently small via diameter, the solder plugs the via. The heater is then turned off, solidifying the solder and forming a permanent seal. This design will be discussed in more detail in the following chapters.
Chapter 1: Introduction and Background

1.5 Thesis Outline

Now that the problem is clearly defined, Chapter 2 will discuss the chosen design concept in more detail. Chapter 3 will model the various aspects of this final design in an effort to optimize the design space under consideration. Chapter 4 will discuss in detail the procedure for fabricating the various test devices. Chapter 5 will discuss the testing methodology, as well as results from the various tests. Finally, Chapter 6 will review the conclusions of these results as well as possible areas for future work.

Figure 1-4: Schematic of the final chosen design. Note that the schematic in the lower right region represents the solder structure just before it balls up. The resulting balled-up structure is not shown above.
Chapter 2: Device Concept

2.1 Introduction

This chapter aims to familiarize the reader with the general functioning of the design concept introduced at the end of Chapter 1, without going into detailed analyses and calculations (which are the focus of Chapter 3). It first examines the various components of the design concept and their intended interactions with each other. It then reviews the material choices for the various components and highlights the most promising candidates. Finally, it describes some proof-of-concept tests to validate the feasibility of those parts of the design concept that have the highest level of risk associated with them.

2.2 Design Concept

Let us re-examine the device design concept (Figure 2-1).
As described in Chapter 1, this concept relies on the reflow of a central solder structure to create a leak-free seal. The test die is assumed to be made from silicon, as this is the starting point for most microfabricated devices. This choice of die material will be justified with models in Chapter 3. Before reflow, the solder structure is shaped like a hollow cylinder with a through via in the middle. This structure sits on top of a silicon island that also has a through via which forms a connecting flow path with the via of the solder structure. To reflow the solder, the central silicon island is heated up to a temperature higher than the melting point of the solder being used. This thermal actuation is achieved using a resistive heater on the bottom of the central island that selectively heats the island while the membrane thermally insulates it from the
rest of the die. As described in Section 1.2, this device is designed to experience a pressure difference of up to 1 atmosphere between two sides of the membrane.

As depicted here, this design has three main structural and functional components: the solder structure, the membrane, and the heater. Each of these is explored below in more detail.

2.2.1 Solder structure

The purpose of the solder structure is to allow flow through the valve in the open state, and to provide a leak-free seal in the closed state. Proper functioning of this structure is therefore critical to the success of the proposed design.

Fabricating an initially-open solder structure with a through via, while not trivial, is not as challenging as ensuring that the structure provides a leak-free seal after reflowing. As seen in the literature review in Section 1.3, most MEMS valves struggle with leakage, and the ability of our proposed design to provide a leak-free seal is what will set it apart from other MEMS valves that already exist. To ensure this leak-free seal, the interface between the reflowed solder and the substrate on which it sits will have to be leak-free. Moreover, the solder and substrate(s) will have to be chosen so that the solder will ball up upon reflow (as shown in Figure 2-1) instead of spreading out or exhibiting some other behavior. The ideal solder for this device should, therefore, “wet” the substrate it directly sits on, but “non-wet” the surrounding substrate. This will ensure that upon reflow it will not only ball up, but also stay in place on the wetting substrate. Moreover, this solder should have a low melting point (so that a minimum amount of power is required to melt it) and a very high boiling point (so that the vapor pressure of the melted solder will be low, thereby preventing any contamination of the vacuum during sealing).

A number of solders were considered for this design, including lead, gold, tin and indium-based alloys. Of all of these, indium is the most promising candidate because it has a low melting point of only 157°C [37] and an extremely high boiling point of 2000°C [38]. Moreover, a literature search suggests that indium wets nickel [39], a MEMS-compatible metal, and non-wets silicon, which is the most likely candidate for the test die as mentioned previously.
2.2.2 Membrane

The next key functional component of the design is the membrane on which the central island sits. Its foremost function is to provide thermal insulation to the central island, so that the heating is confined to that region during actuation (thereby minimizing the necessary power input and protecting excessive heat from flowing into other devices that this design might be attached to). When used in conjunction with the Chip-Scale Vacuum Micro Pump, as described in Section 1.2, this design will experience a pressure difference of up to 1 atmosphere across the two sides of the membrane. Therefore, in addition to providing thermal insulation, the membrane must be robust enough to withstand a pressure differential of at least 1 atmosphere. The ideal membrane material should, therefore, have a low thermal conductivity (for good thermal insulation), but a high failure strength (for withstanding a high pressure differential).

Keeping these two requirements in mind, a number of materials were considered. Common MEMS-compatible materials include silicon, silicon oxide, silicon nitride and a variety of metals. Since silicon has a high thermal conductivity of 149 W/m-K [40] (higher even than that of brass), silicon is not a promising choice for the thermally-insulating membrane material, despite its microfabrication convenience. The high thermal conductivities of typical metals also limit their applicability for an insulating membrane. Of the two remaining candidates, silicon nitride and silicon oxide both have a lower thermal conductivity than silicon (30 W/mK [41] and 1.4 W/mK [42] respectively, compared with 149 W/mK for silicon). However, silicon nitride is much stronger than silicon oxide, with a failure strength of over 10 GPa [43](compared to approximately 1 GPa for silicon oxide [44]). In addition, silicon nitride’s typically tensile residual stress is more advantageous for suspended membranes than is silicon oxide’s typically compressive residual stress. While the thermal conductivity of silicon nitride is higher than that of oxide, it will be shown in Chapter 3 that it is still low enough to provide adequate thermal insulation. Moreover, its high strength puts it at a unique advantage compared to silicon oxide. It is therefore the most promising candidate for the membrane. Based on models and analyses in Chapter 3, this material will, in fact, be chosen as the membrane material.
2.2.3 Heater

The last key functional component of the design is the resistive heater that is located on the back side of the central silicon island. The function of the heater is to provide enough power to heat the central silicon island to a temperature that is high enough to melt the solder structure. A number of common heater materials (such as elemental metals, alloys, highly-doped polysilicon, etc.) can be used to do this. However, an important consideration for microscale heaters is the current density in the heater structures. As the size of the heater wires is scaled down, the current density values rise and can reach very high values (even for small current inputs). Every material has a current density limit, beyond which the heater wires fail (by either melting or electromigration [45-47]). Since gold has a relatively high current density limit as compared with other common heater materials, and since gold MEMS heaters are common in literature [48, 49], this is the material chosen for the heater. Models in Chapter 3 will show that this choice does, in fact, satisfy the device requirements.

2.3 Proof-of-concept wetting tests

Of the three components described in Section 2.2, the gold resistive heater has the lowest level of risk associated with it, since such MEMS heaters are very common [48, 49] and since the proposed heater for the valve design is not intended to do anything that has not been done before. The membrane structure is slightly less common, but silicon nitride membranes are still relatively common in the literature [43, 50-52] and have been demonstrated to have the high failure strengths and low levels of residual stress that is desired in the device membrane.

The solder structure, on the other hand, is a more novel idea. To our knowledge, no similar thermally-activated solder sealing structure has been designed in literature. The successful performance of this component is critical to the success of the valve design. As a result, there is a high level of risk associated with this component. To mitigate this risk, a proof-of-concept test was first performed to ensure that the provisionally-selected solder material (indium) does, in fact, wet the provisionally-selected wetting substrate (nickel) and non-wet the
provisionally-selected non-wetting substrate (silicon). These tests consisted of depositing a solder on a hot substrate to examine the solder-substrate interaction.

Preliminary tests with indium, silicon and nickel were not encouraging. Figure 2-2 below shows an indium wire on a silicon substrate that was heated to a temperature above that of the melting point of indium, cooled back down, and then cross-sectioned. As can be seen from the cross-section, the shape of the wire remains almost unchanged, and it does not “ball up” as predicted by theory.

![Figure 2-2: Indium wire on silicon before and after melting, without the use of flux](image)

Most experiments that examine solder contact angles in the literature were either performed in vacuum environments or used solder flux to dissolve the oxide layer [39]. Moreover, indium oxidation has been explicitly shown to affect the wetting capability of this solder [53]. In atmosphere, a thin layer of native indium oxide is present on the indium. This oxide has a melting temperature of 1910°C, which causes it to form a thin shell around the indium wire, preventing the molten indium inside from interacting with the substrate. A solder flux is a chemical commonly used to react with the oxides on the solder as well as with those on the substrate surfaces. It dissolves the oxides to create an oxide-free solder-substrate interface, thereby restoring the wetting properties of the solder. The flux residue can then be cleaned away.

For subsequent tests, all surfaces were, therefore, cleaned with glutamic acid hydrochloride (5-10%), an organic acid flux commonly used with many solders. The contact angle results were found to be in agreement with literature values. The contact angle ($\theta$) of indium on silicon was estimated (with the naked eye using close-up photographs such as in
Figure 2-3), to be higher than $140^\circ$, whereas that of indium on nickel was estimated to be less than $30^\circ$.

![Figure 2-3: Photograph of indium wire on silicon, before and after melting. Organic acid flux was used. The contact angle was estimated to be over $140^\circ$.]

Figure 2-4 Photograph of an indium shot on nickel foil, before and after melting. Organic acid flux was used. The contact angle was estimated to be less than $30^\circ$.

Thus, these proof-of-concept tests successfully demonstrated a key process and paved the way for moving forward with the device concept as envisioned in Figure 2-1.

2.4 Modeling and Testing Roadmap

In order to find the optimal dimensions for the final design, it is necessary to model its three structural components and to test their performance. Figure 2-5 shows a general roadmap used to guide the device modeling and testing.
The wetting model predicts optimal solder structure dimensions in order to ensure that the solder will ball up upon reflow and plug the central via. The membrane structural and thermal models aim to optimize the membrane dimensions so that it can provide adequate thermal insulation but also withstand a 1 atmosphere pressure differential. Finally, the heater model is used to guide the choice of resistive heater dimensions. These models are described in detail in Chapter 3.

As mentioned in Section 2.3, of the three components listed here, the resistive heater is the lowest risk element. In order to reduce the risk associated with the design of the other two higher-risk components, they are first tested separately in “short loop tests”, a common optimization and risk mitigation strategy. These short loop tests, as well as the final device test are described in Chapters 4 and 5.

---

**Figure 2-5: Device testing and modeling roadmap**

<table>
<thead>
<tr>
<th>Structural Components</th>
<th>Function</th>
<th>Function Modeled by</th>
<th>Function Tested by</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder apparatus</td>
<td>Sealing</td>
<td>Wetting model</td>
<td>Sealing short loop &amp; wetting tests</td>
</tr>
<tr>
<td>Membrane</td>
<td>Withstand 1 atm pressure differential</td>
<td>Membrane structural model</td>
<td>Membrane short loop</td>
</tr>
<tr>
<td>Resistive heater</td>
<td>Thermal isolation and heating of central island</td>
<td>Membrane thermal model &amp; heater model</td>
<td>Full device test</td>
</tr>
</tbody>
</table>
Chapter 3
Modeling

3.1 Introduction

In order to optimize various aspects of the device, including its dimensions and constituent materials, it is important to gain a deeper understanding of how it interacts with the environment. With this goal in mind, four analytical models were created to predict the behavior of the key structural components of the device, namely, the solder apparatus, the membrane and the gold resistive heater, and their interactions with each other.

1. A simple geometrical “wetting model” was created to model the solder apparatus and predict its behavior before and after reflow.

2. A “thermal model” was used to model the flow of heat through the system.

3. A “structural model” was used to predict the mechanical integrity of the membrane structure.
4. A “heater model” to model the electrical properties associated with the resistive heater.

### 3.2 Wetting Model

The valve concept relies on the solder structure to ball up upon reflow and plug the initially-open flow port. A model is needed to guide the geometry of the initial solder structure to ensure that it will ball up upon reflow. This section describes the geometrical wetting model used for this purpose. This simple model captures the key qualitative tradeoffs between the central via diameter, the initial diameter of the solder structure and the initial height of the solder structure, but it does not accurately capture the effects of contact angle variation, especially for contact angles below $90^\circ$. However, only lyophobic solders (contact angles $>>90^\circ$) will be considered for this device, as explained in Section 3.2.1. Therefore, this model is still very useful in providing key insights into the solder structure design.

Figure 3-1 shows a schematic of the design concept with a close-up of the solder structure. The final device consists of a solder structure that resembles a partially-cut toroid before reflow and a partially-cut sphere after reflow. However, for ease of calculation, the structure is modeled as shown in Figure 3-2.

![Solder Structure Diagram]
Figure 3-2: Model of the solder structure. Note that the schematic in the lower right region represents the solder structure just before it balls up. The resulting balled-up structure is not shown above.

The shape of the solder ball after reflow is determined by the contact angle ($\theta_c$), a measure of the degree to which the solder "wets" the substrate it sits on: the lower the contact angle, the higher the degree of wetting.

Figure 3-3: Schematic illustrating the concept of a contact angle.
Before reflow, the volume of the solder structure \( V_{BR} \) is equal to the volume of the outer cylinder minus the volume of the inner cylinder, and is given by

\[
V_{BR} = \pi \left( w + \frac{d}{2} \right)^2 h - \pi \left( \frac{d}{2} \right)^2 h = \pi hw(w + d), \quad (3-1)
\]

where \( w \) is the initial solder width, \( d \) is via diameter, and \( h \) is the initial solder height. Assuming the this initial volume is “just sufficient” to plug the central via, the solder forms a donut-like structure after reflow, as shown in Figure 3-2. Its new volume \( V_{AR} \) can be calculated by revolving the cross-sectional area around the circumference of a circle with radius \( r \), and is given by

\[
V_{AR} = \left[ \pi r^2 - \frac{r^2}{2} (\theta - \sin \theta) \right] (2\pi)(r), \quad (3-2)
\]

where \( r \) is the radius of the donut (as shown in Figure 3-2) and \( \theta \) is the angle subtended by the circular segment (as shown in Figure 3-3). Note that

\[
\theta = 2\pi - \theta_c. \quad (3-3)
\]

For the case, where the structure barely plugs the via after reflow, the value of \( r \) is given by

\[
r = \frac{d+w}{2}, \quad (3-4)
\]

and the two volumes \( V_{AR} \) and \( V_{BR} \) are equal. Therefore, substituting equation 3-4 in 3-2 and equating it to 3-1, the value of the minimum initial solder height is given by

\[
h_{min} = \frac{1}{w} \left( \frac{d+w}{2} \right)^2 \left[ \pi - \left( \frac{\theta - \sin \theta}{2} \right) \right]. \quad (3-5)
\]

Thus, this model can give the approximate height \( h \) of the initial solder structure required for any given width \( w \), hole diameter \( d \) and contact angle \( \theta_c \). The assembly method chosen (described in detail in Chapter 4) limits the value of \( d \) to 380 \( \mu m \), 580 \( \mu m \) or 780 \( \mu m \). For each of these values of \( d \), several values of the width \( w \) are chosen for analysis.

The model can be, thus, be represented as shown in Figure 3-4.
3.2.1 Optimizing the contact angle

Figure 3-5 plots the minimum necessary initial solder height as a function of the hole diameter for contact angles of 100° (slightly lyophobic), 140° (very lyophobic) and 170° (superlyophobic), and a constant solder width of 3 µm (since varying the width does not affect the qualitative relationship of these curves). Note that lyophobicity refers to the degree with which any molten substance wets a given substrate.
Figure 3-5: Initial minimum necessary solder height vs. hole diameter for 3 different contact angles.

Figure 3-5 shows that increasing the contact angle increases the required initial height of the solder structure. This seems counterintuitive at first, but upon further examination, it is apparent that this is a result of the way the geometric model is set up. Our model allows the initial solder structure to "spread out", as shown in Figure 3-6. Therefore from the above equation, for a structure with a contact angle of $90^\circ$, Equation 3-5 reduced to

$$h_{\text{min},w} = \frac{\pi r^2}{2},$$

but for a contact angle of $180^\circ$, the same equation reduces to

$$h_{\text{min},w} = \pi r^2.$$
Thus, the model predicts that a structure with a contact angle of $90^\circ$ will have a radius that is $1.414$ times the radius of a reflowed structure with a contact angle of $180^\circ$. Thus, the model predicts that a solder structure with a smaller contact angle will have a higher radius, and hence, a lower required height. A key assumption made by the model is that the solder is allowed to seal by “spreading out” with the increased radius as shown in Figure 3-6 below. However, in reality, the central via prevents the solder from spreading out in the center; it must “bulge out” instead to plug the hole. Therefore, at contact angles below or near $90^\circ$, the mechanism of sealing allowed by the model (spreading out), does not accurately represent reality. However, at contact angles much higher than $90^\circ$, the mechanism of sealing assumed by the model (bulging out), is a good representation of how the solder seals in reality. Moreover, the higher the contact angle of the solder on the substrate, the more it will bulge out. Therefore, we select for solders that are very non-wetting towards the chosen substrate.

![Figure 3-6](image)

Figure 3-6: A schematic showing a scenario (contact angle $90^\circ$), which is allowed by the model, but impossible in reality due to the central via.

Even though this model does not accurately represent the effects of contact angle variation on the solder structure geometry (for contact angles below $90^\circ$), it can give us valuable insights about other geometrical aspects of the solder structure (optimal via diameter, optimal solder height, and optimal solder width) for any given contact angle. Therefore, for the rest of this subsection, we will assume a solder contact angle of $140^\circ$, and optimize the initial solder structure geometry.
3.2.2 Optimizing the via diameter and initial solder width

Figure 3-7 varies $d$ from 5 to 100 μm and $w$ from 3 to 50 μm. The minimum values of $d$ and $w$ were chosen based on approximate microfabrication limits for effectively aligning the via and solder structures with each other.

As can be seen from this graph, for higher values of $d$ and $w$, the required values for $h$ are in the hundreds of microns. If we plan to deposit and pattern the solder structure using conventional microfabrication techniques, the maximum value of $h$ that can be allowed is approximately 20 μm, since that is the limit of common photoresist mold thicknesses.
Figure 3-8: Solder height vs. solder width vs. hole diameter for a contact angle of 140°.

Figure 3-8 shows a zoomed-in view of the lower values of $d$ and $w$, since this is the region where the value of $h$ is also most likely to be below the fabrication limit of 20 μm. The figure shows that the minimum required solder heights occur for the smallest value of $w$ chosen (3 μm), and for the smallest hole diameter of 5 μm. Even at these limits of fabrication, the minimum value of $h$ is approximately 15 μm. Given the uncertainties in the model, we would like to overdesign the structure by at least a factor of safety of two to ensure that it will work.
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This would put the initial solder height at a minimum of 30 μm. To get such high solder structures, equally high photoresist plating walls are required. However, it is hard to achieve photoresist structures this high using conventional microfabrication techniques, especially given the narrowness of the features.

We, therefore, use a different non-conventional method of depositing the solder structure. This method, described in detail in the Chapter 4, involves using mesoscale solder structures such as those used in the assembly of printed circuit boards. To look at relationships on this scale, Figure 3-9 plots the minimum necessary initial solder height as the via diameter is varied from 100 to 1000 μm and the width w from 1500 to 3500 μm.

![Figure 3-9: Minimum necessary initial solder height vs. solder width vs. hole diameter for a contact angle of 140°.](image-url)
Chapter 3: Modeling

It can be seen that at $d = 400 \mu m$, the structure requires an aspect ratio of approximately 1 for a width of 1500 $\mu m$ and an aspect ratio of slightly less than 1 for a width of 3500 $\mu m$. Similarly, at $d = 600$ and 800 $\mu m$, the required aspect ratios are all approximately 1.

3.2.3 Model Predictions

Thus, the model predicts that at the mesoscale, an aspect ratio slightly greater than 1 should be sufficient for ensuring that the solder plugs the hole, upon reflow. A range of mesoscale variations in the hole diameter and the solder width were tested in the sealing short loop tests described in the subsequent sections.

3.3 Thermal Model

3.3.1 Overview

The center island (Figure 3-2) needs to heat up to the melting temperature of the solder being used (157°C/430 K, in the case of indium). The membrane design must be optimized to provide the necessary thermal resistance to achieve this temperature differential while also meeting the requirements of mechanical robustness (see Section 3.4). The schematic in Figure 3-10 describes the inputs and the outputs for the model that calculates this membrane thermal resistance. The target value of thermal resistance is a few hundred K/W, so that at the maximum allowed power input of 1 W (Section 1.4), there is a minimum temperature drop of at least a few hundred K, high enough to melt the indium.
Figure 3-10: Thermal Model – Inputs and Outputs.

3.3.2 Modeling the Membrane as an Annular Fin

To estimate the thermal resistance of the membrane, it is modeled using a Bessel approximation for heat transfer through annular fins [54].
Figure 3-11: Annular fin used to model the device membrane.

Consider an annular fin (Figure 3-11) of uniform thickness 2t, inner boss radius $r_1$, and outer radius $r_2$. Applying the principal of conservation of energy to a differential element between radii $r$ and $r+\Delta r$, we get,

$$q(2\pi r)(2t)|_r - q(2\pi r)(2t)|_{r+\Delta r} - h_c(2\pi r \Delta r (T - T_e)) = 0, \quad (3-8)$$

where $q$ is the heat flow rate, $t$ is half the fin thickness, $h_c$ is the convection coefficient, $T_e$ is the room temperature and $T$ is the temperature at any given radius $r$. Dividing Equation 3-11 throughout by $4\pi \Delta r$ and letting $\Delta r \rightarrow 0$, we get,

$$-\frac{d}{dr} (rtq) - \frac{h_c r}{tk} (T - T_e) = 0. \quad (3-9)$$

Substituting Fourier’s law ($q = -k \frac{dT}{dr}$) in Equation 3-12 and dividing by $(tk)$ gives

$$\frac{d}{dr} \left( r \frac{dT}{dr} \right) - \frac{hr}{tk} (T - T_e) = 0. \quad (3-10)$$
This can be re-arranged as

\[ r^2 \frac{d^2 T}{dr^2} + r \frac{dT}{dr} - \beta^2 r^2 (T - T_e) = 0, \]  
(3-11)

where \( \beta^2 = \frac{h_c}{tk} \). Introducing the new variables,

\[ z = \beta r, \]  
(3-12)

\[ \theta = \frac{T - T_e}{T_B - T_e}, \]  
(3-13)

Equation 3-14 can now be written as,

\[ z^2 \frac{d^2 \theta}{dz^2} + z \frac{d\theta}{dz} - z^2 \theta = 0. \]  
(3-14)

Note that \( T_B \) is the temperature at the base of the fin. Equation 3-17 is a modified Bessel equation of zero order and has the solution:

\[ \theta = C_1 I_0(z) + C_2 K_0(z) \]  
(3-15)

where \( I_0 \) and \( K_0 \) are zero-order modified Bessel functions of the first and second kinds, respectively, and \( C_1 \) and \( C_2 \) are constants that are solved for using the boundary conditions.

### 3.3.2.1 Actual Boundary Conditions:

At the base of the fin \((r = r_1)\), the value of \( \theta \) is identically one (from Equation 3-13). Thus, the first boundary condition can be written as

\[ T = T_B \text{ at } r = r_1 \text{ or } \theta = 1 \text{ at } z = z_1. \]  
(3-16)

The boundary condition at the edge of the fin \((r = r_2)\) is more complicated. On this edge, the membrane system couples to the surrounding die system. To accurately solve for the temperature distribution the fin, both systems need to solved simultaneously, with the heat transfer at their interface satisfying the equation.
where the first term represents heat conduction from the membrane side of the interface and the second term represents heat conduction to the die side of the interface. Here, $k_{\text{membrane}}$ and $k_{\text{die}}$ are the respective thermal conductivities of membrane and die material, and $A_{\text{membrane}}$ and $A_{\text{die}}$ are the respective cross-sectional areas for conduction.

Using the boundary conditions in 3-16 and 3-17 in Equation 3-15 will yield accurate solutions for the temperature distribution in the membrane. However, boundary condition 3-20 makes it very complicated to solve for the temperature distribution analytically. Besides, a rough estimate of the effective membrane thermal resistance is sufficient for the purposes of the valve design, and an accurate temperature distribution across the entire system is not required.

In order to estimate this thermal resistance, the following simplified boundary conditions are considered.

### 3.3.2.2 Simplified Boundary Condition Model 1

![Figure 3-12: Simplified boundary condition 1 – insulated outer edge.](image)

This boundary condition model assumes that the entire outer edge of the membrane is insulated (analogous with an insulated tip boundary condition for a pin fin) as shown in Figure 3-
12. The first boundary condition is the same as in 3-16 but the second boundary condition now becomes

\[ \frac{dT}{dr} = 0 \text{ at } r = r_2 \text{ or } \frac{d\theta}{dz} = 0 \text{ at } z = z_2, \]  

(3-18)
since an insulated edge implies a zero slope for the temperature distribution at this boundary. This second boundary condition is not an accurate representation of the temperature distribution our system at all, since an insulated edge condition artificially restricts the flow of heat out of the membrane, and significantly underestimates the temperature drop. However, this is the case that Mills [54] analytically solves for, and hence it serves as a good benchmark. Using this boundary condition, the constants \( C_1 \) and \( C_2 \) are calculated to be

\[ C_1 = \frac{K_1(z_2)}{I_0(z_1)K_1(z_2)-I_1(z_2)K_0(z_1)}, \]  

(3-19)

and

\[ C_2 = \frac{I_1(z_2)}{I_0(z_1)K_1(z_2)-I_1(z_2)K_0(z_1)}, \]  

(3-20)

where \( I_1 \) and \( K_1 \) first-order modified Bessel functions of the first and second kinds, respectively. Equations 3-19 and 3-20 can be plugged into Equation 3-15 to solve for the temperature distribution in the fin.

### 3.3.2.3 Simplified Boundary Condition Model 2

Another boundary condition that can be used instead of 3-18 is one that assumes a specified edge temperature that is midway between the base temperature and the surrounding temperature (Figure 3-13). This choice of edge temperature might seem arbitrary at first, but it is supported by estimations of various resistances in the simplified network of thermal resistances (Figure 3-16), as will be seen in Section 3.3.3. Thus, the first boundary condition is still Equation 3-16 whereas the second one becomes

\[ T = T_B - \frac{(T_B - T_e)}{2} \text{ at } r = r_2 \text{ or } \theta = 0.5 \text{ at } z = z_2. \]  

(3-21)
The constants $C_1$ and $C_2$ are, therefore, calculated to be

$$C_1 = \frac{0.5K_0(z_1) - K_0(z_2)}{I_0(z_2)K_0(z_1) - I_0(z_1)K_0(z_2)},$$

(3-22)

and

$$C_2 = \frac{I_0(z_2) - 0.5I_0(z_1)}{I_0(z_2)K_0(z_1) - I_0(z_1)K_0(z_2)}.$$

(3-23)

Equations 3-22 and 3-23 can be plugged into Equation 3-15 to solve for the temperature distribution in the fin, which is then plugged into Equation 3-24 to solve for the power input. The thermal resistance can then be calculated by dividing the temperature drop by the power consumed.
3.3.2.4 Simplified Boundary Condition Model 3 – Infinite Fin

A third method of estimating the membrane thermal resistance is to use boundary conditions 3-16 and 3-18, but to assume that the fin extends infinitely, so that the 2nd B.C. is irrelevant. This assumption is justified by the fact that silicon has a much higher thermal conductivity compared to nitride, and acts as a heat sink around the membrane. This simplification is similar to boundary condition model 1, except that in this case \( r_2 \) (and hence \( z_2 \)) is replaced by infinity or an extremely large number. The temperature drop in the membrane can be estimated by sampling the temperature predicted by the model at \( r = r_2 \). The thermal resistance can then be calculated by dividing this temperature drop by the power consumed (Equation 3-24).
3.3.2.5 Heat Flow

For all the three cases listed above, the heat flow through the base of the fin is given by

\[ \dot{Q} = -k A_c \frac{dT}{dr} \bigg|_{r=r_1} = -k (2\pi r_1) (2t) (T_B - T_e) \beta \frac{d\theta}{dz} \bigg|_{z=z_1}, \]  

where \( k \) is the thermal conductivity of the membrane material and \( A_c \) is the cross-sectional area.

3.3.3 Thermal Circuit

The simplified boundary condition in Section 3.3.2.3 had assumed a temperature drop across the membrane roughly equal to half the temperature difference between the membrane base and the environment. This assumption is justified by considering the network of thermal resistance shown in Figure 3-15. Heat enters the system via the gold resistive heater on one side of the central silicon island. The heat is then dissipated from this structure via three pathways. The first consists of conduction up the central silicon island, to the solder structure on top of the device. The second consists of conduction through the thin membrane, to the rest of the silicon die. And the last pathway is directly into the atmosphere via convection. The silicon die also convects heat out into atmosphere, as does the solder apparatus.

Note that the network of thermal resistances considered is for steady-state heat transfer. In reality, the central silicon island as well as the solder will have thermal capacitances. However, for the masses under consideration the transience times for these capacitances are on the order of a few seconds. Hence, the steady-state approximation is valid.
3.3.3.1 Estimating $R_1$

In general, the conductive thermal resistance through a structure of given geometry is given by

$$R_{\text{conduction}} = \frac{L_{\text{cond}}}{kA},$$

(3-25)

where $L_{\text{cond}}$ and $A$ are the length and cross-sectional area of the heat flow pathway, respectively, and $k$ is the thermal conductivity of the material. When the conductive pathway comprises several thermally resistive elements in series, the total conductive resistance is given by the sum of the conductive thermal resistances from each element,

$$R_{\text{total}} = R_1 + R_2 + \ldots + R_n.$$

(3-26)
3.3.3.2 Estimating $R_3, R_4$ and $R_5$

$R_3, R_4$ and $R_5$ are all dominated by convection. In general, convective thermal resistance is given by:

$$R_{\text{convection}} = \frac{1}{hA} \quad (3-27)$$

where $A$ is the surface area at the fluid interface. Convection acts on the bottom surface of the central island structure.

3.3.3.3 Simplifying the network of resistances

Assuming a central silicon island with a 2 mm diameter, a 1 cm x 1 cm x 500 μm thick silicon die, a 0.5 μm oxide layer and a 2.4 μm nitride layer, $R_1, R_3, R_4$ and $R_5$ are estimated to be 2.32 K/W, 32,000 K/W, 538 K/W and 32,000 K/W respectively. Since $R_3$ and $R_5$ are two orders of magnitude higher than $R_2$ and $R_4$, they can be neglected. Also, since $R_1$ is two orders of magnitude lower than $R_2$ and $R_4$, the heater apparatus and the solder structure can be considered to be isothermal. The simplified network of thermal resistances then looks like Figure 3-16.

![Figure 3-16: Simplified steady network of thermal resistances that connect the central island to the environment.](image-url)
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It should be noted that the 0.5 μm oxide layer on top of the nitride is also neglected for these thermal resistance calculations. Silicon oxide has a thermal conductivity of 1 W/mK (compared to 30 W/mK for silicon nitride). Hence, a 0.5 μm thick oxide membrane with the dimensions listed in the table, has a thermal resistance on the order of tens of thousands of K/W, at least an order of magnitude higher than that of the 2.4 μm thick silicon nitride membrane alone. It is, therefore, reasonable to assume that a majority of the heat passes through the nitride membrane alone. This simplifies the calculations significantly.

The assumption in Section 3.3.2.3 would be valid if \( R_2 \) were on the order of a few hundred K/W, which is indeed the case for the typical dimensions considered (as will be seen in Section 3.4.4).

3.3.4 Optimizing Model Inputs

Some of the inputs in the thermal model of the membrane are also the inputs in the structural model of the membrane that follows. Moreover, there is a tradeoff between the thermal isolation the membrane provides and the strength of the membrane. For example, a thicker membrane will be less thermally isolating but stronger. It, therefore, becomes necessary to review the membrane structural model equations before any of the membrane dimensions can be optimized.

3.4 Membrane – Structural Model

In addition to providing thermal isolation to the solder apparatus, the device membrane must also be strong enough to withstand a 1 atmosphere pressure differential without rupturing. We use the “Theory of Plates and Shells” by Timoshenko [55] to model the structural properties of the membrane. The membrane was also modeled using ADINA, a finite element modeling software, to estimate the deflection and stresses in the membrane and cross-check it with the value obtained using the analytical Timoshenko model.
3.4.1 Membrane Modeling

The membrane can be modeled as a uniformly loaded circular plate that bends symmetrically (Figure 3-17).

![Diagram of uniformly loaded circular plate with movable central boss and pressure applied]

It can be shown that for such a case, the maximum stress \( \sigma_{\text{max}} \) in the membrane is given by [55]:

\[
\sigma_{\text{max}} = k_1 \frac{q(r_2)^2}{(2t)^2},
\]

(3-28)

where \( k_1 \) is a correction factor depending on the ratio of the membrane outer and inner diameters. \( k_1 \)-values for common outer-to-inner diameter ratios are listed in Table 3-1 below.
Table 3-1: Table of $k_i$ values for some inner diameter to outer diameter ratios.

<table>
<thead>
<tr>
<th>Outer-to-inner diameter ratio</th>
<th>$k_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.25</td>
<td>0.090</td>
</tr>
<tr>
<td>1.5</td>
<td>0.273</td>
</tr>
<tr>
<td>2</td>
<td>0.71</td>
</tr>
</tbody>
</table>

Note that the membrane, as shown in Figure 3-18, will experience stress due to bending as well as due to stretching. Equation 3-28 neglects stress due to stretching, an assumption that is supported by the analysis in Section 3.4.2 below. Also note that in the absence of a central boss structure, the maximum stress in the membrane is given by

$$\sigma_{\text{max}} = 0.75 \frac{q(r_2)^2}{(2t)^2}. \quad (3-29)$$

### 3.4.2 Neglect of the stretching term

It is important to note that both the Timoshenko model and ADINA assume pure bending of the membrane, and neglect any “stretching”. This is a reasonable approximation for “small” deflections, but we need to verify that our membrane falls in this regime by calculating the stress due to this term and comparing it with the stress due to pure bending. To validate this assumption, consider the complete pressure-deflection relation for a clamped square plate [40]. This model is derived using energy methods and includes the effects of stretching and residual stress along with those of bending, although the prefactors are approximate. It uses a sinusoidal curve as a trial function and predicts that

$$q = \left\{ C_r \left[ \frac{\sigma_0}{(2a)^2} + C_b \left[ \frac{E(2t)^3}{(1-v^2)(2a)^4} \right] \right] \delta + C_s f_s(v) \left[ \frac{E(2t)}{(1-v)(2a)^4} \right] \delta^3, \quad (3-30) \right\}$$
where $q$ is the applied external pressure, $\sigma_0$ is the residual stress in the membrane, $\delta$ is the membrane deflection, $\nu$ is the Poisson’s ratio, $E$ is the Young’s modulus of the material and $a$ is the length of the square side. The constants are given by

\[ C_r = \frac{3\pi^2}{2}, \quad (3-31) \]
\[ C_b = \frac{2\pi^4}{3}, \quad (3-32) \]
\[ C_s = \frac{\pi^4}{4}, \quad (3-33) \]
\[ \text{and } f_s(\nu) = \frac{(7-2\nu)(5+4\nu)}{32(1+\nu)}. \quad (3-34) \]

It should be noted that this equation is for a square membrane without a central boss. A structure with a central boss will be stiffer than one without, and hence will deflect less. Hence, the above equation will overestimate the deflection $\delta$ due to any given applied external pressure $q$. Therefore, if it can be shown that the stress due to stretching is negligible at this overestimate of deflection, it should follow that we can also neglect the stretching term for a case with a central boss structure.

Consider a membrane with a 4 mm diameter, the maximum value that will be considered in this section based on the approximate size restrictions on the test die. Assume that the membrane has no central boss, a Poisson’s ratio of 0.3 and a Young’s modulus of 317 GPa (the Young’s modulus value for silicon nitride). Neglect any residual stress. These assumptions yield a deflection of approximately 93 μm for an external applied pressure of 1 atmosphere. The flexural or “stretching” stress in the membrane is given by [56]

\[ \sigma_x(x, y) = \frac{-Ey}{\rho(x)}, \quad (3-35) \]

where $E$ is the Young’s modulus of the material, $y$ is the lateral distance from the neutral axis and $\rho(x)$ is the radius of curvature, which is defined as
\[ \rho(x) = \frac{1}{d^2} \frac{d^2S}{dx^2} \]  

where \( \delta(x) \) is the shape of the deflection curve. A sinusoidal shape for the deflection curve is assumed (Figure 3-18), as mentioned before. Although this might not be the exact shape of the actual deflection, it serves as a good estimate for the flexural stress. Note that the amplitude of the curve is assumed to be 50\( \mu \)m, an overestimate based on the calculated total deflection of 93\( \mu \)m.

![Assumed sinusoidal deflection for the membrane.](image)

**Figure 3-18:** Assumed sinusoidal deflection for the membrane.

This curve can be written as

\[ \delta(x) = A \cos[2\pi fx], \]  

where \( A \) is 50 \( \mu \)m and \( f \) is 250m\(^{-1}\) for the deflection curve shown in Figure 3-19. Substituting Equation 3-36 in 3-34 and 3-35, we can get a relation for the flexural stress in terms of \( x \) and \( y \). The maximum value of the this stress (\( \sigma_{x,\text{max}} \)) will occur at the clamped edges (\( x=0 \)), and on the surface of the membrane (\( y=h/2 \)). This is calculated to be 0.05 GPa. In comparison, the bending stress calculated for a 2 \( \mu \)m thick circular membrane with similar dimensions, using Equation 3-29, is 75 GPa, giving a ratio of predicted bending to stretching stress of 1500. Therefore, the assumption that the plate is in pure bending is valid.
3.4.3 Confirmation with numerical results

ADINA, a finite element modeling software, was used to numerically solve for the maximum stress in the membrane and serve as a cross-check for the theory of plates and shells described in Section 3.4.1.

![ADINA model for a 1 cm x 1cm x 2 μm membrane subject to a 0.5 atmosphere pressure differential.](image)

**Figure 3-19:** ADINA model for a 1 cm x 1cm x 2 μm membrane subject to a 0.5 atmosphere pressure differential.

Figure 3-19 above shows a 2 μm thick square membrane with a 1 cm side length and subjected to a 0.5 atmosphere pressure differential. It can be seen that the ADINA model predicts a maximum stress of 3.4 GPa in the membrane. In comparison, the maximum stress in a circular plate, according to the theory of plates and shells (Equation 3-29), for a 2 μm thick, 500 μm
radius membrane subject to 0.5 atmosphere pressure differential is 2.38 GPa. This is very similar to the 3.4 GPa value that was calculated using ADINA, thereby validating the theory used in Section 3.4.1.

Note that the ADINA model uses a square membrane whereas Equation 3-29 is for a circular membrane. This difference is because a square geometry is easier to setup in ADINA, while a circular membrane is easier to model theoretically. It is still valid to compare the two as the difference is geometries should not affect the predicted maximum stress by that much. The square geometry would be expected to result in a slightly higher maximum stress because of stress concentrations at the corners; this is confirmed by the ADINA model predicting a higher stress compared to the theory of plates and shells.

Note also that both the ADINA model as well as the theory of plates and shells assumes that the plate is in pure bending. Note also that the ADINA and Senturia (Equation 3-30) models are for a square membrane, whereas the Timoshenko model (Equation 3-29) is for a circular membrane. As a result, these models are only approximately comparable.

3.4.4 Optimizing Membrane Dimensions

Now that both the thermal and structural models for the membrane are defined, the membrane dimensions can be optimized. Note that, as stated in Section 2.2.2, the membrane material was chosen to be silicon nitride.

1. Membrane Thickness

A thicker membrane is less thermally isolating but stronger. It can be seen from the structural model that a thicker membrane increases the strength of the membrane to the 2\textsuperscript{nd} order, whereas it decreases its thermal insulation only linearly.
As the membrane thickness is increased, it does not affect the surface area available for convective heat transfer, leaving this process unaffected. However, it does increase the cross-sectional area for the conductive heat transfer path linearly. Thus, we can assume that the thermal isolation of the membrane decreases approximately linearly, as the thickness is increased (although this decrease might be linearly offset from the origin). On the other hand, Equation 3-28 shows that the maximum stress in the membrane decreases to the 2nd order as the thickness is increased.

Thus, there is no global optimum for the membrane thickness. A thicker, wider membrane is always better than a thinner one. However, at a certain point, the membrane becomes so thick that to ensure adequate thermal isolation its outer radius has to be designed to be extremely large (>1cm). The membrane then becomes too big to be integrated into the rest of the chip-scale vacuum pump (or to be considered a MEMS device).

In practice, the thickness of the membrane layer is limited by the deposition tool to approximately 2.4 μm for a silicon nitride membrane. Since a thicker, larger radius membrane offers the best combination of mechanical robustness and thermal isolation, as described above, the design process begins by assuming this thickness and calculating the required membrane outer and inner radii that satisfy both thermal and structural considerations. If the resulting membrane dimensions are impractically large and the thermal and mechanical constraints are simultaneously met, then there is the option to reduce the membrane thickness until its other dimensions are reasonable. In the design process used here, the required outer radius for a 2.4 μm thick silicon nitride membrane was compared with 1 cm (the approximate assumed die size). As long as the necessary outer radius is less than the 1 cm maximum size, the thickness is kept constant and the other dimensions are optimized.

As will be seen later, a membrane with this thickness requires an outer diameter of at most 3.5mm, which is still small enough to be integrated with the micropump. Therefore, we assume a membrane thickness of 2.4 μm for all subsequent calculations.
2. Membrane Inner and Outer Radii

The membrane inner and outer radii values are varied, in order to optimize the membrane dimensions. The smallest inner radius is limited by the via diameter (400 μm). The outer diameter is, therefore, varied for a fixed membrane thickness, for different inner radii (500 μm, 650 μm, 800 μm, 950 μm, 1100 μm, 1250 μm). For each case, the thermal resistance must be greater than 300K/W, so that 1 W of power input results in a temperature rise of at least 300K, thereby melting the solder. It is also necessary that the maximum stress in the membrane be less than 11GPa, the failure stress for silicon nitride thin films [43].

**Figure 3-20:** Predicted thermal resistance as a function of the membrane outer radius for a 500 μm membrane. Arrows indicate regime that meets the design specifications.

**Figure 3-21:** Predicted maximum stress as a function of the membrane outer radius for a 500 μm membrane. Arrows indicate regime that meets the design specifications.
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**Figure 3-22:** Predicted thermal resistance as a function of the membrane outer radius for a 650 µm membrane. Arrows indicate regime that meets the design specifications.

**Figure 3-23:** Predicted maximum stress as a function of the membrane outer radius for a 650 µm membrane. Arrows indicate regime that meets the design specifications.

**Figure 3-24:** Predicted thermal resistance as a function of the membrane outer radius for a 800 µm membrane. Arrows indicate regime that meets the design specifications.

**Figure 3-25:** Predicted maximum stress as a function of the membrane outer radius for a 800 µm membrane. Arrows indicate regime that meets the design specifications.
Figure 3-26: Predicted thermal resistance as a function of the membrane outer radius for a 950 μm membrane. Arrows indicate regime that meets the design specifications.

Figure 3-27: Predicted maximum stress as a function of the membrane outer radius for a 950 μm membrane. Arrows indicate regime that meets the design specifications.

Figure 3-28: Predicted thermal resistance as a function of the membrane outer radius for a 1100 μm membrane. Arrows indicate regime that meets the design specifications.

Figure 3-29: Predicted maximum stress as a function of the membrane outer radius for a 1100 μm membrane. Arrows indicate regime that meets the design specifications.
The arrows in the above graphs of thermal resistance and maximum stress represent allowable design space, given thermal and structural constraints, respectively. Thus, for a 2.4 µm thick silicon nitride membrane, with inner radii ranging from 500 µm to 1250 µm, there exist values of outer radii, such that the membrane satisfies both thermal and structural requirements. These theoretical predications (and experiments verifying them) inform the membrane dimensions used for the final device.

Residual stresses as well as stress concentrations in the membrane may result in a maximum stress greater than that predicted by the model above. If this is the case, test dies with a smaller outer radius and/or a smaller outer-to-inner radius ratio would have to be chosen for the final device (since a smaller outer radius reduces the stress in the membrane for a given pressure, as does a smaller outer-to-inner radius ratio).

On the other hand, fillets at the edges of the membrane may result in a smaller effective membrane, resulting in a lower maximum stress, than predicted above. If this is the case, the final device could afford to have a larger inner radius and/or a larger outer-to-inner radius ratio (since a larger radius provides better thermal isolation).
3.5 Modeling the Resistive Heater

The gold resistive heater heats up the central silicon island to melt the solder structure. It needs to be modeled to ensure that the chosen heater dimensions are sufficient to provide the required maximum power of 0.9 W (Section 1.4). A particular concern for microscale resistive heaters is the current density, the amount of current flowing through a given cross-sectional area of the heater. For bulk heater wires, current density values rarely reach failure limits. However, for microscale heaters, the small cross-sectional areas result in relatively high current densities even for small currents. If the current densities are too high, it can lead to failure by electromigration or melting [45-47]. The heater model must, therefore, also predict current densities values to ensure that they are within the failure limits for the chosen heater material.

3.5.1 Heater Model

The proposed heater structure is shown in Figure 3-30. The area available for the heater is limited by the diameter of the central island, as well as the diameter of the central via. We therefore derive the dependence on the device geometry on the current density, and then optimize this geometry to prevent device failure.

The width of the heater structure is assumed to be \( w \), and its spacing is assumed to be \( s \), as shown in Figure 3-33 below. Each “unit” of the heater is \((2w+2s)\) wide. The number of such units that fit in a square of side \( a \) is then \( a/(2w+2s) \). The length of the heater wire in each unit is approximately \( 2a \).
Figure 3-32: Schematic of the resistive gold heater structure.

Figure 3-33: Section of the heater showing line width and line spacing.

The total length of the heater in any die is then the length of each unit times the number of units, and is given by
The resistance of the heater is then given by

\[ R_{\text{heater}} = \frac{\rho L_{\text{heater}}}{A_{\text{cross-section}}} = \frac{\rho a^2}{tw(w+s)}, \tag{3-39} \]

where \( \rho \) is the electrical resistivity of the heater material and \( A_{\text{cross-section}} \) is the cross-sectional area of the heater line given by \( tw \). The power input is given by

\[ P = I^2 R, \tag{3-40} \]

where \( I \) is the current through the heater and \( R \) is the electrical resistance of the heater. The current density is defined as

\[ J = \frac{I}{A_{\text{cross-section}}}. \tag{3-41} \]

Using Equations 3-39, 3-40 and 3-41, the current density can, therefore, be written in terms of the device geometry as follows:

\[ J = \frac{\sqrt{P(w+s)}}{\sqrt{\rho a^2 tw}}. \tag{3-42} \]

This current density value needs to be below the failure limit for the chosen heater material for a power input of 1W (maximum input power). The current and voltage, in terms of the device geometry and power input, can be written as follows:

\[ I = \sqrt{\frac{Ptw(w+s)}{\rho a^2}}, \tag{3-43} \]

\[ V = \sqrt{\frac{Ppa^2}{tw(w+s)}}. \tag{3-44} \]
3.5.2 Optimizing Heater Dimensions

We can use Equation 3-42 to find the optimal heater material as well as optimal values for the heater dimensions.

1. Heater Material

For robust operation, the heater material should have a high failure current density ($J_{\text{fail}}$)-to-actual current density ($J$) ratio. From Equation 3-42, this then simplifies to a high $J_{\text{fail}}\sqrt{\rho}$ term, for heaters with the same dimensions. This term is tabulated for potential heater material candidates below. For this table, $J_{\text{fail}}$ values for the metals are assumed to be $10^{10}$ A/m² [57, 58].

Table 3-2: Comparison of candidate heater materials.

<table>
<thead>
<tr>
<th>Heater Material</th>
<th>$J_{\text{fail}}\sqrt{\rho}$ (Am⁻³Ω⁻¹/²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nichrome</td>
<td>$1.0 \times 10^7$</td>
</tr>
<tr>
<td>Gold</td>
<td>$1.5 \times 10^6$</td>
</tr>
<tr>
<td>Highly doped poly</td>
<td>$7.1 \times 10^3$</td>
</tr>
<tr>
<td>Aluminum</td>
<td>$1.6 \times 10^6$</td>
</tr>
<tr>
<td>Copper</td>
<td>$1.3 \times 10^6$</td>
</tr>
<tr>
<td>Nickel</td>
<td>$2.6 \times 10^6$</td>
</tr>
<tr>
<td>Chromium</td>
<td>$3.5 \times 10^6$</td>
</tr>
</tbody>
</table>

The table above indicates that all the metals considered above would be good candidates. However, gold deposition techniques are well-characterized, and gold heater structures have been extensively fabricated in literature [48, 49]. The heater material is, therefore, chosen to be gold.

2. Square side $a$

The larger the size of the square that the heater fits in, the lower the current density will be. Thus, a larger square is always better. However, this size is limited by the size of central
island/boss structure, which is determined by the wetting model and the membrane thermal and structural models.

3. **Heater thickness**

Equations 3-42 and 3-43 show that increasing the heater thickness $t$ will reduce the current density in the heater. It also, however, increases the currents in the structure by the same order for a given design power level. Thus, a thicker heater structure is always better, as long as predicted voltages or currents are not prohibitively larger for the external power supply. However, the maximum thickness is limited by microfabrication considerations. A thickness of 1 $\mu$m for gold is usually considered very thick. Figures 3-34 and 3-35 show the currents and voltages as a function of heater thickness, for a gold heater with a 10 $\mu$m line spacing, a 20 $\mu$m line width, a value of $a$ of 1.5 mm, and a design power level of 1 W. Figures 3-36 and 3-37 show the current and voltages as a function of heater thickness, for a gold heater with a 20 $\mu$m line spacing, a 100 $\mu$m line width, a value of $a$ of 1.0 mm, and a design power level of 1 W. These values of line width, line spacing and square side are chosen to represent arbitrary heater dimensions.

![Figure 3-34: Current vs. heater thickness for a gold heater with $s=10$ $\mu$m, $w=20$ $\mu$m, $a=1.5$ mm and a design power of 1 W.](image)
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Figure 3-35: Voltage vs. heater thickness for a gold heater with $s=10 \, \mu m$, $w=20 \, \mu m$, $a=1.5 \, mm$ and a design power of $1 \, W$.

Figure 3-36: Current vs. heater thickness for a gold heater with $s=20 \, \mu m$, $w=100 \, \mu m$, $a=1.0 \, mm$ and a design power of $1 \, W$. 


Thus, it can be seen that the maximum thickness of 1 μm does not involve prohibitively large currents or voltages. Thus, the heater thickness is chosen to be 1 μm.

4. Line width $w$ and line spacing $s$

All other quantities constant, the current density is proportional to the ratio $s/w$ (Equation 3-42). However, the line spacing $s$ has a lower limit imposed by microfabrication techniques. Since the most likely candidates for this heater are metals, the structure will be patterned using a “lift off” process. If the line spacing is much smaller than 10 μm, parts of the geometry might not be patterned correctly, resulting in short-circuiting of the heater. Thus, the line spacing is chosen to be 10 μm. A larger value of $w$ increases the current to a higher power than it decreases the current density. Again, this might be a consideration if the currents in the heater are too high for the external power supply. The current density thus, only has a weak dependence on the heater width.
Figure 3-38: Current density vs. heater width for a 1 μm thick gold heater with s=10 μm, a=1.5 mm and a design power of 1 W.

Figure 3-39: Voltage required for a 1W power input vs. heater width for a 1 μm thick gold heater with s=10 μm, a=1.5 mm and a design power of 1 W.
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**Figure 3-40:** Current required for a 1W power input vs. heater width for a 1 μm thick gold heater with $s=10 \, \mu m$, $a=1.5 \, mm$, and a design power of 1 W.

**Figure 3-41:** Resistance vs. heater width for a 1 μm thick gold heater with $s=10 \, \mu m$, $a=1.5 \, mm$, and a design power of 1 W.
Final Dimensions

The heater is, therefore, chosen to be made from gold (resitivity $1.25 \times 10^{-6} \ \Omega\cdot m$, failure current density $\approx 10^{10} \ A/m^2$), with a thickness of 1 $\mu m$, a line width of 20 $\mu m$, and a line spacing of 10 $\mu m$. For these dimensions, the current density is calculated to be $5.2 \times 10^9 \ A/m^2$. This is smaller than the failure current density values reported in literature for bulk gold [57, 58].

It should also be noted that the thermal model indicated that a power input of approximately 0.1 W should be sufficient to melt the solder. For this power input, the current density reduces further to $1.6 \times 10^9 \ A/m^2$. 
Chapter 4

Fabrication Process Development

4.1 Overview

The valve being designed has multiple functional components, which were modeled in Chapter 3 to predict their performance. However, instead of directly building the final test device based on these models, it was decided to first test the key functional aspects of the device separately in short loop tests. Short loops tests are commonly used as part of a risk mitigation and optimization strategy for complex designs. They serve to demonstrate that key unit processes work independently of each other first, before testing them together in the full system where complex interactions between processes might make it harder to troubleshoot problems with any particular process. In the particular case of microfabrication, short loop tests also serve to identify any systemic fabrication variations that will bias the results and affect the mask geometry that is needed to produce the desired final device structure. In these ways, short loop tests enable optimization of the device components and the overall system.

A summary of the short loop tests performed for this work is shown in Figure 4-1. The sealing short loop is designed to test the sealing capability of the solder apparatus, whereas the
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membrane short loop is designed to test the mechanical stability of the membrane structures. This chapter will first discuss the fabrication of these short loop tests. It will then describe the fabrication process for the complete test device. Post-fabrication steps, where applicable, will also be described in detail.

Figure 4-1: Short loop tests.

Note that all test dies were fabricated using conventional microfabrication techniques in the Microsystems Technologies Laboratory (MTL) at MIT. Techniques used include (but are not limited to) photolithography, deep reactive ion etching (DRIE), electron-beam deposition of metals, low-pressure chemical vapor deposition (LPCVD) of silicon nitride and thermal oxidation of silicon.

4.2 Sealing Short Loop

The sealing short loop aims to confirm that the chosen solder material (indium) wets the "wetting substrate" (nickel), and non-wets the "non-wetting substrate" (silicon), so that a cylindrical piece of solder with a through via transforms into a solder ball upon reflow, thereby
plugging the hole (as described in Section 1.4). Although the preliminary wetting tests described in Chapter 2 have demonstrated the solder/substrate interaction, these tests cannot confirm that the solder/substrate interface is leak-free. The short loop aims to confirm that the solder seals the via without leaking. Moreover, it tries to emulate the final test device by using solder structure dimensions that are most likely to be used in the final device based on the model predictions in Section 3.2. A brief overview of the fabrication steps is shown in Figure 4-2 below.

1. The starting materials for this short loop were 500 μm thick double side polished (DSP) wafers. Initially, 0.5 μm alignment marks were etched onto the wafers, using patterned positive photoresist as an etch mask. The AME5000 tool in ICL was used for etching the silicon.

2. 1.8 μm of negative photoresist was then patterned in preparation for the metal liftoff in step 4.

3. A 100 nm titanium adhesion layer was then deposited, followed by a 700 nm nickel layer. Both metals were deposited using electron beam evaporation (eBeamAu tool in TRL).

4. The wafers were then soaked in an acetone bath for a few minutes to liftoff the metal.

5. Double thick resist (approximately 20 μm thick) was then spun onto the wafer and patterned with photolithography to define the through hole pattern; the patterned wafer was then mounted onto a quartz handle wafer using thick resist.

6. Through holes were then etched in the wafer using deep reactive ion etching (alternating SF₆ etch and C₄F₈ passivation cycles). The “mitS6” recipe (see appendix for details), on the STS1 tool in TRL, was used for this etch.

7. The test wafers were then soaked in an acetone bath overnight to dismount the handle wafer and remove any photoresist. The wafers were then cut into dies with a diesaw.
1. Alignment Marks

2. Deposit 1.5 μm of negative PR

3. Deposit 100 nm Ti + 800 nm Ni

4. Lift off in acetone bath

5. Coat with double thick PR and mount to handle wafer

6. Etch a through hole

7. Dismount handle in acetone bath

Figure 4-2: Fabrication process flow for the sealing short loop test.

A photograph of a sample test die after fabrication (but before solder assembly) is shown in Figure 4-3 below.
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Figure 4-3: Photograph of a sealing short loop test die.

The masks are designed to test variations in the via diameter, as well as in the outer diameter of the nickel ring. The variations are shown below, alongside model predictions (Section 3.2) for the required solder structure.

Table 4-1: Proposed die variations for the wetting short loop.

<table>
<thead>
<tr>
<th>Test die variations</th>
<th>Model predictions for the given variations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hole diameter $d$</td>
<td>Initial solder width $w$</td>
</tr>
<tr>
<td>400 $\mu$m</td>
<td>1.5mm</td>
</tr>
<tr>
<td></td>
<td>2mm</td>
</tr>
<tr>
<td></td>
<td>2.5mm</td>
</tr>
<tr>
<td></td>
<td>3.0mm</td>
</tr>
<tr>
<td>600 $\mu$m</td>
<td>1.5mm</td>
</tr>
<tr>
<td></td>
<td>2mm</td>
</tr>
<tr>
<td></td>
<td>2.5mm</td>
</tr>
</tbody>
</table>
### It should be noted that the hole diameters are chosen based on the diameters of commercially available pencil leads, which were intended to be used in the assembly process described in Figure 4-3 below. These hole diameters, as well as the outer diameter of the nickel ring, could have been greatly miniaturized if the indium were deposited via electroplating. However, an indium electroplating apparatus was not readily available at MIT, and shipping the dies out for electroplating would have been time- and cost-prohibitive.

The assembly of the test dies is as shown in Figure 4-4. First, a pencil lead with a diameter slightly smaller than the through hole diameter is inserted in the via, to act as a mold. The die is placed on a hot plate and heated to approximately 300°C. A few drops of glutamic acid hydrochloride (5-10%), a type of organic acid flux, are dropped on the nickel surface to remove any native oxide that might have formed during storage. Indium wire (1.0 mm diameter), soaked in the same flux, is then deposited onto the nickel part of the die. As the die is at a much higher temperature than the melting point of indium (157°C), the indium melts upon contact and forms a cylindrical shape around the pencil lead. The die is then removed from the hot plate and cooled. The pencil lead is manually removed, resulting in a structure shown in step 3 of the assembly, below (as well as Figures 4-5 and 4-6).
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1. Insert Lead
2. Deposit Melted Solder
3. Remove Lead

**Figure 4-4:** Assembly process.

Upon heating the die again, the indium reflows and balls up on the nickel ring, physically plugging the hole, as shown in Figures 4-5 and 4-6. As long as the indium wets the underlying surface around the full circumference of the hole, the hole is then expected to be sealed.

**Figure 4-5:** Reflow.

**Figure 4-6:** Photographs of actual wetting short loop dies, before and after reflow.

Before reflow (open state)  After reflow (closed state)
Visual inspection of the test dies after reflow indicates sealing of the via, as seen in Figure 4-4. Extensive pressure tests, described in Section 5.4.1, ensure that this sealing is leak-proof to within the detection limits of the testing apparatus.

Note that while the assembly process (Figure 4-4) described earlier was intended to be used for the final test dies as well, it was modified later due to other considerations. This modified assembly method for the final dies will be described in Section 4.3.

Also, note that several different layer structures were tested before selecting a 700 nm thick layer of nickel over a 100 nm thick Ti adhesion layer as the design for the final devices. Initial tests used a 100 nm thick nickel layer without an adhesion layer. This resulted in nickel that peeled off from most test dies (Figure 4-7). Dies that retained the nickel were tested; however, the nickel layer appeared to dissolve in the molten solder.

![Flux residue and Peeled-off nickel](Image)

**Figure 4-7:** Photograph of nickel peeling off silicon, due to the possible formation of an intermetallic.

It is posited that this was due to the nickel forming an intermetallic with the indium. Such intermetallics are known to have thicknesses greater than 100 nm for temperatures in the range of those that the dies experience during assembly [59]. This problem can be remedied by including an adhesion layer under the nickel to prevent peeling and by increasing the thickness...
of the nickel layer to values greater than the anticipated thickness of the intermetallic layer. If intermetallic formation were the only consideration, then the nickel layer would ideally be as thick as possible to ensure that the intermetallic layers cannot consume all of the nickel. However, as the nickel thickness continues to increase, film stress leads to cracking. For the deposition tool used here, 800 nm was to the approximate thickness limit before the onset of film cracking.

4.3 Membrane Short Loop

The membrane short loop aims to demonstrate the mechanical robustness of membranes that are also designed to provide adequate thermal isolation. A brief overview of the fabrication steps for this short loop test is shown in Figure 4-8.

Figure 4-8: Fabrication steps for the membrane short loop.
Figure 4-9: Photograph of a membrane short loop die, with a membrane inner radius of 500 μm and an outer radius of 750 μm.

1. The starting materials for this short loop were 500 μm thick double-side polished (DSP) wafers. A 500 nm thermal oxide layer was first grown on the test wafers (TubeOx5C), following an RCA clean. A 2.4 μm low-stress nitride layer was then deposited using Low-Pressure Chemical Vapor Deposition (LPCVD).

2. A 10 μm thick positive photoresist layer was then deposited and patterned to form an etch mask for the nitride. The nitride was etched in the STS3 tool in MTL-TRL using the “nitride” recipe, which utilizes SF₆ plasma to etch isotropically through the nitride.

3. The photoresist mask was then used to further etch the 500 nm oxide layer by soaking in a buffered oxide etch bath for approximately 10 minutes.

4. The photoresist was then stripped using the Asher tool in MTL-TRL. Another 20 μm layer of photoresist was then spun onto the wafer and patterned to form the membrane release etch mask; the wafer was then mounted to a handle wafer. The silicon was etched using the “hqli_u” recipe on the STS3 tool in MTL-TRL. This releases the membranes while
also simultaneously etching along the die lines, so that the dies can be separated by “snapping”. This prevents the risk of membrane rupture due to vibrations in the diesaw. After the etch, the wafers were soaked in an acetone bath to remove the photoresist, and to dismount from the handle wafer. Figure 4-9 shows a sample membrane short loop die after fabrication.

**Die variations**

Based on theoretical models, membranes with the following dimensions were fabricated and tested. The structural and theoretical predictions are listed alongside the dimensions.

**Table 4-2:** Proposed die variations for the membrane short loop.

<table>
<thead>
<tr>
<th>Inner Radius (μm)</th>
<th>Outer Radius to Inner/Boss Radius Ratio</th>
<th>Outer Radius (μm)</th>
<th>Maximum Stress (GPa) predicted by Timoshenko Model</th>
<th>Thermal Resistance (K/W) predicted (Simplified B.C. 2)</th>
<th>Thermal Resistance (K/W) predicted (Simplified B.C. 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>1.25</td>
<td>625</td>
<td>0.64</td>
<td>492</td>
<td>482</td>
</tr>
<tr>
<td>500</td>
<td>1.3</td>
<td>650</td>
<td>0.83</td>
<td>577</td>
<td>553</td>
</tr>
<tr>
<td>500</td>
<td>1.4</td>
<td>700</td>
<td>1.29</td>
<td>738</td>
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<td>1.5</td>
<td>750</td>
<td>1.85</td>
<td>885</td>
<td>982</td>
</tr>
<tr>
<td>650</td>
<td>1.25</td>
<td>812.5</td>
<td>1.09</td>
<td>491</td>
<td>476</td>
</tr>
<tr>
<td>650</td>
<td>1.3</td>
<td>845</td>
<td>1.41</td>
<td>575</td>
<td>569</td>
</tr>
<tr>
<td>650</td>
<td>1.4</td>
<td>910</td>
<td>2.18</td>
<td>734</td>
<td>723</td>
</tr>
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<td>650</td>
<td>1.5</td>
<td>975</td>
<td>3.13</td>
<td>878</td>
<td>862</td>
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<td>800</td>
<td>1.3</td>
<td>1040</td>
<td>2.13</td>
<td>573</td>
<td>644</td>
</tr>
<tr>
<td>800</td>
<td>1.4</td>
<td>1120</td>
<td>3.30</td>
<td>729</td>
<td>726</td>
</tr>
</tbody>
</table>
### 4.4 Complete Device

The fabrication steps for the complete device are shown in Figure 4-9 below.

1. The starting materials for this process are 500 μm thick double-side polished (DSP) silicon wafers. A 500 nm thermal oxide layer was first grown on the test wafers (TubeOx5C), following an RCA clean. A 2.1 μm LPCVD nitride layer was then deposited. Note that this thickness is smaller than the 2.4 μm thickness used for the membrane short loop tests. 2.4 μm is the upper limit on the deposition thickness for the VTR tool used. However, not all runs can achieve this maximum thickness.

2. The nitride layer on the top surface was then etched using the "nitride" recipe on the LAM590 tool. The oxide layer was then removed by soaking the wafers in buffered oxide etch. The bottom side was protected with a thin photoresist film during this soak.

3. Alignment marks were then patterned in a resist mask and etched 0.5 μm deep into the top surface using the AME5000 tool.
4. Negative photoresist (2 \( \mu \text{m} \) thick) was then patterned onto the bottom surface, for the subsequent liftoff step. A 50 nm chromium adhesion layer was then deposited on the bottom surface, followed by 1 \( \mu \text{m} \) gold. These metal depositions were done using the eBeamAu tool in MTL-TRL. The wafer was then placed in an acetone bath for several minutes to liftoff the metal and to remove any photoresist from the surface.

5. Photoresist was then patterned onto the bottom side, and used as a mask to etch the nitride using the “nitride” recipe on LAM590 tool. The oxide was then etched in the same tool. This step prepares the bottom side for the definition of the through via in the center (step 7).

6. 2 \( \mu \text{m} \) of negative photoresist was then patterned on the top side, for the subsequent liftoff step. A 100 nm Ti adhesion layer was then deposited on the top side, followed by an 0.8 \( \mu \text{m} \) thick nickel layer. Both these depositions were done using the eBeamAu tool in MTL-TRL.

7. In this final step, the top side of the wafer was coated with double thick photoresist (20 \( \mu \text{m} \) thick) and patterned to define the membrane region and central through hole. The wafer was then attached to a handle wafer. The “hqli_u” recipe on STS1 was then used to etch the silicon using deep reactive ion etching. This releases the membrane, completes the etching of the through via in the center, and etches along the die lines so that the dies can be separated by “snapping” without risking membrane rupture in the diesaw.

Note that through-wafer silicon etches such the ones described in all three processes above, have the risk of generating “black silicon”. Black silicon is silicon that has been roughened during the etch process to the extent that it appears black. It is near-impossible to etch and, once formed, notoriously difficult to remove. Two main causes of black silicon are an improperly functioning DRIE tool and a rough starting silicon surface. Improper ratios of passivation and etch gases, improper plasma settings or contaminants within the DRIE tool can lead to black silicon. Similarly, a starting silicon surface that might have photoresist or other residue is another possible cause of black silicon. It is important to ensure that all test wafers have been thoroughly cleaned to remove any residue before starting a DRIE process. For the
processes described in this chapter, black silicon was observed in a few instances with the “mit59” and “mit56” recipes on the STS 1 and STS 3 tools, although it is unclear whether the cause was surface roughness, a faulty recipe, or a malfunctioning tool.

![Diagram of fabrication steps](image)

**Figure 4-10**: Fabrication steps for the complete device. Mask patterns are schematic and not to scale.
Figure 4-11 to 4-13 below show photographs of the test die after step 7 of the fabrication process described in Figure 4-10.

Figure 4-11: Photograph of the front side of an F type die with a central via diameter of 580 μm and membrane inner and outer diameters of 2.0 mm and 3.6 mm respectively. Note that these are mask dimensions; actual dimensions may vary slightly depending on process biases.
Figure 4-12: Photograph of the back side of a D type die with a central via diameter of 580 μm and membrane inner and outer diameters of 2.0 mm and 3.2 mm respectively. Note that these are mask dimensions; actual dimensions may vary slightly depending on process biases.
The short loop tests described earlier inform the optimal dimensions for the complete device. The wetting short loop tests indicated that the optimal hole diameters can range from 400μm to 800μm, while the outer nickel ring diameter can range from 3.4mm to 6.8mm. The membrane short loop tests indicated that the membrane inner diameters can range from 1mm to 2.5mm, and the outer diameters can range from 1.35mm to 3.6μm. These results of tests on these structures are described in detail in the following chapter.

Based on the results of the short loop tests, as well as model predictions, the dimensions of the final device were chosen as shown in Table 4-3.
Table 4-3: Proposed die variations for the final device. Predicted values are for a 2.1 μm nitride + 0.5 μm oxide membrane. The thermal resistance calculations are performed using simplified boundary condition 2.

<table>
<thead>
<tr>
<th></th>
<th>Via diameter (μm)</th>
<th>Outer diameter of solder ring (mm)</th>
<th>Inner diameter of the membrane (mm)</th>
<th>Outer diameter of the membrane (mm)</th>
<th>Predicted failure pressure differential (Torr)</th>
<th>Predicted membrane thermal resistance (K/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>400</td>
<td>2.1</td>
<td>2.2</td>
<td>3.3</td>
<td>750</td>
<td>960</td>
</tr>
<tr>
<td>B</td>
<td>580</td>
<td>2.1</td>
<td>2.2</td>
<td>3.3</td>
<td>750</td>
<td>960</td>
</tr>
<tr>
<td>C</td>
<td>400</td>
<td>1.9</td>
<td>2.0</td>
<td>3.2</td>
<td>600</td>
<td>1100</td>
</tr>
<tr>
<td>D</td>
<td>580</td>
<td>1.9</td>
<td>2.0</td>
<td>3.2</td>
<td>600</td>
<td>1100</td>
</tr>
<tr>
<td>E</td>
<td>400</td>
<td>1.9</td>
<td>2.0</td>
<td>3.6</td>
<td>317</td>
<td>1310</td>
</tr>
<tr>
<td>F</td>
<td>580</td>
<td>1.9</td>
<td>2.0</td>
<td>3.6</td>
<td>317</td>
<td>1310</td>
</tr>
<tr>
<td>G</td>
<td>400</td>
<td>2.4</td>
<td>2.5</td>
<td>3.625</td>
<td>690</td>
<td>880</td>
</tr>
<tr>
<td>H</td>
<td>580</td>
<td>2.4</td>
<td>2.5</td>
<td>3.625</td>
<td>690</td>
<td>880</td>
</tr>
</tbody>
</table>

Since the gold heater structure had not been tested before in a short loop test due to time constraints, the final device dies vary some of the parameters that would otherwise have been tested in this short loop. For example, type A and B dies are stronger at the expense of a lower thermal resistance. Dies of the C and D type have a higher thermal resistance at the expense of a smaller central boss structure (and therefore reduced area for the gold resistive heater). Dies of the E and F type trade membrane strength for a very high thermal resistance. G and H type dies have a larger central boss (more area for the gold heater and hence reduced current density) at the expense of membrane strength and thermal resistance.

Note that Figure 4-14 shows the back side of a test wafer before the final etch step. The bulls-eye pattern used to mount the wafer to a quartz handle is clearly visible in this photograph. This pattern provides a flow path for the acetone during the dismounting step, and minimizes dismount time by providing a larger area for the acetone to dissolve the photoresist.
Note also that the process for assembling the solder structure onto the fabricated test dies was modified from what was previously planned (Figure 4-4). This previous assembly method involved pulling the pencil lead out of the central via after the solder had solidified around it. Even though indium does not wet graphite, there is enough adhesion at that interface to cause the membranes to deflect excessively while the lead is being pulled out. Because of this, the previous assembly method had a very low yield for the assembly (~5%). This method was, therefore, modified as follows. The pencil lead is not initially placed in the via. Instead indium wire (soaked in glutamic acid hydrochloride flux) is deposited onto the test die. A few drops of flux are also added to the die. Upon melting the indium balls up on the nickel ring of the central silicon island. The test die is then cooled down, and the solder is physically moved around the die with a pencil lead to expose the central via. Molten indium is very non-wetting toward the graphite and does not stick to it. As it cools down it retains this non-wetting property for a while, even after it has solidified enough to stop reflowing back over the central via. At this point, the pencil lead can be removed without any problems due to adhesion effects from the solder structure. Figure 4-15 shows a photograph of a sample test die after solder assembly.
Figure 4-15: Photograph of test die (type D) before reflow, using the modified assembly method. Notice how this method leads to a less symmetrical pre-reflow solder structure, compared to Figure 4-5.
Chapter 5

Testing

5.1 Overview

The final device aims to provide a leak-free seal at an interface that is exposed to vacuum on one side and atmospheric pressure on the other. Therefore, tests for this final device, as well as for the short loop devices, need to be able to measure any leakage through a test die when it is subjected to a pressure difference of up to 1 atm. This chapter first describes the test setup used to achieve this. It then describes the methodology used for the tests. Finally, it describes in detail the results of the short loop tests and the complete device tests.
5.2 Test Setup

The various short loop tests and final device tests require the use of two test setups: a solder reflow test setup designed to switch dies from the open state to the closed state by reflowing the solder structure, and a pressure measurement test setup designed to measure the flow rates of open dies and the leak rates of sealed dies.

5.2.1 Solder Reflow Test Setup

The method for assembling the indium solder structure onto the wetting short loop dies and the final device dies is described in Section 4.2. A hot plate (shown in Figure 5-1 below) is used in this solder structure assembly process. Moreover, for the wetting short loop test, the solder on the dies is reflowed using this hot plate.

Figure 5-1: Photograph of VWR hotplate used in the solder assembly for the wetting short loop test dies.

For the final device, however, the solder on the test dies (the fabrication of which was described in Section 4.4) is reflowed by applying a voltage across the gold resistive heater.
integrated into the die. The test setup used for this is designed to hold the test die in place in a vertical position (to allow gravity to assist the solder reflow process) while leaving the contact pads exposed on the outer surface. This test set up is shown in Figure 5-2 below. The test die to be reflowed is first attached to one of the aluminum test jig pieces (Figure 5-7) using kapton tape across the two corners of the die on which there are no electrical contact pads. Gold-plated probe tips are then put into contact with the gold electrical contact pads on the back side of the test die. Electrical leads from the probe tips are connected to a power supply, which is used to apply a voltage across (and therefore pass a current through) the gold resistive heater on the die, thereby heating the central silicon island and melting the indium solder structure.

![Figure 5-2: Schematic of electrical test setup for solder reflow.](image)
Figure 5-3 shows the Micromanipulator Series 110 manipulator stage with a 50 μm tip gold-plated probe. The electrical lead from the probe is connected to an Agilent 6614C DC power supply unit, shown in Figure 5-4. The test setup is used as follows. First, the power supply is used to apply a voltage across the gold heater. The current in the circuit is simultaneously measured using a built-in ammeter in the power supply. The voltage is increased from 2.0 V in steps of 1.0V while visually monitoring the test die for sealing.

Figure 5-3: Photograph of the Micromanipulator Series 110 manual manipulator with probe.
5.2.1 Pressure Measurement Test Setup

The pressure measurement test setup is used for both short loop tests, as well as for the final device. It is designed to measure leakage through a 1 cm x 1 cm x 0.5 mm test die when it is subjected to a pressure differential of up to 1 atm. Leakage is detected and quantified by measuring the change in pressure in a sealed space on one side of the test die over time when a given pressure difference is applied across the die. Thus, any leakage through the final device can be measured while simulating the pressure environment in which the valve will eventually operate, such as in the chip scale vacuum micro pump. The same setup is also used to measure leakage through the sealing short loop test dies and the integrity of the membrane short loop test dies.

Fig 5-5 shows a schematic diagram of this test setup. The test die is placed between two machined aluminum package plates and fixed in place using bolts. O-rings form the seal between the test die and the two package plates. These aluminum blocks were custom-designed and machined, and are fitted with KF-25 vacuum flanges that are welded on to its surface.
Chapter 5: Testing

One side of the test die is connected to atmosphere via valve 1. The other side is connected to an Adixen 2010SD roughing pump via valve 3. This roughing pump is a standard two-stage oil-sealed rotary-vane pump capable of achieving a maximum vacuum of $10^{-4}$ Torr.

The pressure on the vacuum side of the test die is measured using an MKS Series 910 pressure transducer, which is a dual micro pirani and absolute piezo transducer capable of reading pressures ranging from $10^{-5}$ Torr to 1500 Torr. Its readings are accurate to $\pm 10\%$ in the $5 \times 10^{-4}$ to $10^{-3}$ range, to $\pm 5\%$ in the $10^{-3}$ to 50 Torr range, and to $\pm 1\%$ in the 50 to 1500 Torr range. The repeatability values in those ranges are $\pm 8\%$, $\pm 2\%$ and $\pm 0.5\%$, respectively. The transducer is fitted with a KF-25 vacuum flange connection.

This transducer converts the pressure to a voltage which is sent to a gauge controller and pressure readout system (PDR 900 series). The controller sends the voltage signal to the PCI 6221 National Instruments Data Acquisition (DAQ) card installed in the PCI slot of a computer. Using the manufacturer-specified calibration curve for the pressure transducer, LabView can then record the pressure reading and store it in a file accessible by Microsoft Excel or MATLAB for subsequent data processing.

All vacuum connections in the setup are of the KF-25 type, which are rated for pressures as low as $10^{-9}$ Torr. However, the o-rings that hold the test die in place have the potential of leaking at a much higher rate than the KF-25 connections, and are the most likely source of potential test jig leakage.
Figure 5-5: Schematic showing the test setup.
Figure 5-6: Photograph of part of the test setup, including the test jig, valves, roughing pump and pressure transducer.

Figure 5-6 above shows a photograph of part of the test setup. Valve 1 is a butterfly valve, whereas valves 2 and 3 are inline and angle valves respectively. The butterfly valve has mainly two states (open or closed), but the inline and angle valves can be partially open to allow a reduced air flow. These valves have been tested by the manufacturer using a helium mass spectrometer, and have been certified to have a leak rate less than $2 \times 10^{-8}$ sccm. Figure 5-7 shows a close-up photograph of the two aluminum packaging plates that can also be seen in Figure 5-6.

Figure 5-10 shows the pressure transducer, and Figure 5-11 shows the PDR 900 series controller and readout system, as well as the connector block that plugs into the DAQ card.
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Clearance holes for 1/4-20 bolts

O-rings

KF-25 flanges

1 cm x 1 cm groove for test die

Figure 5-7: Photograph of the aluminum test jig package plates A (left) and B (right).

Figure 5-8: Engineering drawing of test jig package plate A (left). All dimensions are in inches.
Figure 5-9: Engineering drawing of test jig package plate B (right). All dimensions are in inches.

Figure 5-10: A close-up of the MKS Series 910 pressure transducer, attached to the test jig with a KF 25 vacuum flange.
Figure 5-11: Gauge controller/readout (left) and connector block (right) that transfers signals from the gauge controller to the DAQ card (not shown).

5.3 Testing Methodology

The test setup described in the previous section can be used to measure the leak rate through a test die by measuring the pressure rise on the vacuum side of the die after the other side has been exposed to atmosphere. The methodology is as follows:

1. Valves 1 and 3 are closed, while valve 2 is kept open. The roughing pump is then turned on, and valve 3 is opened slowly. This evacuates both sides of the test die in a slow and controlled manner (Figure 5-12).

   \[ \text{Vacuum} \]

   \[ \text{Vacuum} \]

   Figure 5-12: Initial conditions for the test die.

2. Valves 2 and 3 are then closed. Atmosphere is introduced approximately as a step function to one side of the die by opening valve 1 (Figure 5-13). In reality, the valve is
manually opened over a period of about three seconds. This delay is a practical necessity for this manually-controlled set up; the gradual application of the pressure difference also emulates the valve’s intended operating conditions more accurately than would a genuine step.

![Atmosphere](Atmosphere.png) ![Vacuum](Vacuum.png)

**Figure 5-13:** Final conditions for the test die.

3. The pressure rise on the vacuum side is then measured over time.

The leak rate \((L)\) of the test die can be calculated from the slope of the pressure vs. time curve, as follows.

\[
L = \frac{dP}{dt} \times \frac{V}{P_a},
\]

(5-1)

where \(P_a\) is the atmospheric pressure, \(V\) is the volume of the test setup and \(dP/dt\) is the slope of the pressure rise curve. It is important to note that the leakage calculated this way includes any leakage from the test die, as well as any parasitic leakage from the test setup itself. In order to decouple these two leakages, several blank test dies (squares of plain silicon) were tested. Since there is no leakage through a blank die, all the leakage measured this way can be attributed to the parasitic test setup leakage. In this way, the parasitic leakage can be characterized.

This method only measures the test die leakage accurately if it is sufficiently large compared to the parasitic test jig leakage. The degree to which the test die leakage needs to be larger than the parasitic leakage in order to be detectable depends on the resolution of the measurement system and the statistical repeatability of the data. Thus, the resolution with which the test die leakage can be calculated will be limited by the parasitic test jig leakage.
Note that the majority of the volume on the vacuum side of the test setup is due to the flexible tubing connecting the test setup to the roughing pump. This tubing has a radius of 1.27cm and a length of 0.61m. This gives a volume of 310cm$^3$. This is the volume used for all subsequent leak rate calculations. Note that this volume assumption neglects the dead volume of the roughing pump and the test jig, which is estimated to be approximately 10 to 20 cm$^3$. As a result, the volume assumption used for all subsequent calculations slightly underestimates the leak rate.

5.4 Test Results

This sub-section will describe the results from the sealing short loop test, the membrane short loop test and, finally, the complete device test. The test dies in this section are named according to the following convention:

- “Sx” are sealing short loop test dies, where x is the die number
- “Mx” are membrane short loop test dies, where x is the die number
- “Vx” are final valve test dies, where x is the die number
- “BDx” are blank silicon test dies, where x is the die number

5.4.1 Sealing Short Loop

This section describes the results of tests on the sealing short loop test dies whose fabrication was discussed in section 4.2.

5.4.1.1 Open Flow Rate Tests

All sealing short loop dies tested showed visible confirmation of sealing through the visible reflow of the solder upon heating. Two of these dies were further tested using the test apparatus described in Section 5.2.1 to measure the exact leak rate, if any. The first die, which will be referred to as “S1” in the rest of this sub-section, had a central via diameter of 580 µm,
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and a nickel line width of 3 mm. The second die, which will be referred to as “S2”, had a central via diameter of 400 μm and a nickel line width of 2 mm. Indium was assembled onto these dies using the method described in Section 4.2, to have an approximate width-to-height ratio of 1. Die S1 is shown in Figure 5-14.

![Before reflow (open state) vs. After reflow (closed state)](image)

**Figure 5-14** Sealing short loop die before reflow (left) and after reflow (right).

The dies were first tested in the “open” configuration using the methodology described in Section 5.3. They were then refloowed and tested again in the sealed configuration. Figure 5-15 plots the pressure rise curve for die S1 in the open configuration. As can be seen, the pressure on the vacuum side of the die rises to 760 Torr in a span of less than 20 seconds when the other side is exposed to approximately step atmosphere. This curve has a slope of approximately 50.4 Torr/second in the region between 0 and 10 seconds. This number can be converted using Equation 5-1 to get a flow rate of 1230 sccm.
**Figure 5-15:** Pressure rise curve for the sealing short loop test die S1 in the open configuration.

**Figure 5-16:** Pressure rise curves for the sealing short loop test die S2 in the open configuration.
Figure 5-16 above shows a similar plot for die S2. In this case the test die was tested three times, removing the test die from the test setup after each test and reseating it again before the start of every new test. This was done to measure any variations in the data that might arise from the way the die is seated in the test chamber, and to ensure repeatability across tests. However, as seen in the plot, the three curves are almost indistinguishable, suggesting that there is no detectable variation in the pressure rise between tests, at least for dies in the open configuration. The pressure rise is measured to be 23.7 Torr/second which translates to a flow rate of 578 sccm. Notice that this flow rate is lower than that (1230sccm) of die S1. This is reasonable given that S1 has a larger central hole diameter (580 µm), compared to that (400 µm) of S2, and hence a lower flow resistance. For a laminar, viscous and incompressible flow, the Hagen-Poiseuille equation relates the volumetric fluid flow rate \(Q\) through a cylindrical pipe to the pressure drop \(\Delta P\) as follows [60].

\[
\Delta P = \frac{128\mu L_{pipe}}{\pi d^4} Q, \tag{5-2}
\]

where \(\mu\) is the dynamic viscosity of the fluid, \(L_{pipe}\) is the pipe length and \(d\) is the pipe diameter. At room temperature \(\mu = 1.983 \times 10^{-5} \text{ kgm}^{-1}\text{s}^{-1}\) for air [60]. This equation is not strictly applicable to the present case because of the relatively short length of the via compared to its width and because the dimensions of the central via hole become wider in the indium ring than they are in the silicon die. However, the equation may still be used to provide approximate upper and lower bounds on the expected flow rates. A lower bound is obtained by assuming that the via diameter remains 0.5 mm both through the silicon die and through the entire height of the indium. Assuming a solder height of 2 mm, the effective pipe length is 2.5 mm for both dies S1 and S2 (since the wafer is 0.5 mm thick). This gives a predicted lower bound flow rate of 340 sccm for die S1 and 77 sccm for die S2, for a \(\Delta P\) of 1 atm. An approximate upper bound on flow rate is obtained by assuming that the via through the indium widens rapidly enough that the flow resistance is dominated by the short, 0.5 mm length of the via through the silicon die itself. For this case, \(L\) is considered to be equal 0.5 mm for both dies. This translates to predicted open flow rates of 1703 sccm and 385 sccm for dies S1 and S2, respectively. These estimated flow rates are reasonably consistent with the measured values of 1230 and 578 sccm to within the limits of
the approximations, such as the application of the Hagen-Poiseuille equation to a pipe with a 1:1 ratio of pipe length to pipe diameter.

It should be noted that the measured flow rate values are well within the design specifications listed in Table 2-1, suggesting that these short loop test die dimensions are good starting points on which to base the final device dimensions.

5.4.1.2 Leak Rate Tests

After the open flow rates of the test dies were measured, the dies were sealed by heating them on a hot plate (Figure 5-1) to reflow the indium structure, as described in Section 4-2. Before starting the tests, the dies were cleaned with acetone to remove any flux or other residue. Figure 5-17 shows the pressure rise curves (time-averaged over 300 seconds to remove electrical noise) for the sealed die S1. To obtain these repeatability results, leakage through the die was measured four times, and the test setup o-rings were replaced before each of the four tests. It can be seen that the pressure rises from approximately 30 mTorr to up to 0.8 Torr in a period of a few hours. All four curves show an initial transient period in which the pressure rises faster and then settles out to a constant slope. Possible reasons for the existence of this transient period are explained later in this section. The slopes of the curves in the constant-slope region are listed in Table 5-1. These slopes can be converted to leak rates using equation 5-1. These leak rates are also listed in table 5-1. It should be noted again that these leak rates are the sum of the test die leakage (if any) and the parasitic test jig leakage.
To separate out the test jig leakage from the measured leakage, three tests were also performed on a blank silicon die. Any measured leakage from these tests would capture all of the parasitic test jig leakage since there is no leakage through a blank silicon die. Figure 5-18 shows these blank die pressure rise curves overlaid on the S1 test die pressure rise curves. As with the test dies, the pressure for the blank die tests also rises from approximately 30 mTorr to up to 0.8 Torr in a period of a few hours. They also show an initial transient period in which the pressure rises faster before settling out to a constant slope. If the transient region were observed only for dies with a flux seal, the transient might be attributed to some artifact of the seal itself, such as flux residue from the test die outgassing into the chamber. However, since the transient is observed for blank dies as well as test dies, it is instead attributed to an artifact of the test jig setup. One possibility is that the test jig adsorbs water vapor and gases when not in use, and outgases them at the beginning of each experiment.
Figure 5-18: Pressure rise curves for multiple tests of a single sealing short loop test die S1 (sealed configuration), with the corresponding blank die tests. Data are time-averaged over 5 minutes.

The steady-state slopes of the pressure rise curves (and the corresponding leak rates) for die S1 and for the blank die are listed in Table 5-1 and Table 5-2 respectively. As stated before, the measurement system is only repeatable to ±2% of the pressure reading. This error propagates linearly to the leak rate calculations as well, and is reflected in the Tables 5-1 and 5-2, as well as all subsequent leak rate tables in this section, unless otherwise specified.

Uncertainty is also introduced due to the variation of the o-ring seating from test to test. Changing o-rings before a new test and reseating the test die in the test jig leads to variation in the pressure rise curves, even for the tests with the same test die. This variation can be seen in the "spread" of the pressure rise curves in Figure 5-18. This scatter is much larger than the error rate due to repeatability limits of the sensor. It is important to note that while the number of tests shown in this figure is not large enough to draw statistically significant conclusions about the
average or standard deviation of the two sets of curves, the curves also do not show any visible “bunching” between the test dies and the blank dies. In other words, the test die leakage (if there is any present at all) is not detectable above the parasitic test jig leakage which is on the order of $10^{-4}$ sccm.

These data are, therefore, consistent with a leak-free seal. On the other hand, they are also consistent with a seal that leaks at a level below the parasitic test jig leakage. However, it is challenging to quantify this leakage to a resolution beyond the level of the test jig leakage, without statistically significant amounts of tests. This is discussed in more detail in Section 6.2.

**Table 5-1:** Leak rates for multiple tests for the sealing short loop test die S1. Regression performed over data points taken 5 hours to 25 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 – Test 1</td>
<td>(3.79 ± 0.08) x 10^{-2}</td>
<td>(2.57 ± 0.05) x 10^{-4}</td>
</tr>
<tr>
<td>S1 – Test 2</td>
<td>(3.73 ± 0.07) x 10^{-2}</td>
<td>(2.53 ± 0.05) x 10^{-4}</td>
</tr>
<tr>
<td>S1 – Test 3</td>
<td>(2.74 ± 0.05) x 10^{-2}</td>
<td>(1.85 ± 0.04) x 10^{-4}</td>
</tr>
<tr>
<td>S1 – Test 4</td>
<td>(2.95 ± 0.06) x 10^{-2}</td>
<td>(2.00 ± 0.04) x 10^{-4}</td>
</tr>
<tr>
<td><strong>Average</strong></td>
<td></td>
<td>(2.24 ± 0.36) x 10^{-4}</td>
</tr>
</tbody>
</table>

**Table 5-2:** Leak rates for multiple tests for BD1. Regression performed over data points taken 5 hours to 25 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD1 – Test 1</td>
<td>(3.52 ± 0.07) x 10^{-2}</td>
<td>(2.38 ± 0.05) x 10^{-4}</td>
</tr>
<tr>
<td>BD1 – Test 2</td>
<td>(3.13 ± 0.06) x 10^{-2}</td>
<td>(2.12 ± 0.04) x 10^{-4}</td>
</tr>
</tbody>
</table>
Figures 5-19 and 5-20 show similar pressure rise curves for die S2 after it is sealed and for the corresponding blank die. The slopes of these curves in the steady-state region are tabulated in Tables 5-3 and 5-4. Again, to within the scatter of data, the leak rates measured for Test Die 2 and the corresponding blank die are the same, indicating that any actual leakage through Test Die 2 is not detectable above the parasitic test jig leakage.
Figure 5-20: Pressure rise curves for multiple tests of the sealing short loop test die S2 (sealed configuration), along with the corresponding blank die tests. Data are time-averaged over 5 minutes.

Table 5-3: Leak rates for multiple tests for the sealing short loop test die S2. Regression performed over data points taken 4 hours to 9 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2 - Test 1</td>
<td>$(7.60 \pm 0.15) \times 10^{-2}$</td>
<td>$(5.15 \pm 0.10) \times 10^{-4}$</td>
</tr>
<tr>
<td>S2 - Test 2</td>
<td>$(8.84 \pm 0.18) \times 10^{-2}$</td>
<td>$(5.99 \pm 0.12) \times 10^{-4}$</td>
</tr>
<tr>
<td>S2 - Test 3</td>
<td>$(6.65 \pm 0.13) \times 10^{-2}$</td>
<td>$(4.51 \pm 0.09) \times 10^{-4}$</td>
</tr>
<tr>
<td>S2 - Test 4</td>
<td>$(5.50 \pm 0.11) \times 10^{-2}$</td>
<td>$(3.73 \pm 0.07) \times 10^{-4}$</td>
</tr>
<tr>
<td>Average</td>
<td></td>
<td>$(4.85 \pm 0.96) \times 10^{-4}$</td>
</tr>
</tbody>
</table>
Table 5-4: Leak rates for multiple tests for blank die 2. Regression performed over data points taken 4 hours to 9 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD2 – Test 1</td>
<td>(7.95 ± 0.16) x 10^{-2}</td>
<td>(5.39 ± 0.11) x 10^{-4}</td>
</tr>
<tr>
<td>BD2 – Test 2</td>
<td>(6.57 ± 0.13) x 10^{-2}</td>
<td>(4.46 ± 0.09) x 10^{-4}</td>
</tr>
<tr>
<td>BD2 – Test 3</td>
<td>(6.51 ± 0.13) x 10^{-2}</td>
<td>(4.42 ± 0.08) x 10^{-4}</td>
</tr>
<tr>
<td><strong>Average</strong></td>
<td></td>
<td>(4.75 ± 0.56) x 10^{-4}</td>
</tr>
</tbody>
</table>

An important difference between Figure 5-18 and Figure 5-20 is that the transience for S2 and BD2 is considerably more pronounced than that for S1 and BD1. The steady-state slopes of all dies in Figure 5-20 are also approximately twice the steady-state slopes of the dies in Figure 5-18. There was no difference in the way the four dies were processed, except that the experiments for S2 and BD2 were performed approximately three months after the experiments for the other two dies S1 and BD1. As stated previously, one possible reason for this increased transience might be the test jig adsorbing gases and water vapor over time, which it slowly releases during the test causing a higher initial pressure rise and a higher steady-state pressure rise. One possible solution to this problem is described in Section 6.2.

The tests for BD1 and BD2 are shown in Figure 5-21 below, to better compare the two transience effects.
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5.4.2 Membrane Short Loop

This section describes the results of tests on the membrane short loop test dies whose fabrication was discussed in section 4.3.

The testing methodology is similar to that described in Section 5.3, but with a slight modification. Instead of evacuating one side of the die to vacuum, these tests vary the pressure $P_x$ to which the low pressure side is evacuated. The die is held in this configuration for approximately 5 minutes to ensure that membrane remains intact at this pressure differential. It is possible that 5 minutes might not be long enough to ensure the stability of the membrane, and that micro cracks that initiate at a lower pressure differential only manifest themselves in membrane failure at a higher pressure differential. To account for this, it might be worth increasing the holding time from 5 minutes to a few hours for future tests. For this test, $P_x$ is progressively reduced from 700 Torr to vacuum at intervals of 50 to 100 Torr. Thus, the membrane is subjected to progressively higher pressure differentials of up to one atmosphere.

Figure 5-21: Pressure rise curves for blank dies BD1 and BD2. Data are time-averaged over 5 minutes.
An important characteristic that needs to be considered while performing these tests is the asymmetry of the membranes. Recall that the fabrication process produces a bilayer membrane of oxide and nitride, instead of a single layer of nitride because of the necessity of including an etch stop for the final silicon etch step. The configuration with the nitride layer facing higher pressure is called “configuration 1” and that with the oxide layer facing higher pressure is called “configuration 2”. It is not readily apparent which configuration is stronger, but tests indicate that configuration 1 seems to be slightly stronger than configuration 2, as will be seen later in this section. A statistically significant number of tests have not been done to fully back this claim, however.

A sample test is shown in Figure 5-22 below.

![Figure 5-22](image)

**Figure 5-22:** Pressure rise curve for a membrane short loop test die (2.2 mm inner diameter, 3.3 mm outer diameter) in configuration 1, as the pressure on the vacuum side is successively decreased from 700 Torr to 0 Torr in 50 Torr intervals. The time is re-zeroed at the start of each new pressure step. Membrane breakage would appear as an abrupt increase in measured pressure; in this case, the membrane did not break.
Five dies (M1, M2, M3, M4 and M5) were tested in this short loop test. Table 5-5 below lists the dimensions of the test dies, along with predictions and experimental measurements of the pressure differences across the membrane at which they fail (if any). The yield for the membrane short loop test wafers was very low because of tool problems that were unrelated to the fabrication process flow. As a result, only a handful of membrane short loop test dies were tested.

Dies M1, M2 and M3 were of the same type and were the most likely to fail based on model predictions. They failed in configuration 2 at pressure differentials very similar to ones predicted by the model. Dies 4 and 5 were over-designed, and as predicted they did not fail at a 1 atmosphere pressure differential.

### Table 5-5: Dimensions, predictions, and test results for membrane short loop test dies. All membranes were 2.4 μm thick silicon nitride with a 0.5 μm oxide layer. The predicted thermal resistance values are calculated using the simplified boundary condition 2

<table>
<thead>
<tr>
<th>Die ID Number</th>
<th>Inner Dia (mm)</th>
<th>Outer Dia (mm)</th>
<th>Failure Pressure Differential in Torr (Predicted)</th>
<th>Failure Pressure Differential in Torr (1st config)</th>
<th>Failure Pressure Differential in Torr (2nd config)</th>
<th>Predicted Thermal Resistance of the Membrane (K/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>2.5</td>
<td>3.75</td>
<td>720</td>
<td>Did not fail</td>
<td>650</td>
<td>830</td>
</tr>
<tr>
<td>M2</td>
<td>2.5</td>
<td>3.75</td>
<td>720</td>
<td>Did not fail</td>
<td>750</td>
<td>830</td>
</tr>
<tr>
<td>M3</td>
<td>2.5</td>
<td>3.75</td>
<td>720</td>
<td>Did not fail</td>
<td>750</td>
<td>830</td>
</tr>
<tr>
<td>M4</td>
<td>2.2</td>
<td>2.86</td>
<td>2070</td>
<td>Did not fail</td>
<td>Did not fail</td>
<td>570</td>
</tr>
<tr>
<td>M5</td>
<td>1.3</td>
<td>1.82</td>
<td>3840</td>
<td>Did not fail</td>
<td>Did not fail</td>
<td>733</td>
</tr>
</tbody>
</table>
More tests would be needed to fully validate the stress model for the membrane; however, these results serve as an initial indicator to guide the design of the full test devices. This allows us to move forward with the final device fabrication, while using the complete device tests to get more complete data on the various membranes.

5.4.3 Complete Device

This section describes the results of tests on the final device test dies whose fabrication was discussed in Section 4.4. It will first describe open flow rate tests for all test dies. The gold resistive heater tests used to reflow the solder will then be described in detail. This will be followed by leak rate tests for the sealed test dies. The section will conclude with membrane tests, to measure the integrity of the silicon nitride membranes and their ability to withstand a 1 atm pressure differential.

The four dies tested will be referred to as V1, V2, V3 and V4 respectively. The first three dies were identical with a central via diameter of 400 μm, a membrane inner diameter of 2.2 mm, a membrane outer diameter of 3.3 mm. Die V4 had a central via diameter of 400 μm, a membrane inner diameter of 2.0 mm, a membrane outer diameter of 3.2 mm. All dies also had a gold resistive heater on the backside, a feature not tested in separate short loop tests.

5.4.3.1 Open Flow Rate Tests

The test dies were tested using the pressure measurement test setup described in Section 5.2 to measure flow rates of open dies, such as the one shown in Figure 5-23 below.
Figure 5-23: Photograph of final test device before reflow.

The results for the open flow rate tests for test dies are shown in Figure 5-24. As can be seen, for three of the dies (V1, V2 and V3), the pressure on the vacuum side of the die rises to 760 Torr in a span of less than a minute from when the other side is exposed to atmosphere (approximately in a step as described previously). It takes over 5 minutes for the die V4 to reach atmospheric pressure, even though the nominal central via diameter for this die is the same (400 μm) as for the other three dies. This is because the solder assembly process leads to variations in the hole diameter in the non-reflowed solder structure. As a result, the effective diameter of the flow path for the air can be smaller than the nominal via diameter of the die.

The slopes of these curves are listed in Table 5-6. The corresponding flow rates are calculated using Equation 5-1 and are also listed in Table 5-6. It should be noted that these flow rates range from 63 to 399 sccm (over a pressure differential ranging from 100 to 760 Torr). This is well within the design specifications listed in Table 1-1.
Figure 5-24: Pressure rise curves for four complete device test dies in the open configuration.

Table 5-6: Flow rate of 4 final device test dies in the open configuration.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/sec)</th>
<th>Open Flow Rate (scccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>16.35 ± 0.08</td>
<td>399 ± 2</td>
</tr>
<tr>
<td>V2</td>
<td>12.16 ± 0.06</td>
<td>297 ± 1</td>
</tr>
<tr>
<td>V3</td>
<td>10.06 ± 0.05</td>
<td>245 ± 1</td>
</tr>
<tr>
<td>V4</td>
<td>2.60 ± 0.01</td>
<td>63 ± 0</td>
</tr>
</tbody>
</table>

5.4.3.2 Solder Reflow Tests

After completing the open flow rate measurements, the test dies were sealed by applying a voltage across the leads of the gold resistive heater, as described in Section 5.2. Figure 5-25 shows a test die after reflow. This step aims to simulate the in-situ thermal actuation of the test device when it will be used in its final application.
Figure 5-25: Photograph of a complete valve chip after reflow.

The current, voltage and power required to reflow the solder are tabulated in Table 5-7 below. Note that V1, V2 and V3 all have similar dimensions. The steady-state reflow power for these dies was measured to be between 0.28 and 0.3128 W, which is well within the power limit of 1 W specified for the valve in Section 1.3. Moreover, the indium solder melts at 157°C (430 K). Assuming a room temperature of 20°C (293 K), the membrane sees a 137 K rise in temperature at the time of reflow. The thermal resistance of the membrane is then calculated by dividing this temperature rise by the power input. This gives membrane thermal resistance values ranging from 438 to 489 K/W. The thermal model described in Section 3.3 predicts a membrane thermal resistance values of approximately 1100 K/W for a simplified boundary condition model 2. It is possible that the membrane has fillets around the edges, which would reduce the predicted effective thermal resistance. The extent of these fillets, if they exist, is not known, and procedures for estimating this fillet length are described in Section 6.2. For a 75 µm fillet length (typical for a common recipe (such as “hqli_u” used on the etcher tool), the predicted thermal resistance value for V1, V2 and V3 is now approximately 844 K/W, which is closer to the measured value. The discrepancy is explained by the hypothesis that the temperature at which solder reflow is visible might be slightly higher than the melting temperature of indium, which might result in overestimating the measured reflow power. This would in turn underestimate the measured value the membrane thermal resistance.
Thus, the experimental thermal resistance values are in the same order of magnitude as the predictions, thereby validating the accuracy of the thermal model, at least to a first-order.

Table 5-7: Voltage, current and power required to reflow the solder. Thermal resistance predictions use simplified boundary condition 2

<table>
<thead>
<tr>
<th></th>
<th>Reflow voltage (V)</th>
<th>Reflow current (mA)</th>
<th>Reflow power (W)</th>
<th>Membrane thermal resistance (K/W)</th>
<th>Predicted membrane thermal resistance without fillets (K/W)</th>
<th>Predicted membrane thermal resistance with a 75 μm fillet (K/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>v1</td>
<td>7.0</td>
<td>40.0</td>
<td>0.28</td>
<td>489</td>
<td>1100</td>
<td>844</td>
</tr>
<tr>
<td>v2</td>
<td>8.0</td>
<td>38.8</td>
<td>0.3104</td>
<td>441</td>
<td>1100</td>
<td>844</td>
</tr>
<tr>
<td>v3</td>
<td>8.0</td>
<td>39.1</td>
<td>0.3128</td>
<td>438</td>
<td>1100</td>
<td>844</td>
</tr>
<tr>
<td>v4</td>
<td>Not measured</td>
<td>Not measured</td>
<td>Not measured</td>
<td>Not measured</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The measured reflow voltage and current values in Table 5-7 can also be used to calculate the electrical resistance of the heater at reflow. Electrical resistance calculated this way is compared in Table 5-8 to the electrical resistance measured before the reflow experiments, using a multimeter. Note that the electrical resistance of the heater at reflow is higher than that before reflow. This is expected since gold has a positive temperature coefficient of resistance ($\alpha$), so that resistance increases with temperature as given by the general equation

$$R = R_{ref}[1 + \alpha(T - T_{ref})],$$  \hspace{1cm} (5-3)

where $R$ is the electrical resistance at a temperature $T$ and $R_{ref}$ is the electrical resistance at a reference temperature $T_{ref}$. Table 5-8 also lists the temperature coefficient of resistance values calculated this way, using the electrical resistance before reflow for $R_{ref}$ and that after reflow for $R$. The reference temperature $T_{ref}$ is assumed to be 20°C (293 K), and $T$ is assumed to be 157°C.
(430 K), which is the melting temperature of indium. It is seen that the measured temperature coefficient of resistance values range from 0.0020 to 0.0074 K\(^{-1}\), which is very close to the actual value reported in literature of 0.0034 K\(^{-1}\). The discrepancy can be attributed to the sensitivity of the calculated \(\alpha\)-values to resistance values at reflow, as well as to the reflow temperature. For example, if the measured value of resistance for die V2 at reflow was 175 \(\Omega\) instead of 206 \(\Omega\), it would translate to an \(\alpha\) value of 0.0042 K\(^{-1}\), instead of 0.0064 K\(^{-1}\). Moreover, the temperature at which reflow is visible might be slightly higher than the melting temperature of indium, which might result in overestimating the value of \(\alpha\).

However, these results indicate that, to first order, the measured \(\alpha\)-values match literature values. This lends further credibility to the heater model and design.

**Table 5-8:** Heater electrical resistance before and after reflow.

<table>
<thead>
<tr>
<th></th>
<th>Measured heater electrical resistance ((\Omega)) before reflow experiments</th>
<th>Heater electrical resistance ((\Omega)) at reflow</th>
<th>Calculated temperature coefficient of resistance (K(^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>138</td>
<td>175</td>
<td>0.0020</td>
</tr>
<tr>
<td>V2</td>
<td>110</td>
<td>206</td>
<td>0.0064</td>
</tr>
<tr>
<td>V3</td>
<td>102</td>
<td>205</td>
<td>0.0074</td>
</tr>
<tr>
<td>V4</td>
<td>83</td>
<td>Not measured</td>
<td></td>
</tr>
</tbody>
</table>

The reflowed dies were also weighed and their weights were compared to dies without solder, in order to estimate the amount of solder on each die. The solder amounts on dies V1, V3 and V4 were calculated to be 14, 9 and 7 mg respectively. These are lower bounds since the test dies chip as a result of seating and reseating in the test apparatus. These chips weigh approximately 3-5 mg, and each of the dies weighed had a portion chipped. Note also that there is some variation in the amount of solder added from die to die. This is another reason for the scatter in the measured solder weights.
A different way to estimate solder weights is to estimate the volume of the solder structures and use the density of indium to solve for the weight. Test die pictures after reflow indicate that the solder structure can be approximately modeled as a sphere with a radius of 1mm. For a density of indium of 7310 kg/m³, this gives a weight of 30 mg. Note that both these methods of calculating the solder structure weight are only approximate, but provide a good order-of-magnitude estimate.

5.4.3.3 Leak Rate Tests

The sealed test dies were tested for measure any potential leakage through them. First, one die (V2) was tested repeatedly to explore any variations in the measurements due to the way the test die is seated in the test setup, and to ensure repeatability across tests. The die was reseated on the o-ring before each test. These results are shown in Figure 5-26. The pressure rises from approximately 100 mTorr to more than 1 Torr in 7 hours. Like the sealing short loop test dies, these dies exhibit an initial transient period in which pressure rises more rapidly than in steady state. The slopes for the steady-state region (as well as the corresponding leak rates) are listed in Table 5-9. The steady slope for V2-Test1 seems to be higher than average. This is likely an outlier, perhaps due to the way that the o-ring was seated; this hypothesis will be confirmed in Section 5.4.4.
Figure 5-26: Pressure rise curves for multiple tests for test die V2 in the sealed configuration. Data are time-averaged over 5 minutes.

Table 5-9: Leak rates for multiple tests of a final device test die V2 in the sealed configuration. Regression performed over data points taken 4 hours to 7 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th>Test</th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V2 - Test 1</td>
<td>(7.94 ± 0.16) x 10^{-2}</td>
<td>(5.38 ± 0.10) x 10^{-4}</td>
</tr>
<tr>
<td>V2 - Test 2</td>
<td>(7.45 ± 0.15) x 10^{-2}</td>
<td>(5.05 ± 0.10) x 10^{-4}</td>
</tr>
<tr>
<td>V2 - Test 3</td>
<td>(6.90 ± 0.14) x 10^{-2}</td>
<td>(4.68 ± 0.09) x 10^{-4}</td>
</tr>
<tr>
<td>V2 - Test 4</td>
<td>(14.0 ± 0.28) x 10^{-2}</td>
<td>(9.51 ± 0.19) x 10^{-4}</td>
</tr>
<tr>
<td><strong>Average</strong></td>
<td></td>
<td>(6.16 ± 2.25) x 10^{-4}</td>
</tr>
</tbody>
</table>
With repeatability across tests characterized, three other dies (V1, V3, and V4) were tested as shown in Figure 5-27 to demonstrate repeatability across dies. It can be seen that the pressure rises from approximately 100 mTorr to approximately 1 Torr in 6 hours. The slopes for the steady-state region (as well as the corresponding leak rates) are listed in Table 5-10.

As mentioned previously, these measured leak rates are the sum of any actual test die leakage and the parasitic test jig leakage. To isolate the test jig leakage, the pressure rise curves for the 4 test dies are overlaid on the pressure rise curves for a blank die, as seen in Figure 5-28. To within the limits of scatter in the data, both sets of curves are identical in the transition region as well as the steady-state region. The slopes of the blank die test die curves and the corresponding leak rates in the steady-state region are listed in Tables 5-10 and 5-11.

These data are consistent with a leak-free seal, although higher resolution testing will need to be done in order to quantitatively measure the seal’s leak rate.

![Figure 5-27](image-url)  
**Figure 5-27:** Pressure rise curves for multiple test dies in the sealed configuration. Data are time-averaged over 5 minutes.
Figure 5-28: Pressure rise curves for multiple test dies (sealed), along with the corresponding blank dies. Data are time-averaged over 5 minutes.

Table 5-10: Leak rates for representative tests of 4 final device test dies in the sealed configuration. Regression performed over data points taken 4 hours to 7 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>(8.95 ± 0.17) x 10^2</td>
<td>(6.07 ± 0.12) x 10^-4</td>
</tr>
<tr>
<td>V2 - Test 2</td>
<td>(7.45 ± 0.15) x 10^2</td>
<td>(5.05 ± 0.10) x 10^-4</td>
</tr>
<tr>
<td>V3</td>
<td>(7.99 ± 0.16) x 10^2</td>
<td>(5.42 ± 0.11) x 10^-4</td>
</tr>
<tr>
<td>V4</td>
<td>(7.56 ± 0.15) x 10^2</td>
<td>(5.12 ± 0.10) x 10^-4</td>
</tr>
<tr>
<td>Average</td>
<td></td>
<td>(5.41 ± 0.46) x 10^-4</td>
</tr>
</tbody>
</table>
Table 5-11: Leak rates for 3 tests of a blank die in the sealed configuration. Regression performed over data points taken 4 hours to 7 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer, whereas the uncertainty value in the average represents scatter in the data.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD2 – Test 1</td>
<td>(7.98 ± 0.16) x 10²</td>
<td>(5.41 ± 0.11) x 10⁻⁴</td>
</tr>
<tr>
<td>BD2 – Test 2</td>
<td>(6.57 ± 0.13) x 10²</td>
<td>(4.46 ± 0.09) x 10⁻⁴</td>
</tr>
<tr>
<td>BD2 – Test 3</td>
<td>(6.51 ± 0.13) x 10²</td>
<td>(4.42 ± 0.09) x 10⁻⁴</td>
</tr>
<tr>
<td>Average</td>
<td></td>
<td>(4.76 ± 0.56) x 10⁻⁴</td>
</tr>
</tbody>
</table>

5.4.4 Repeatability of leak rate tests and potential sources of data scatter

This section will explore the limits of repeatability of the test data, as well as possible explanations for the scatter of data that is observed. The sealing short loop tests as well as the main device tests (Figures 5-18, 5-20, 5-26, 5-28) indicate considerable variation in the pressure rise curves, both between tests on different dies as well as between tests on the same die. There are two important trends in the scatter of data found in all of these pressure rise curves. First, all curves show some degree of transience at the beginning of each test. Second, the pressure rise curves for dies S1 and BD1 (Figure 5-18) have much shorter transient times and slightly smaller steady-state slopes than those for all other test dies. Figure 5-29 captures this difference in transience times well.
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Figure 5-29: Pressure rise curves for tests on the BD1 and BD2 tests. Data are time-averaged over 5 minutes.

It is proposed that these observations are a result of the test setup adsorbing contaminants over time and outgassing them during the tests. This hypothesis is supported by the following arguments. First, recall that the tests for the die S1 and BD1 were performed approximately three months before all other leak rate tests. There was no other fundamental difference in the way the tests were performed. This suggests that something changed with the test setup over time. The most likely explanation is that the test jig (which is made of aluminum) adsorbed water vapor and other gases over time. To test this hypothesis, two sets of tests (BD3_set1 and BD3_set2) were performed with a third blank die, with reseating between the two sets but without reseating between the tests in the same set. That is, the test die was reseated at the beginning of BD3_set1 - Test 1 and BD3_set2 - Test 1, but not at the beginning of any other tests in the two sets.

Figure 5-30 shows the BD3_set2 tests along with the tests for dies BD1 and BD2. Recall that for all previous tests, the test die was reseated and the o-rings changed before every test. Not reseating this third die BD3 between tests minimizes the time the vacuum side of the test setup is exposed to atmosphere in between tests to a few seconds. This should minimize the readsorption of contaminants by the test setup. Indeed Figure 5-30 and Figure 5-31 show that the BD3_set2
tests start out closer to the BD2 test levels, but eventually end up at the original levels of BD1. This confirms the outgassing hypothesis.

Figure 5-30: Pressure rise curves for BD3 dies superimposed on the BD1 and BD2 tests. Data are time-averaged over 5 minutes.
Figure 5-31: Pressure rise curves for BD3 dies superimposed on the BD1 and BD2 tests. Data are time-averaged over 5 minutes.

Table 5-12: Leak rates for multiple tests for second set of blank die 3 tests, as well as BD2 and BD1 tests. Regression performed over data points taken 1 hour to 2 hours from the start of the experiment. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer.

<table>
<thead>
<tr>
<th></th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BD2 – Test 1</strong></td>
<td>(1.42 ± 0.28) x 10^{-1}</td>
<td>(9.63 ± 0.19) x 10^{-4}</td>
</tr>
<tr>
<td><strong>BD2 – Test 2</strong></td>
<td>(1.03 ± 0.20) x 10^{-1}</td>
<td>(6.98 ± 0.14) x 10^{-4}</td>
</tr>
<tr>
<td><strong>BD2 – Test 3</strong></td>
<td>(1.26 ± 0.24) x 10^{-1}</td>
<td>(8.54 ± 0.18) x 10^{-4}</td>
</tr>
<tr>
<td><strong>BD3_set2 – Test 1</strong></td>
<td>(7.08 ± 0.14) x 10^{-2}</td>
<td>(4.80 ± 0.10) x 10^{-4}</td>
</tr>
<tr>
<td><strong>BD3_set2 – Test 2</strong></td>
<td>(5.88 ± 0.12) x 10^{-2}</td>
<td>(3.99 ± 0.08) x 10^{-4}</td>
</tr>
<tr>
<td><strong>BD3_set2 – Test 3</strong></td>
<td>(5.35 ± 0.11) x 10^{-2}</td>
<td>(3.63 ± 0.07) x 10^{-4}</td>
</tr>
<tr>
<td>BD1 – Test 1</td>
<td>((5.62 \pm 0.11) \times 10^2)</td>
<td>((3.81 \pm 0.08) \times 10^{-4})</td>
</tr>
<tr>
<td>BD1 – Test 2</td>
<td>((4.19 \pm 0.08) \times 10^2)</td>
<td>((2.84 \pm 0.06) \times 10^4)</td>
</tr>
<tr>
<td>BD1 – Test 3</td>
<td>((5.15 \pm 0.10) \times 10^2)</td>
<td>((3.49 \pm 0.07) \times 10^{-4})</td>
</tr>
</tbody>
</table>

Figure 5-33 shows the BD3_set1 tests alongside tests for BD1 and BD2. Two important observations can be made from these tests. First, the observed transience reduces significantly over successive tests (just like with the BD3_set2 tests in Figure 5-31), until eventually the pressure rise curves are almost straight lines. Again, this supports the hypothesis that test chamber outgassing is the main cause of transience in the pressure rise tests. Second, Figure 5-33 and Table 5-13 show that the steady-state slopes for BD3_set1 tests are all higher than those for BD1 and BD2 tests. This indicates that die seating might play an important role in the scatter of data as well. It is posited that the die was not properly seated at the start of the BD3_set1 tests, and this resulted in a higher steady-state slope that persisted through successive tests, even as the transience effects died out. Recall V2 – Test 4 in Figure 5-24 had such a higher slope than the other corresponding curves as well, and is probably due to the same reason.

Note also that the BD3_set2 tests (Figure 5-30) start out at a level lower than the BD2 tests. This is probably because the BD3_set1 tests conducted immediately before the BD3_set2 tests, resulted in considerable desorption of contaminants from the test chamber (since the die was not reseated in these tests, and the cumulative run time of these tests was close to a day). Since the test chamber was only exposed to atmosphere for a few minutes between the end of the BD3_set1 tests and the start of the BD3_set2 tests, it most likely did not have sufficient time to readsorb enough contaminants for the pressure curves to go back to BD1 levels.

Thus, the above discussion indicates that the variation in the pressure rise curves may be caused due to test chamber outgassing as well as due to variations in the quality of the die seating. More tests will be needed to accurately determine the proportion to which each factor contributes to the test data scatter. However, it should be noted that of all the tests, only BD3_NR2 and V2 – Test 4 had the problem of a higher steady-state slope than average, but all
tests showed transience. This indicates that test chamber outgassing is a bigger problem for data scatter, than improper test die seating. Section 6.2 explores ways for reducing this data scatter.

**Figure 5-32:** Pressure rise curves for the second set of BD3 tests. Data are time-averaged over 5 minutes.
**Figure 5-33:** Pressure rise curves for the second set of BD3 tests, along with the BD1 and BD2 tests. Data are time-averaged over 5 minutes.

**Table 5-13:** Leak rates for BD3_set1 tests. Regression performed over data points taken 0.5 to 1 hour, 0.5 to 2 hours, and 1.5 to 4 hours from the start of the experiment for Test 1, Test 7, and the remaining tests respectively. Note that the uncertainty values listed for the leak rate and pressure rise values for the individual tests represent errors in repeatability due to limits of the pressure transducer.

<table>
<thead>
<tr>
<th>BD3_set1 - Test</th>
<th>Pressure Rise (Torr/hr)</th>
<th>Leak Rate (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$(2.80 \pm 0.06) \times 10^{-1}$</td>
<td>$(1.90 \pm 0.03) \times 10^{-3}$</td>
</tr>
<tr>
<td>2</td>
<td>$(1.59 \pm 0.03) \times 10^{-1}$</td>
<td>$(1.08 \pm 0.02) \times 10^{-3}$</td>
</tr>
<tr>
<td>3</td>
<td>$(1.28 \pm 0.03) \times 10^{-1}$</td>
<td>$(8.69 \pm 0.17) \times 10^{-4}$</td>
</tr>
<tr>
<td>4</td>
<td>$(1.18 \pm 0.02) \times 10^{-1}$</td>
<td>$(7.98 \pm 0.16) \times 10^{-4}$</td>
</tr>
<tr>
<td>5</td>
<td>$(1.12 \pm 0.02) \times 10^{-1}$</td>
<td>$(7.59 \pm 0.15) \times 10^{-4}$</td>
</tr>
<tr>
<td>6</td>
<td>$(1.05 \pm 0.02) \times 10^{-1}$</td>
<td>$(7.13 \pm 0.14) \times 10^{-4}$</td>
</tr>
<tr>
<td>7</td>
<td>$(1.02 \pm 0.02) \times 10^{-1}$</td>
<td>$(6.93 \pm 0.14) \times 10^{-4}$</td>
</tr>
</tbody>
</table>
5.4.3.4 Membrane Integrity Tests

The final device dies were also tested to measure the strength of the membranes. The test results (along with the model predictions from Section 3.4) are listed in Table 5-14.

Table 5-14: Membrane integrity tests. Predicted values are for a 2.1 μm nitride + 0.5 μm oxide membrane

<table>
<thead>
<tr>
<th></th>
<th>Inner Dia (mm)</th>
<th>Outer Dia (mm)</th>
<th>Predicted Failure Pressure Differential in Torr (no fillets, no overetch)</th>
<th>Predicted Failure Pressure Differential in Torr (75 μm fillets, no overetch)</th>
<th>Predicted Failure Pressure Differential in Torr (150 μm overetch, no fillets)</th>
<th>Failure Pressure Differential in Torr (1st config – higher pressure on nitride)</th>
<th>Failure Pressure Differential in Torr (2nd config – higher pressure on oxide)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>2.2</td>
<td>3.3</td>
<td>750</td>
<td>1210</td>
<td>274</td>
<td>Did not fail</td>
<td>Not tested</td>
</tr>
<tr>
<td>V2</td>
<td>2.2</td>
<td>3.3</td>
<td>750</td>
<td>1210</td>
<td>274</td>
<td>Did not fail</td>
<td>Not tested</td>
</tr>
<tr>
<td>V3</td>
<td>2.2</td>
<td>3.3</td>
<td>750</td>
<td>1210</td>
<td>274</td>
<td>Did not fail</td>
<td>Not tested</td>
</tr>
<tr>
<td>V4</td>
<td>2.0</td>
<td>3.2</td>
<td>600</td>
<td>844</td>
<td>243</td>
<td>Did not fail</td>
<td>Not tested</td>
</tr>
<tr>
<td>V5</td>
<td>2.0</td>
<td>3.6</td>
<td>317</td>
<td>510</td>
<td>196</td>
<td>Did not fail</td>
<td>650 to 760</td>
</tr>
<tr>
<td>V6</td>
<td>2.0</td>
<td>3.6</td>
<td>317</td>
<td>510</td>
<td>196</td>
<td>650 to 760 to 7torr</td>
<td>-</td>
</tr>
<tr>
<td>V7</td>
<td>2.0</td>
<td>3.6</td>
<td>317</td>
<td>510</td>
<td>196</td>
<td>Did not fail</td>
<td>650 to 760</td>
</tr>
</tbody>
</table>

Note that the first column for the predicted failure stress includes values of stress predicted by the membrane model without any non-idealities in the fabrication process. However, several non-idealities can exist in the fabrication process. First, a through-wafer etch (last step of the fabrication process described in Section 4.4) that is not perfectly anisotropic will result in overetching of the sidewalls. This will cause the membranes to be become larger than
they were initially designed to be and, therefore, weaker. Second, a through-wafer etch that is non-uniform across a trench will result in a "U-shaped" profile, resulting in fillets around the membrane edges. These fillets will serve to shorten the effective width of the membrane and make them stronger; however this will also reduce the ability of the membrane to thermally isolate the central structure from the surroundings. Third, there is an oxide layer up to 0.5 µm thick on the nitride, which is used as an etch-stop during the fabrication process (Section 4.4). Different parts of the wafer etch differently during the through etch; therefore, some or all of this oxide might be etched through. If most of this oxide layer is still intact, it will serve to strengthen the nitride membrane, although the residual stress mismatch between the two layers may also impact the membrane’s mechanical performance.

To characterize any overetch, optical microscope images were taken for a few test dies using an inverted microscope. Figure 5-34 shows one such image of a die, with membrane dimensions similar to those of test dies V1, V2 and V3. The translucent circular band on the edge where the gold heater structure is partially visible indicates a region of overetch. For a perfectly anisotropic etch, all of the gold heater structure would have been covered with wafer-thick silicon and a translucent ring would not have been seen. Figure 5-35 is a zoomed-in image of the same die. The overetch is estimated to be approximately 150µm from these images. This means that the effective membrane inner radius is reduced by 150 µm and the effective membrane outer radius is increased by 150 µm, compared the dimensions it was designed to have.

Another die, imaged similarly (but not shown here), was measured to have an overetch of approximately 100 µm.
Chapter 5: Testing

**Figure 5-34:** Optical microscope image of a final test die, with dimensions similar to test dies V1, V2 and V3, and taken from the same test wafer. Note that the designed heater line width is 20 μm. This image was taken with a Nikon TE2000_U Eclipse microscope.

**Figure 5-35:** Close-up image of the same die as in Figure 5-27. Image taken with a Nikon TE2000_U Eclipse microscope.
Figure 5-36: Photograph of an “F” type final test die. A slight overetch is visible at the edges of the gold heater boundary.
Figure 5-37: Photograph of an "F" type final test die. A slight overetch is visible at the edges of the gold heater boundary.

Figure 5-38: Photograph of an "F" type final test die. A slight overetch is visible at the edges of the gold heater boundary.
Characterizing the fillet shape and the thickness of the remaining oxide is more difficult, and approaches to making this characterization in the future are described in Section 6.2. However, Figures 5-34 to 5-38 indicate that the overetch is roughly 100 μm.

An upper bound is calculated on the membrane strength by assuming a 150 μm overetch, and no fillets. Note that the membrane is actually only 2.1 μm thick, with a maximum oxide layer thickness of 0.5 μm. Even though oxide is not as strong as silicon nitride, the entire thickness (2.6 μm) is assumed to be nitride. A lower bound is also calculated on the membrane strength by assuming a 150 μm overetch and no fillet. Table 5-15 indicates that the tests are closer to the upper bound of the membrane strength; however, the number of tests performed is too small to draw statistically significant conclusions. It may nevertheless be concluded that valved membranes that are robust enough to withstand operation under a 1 atm pressure difference can be and have been designed, implemented, and demonstrated.
Chapter 6

Conclusions and Future Work

6.1 Summary of Contributions and Conclusions

This work has demonstrated the design and fabrication of a new type of leak-free MEMS seal, with an open flow rate ranging from 60 to 400 sccm, and a leak rate less than $10^{-4}$ sccm. To our knowledge, this open-to-closed flow rate ratio of approximately $10^5$ to $10^6$ is the highest reported ratio amongst any moderately high open flow rate (>50 sccm) MEMS valve/seal, with the possible exception of the single-use openable valve by Stenmark et. al [34]. The tradeoff for this high pressure ratio and extremely low leak rate is that the current version of the device described in this work is designed for a single-use sealing application.

An important factor that went into designing the concept of this device was the high reported leak rates ($\sim 10^3$ sccm) of current MEMS valves. For proper functioning of the ion pumps in the Chip-Scale Vacuum Micro Pump, a leak rate of no more than $10^{-9}$ sccm can be tolerated for the valve. To circumvent the problem of leakage through two mating surfaces in contact (a commonly used method of closing MEMS valves), it was decided to use a molten seal
on an initially-open flow port. A thermal actuation scheme was chosen as the natural choice for actuation, based on the need to melt the seal to actuate the valve shut.

The design concept, therefore, called for a solder material that could easily be melted by an on-chip thermal actuation mechanism so that surface tension would cause it to flow over an initially-open flow port, providing a leak-free seal. Indium was chosen as this solder material due to its low melting temperature of 157°C (and, therefore, low actuation power input requirement) and high boiling temperature of 2072°C (and consequently low vapor pressure, which is important to maintain the vacuum integrity of the chamber being sealed). For the valve concept to work, it was necessary to find two substrate materials: one that would interact lyophilically with indium and another that would interact lyophobically with indium. This would allow manipulation of the solder structure to ensure that it “balls up” upon melting to seal the initially-open flow port. Based on a literature review, MEMS-compatibility and preliminary proof-of-concept wetting tests, the lyophilic and lyophobic substrates were chosen to be nickel and silicon respectively. The preliminary wetting tests also informed the need for an organic acid flux during the initial solder assembly process to remove any native oxide layer on the indium and/or nickel that would otherwise prevent proper solder/substrate interactions. The application of additional flux during the solder reflow process was found to be unnecessary.

In order to ensure that the power required to thermally actuate the device is minimal, it was decided to thermally isolate the central solder structure by supporting it in the center of a thin membrane. Silicon nitride was chosen as the membrane material based on its high fracture strength, relatively low thermal conductivity compared to silicon, and compatibility with MEMS tools and processes. The thermal actuation mechanism itself was chosen to be a gold resistive heater, given its high failure current density and MEMS-compatibility.

Geometrical, thermal, structural and electrical models were used to predict the optimal range of dimensions for the various parts of the device. A decision was made early in the design process to have a meso-scaled solder structure, based on predictions of the geometrical wetting model and the time and equipment constraints of fabricating a microscale solder structure.
First, two short loop tests were conducted as part of the risk mitigation and optimization strategy. The first was the sealing short loop, which was designed to verify the geometrical wetting model and the seal integrity of a thermally actuated indium seal. Although the leak rate of the sealed test die could not be quantified with a resolution beyond the parasitic test setup leakage ($10^{-4}$ standard cm$^3$ per minute), the results from these tests indicated that the test die leakage (if any) could not be detected above the background parasitic test jig leakage.

The membrane short loop test was the second short loop test conducted. Its purpose was to verify the integrity of the thermally-insulating silicon nitride membrane structure. Even though some of the test dies were designed to operate with a factor of safety of two, the results of the short loop tests indicated that the membranes were as strong as predicted by theory. Many test dies were able to survive a one atmosphere pressure differential for an extended period of time (hours to days) without rupturing. It should be noted that while the results of these tests were promising enough to move forward with the final device fabrication, more membrane tests would be needed to make statistically relevant claims on the accuracy of the membrane structural model.

Finally, the entire device structure was fabricated, assembled and tested. It should be noted that the gold heater structure on this device was not tested in an earlier short loop test due to time constraints, but the pervasiveness of gold resistive MEMS heaters contributed to a high level of confidence in predicted performance of the heater. Tests on the final device indicated that the heater structure does indeed perform as predicted, with an approximate power input of 0.3 W at solder reflow (well within the design specification of 1 W). The membranes in the final device were also shown to be able to withstand a one atmosphere pressure differential while the sealing structure data were, once again, consistent with those from a leak-free seal. The resolution on the test die leak rate measurement is limited by the level of the parasitic test jig leakage. The next section addresses ways in which this resolution can be increased.
6.2 Future Work

A very important limitation of this device design is that it is single-use only. Finding a way to modify this design so that it can be used as a multiple-use valve has the potential to revolutionize the field of MEMS valves (which are currently limited by their high leak rates and low open-to-closed rate ratios) and offer exciting opportunities for the design of new MEMS systems. This and other areas of future work are described in detail below, presented roughly in increasing order of estimated time and resources required.

6.2.1 Increasing resolution of the test data through a better measurement system, and a rigorous statistical analysis

The test jig leakage restricts the resolution with which the leak rate of the test die can be measured. Reducing test jig leakage can help reduce the proportion of the total measured leakage that is due to the test jig, thereby increasing the resolution for the upper bound of the test die leakage. The most likely cause of test jig leakage is the use of o-rings at the test die/test jig interface, as all other vacuum connections in the test jig used were rated for a much lower leakage \((10^{-9} \text{ sccm})\) than what was measured \((10^{-4} \text{ sccm})\). It is worth investigating other methods of attaching the test die to the test setup, such as solder.

One way to increase the resolution of the test data without having to modify the test setup would be to run a much larger number of tests, so that statistically significant conclusions can be drawn about the average values of the various leak rates as well as their standard deviations.
6.2.2 **Heat jacket to remove adsorbed contaminants**

As is mentioned in Chapter 5, the sealing short loop tests and the full device tests indicated an increase in transient effects and an increase in the apparent steady-state leak rate over time for both test dies and blank dies (see Figures 5-16, 5-18 and 5-19). One hypothesis for this phenomenon is that the test chamber adsorbs water vapor and gases over time and outgases them during the vacuum tests; this hypothesis is supported by the tests of Chapter 5. This is a common problem with macroscale UHV systems, a general solution to which involves heating the entire test chamber for a few hours (using an electrical heating jacket) while running vacuum. This helps desorb many of the adsorbed substances that can accumulate on the chamber walls over time, and is a maintenance operation usually performed every few months as well as before important tests. Doing this for the test jig being used in this work and running tests before and after the procedure, will help provide further proof or disproof of the hypothesis above.

6.2.3 **Effect of flux residue on vacuum**

There is no detectable difference between the pressure curves for the test dies and those for the corresponding blank dies in both the sealing short loop tests and the final device tests. This indicates that any additional rise in pressure (if any) due to flux residue on the test dies is not detectable above the parasitic test jig leakage. An important difference between these tests and the actual environment in which the device is designed to work is that the thermal actuation in the actual pump system will occur in-situ, while the die is still exposed to vacuum, as compared to the tests in this work, in which the actuation is done in the solder reflow apparatus in atmosphere and at room temperature. It is possible that the flux residue does not outgas at room temperature after reflow is complete, but may do so on a transient basis during the reflow process or later on at the potentially elevated temperatures of a complete, operating micropump system. One way to test for transient outgassing during solder reflow would be to reflow the solder while the valve is in its vacuum environment and to observe any resulting pressure rise. This would require the design of a test setup in which the test die does not have to be removed.
Chapter 6: Conclusions and Future Work

from the setup during thermal actuation. This would allow measurement of the pressure on the vacuum side when the valve is open, when the valve is being closed, and when the valve is closed. The experiments discussed in this thesis only measure the pressure when the valve is open and when the valve is closed. However, a setup that has the capability to perform the thermal actuation in-situ would allow the measurement of pressure while the valve goes from open to closed, all in one continuous measurement.

A straightforward way to characterize the effects of solder reflow and elevated temperature without substantially revising the test apparatus would be to perform the leak rate tests on a sealed die as the chamber is simultaneously heated with an electrical thermal jacket to a temperature near the melting point of indium. Comparing data on tests run this way for sealed valve dies and for blank dies will help detect any pressure spikes caused by residual flux outgassing from the test dies.

6.2.4 Integration and packaging

An important area not addressed effectively in this work is the integration between this valve and the rest of the Chip-Scale Vacuum Micro Pump. Even if the valve is shown to be leak-free, it cannot be attached to the CSVMP using o-rings, as they will have an unacceptably high leak rate, as evidenced by the $10^{-4}$ sccm leak rates measured in this work. This will defeat the purpose of the valve itself being leak-free.

A leak-free integration method commonly used for MEMS devices is wafer bonding. However, this process is carried out at extremely high temperature, much higher than the melting point of the indium solder used in this device. This would cause the solder structure to reflow during integration and seal the flow port even before the device can begin operating.

A good solution to this problem is critical for the successful use of this valve with the CSVMP, as well as other MEMS devices. One possible solution that can be explored further is using a higher melting temperature solder instead of indium and packaging the chip with low-temperature bonding. Another possible solution is using solder-based assembly to bond the chip
to the package with a solder than melts at a lower temperature than the solder that will be used for the sealing structure. Future versions of this device should take these and other possibilities into consideration.

6.2.5 Resealable valve

As was mentioned previously, while the seal described in this work is essentially leak-free, its major drawback is that it is a single-use device. Once sealed, it is not designed to be reopened. An important area for future work would be to modify the seal design so that it can be a multiple-use valve. This would open up a host of possibilities for integrating this device with other new and exciting MEMS devices.

In conclusion, this work has demonstrated the design, fabrication and testing of a new, leak-free, permanently sealable MEMS valve with an open state flow rate of 60 to 400 standard cm\(^3\) per minute (sccm), a closed state leak rate not detectable above that of the test jig used (10\(^{-4}\) sccm), and an open-to-closed flow rate ratio of greater than 10\(^5\) to 10\(^6\). While this version of the device is still a single-use seal, it is an important step in the design of new leak-free MEMS valves with very high open-to-closed flow rate ratios.
References


34. Lars Stenmark, P.R., High Pressure Isolation Valve System, 2008, Nanospace AB.


Appendix A – Process Flow for the Sealing Short Loop

<table>
<thead>
<tr>
<th>Feature</th>
<th>Step#</th>
<th>Lab</th>
<th>Process step</th>
<th>Machine</th>
<th>Chemicals</th>
<th>Color</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alignment marks</td>
<td>1</td>
<td>TRL</td>
<td>RCA Clean</td>
<td>TRL-RCA</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>2</td>
<td>TRL</td>
<td>HMDS</td>
<td>HMDS-TRL</td>
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<td>thin resist recipe</td>
<td></td>
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<tr>
<td></td>
<td>3</td>
<td>TRL</td>
<td>Spin on resist (front)</td>
<td>coater</td>
<td>OCG 825-20CS</td>
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<td>1 um, positive resist</td>
</tr>
<tr>
<td></td>
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<td>TRL</td>
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<td>EV1</td>
<td>green</td>
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<tr>
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<td>TRL</td>
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<td>postbake</td>
<td>green</td>
<td>90C, 30 min</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>ICL</td>
<td>front Si etch</td>
<td>AME5000</td>
<td>green</td>
<td>Chamber B, 0.5 um</td>
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</tr>
<tr>
<td></td>
<td>8</td>
<td>ICL</td>
<td>piranha + rinse + spin dry</td>
<td>ICL-premetal</td>
<td>sulfuric acid, peroxide</td>
<td>green</td>
<td>piranha clean</td>
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</table>

<table>
<thead>
<tr>
<th>Feature</th>
<th>Step#</th>
<th>Lab</th>
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<th>Machine</th>
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<tbody>
<tr>
<td>Ni pattern using liftoff</td>
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<td>HMDS</td>
<td>HMDS-TRL</td>
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<tr>
<td></td>
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<td>TRL</td>
<td>Spin on resist (front)</td>
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<td>AZ 5214</td>
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<td>5214 Image Reversal resist for liftoff</td>
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<td>prebake</td>
<td>green</td>
<td>90C, 30 min</td>
<td></td>
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<tr>
<td></td>
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<td>TRL</td>
<td>expose front</td>
<td>EV1</td>
<td>green</td>
<td>Mask 1 (Ni Patter Mask), about 5 secs</td>
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<td>TRL</td>
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<td>postbake</td>
<td>green</td>
<td>90C, 30 min</td>
<td></td>
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<td></td>
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<td>TRL</td>
<td>Flood exposure</td>
<td>EV1</td>
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<td>about 50 secs</td>
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<tr>
<td></td>
<td>9</td>
<td>ICL</td>
<td>Deposit 100nm Ti + 800 nm Nickel</td>
<td>eBeamAu</td>
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<td>Dep rate 2 A/sec for both</td>
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<tr>
<td></td>
<td>10</td>
<td>ICL</td>
<td>Liftoff</td>
<td></td>
<td>blue</td>
<td>Acetone bath in sonicator for 20 minutes</td>
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<th>Machine</th>
<th>Chemicals</th>
<th>Color</th>
<th>Comments</th>
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<td>TRL</td>
<td>Spin on resist (front of main wafer)</td>
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<td>AZ 4620</td>
<td>blue</td>
<td>10 um, positive resist</td>
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<td>Equipment</td>
<td>Result</td>
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<td>--------</td>
<td>-----------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>TRL</td>
<td>prebake prebake</td>
<td>blue</td>
<td>90C, 30 min</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>4</td>
<td>TRL</td>
<td>Spin on resist coater AZ 4620</td>
<td>blue</td>
<td>10 um, positive resist</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>TRL</td>
<td>prebake prebake blue</td>
<td>90C, 60 min</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>6</td>
<td>TRL</td>
<td>expose front EV1 blue</td>
<td>Mask 2 (300 micron diam holes) 15 secs on, 15 secs off, repeat 8 times</td>
<td></td>
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</tr>
<tr>
<td>7</td>
<td>TRL</td>
<td>develop photo-wet AZ 440 blue</td>
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</tr>
<tr>
<td>8</td>
<td>TRL</td>
<td>Spin on resist on dummy handle coater AZ 4620</td>
<td>blue</td>
<td>10 um, positive resist</td>
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<tr>
<td>9</td>
<td>TRL</td>
<td>Place main wafer on dummy blue</td>
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<tr>
<td>10</td>
<td>TRL</td>
<td>postbake postbake blue</td>
<td>90C for 60 mins</td>
<td></td>
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<tr>
<td>12</td>
<td>ICL</td>
<td>Si etch STS3 blue</td>
<td>Etch a through hole in Si 'mit59' recipe for approximately 6 hours</td>
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<tr>
<td>13</td>
<td>TRL</td>
<td>Strip PR BAR asher-TRL blue</td>
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<tr>
<td>14</td>
<td>TRL</td>
<td>Remove Handle wafer acetone blue</td>
<td>Soak in acetone for 24 hours</td>
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<tr>
<td>15</td>
<td>TRL</td>
<td>Clean wafer photo-wet Nanostrip blue</td>
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</table>
Alignment Mask
Alignment Mask – zoomed-in
Mask 1
Mask 1 – zoomed-in
Mask 2
Mask 2
## Appendix B – Process Flow for Membrane Short Loop

<table>
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<th>Feature</th>
<th>Step#</th>
<th>Lab</th>
<th>Process step</th>
<th>Machine</th>
<th>Chemicals</th>
<th>Color</th>
<th>Comments</th>
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<td>RCA Clean</td>
<td>1</td>
<td>ICL</td>
<td>RCA</td>
<td>ICL-rca</td>
<td></td>
<td></td>
<td>Clean</td>
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<tr>
<td>Grow Thermal Oxide</td>
<td>2</td>
<td>ICL</td>
<td>Grow Thermal Oxide</td>
<td>ICL-Tube 5D</td>
<td>green</td>
<td></td>
<td>5000A of oxide, 2 um of low-stress nitride, Bob / Kris Payer in charge of recipe parameters</td>
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<tr>
<td>Deposit Nitride</td>
<td>3</td>
<td>ICL</td>
<td>Deposit Nitride</td>
<td>VTR</td>
<td>green</td>
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<tr>
<td>Remove the nitride layer from the front side</td>
<td>4</td>
<td>ICL</td>
<td>Spin on resist on the back side</td>
<td>HMDS-TRL</td>
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<td>10um thick resist</td>
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<td></td>
<td>6</td>
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<td>prebake</td>
<td>prebake</td>
<td>AZ 4620</td>
<td></td>
<td>90C, 30min</td>
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<td></td>
<td>7</td>
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<td>expose</td>
<td>EV1</td>
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<td>8</td>
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<td>develop</td>
<td>photo-wet</td>
<td>AZ 440</td>
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<td></td>
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<tr>
<td></td>
<td>9</td>
<td></td>
<td>postbake</td>
<td>postbake</td>
<td></td>
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<td></td>
<td>10</td>
<td></td>
<td>Nitride Etch</td>
<td>STS</td>
<td></td>
<td></td>
<td>Nitride recipe, ~ 1 hr 30 mins</td>
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<td>11</td>
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<td>Strip Resist</td>
<td>TRL-asher</td>
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<tr>
<td>Remove the oxide layer from the front side</td>
<td>12</td>
<td>BOE</td>
<td></td>
<td>BOE</td>
<td></td>
<td></td>
<td>7:1 HF solution for 10 mins</td>
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<td>Membrane Release</td>
<td>13</td>
<td>HMDS</td>
<td>Spin on resist (front)</td>
<td>HMDS-TRL</td>
<td>thick resist recipe</td>
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<td></td>
<td>14</td>
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<td>prebake</td>
<td>prebake</td>
<td>AZ 4620</td>
<td></td>
<td>10 um, positive resist</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td></td>
<td>spin on resist</td>
<td>prebake</td>
<td>AZ 4620</td>
<td></td>
<td>90C, 30 min</td>
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<td>16</td>
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<td>expose front</td>
<td>EV1</td>
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<td>Membrane Release Mask</td>
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<td>17</td>
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<td>develop</td>
<td>photo-wet</td>
<td>AZ 440</td>
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<td>18</td>
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<td>Mount handle to handle wafer</td>
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<td></td>
<td>20</td>
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<td>Mount handle</td>
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<tr>
<td></td>
<td>postbake</td>
<td>postbake</td>
<td>90°C for 60 mins</td>
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<td>21</td>
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<td>'mit59' gave black silicon, switched to 'hqli_u' recipe for later wafers</td>
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<tr>
<td>22</td>
<td>Si etch</td>
<td>STS3</td>
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<tr>
<td>23</td>
<td>Strip PR</td>
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<td>Acetone etch to remove PR and handle wafer</td>
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**Membrane Release Mask**
Membrane Release Mask – zoomed-in
## Appendix C – Process Flow for Complete Device

<table>
<thead>
<tr>
<th>Feature</th>
<th>Step#</th>
<th>Lab</th>
<th>Process step</th>
<th>Machine</th>
<th>Chemicals</th>
<th>Color</th>
<th>Comments</th>
</tr>
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<tbody>
<tr>
<td>RCA Clean</td>
<td>1</td>
<td>ICL</td>
<td>RCA</td>
<td>ICL-rca</td>
<td>green</td>
<td>Clean</td>
<td></td>
</tr>
<tr>
<td>Grow Thermal Oxide</td>
<td>2</td>
<td>ICL</td>
<td>Grow Thermal Oxide</td>
<td>ICL-Tube 5D</td>
<td>green</td>
<td>5000A of oxide</td>
<td></td>
</tr>
<tr>
<td>Deposit Nitride</td>
<td>3</td>
<td>ICL</td>
<td>Deposit Nitride</td>
<td>VTR</td>
<td>green</td>
<td></td>
<td>2.4 um of low-stress nitride</td>
</tr>
<tr>
<td>Etch Nitride from top</td>
<td>4</td>
<td>TRL</td>
<td>STS etch</td>
<td>STS2/3 or LAM</td>
<td>green</td>
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<td></td>
</tr>
<tr>
<td>Etch Oxide from Top</td>
<td>5</td>
<td>TRL</td>
<td>BOE</td>
<td>BOE</td>
<td>green</td>
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<td>Alignment Marks</td>
<td>6a</td>
<td>TRL</td>
<td>HMDS</td>
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<td>green</td>
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<td></td>
<td>6b</td>
<td>TRL</td>
<td>spin on thin resist</td>
<td></td>
<td>green</td>
<td>1 um positive resist</td>
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<tr>
<td></td>
<td>6c</td>
<td>TRL</td>
<td>prebake</td>
<td>prebake</td>
<td>green</td>
<td>90C, 30 min</td>
<td>Mask 1</td>
</tr>
<tr>
<td></td>
<td>6d</td>
<td>TRL</td>
<td>expose</td>
<td>EV-1</td>
<td>green</td>
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<td></td>
<td>6e</td>
<td>TRL</td>
<td>develop</td>
<td>photo-wet</td>
<td>OCG-934</td>
<td>green</td>
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<tr>
<td></td>
<td>6f</td>
<td>TRL</td>
<td>postbake</td>
<td>postbake</td>
<td>green</td>
<td>120C, 30min</td>
<td></td>
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<tr>
<td></td>
<td>6g</td>
<td>ICL</td>
<td>Etch</td>
<td>AME5000</td>
<td>green</td>
<td>Chamber B, 0.5um</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6h</td>
<td>ICL</td>
<td>Piranha+rinse+spin-dry</td>
<td>ICL-premetal</td>
<td>sulfuric acid, peroxide</td>
<td>green</td>
<td></td>
</tr>
<tr>
<td>Deposit Au or nichrome on the bottom with liftoff</td>
<td>7a</td>
<td>TRL</td>
<td>HMDS</td>
<td>HMDS-TRL</td>
<td>green</td>
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</tr>
<tr>
<td></td>
<td>7b</td>
<td>TRL</td>
<td>Spin on negative resist (bottom)</td>
<td>coat</td>
<td>green</td>
<td>5214 Image reversal resist for liftoff</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7c</td>
<td>TRL</td>
<td>prebake</td>
<td>prebake oven</td>
<td>green</td>
<td>90C, 30min</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7d</td>
<td>TRL</td>
<td>expose bottom</td>
<td>EV-1</td>
<td>green</td>
<td>Mask 2, about 5</td>
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157
<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Time/Temp/Condition</th>
</tr>
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<tbody>
<tr>
<td>7e</td>
<td>TRL postbake hotplate</td>
<td>green 120°C for 1 min</td>
</tr>
<tr>
<td>7f</td>
<td>TRL flood exposure EV-1</td>
<td>green about 50 seconds</td>
</tr>
<tr>
<td>7g</td>
<td>TRL develop photo-wet</td>
<td>green 50 nm Cr + 1 um gold or 50 nm Cr + 1 um nichrome</td>
</tr>
<tr>
<td>7h</td>
<td>TRL Deposit gold or nichrome eBeamAu</td>
<td>red Acetone bath</td>
</tr>
<tr>
<td>7i</td>
<td>TRL Liftoff photo-wet</td>
<td>red</td>
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### Etch holes in the nitride/oxide on the bottom side

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<th>Time/Temp/Condition</th>
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<tr>
<td>8a</td>
<td>HMDS</td>
<td>red 10 um thick resist</td>
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<tr>
<td>8b</td>
<td>Spin on thick resist on the bottom</td>
<td>red 90°C, 30 min</td>
</tr>
<tr>
<td>8c</td>
<td>prebake prebake</td>
<td>red Mask 3</td>
</tr>
<tr>
<td>8d</td>
<td>expose EV-1</td>
<td>red</td>
</tr>
<tr>
<td>8e</td>
<td>develop photowet</td>
<td>red 120°C, 30 min</td>
</tr>
<tr>
<td>8f</td>
<td>postbake postbake</td>
<td>red</td>
</tr>
<tr>
<td>8g</td>
<td>Etch nitride STS1 or TRL-LAM</td>
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<td>8h</td>
<td>Etch oxide acidhood BOE</td>
<td>red</td>
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<td>8i</td>
<td>Strip resist asher</td>
<td>red Ash resist</td>
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### Deposit nickel on the top using liftoff

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<th>Process</th>
<th>Time/Temp/Condition</th>
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<tr>
<td>9a</td>
<td>TRL HMDS HMDSTRL</td>
<td>red 5214 Image reversal resist for liftoff</td>
</tr>
<tr>
<td>9b</td>
<td>TRL Spin on negative resist coater</td>
<td>red</td>
</tr>
<tr>
<td>9c</td>
<td>TRL prebake prebake oven</td>
<td>red Mask 4 90°C, 30 min</td>
</tr>
<tr>
<td>9d</td>
<td>TRL expose EV-1</td>
<td>red Mask 4</td>
</tr>
<tr>
<td>9e</td>
<td>TRL post exposure bake postbake oven</td>
<td>red 120°C hotplate for 1 min</td>
</tr>
<tr>
<td>Step</td>
<td>Process</td>
<td>Material</td>
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<tr>
<td>9f</td>
<td>TRL flood exposure</td>
<td>EV-1 red</td>
</tr>
<tr>
<td>9g</td>
<td>TRL develop</td>
<td>photo-wet red</td>
</tr>
<tr>
<td>9h</td>
<td>TRL Deposit Ti/Ni</td>
<td>eBeamAu red</td>
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<td>9i</td>
<td>TRL LiftOff</td>
<td>photo-wet red</td>
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<td>10a</td>
<td>Spin on resist</td>
<td>coater AZ 4620 red</td>
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<td>10b</td>
<td>prebake</td>
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<tr>
<td>10c</td>
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<td>10e</td>
<td>expose front</td>
<td>EV1 red</td>
</tr>
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<td>10f</td>
<td>develop</td>
<td>photo-wet AZ 440 red</td>
</tr>
<tr>
<td>10g</td>
<td>Mount handle</td>
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<td>10h</td>
<td>postbake</td>
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<td>10j</td>
<td>Si etch</td>
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<tr>
<td>Time</td>
<td>Process</td>
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</tr>
<tr>
<td>10k</td>
<td>BOE</td>
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<tr>
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Mask 1 – zoomed-in
Mask 1 – zoomed-in
Mask 2
Mask 2 – zoomed-in
**Mask 3**

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Mask 4
Mask 4 – zoomed-in
Mask 5
Mask 5 – zoomed-in