DSENT — A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling
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Abstract—With the advent of many-core chips that place substantial demand on the NoC, photonics has been investigated as a promising alternative to electrical NoCs. While numerous opto-electronic NoCs have been proposed, their evaluations tend to be based on fixed numbers for both photonic and electrical components, making it difficult to co-optimize. Through our own forays into opto-electronic NoC design, we observe that photonics and electronics are very much intertwined, reflecting a strong need for a NoC modeling tool that accurately models parameterized electronic and photonic components within a unified framework, capturing their interactions faithfully. In this paper, we present a tool, DSENT, for design space exploration of electrical and opto-electrical networks. We form a framework that constructs basic NoC building blocks from electrical and photonic technology parameters. To demonstrate potential use cases, we perform a network case study illustrating data-rate tradeoffs, a comparison with scaled electrical technology, and sensitivity to photonics parameters.

I. INTRODUCTION

As CMOS technology scales into the deep sub-100 nm regime, improvements in transistor density have resulted in greater processor parallelism as the means to improve processor performance, leading to rapidly increasing processor core counts. The rise of the many-core era, however, comes with the challenge of designing the on-die interconnect fabric to allow for efficient delivery of bits between an ever increasing number of processor cores, memories, and specialized IP blocks both on- and off-chip. Traditional approaches, such as the shared bus or global crossbars, scale poorly in either performance or cost for large numbers of network endpoints, driving the need for efficient Network-on-Chip (NoC) architectures to tackle the communication requirements of future many-core machines.

Recognizing the potential scaling limits of electrical interconnects, architects have recently proposed emerging nanophotonic technology as an option for both on-chip and off-chip interconnection networks. As optical links avoid the capacitive, resistive and signal integrity constraints imposed upon electronics, photonics allows for efficient realization of physical connectivity that is costly to accomplish electrically. Many photonic architectures have been proposed recently [1, 2, 3, 4] for both on-chip and chip-to-chip applications.

Photonics technology itself, however, remains immature and there remains a great deal of uncertainty in its capabilities. Whereas there has been significant prior work on electronic NoC modeling (see Section II-C), evaluations of photonic NoC architectures have not yet evolved past the use of fixed energy costs and losses for both photonic and electronic components [1, 3, 4, 5], which also vary significantly from study to study. Yet, there are inherent interactions and tradeoffs between the electronic/photonic components that need to be captured in order to accurately bring forth the capabilities of this emerging technology.

In this paper, we propose a unified framework for photonics and electronics, DSENT (Design Space Exploration of Networks Tool), that enables rapid cross-hierarchical area and power evaluation of opto-electronic on-chip interconnects. We design DSENT for two primary usage modes. When used standalone, DSENT functions as a fast design space exploration tool capable of rapid power/area evaluation of hundreds of different network configurations, allowing for impractical or inefficient networks to be quickly identified and pruned before detailed cycle-accurate evaluation. When integrated with an architectural simulator [6, 7], DSENT can be used to generate traffic-dependent power-traces and area estimations for the network.

This paper makes the following contributions:

• DSENT provides accurate (within 5–15%) parameterized models for both photonics and electronics, validated against SPICE and published literature.
• This is the first tool that permits exploration of the interactions of photonics and electronics in an opto-electronic NoC.
• This is the first architecture-level integrated timing, area, and power model of electrical NoC components.
• Using DSENT, we were able to project the necessary technology trends for future scaling of photonic and electronic components.

The rest of the paper is organized as follows. Section II introduces the main building blocks of photonic NoCs and recaps existing work in photonic architectures and NoC modeling. We describe the DSENT framework in Section III and present its models for electrical and optical components in Sections IV and V respectively. Validation of DSENT is shown in Section VI, followed by a case study demonstrating its potential use scenarios in Section VII. Section VIII concludes the paper.

1We focus on the application of DSENT to opto-electronic NoCs in this paper, though naturally, its electrical transistor and circuit models can also be applied to pure electrical NoCs and other electrical circuits systems.
II. BACKGROUND

A. Silicon Photonics Technology

a) Waveguides, Couplers, and Lasers: Waveguides are the primary means of routing light within the confines of a chip. Vertical grating couplers [8] allow light to be directed both into and out-of the plane of the chip and provide the means to bring light from a fiber onto the chip or couple light from the chip into a fiber. In this paper, we assume commercially available off-chip continuous wave lasers, though we note that integrated on-chip laser sources are also possible [9, 10].

b) Ring Resonators: The optical ring resonator is the primary component that enables on-chip wavelength division multiplexing (WDM). When coupled to a waveguide, rings perform as notch filters; wavelengths at resonance are trapped in the ring and can be potentially dropped onto another waveguide while wavelengths not at resonance pass by unaffected. The resonant wavelength of each ring can be controlled by adjusting the device geometry or the index of refraction. As resonators are highly sensitive to process mismatches and temperature, ring resonators require active thermal tuning [11].

c) Ring Modulators and Detectors: Ring modulators modulate its resonant wavelength by electrically influencing the index of refraction [12]. By moving a ring’s resonance in and out of the laser wavelength, the light is modulated (on-off keying). A photodetector, made of pure germanium or SiGe, converts optical power into electrical current, which can then be sensed by a receiver [13] and resolved to electrical ones and zeros. Photodetectors used standalone are generally wideband and require ring filters for wavelength selection in WDM operation.

d) Photonic Links: The dynamics of a wavelength-division-multiplexed (WDM) photonic architecture are shown in Figure 1. Wavelengths are provided by an external laser source and coupled into an on-chip waveguide. Each wavelength is modulated by a resonant ring modulator dropped at the receiver by a matching ring filter. Using WDM, a single waveguide can support dozens of independent data-streams on different wavelengths.

B. Prior Photonic NoC Architectures

Many photonics-augmented architectures have been proposed to address the interconnect scalability issue posed by rapidly rising core-counts. The Corona [4] architecture uses a global 64x64 optical crossbar with shared optical buses employing multiple matching ring modulators on the same waveguide. Firefly [3] and ATAC [2] also feature global crossbars, but with multiple matching receive rings on the same waveguide in a multi-drop bus configurations. The photonic clos network [5] replaces long electrical links characteristic of clos topologies with optical point-to-point links (one set of matching modulator and receiver ring per waveguide) and performs all switching electrically. Phastlane [14] and Columbia [15] networks use optical switches in tile-able mesh-like topologies. While each of these prior works performs evaluations of their respective networks, we note that the analyses in these prior works all rely on fixed numbers for active photonic devices and electronic components, making it difficult to explore design tradeoffs and interactions between photonics and electronics.

C. Existing NoC Modeling Tools

Several modeling tools have been proposed to estimate the timing, power and area of NoCs. Chien proposed a timing and area model for router components [16] that is curve-fitted to a specific process without providing any information how the model can scale with the technology. Peh and Dally proposed a timing model router components [17] based on logical effort that is technology independent; however, only one size of each logic gate and no wire model is considered in its analysis. These tools also estimate only timing and area but not power.

Among all the tools that provide power models for NoCs [18, 19, 20, 21], Orion [18, 21], which provides parametrized power and area models for routers and links, is the most widely used in the community. However, Orion lacks a delay model for router components, allowing router clock frequency to be set arbitrarily without impacting energy/cycle or area. Furthermore, Orion uses a fixed set of technology parameters and standard cell sizing, scaling the technology through a gate length scaling factor that does not reflect the effects of other technology parameters. For link components, Orion supports only limited delay-optimal repeated links. Orion does not model any optical components.

PhoenixSim [22] is the result of recent work in photonics modeling, improving the architectural visibility concerning the trade-offs of photonic networks. PhoenixSim provides parameterized models for photonic devices. However, PhoenixSim lacks electrical models, relying instead on Orion for all electrical routers and links. As a result, PhoenixSim uses fixed numbers for energy estimations for electrical interface circuitry, such as modulator drivers, receivers, and thermal tuning, losing many of the interesting dynamics when transistor technology, data-rate, and tuning scenarios vary. PhoenixSim in particular does not capture trade-offs among photonic device and driver/receiver specifications that result in an area or power optimal configuration.

To address shortcomings of these existing tools, we propose DSENT to provide a unified electrical and optical framework that can be used to model system-scale aggressive electrical and opto-electronic NoCs in future technology nodes.

III. DSENT FRAMEWORK

In our development of the generalized DSENT modeling framework, we observe the constant trade-offs between the amount of required user input and overall modeling accuracy.
**Fig. 2:** The DSENT framework with examples of network-related user-defined models.

All-encompassing technology parameter sets can enable precise models, at the cost of becoming too cumbersome for predictive technologies where only basic technology parameters are available. Overly simplistic input requirements, on the other hand, leaves significant room for inaccuracies. In light of this, we design a framework that allows for a high degree of modeling flexibility, using circuit- and logic-level techniques to simplify the set of input specifications without sacrificing modeling accuracy. In this section, we introduce the generalized DSENT framework and the key features of our approach.

### A. Framework Overview

DSENT is written in C++ and utilizes the object-oriented approach and inheritance for hierarchical modeling. The DSENT framework, shown in Figure 2, can be separated into three distinct parts: user-defined models, support models, and tools. To ease development of user-defined models, much of the inherent modeling complexity is off-loaded onto support models and tools. As such, most user-defined models involve just simple instantiation of support models, relying on tools to perform analysis and optimization. Like an actual electrical chip design, DSENT models can leverage instancing and multiplicity to reduce the amount of repetitive work and speed up model evaluation, though we leave open the option to allow, for example, all one thousand tiles of a thousand core system to be evaluated and optimized individually. Overall, we strive to keep the run-time of a DSENT evaluation to a few seconds, though this will vary based upon model size and complexity.

### B. Power, Energy, and Area Interface

The typical power breakdown of an opto-electronic NoC can be formulated as Equation 1. The optical power is the wall-plug laser power (lost through non-ideal laser efficiency and optical device losses). The electrical power consists of the power consumed by electrical routers and links as well as electric-optical interface circuits (drivers and receivers) and ring tuning.

\[
P_{\text{total}} = P_{\text{electrical}} + P_{\text{optical}}
\]

\[
P_{\text{electrical}} = P_{\text{router}} + P_{\text{link}} + P_{\text{interface}} + P_{\text{tuning}}
\]

\[
P_{\text{optical}} = P_{\text{laser}}
\]

We classify each power component into one of two groups: non-data-dependent power, and data-dependent energy. Non-data-dependent power is power that is consumed by the model regardless of whether the circuit is being used or sitting idle, such as leakage and un-gated clock power. Data-dependent energy is defined per event or transaction that the model makes, and refers to the energy consumed in order to make the transaction. Crossbar traversal, buffer read and buffer write are examples of events for a router, each with their own associated data-dependent energy cost. The power consumption of a component is defined as \( P_{\text{total}} = P_{\text{NDD}} + \sum E_i f_i \), where \( P_{\text{NDD}} \) is the total non-data-dependent power of the model and \( E_i, f_i \) are the energy cost of an event and the frequency of such events, respectively. Though both area and the non-data-dependent components of power may be estimated statically, data-dependent power calculation requires knowledge of the overall system behavior and activities. An architectural simulator can be used to supply the event counts at the network or router-level, such as router or link traversals. Events at the gate- and transistor-level, however, are too low-level to be kept track of by these means, motivating our expected transition probability approach, to be discussed in Section IV-C.

Area estimates are similarly broken down into their respective electrical (logic, wires, etc.) and optical (rings, waveguides, couplers, etc.) and components. The total area is the sum of these components, with a further distinction made between active silicon area, per-layer wiring area, and photonic device area (if a separate photonic plane is used).

### IV. DSENT Models and Tools for Electronics

As the usage of standard cells is practically universal in modern digital design flows, detailed timing, leakage, and energy/op characterization at the standard-cell level can enable a high degree of modeling accuracy. Thus, given a set of technology parameters, DSENT constructs a standard cell library and uses this library to build models for the electrical network components, such as routers and repeated links.

#### A. Standard Cells

The standard-cell models (Figure 3) are portable across technologies, and the library is constructed at run-time based on design heuristics extrapolated from open-source libraries [24] and calibrated with commercial standard cells.

We strive to rely on only a minimal set of technology parameters, as shown in Table I, that best captures the major characteristics of deep sub-100 nm technologies without diving into transistor modeling. Both interconnect and transistor properties are paramount at these nodes, as interconnect parasitics

### Table I: DSENT electrical parameters.

<table>
<thead>
<tr>
<th>Process Parameters</th>
<th>45nm SOI</th>
<th>11nm TG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Supply Voltage ( (V_{DD}) )</td>
<td>1.0V</td>
<td>0.7V</td>
</tr>
<tr>
<td>Minimum Gate Width</td>
<td>150nm</td>
<td>40nm</td>
</tr>
<tr>
<td>Contacted Gate Pitch</td>
<td>180nm</td>
<td>44nm</td>
</tr>
<tr>
<td>Gate Capacitance / Width</td>
<td>1.0 fF/um</td>
<td>2.42 fF/um</td>
</tr>
<tr>
<td>Drain Capacitance / Width</td>
<td>0.6 fF/um</td>
<td>1.15 fF/um</td>
</tr>
<tr>
<td>Effective On Current / Width</td>
<td>630 aA/um</td>
<td>738 aA/um</td>
</tr>
<tr>
<td>Single-transistor Off Current</td>
<td>600 aA/um</td>
<td>1000 aA/um</td>
</tr>
<tr>
<td>Subthreshold Swing</td>
<td>200 mV/dec</td>
<td>200 mV/dec</td>
</tr>
<tr>
<td>DIBL</td>
<td>150 mV/V</td>
<td>150 mV/V</td>
</tr>
<tr>
<td>Wire Capacitance (Min Pitch)</td>
<td>0.155 fF/um</td>
<td>0.167 fF/um</td>
</tr>
</tbody>
</table>

*Values are shown for NMOS and local-layer wires.*
play an ever larger role due to poor scaling trends [25]. These parameters can all be obtained from ITRS roadmap projection tables for predictive technologies or characterized from SPICE and process design kits when available. We currently model the 45nm SOI and 11nm Tri-Gate technology nodes, with technology parameters extracted using SPICE models for 45nm SOI and projected [26] using the virtual-source transport [27] and parasitic capacitance model [28] for 11nm Tri-Gate.

For the standard cell library, we pick a global standard cell height, $H = H_{ex} + \alpha \cdot (1 + \beta) \cdot W_{min}$, where $\beta$ represents the P-to-N ratio, $W_{min}$ is the minimum transistor width, and $H_{ex}$ is the extra height needed to fit in supply rails and diffusion separation. $\alpha$ is heuristically picked such that large (high driving strength) standard cells do not require an excessive number of transistor folds and small (low driving strength) cells do not waste too much active silicon area. For each standard cell, given a drive strength and function, we size transistors to match pull-up and pull-down strengths, folding standard cell, given a drive strength and function, we size transistors to match pull-up and pull-down strengths, folding

$$f_{i} = \frac{\sum C_i \cdot V_i^2 \cdot f_i}{\sum C_i}$$

where $C_i$ is the total downstream capacitance it sees: $C_i = \sum C_{in} \cdot R_{in} \cdot C_{m}$

Note that any resistances or capacitances due to wiring parasitics is automatically factored along the way. If a register-to-register delay constraint, such as one imposed by the clock period, is not satisfied, timing optimization is required to meet the delay target. To this end, we employ a greedy incremental timing optimization algorithm. We start with the identification of a critical path. Next, we find a node to optimize to improve the delay on the path, namely, a small gate driving a large output load. Finally, we size up that node and repeat these three steps until the delay constraint is met or if we realize that it is not possible and give up. Our method optimizes for minimum energy given a delay requirement, as opposed to logical-effort based approaches employed by existing models [31, 32], without regards for energy. Though lacking the rigorouness of timing optimization algorithms used by commercial hardware synthesis tools, our approach runs fast and performs well given its simplicity.

C. Expected Transitions

The primary source of data-dependent energy consumption in CMOS devices comes through the charging and discharging of transistor gate and wiring capacitances. For every transition of a node with capacitance $C$ to voltage $V$, we dissipate an energy of $E = \frac{1}{2}C \cdot V^2$. To calculate data-dependent power usage, we sum the energy dissipation of all such transitions multiplied by their frequency of occurrence, $P_{DD} = \sum C_i \cdot V_i^2 \cdot f_i$. Node capacitance $C_i$ can be calculated for each model and, for digital logic, $V_i$ is the supply voltage. The frequency of occurrence, $f_i$, however, is much more difficult to estimate accurately as it depends on the pattern of bits flowing through the logic. As event counts and signal information at the logic gate level are generally not available except through structural netlist simulation, DSENT uses a simplified expected transition probability model [33] to estimate the average frequency of switching events. Probabilities derived using this model are also used with state-dependent leakage in the standard cells to form accurate leakage calculations.

D. Summary

DSENT models a technology-portable set of standard cells from which larger electrical components such as routers and networks are constructed. Given a delay or frequency constraint, DSENT applies (1) timing optimization to size gates for energy-optimality and (2) expected transition propagation to accurately gauge the power consumption. These features allow DSENT to outpace Orion in estimating electrical components and in projecting trends for future technology nodes.

V. DSENT MODELS AND TOOLS FOR PHOTONICS

A complete on-chip photonic network consists of not only the photonic devices but also the electrical interface circuits and the tuning components, which dominate the link energy cost. In this section we present how we model these components in DSENT and useful tools that explore the design trade-offs of photonic links and other electrical components.

A. Photonic Device Models

Similar to how it builds the electrical network model using standard cells, DSENT models a library of photonic devices necessary to build integrated photonic links. The library includes models for lasers, couplers, waveguides, ring resonators, modulators and detectors. The total laser power required at the laser source is the sum of the power needed by each photodetector after applying optical path losses:

$$P_{laser} = \sum P_{sense, i} \cdot 10^{\frac{loss_i}{10}}$$

where $P_{sense, i}$ is the laser power required at photodetector $i$ and $loss_i$ is the loss to that photodetector, given in dB.
B. Interface Circuitry

The main interface circuits responsible for electrical-to-optical and optical-to-electrical conversion are the modulator drivers and receivers. The properties of these circuits affect not only their power consumption, but also the performance of the optical devices they control and hence the laser power [11].

1) Modulator Driver: We adopt the device models of [11] for a carrier-depletion modulator. We first find the amount of charge $\Delta Q$ that must be depleted to reach a target extinction ratio, insertion loss, and data-rate. Using equations for a reverse-biased junction, we map this charge to a required reverse-biased drive voltage ($V_{RB}$) and calculate the effective capacitance using charge and drive voltage $C_{eff} = \Delta Q/V_{RB}$. Based on the data-rate, we set a delay constraint and use DSENT’s timing optimization tool to size a chain of buffers to drive $C_{eff}$. The overall energy cost for a modulator driver can be expressed as:

$$E_{driver} = \frac{1}{\gamma} \cdot C_{eff} \cdot V_{DD} \cdot V_{RB} + E_{buffers}(f)$$

where $\gamma$ is the efficiency of generating a supply voltage of $V_{RB}$ and $E_{buffers}(f)$ is the energy consumed by the chain of buffers that are sized based on the data-rate $f$.

2) Receiver: We assume the integrating receiver topology of [11] consisting of a photodetector connected across the input terminals of a sense-amplifier. Electrical power and area footprints of the sense-amplifier can be calculated based on sense-amplifier sizing heuristics and scaled with technology. A simplified expression for the required voltage buildup necessary at the receiver input terminal can be formulated as

$$V_d = v_s + v_{os} + \Phi(BER) \cdot \sqrt{\sum \sigma_n^2}$$

which is the sum of the sense-amp minimum latching input swing ($v_s$), the sense-amp offset mismatch ($v_{os}$), and all Gaussian noise sources multiplied by the number of standard deviations corresponding to the receiver bit error rate. The required input can then be mapped to a required laser power requirement, $P_{sense}$ at the photodetector:

$$P_{sense} = \frac{1}{R_{pd}} \cdot \frac{ER}{ER - 1} \cdot V_d \cdot C_{par} \cdot f_{data}$$

where $R_{pd}$ is the photodetector responsivity (in terms of Amps/Watt), $ER$ is the extinction ratio provided by the modulator, $C_{par}$ is the total parasitic capacitance present at the receiver input node, and $f_{data}$ is the data rate of the receiver.

3) Serializer and Deserializer: DSENT provides models for a standard-cell-based serializer and deserializer (SerDes) blocks, following a mux/de-mux-tree topology [34]. These blocks provide the flexibility to run links and cores at different data-rates, allowing for exploration of optimal data-rates for both electrical and optical links.

C. Ring Tuning Models

An integrated WDM link relies upon ring resonators to perform channel selection. Sensitivity of ring resonances to ring dimensions and the index of refraction leaves them particularly vulnerable to process- and temperature-induced resonance mismatches [35, 36, 37], requiring active closed-loop tuning methods to add to system-wide power consumption [5]. In DSENT, we provide four models for four alternative ring tuning approaches [11]: thermal-only tuning, bit-reshuffled tuning, electrically-assisted tuning, and athermal tuning. Thermal-only tuning is the conventional method of heating using resistive heaters to align their resonances to the desired wavelengths. Ring heating power is considered non-data-dependent, as thermal tune-in and tune-out times are too slow to be performed on a per-flit or per-packet basis and thus must remain always-on. Bit-reshufflers provide freedom in the bit-positions that each ring is responsible for, allowing rings to tune to its closest wavelength instead of a fixed absolute wavelength. This reduces ring heating power at the cost of additional multiplexing logic. Electrically-assisted tuning uses the resonance detuning principle of carrier-depletion modulators to shift ring resonances. Electrically-tuned rings do not consume non-data-dependent ring heating power, but is limited in tuning range and requires bit-reshufflers to make an impact. Note that tuning distances too large to be tuned electrically can still be bridged using heaters at the cost of non-data-dependent heating power. Athermal tuning represents an ideal scenario in which rings are not sensitive to temperature and all process mismatches have been compensated for during post-processing.
TABLE II: DSENT validation points.

<table>
<thead>
<tr>
<th>Model</th>
<th>Comparison Point</th>
<th>DSENT Value</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring Modulator Driver</td>
<td>[38]–50</td>
<td>60.87</td>
<td>11 Gb/s, ER = 10 dB, IL = 6 dB</td>
</tr>
<tr>
<td>Receiver (D/bit)</td>
<td>[13]–52</td>
<td>21.52</td>
<td>3.5 Gb/s, 45 nm SOI</td>
</tr>
<tr>
<td>Buffer (mW)</td>
<td>SPICE-6.95</td>
<td>7.55</td>
<td>6 input ports</td>
</tr>
<tr>
<td></td>
<td>Orion2.0-34.4†</td>
<td>6 output ports</td>
<td></td>
</tr>
<tr>
<td>Crossbar (mW)</td>
<td>SPICE-2.14</td>
<td>2.06</td>
<td>64-bit flit width</td>
</tr>
<tr>
<td></td>
<td>Orion2.0-14.5†</td>
<td>8 virtual channels per port</td>
<td></td>
</tr>
<tr>
<td>Control (mW)</td>
<td>SPICE-0.75</td>
<td>0.83</td>
<td>16 buffers per port</td>
</tr>
<tr>
<td></td>
<td>Orion2.0-1.39†</td>
<td>1 GHz clock frequency</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Orion2.0-0.31†</td>
<td>0.16 flit injection rate</td>
<td></td>
</tr>
<tr>
<td>Clock (mW)</td>
<td>SPICE-0.74</td>
<td>0.63</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Orion2.0-28.8†</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total (mW)</td>
<td>SPICE-10.6</td>
<td>11.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Orion2.0-91.3†</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Orion2.0-5.56†</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Area (mm²)</td>
<td>SPICE-0.070</td>
<td>0.062</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Orion2.0-0.129†</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Orion2.0-0.067†</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

† Values obtained from original Orion 2.0.
‡ Values obtained from re-calibrated Orion 2.0.

D. Optical Link Optimization

Equations 4 and 6 suggest that both the modulator driver’s energy cost and the laser power required at the photodetector depend on the specification of extinction ratio and insertion loss of the modulator on the link. This specification can be relaxed to reduce the power consumption of the modulator driver circuit at a cost of increased laser power. In DSENT, we build optical link models by connecting optical devices together into an optical graph. We trace through the graph to identify optical paths that each starts from a modulator and ends with a detector. Looping through combinations of the extinction ratio and insertion loss, DSENT finds the combination that leads to the lowest power consumption for each identified optical path.

E. Summary

DSENT provides models not only for optical devices but also for the electrical backend circuitry including modulator driver, receiver and ring tuning circuits. These models enable link optimization and reveal tradeoffs between optical and electrical components that previous tools and analysis could not accomplish using fixed numbers.

VI. Model Validation

We validate DSENT results against SPICE simulations for a few electrical and optical models, all for a 45nm SOI technology. For the receiver and modulator models, we compare against a few early prototypes available in literature (fabricated at different technology nodes) to show that our results are numerically within the expected order of magnitude. We also compare our router models with a post-place-and-route SPICE simulation of a textbook virtual channel router and with the estimates produced by Orion 2.0 [21]. To be fair, we also report the results obtained from a modified Orion 2.0 where we replaced Orion 2.0’s original scaling factors with characterized parameters for the 45 nm SOI node and calibrated its standard cells with those used to calibrate DSENT.

VII. Example Photonic Network Evaluation

Though photonic interconnects offer potential for improved network energy-efficiency, they are not without their drawbacks. In this section, we use DSENT to perform a photonic network optimization, a comparison to an electrical alternative at a scaled 11 nm processes, and a technology sensitivity study as an example network study. We choose a 256-tile version of the 3-stage photonic clos network proposed by [5] as the network for these studies. Like [5], the core-to-ingress and egress-to-core links are electrical, whereas the ingress to middle and middle to egress links are photonic. While DSENT is capable of analyzing a broader selection of networks, we choose this topology because it has an electrical network that is logically equivalent (an electrical clos) and carries a reasonable balance of photonic and electrical components. To obtain network-level event counts with which to animate DSENT’s physical models, we implement the clos network in Garnet [6] as part of the GEM5 [40] architecture simulator. Though the GEM5 simulator is primarily used to benchmark real applications, we assume a uniform random traffic pattern to capture network energy at specific loads. Given network event counts, DSENT takes a few seconds to generate an estimation. In this study, we pick energy cost per bit delivered by the network as our figure of merit. Parameters for our baseline configurations are shown in Table III.

A. Network Energy Tradeoffs

First, we examine the impact of varying the degree of WDM channelization on network energy-per-bit. Recall from the parameters of Table III that each link in the network is expected to provide 256 Gb/s of throughput (128 bits/cycle at 2 GHz). Depending on how many λ’s we allocate for a link, the data-rate that each λ carries will be different to maintain the same 256 Gb/s of aggregate throughput. For example, if links run at 8 Gb/s per λ we require only 32 λ (with appropriate SerDes logic to interface an 8 Gb/s link with a 2 GHz core), whereas 64 λ are needed for 4 Gb/s per λ. We
Fig. 5: Energy per bit at various photonic link data-rates plotted across network utilization (left) and a part-by-part breakdown at 16 Gb/s utilization (right). Utilization is plotted up to the point where the network saturates. All data shown are for 45 nm SOI.

Fig. 6: Comparison of network energy per bit vs utilization for both electrical clos (EClos) and photonic clos (PClos) at the 45nm and 11nm technology nodes.

optimize using this degree of freedom in Figure 5. For this network under the this set of parameters, the configuration of 128 \( \lambda \) at 2 Gb/s per \( \lambda \) is optimal across all utilizations. One may expect that the high number of rings at 2 Gb/s results in huge ring tuning costs. However, the bit-shuffling strategy strategies of [11, 39] allow tuning costs to remain comparable; the large modulator, receiver, SerDes, and laser energy costs per bit incurred at high data-rate overwhelm the small savings in tuning power from having fewer \( \lambda \) and rings.

B. Comparison with Scaled Electrical Technology

With an optimized photonic link configuration of 128 \( \lambda \) at 2 Gb/s, we next compare the photonic clos network an electrical equivalent, where all photonic links are replaced an electrical link of equal latency (128 wires, each at 2 GHz). We perform this comparison at the 45 nm SOI and 11 nm Tri-Gate technology nodes, representing present and future electrical technology scenarios, respectively.

From Figure 6, we note that energy per bit rises sharply at low network utilization, as non-data-dependent (NDD) power consumption (leakage, ungated clocks, etc.) is amortized over fewer bits. We note that the trend is more prominent in the photonic clos as compared to the electrical clos due to additional NDD power from ring thermal tuning and laser. This allows the electrical clos to become the energy-optimal implementation below a certain utilization. The photonic clos presents smaller data-dependent (DD) switching costs, however, and thus remains optimal at high utilization.

Comparing 45 nm and 11 nm, it is apparent that both photonic and electrical clos networks benefit from electrical scaling, as routers and logic become cheaper. However, laser and thermal tuning cost scale marginally, if at all, allowing the electrical implementation to benefit more. In the 11 nm scenario, the electrical clos is the more efficient up to roughly half network utilization.

C. Photonic Technology Scaling

For photonics to remain competitive with electrical alternatives at the 11 nm node and beyond, photonic links must similarly scale. We identified non-data-dependent laser and tuning power as particularly problematic, as networks are often over-provisioned to not operate at high utilizations where contention delays are significant. In Figure 7, we evaluate the sensitivity of the photonic clos to waveguide loss and ring heating efficiencies, which affect laser and tuning costs. We see that our loss assumption of 1 dB/cm brings the photonic clos quite close to the ideal (0 dB/cm) and the network could tolerate up to around 1.5 dB/cm before laser power grows out of proportion. Ring tuning power will fall with better heating efficiency. However, since it is not clear whether a 400 K/mW efficiency is physically-realizable, it is worthwhile to consider alternatives such as the electrically-assisted tuning of [11].

VIII. Conclusion

Integrated photonic interconnects is an attractive interconnect technology for future manycore architectures. Though it promises significant advantages over electrical technology, evaluations of photonics in existing proposals have differed greatly in technology assumptions and relied on significant simplifications of active devices. To bring further insight into the dynamic behavior of these active components, we proposed a new tool – DSENT – to capture the interactions between photonics and electronics. By introducing standard-cell-based electrical models and active interface circuit models, we complete the connection between photonic devices and the rest of the opto-electrical network. DSENT will be released to the community.

REFERENCES

Achieved Throughput [Tb/s] Energy per Bit [pJ/bit]

(a) Sensitivity to waveguide loss. Energy per bit vs throughput (left) and energy per bit breakdown at 16 Tb/s throughput (right).

(b) Sensitivity to ring heating efficiency. Energy per bit vs throughput (left) and energy per bit breakdown at 16 Tb/s throughput (right).

Fig. 7: Sensitivity of the photonic clos network to a few select technology parameters. All plots assume the 11 nm electrical technology model.
