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Low-Swing Signaling on Monolithically Integrated Global Graphene Interconnects

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Abstract—In this paper, we characterize the performance of monolithically integrated graphene interconnects on a prototype 0.35- μm CMOS chip. The test chip implements an array of transmitter/receivers to analyze the end-to-end data communication on graphene wires. Large-area graphene sheets are first grown by chemical vapor deposition, which are then subsequently processed into narrow wires up to 1 mm in length. A low-swing signaling technique is applied, which results in a transmitter energy of 0.3–0.7 pJ/b \cdot mm⁻¹ and a total energy of 2.4–5.2 pJ/b \cdot mm⁻¹. Bit error rates below 2×10^{-10} are measured using a $2^{31} - 1$ pseudorandom binary sequence. Minimum voltage swings of 100 mV at 1.5-V supply and 500 mV at 3.3-V supply have also been demonstrated. At present, the graphene wire is largely limited by its growth quality and high sheet resistance.

Index Terms—complementary metal–oxide–semiconductor (CMOS) integrated circuits, graphene, interconnects, low-swing signaling.

I. INTRODUCTION

THE semiconductor industry has advanced at an exponential rate over the last few decades. In recent years, interconnects have become a major limiting factor on the performance of very large scale integrated systems [1]–[3]. Latency, energy dissipation, and signal integrity have all become an increasingly difficult problem to cope with. Many solutions have emerged to address these challenges, ranging from new materials and processes to novel microarchitectures. Improving fundamental material properties are expected to become more important in highly scaled technologies. Surface scattering of conducting electrons is projected to be a major concern, drastically increasing the effective resistivity of copper interconnects [4]. This results from a combination of smaller cross-sectional dimensions and increased liner thicknesses. Heat management will also be increasingly important, as higher energy dissipation of wires and poor thermal conductivity of low- k insulators contribute to substantial temperature increases.

Among many materials, graphene has received much attention in recent years as a replacement for copper intercon-

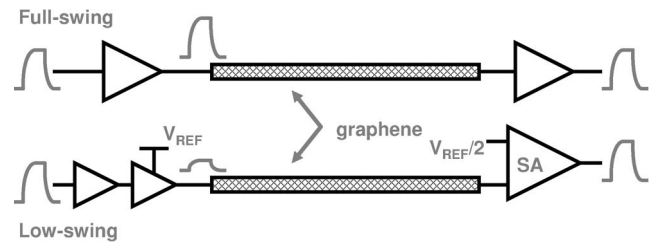


Fig. 1. Overview of the chip. Graphene wires are monolithically integrated and electrically connected to a transmitter and a receiver.

nects. Graphene is a planar sheet composed of carbon atoms. Graphene exhibits ballistic transport [5], [6], high intrinsic mobility [6], [7], high thermal conductivity [8], [9], and high current-carrying capacity [10], making it attractive not only for transistors [11], [12] but also for interconnects [13], [14] and even as a thermal interface material [15]. Theoretical projections show that, at small linewidths (< 8 nm), graphene will outperform copper with a 1 : 1 aspect ratio [13]. Graphene sheets are also an attractive alternative to carbon nanotubes (CNT) as they are more compatible with conventional lithography methods. While selective growth and placement of CNTs has been difficult, graphene can be grown in large sheets [16], [17] and then be subsequently patterned and etched. This results in better control and higher reproducibility of graphene devices.

DC characterization of sub-50-nm graphene interconnects has been reported [10], [14], but very few studies exist on evaluating their performance when integrated with CMOS. Off-chip measurements have limited scope and often require expensive equipment. Furthermore, demonstrating integration with CMOS is a critical step in establishing a path for graphene electronics. These topics are addressed by demonstrating 1-mm graphene wires integrated with a CMOS low-swing transmitter/receiver pair operating up to 50 Mb/s. Chen *et al.* have recently reported the first integrated graphene/CMOS system [18], where CMOS ring oscillators are used to indirectly measure the performance of short graphene wires. In contrast, this paper focuses on end-to-end data communication on medium to long graphene wires (Fig. 1). The performance of each graphene wire is measured in detail, using isolated transmitters and receivers. Wire lengths range from 0.5 to 1 mm for ease of delay measurements and for demonstrating reliable fabrication and signal transmission over longer length scales.

This paper is organized as follows: Section II describes the characteristics of graphene interconnects and their integration

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process with CMOS. Section III discusses the CMOS chip architecture and test setup. Section IV presents the on-chip measurement results. Finally, Section V concludes this paper.

II. GRAPHENE INTERCONNECTS

A. Graphene Growth and Patterning

In this paper, large graphene sheets are grown by chemical vapor deposition (CVD) [16], [17], [19]. Previously, mechanical exfoliation has been used to obtain high-quality graphene [10], [14], but this method produces small flakes of graphene and is not suitable for large-scale integration. CVD-grown graphene can produce arbitrarily large graphene sheets [19], which can then be processed by standard lithography methods to produce narrow graphene wires. For interconnect applications, multilayer graphene is more desirable than a single layer. Thus, the CVD process used in this study uses a Ni catalyst, whereas a Cu catalyst yields monolayer graphene growth [19], [20].

CVD growth is carried out on a 500-nm Ni substrate for 5 min at 1000 °C, with 5–30 sccm of methane and 1300 sccm of hydrogen [17]. This results in a large-area multilayered graphene sheet directly on top of the nickel film. After the growth is completed, a layer of poly(methyl methacrylate) (PMMA) is spun on top of the graphene/Ni substrate. A 10% HCl aqueous solution is used to detach the PMMA/graphene layer from the underlying Ni substrate. This PMMA/graphene film can then be placed on an arbitrary target substrate, whereafter the PMMA layer is rinsed off with acetone [17].

B. Off-Chip Electrical Characterization

For off-chip electrical characterization, the graphene film is placed on a blank SiO₂/Si substrate. The current CVD process yields graphene sheets with an average thickness of 10–15 nm, and the four-point probe measurements yield an approximate sheet resistance between 600 and 900 Ω/sq. An electron-beam lithography step followed by an O₂ plasma etch produces the graphene wires with widths of 1 and 10 μm and lengths from 50 to 300 μm. Either Ti/Au, Cr/Au, or Ti/Pt metal pads have been deposited to make contacts for probing. Fig. 2 shows the resistance of graphene wires as a function of length/width ratio. For this particular batch of devices, the extracted sheet resistance from the slope was roughly 790 Ω/sq, which is close to the value of 740 Ω/sq obtained from the four-point probe measurements.

C. Integration With CMOS

All processes for graphene/CMOS integration are CMOS compatible and follow a similar flow as in [18]. Fig. 3 shows both a drawing and an optical image of the CMOS chip at one end of the graphene wire. A similar flow as in the previous section is used to transfer the graphene film to the CMOS chip and then define the graphene wires. After Ti/Pt contacts are deposited, a CF₄/Ar etch process opens the passivation layer to expose the top metal layer of the CMOS chip. A brief Ar

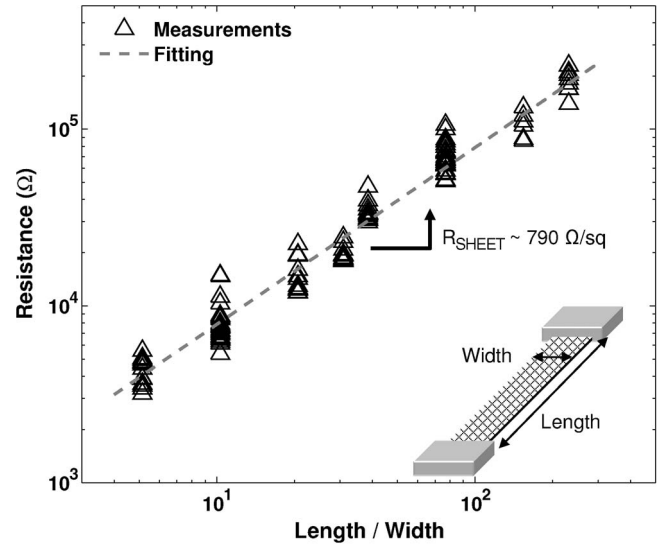


Fig. 2. Resistance of graphene wires fabricated on SiO₂/Si test wafers.

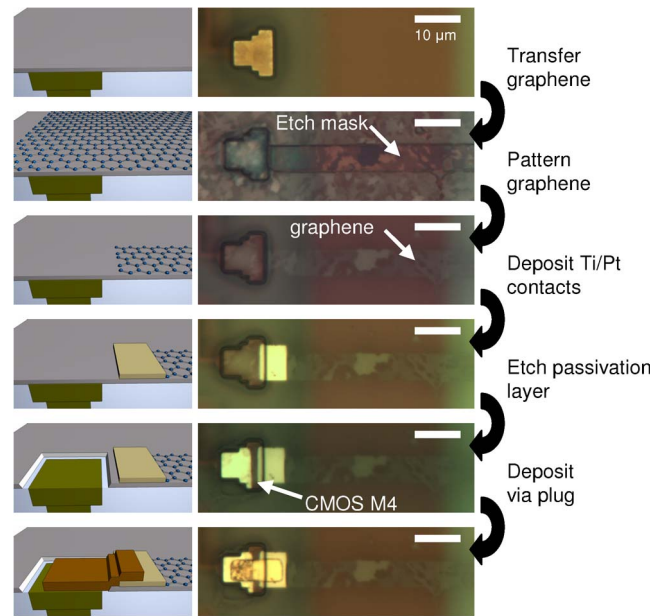


Fig. 3. Process flow for graphene and CMOS integration. A drawing and an optical image at one end of the graphene wire are shown.

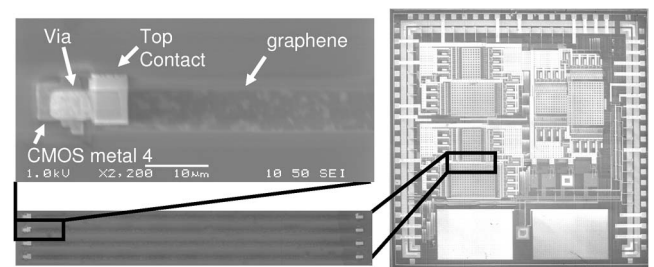


Fig. 4. Scanning electron microscope image of the CMOS die and the integrated graphene wires.

plasma is used to clean the native oxide formed on the exposed Al wires. Finally, Ti is sputtered to make the via plugs between the graphene contacts and the CMOS metal layer. Fig. 4 shows

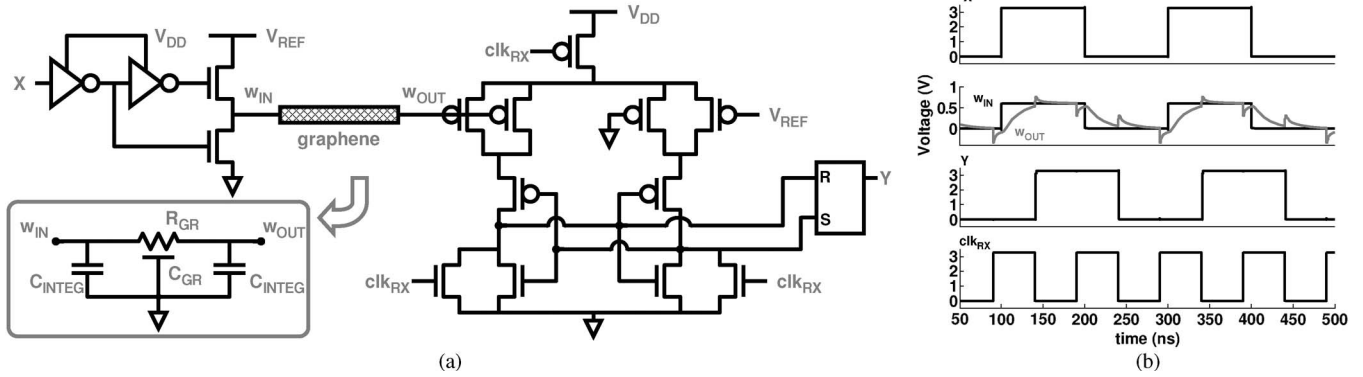


Fig. 5. (a) Diagram of the low-swing design. The graphene wire is simulated as a $\pi 3$ distributed RC wire. (b) Waveform of the simulated low-swing design using $V_{DD} = 3.3$ V, $V_{REF} = 0.6$ V, $R_{GR} = 180$ k Ω , $C_{GR} = 200$ fF, and $C_{INTEG} = 3$ fF.

the CMOS die and the graphene wires. The graphene wires are integrated and electrically connected to the underlying CMOS drivers and receivers.

III. CHIP OPERATION AND TEST SETUP

The CMOS chip includes an array of drivers/receivers to test signal transmission on integrated graphene wires. Full- and low-swing designs are included. The full-swing topology uses an inverter chain to drive the signal and is unrepeated. The energy for signal transmission on a wire is roughly $C_w V_{sw}^2$, where C_w is the capacitance of the wire, and V_{sw} is the voltage swing on the wire. Thus, by reducing the voltage swing, the energy used to transmit a signal can be significantly reduced. While many variants exist [21]–[24], this chip uses an NMOS push-pull driver and a secondary reference voltage source V_{REF} to generate a low-swing signal on the graphene wire. The receiver is a single-ended pseudodifferential latch-based sense amplifier [see Fig. 5(a)] [24].

The graphene wire was simulated using a $\pi 3$ distributed RC wire model. The distributed resistance R_{GR} was estimated from the experimental values of the graphene sheet resistance. The capacitance C_{GR} of the wire was estimated from a field solver using the dimensions of the CMOS metal stack and the passivation layer. The parasitic capacitance due to integration, i.e., C_{INTEG} , was also estimated as 2–5 fF.

The measurement setup is shown in Figs. 6 and 7. The transmitter and the receiver are independently clocked with a programmable delay. The balanced clock tree for the transmitter and the receiver are matched to provide minimal skew. Furthermore, the worst-case delay of the transmitter and receivers are 0.59 ns, which is at least an order of magnitude smaller than the delay of the wire. The data input for each channel can either be an alternating 0101 pattern or a $2^{31} - 1$ pseudorandom binary sequence (PRBS).

IV. MEASUREMENT RESULTS

A. Process and Device Reliability

The test chip was implemented in a standard 0.35- μ m CMOS process. As the integrated graphene/CMOS chip primarily serves as a technology demonstrator, a more advanced CMOS

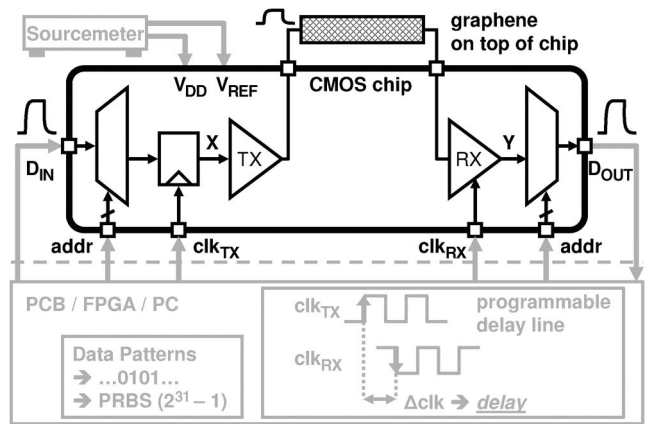


Fig. 6. Diagram of the experimental setup.

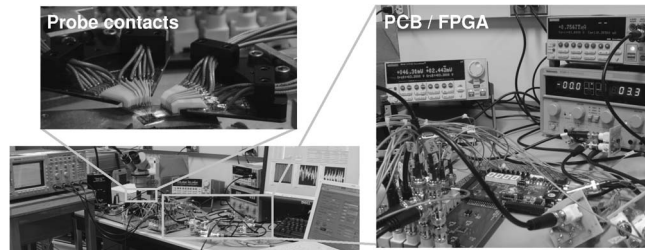


Fig. 7. Photo of the experimental setup.

technology was not needed and not used here. Similarly, the graphene wire widths are relatively large (4 μ m) for ease of fabrication, but the results are expected to scale as linewidths are reduced. The length of the wires are 0.5 and 1 mm. All measurements have used data rates between 1 and 50 Mb/s. Fig. 8 shows the transient waveforms for the low-swing design. A similar waveform is obtained for the full-swing topology. The data output D_{OUT} signal shows that it follows the input D_{IN} pattern and confirms connectivity of the graphene data channel.

The total yield of the working devices was about 60% for 0.5-mm wires and about 3% for 1-mm wires. Unlike the test devices fabricated on flat SiO_2/Si wafers, the device yield for the longer wires has been affected by the topology of the CMOS passivation layer and the increased number of processing steps.

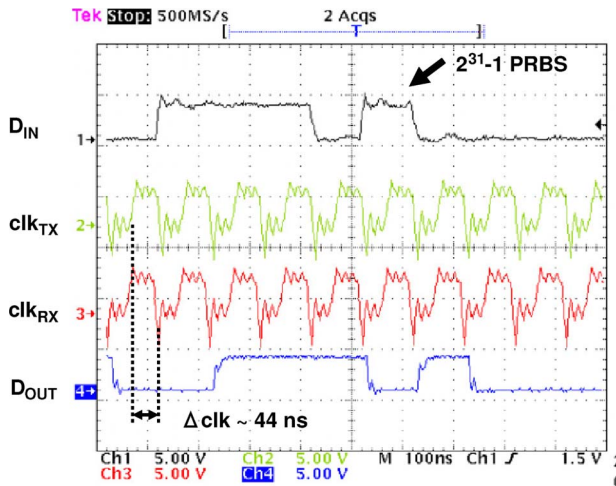


Fig. 8. Transient waveform of digital signals for the low-swing design with a $2^{31} - 1$ PRBS input pattern ($V_{DD} = 3.3$ V, $V_{REF} = 0.5$ V).

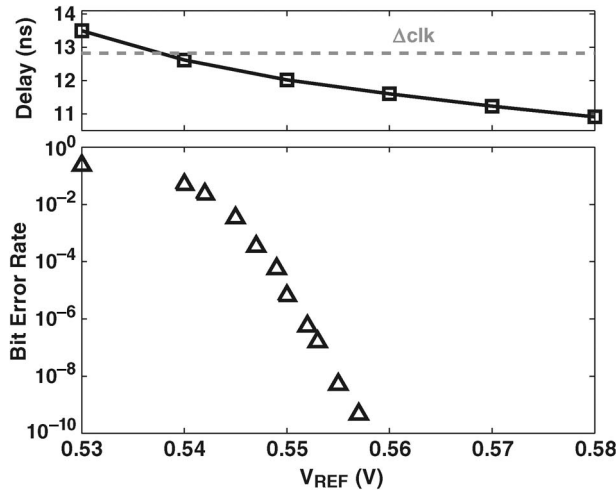


Fig. 9. (Top) Measured delay and (bottom) BERs of a low-swing graphene channel. The clock delay Δclk is fixed at 12.8 ns. The BER is measured using a $2^{31} - 1$ PRBS at $V_{DD} = 3.3$ V.

However, similar to [18], the integration process did not appear to alter the graphene quality. The extracted R_{GR} values from the measurements are close to the expected values. Graphene wires that did not function were mainly a result of lithography alignment errors or tears/voids along the graphene channel. Visual inspection of the chip after each step revealed that graphene teared apart mostly during various lithography/etch steps. Handling small CMOS chips also contributed to lithography challenges. As recent work has demonstrated, the device yield is expected to increase with further process optimization and by working with wafer-scale graphene sheets and CMOS wafers [19], [25].

Overall, the measurements were repeatable and did not show any signs of degradation over the period of a month. Fig. 9 shows the measured bit error rates (BERs) using a $2^{31} - 1$ PRBS. The transmitter/receiver clocks are fixed at a relative skew of roughly 12.8 ns. As V_{REF} decreases, the delay of the channel increases. A sufficient timing margin is guaranteed when the channel delay is much smaller than the preset clock

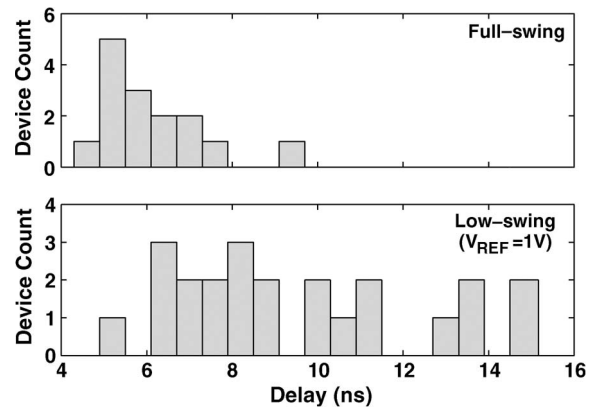


Fig. 10. Histogram of delay measurements ($L = 0.5$ mm) at $V_{DD} = 3.3$ V. For the low-swing design, the plotted data are at $V_{REF} = 1$ V, where the channel delay is minimized.

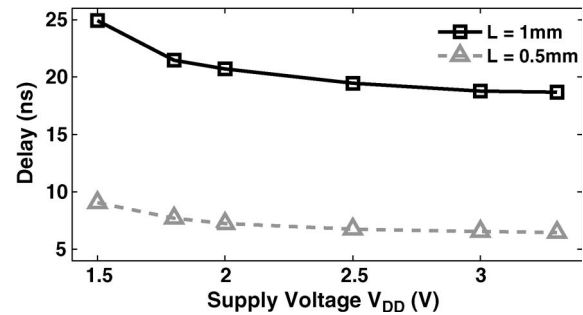


Fig. 11. Measured channel delay of the graphene wire in a full-swing topology.

skew, resulting in a very small BER. This timing margin becomes more difficult to meet as the channel delay approaches and exceeds the preset skew, which is reflected in the increase in BER. For the nominal measurements, the graphene wires show BERs less than 2×10^{-10} at data rates between 10 and 25 Mb/s. This shows reliable operation and that the properties of graphene wires do not drastically change under operating conditions.

B. Delay Performance

The distribution of the measured channel delay is shown in Fig. 10. In Fig. 11, the delay of the full-swing design slightly increases at lower supply voltages. For the low-swing topology, V_{REF} sets the voltage swing on the wire. As V_{REF} is reduced, the delay of the channel also increases (Fig. 12). This appears to be mainly limited by the noise margin and sensitivity of the sense amplifier at the receiver. For lower supply voltages V_{DD} , the kickback voltage at the receiver input node is reduced and thus allows the low-swing design to operate at lower voltage levels. The data in Fig. 12 could be further improved with better amplifier design but nonetheless illustrates an advantage of the low-swing design. At $V_{DD} = 1.5$ V, the delay of a full-swing design increases, whereas the low-swing design maintains a smaller delay by tuning V_{REF} .

A minimum width M4 Al wire ($L = 1$ mm) is included as a reference wire. For the low-swing topology, the measured delay

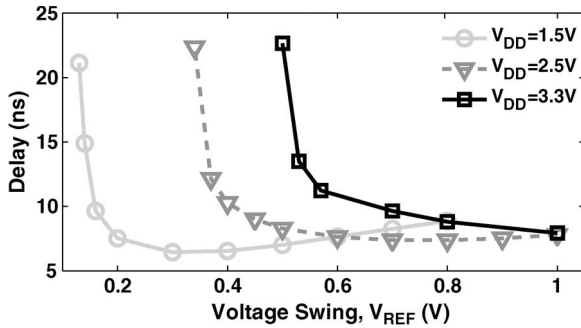


Fig. 12. Measured channel delay of the graphene wire in a low-swing topology ($L = 0.5$ mm).

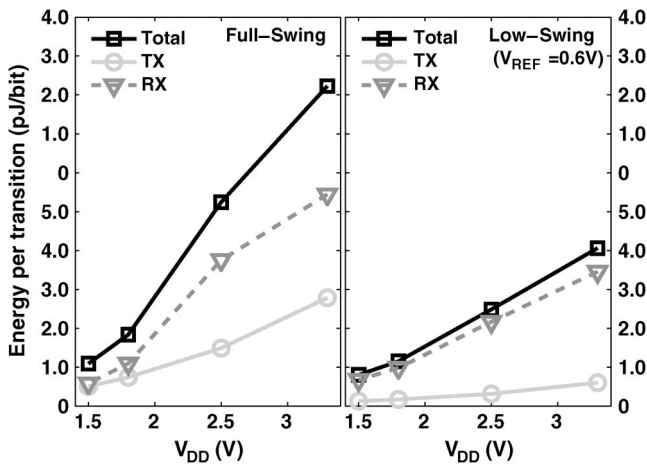


Fig. 13. Measured energy profile of the graphene wire.

on the M4 wire is 0.497 ns, and the delay on the graphene wire with $L = 1$ mm is 13.915 ns. The actual M4 wire delay is likely smaller than 0.497 ns as the measurement is dominated by the transmitter and receiver delay. The graphene wire width is $6\times$ that of the M4 wire but $58\times$ smaller in thickness. The resulting cross-sectional area of the M4 wire is roughly $9\times$ larger than that of the graphene wire. While a fair comparison may be difficult, the (per-width) delay performance of the graphene wire clearly underperforms the M4 Al wire. The performance of the graphene wire is limited by its high sheet resistance (600–900 Ω/sq). Ultimately, better control over the growth process is needed to grow highly uniform multilayer graphene films. The projected limits of graphene in comparison to Cu are shown in Section IV-D.

C. Energy Performance

While the total energy of the low-swing design shows modest improvement ($1.4\text{--}2.1\times$) over the full-swing design, this is limited by the receivers in this paper. In comparison, the transmitter energy of the low-swing design is $4\text{--}4.7\times$ lower than that of the full-swing design. For both design topologies, only 10%–40% of the total energy is dissipated through the transmitters (Fig. 13). While the transmitter energy scales with wire length, the receivers are clocked and require relatively constant conversion energy. For longer wire lengths and higher

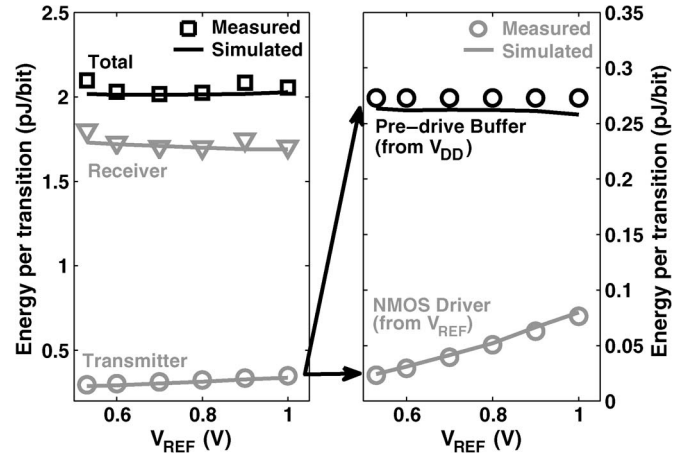


Fig. 14. Comparison of the measured and simulated energy profiles of a low-swing data channel at $V_{DD} = 3.3$ V. The data points are the measured values, whereas the solid lines are from the simulations using the values of $R_{GR} = 90$ k Ω , $C_{GR} = 115$ fF, and $C_{INTEG} = 3$ fF.

density interconnect fabrics, the transmitter energy, and hence the overall energy improvements, is projected to increase.

Although the main advantage of the low-swing design comes from reducing V_{REF} and the energy dissipation on the wire, this energy only accounted for a small portion of the total energy. The energy dissipated from the (low-swing) NMOS drivers is less than 22% of the transmitter energy and less than 4% of the total energy (Fig. 14). Nonetheless, the solid lines in Fig. 14 are from the simulation results using the values of $R_{GR} = 90$ k Ω , $C_{GR} = 115$ fF, and $C_{INTEG} = 3$ fF, which shows good agreement with the measured results. To compare the capacitive load of the wires, another reference wire was included on top of the passivation layer. A 40-nm Ti/Pt wire with the same width as the graphene wire was fabricated. At $V_{REF} = 1$ V, the measured energy dissipation values of the NMOS transistors to drive the wire load are 103.23 and 212.73 fJ for the graphene and Ti/Pt wires, respectively. The Ti/Pt wire is roughly $2.5\times$ thicker than the graphene layer, and this is reflected in the larger energy dissipation from the NMOS drivers. A summary of the on-chip measurements is shown in Table I, and the delay and energy performance show good agreement with the expected values of R_{GR} and C_{GR} .

D. Future Prospects

Most importantly, the graphene quality needs to be improved to be competitive with copper interconnects. The graphene used in this paper is too resistive, but sheet resistances as low as 30 Ω/sq from four layers have been reported from p-doped CVD-grown graphene [25]. Chemical doping of AuCl_3 has also been proven to be very effective on one- to two-layer graphene films, reducing their sheet resistance up to 77% [26].

Table II compares the graphene and CMOS wire performance. A monolayer graphene (on SiO_2) is highly resistive and may also present manufacturing reliability concerns. Multilayer stacking and doping is necessary to achieve comparable numbers to copper. To achieve the same resistance and dimensions of a copper wire in 16-nm CMOS, the desired number of layers

TABLE I
SUMMARY OF MEASUREMENTS

Technology	0.35 μm , 3.3V CMOS	
Graphene Wires	W=4 μm , L=0.5, 1 mm	
	Full-Swing	Low-Swing
Delay (L=0.5mm)	4.7 - 9.6 ns (avg. 6.2 ns)	5.2 - 15.2 ns (avg. 9.5 ns)
Transmitter Energy	2.6-2.8 pJ/bit/mm	0.3-0.7 pJ/bit/mm
Total Energy	6.2-8.2 pJ/bit/mm	2.4-5.2 pJ/bit/mm
Energy-Delay-Product	(low-swing vs. full-swing) up to 3.3x improvement	
Bit error rates	less than 2×10^{-10}	
Minimum voltage swing	100mV (@ $V_{DD}=1.5\text{V}$) 500mV (@ $V_{DD}=3.3\text{V}$)	
Data rates	1 - 50 Mbps	

TABLE II
COMPARISON BETWEEN GRAPHENE AND CMOS GLOBAL WIRES

	R_{SHEET} (Ω/sq)	Graphene Layer #	R ($\text{k}\Omega/\text{mm}$)	C (fF/mm)	Width (nm)
This Work					
Graphene wire	~ 800	16 nm ^a	200	165	4000
Projected Limit of Graphene on SiO₂ ^b					
Single-layer ^c	30	1	1200	57	25
Multi-layer ^c	0.79	38	32	93	25
AsF ₅ -doped ^d	0.73	38	29	115	25
Global Copper Wire ^e					
22 nm CMOS	-	-	19	150	30
16 nm CMOS	-	-	32	180	25

of a multilayer stack is roughly 38, which results in a smaller thickness than that of copper. This leads to roughly half the wire capacitance than copper and, hence, better performance. Furthermore, for the same number of layers, the resistance can be further reduced if the graphene is doped with AsF₅ [27]. The resulting wire capacitance is slightly larger as the interlayer spacing is slightly larger than an undoped multilayer graphene stack.

While Table II lists the ideal values, recent demonstration of sub-50-nm graphene interconnects has shown that the best devices are comparable to copper [14]. Nonetheless, obtaining thick multilayer stacks that approach this limit requires further research. At much narrower linewidths, impurity scattering and line edge roughness are also expected to play a bigger role and increase the resistivity. Finding a reliable method that grows multiple layers while suppressing the interlayer and edge scattering effects remains a future step.

Although the design requirements and process capabilities dictate the graphene thickness, using graphene wires with lower capacitance can be advantageous in energy-constrained systems. The highly resistive wires may be acceptable since many ultralow-energy circuits [28] have modest speed requirements (10 kHz to 10 MHz). More importantly, the ability to grow

very thin layers with high precision provides a manufacturing advantage over copper. This may be important even for general-purpose wires, where the performance benefit shown in Table II is rather modest. The combination of these advantages along with other remarkable properties, namely, high current capacity and thermal conductivity, may prove to be a more compelling reason for adopting graphene. Although producing homogeneous and defect-free graphene layers limits the performance here, this paper establishes a platform to evaluate graphene wires and provides an important step toward realizing a truly integrated graphene/CMOS system.

V. CONCLUSION

This paper has characterized the performance of low-swing signaling on monolithically integrated graphene wires. CVD-grown graphene was fabricated into wires up to 1 mm in length on a 0.35- μm CMOS chip. This paper has primarily focused on technology demonstration, and thus, a more advanced CMOS process was not needed and not used here. Reliable operation of end-to-end data communication on these graphene wires was demonstrated, achieving BERs below 2×10^{-10} . A low-swing signaling technique was used to achieve a transmitter energy of 0.3–0.7 pJ/b · mm⁻¹ and a total energy efficiency of 2.4–5.2 pJ/b · mm⁻¹. Despite the high sheet resistivity of as-grown graphene ($> 600 \Omega/\text{sq}$), integrated graphene links running at 50 Mb/s was demonstrated. On-chip measurements were in good agreement with the simulated results, and recent work shows promise as the reported sheet resistivity is an order of magnitude smaller than the graphene devices used in this paper. Ultimately, cleaner processing steps and optimized CVD growth conditions are necessary to produce higher quality graphene films. Other unique electrical and thermal properties of graphene may also play an important role in establishing graphene as a viable replacement for copper interconnects.

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