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The effect of surface conductance on lateral gated quantum devices in Si/SiGe heterostructures

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Abstract: Quantum dots in Si/SiGe heterostructures are expected to have relatively long electron spin decoherence times, because of the low density of nuclear spins and the weak coupling between nuclear and electron spins. We provide experimental evidence suggesting that electron motion in a conductive layer parallel to the two-dimensional electron gas, possibly resulting from the donors used to dope the Si quantum well, is responsible for the well-known difficulty in achieving well-controlled dots in this system. Charge motion in the conductive layer can cause depletion on large length scales, making electron confinement in the dot impossible, and can give rise to noise that can overwhelm the single-electron charging signal. Results of capacitance versus gate bias measurements to characterize this conductive layer are presented.

1. Introduction

Semiconductor lateral quantum dots used to trap and manipulate individual electrons are promising candidates as qubits for quantum computation¹⁻³. The spin state of the trapped electron can be electrically read out through its effect on the electron motion in a magnetic field⁴⁻⁷. Although well-controlled lateral quantum dots have been made in Gallium-Arsenide (AlGaAs/GaAs) heterostructures, their potential for use as qubits is limited by the hyperfine interaction that causes decoherence of the spin states by coupling the electron's spin to nearby nuclei^{7,8}. In contrast, silicon-based quantum dots are expected to have very long decoherence times (T_2), because of the smaller nuclear magnetic moment, the lower concentration of magnetic nuclei, and the smaller overlap between nuclear and electronic wave functions⁹. In principle, even longer T_2 could be achieved in silicon quantum wells grown using isotopically pure ²⁸Si. A specific device in a Si quantum well confined by SiGe has been proposed by Friesen et al.³ SiGe heterostructures also have the advantage of being widely used in modern silicon technology.

In typical SiGe heterostructures, a Si quantum well is sandwiched between flat Si/SiGe interfaces. The conduction band discontinuity of the SiGe/Si/SiGe heterostructure allows for modulation doping and the associated confinement of electrons in the quantum well of Si, which is under tensile strain; the electrons form a two-dimensional electron gas (2DEG)¹⁰. Much effort has been devoted to the development of quantum dots in this 2DEG¹¹⁻²². The electrons have been confined either by etching or by Schottky gates that deplete the underlying 2DEG forming regions surrounding the quantum dot. Confinement with gates has the advantage of allowing control of the tunneling rates, which is valuable in coupling multiple qubits together. This paper presents evidence for what appears to be a leading

cause of the difficulty experienced by us and by other research groups in reproducibly forming controlled quantum dots in these 2DEGs.

2. Experimental Details

The strained Si channel, and thus the 2DEG, is located 50 nm below the sample surface. The SiGe layers contain 20% Ge and are completely relaxed with the heterostructure, being epitaxially grown on a compositionally graded, relaxed SiGe buffer layer¹⁰. The Si layer is under $\sim 0.8\%$ tensile strain. In view of the well known difficulty to precisely control doping concentration with molecular beam epitaxy (MBE) SiGe, the control of 2DEG density is usually achieved by varying the doping setback layer thickness. It has been shown that above a critical δ -doping density, this approach allows for reasonably well controlled 2DEG density^{23, 24}. As will be illustrated below, we believe that a conductive layer, possibly the Sb donor layer, leads to the observed difficulty in reproducibly forming controlled quantum dots. To study the effect of the donor layer, we have made a series of wafers with a wide range of donor concentrations. The magneto-transport of each wafer has been measured, and the sample (Sample A) with the lowest donor concentration is studied in detail in this paper. We also show measurements on a sample (Sample B) with higher donor concentration, where both the setback thickness and the donor density control the 2DEG density. The 2DEG density and mobility of Sample A, obtained from integer quantum Hall effect measurements, are $2.0 \times 10^{11} \text{ cm}^{-2}$ and $2.2 \times 10^4 \text{ cm}^2/\text{Vs}$, respectively, with a doping level of $3 \times 10^{11} \text{ cm}^{-2}$. The doping level in Sample B is $2 \times 10^{12} \text{ cm}^{-2}$ and its 2DEG density is $4.0 \times 10^{11} \text{ cm}^{-2}$.

A mesa is defined by dry plasma etching, after which Sb/Au ohmic contacts are deposited using e-beam evaporation and are annealed at 325° C for 5 minutes. We define Ti/Au top gates using either photolithography or electron-beam lithography, depending on the dimensions. The Ti/Au forms

Schottky gates, allowing us to deplete the 2DEG underneath them, with the goal of creating a lateral quantum dot, as is commonly done in GaAs/AlGaAs devices.

3. Results

In almost all cases, when the gates are biased negatively enough to deplete the 2DEG directly beneath them our quantum dot devices are completely insulating. From this we conclude that the 2DEG in the entire region of the dot is depleted. To determine how far the depletion spreads from the gate we have fabricated the device from Sample A, sketched in Fig. 1 (inset), containing constrictions with gate separations varying in size from 3 μm to 10 μm , much larger than those used to form quantum dots. We find that at 4 K conduction (measured at 130 Hz) between ohmic contacts on opposite ends of the mesa (outside the region sketched in Fig. 1 inset) is turned off completely when a voltage more negative than about -6 V is applied to any pair of gates. In fact, applying this voltage to even a single gate turns off the conductance, showing that the entire mesa, at least at its narrowest point ($\sim 30 \mu\text{m}$ wide), is completely depleted. From this we conclude that there must be a small amount of leakage between the gate and a conductive layer parallel to the 2DEG, allowing the gate to deplete the surrounding area. We have tried, unsuccessfully, to measure this leakage directly. One candidate for this conductive layer is the Sb δ -doping donor layer. Alternatively, the conduction could be in the cap layer, a layer of Si $\sim 2\text{-}4$ nm thick, deposited on the surface of the heterostructure to avoid oxidation of the SiGe. This cap layer would be conducting if the band bending at the oxide interface is strong enough to pull the electrochemical potential below that of the 2DEG. In either case, the conduction outside the 2DEG would presumably increase with doping density. Both the donor layer and Si cap layer extend to the ohmics, where the sample is grounded.

To further characterize the 2DEG and the extra parallel conductive layer, we have measured the capacitance between each gate and one of the ohmic contacts, as a function of DC gate voltage and frequency. Fig. 1 shows the dependence of the capacitance on gate voltage (Gate_1), measured at 130 Hz. The amount of stray capacitance, measured with an empty chip carrier in the cryostat, is around 0.1 pF, and it has been subtracted in all data presented in this paper. There are two steps in the capacitance as the bias is made more negative. We observe large hysteresis when the gate voltage is swept up and down through the second step at -6 V. We infer that the first step in capacitance, at roughly -0.5 V, corresponds to depletion of the 2DEG directly under the gate. Capacitance measurements as functions of gate bias for different gates are plotted in Fig. 2(a). The amount by which the capacitance changes at the first step is in agreement with the calculated parallel-plate capacitance between the top gates and the 2DEG, as summarized in Fig. 2(a) inset.

We provide a simple model to explain our results, as sketched in Fig. 2(b). C_1 refers to the capacitance between the top gate and the 2DEG directly underneath it; C_2 refers to that between the top gate and the conductive layer not directly under it; C_3 refers to the capacitance between the 2DEG and conductive layer in regions of the mesa where there are no gates; R_1 is the leakage resistance between the top gate and the conductive layer, which may vary with the DC voltage applied to the gate at -6 V; and R_2 is the resistance within the conductive layer. We assume that the conductive layer does not exist underneath the gates, possibly because the Schottky barrier caused by the metal gate depletes the charge carriers.

At zero gate voltage (Fig. 2(b)) the 2DEG resides throughout the mesa. When the gate voltage is between -1 V and -6 V, the 2DEG is depleted under the gate, but remains in the rest of the mesa. When the gate voltage approaches -6 V, leakage between the top gate and the conductive layer spreads the

negative potential along the conductive layer. This causes the 2DEG under the area surrounding the gate to be depleted and further reduces the capacitance.

Fig 2(c) is a circuit diagram to explain the capacitance step around -0.5 V. If around 0 V, the combination impedance Z_{bot} of R_1 , R_2 , C_2 and C_3 is mostly capacitive, removing C_1 from the top circuit of Fig. 2(c) causes a capacitance change of approximately C_1 . In order for Z_{bot} to be mostly capacitive at $V_g = 0$ V, R_1 and R_2 must be much smaller than the impedance of C_3 at our measurement frequency. The frequency dependence measurements presented later support this assumption. Because there is no conduction in the 2DEG under the gate when V_g is more negative than -0.5 V, the capacitor C_1 cannot be charged in response to the AC excitation. C_1 is effectively eliminated from the circuit, as illustrated in the bottom circuit of Fig. 2(c). This results in the capacitance step around -0.5 V in agreement with the calculated capacitance change, as seen in Fig 2 (a) inset.

We have measured the capacitance and the conductance between Gate_1 and the ohmics at frequencies between 130 and 9700 Hz (Fig. 3). Because of the hysteresis at more negative voltage, the frequency study is carried only for gate voltages between 0 and -1 V. The circuit models of Fig. 2 are fit to this frequency dependence. We find that R_1 between the top gate and the conductive layer and R_2 , the resistance within the conductive layer, are both ~ 10 M Ω , although the errors in the best fit values are very large. $C_1 = (0.3 \pm 0.1)$ pF, $C_2 = (0.2 \pm 0.9)$ pF and $C_3 = (2.5 \pm 0.1)$ pF, respectively. Although the values of the resistances and C_2 are poorly determined by the fit, C_1 and C_3 are well-constrained, and the simple model is consistent with the overall frequency dependence. Note that our simple model cannot account for the change with gate voltage in the conductance at the higher frequencies.

Since we have strong evidence for conduction parallel to the 2DEG, it is not surprising that Sample B, which has higher doping density than Sample A, cannot be used to form laterally-gated quantum dots. Furthermore, we have evidence that even if this were possible, we would not be able to observe Coulomb blockade because of noise, probably coming from the donor layer.

Fig. 4 inset shows the gate electrodes for a device made with Sample B, in which we attempted unsuccessfully to make a quantum dot. The device is cooled in a ^3He refrigerator to a base temperature of 400 mK, and a negative voltage is applied to the highlighted gates (colored red) in the hope of forming a narrow conduction path known as a quantum point contact (QPC). Such QPC's are very sensitive to the electrostatic environment. The time dependence of the conductance acts as a sensitive probe of the charge motion near the constriction, because such motion alters the potential in the constriction. A standard two-lead differential conductance measurement is carried out with an excitation voltage of 92 μV at 103 Hz to obtain the pinch-off profile of the QPC. We then fix the gate voltage at $V_g = -1.3$ V and measure the DC resistance of the QPC by applying a voltage across the QPC and monitoring the current through the constriction.

From the slope of G versus V_g we find that the jumps (ΔG) observed in the conductance (Fig. 3(b)) correspond to a change of gate voltage (Fig. 3(a)) of 200 mV. This is ten times larger than the expected Coulomb blockade peak spacing in a quantum dot of the size that would be created using all the gates in Fig. 4. Thus, even if we were able to confine electrons in this dot, the single-electron Coulomb charging peaks in conductance could not be observed unless the quantum dot is an order of magnitude smaller in size. Fabrication of such small dots poses technical difficulties.

4. Discussion

We have provided evidence that conduction in the δ -doping layer or the cap layer is responsible for the difficulty we have had in creating controlled quantum dots using Si quantum wells in SiGe heterostructures. In either case, the high doping density is not in our favor. The capacitance as a function of voltage is consistent with depletion of the 2DEG under the gates at small negative voltage, and with depletion over a much larger area at larger negative voltage. The latter requires transfer of charge between the gate and the donor layer or the cap layer, but we have been unable to directly detect a leakage path that could be responsible. The observation that the conductance can be eliminated over distances as large as $\sim 30 \mu\text{m}$ makes it clear why we are unable to form quantum dots in devices, like that in Fig. 4, with dimensions $\sim 300 \text{ nm}$.

We speculate that other workers, who have reported controlled quantum dots in Si quantum wells, have been more successful at reducing the effect of donor layer. However, such fine tuning is not an attractive way to create quantum dots for applications such as single-electron qubits. This raises the question of why the donor layer is so troublesome in SiGe heterostructures but not in GaAs/AlGaAs heterostructures. We speculate that the donors in AlGaAs are much more localized than the shallow Sb donors in Si. Indeed, we have found that there is charge motion in the donor layer in GaAs/AlGaAs heterostructures at 4 K, when the doping is done in GaAs, where the donors are shallow. The evidence for this is that the density in a QPC anneals with time at 4 K²⁵.

Having reported our lack of success in making controlled quantum dots in SiGe quantum wells using modulation doping, we nonetheless believe that the effort to make such dots is very important. We hope that it will be more effective to induce the 2DEG capacitively, so that the donor layer can be completely eliminated.

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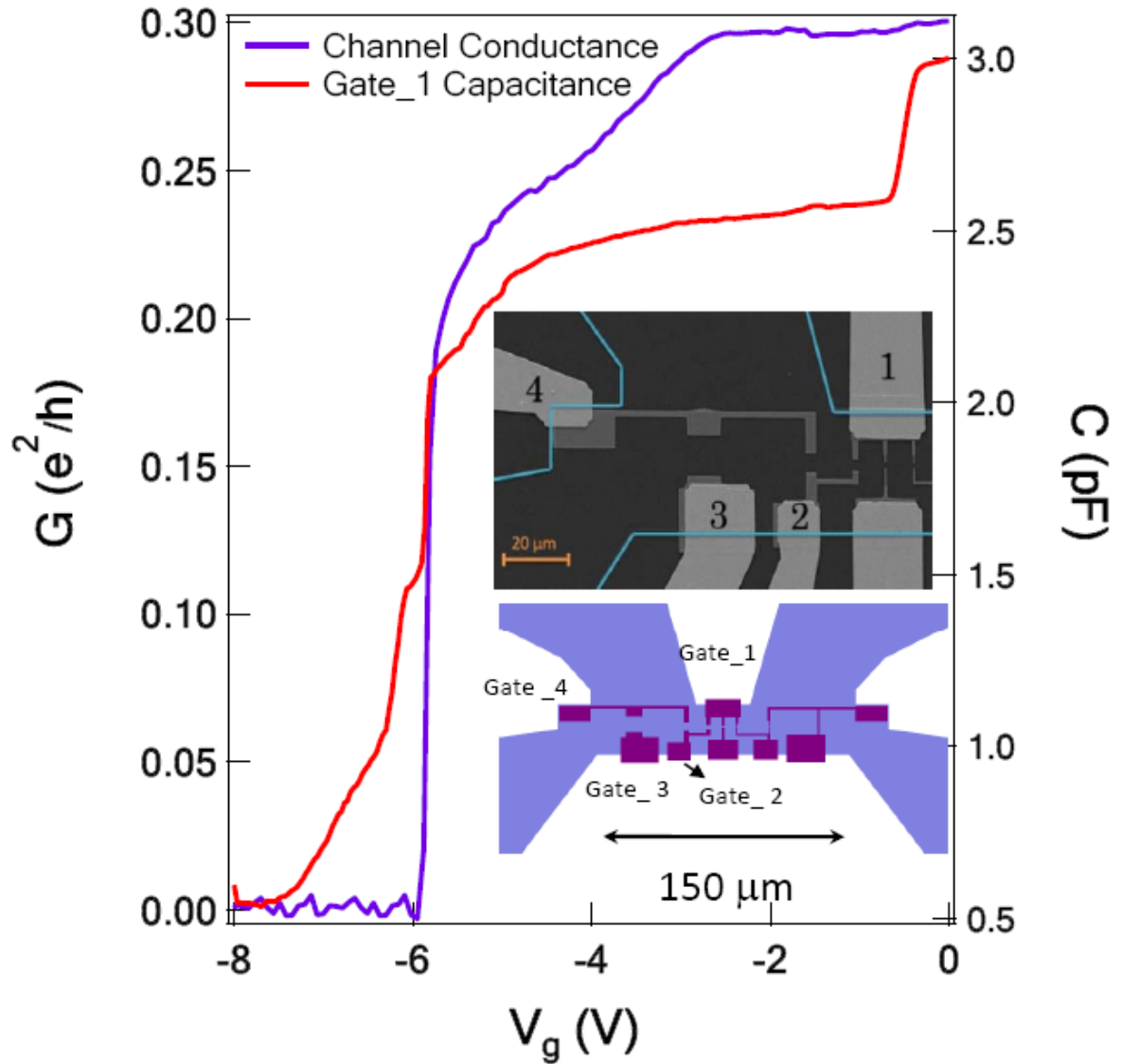


Figure 1. Differential conductance and capacitance of Sample A as a function of voltage applied to only Gate_1 at 4 K. The inset shows a false-color micrograph and a sketch of the active region of the device. The blue area in the sketch is the mesa nearby the gates; the four corners of the mesa extend beyond the sketch by ~ 1 mm, where there are four 0.08 mm^2 ohmic contacts near the edges of the corners. Each pair of top gates (purple color) forms a conducting channel; the separation between Gate_1 and Gate_2 is $3 \mu\text{m}$; between Gate_2 and Gate_4 is $5 \mu\text{m}$; between Gate_3 and Gate_4 is $10 \mu\text{m}$. All the gates

shown in the inset extend outside the mesa and are bonded to a chip carrier. The unmarked gates are not used for measurement but they are bonded and grounded through this study.

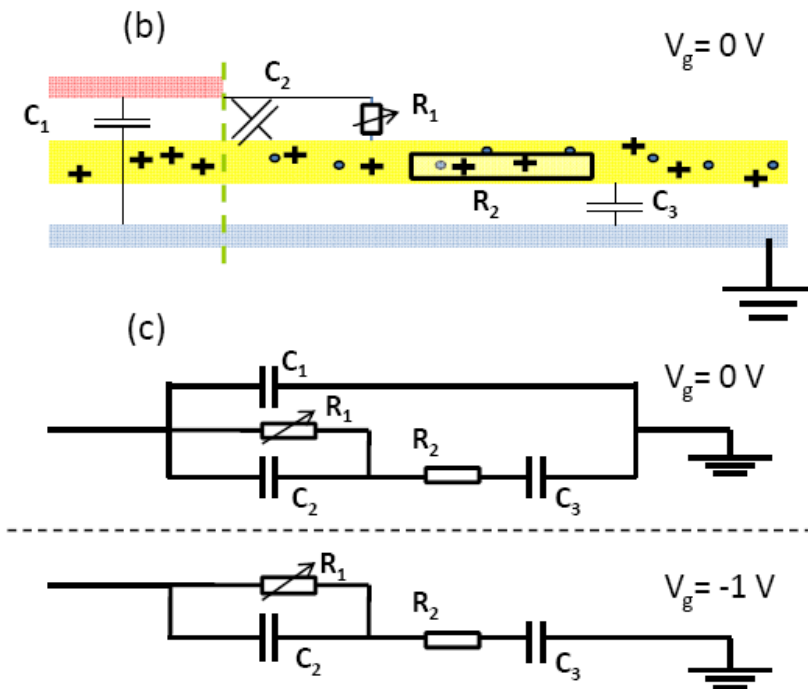
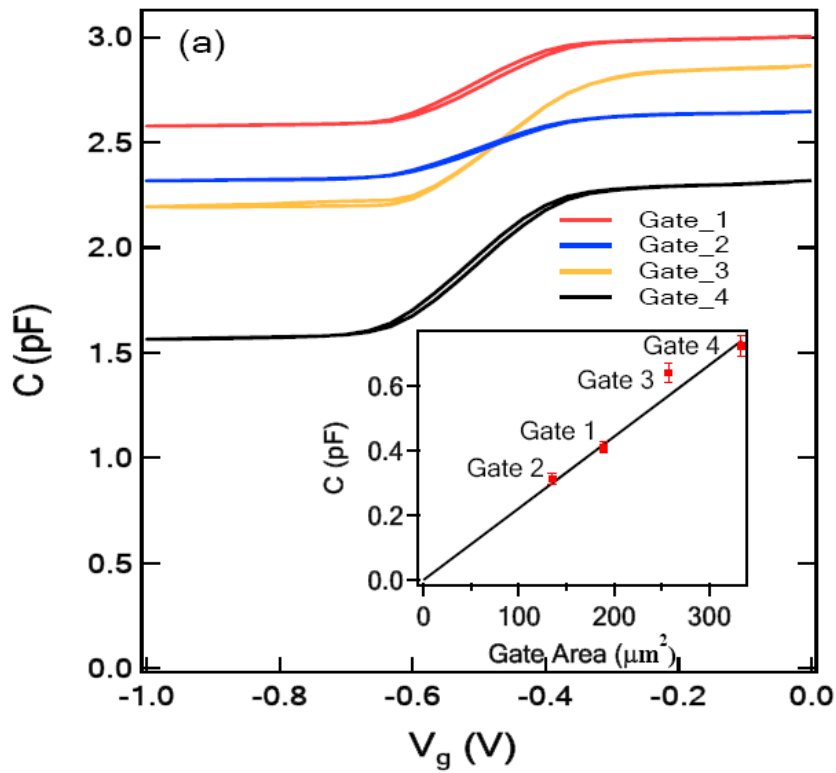


Figure 2. (a) Capacitance as a function of gate voltage for the individual gates in Fig. 1, in the range -1 to 0 V, showing only small hysteresis upon change of sweep direction. Inset: The black solid line is the calculated parallel plate capacitance between a top gate and the 2DEG underneath, as a function of the area of the top gate that overlaps the 2DEG. The red data points are the measured capacitance changes at the step near $V_g = -0.5$ V for each gate, plotted against the gate's area of overlap with the underlying 2DEG. (b) Simplified model to explain the capacitance measurements. The top gate is colored red, the conductive layer yellow, with fixed ions (+'s) and mobile electrons (small dots), and the 2DEG blue. Both AC and DC voltages are applied to the top gate, and the 2DEG is grounded by the ohmic contacts, which are not shown. Near $V_g = 0$, before the first capacitance step has occurred, the conductive layer underneath the gate is depleted by the Schottky barrier caused by the metal gate. (c) Simplified circuit to describe the situation near $V_g = 0$ V (top) and $V_g = -1$ V (bottom), in which the 2DEG is depleted under the gate.

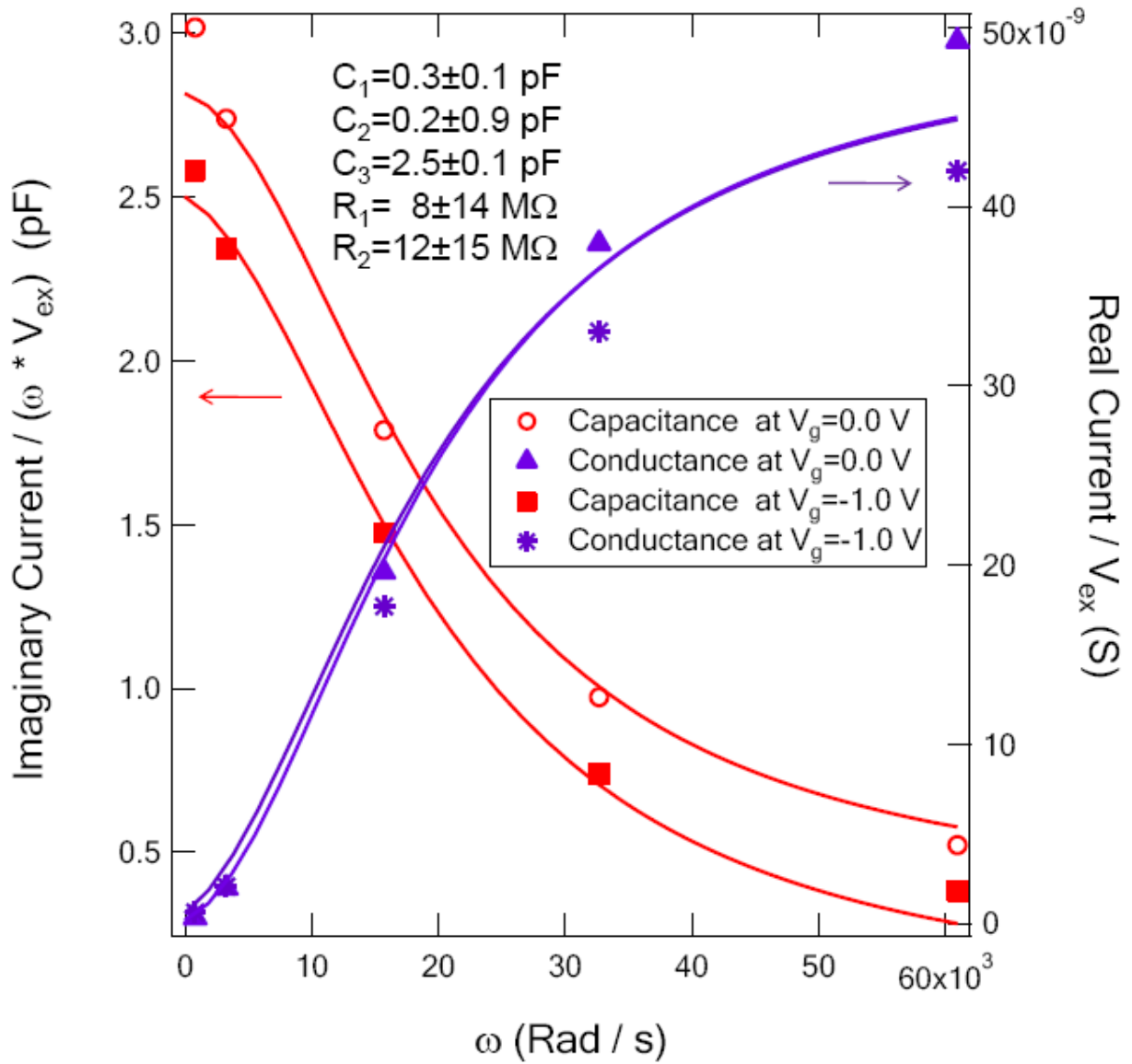


Figure 3: Frequency dependence of the imaginary current normalized by the excitation voltage and angular frequency (Left Axis, red), and real current normalized by the excitation voltage (Right Axis, purple) for Gate_1. The curves are fits based on the circuits of Fig. 2 (c).

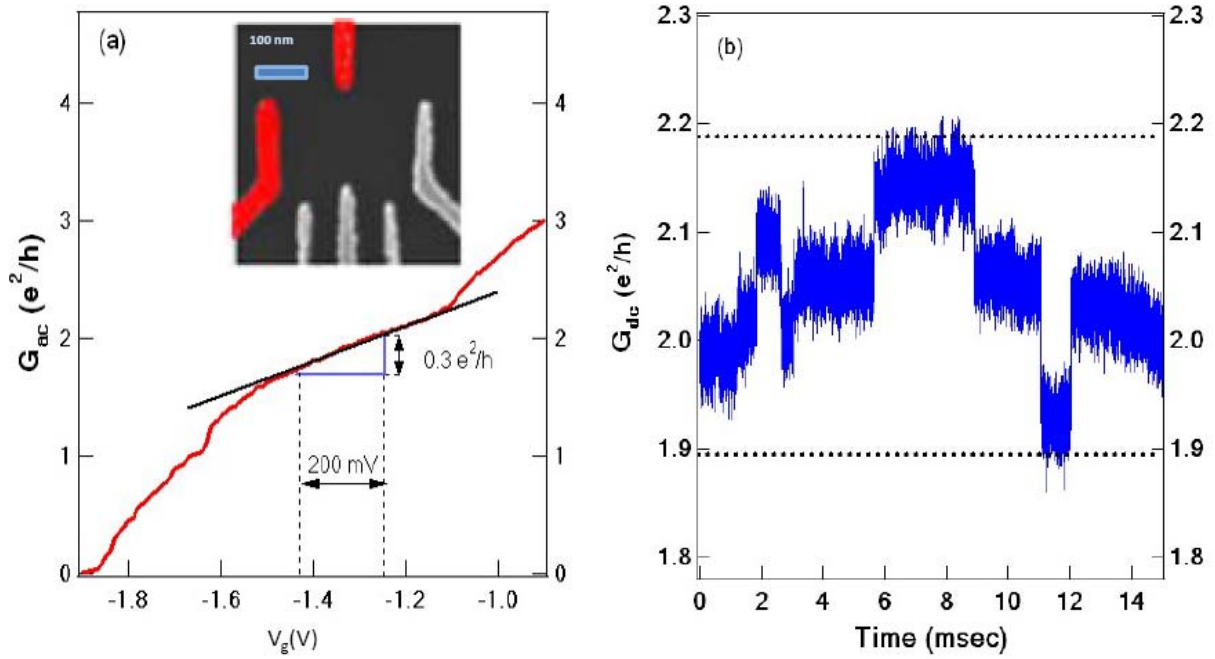


Figure 4. (a) Conductance as a function of the voltage applied to a pair of split gates fabricated on Sample B, measured using AC voltage excitation across the constriction. Inset: False-color micrograph of the device. Only the highlighted gates were used to form the constriction. The conduction channel of the 2DEG is completely pinched off at -2 V. (b) An example of telegraph noise of magnitude $0.3 e^2/h$, measured at $V_g = -1.3$ V, with a bandwidth from zero to 300 kHz.

References:

1. D. Loss and D. P. DiVincenzo, *Phys. Rev. A* **57**, 120 (1998).
2. R. Vrijen et al., *Phys. Rev. A* **62**, 012306 (2000).
3. M. Friesen et al., *Phys. Rev. B* **67**, 121301(R) (2003).
4. J. M. Elzerman et al., *Nature(London)* **430**, 431 (2004).

5. K. Ono, D. G. Austing, Y. Tokura and S. Tarucha, *Science* **297**, 1313 (2002).
6. A. C. Johnson, J. R. Petta, C. M. Marcus, M. P. Hanson and A. C. Gossard, *Phys. Rev. B* **72**, 165308 (2005).
7. F. H. L. Koppens et al., *Science* **309**, 1346 (2005).
8. J. R. Petta et al., *Science* **309**, 2180 (2005).
9. C. Tahan, M. Friesen and R. Joynt, *Phys. Rev. B* **66**, 035314 (2002).
10. F. Schaffler, *Semicond. Sci. Technol.* **12**, 1515 (1997).
11. L. J. Klein et al., *Appl. Phys. Lett.* **84**, 4047 (2004).
12. M. R. Sakr, H. W. Jiang, E. Yablonovitch and E. T. Croke, *Appl. Phys. Lett.* **87**, 223104 (2005).
13. T. Berer et al., *Appl. Phys. Lett.* **88**, 162112 (2006).
14. L. J. Klein, D. E. Savage, and M. A. Eriksson, *Appl. Phys. Lett.* **90**, 033103 (2007).
15. N. Shaji et al., *Nature Physics* **4**, 540 (2008).
16. M. Thalakulam et al., *Appl. Phys. Lett.* **96**, 183104 (2010).
17. C. B. Simmons et al., *Phys. Rev. B* **82**, 245312 (2010).
18. A. Wild et al., *New Journal of Physics* **12**, 113019 (2010).
19. M. Thalakulam et al., arXiv:1010.0972v1 (2010).
20. M. G. Borselli et al., *Appl. Phys. Lett.* **98**, 123118 (2011).
21. M. Yuan et al., *Appl. Phys. Lett.* **98**, 142104 (2011).

22. C. B. Simmons et al., *Phys. Rev. Lett.* **106**, 156804 (2011).
23. F. Stern and S. E. Laux, *Appl. Phys. Lett.* **61**, 1110 (1992).
24. F. Monsef et al. *J. of Appl. Phys.* **95**, 3587 (2004).
25. I. P. Radu. et al. *Science* **320** 899 (2008).