Analysis of a Transfer Admittance Technique for Automatic Testing of Flat Panel Displays

by

Paul R. Pilotte

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1992

copyright (c) Paul R. Pilotte, MCMXCII. All rights reserved.

The author hereby grants to MIT permission to reproduce and to distribute copies of this thesis document in whole or in part.
Analysis of a Transfer Admittance Technique for Automatic Testing of
Flat Panel Displays

by

Paul R. Pilotte

Submitted to the Department of Electrical Engineering and Computer Science on May 8, 1992 in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering and Computer Science

Abstract

A theoretical and experimental study was carried out on the use of measurements of the pixel admittances in a TFT active matrix liquid crystal display (TFT-LCD) for automatic testing of such displays. Series and parallel equivalent circuit models were used to model the admittances of individual pixels. Transmission line theory was used to model the effect of panel line resistances and shunt capacitances on the admittance measurements at various locations on the panel.

The results of experiments taken on a TFT active matrix substrate with 480 gate and 1920 drain lines showed that individual pixel admittances could be measured with a standard deviation of less than .001pF and .05nS. The measurements also showed that the series circuit pixel measurements could measure TFT on conductance with a standard deviation of less than 0.1nS. Measurements along a gate and along a drain showed that the transmission line model accurately predicted the variation in pixel admittance measurements across a panel.

The use of a transfer admittance method for panel measurements and for diagnosing defects on a TFT-LCD substrate has been shown. A test system using the transfer admittance method to quickly and automatically test and diagnose defects and characteristics of TFT-LCD panels is described.

Thesis Supervisor: John L. Wyatt
Title: Professor of Electrical Engineering, MIT

Thesis Supervisor: Henry P. Hall
Title: Senior Staff Scientist, GenRad
Acknowledgements

I would like to thank all the people at GenRad for their guidance and support over the last three years. I would especially like to thank Henry Hall with whom I have worked very closely since my first day here at GenRad. Henry's enthusiasm for his work and his 40+ years experience in measuring impedance has helped shaped me both technically and personally.

In order to make this thesis a summary of the transfer admittance test method, I have included some background material for which I was a contributor and not the principal designer. The transfer admittance test method was the invention of Henry Hall, who holds a patent for the test technique. In working with Henry since the beginning of this project, I have made contributions in all subjects described here. I was particularly responsible for the admittance measurement hardware and software implementation of the LCD test system for which I built two prototype breadboards as a proof of concept. I worked closely with Henry in developing much of the test theory. I made significant contributions in the pixel model for LCD testing, the transmission line effects, and the improvements for automatic testing. I played a smaller role in the development of the guarding theory presented at the end of chapter 2. All of the measurement data presented in this thesis was taken using the GenRad GTS-1 LCD test and measurement system with an automatic prober supplied by Tokyo Electron Limited (TEL) of Japan with whom GenRad has partnered in the development of the LCD test system.
I would also like to thank GenRad's "Looking Glass" (the company name for the LCD tester project) team with whom I have worked over the last two years in applying the theory Henry and I developed into a working test system: Pete Dolan, John Lyons, David Martin, Geoff Templeton, Tony Suto, Rick Santarpio, Sharon Albertini, Craig Dawson, Joan Schopf, Lisa Martin, Paul Porreca, and everyone else who was involved. I also thank the people at TEL for their gracious hospitality when I was in Japan acquiring data for my thesis. I especially want to thank Mick Nanbu of TEL with whom I have worked very closely over the past three years. I thank Dave Warnock, Fred Otto, and Ron Roetzer with whom I worked when I first came to GenRad and who have since started a successful company.

I want to thank Professor John Wyatt for his support and enthusiasm for my work and his suggestions for possible improvements and future work. I also thank Prof. Walter Reintjes for his work in the success of the Masters in Industry Program which enabled me to study at MIT while working at GenRad.

I would especially like to thank my family for their support in all of my education and upbringing. Thanks Mom and Dad!
# Table of Contents

List of Figures. ......................................................... .8

List of Tables ......................................................... .11

1. Introduction ......................................................... 12
   1.1 Liquid Crystal Cell Operation. ................................. 12
   1.2 Liquid Crystal Display Types ................................. 14
   1.3 TFT Active-Matrix Topologies ................................. 15
   1.4 Economics of Testing AM-TFT-LCDs ......................... 16
   1.5 Other AM-TFT-LCD Test Methods. ........................... 18

2. Transfer Admittance Test Method ................................. 20
   2.1 Review of Admittance and Impedance ....................... 20
   2.2 Summary of Transfer Admittance Test Technique ........... 23
   2.3 Admittance Measurement and Calibration ................... 26
   2.4 Measurement Precision and Digital Filtering of Noise .... 29
   2.5 Varying Measurement Test Conditions ..................... 33
   2.6 Effect of LCD Substrate Parameters ....................... 34
      2.6.1 Rprg value
      2.6.2 Rcsr value
      2.6.3 Rprd value
2.7  Measurement Connections Errors ........................................... 37
2.8  Guarding of Inactive Gate and Drain Lines ......................... 40

3.  Pixel Model for LCD Testing ............................................. 44
   3.1  Equivalent Pixel Model for AM-TFT-LCD Pixels ................ 44
   3.2  Parallel Admittance Measurements .................................. 46
   3.3  Series Admittances to Measure TFT On Conductance ............ 52
   3.4  Measurement of TFT Off Conductance ............................... 55
   3.5  Characterization of LCD Operation Effects with Pixel
        Admittance Measurements ........................................... 55

      3.5.1  Effect of TFT "on" Conductance on LCD Operation
      3.5.2  Voltage Feedthrough Effect
      3.5.3  TFT Threshold Effect
      3.5.4  Pixel Leakages
      3.5.5  TFT Leakages

4.  Transmission Line Effects ............................................. 60
   4.1  Model for LCD Transmission Line Effect .......................... 60
        4.1.1  Complete Transmission Line Model
        4.1.2  Simplified Transmission Line Model
   4.2  Row Measurements on a LCD panel ................................. 64
   4.3  Column Measurements on a LCD Panel ............................. 67

5.  Conclusion ............................................................... 69

Appendix 1.  Glossary ....................................................... 71

Appendix 2. TFT Topology .................................................. 74
Appendix 3. Specifications for TFT-LCD Substrate Used for Experimental Measurements . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 76

Bibliography. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 78
# List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1</td>
<td>Operation of the liquid crystal material in a LCD</td>
<td>13</td>
</tr>
<tr>
<td>1-2</td>
<td>480x1920 TFT-LCD substrate with storage capacitors tied to a common Cs bus line</td>
<td>16</td>
</tr>
<tr>
<td>1-3</td>
<td>Possible faults on a TFT-LCD substrate with storage capacitors tied to a Cs bus line</td>
<td>18</td>
</tr>
<tr>
<td>2-1</td>
<td>Measurement of impedance or admittance.</td>
<td>21</td>
</tr>
<tr>
<td>2-2</td>
<td>Two-terminal equivalent circuit models (a) Series equivalent circuit model (b) parallel equivalent circuit model</td>
<td>22</td>
</tr>
<tr>
<td>2-3</td>
<td>Ideal transfer admittance test of an LCD substrate with a guard ring</td>
<td>22</td>
</tr>
<tr>
<td>2-4</td>
<td>Transfer admittance test of a TFT-LCD substrate of type &quot;Cs tied to next gate line&quot;</td>
<td>24</td>
</tr>
<tr>
<td>2-5</td>
<td>Transfer admittance test of a TFT-LCD substrate of type &quot;no Cs capacitor&quot;</td>
<td>25</td>
</tr>
<tr>
<td>2-6</td>
<td>Transfer admittance test of a TFT-LCD substrate of type &quot;Cs capacitor tied to Cs common line&quot;</td>
<td>26</td>
</tr>
<tr>
<td>2-7</td>
<td>Current detector block diagram</td>
<td>27</td>
</tr>
<tr>
<td>2-8</td>
<td>Equivalent noise sources at detector input</td>
<td>30</td>
</tr>
<tr>
<td>2-9</td>
<td>Detector input noise currents as a function of Rprd</td>
<td>31</td>
</tr>
<tr>
<td>2-10</td>
<td>The power magnitude response of the DFT filter with $M'=23$ and $N'=128$. The abscissa shows the DFT bin number. The 0th bin is dc while the 63rd bin is the Nyquist frequency</td>
<td>32</td>
</tr>
<tr>
<td>2-11</td>
<td>Substrate connections which may affect the measurement accuracy and precision</td>
<td>35</td>
</tr>
<tr>
<td>Section</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>2-12</td>
<td>Three-terminal, single guard TFT-LCD substrate measurement connections</td>
<td></td>
</tr>
<tr>
<td>2-13</td>
<td>Three-terminal, single guard simplified circuit diagram</td>
<td></td>
</tr>
<tr>
<td>2-14</td>
<td>Three-terminal, double guard TFT-LCD substrate measurement connections</td>
<td></td>
</tr>
<tr>
<td>2-15</td>
<td>Circuit diagram of the LCD active matrix with some gate and drain lines left unguarded. This diagram shows the alternate current paths through the line crossing capacitances in the LCD matrix.</td>
<td></td>
</tr>
<tr>
<td>3-1</td>
<td>Equivalent circuit model for TFT &quot;off&quot; and &quot;on&quot; measurements with a Cs common bus topology</td>
<td></td>
</tr>
<tr>
<td>3-2</td>
<td>Equivalent circuit model for delta admittance measurements with a Cs common bus topology</td>
<td></td>
</tr>
<tr>
<td>3-3</td>
<td>Simulated effect of pixel leakage conductance, Gpixel, on the measured value of ΔGp. Curves for measured ΔGp versus Gpixel are shown for three frequencies, 4kHz, 8kHz, and 12kHz. The measurement precision at 8kHz is shown for reference</td>
<td></td>
</tr>
<tr>
<td>3-4</td>
<td>Simulated effect of TFT on conductance, Gtft, on the measured value of ΔGp. Curves for measured ΔGp versus Gpixel are shown for three frequencies, 4kHz, 8kHz, and 12kHz. The measurement precision at 8kHz is shown for reference</td>
<td></td>
</tr>
<tr>
<td>3-5</td>
<td>ΔCp measurement versus dc bias voltage on a 10&quot; panel with &quot;Cs to next gate&quot; topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz</td>
<td></td>
</tr>
<tr>
<td>3-6</td>
<td>ΔGp measurement versus dc bias voltage on a 10&quot; panel with &quot;Cs to next gate&quot; topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz</td>
<td></td>
</tr>
<tr>
<td>3-7</td>
<td>ΔCs measurement versus dc bias voltage on a 10&quot; panel with &quot;Cs to next gate&quot; topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz</td>
<td></td>
</tr>
<tr>
<td>3-8</td>
<td>ΔGs measurement versus dc bias voltage on a 10&quot; panel with &quot;Cs to next gate&quot; topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz</td>
<td></td>
</tr>
</tbody>
</table>
3-9 Voltage waveforms for a TFT-addressed pixel. The solid line shows the voltage on the pixel pad, and the dashed line shows the voltage on the gate or scan line. Edata is the voltage placed on the drain line.

4-1 The circuit diagram used to characterize the transmission line behavior across gate, drain, and Cs lines.

4-2 Complex admittance diagram showing the effect on ΔCp and ΔGp from the transmission line phase shift of angle θ. Since the ideal pixel admittances are mostly capacitive, the phase shift will slightly decrease the measured ΔCp and will make a more pronounced increase in the measured ΔGp.

4-3 Circuit diagram for traditional transmission line. Equations (4.1) and (4.2) describe the voltage and current at the input to the line.

4-4 Circuit diagram for calculating the transmission line effect along the gate line.

4-5 Circuit diagram for calculating the transmission line effect along the drain line.

4-6 ΔCp measurements for row 240 on a LCD panel with Cs connected to the next gate line.

4-7 ΔGp measurements for row 240 on a LCD panel with Cs connected to the next gate line. A curve estimating the change in ΔGp across the row with the transmission line model is also shown.

4-8 ΔCp measurements for column 1 on a LCD panel with Cs connected to the next gate line.

4-9 ΔGp measurements for column 1 on a LCD panel with Cs connected to the next gate line. A curve estimating the change in ΔGp across the column with the transmission line model is also shown.

A2-1 Cross-sectional view of an amorphous silicon TFT with an inverted staggered structure.

A2-2 Top view of an amorphous silicon TFT with an inverted staggered structure.

A3-1 480x1920 TFT-LCD substrate with Cs storage capacitors connected to the next gate line. This substrate was used for all experimental measurements.
List of Tables

2-1 Effect of unprobed gate and drain lines for a Cs bus topology with M=480, N=1920, Cgs=0.05pF, Cgd=0.05pF, Ccsdl=0.03pF, Cs=0.5pF .......................... 42

2-2 Effect of unprobed gate and drain lines for a Cs to next gate line topology with M=480, N=1920, Cgs=0.05pF, Cgd=0.05pF, Cs=0.5pF ...................... 42

2-3 Effect of unprobed gate and drain lines for a no Cs topology with M=480, N=1920, Cgs=0.05pF, Cgd=0.05pF ................................................. 42

3-1 Measurements of a typical pixel (G2,D4) on a 10" LCD substrate with the "Cs connected to next gate" topology. The test conditions were Ftest=8kHz, acv=3.0Vpeak, TFT "off" bias=-5V, TFT "on" bias=+15V, and the unused gate and drain lines were all guarded. The mean and standard deviation were computed using 25 measurements ....................................... 49

3-2 Measurements of a typical pixel (G2,D4) on a 10" LCD substrate with Cs connected to next gate. The test conditions were Ftest=8kHz, acv=1.0Vpeak, TFT "off" bias=-5V, TFT "on" bias=+3V. The mean and standard deviation were computed using 25 measurements ........................................ 53

4-1 Series R and Shunt C for the transmission line models of the three LCD topologies ......................................................................................... 62

A3-1 Specifications for 10" TFT-LCD substrate used for experiments ............................. 76
Chapter 1

Introduction

Active-matrix liquid crystal displays (AM-LCDs) have become an attractive solution for applications where a thin profile, light weight, and low power are requirements. AM-LCDs have been targeted for laptop displays, automotive consoles, aircraft consoles, portable televisions, and others. Their success in penetrating these niche markets will largely determine whether they can supplant the CRT in television and HDTV applications in the future.

1.1 Liquid Crystal Cell Operation

AM-LCDs are the latest instance of flat panel displays made by sandwiching liquid crystal (LC) material between two glass plates. The development of room-temperature LC materials was critical to their use in displays. When LC materials are heated above their melting point, the molecules become rodlike. The class of liquid crystal materials most often used for LCDs is called cholesteric. The molecules of cholesteric liquid crystal stack in layers which have a twist and tilt giving the molecules a spiral configuration as shown in Figure 1-1. The structure of the LC molecules can be altered

---

by applying a controlled electric field across them so the LC material serves as a light switch.

The use of LC material in a display is shown in Figure 1-1. The liquid crystal material is sandwiched between two glass plates. Chemicals are used on each plate to orient the long axes of the LC molecules in one direction. The orientation of the LC molecules on the top is designed to form a 90 degree angle with the orientation of the bottom plate. Light polarizers are deposited on each glass plate to selectively pass light which is in the same direction as the LC molecules on the respective plate. With no dc voltage applied across the plates, Figure 1-1(a), the polarized light passing through the top plate is 90 degrees shifted by the twisted liquid crystal material and passes through the second polarizer. With dc bias voltage applied, Figure 1-1(b), the LC molecules line up with the electric field and do not rotate light, and the light is blocked by the bottom plate's polarizer. The intensity of light passing through the LC cell can be controlled by varying the voltage across the two plates.

Figure 1-1: Operation of the liquid crystal material in a LCD. (a) With no dc bias voltage across the LC material, the polarized light is rotated 90 degrees and is transmitted through the second polarizer. (b) With a sufficient dc bias voltage across the LC material, the polarized light is not rotated and is blocked by the second polarizer. (photo by Terry Scheffer, Tektronix, Inc. as it appeared in "Flat-panel Displays for Laptop Computers", Information Display, March 1989, p. 13.)
1.2 Liquid Crystal Display Types

The circuit designs for addressing the liquid pixel cells have been evolving ever since the light switching properties of LC material were first discovered. Liquid crystal material was first used in direct addressed LCDs found in watches and calculators. Later, LC material was considered for use as the light controlling element for pixels in flat panel displays. Because of the large number of pixels in a high information content display, a matrix addressing scheme was developed to replace the direct address method. Early flat panel displays used a passive addressing method with transparent conductive film to form the rows and columns. A potential between the row electrodes deposited on the top glass plate and the column electrodes on the bottom glass plate controlled the light transmission of each pixel. Due to problems in their response time, contrast ratio, and pixel cross-coupling, the passive LCDs have been replaced by active-matrix LCDs for high performance applications.

Active-matrix LCDs are expected to be the future for high information content flat panel displays. They use an active device to control the voltage at each LC cell. Unlike the passive matrix displays, the active device can maintain a voltage continuously across the LC cell, thus dramatically improving the display's contrast ratio and viewing angle. Various nonlinear devices, such as a MIM diodes, nonlinear resistors and thin-film transistors (TFTs) have been proposed as the controlling pixel element\(^3,4,5\). The TFT has become the most popular choice among active-matrix designs because it affords the superior display performance. Since the transfer admittance test technique is tailored for measuring active-matrix TFT-LCDs, this thesis will consider only TFT-LCD panel types.

---

1.3 TFT Active-Matrix Topologies

There are three dominant TFT active-matrix topologies. All topologies have the TFT gate terminal connected to the horizontal gate line, sometimes called the row or control line. The TFT drain terminal is connected to the drain line, sometimes called the column or data line. The TFT source terminal is connected to a pixel electrode. Because the TFT is a symmetrical device, sometimes the drain and source terminal names are switched. The first topology, shown in Figure 1-2, has a Cs storage capacitor connected from each pixel electrode to a common bus line. The Cs capacitor helps to maintain the charge on each pixel electrode while other rows in the display are being scanned. This is the most recent topology but is also the one with the highest defect probability because of its complexity.

The second topology is similar to the first, except it has its storage capacitors connected to the next gate line. This removes the need for the common bus line which is not present in this topology. The advantage is a simpler circuit with lower defect probabilities. However, this topology does allow the chance of crosstalk between a given pixel and the pixel to which its Cs is connected. A diagram for this topology is shown in Appendix 1.

The third topology is the oldest and least common of the three. It does not have a Cs capacitor, but instead relies on the capacitance of the liquid crystal material deposited atop the pixel electrode to maintain the pixel voltage level while other rows are being scanned. Because the liquid crystal capacitance is a nonlinear function of voltage and has significant leakage, this topology has difficulty providing uniform pixel charge storage.

As shown in Figure 1-2, most TFT-LCD topologies use a common "guard ring" to which each gate and drain line is connected through a resistance. The "guard ring" and resistors are necessary to protect the TFTs during manufacturing. To help the liquid
crystal adhere to the glass substrate, the substrate must go through a rubbing process. This process induces static charges on the substrate and could create very large potentials between gate and drain lines which could damage the TFTs if the "guard ring" with resistors were not used.

![Guard Ring Diagram](image)

Figure 1-2: 480x1920 TFT-LCD substrate with storage capacitors tied to a common Cs bus line.

### 1.4 Economics of Testing AM-TFT-LCDs

The development of AM-TFT-LCDs has been slowed by the difficulty in manufacturing defect-free displays. The complicated active-matrix addressing circuitry requires numerous processing steps each introducing the possibility of defects. Some of the more
common defects are opens in the gate or drain lines and shorts between TFT terminals and gate or drain lines caused by pinholes in insulation layers or contaminants. Figure 1-3 is a diagram of possible faults for a TFT-LCD with storage capacitors tied to a Cs common bus6.

The extremely low yields of perfect AM-TFT-LCDs can be appreciated by considering the size and tolerance requirements. For a conventional 640x480 pixel color laptop display, 921,600 pixels must be integrated on a glass substrate measuring 10" on the diagonal. One third of these pixels are used for each of the red, green, and blue colors to make the color display. The glass substrate must be extremely flat and smooth, the deposition masks must be precisely aligned, there must be very few dust particles in the clean room, and finally there must be virtually no defects for a functional display. These production difficulties will be exacerbated in the larger HDTV displays of the future.

To lower the costs of producing good AM-TFT-LCD panels, a test and repair strategy is being considered. Testing requires an efficient technique to detect, locate, and identify panel defects. The test information could then be passed to a repair station which could use metal film deposition equipment to repair open defects and laser cutting equipment to repair short defects. The benefits of such a strategy are twofold. LCDs which have many defects could be diagnosed and disposed of at an early production stage, thus saving the expense of further production stages. Secondly, panels with a small number of defects could be economically repaired.7,8 Clearly, finding a suitable test method to diagnose pixel defects is of paramount importance in the development of AM-TFT-LCDs.

6 H.P. Hall, "Identification of Faults on TFT-LCD Substrates Using Transfer Admittance Measurements", SID 1992 Digest, to be published.
Figure 1-3: Possible faults on a TFT-LCD substrate with storage capacitors tied to a Cs bus.

1.5 Other AM-TFT-LCD Test Methods

This thesis presents a test method for testing TFT-LCDs by employing transfer admittance measurements. The measurement theory and application to testing and characterizing these displays is explored in detail. Before beginning the discussion,

of the transfer admittance test technique, references to other test methods for diagnosing TFT-LCD defects are given.

R.L. Wisnieff et al. have developed a dc test method which charges a pixel's storage capacitor and then measures the charge with a sensitive current integrating circuit.\textsuperscript{13,14,15} F.J. Henley et al. have developed a voltage imaging method which uses the Pockel's effect to measure voltage differences at each pixel.\textsuperscript{16,17} L.H. Lin et al. have developed a method for testing the TFT array pattern by using optical spatial frequency filtering and laser holography.\textsuperscript{18}

\begin{itemize}
\item \textsuperscript{13} R.L. Wisnieff, L. Jenkins, R.J. Polastre, and R.R. Troutman, "In-Process Testing of Thin-Film Transistor Arrays", 1990 Society for Information Display, paper 11.2, pp 190-193.
\item \textsuperscript{15} R.R. Troutman, "Forecasting Array Yields for Large-Area TFT-LCDs", 1990 Society for Information Display, paper 11.4, pp. 197-200.
\item \textsuperscript{17} J.C. Speedy et al., "An In-Process Test System Using 'Voltage Imaging'", 1992 Society for Information Display, paper 21.4, to be published.
\end{itemize}
Chapter 2

Transfer Admittance Test Method

2.1 Review of Admittance and Impedance\textsuperscript{19}

To understand the theory of transfer admittance testing, a brief review of the definitions and equivalent circuits for admittance and impedance is required. Since the test method measures pixel capacitances and conductances, the impedance and admittance will be defined in terms of capacitance and resistance. Small inductances in the circuit can be ignored since the impedances are high and a low frequency is used. Impedance, $Z$, is defined as the complex ratio of ac voltage, $E_{ac}$, to ac current, $I_{ac}$, through a two-terminal network, as shown in Figure 2-1. The real part of impedance is the ac resistance, $R$, and the imaginary part is the reactance, $X$. Assuming the reactance is capacitive and a radian frequency, $\omega = 2\pi f$ frequency, $Z$ is defined by:

$$Z = R_{series} + jX_{series} = R_{series} + \frac{1}{j\omega C_{series}} \quad (2.1)$$

Since the impedance of elements connected in series are additive, the impedance can be modeled as an ideal resistor in series with an ideal capacitor as shown in Figure 2-2. The equivalent series parameters are denoted by the subscript 'series'.

\textsuperscript{19} "Series and Parallel Impedance Parameters and Equivalent Circuits", GenRad application note, Component Test Division.
Admittance, $Y$, is defined as the complex ratio of ac current to ac voltage across a two-terminal network, as shown in Figure 2-1. The real part is the ac conductance, $G$, and the imaginary part is the susceptance, $B$. Assuming the susceptance is capacitive, $Y$ is defined by:

$$Y = G_{\text{parallel}} + jB_{\text{parallel}} = G_{\text{parallel}} + j\omega C_{\text{parallel}}$$  \hspace{1cm} (2.2)

Since the admittances of elements connected in parallel are additive, the admittance can be modeled as an ideal conductance in parallel with an ideal capacitance as shown in Figure 2-2. The equivalent parallel parameters are denoted by the subscript 'parallel'.

![Figure 2-1: Measurement of impedance or admittance](image)

Either a series or parallel equivalent circuit completely describes the impedance or admittance between two points at any given frequency. The choice of the better equivalent circuit depends on the circuit to be modeled and the frequency range of interest. In measuring pixel admittances, for example, the pixel capacitance is in parallel with some conductance and these are in series with relatively low TFT channel resistance as shown in Figure 2-3. In this case the parallel equivalent circuit is useful for finding the pixel capacitance and conductance while the series equivalent circuit is more useful for finding the TFT channel resistance. Chapter 3 will explore in detail the use of parallel and series admittance parameters to find pixel characteristics. The equations for converting between the parallel and series equivalent circuits are given in (2.3) through (2.6). The dissipation factor, $D$, is also defined to simplify the equations. When no
subscript is used, the parallel model is assumed for admittances and the series model is assumed for impedances.

A transfer admittance is the ratio of any current to any voltage in a circuit. The transfer admittance method described herein refers to the more specific case where the current and voltage are referenced to a common terminal, the guard ring, as shown in Figure 2-3.

\[
R_{\text{series}} = \frac{1}{G_{\text{series}}}
\]

\[
C_{\text{series}} = \frac{1}{\omega R_{\text{parallel}} C_{\text{parallel}}}
\]

\[
C_{\text{series}} = \frac{1}{\omega R_{\text{parallel}} C_{\text{parallel}}}
\]

\[
R_{\text{series}} = \frac{D^2}{1 + D^2} R_{\text{parallel}}
\]

\[
G_{\text{series}} = \frac{1}{R_{\text{series}}} = \frac{1 + D^2}{D^2} G_{\text{parallel}}
\]

Figure 2-2: Two-terminal equivalent circuit models (a) Series equivalent circuit model (b) parallel equivalent circuit model.

\[
D = \omega R_{\text{series}} C_{\text{series}} = \frac{1}{\omega R_{\text{parallel}} C_{\text{parallel}}}
\]

\[
C_{\text{series}} = (1 + D^2) C_{\text{parallel}}
\]

\[
R_{\text{series}} = \frac{D^2}{1 + D^2} R_{\text{parallel}}
\]

\[
G_{\text{series}} = \frac{1}{R_{\text{series}}} = \frac{1 + D^2}{D^2} G_{\text{parallel}}
\]

Figure 2-3: Ideal transfer admittance test of an LCD substrate with a guard ring.
2.2 Summary of Transfer Admittance Test Technique\textsuperscript{20,21}

The test technique can determine pixel defects by measuring the admittances of each pixel. The main pixel admittances measured are the parasitic TFT gate-source capacitance, \( C_{gs} \), and the storage capacitor, \( C_s \). These pixel admittances are measured with a three-terminal connection using the substrate guard ring as a common point, as shown in Figure 2-4. Pixel defects are easily detected by noticing gross variations in the measured pixel admittances. For example, pixels with high conductances are likely to suffer from short defects, while pixels with zero admittance are likely to suffer from line opens. Since they are directly effected by pixel defects, the pixel admittances can be efficiently used to detect, locate, and identify the many types of open and short defects on LCD panels. The high precision and accuracy measurements of pixel admittances can also be useful in characterizing other phenomena affecting LCD behavior.

Figure 2-4 shows a pixel model for an AM-TFT-LCD pixel with a \( C_s \) storage capacitor tied to the next gate line. The sources used for ac testing and biasing the TFT are also shown. An admittance measurement is made by applying an ac test voltage to the two gate lines and measuring the resultant ac current in the drain line. The test technique requires two admittance measurements to be made, one with the TFT biased in its "on" state and one with the TFT biased in its "off" state. The "off" admittance, \( G_{off} + j\omega C_{off} \), is a measure of the crossover capacitance from the gate lines to the drain line. The measured "on" admittance, \( G_{on} + j\omega C_{on} \), is equal to the "off" admittance plus the admittance of the pixel capacitances, \( C_{gs} \) and \( C_s \). A third admittance, called a delta admittance, is calculated by taking the difference between "on" and "off" admittance measurements. This delta admittance, \( \Delta G + j\omega \Delta C \), is the most useful in detecting and

identifying defect pixels. In the ideal case of zero leakage across the pixel capacitors and ideal TFT switching, \(\Delta G=0\) and \(\Delta C=C_{gs}+C_{S}\), for a normal pixel. These ideal assumptions of zero conductance and ideal TFT switching will be relaxed in Chapter 3 where a more detailed analysis of pixel measurements is presented.

\[
C_{\text{off}} = C_{gd1} + C_{gd2} \\
C_{\text{on}} = C_{gd1} + C_{gd2} + C_{gs} + C_{S} \\
\Delta C = C_{gs} + C_{S}
\]

Figure 2-4: Transfer admittance test of a TFT-LCD substrate of type "Cs tied to next gate line"

The test connections for the three types of AM-TFT-LCD panels will differ slightly. The case of the \(C_{S}\) capacitor connected to the next gate line was just considered. The connections for a substrate with no \(C_{S}\) storage capacitors is shown in Figure 2-5. In this case a single ac source is used to stimulate the gate line. The delta measurement of \(\Delta C\) equals the pixel's \(C_{gs}\) capacitance in the ideal case.
\[ C_{\text{off}} = C_{\text{gd}} \]
\[ C_{\text{on}} = C_{\text{gd}} + C_{\text{gs}} \]
\[ \Delta C = C_{\text{gs}} \]

Figure 2-5: Transfer admittance test of a TFT-LCD substrate of type "no Cs capacitor"

The connections for a substrate with the Cs capacitor connected to a common Cs line is shown in Figure 2-6. In this case the Coff measurement will be very large because of the M crossings between the Cs bus line and the drain line. The capacitance at each of these Cs bus to drain line crossings is defined as Ccsdl, and the total measured Coff capacitance will be M*Ccsdl + Cgd. In some cases the size of the Coff capacitance forces the use of a smaller ac test voltage to keep the current detectors within their fixed range. The smaller ac test voltage will cause a proportional decrease in measurement precision. This potential problem has been solved by an "admittance subtractor" circuit which can inject a current of arbitrary magnitude and phase into the current detectors. By appropriate setting of the "admittance subtractor", the large Coff capacitance can be nulled. This allows the use of a larger test voltage to get improved precision in the delta admittance measurements.
2.3 Admittance Measurement and Calibration

A block diagram of the current detector is shown in Figure 2-7. The small currents are amplified by a high gain transresistance operational amplifier (OpAmp) followed by subsequent moderate gain filter stages. The amplified voltage is digitized with a high-accuracy sampling A/D converter. A multi-order analog low-pass filter is used to prevent aliasing of frequencies higher than the Nyquist sampling rate, and a multi-order high-pass filter is used to attenuate power line frequency noise at 60Hz.
The admittance measurement utilizes a DSP-based coherent monotone testing scheme\textsuperscript{22}. The ac voltage is measured by taking N' samples over M' cycles of the signal. If Fsamp is the converter sampling rate and Ftest is the monotone test frequency, then the fundamental requirement for coherence is shown in (2.7). If M' and N' are chosen to be relatively prime, then each sample is unique resulting in optimal information content from the samples and a reduction of the effects of harmonics.

\[
\frac{F_{\text{test}}}{F_{\text{samp}}} = \frac{M'}{N'} \tag{2.7}
\]

A DFT (Discrete Fourier Transform) algorithm is used to process the A/D converter samples in calculating the admittances. An efficient DFT algorithm, the Goertzel algorithm\textsuperscript{23}, is used to compute the M' th bin of the DFT in real time from the N' sample points. This FFT algorithm is preferable for measuring a single DFT bin because it is computationally fast and does not require extensive sine and cosine lookup tables. The real and imaginary parts of the DFT are used to compute the capacitance and conductance of the unknown. A calibration measurement of the standard resistance, Rs, is used as a reference in computing the unknown admittance. Equations (2.8) and (2.9)

\begin{thebibliography}{99}
\end{thebibliography}
give the formulae for computing the unknown admittance \((Gx + jBx)\) in terms of the standard admittance \((Gs + jBs)\), the measurement of the unknown admittance \((Gxm + jBxm)\), and the measurement of the standard admittance \((Gsm + jBsm)\), the calibration voltage \((Ecal)\), and the measurement voltage \((Emeas)\).

\[
Gx = \frac{Gs \left( \frac{Gxm + Bxm \cdot Bsm}{Gsm} \right) + Bs \left( \frac{Gxm \cdot Bsm}{Gsm} - Bxm \right)}{Emeas \cdot \frac{Ecal}{Gsm} \left( 1 + \frac{Bsm^2}{Gsm^2} \right)}
\]

(2.8)

\[
Bx = \frac{Gs \left( \frac{Bxm - Gxm \cdot Bsm}{Gsm} \right) + Bs \left( Gxm + \frac{Bxm \cdot Bsm}{Gsm} \right)}{Emeas \cdot \frac{Ecal}{Gsm} \left( 1 + \frac{Bsm^2}{Gsm^2} \right)}
\]

(2.9)

The calibration measurements are saved for each detector circuit. When measuring an unknown, the calibration measurements for that detector are used to compute the unknown admittance. By measuring and calibrating with the same circuit, any component errors in the detector circuitry will cancel in the above calculations. This allows relaxed tolerances on the detector circuitry while maintaining high measurement accuracy. Note that the calibration and measurement voltages can be different enabling each to be selected for high measurement precision.

A method to test for saturation of the individual current detectors has been implemented in software. The test is to check the magnitude of the real and imaginary parts computed from the DFT against a predetermined upper bound. The DFT magnitude at the edge of saturation is given by the upper bound in (2.10), where \(E_{fs}\) is the full scale voltage of the A/D converter and \(N'\) is the total number of samples. \(E_{magUB}\) is the Fourier transform of a sinusoid with \(E_{fs}\) height and windowed by a boxcar of \(N'\) samples. An input voltage which saturates the A/D converter will have a voltage magnitude which is necessarily larger than \(E_{magUB}\) and will approach the
voltage magnitude of a windowed square wave of height $E_{fs}$, shown in (2.11). The DSP software can check for A/D converter saturation by testing the voltage magnitude of any measurement against $E_{MagUB}$, or some percentage of $E_{MagUB}$ to account for possible noise in the input voltage. If the voltage magnitude is larger than $E_{MagUB}$, then the A/D converter is saturated.

$$E_{MagUB} = \frac{E_{fs} N'}{2}$$

(2.10)

$$E_{MagSW} = \frac{4}{\pi} E_{MagUB}$$

(2.11)

### 2.4 Measurement Precision and Digital Filtering of Noise

Measurements of pixel admittances must be made with sufficient precision to permit discernable differences in the measurements of good and defect pixels. Because of the very small admittance levels being measured ($< .05\text{pF}$ in some cases), the effects of noise on measurement precision must be considered. Most of the noise will result from noise at the input to the detector. Because the detector has very high gain to measure very low currents, any noise at the detector input will likewise be amplified by the high gain.

Any noise current at the input to the first stage will be amplified and will degrade measurement precision. The dominant input noise sources are Gaussian "white" noise in the OpAmp and the Gaussian "white" thermal noise of the $R_{prd}$ resistor connected across the detector input. The frequencies of interest are high enough that $1/f$ noise does not have a major noise contribution.
The method of modeling OpAmp noise as both current and voltage noise sources referenced at the OpAmp's inputs will be used. Figure 2-8 shows the current and voltage noise sources at the detector input. In and En are defined as the total input referred OpAmp current and voltage noises. These are found by multiplying the OpAmp's current and voltage noise spectral densities (NSD), expressed in pA and nV per root Hertz, by the square root of the circuit's equivalent noise power bandwidth, (ENBW). En,Rprd is the familiar Johnson or thermal noise of the Rprd resistor as shown in (2.12), where $k$ is the Boltzmann constant (1.38e-23 J/degK), T is temperature (degK), and BW is equal to the ENBW:

$$ En,Rprd = \sqrt{4(k)(T)(BW)(Rprd)} \quad (2.12) $$

If En and In are uncorrelated, then the error terms in the admittance measurement are as shown in (2.13). The $R_{prd}$ resistor, which is often integrated onto the LCD substrate for protection against static discharge, becomes a significant noise source. A graph of the total input referred noise current versus $R_{prd}$ is shown in Figure 2-9. The graph shows that the thermal noise of $R_{prd}$ dominates for $60\,\text{ohms} < R_{prd} < 20\,\text{kohms}$ and the transresistance amplifier's current noise dominates when $R_{prd}$ is larger. Because low operational amplifier voltage and current noise are opposing performance criteria in

---

OpAmp design, a choice of a low current or low voltage noise OpAmp may be beneficial depending on the size of Rprd.

\[
Y_{\text{meas}} \approx Y_x \left( \frac{R_{\text{prd}}}{R_{\text{prd}} + Z_{\text{in}}} \right) + \sqrt{\left( \frac{E_n}{E_x R_{\text{prd}}} \right)^2 + \left( \frac{I_n}{E_x R_{\text{prd}} + Z_{\text{in}}} \right)^2 + \left( \frac{\sqrt{4kT}}{E_x \sqrt{R_{\text{prd}}}} \right)^2} \sqrt{\text{ENBW}} \quad (2.13)
\]

![Figure 2-9: Detector input noise currents as a function of Rprd.](image)

An important function of the DFT is digital filtering of broadband noise. The DFT parameters set the equivalent noise power bandwidth (ENBW) defined above, assuming adequate low-pass filtering is used to reject noise above the Nyquist frequency. For a rectangular windowing function, the ENBW is defined in (2.14). This clearly
shows that improved measurement precision can be obtained by using a longer test time. The filter power magnitude response is shown in figure 2-10 for a 128-point DFT of 23 test cycles at 8000Hz test frequency. The graph shows that the digital filter has nulls at frequency multiples of \( F_{\text{test}}/M' \), except at the signal of interest, \( F_{\text{test}} \), where the magnitude response peaks. The ENBW is the power bandwidth which equals the area under the filter's power magnitude response shown in figure 2-10. It can be shown that the rectangular window used is the optimal window for minimizing white noise error because this window has minimal ENBW.  

\[
\text{ENBW} = \frac{F_{\text{test}}}{M'} = \frac{1}{\text{test time}} \tag{2.14}
\]

![Figure 2-10: The power magnitude response of the DFT filter with \( M' = 23 \) and \( N' = 128 \). The abscissa shows the DFT bin number. The 0th bin is dc while the 63rd bin is the Nyquist frequency.](image)

Equation (2.14) can be used to estimate a lower bound for the standard deviation of the admittance measurement. An example is a typical measurement condition of

$R_{prd} = 500\text{ohms}$, test time = 3msecs., $E_x = 1V_{rms}$, and $Z_{in} << R_{prd}$. For an LT1028\textsuperscript{27} low noise OpAmp, $E_n = 1nV/\text{rootHz}$, $I_n = 1pA/\text{rootHz}$. Figure 2-9 shows a total noise current of $6pA/\text{rootHz}$. From (2.14), the ENBW is 333Hz. Using these numbers, the rms error in admittance, which is equal to the standard deviation, is $G_{error} = 0.1nS$ and $C_{error} = 0.002pF$.

There are other noise sources in the measurement circuit which have been neglected because they have negligible contributions to the total noise. These include the noise in the TFT itself which is dominated by the shot noise, the source's voltage noise, the thermal noise from the gate and drain line resistances which will rms add to the source's voltage noise, and electromagnetic interference noise which may couple into the detector through the gate or drain cables. The source's equivalent voltage noise sources are negligible when a very low admittance is being measured since the noise current through the test admittance will be so small. However, these source voltage noises may become important when a large off admittance is measured. For instance a panel with the Cs bus connection has a large $C_{off}$ and therefore will be more susceptible to source voltage noises than other topologies.

2.5 Varying Measurement Test Conditions

The conditions of test frequency, ac test voltage, and dc bias voltage can be adjusted to optimize the measurement of various panel parameters. The test frequency can be adjusted to reduce or accentuate the transmission line behavior across the gate and drain lines of the LCD panel. Lower frequencies reduce the transmission line effect and permit more accurate measurements of the pixel capacitances. Higher frequency measurements accentuate the transmission line effect which can be used to quantify the propagation

\textsuperscript{27} Linear Technology 1990 Databook, p. 2-162.
delay of signals across the drain or gate lines during operation. These transmission line
effect issues will be explored in more detail in Chapter 4.

The dc bias voltage can be adjusted to measure the pixel capacitances at various
degrees of TFT turn on. A dc bias voltage test can be used to determine the TFT
threshold voltages. The TFT threshold voltage is important because large variations in it
may cause poor LCD performance.

The test voltage level can be increased to improve the measurement precision.
Equation (2.13) shows that the "white" noise admittance terms can be reduced by
increasing $E_{\text{test}}$. The size of $E_{\text{test}}$ is somewhat limited for the $C_s$ common LCD panel
type because a large $C_{\text{off}}$ capacitance results from the many crossovers between the $C_s$
bus and each drain line. Although each crossover capacitance is small (< .03pF), there
are typically 480 crossings resulting in a total measured $C_{\text{off}}$ capacitance exceeding
14pF. This $C_{\text{off}}$ takes up almost 98% of the A/D converter's dynamic range for typical
pixel capacitances of 0.3pF. The "admittance subtractor" method, which introduces a
"bucking" current of arbitrary magnitude and phase, can be used to subtract this large
$C_{\text{off}}$ capacitance and allow higher test voltages.

2.6 Effect of LCD Substrate Parameters

The admittance measurements will depend on the LCD substrate's design parameters and
on the imperfections in the test connections. Differences in panel design and connections
must therefore be considered when interpreting the measurements. This chapter will
analyze the important substrate and connection effects and will present formulae for
predicting the effects.

Figure 2-11 shows the various substrate parameters which may influence the
admittance measurements. The values of $C_{\text{gs}}$, $C_s$, and $C_{\text{csdl}}$ will have a direct effect on
the measured $C_{\text{off}}$ and $\Delta C$ as was shown in Chapter 3. The effect of line resistance was
quantified in the transmission line effect discussion in Chapter 4. The values of Rprg, Rprd, and Rcsr will also influence the admittance test.

2.6.1 Rprg value

Rprg is the resistance between the gate probe pad and the guard ring. The value of Rprg must be large enough to allow the current-limited voltage sources to drive the gate line without distortion. A large current will flow through a low Rprg and must return to the source through the guard ring. This creates voltage drops along the gate guard ring which may stimulate other gate lines.

The combination of Rprg and the gate pad contact resistance, Rgcnt, may cause a voltage divider error thus reducing both the ac and dc voltage stimulating the gate line:

Figure 2-11: Substrate connections which may affect the measurement accuracy and precision.
The attenuated ac or dc voltage will result in an accuracy error in all admittance measurements. Perhaps more important than this is a variation in either Rgcnt or Rprg which will cause a relative error in measurements on different gate lines. The variation error between pixels of different gate lines must be included in the pixel measurement precision in determining the ability to detect faults.

Rprg is also necessary in guarding the gate lines when the distributed return connection is not used. This guarding effect and the potential errors caused by improper guarding will be examined in Section 2.8.

### 2.6.2 Rcsr value

Rcsr is the resistance between the Cs bus pad and the guard ring. The effect of Rcsr is similar to that of Rprg; its value must be large enough to allow the source to drive it and to reduce the voltage attenuation error due to the Cs bus pad contact resistance. In the case where there are multiple Cs bus pads, the Rcsr resistance is the value of the Cs bus-to-pad resistance of a single pad divided by the number of pads.

### 2.6.3 Rprd value

Rprd is the resistance between the drain pad and the guard ring. The Rprd value will influence three separate effects. First, there will be a current division error due to the finite input impedance of the current detector. Variations in the Rprd value or in the drain pad contact resistance, Rdcnt, or the detector input impedance, Zdet, will cause measurement errors between drain lines as shown in (2.15). The error from Zdet is eliminated by using a calibration procedure. The drain pad contact resistance error will be constant for all measurements on the same column of the display. For this reason and
because all column measurements are made with the same processor, good and bad pixels are diagnosed along a column.

Secondly, the Rprd values must be sufficiently low to guard the drain lines not being detected. An explanation of this error is given in Section 2.8. Thirdly, the Rprd will contribute to the white noise errors at the detector input. As was described in Section 2.3, Rprd causes both a thermal noise error term and a current noise error term at the input of the transresistance amplifier. Figure 2-9 showed the total input referred noise as a function of the Rprd value.

\[
\text{Drain errors} = \frac{-(R\text{dct} + Z\text{det})}{R\text{prd} + R\text{dct} + Z\text{det}} \times 100\% \quad (2.15)
\]

2.7 Measurement Connections Errors

A simplification of the test connections circuit diagram was shown in Figure 2-3. The pixel admittance is measured by the ratio of detected current, \(I_{\text{det}}\), to the source voltage, \(E_{\text{test}}\). Here, all components, sources, and detectors are assumed to be ideal. The source has zero output impedance, the detector has zero input impedance, substrate probe connections have zero contact resistance, and the gate line, drain line, and guard ring all have zero resistance. The source return and detector ground are connected and are each tied to the guard ring. With these simplifications the measured admittance is identical to the desired pixel admittance, \(Y_x\), as shown in (2.16).

\[
Y_{\text{meas}} = \frac{I_{\text{meas}}}{E_{\text{test}}} = Y_x \quad (2.16)
\]

In practice the line resistance, source and detector impedances, and probe resistances must be considered. The non-ideal test connections to the substrate are shown in Figure 2-12. A \(\Delta-Y\) transformation\(^{28}\) is used to simplify the analysis and the resulting

\(^{28}\) "Electric Circuits: A First Course in Circuit Analysis for Electrical Engineers", MIT electrical engineering staff, 1943, pp. 146-150.
circuit is shown in Figure 2-13. The grounding of the source and detector will have an important effect on measurement accuracy. The simplest grounding scheme, but one which introduces a large error term, is to connect the source return and the detector ground. This topology is called a "three-terminal, single-guard" measurement. If the error terms are small, the measured admittance can be expressed as:

\[
Y_{m} = \frac{I_{\text{meas}}}{E_{\text{test}}} = Y_{x} \left[ 1 - (R_{s} + R_{d})Y_{x} - \frac{R_{s}'}{R_{\text{prg}}} - \frac{R_{d}'}{R_{\text{prd}}} + \frac{R_{c}}{Y_{x}R_{\text{prg}}R_{\text{prd}}} \right] \tag{2.17}
\]

where:

\[
R_{c} = \frac{R_{\text{rtn.probe}} - R_{\text{gnd.probe}}}{R_{\text{gr}}} \tag{2.18}
\]

The last term is an error due to resistance in the single guard lead. Using typical numbers, \( F_{\text{test}} = 8000 \text{Hz}, \) \( R_{\text{rtn.probe}} = 3 \text{ohms}, \) \( R_{\text{gnd.probe}} = 3 \text{ohms}, \) \( Z_{x} = 1 = (2\pi 8000)(15 \text{pF}), \) \( R_{\text{gr}} = 100, \) \( R_{\text{prg}} = 500 \text{W}, \) \( R_{\text{prd}} = 500 \text{W}, \) the error term results in a -48% error in impedance.

The problematic guard lead error term in (2.17) can be avoided with the use of a double guarded measurement as shown in Figure 5-4. This requires a "floating" source whose return connection is isolated from the detector's ground point. The "floating" source gives a "three-terminal, double guard" measurement. Now the measured impedance has the small error terms shown in (2.19)

\[
Y_{m} = \frac{I_{\text{meas}}}{E_{\text{test}}} = Y_{x} \left[ 1 - (R_{s} + R_{d})Y_{x} - \frac{R_{s}'}{R_{\text{prg}}} - \frac{R_{d}'}{R_{\text{prd}}} - R_{\text{gr}}Y_{x} \right] \tag{2.19}
\]

The "three-terminal, double guard" measurement is the preferred method of testing TFT-LCD substrates with a guard ring, when the \( R_{\text{prg}} \) and \( R_{\text{prd}} \) resistors are relatively low. When \( R_{\text{prg}} \) and \( R_{\text{prd}} \) are very high, the source return must be connected to the detector.

---

29 "Multi-terminal Impedance Measurements, or... Why Do Those New Bridges Use So Many Connections?", GenRad application note, Component Test Division.

30 Ibid.
ground to provide a return path for the current. In this case the guard lead error term is very small.

\[ Y_x = \frac{I_{det}}{E_{ac}} \]

\[ R_{s'} = R_{source} + R_{source.probe} \]

\[ R_{d'} = Z_{det} + R_{det.probe} \]

Figure 2-12: Three-terminal, single guard TFT-LCD substrate measurement connections

Assuming:
\[ R_{rtn.probe} \ll R_{gr} \]
\[ R_{gnd.probe} \ll R_{gr} \]
\[ R_{prg} \approx R_{prg} \]
\[ R_{prd} \approx R_{prd} \]
\[ R_{c} \approx \frac{R_{rtn.probe} R_{gnd.probe}}{R_{gr}} \]

Figure 2-13: Three-terminal, single guard simplified circuit diagram.
2.8 Guarding of Inactive Gate and Drain Lines

The accurate measurement of the pixel admittances embedded in a matrix of lines requires proper guarding of the unused lines. In this discussion the inactive lines refer to all lines other than the single gate line being stimulated and the drain lines whose currents are being detected. Every gate and drain line crossing in the matrix has some capacitance. These capacitances can provide alternate paths for the test current to flow from the source to the detector. To break these alternate current paths, guarding by connecting the unused gate lines to the source return and the unused drain lines to the detector ground can be very effective.

When the substrate being tested has a guard ring with low-valued Rprg and Rprd resistors, the matrix can be adequately guarded by probing the guard ring in several places. Probes along the gate side of the guard ring should be connected to signal return and probes on the drain sides of the guard ring should be connected to detector ground. This will maintain the preferred "three-terminal, double guard" measurement topology.

In cases where there is no guard ring or the Rpr resistors are very high, proper guarding is done by probing the unused gate and drain lines. In this case both the unused
gate probes and the unused drain probes should be connected to the source return to provide a direct path for the current from the alternate paths to return to the source. If the drain probes were grounded, the current in these probes would return through the guard ring and may cause measurement errors if they cause significant voltage drops in the guard ring.

In some cases it is impractical to probe all of the gate and drain lines. Unprobed lines will be left unguarded and may cause measurement errors. Figure 2-15 shows the circuit diagram for the case where some of the gate and drain lines are left unguarded. In this diagram, N is the total number of drain lines, n is the number of probed drain lines, M is the total number of gate lines, and m is the number of probed gate lines. Cx is the capacitance between the gate line and drain line being tested and will be different for the TFT "off" and "on" measurements. In the case where a Cs storage capacitor is connected to a Cs bus or to an adjacent gate line, Cx also includes the capacitance from the extra gate or Cs bus line to the drain line being tested.

The case of infinite Rprd and Rprg is considered here because it causes the largest guarding errors and also simplifies the analysis. Since the probed gate and drain lines are connected to signal return or detector ground, their resistances are ideally zero. The effect of resistance in the gate and drain lines has little effect on the results, and therefore Rgl and Rdl will be assumed to be zero. With these assumptions, the measured capacitance will be:

\[
C_m = C_x + \frac{(N-n) (M-m) \ C_{gd} C_x}{n (M-m) \ C_{gd} + N (C_x + (m-1) \ C_{gd})}
\]

The second term in this equation is the error in the measurement due to improper guarding. Tables 2-1 to 2-3 show the errors in Coff, Con, and ΔCp for different numbers of unprobed gate and drain lines for the three different LCD substrate topologies. The error tables show that it is always preferable to measure with all of the gate and drain
lines probed and guarded. The near zero ΔC_p error with m=1 and n=1 shown in table 5-1 results from the high C_x capacitance for both on and off measurements. This example of an unguarded measurement is not preferred because of the large errors in the C_off and C_on measurements.

![Circuit diagram of the LCD active matrix with some gate and drain lines left unguarded. This diagram shows the alternate current paths through the line crossing capacitances in the LCD matrix.](image)

**Figure 2-15:** Circuit diagram of the LCD active matrix with some gate and drain lines left unguarded. This diagram shows the alternate current paths through the line crossing capacitances in the LCD matrix.

<table>
<thead>
<tr>
<th>m</th>
<th>n</th>
<th>C_off Error (pF)</th>
<th>C_on Error (pF)</th>
<th>ΔC_p Error (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>23.92</td>
<td>23.92</td>
<td>0.001</td>
</tr>
<tr>
<td>120</td>
<td>480</td>
<td>7.82</td>
<td>7.93</td>
<td>0.11</td>
</tr>
<tr>
<td>240</td>
<td>960</td>
<td>2.67</td>
<td>2.72</td>
<td>0.05</td>
</tr>
<tr>
<td>360</td>
<td>1440</td>
<td>0.59</td>
<td>0.60</td>
<td>0.01</td>
</tr>
<tr>
<td>480</td>
<td>1920</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

**Table 2-1:** Effect of unprobed gate and drain lines for a Cs bus topology with M=480, N=1920, Cgs=0.05pF, Cgd=0.05pF, Ccsd=0.03pF, Cs=0.5pF.
Table 2-2: Effect of unprobed gate and drain lines for a Cs to next gate line topology with M=480, N=1920, Cgs=0.05pF, Cgd=0.05pF, Cs=0.5pF.

<table>
<thead>
<tr>
<th>m</th>
<th>n</th>
<th>Coff Error (pF)</th>
<th>Con Error (pF)</th>
<th>ΔCp Error (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>21.28</td>
<td>23.45</td>
<td>2.17</td>
</tr>
<tr>
<td>120</td>
<td>480</td>
<td>0.128</td>
<td>0.733</td>
<td>0.605</td>
</tr>
<tr>
<td>240</td>
<td>960</td>
<td>0.033</td>
<td>0.194</td>
<td>0.161</td>
</tr>
<tr>
<td>360</td>
<td>1440</td>
<td>0.007</td>
<td>0.039</td>
<td>0.032</td>
</tr>
<tr>
<td>480</td>
<td>1920</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

Table 2-3: Effect of unprobed gate and drain lines for a no Cs topology with M=480, N=1920, Cgs=0.05pF, Cgd=0.05pF, Cs=0.5pF.

<table>
<thead>
<tr>
<th>m</th>
<th>n</th>
<th>Coff Error (pF)</th>
<th>Con Error (pS)</th>
<th>ΔCp Error (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>19.15</td>
<td>21.28</td>
<td>2.13</td>
</tr>
<tr>
<td>120</td>
<td>480</td>
<td>0.064</td>
<td>0.128</td>
<td>0.064</td>
</tr>
<tr>
<td>240</td>
<td>960</td>
<td>0.017</td>
<td>0.033</td>
<td>0.016</td>
</tr>
<tr>
<td>360</td>
<td>1440</td>
<td>0.003</td>
<td>0.007</td>
<td>0.004</td>
</tr>
<tr>
<td>480</td>
<td>1920</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>
Chapter 3

Pixel Model for LCD Testing

This chapter introduces an equivalent pixel model used to interpret the transfer admittance measurements. The model will show that the parallel delta admittances, $\Delta C_p$ and $\Delta G_p$, and the series delta admittances, $\Delta C_s$ and $\Delta G_s$, can be used to detect pixel faults and to characterize individual pixels. To a first approximation the delta admittance measurements are only effected by the components of a single pixel. This model assumes that the line resistances and shunt capacitances are small and have negligible effect on the measurements. Chapter 4 will present a transmission line model which quantify the effect of these line resistances and shunt capacitances.

Experiments made on a 10" LCD substrate will be used to show the validity of the pixel model. Refer to Appendix 1 for more information on the 10" LCD substrate used in these experiments.

3.1 Equivalent Pixel Model for AM-TFT-LCD Pixels

Figure 3-1 shows an equivalent pixel model for the AMLCD topology with Cs connected to a common Cs bus. This topology was chosen for discussion because it shows the clear advantage in measuring with parallel admittances. To isolate each pixel, the measurements of $C_{off}$, $G_{off}$, $C_{on}$, and $G_{on}$ should be made using a parallel equivalent circuit model. Then, the computed delta admittances, $\Delta C_p$ and $\Delta G_p$, will cancel the
parallel shunt admittances, most notably the large $M \times C_{csdl}$ capacitance, and will be a measure of the reduced pixel model shown in Figure 3-2. The delta admittances, $\Delta C_p$ and $\Delta G_p$, are also parallel measurements since they are the differences of parallel measurements. The "off" leakage terms, $G_{gd}$ and $M \times G_{csdl}$, will not affect the delta admittances unless they are large enough to saturate the detector. The reduced pixel model in figure 3-2, with the "Cs line" relabeled as the "next gate line", is also an accurate model for the Cs to next gate line LCD topology.

Figure 3-1: Equivalent circuit model for TFT "off" and "on" measurements with a Cs common bus topology.

Figure 3-2: Equivalent circuit model for delta admittance measurements with a Cs common bus topology.
3.2 Parallel Admittance Measurements

The parallel admittances which are computed from the reduced pixel model are defined in (3.1) and (3.2) with \( \omega = 2\pi f_{\text{test}} \). \( \Delta C_p \) is equal to the pixel capacitance, \( C_{\text{pixel}} \), when the TFT conductance, \( G_{\text{tft}} \), is much larger than the pixel leakage conductance, \( G_{\text{pixel}} \), and the pixel admittance, \( \omega C_{\text{pixel}} \). Since normal pixels have very low leakage, the requirement for adequately measuring \( C_{\text{pixel}} \) is sufficient dc bias voltage to make \( G_{\text{tft}} \) much larger than \( \omega C_{\text{pixel}} \). \( \Delta G_p \) is a useful measure of the leakage resistance across either the \( C_{\text{gs}} \) or \( C_{\text{s}} \) capacitances. Leakage conductance is important because it can result in decay of the pixel electrode voltage during the scan cycle causing poor image quality. In the extreme case where the leakage conductance, \( G_{\text{pixel}} \), is greater than \( G_{\text{tft}} \), the \( \Delta G_p \) measurement approaches \( G_{\text{tft}} \) and the fault is easily detected.

\[
\Delta C_p = C_{\text{pixel}} \frac{G_{\text{tft}}^2}{(G_{\text{tft}} + G_{\text{pixel}})^2 + (\omega C_{\text{pixel}})^2} \tag{3.1}
\]

\[
\Delta G_p = G_{\text{tft}} \frac{G_{\text{pixel}} (G_{\text{tft}} + G_{\text{pixel}}) + (\omega C_{\text{pixel}})^2}{(G_{\text{tft}} + G_{\text{pixel}})^2 + (\omega C_{\text{pixel}})^2} \tag{3.2}
\]

To be useful the admittance measurements must have adequate precision to be able to detect leakages. The precision of the \( \Delta C_p \) and \( \Delta G_p \) measurements when using a 1.0V\text{ac} test voltage, an 8kHz test frequency, and a 10msec. measurement time for both "off" and "on" measurements were found to be about 0.002pF and 0.1nS standard deviation, respectively. To show the effects of pixel leakage and TFT conductance on the measured values of \( \Delta C_p \) and \( \Delta G_p \), simulations are shown in figure 3-3 and figure 3-4, respectively. A typical value of \( C_{\text{pixel}}=0.5\text{pF} \) is used for this simulation and three different test frequencies, 4kHz, 8kHz, and 12kHz are considered. For reference the precision of the \( \Delta C_p \) and \( \Delta G_p \) measurements at 8kHz are shown.
Figure 3-3 shows the effect of pixel leakage conductance, \( G_{\text{pixel}} \), on \( \Delta G_p \) assuming a TFT "on" conductance \( G_{\text{tft}} = 100 \text{nS} \). When there is very low leakage, the \( \Delta G_p \) measurement equals \( \Delta G_p, \text{min} \) shown in (3.3). When \( G_{\text{pixel}} \) becomes larger than the admittance of \( C_{\text{pixel}} \), \( \Delta G_p \) is approximately equal to \( G_{\text{pixel}} \). However, when the leakage conductance is larger than the \( \omega C_{\text{pixel}} \) admittance, \( \Delta G_p \) approaches the TFT on conductance, \( G_{\text{tft}} \). When the leakage conductance is larger than the \( \Delta G_p \) measurement precision, the leakage fault can easily be detected. The minimum measurable leakage at \( f_t = 8 \text{kHz} \) and 10msec. test time is \( 0.1 \text{nS} \), or 10Gohm. The detectability of leakage improves with lower test frequencies and increased test time.

Figure 3-4 shows the effect of TFT "on" conductance on \( \Delta G_p \) assuming no pixel leakage, \( G_{\text{pixel}} = 0 \text{nS} \). At \( G_{\text{tft}} = 100 \text{nS} \), \( \Delta C_p \) approximately equals \( C_{\text{pixel}} \) at all test frequencies and \( \Delta G_p \) equals \( \Delta G_p, \text{min} \) defined in (3.3).

\[
\Delta G_p, \text{min} = \frac{(\omega C_{\text{pixel}})^2}{G_{\text{tft}}} \tag{3.3}
\]

Table 3-1 shows pixel measurements on the 10" LCD panel with the "Cs connected to the next gate line" topology. The standard deviation of \( \Delta C_p \) and \( \Delta G_p \), 0.0009pF and 0.047nS respectively, shows excellent measurement precision. Gaussian probability theory says that occurrences of Gaussian random process will be within \( +/- 5 \) standard deviations of the process' mean value with a probability in excess of 1 in a million. Assuming the measurements pixel admittances are also a Gaussian random process and assuming all pixels on a panel have the same delta admittances, one can conjecture that measurements of all pixels on a 10" panel, about one million pixels, could detect pixel admittances outside a bound of \( +/- 4.5 \text{fF} \) and 0.23nS. Faults which cause the pixel admittances to be outside these bounds would all be detected. The standard deviation for individual measurements can be even lower if a higher ac test voltage is used or if a longer measurement time is taken. For example, the same pixel
Figure 3-3: Simulated effect of pixel leakage conductance, \( G_{\text{pixel}} \), on the measured value of \( \Delta G_p \). Curves for measured \( \Delta G_p \) versus \( G_{\text{pixel}} \) are shown for three frequencies, 4kHz, 8kHz, and 12kHz. The measurement precision at 8kHz is shown for reference.

Figure 3-4: Simulated effect of TFT on conductance, \( G_{\text{tft}} \), on the measured value of \( \Delta G_p \). Curves for measured \( \Delta G_p \) versus \( G_{\text{pixel}} \) are shown for three frequencies, 4kHz, 8kHz, and 12kHz. The measurement precision at 8kHz is shown for reference.
measurements in Table 3-1 would have a standard deviation of about +/- 0.45fF and 23pS if a full second were taken for the pixel measurement.

The measurement of Cgs, found by applying the ac voltage on the gate line only, was found to be 0.1pF. This is about twice the designed value for Cgs which was 0.05pF (see Appendix 1 for the panel specifications). This discrepancy is due to the definition of the Cgs capacitance. The manufacturer defines Cgs as the capacitance from the gate line to half of the TFT drain-to-source channel. Since the measurement of Cgs will include the entire channel capacitance, the measured value should be about twice the designed value. Because the feedthrough voltage error which results from a large Cgs will be effected by the capacitance to the entire channel, it seems reasonable that the measured Cgs value should be used.

<table>
<thead>
<tr>
<th></th>
<th>Coff (pF)</th>
<th>Goff (nS)</th>
<th>ΔCp (pF)</th>
<th>ΔGp (nS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>both</td>
<td>mean</td>
<td>0.3980</td>
<td>1.8731</td>
<td>0.5019</td>
</tr>
<tr>
<td></td>
<td>std</td>
<td>0.0003</td>
<td>0.0380</td>
<td>0.0009</td>
</tr>
<tr>
<td>gate only</td>
<td>mean</td>
<td>0.1877</td>
<td>0.8436</td>
<td>0.1114</td>
</tr>
<tr>
<td></td>
<td>std</td>
<td>0.0004</td>
<td>0.0300</td>
<td>0.0007</td>
</tr>
<tr>
<td>next gate only</td>
<td>mean</td>
<td>0.2099</td>
<td>0.9805</td>
<td>0.3914</td>
</tr>
<tr>
<td></td>
<td>std</td>
<td>0.0006</td>
<td>0.0141</td>
<td>0.0013</td>
</tr>
</tbody>
</table>

Table 3-1: Measurements of a typical pixel (G2,D4) on a 10” LCD substrate with the "Cs connected to next gate" topology. The test conditions were Ftest=8kHz, acv=3.0Vpeak, TFT "off" bias=-5V, TFT "on" bias=+15V, and the unused gate and drain lines were all guarded. The mean and standard deviation were computed using 25 measurements.

The measurement of Cs, found by applying the ac voltage to the next gate only, was found to be 0.4pF. This is smaller than the 0.5pF storage capacitance specified by the manufacturer. There is no apparent explanation for this discrepancy. Measurements

---

31 R. Bruce et al, "Polysilicon: the Next Wave for TFTs?", Information Display, p. 16.
presented in the next chapter show that the measured Cs value was the same for all pixels on the panel and at different frequencies. Further information, which is not currently available, about the manufacturer's calculate of Cs may explain the apparent discrepancy.

The ΔGp measurements in table 3-1 are also consistent with the pixel model and the simulation in figure 3-5. The ΔGp measurement with acv on the gate only is the smallest of the three acv measurements because Cpixel is smallest. The sum of the ΔGp measurements with acv on gate only and next gate only approximately equals the ΔGp with acv on both, as expected from (3.2) when Gtft is much larger than ωCpixel.

Measurements of typical pixels versus dc bias voltage and at different frequencies are shown in figure 3-5 for ΔCp and figure 3-6 for ΔGp. From equation (3.2) if Gpixel=0, ΔGp peaks and ΔCp equals half of Cpixel when the admittance of the TFT conductance equals the admittance of the pixel capacitance, ωCpixel. The TFT conductance at various dc bias voltages can be found from figure 3-5. Gtft will be half the Cpixel admittance when the ΔGp curve is at a maximum. Therefore, Gtft is about 13nS at 1.6V (from the 4kHz curve), 25nS at 2.1V (from the 8kHz curve), and 38nS at 2.6V (from the 12kHz curve). Note that series delta conductance, ΔGs, is equal to Gtft as will be shown in the next section.

The ΔCp curves at higher frequencies reach the final Cpixel capacitance at a higher dc bias voltage. The ΔGp curves at higher frequencies have a higher peak value and the peak value occurs at a higher dc bias voltage. The ΔCp measurement approaches the pixel capacitance as the TFT conductance increases. Note that the measurements of ΔCp are relatively constant for dc voltages of 13V or higher. For this reason 15V is normally used to bias the transistor during the TFT "on" measurement so that the acv modulation of the TFT conductance will not affect the ΔCp
Figure 3-5: ΔCp measurement versus dc bias voltage on a 10" panel with "Cs to next gate" topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz.

Figure 3-6: ΔGp measurement versus dc bias voltage on a 10" panel with "Cs to next gate" topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz.
measurements. The dc voltage at which $\Delta G_p$ peaks will be an important consideration in the next section where high precision $\Delta G$s measurements are derived in part from the $\Delta G_p$ measurement.

### 3.3 Series Admittances to Measure TFT On Conductance

Using a series equivalent circuit to measure the pixel admittances can be very useful if there is no pixel leakage. Series difference admittances, $\Delta C$s and $\Delta G$s, of the reduced pixel model in Figure 3-2 can be computed from the parallel difference admittances. This can be done using the traditional parallel to series admittance conversion formulae previously given in equations (2.4) and (2.6). $\Delta G$s is a good measure of the TFT on conductance and is useful in determining the pixel's turn on capability. The measurement of TFT on resistance is important to ensure that pixel write time is sufficient to fully charge the pixel storage capacitor through the TFT on resistance. For a normal pixel with no leakage, $G_{pixel}=0$, $\Delta G$s in equation (3.5) exactly equals $G_{tft}$ and $\Delta C$s in equation (3.4) exactly equals $C_{pixel}$.

\[
\Delta C_s = C_{pixel} + \frac{G_{pixel}^2}{\omega^2 C_{pixel}} \quad (3.4)
\]

\[
\Delta G_s = G_{tft} \frac{G_{pixel}^2 + (\omega C_{pixel})^2}{G_{pixel} (G_{tft} + G_{pixel}) + (\omega C_{pixel})^2} \quad (3.5)
\]

Table 3-2 shows measurements of parallel and series delta admittances on a 10" LCD panel with the Cs connected to the next gate line. The measurement with ac on both the gate and the next gate shows a TFT conductance of 43.9nS or 22.8Mohms at 3V bias.

Experimental data showing the transfer admittance measurements of a "good" pixel with no pixel leakage values are shown in Figure 5 and Figure 6. The $\Delta G$s
measurement shows the TFT channel resistance as a function of the dc bias voltage. The
ΔCs measurement is closely equal to the pixel capacitance, C_pixel, except at very low dc bias voltages where the TFT is off.

<table>
<thead>
<tr>
<th>ac voltage</th>
<th>ΔCp (pF)</th>
<th>ΔGs (nS)</th>
<th>ΔCs (pF)</th>
<th>ΔGs (nS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>both</td>
<td>mean</td>
<td>0.3713</td>
<td>10.4026</td>
<td>0.4866</td>
</tr>
<tr>
<td>std</td>
<td>0.0017</td>
<td>0.0977</td>
<td>0.0018</td>
<td>0.5</td>
</tr>
<tr>
<td>gate only</td>
<td>mean</td>
<td>0.0888</td>
<td>1.3024</td>
<td>0.0964</td>
</tr>
<tr>
<td>std</td>
<td>0.0019</td>
<td>0.0887</td>
<td>0.0021</td>
<td>1.1</td>
</tr>
<tr>
<td>next gate only</td>
<td>mean</td>
<td>0.2838</td>
<td>9.3522</td>
<td>0.4058</td>
</tr>
<tr>
<td>std</td>
<td>0.0020</td>
<td>0.0966</td>
<td>0.0025</td>
<td>0.4</td>
</tr>
</tbody>
</table>

Table 3-2: Measurements of a typical pixel (G2,D4) on a 10" LCD substrate with Cs connected to next gate. The test conditions were Ftest=8kHz, acv=1.0Vpeak, TFT "off" bias=-5V, TFT "on" bias=+3V. The mean and standard deviation were computed using 25 measurements.

The precision of the ΔGs measurement depends to a large extent on the value of ΔGp from which it is calculated. Figure 3-8 shows that the ΔGs measurement is very precise at low dc bias voltages but becomes unpredictable at dc bias voltages above 10V. The sensitivity of ΔGs to changes in ΔGp can be expressed by taking the partial derivative of ΔGs in (3.5) with respect to ΔGp and is shown in (3.6). Clearly, the sensitivity is a minimum when ΔGp equals 2π freq ΔCp which from the above discussion occurs when ΔGp is a maximum. (Note: This is a minimum because the second partial derivative of (3.5) is negative). Therefore, the best precision in ΔGs is obtained by measuring at a low dc bias voltage where ΔGp is a maximum. However, measuring at a lower dc voltage than used for the normal parallel admittance testing requires a separate measurement which would almost double the test time of a complete panel if testing the ΔGs of all pixels is required. As a compromise, an intermediate dc bias voltage of about...
Figure 3-7: $\Delta C_s$ measurement versus dc bias voltage on a 10" panel with "Cs to next gate" topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz.

Figure 3-8: $\Delta G_s$ measurement versus dc bias voltage on a 10" panel with "Cs to next gate" topology. Measurements were made at three frequencies, 4kHz, 8kHz, and 12kHz.
7V could be used to test for faults with the parallel delta admittances and for TFT "on" conductance with the $\Delta G_s$ measurement.

\[
\frac{\delta(\Delta G_s)}{\delta(\Delta G_p)} = 1 - \frac{(2\pi \text{freq } \Delta C_p)^2}{\Delta G_p^2}
\]  (3.6)

### 3.4 Measurement of TFT Off Conductance

The TFT off conductance, $G_{tftoff}$, can be measured with either $G_{off}$ or with $\Delta G_p$. The $G_{off}$ measurement will be effected by $G_{tftoff}$ as shown in (3.7). If $G_{tftoff}$ is much less than the pixel admittance, $\omega C_{pixel}$, then the $G_{off}$ measurement will be high by $G_{tftoff}$. Since the $\Delta G_p$ measurement is not effected by $G_{gd}$ and $G_{csdl}$, it is more sensitive than the $G_{off}$ measurement when used to detect the slightly high TFT off conductance. Equation (3.8) shows that $\Delta G_p$ will be lower than normal if $G_{tftoff}$ is high. If $G_{tftoff}$ is less than $\omega C_{pixel}$, then $\Delta G_p$ will be low by $G_{tftoff}$. The detectability of this type of fault will depend on the precision of the $\Delta G_p$ measurement, which is about 0.05nS at 8kHz with a 3.0Vpeak test voltage.

\[
G_{off} = G_{off,normal} + G_{tftoff} \frac{(\omega C_{pixel})^2}{(G_{tftoff}^2 + (\omega C_{pixel})^2)}
\]  (3.7)

\[
\Delta G_p = \Delta G_{p,normal} - G_{tftoff} \frac{(\omega C_{pixel})^2}{(G_{tftoff}^2 + (\omega C_{pixel})^2)}
\]  (3.8)

### 3.5 Characterization of LCD Operation Effects with Pixel Admittance Measurements

The previous sections have shown many pixel parameters which can be precisely measured with the transfer admittance technique. This section will describe the many
LCD operation effects which can be characterized with these measurements. These include TFT turn-on characteristics, TFT threshold measurements, pixel leakages, TFT leakages, and voltage feedthrough measurements.

3.5.1 Effect of TFT "on" Conductance on LCD Operation

The ΔGs measurement was shown to be useful in measuring TFT on conductance. Ideally, the TFT should act like an ideal switch with infinite on conductance and zero off conductance. For proper LCD operation, the TFTs' "on" and "off" characteristics must be close to ideal. Figure 3-9 shows typical voltage waveforms for a TFT-addressed LCD. The TFT "on" conductance must be high enough so that the pixel voltage reaches the desired data voltage, $E_{\text{data}}$. This criterion is equivalent to ensuring a sufficiently low $E_u$, the voltage difference between the column and the pixel at the end of the gate write pulse time.\(^{32}\) The TFT "on" conductance, $G_{\text{tft}}$, required for a given $E_u$ is shown in (3.8). The total pixel capacitance which must be charged is the sum of the pixel storage capacitance, $C_s$, and the capacitance of the liquid crystal material, $C_{\text{lc}}$.

$$G_{\text{tft}} = - \frac{C_s + C_{\text{lc}}}{T_{\text{write}}} \ln \left( \frac{E_u}{E_{\text{data}}} \right)$$  \hspace{1cm} (3.8)

3.5.2 Voltage Feedthrough Effect

Figure 3-9 also shows a feedthrough voltage error which changes the voltage on the pixel electrode when the scan signal changes polarity. This results from a capacitance voltage divider due to the $C_{\text{gs}}$ and $C_s$ capacitances and is expressed in (3.9). This error is problematic especially if the $C_{\text{gs}}$ value changes across the panel. A simple test of measuring all $C_{\text{gs}}$ pixel values by placing the acv only on the gate line can be helpful in determining the feedthrough voltage error across the panel.

3.5.3 TFT Threshold Effect

The TFT threshold is the voltage at which the TFT conductance reaches a value suitable to place the TFT in its on state. A criterion for display uniformity is a minimum variation in the TFT threshold voltage, \( E_t \), across the panel. This requirement for proper panel operation can be tested by using either the series or parallel equivalent circuit model. \( \Delta G_p \) can be measured to find the bias voltage at which the \( G_{tft} \) equals \( \omega C_{pixel} \), which is well known for the panel. Alternatively, the TFT threshold voltage, \( E_t \), can be found by measuring \( \Delta G_s \) at different dc bias voltages.

3.5.4 Pixel Leakages

Figure 3-9 shows the leakage voltage, \( E_{leakage} \), which results from leakage conductances across \( C_{gs} \), \( C_s \), or the TFT. The leakage must be small enough to ensure that the pixel voltage remains relatively constant during the time pixels on other gate
lines are being written. The upper limit on permissible $G_{\text{pixel}}$ for proper panel operation is shown in (3.10) as a function of the pixel capacitances ($C_{\text{pixel}}$), the horizontal scan time ($T_{\text{scan}}$), and the permissible fraction of voltage decay ($K_1$):

$$G_{\text{pixel, max}} = -\ln(K_1) \frac{C_{\text{pixel}}}{T_{\text{scan}}}$$  (3.10)

Assuming a 60Hz scan cycle, $C_{\text{pixel}} = 1pF$, and $K=0.9$, a typical value for $G_{\text{pixel, max}}$ is 6.3pS. The leakage may be difficult to measure for the following reasons. First, to measure such small conductances for a given pixel requires that differences between normal pixels be much smaller than $G_{\text{pixel, max}}$. Second, the conductance measurement precision must be much lower than $G_{\text{pixel, max}}$. With a 10ms test time per pixel, the anticipated conductance measurement precision is 50pS. Better measurement precision can be gained by taking more time to measure or using a larger test voltage. However, the measurement improvement increases only with the square root of the additional time taken.

### 3.5.5 TFT Leakages

The leakage across the TFT can also be a problem in maintaining a constant pixel voltage during the scan cycle. The leakage problem is often a higher than normal TFT "off" conductance, $G_{\text{tft off}}$, which serves as the leakage path. In cases where $G_{\text{tft off}}$ is large, a measurement of $G_{\text{off}}$ can easily detect the leakage. However, a pixel can behave improperly with $G_{\text{tft off}}$ as low as 100pS. In the case of these very low TFT leakages, it may be more effective to test for other TFT characteristics which are affected by slightly high $G_{\text{tft off}}$. We have been advised by manufacturers that high $G_{\text{tft off}}$ causes a change in the shape of the I-V curve of the TFT or a leftward shift in the I-V curve. Both effects will result in a higher TFT current and thus a higher TFT off conductance. The delta admittance measurements taken at different bias voltages may be more sensitive to the
shift or slope change in the I-V curve than the Goff measurement. This will be a subject for further research.
Chapter 4

Transmission Line Effects

In previous chapters the measurements of pixel admittances were assumed to be independent of the position of the pixel in the LCD matrix. This assumption is valid when the resistances along the gate, drain, and Cs bus lines is zero. However, in reality these resistances are not zero and the measurements of $\Delta C_p$ and $\Delta G_p$ will be effected by the pixel's position in the LCD matrix.

4.1 Model for LCD Transmission Line Effect

The measurement of admittance parameters at different places on the LCD panel is effected by a transmission line effect on the gate line voltage and the drain line current. This transmission line behavior results from the resistance of the lines and the lumped capacitance from the line to ground at each pixel in the LCD array. A model for the series and shunt impedances in the transmission lines is shown in figure 4-1 for a "Cs bus" topology. Table 4-1 shows the series R and shunt C for the transmission line models for each of the three LCD topologies. The combination of the series resistance and shunt capacitance creates an RC transmission line for both the horizontal and vertical lines. The transmission line effect will cause a magnitude attenuation and a phase lag in
the gate line voltage and the drain line current. The main effect of the transmission line
phase shift, shown in figure 4-2, will be a clockwise rotation of the admittance phasor in
the complex admittance plane. By using transmission line theory, the transmission line
attenuation and phase shift can be predicted at any point on the panel. This chapter will
model this effect using transmission line theory and will present measured LCD data to
verify the model.

![Circuit Diagram](image)

**Figure 4-1:** The circuit diagram used to characterize the transmission line behavior across gate, drain, and Cs lines. The pixel shown with the TFT is in row m and column n.

### 4.1.1 Complete transmission line model

The equations for a transmission line are shown in (4.1) and (4.2)\(^{33}\), where the input and
output currents and voltages are defined in figure 4.3 and l is the length of the line from
the output. These equations can be manipulated to find the voltage attenuation and phase
shift along the gate and Cs bus lines and to find the current attenuation and

Transmission Line parameters for the three LCD topologies

<table>
<thead>
<tr>
<th>topology</th>
<th>Gate Line</th>
<th>Cs bus / Next gate line</th>
<th>Drain line</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Series R</td>
<td>Shunt C</td>
<td>Series R</td>
</tr>
<tr>
<td>Cs bus</td>
<td>$\frac{R_{gl}}{N}$</td>
<td>$C_{gd}+C_{gs}$</td>
<td>$\frac{R_{csl}}{N}$</td>
</tr>
<tr>
<td>Next gate</td>
<td>$\frac{R_{gl}}{N}$</td>
<td>$C_{gd}+C_{gs}$</td>
<td>$\frac{R_{csl}}{N}$</td>
</tr>
<tr>
<td>No Cs</td>
<td>$\frac{R_{gl}}{N}$</td>
<td>$C_{gd}+C_{gs}$</td>
<td>NA</td>
</tr>
</tbody>
</table>

Table 4-1: Series R and Shunt C for the transmission line models of the three LCD topologies. M is the total number of gate lines and N is the total number of drain lines.

Figure 4-2: Complex admittance diagram showing the effect on $\Delta C_P$ and $\Delta G_P$ from the transmission line phase shift of angle $\theta$. Since the ideal pixel admittances are mostly capacitive, the phase shift will slightly decrease the measured $\Delta C_P$ and will make a more pronounced increase in the measured $\Delta G_P$.

\[
\text{Im}(Y) = j\omega \Delta C_P
\]

\[
\Delta C_P,\text{pixel} \quad \Delta C_P,\text{meas}
\]

\[
\Delta G_P,\text{pixel} \quad \Delta G_P,\text{meas}
\]

\[
\theta
\]

\[
\text{Re}(Y) = \Delta G_P
\]

\[
E_1 = E_2 \cosh(\sqrt{ZY} l) + I_2 Z_0 \sinh(\sqrt{ZY} l) \quad (4.1)
\]

\[
I_1 = I_2 \cosh(\sqrt{ZY} l) + \frac{E_2}{Z_0} \sinh(\sqrt{ZY} l) \quad (4.2)
\]
Figure 4-3: Circuit diagram for traditional transmission line. Equations (4.1) and (4.2) describe the voltage and current at the input to the line.

...phase shift along the drain lines. From the diagram in figure 4.4 and (4.1) and (4.2), the ratio of the pixel voltage to the source voltage is shown in (4.3) as a function of the position along the gate line, n, and the total number of drain lines, N. Similarly the ratio of the measured current to the pixel current can be found from figure 4.5 and is given in (4.4) as a function of the position along the drain line, m, and the total number of gate lines, M. From these equations for the voltage and current, an equation for the measured pixel admittance in terms of the actual pixel admittance and the position in the LCD matrix can be found, (4.6). This equation is useful for correcting the measured pixel admittance to predict the actual pixel admittance.

Figure 4-4: Circuit diagram for calculating the transmission line effect along the gate line.

\[
\frac{E_{\text{pixel}}}{E_{\text{source}}} = \frac{\cosh(\sqrt{ZY}(N-n))}{\cosh(\sqrt{ZY}N)} \quad (4.3)
\]

\[
\frac{I_{\text{meas}}}{I_{\text{pixel}}} = \frac{\cosh(\sqrt{ZY}(M-m))}{\cosh(\sqrt{ZY}M)} \quad (4.4)
\]

\[
Y_{\text{meas}} = Y_{\text{pixel}} \frac{\cosh(\sqrt{ZY}(M-m)) \cosh(\sqrt{ZY}(N-n))}{\cosh(\sqrt{ZY}M) \cosh(\sqrt{ZY}N)} \quad (4.5)
\]
4.1.2 Simplified transmission line model

An approximation of the transmission line effect at the end of the gate or drain line can be made by using a lumped model with the total line resistance shunted by capacitances at each end of the line equal to half the total shunt capacitance. Since the source and detector are both low impedances, the circuit is now reduced to a single RC time constant. The phase angle and magnitude attenuation at the end of the line are shown in (4.6) and (4.7), respectively. To consider the attenuation and phase lag at individual pixels, the full transmission line model should be used.

\[
\text{Phase Lag} = \tan^{-1} \left( -\frac{\omega R_{\text{line}} C_{\text{line}}}{2} \right) \quad (4.6)
\]

\[
\text{Attenuation} = \frac{1}{\sqrt{1 + \omega^2 R_{\text{line}}^2 C_{\text{line}}^2}} \quad (4.7)
\]

4.2 Row Measurements on a LCD panel

Row measurements on a LCD panel with Cs connected to the next gate line are shown in figure 4-6 for \( \Delta C_p \) and figure 4-7 for \( \Delta G_p \). The \( \Delta C_p \) curve shows a relatively constant
value of about 0.5pF across most of the panel with a slight increase at the end of the row. The transmission line attenuation and phase shift should cause $\Delta C_p$ to be at its maximum at the beginning of the row and decrease slightly along the row. The rise in $\Delta C_p$ and the discontinuities in the measurements after drain line 1500 can be explained by the cable connections from the probed panel to the admittance tester. The drain lines are routed to a pre-multiplexor box where banks of 160 drain lines are selected for measurement. This is necessary because the admittance test system has a limited number of 160 current detectors. The layout of the traces in the pre-multiplexor box causes some of the drain line traces to be longer than others, resulting in more or less parasitic capacitance to ground. The drain lines are routed in groups of 40 lines which explains the groups of discontinuity in the $\Delta C_p$ measurement which also occur in groups of 40. Note that the $\Delta C_p$ value at the beginning of the row is a little smaller than the 0.5019pF measured on the pixel in Table 3-1. This happens because row 240 is half way down the drain line and will be effected by the drain transmission line phase lag (See Appendix 1 for a diagram of the drain pad connections). Row 240 was chosen because the drain lines are alternately connected at the top and bottom of the panel, so that adjacent drain lines have different line lengths depending on the row position. The drain line lengths are equal when row 240 is measured.

The $\Delta G_p$ row measurement shows the effect of the phase lag across the panel. The simulation using the transmission line model is shown to closely approximate the measured effect on $\Delta G_p$. From the simplified model for the total phase shift along the line, the angle change is -5.51 degrees assuming $R_{gl}$=4kohms and $C_{total}$=0.5pF*1920/2. This causes an increase in $\Delta G_p$ of about 2.4OnS, which is close to the measured values shown in figure 4-7. The $\Delta G_p$ also shows the effect of unmatched drain line lengths in the pre-multiplexor box which causes a discontinuity is groups of 40 pixels along the row.
Figure 4-6: \( \Delta C_p \) measurements for row 240 on a LCD panel with Cs connected to the next gate line.

Figure 4-7: \( \Delta G_p \) measurements for row 240 on a LCD panel with Cs connected to the next gate line. A curve estimating the change in \( \Delta G_p \) across the row with the transmission line model is also shown.
4.3 Column Measurements on a LCD Panel

Column measurements on a LCD panel with Cs connected to the next gate line are shown in figure 4-8 for \( \Delta C_p \) and figure 4-9 for \( \Delta G_p \). The \( \Delta C_p \) curve decreases slightly across the first part of the row as expected, and then increases slightly. Because a single drain line and detector is used for this measurement, the pre-multiplexor trace capacitances do not have an effect. One possible explanation is that the pixel capacitances differ slightly across the panel. More experiments with other substrates of the same type need to be performed to verify this.

The \( \Delta G_p \) column measurement shows the effect of the phase lag across the panel. The simulation using the transmission line model is shown to closely approximate the measured effect on \( \Delta G_p \). From the simplified model for the total phase shift along the line, the angle change is \(-4.67 \) degrees assuming \( R_{gl}=40\text{kohms} \) and \( C_{total}=0.17\text{pF*480/2} \). This causes an increase in \( \Delta G_p \) of about 2.03\text{nS}, which is close to the measured value shown in figure 4-9.
Figure 4-8: ΔCp measurements for column 1 on a LCD panel with Cs connected to the next gate line.

Figure 4-9: ΔGp measurements for column 1 on a LCD panel with Cs connected to the next gate line. A curve estimating the change in ΔGp across the column with the transmission line model is also shown.
Chapter 5

Conclusion

The manufacture of TFT-LCD substrates for flat panel display applications has proven to be a formidable manufacturing problem. Because of the low yields in the production of these panels, there is a need for fast automatic testing of the TFT-LCD substrates. A transfer admittance test method has been developed to fill this testing need. A theoretical analysis of the transfer admittance test method has been given and experimental results have shown its feasibility. The transfer admittance test method relies on high precision measurements of each pixel in the TFT-LCD substrate. The measurement theory presented in this thesis is essential for achieving the preferred test conditions necessary in implementing an automatic test system.

The measurement of pixel admittances is a thorough test for almost all types of substrate production defects. Open and short defects can be easily detected because a test current flows in all possible circuit paths. Moreover, the high precision of the measurements allows the detection of small leakage conductances which could result in improper LCD display operation. The parallel delta admittance measurements, ACp and AGp, have measurement standard deviations of .001pF and .05nS respectively at an 8kHz test frequency. The capacitance precision is much smaller than the individual pixel capacitances allowing complete fault coverage for open faults. The conductance precision is sufficiently small to detect shorts, and leakages with resistances greater than
1Gohm. The series delta admittance measurements, $\Delta C$s and $\Delta G$s, have measurement standard deviations of 0.002 pF and 1 nS respectively at an 8 kHz test frequency. The series conductance can detect variations in the TFT on conductance with a precision of 1 Gohm.

The automatic testing of TFT-LCD substrates requires comparison of the pixel admittances across the panel. Line resistances and shunt capacitances were shown to introduce errors in the measured admittances. To solve this problem, a transmission line model was developed to quantify the error factor as a function of the position of the measured pixel. The error factor developed here can be integrated into the automatic test procedure to remove the error due to the line resistance and shunt capacitance.

The theory presented in this thesis has been used to develop an automatic system for testing TFT-LCD substrates. The system is based upon the measurement topology described in chapter 2. The detector noise evaluation was very important in the system development because this noise determines the measurement precision. The discussions of test connection errors and test conditions is also important to optimize the measurement precision and accuracy for various types of TFT-LCD substrates. The theory and experimental results presented in this thesis have also shaped the fault detection and identification algorithms.

The design of an automatic test system requires more than the measurement theory detailed in this thesis. The system throughput is a critical design parameter in the cost of testing. Throughput may be increased by optimizing the allocation of test time. A probabilistic analysis of the occurrences of measured good and bad pixels could help in optimizing this time allocation.

Increasing throughput, improving measurement precision, and refining detection algorithms will all be subjects for future research.
Appendix 1

Glossary

AMLCD  Active matrix liquid crystal display.

Cgd  Gate to drain capacitance. This capacitance includes the parasitic TFT gate to drain capacitance and the capacitance of a gate to drain line crossing.

Cgs  Gate to source capacitance. This capacitance includes the parasitic TFT gate to source capacitance and the gate to pixel electrode capacitance. Since these two are in parallel, they cannot be measured separately and are thus grouped together.

Coff  The measured capacitance with the TFT biased in its off state.

Con  The measured capacitance with the TFT biased in its on state.

Cs  Storage capacitance used to hold the pixel's charge during the horizontal scan cycle. This is the storage capacitance between the pixel electrode and the Cs bus for the "Cs bus" LCD circuit topology. For the "Cs to next gate" LCD topology, this is the storage capacitor between the pixel electrode and the next gate line.

Ccstdl  The crossover capacitance between the Cs bus and a single drain line. The sum of all of these capacitances along a drain line, due to the many Cs bus to drain line crossings, is the main contributor to the large Coff capacitance.

ΔCp  The parallel delta capacitance of a pixel. This quantity is computed by subtracting the measured Coff from the measured Con capacitances.

ΔCs  The series delta capacitance of a pixel. This quantity is computed from the parallel delta admittances using standard parallel to series conversion formulae.

DFT  Discrete Fourier Transform. An algorithm for computing the Fourier coefficients of a discrete time waveform. The FFT is a software implementation of the DFT algorithm which is optimized for speed of calculation or memory requirements.
ΔGp  The parallel delta conductance of a pixel. This quantity is computed by subtracting the measured Goff from the measured Gon conductances.

ΔGs  The series delta conductance of a pixel. This quantity is computed from the parallel delta admittances using the standard parallel to series conversion formulae.

Gcsdl The leakage conductance between the Cs bus and a drain line.

Ggd  The leakage conductance across Cgd.

Ggs  The leakage conductance across Cgs.

Gs   The leakage conductance across Cs.

Goff The measured conductance with the TFT biased in its off state.

Gon  The measured conductance with the TFT biased in its on state.

Gtft The TFT channel conductance.

LC   Liquid Crystal. The chemical material used to control the amount of light passing through a liquid crystal display.

LCD  Liquid Crystal Display.

M    The number of gate lines or the number of pixels along a drain line.

M'   The number of test signal cycles over which the measurement is made.

N    The number of drain lines or the number of pixels along a gate line.

N'   The number of waveform samples that the detector uses to compute the DFT.

nS   nanoSiemens. Unit of conductance equal to 1e-9 Siemans.

pF   picoFarads. Unit of capacitance equal to 1e-12 Farads.

Rdl  Drain line resistance. The total drain line resistance divided by M, the number of pixels along the drain line.

Rgl  Gate line resistance. The total gate line end to end resistance divided by N, the number of pixels along the gate line. This quantity is used in the transmission line calculation.
Rprd  drain pad to guard ring resistance.

Rprg  gate pad to guard ring resistance.

TFT   Thin film transistor used as the controlling element for each pixel in an AMLCD.

Transfer Admittance In the LCD testing application, this refers to the measurement of a pixel's admittances by applying an ac voltage on a horizontal line and measuring the resultant current in the vertical line.

\[ \omega \]  radian frequency \((=2\pi f_{\text{test}})\).

\( Y \)  Complex admittance. This is composed of a real part, conductance, and an imaginary part, susceptance. \( Y = G + j\omega C \).

\( Z \)  Complex impedance. This is composed of a real part, resistance, and an imaginary part, reactance. \( Z = R + j\omega L \).
Appendix 2

TFT Topology

This appendix presents typical diagrams describing the layout of a TFT in the TFT-LCD array. Figure A2-1 shows a cross-sectional view of an amorphous silicon TFT with an inverted staggered structure. This is a common topology used in TFT-LCD displays.

Figure A2-2 shows a top view of the TFT device.

Figure A2-1: Cross-sectional view of an amorphous silicon TFT with an inverted staggered structure. (Redrawn from: Shinji Morozumi, "Active-matrix Displays", 1989 SID Seminar Notes, figure 13, p. 10.22.)
Figure A2-2: Top view of an amorphous silicon TFT with an inverted staggered structure.
Appendix 3

Specifications for TFT-LCD Substrate Used for Experimental Measurements

A TFT-LCD substrate with Cs connected to next gate line was used for all the experimental data presented in this thesis. Table A3-1 shows the specifications for this panel. Figure A3-1 shows a diagram of the TFT-LCD substrate.

<table>
<thead>
<tr>
<th>Specifications for 10&quot; TFT-LCD substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of rows</td>
</tr>
<tr>
<td>Number of columns</td>
</tr>
<tr>
<td>Rgl</td>
</tr>
<tr>
<td>Rd1</td>
</tr>
<tr>
<td>Cgs</td>
</tr>
<tr>
<td>Cgd</td>
</tr>
<tr>
<td>Cs</td>
</tr>
<tr>
<td>topology</td>
</tr>
</tbody>
</table>

* no guard ring and no Rprg or Rprd resistors

Table A3-1: Specifications for 10" TFT-LCD substrate used for experiments.
Figure A3-1: 480x1920 TFT-LCD substrate with Cs storage capacitors connected to the next gate line. This substrate was used for all experimental measurements.
Bibliography

1. Introduction


Troutman, R.R., "Forecasting Array Yields for Large-Area TFT-LCDs", SID 1990 Digest, pp. 197-200.

Wisnieff, R.L., "In-process Testing of Thin-Film Transistor Arrays", SID 90 Digest, pp. 190-193.


2. Transfer Admittance Test Method


GenRad Application Note, Concord, MA., "Multi-Terminal Impedance Measurements, or... Why Do Those New Bridges Use So Many Connections?"


Mahoney, Matthew, DSP-Based Testing, Computer Society of the IEEE, 1987


3. Pixel Model for LCD Testing


GenRad Application Note, Concord, MA., "Series and Parallel Impedance Parameters and Equivalent Circuits"


4. Transmission Line Effects