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Handheld 2-channel impedimetric cell counting system with embedded real-time processing

A. Rottigni*[a], M. Carminati[a], G. Ferrari[a], M. D. Vahey[b], J. Voldman[b], M. Sampietro[a]
[a]DEI, Politecnico di Milano, Piazza Leonardo da Vinci 32, Milano, Italy;
[b]RLE, Massachusetts Institute of Technology, 77 Massachusetts Ave., Cambridge, MA, USA

ABSTRACT

Lab-on-a-chip systems have been attracting a growing attention for the perspective of miniaturization and portability of bio-chemical assays. Here we present a the design and characterization of a miniaturized, USB-powered, self-contained, 2-channel instrument for impedance sensing, suitable for label-free tracking and real-time detection of cells flowing in microfluidic channels. This original circuit features a signal generator based on a direct digital synthesizer, a transimpedance amplifier, an integrated square-wave lock-in coupled to a ΣΔ ADC converter, and a digital processing platform. Real-time automatic peak detection on two channels is implemented in a FPGA. System functionality has been tested with an electronic resistance modulator to simulate 1% impedance variation produced by cells, reaching a time resolution of 50μs (enabling a count rate of 2000 events/s) with an applied voltage as low as 200mV. Biological experiments have been carried out counting yeast cells. Statistical analysis of events is in agreement with the expected amplitude and time distributions. 2-channel yeast counting has been performed with concomitant dielectrophoretic cell separation, showing that this novel and ultra compact sensing system, thanks to the selectivity of the lock-in detector, is compatible with other AC electrical fields applied to the device.

Keywords: Flow Cytometry, Bio-impedance, FPGA, DDS, Lock-in

1. INTRODUCTION

Massive, cross-disciplinary scientific and technological efforts are devoted to the development of microfluidic systems allowing the implementation of bio-chemical analytical and diagnostic assays in miniaturized, portable lab-on-a-chip devices[1]. Unfortunately, very often the portability (and thus the diffusion) of these revolutionary bio-medical devices is significantly limited by dimension and complexity of the instrumentation required for their operation, in particular for liquid driving (pumps), sample preparation (centrifuges) and detection (microscopes).

Among different detection techniques (optical, magnetic), electrochemical sensing represents a very promising candidate for low-cost integration in miniaturized platforms. Furthermore, sub-cellular spatial resolution can be achieved thanks to state-of-the-art processes for micro-fabrication of sensing electrodes. A direct electrical read-out enables automatic, multi-channel, high-throughput and quantitative single-cell screening. Bio-mass impedance detection, in particular, is a versatile tool leveraged for label-free cell detection, analysis and sorting based on intrinsic electrical phenotypes[2].

In the framework of impedance flow cytometry, we present an original handheld instrument that addresses the need for miniaturization and portability, providing high-throughput automatic impedimetric cell counting on two simultaneous channels. It is based on the integration of a custom CMOS lock-in analog demodulator and sigma-delta converter with a field-programmable gate array (FPGA) for real-time digital processing that implements peak detection and manages signal generation and acquisition.

2. ANALYSIS OF IMPEDANCE SENSING SPECIFICATIONS

This portable detection system has been designed to be coupled to a specific microfluidic platform[3] for label-free cell sorting and counting, but it can be easily adapted to enhance the operation of a wide variety of devices. Quantitative design specifications can be identified starting from the analysis of the properties of the pair of micro-scale impedance sensing electrodes (Figure 1a). As illustrated in Figure 1b, the simplest small-signal equivalent circuit of the electrode-solution interface is given by the series of the *double layer* capacitance, accounting for the modulation of the ionic concentration at the interface[4], and the solution resistance. The double layer capacitance (C_{DL}=800pF in our device) can

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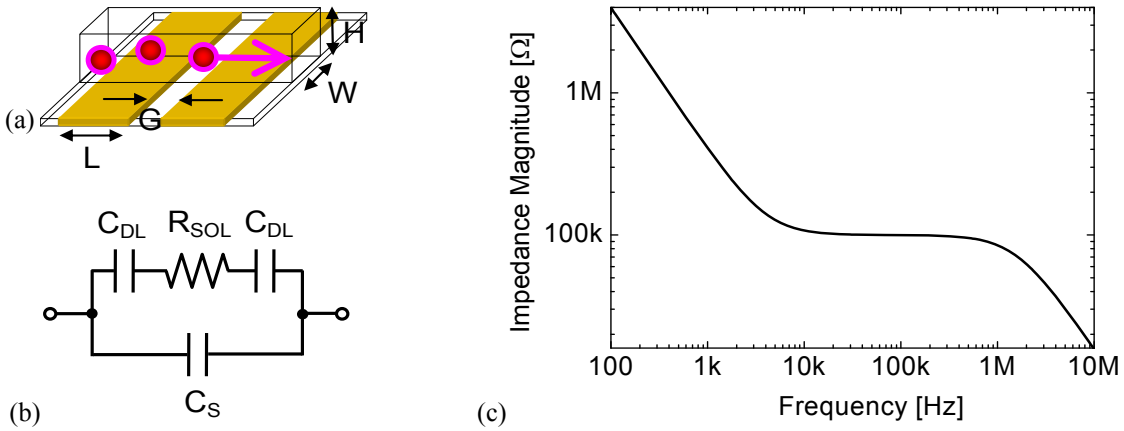

Figure 1. (a) Coplanar electrode configuration at the bottom of a microfluidic channel for impedimetric flow cytometry: L=200µm, G=12µm, W=40µm and H=20µm. (b) Equivalent impedance model comprising the double layer capacitance (C_{DL}=800pF), the solution resistance (R_{SOL}~100kΩ) and a stray capacitance (C_S~1pF). (c) Simulation of the corresponding spectrum. The operating frequency range is 10kHz-1MHz, where the modulation of the resistive plateau is well detectable.

be estimated from the area of the electrode in contact with the solution, considering a specific capacitance of 0.1-0.2pF/µm^2 for standard *Phosphate Buffered Saline* (PBS). The calculation of the solution resistance, scaling with the bulk conductivity of the saline buffer (1.5S/m for PBS), can be more complex depending on the geometry of electrodes (30-100kΩ in our case). In the common case of coplanar electrodes, conformal mapping[5] and finite element numerical simulations can be employed. Numerical simulations are used as well to estimate the intensity of the impedance modulation due to the presence of the cell in the channel over the electrodes. Below the MHz range, cells can be considered as insulating shells. Thus, the perturbation of the electric field between the electrodes can be sensed as an increase of resistance, when a volume of conductive solution crossed by the field lines is replaced by the volume of an insulating cell (similarly to the Coulter technique). The intensity of the resistance increase depends on the cell volume (5-15µm diameter range) and on its vertical position. Optimization of electrode layout[3] (in particular setting G~H) allows maximizing the volume fraction and thus the normalized resistance variation ΔR/R (~1% for 15µm cells).

The expected spectrum is shown in Figure 1c. As a parasitic capacitive coupling is always present between the electrodes and the connection wires, the resistive plateau can be investigated only up to the cut-off frequency (~1MHz for R_{SOL}~100kΩ and C_S~1pF, that is the minimum stray capacitance achievable with a careful setup). Consequently, the detection circuit must be able to measure the real part of impedance in the 10kHz-1MHz frequency span, by applying a sinusoidal signal of the desired amplitude. It must detect, with a suitable signal-to-noise ratio (SNR), relative variations of about 0.1%-1% of the solution resistance (10-100kΩ) complying with a maximum input capacitance of ~10pF.

The detection bandwidth requirements depend on the speed of the particles crossing the sensing volume. In order to reach counting rates comparable with the throughput of state-of-art fluorescent cell sorters (thousands cells per second) a sub-ms temporal resolution is needed. Thus the selectable impedance sampling rate must extend from 1Sa/s up to 5-20kSa/s.

3. DESIGN OF THE ELECTRONIC SYSTEM

3.1 System architecture

In order to detect resistance variations of the channel impedance, a lock-in measurement scheme has been chosen. The system, presented in Figure 2, is composed by a signal generator that imposes a sinusoidal voltage across the electrodes inside the microfluidic channel, followed by a transimpedance amplifier that converts the current flowing in the device into a voltage. The signal is then multiplied by a synchronous square waveform coming from the generator in order to obtain the information about its in-phase component, proportional to the resistive part of impedance. The signal from the multiplier is then converted into the digital domain and low-pass filtered. This signal is then elaborated using an FPGA

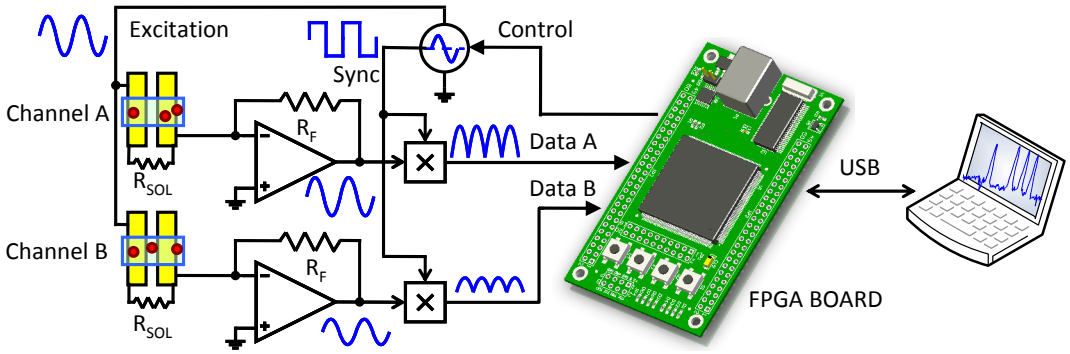

Figure 2. Block diagram of the 2 channels lock-in based impedance measurement system showing its basic blocks: the signal generator, the transimpedance amplifier, the synchronized square waveform multiplier and the USB connected FPGA board for digital data handling and experiment control.

to extract the information regarding the peaks due to the fast changes in channel resistance and the data is transferred to a laptop PC to be visualized, stored and analyzed.

For the correct design of the analog circuit, we first introduce the main equations governing the circuit transfer functions: the voltage output of the lock-in is:

$$V_{OUT,lock-in} = -V_{gen}\frac{R_f}{R_{SOL}}\frac{2}{\pi} \tag{1}$$

where V_{gen} is the output voltage of the generator, R_f is the feedback resistor of the transimpedance amplifier, R_{SOL} is the unknown resistance of the microfluidic channel and the factor $2/\pi$ is the gain of the square waveform multiplier of the lock-in. Since we expect to measure small resistance variations over a reasonably high nominal value, we can linearize (1) obtaining:

$$\Delta V_{OUT,lock-in} = V_{gen}\frac{R_f}{R_{SOL}^2}\frac{2}{\pi}\Delta R_{SOL} \tag{2}$$

Using this relation we can calculate the minimum resistance variation measurable with the instrument (ΔR_{SOL}) knowing the voltage we can apply to the system and the total output voltage noise of the instrument. For instance, for a channel resistance of 100kΩ, an applied voltage of $1V_{pp}$, the rms noise voltage needed for 10Ω resolution is $10\mu V_{rms}$. If we want a lock-in low-pass filter bandwidth of BW=5kHz (suitable for 10kS/s sampling rate), that means that the total noise density at the output of the system (assumed white around the measurement frequency) must be smaller than:

$$S_v < \frac{\sigma V_{OUT,lock-in}}{\sqrt{2BW}} = \frac{10\mu V}{\sqrt{2\times 5kHz}} = 100\frac{nV}{\sqrt{Hz}} \tag{3}$$

In the following sections we illustrate the design of the single blocks: in 3.2 the signal generation path, in 3.3 the transimpedance amplifier and the ASIC designed for lock-in multiplication and ADC conversion. In 3.4 the digital part for low-pass filtering, peak detection and data handling.

3.2 Signal generation

The signal generation path has been designed taking into account the need for (i) sufficient SNR ~80dB for an accurate detection of 0.1% resistance variations, (ii) flexible frequency selection in the 10kHz-1MHz range, in order to adapt to various electrode and channel geometries (iii) low impedance output with configurable amplitude from tens of mV up to a few Volts peak-to-peak (iv) a single-supply voltage compatible with the USB port and batteries operation (<5V).

The architecture that we have chosen for signal generation is based on a *Direct Digital Synthesizer* (DDS) followed by a fully differential transimpedance amplifier (Figure 3). The DDS is chosen for its versatility in frequency selection and its ease of integration in a digital system, while the transimpedance amplifier is needed since voltage output DDS in commerce don't allow free choice of the output mean value; in addition this solution allows differential driving of electrodes, thus providing a technique to deal with low frequency channel impedance variations due to temperature or buffer solution ions concentration. The selected DDS is AD5930 that allows a maximum clock rate of 50MHz and features a MSB output bit that can be used for lock-in synchronization. Output amplitude selection is achieved by modulating the reference current of the DDS with a potentiometer and the resulting output current range from 43μA to 5.5mA for resistor ranging from 3.9kΩ to 500kΩ. Transimpedance resistance (R_{fg}) has been chosen in order to obtain maximum output peak voltage greater than 1V (1.7 V with 620Ω), while R_{B1} and R_{B2} are needed for setting DDS output voltage inside its compliance range. Capacitances C_B and C_f are chosen to low-pass filter the output and in this configuration a gain-bandwidth product of the operational amplifier of 320MHz is needed for 45° of phase margin. To satisfy this condition we choose the LTC6404-1 fully differential amplifier.

The total output noise is due to both to the DDS and to the output buffer. The expected output noise of the DDS (not explicitly reported in the datasheet) can be estimated from the SNR (total noise in the Nyquist frequency at the output of DDS) equal to 60dB and deriving the mean power spectral density, dividing the total noise power by the Nyquist frequency (thus considering the noise white). Output noise from the transimpedance amplifier can be calculated taking into account operational amplifier series and parallel noise and passive components noise. The resulting total noise spectral density can be written as:

$$S_{v,gen} = \sqrt{\left(\frac{V_{DDS,p}}{\sqrt{2}\,SNR_{DDS}}\right)^2 \frac{2}{f_{clk}} + \left(I_{n,FDOA} + \frac{4kT}{R_B} + \frac{4kT}{R_{fg}}\right)R_{fg}^2 + \left(V_{n,FDOA}\left(1 + \frac{R_{fg}}{R_B}\right)\right)^2} \quad (4)$$

Where $V_{DDS,p}$ is the peak voltage of the generated signal, SNR_{DDS} is signal to noise ratio of DDS from datasheet, f_{clk} is DDS clocking frequency, $I_{n,FDOA}$ and $V_{n,FDOA}$ are current and noise voltage of the fully differential operational amplifier and R_b and R_{fg} are the input and feedback resistances of the output buffer (see Figure 3).

3.3 Low noise front-end and lock-in

The basic requirements for the current-reading front-end are proper bandwidth to perform resistance measurements up to 1MHz, a single-supply voltage smaller than 5V, stability with 10pF as the input capacitance and it should be as low-noise as possible. The topology chosen to perform current amplification is the classical transimpedance amplifier (Figure 4) with a feedback resistor and a parallel capacitor for stability reason. In this topology we need to choose the operational amplifier, the feedback resistor and the feedback capacitance, being the input capacitance a parasitic component that can reach 10pF. The loop gain of this structure has 2 poles (the first due to the operational amplifier and the second due to C_{in} and R_{ft}) and one zero (due to R_{ft}//C_{ft}), and the closed loop bandwidth is $GBWP_{OAT}\bullet(C_{ft}+C_{in})/(2\pi C_{ft})$. The ideal gain is R_{ft} with a pole at $1/(2\pi R_{ft}C_{ft})$, and this must be greater than 1MHz. For stability reasons we want the closed loop bandwidth

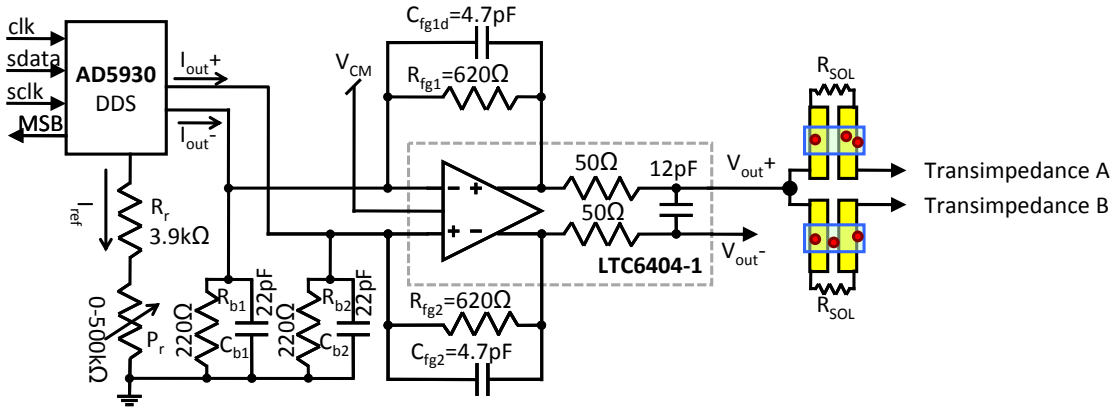

Figure 3. Schematic of the signal generation path: the AD5930 DDS, controlled by the FPGA, is followed by a fully differential output buffer, based on the LTC6404-1 operational amplifier, configured as a transimpedance amplifier, that sets the output mean value and allows differential driving of sensing electrodes.

to be at least 10 times greater than the zero in the loop gain and this sets a lower bound for $GBWP_{OAT}$ (the gain-bandwidth product of the operational amplifier). The total output noise spectral density of the amplifier, including the channel resistance is:

$$S_{v,OUT,TA} = \sqrt{4kTR_{ft} + I_{n,OAT}^2 R_{ft}^2 + V_{n,OAT}^2 \left| 1 + \frac{R_{ft}}{R_{SOL}}(1 + j2\pi f R_{SOL} C_{in}) \right|^2 + \frac{4kT}{R_{SOL}} R_{ft}^2} \quad (5)$$

where $I_{n,OAT}$ and $V_{n,OAT}$ are the current and voltage noise spectral densities of the operational amplifier and f is the frequency. Using this equations we screened commercially available operational amplifiers suitable for this block, determining for each one (i) C_{ft} in order to obtain a closed loop frequency of 50MHz, (ii) R_{ft} for an ideal gain pole of 5MHz and (iii) the total noise density. The configuration with less noise has been chosen and is presented in Figure. 4. In the realized prototype we choose not to add a physical 500fF capacitor in feedback, relying on the resistor parasitic capacitance. The information about resistance of two channels is obtained replying the structure two times.

The signals from the two analog transimpedance amplifiers are fed to two identical custom designed chips for the operations of lock-in and analog to digital conversion. The chip features an analog square wave lock-in and a 2nd order ΣΔ ADC clocked at 10MHz. With proper digital filtering this system can reach 20-bit resolution at 5kSa/s.

3.4 Digital elaboration

All digital operations are performed using an Opal Kelly XEM3001v2 integration module that features a Xilinx Spartan 3 FPGA, and circuitry to generate clocks and communicate with a PC using a USB interface. The basic operations performed by the FPGA are the low-pass filtering and decimation of the 1-bit 10MSa/s signal from the ADC, the detection of peaks in the measured signal and the control of the sinusoidal signal.

Low-pass filtering and decimation of the ADC signal is done using a 3rd order FIR filter with internally generated coefficients[6] and user selectable decimation factor up to 10000 samples, to be able to correctly filter the output of a 2nd order ΣΔ[7]. The choice to generate internally the coefficients for the filter let us save block ram in the FPGA and allows higher data transfer speed due to increased buffer size between FPGA and PC.

The detection of the peaks in the filtered signal is done using a high-pass filter and a threshold detector with hysteresis. The high-pass filter is IIR with a bandwidth equal to the sampling frequency divided by a power of 2 in order to reduce at the minimum the computational power needed for this operation. The threshold detector is a finite state machine that detects when the input signal crosses a user defined threshold with hysteresis and stores the time of the crossing of the threshold in the positive direction, the time between the crossing of the threshold in both direction and the maximum amplitude of the signal between the two crossing. The user can select to transmit to the PC data coming from both the channels and the peak detector, sharing time in the USB connection.

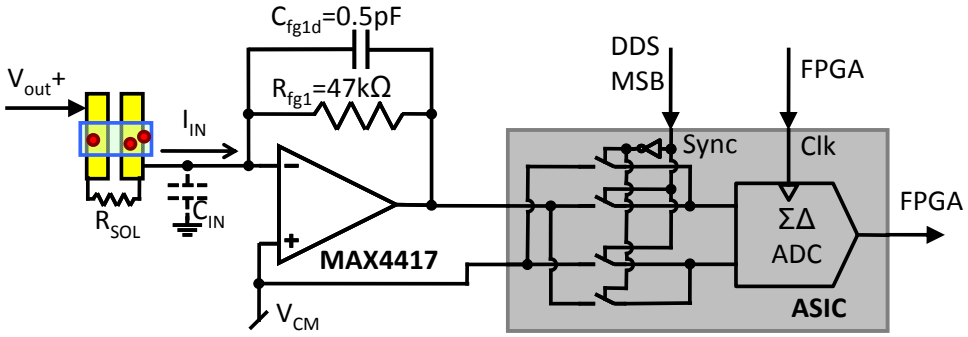

Figure 4. Schematic of the current reading path showing the low-noise transimpedance amplifier, the square waveform multiplier synchronized with the generated signal and the analog to digital converter. This structure is replicated twice to handle data from the two channels.

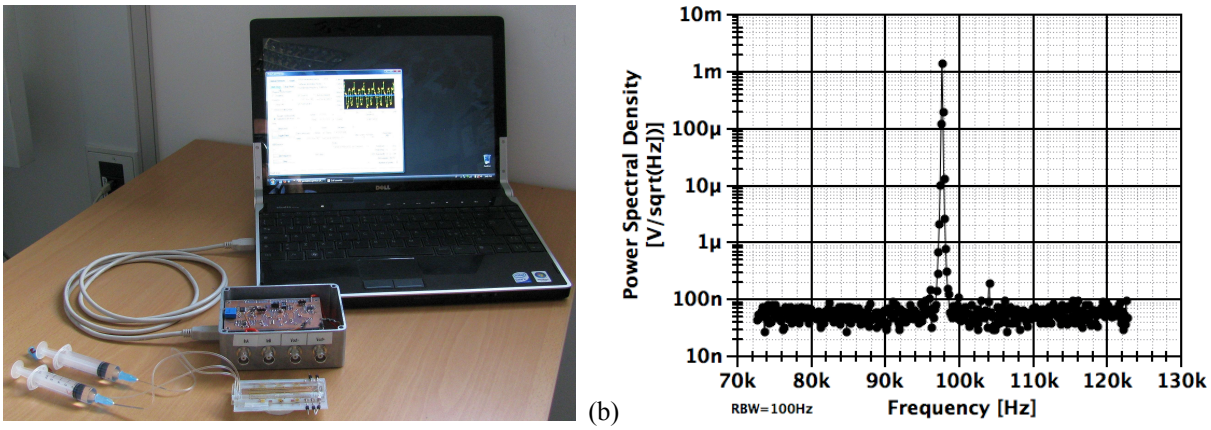

Figure 5. (a) Assembled prototype connected to the laptop for data acquisition and real-time visualization. (b) Output spectrum of the signal generator showing a noise floor of 40nV/sqrt(Hz).

The FPGA also handles serial communication to the DDS generator in order to set its frequency and mode of operation. On the PC side, a custom software written in VisualBasic records and visualizes the data coming from the measurement system and controls its user-selectable features.

4. EXPERIMENTAL RESULTS

4.1 Electronic characterization

The very compact realization of the USB-powered system (a sandwich of two 6cm x 9cm boards) is shown in Figure 5a together with cell sorting and counting microfluidic device and the laptop running the control software. At first, the two analog sections have been separately tested. In Figure 5b the spectrum of the generated sinusoid (at 97.7kHz with a peak amplitude of 20mV) is reported, showing a noise floor of 40nV/sqrt(Hz). The width of the spectral line is smaller than 3Hz (maximum resolution of the HP4195A spectrum analyzer) and the measured spurious-free dynamic range (SFDR) is 50dB, thus confirming the good spectral quality granted by the DDS.

In Figure 6 the characteristics of the transimpedance amplifier are shown: the bandwidth of this block is ~10MHz, (slightly larger than designed, due to a parasitic capacitance of the feedback resistor smaller than 500fF). The measured noise spectral density (Figure 5b) is in agreement with the design values. The signal generator and transimpedance amplifier have been successively tested together with an external lock-in instrument (Zurich Instruments) yielding global noise performances in resistance detection that agree with theoretical ones (Table 1).

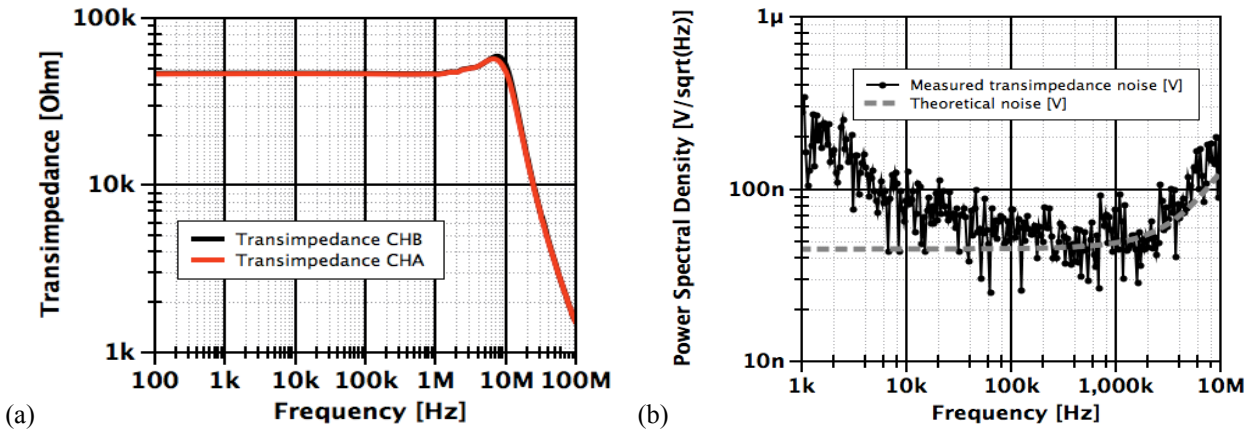

Figure 6. (a) Transfer function of the current reading amplifier showing 10MHz bandwidth and matched characteristics for both channels (b) Noise measurement of the amplifier showing good agreement with theoretical prediction.

Table 1. Comparison of the measured and theoretical noise predicted with (4) and (5), filtered with a low-pass filter with 3 real poles at 5kHz and equivalent noise expressed in Ω using (2) for different generated amplitudes, when the input resistance is equal to 47kΩ and measurement frequency is 100kHz.

Applied Voltage [mV]	Theoretical noise [μV_{rms}]	Measured noise [μV_{rms}]	Equivalent resistance noise [Ω_{rms}]
50	4.5	5.9	5.5
100	4.8	7	3.3
200	5.8	11	2.5

4.2 Validation of the peak detection algorithm

A dummy pulse generator has been realized to validate the real-time peak detection algorithm embedded in the FPGA. A fast analog switch (ADG333) shorts a 200Ω resistor producing 0.75% resistance modulation of a fixed 27kΩ resistor connected in series. The solid-state switch is driven by a custom waveform generator in which various sequences of pulses are loaded. Using this simple and reliable setup, the sequences of the peaks detected by the embedded FPGA have been compared with the results of the detection algorithm running off-line in Matlab on the recorded analog signal, acquired for the same pattern of pulses. As reported in Figure 7, good matching is obtained both with a Gaussian (a-b) and uniform (c-d) distributions of peak duration and both at medium (a-c 100pulses/s) and at high speed (b-d 1000pulses/s).

Experimental demonstration of error-free peak detection up to 2000pulse/s is shown in Figure 8f-h. Providing adequate electromagnetic shielding, by applying 200mV at 100kHz to the 27kΩ resistor, a SNR of 9 is achieved at a sampling rate of 20kSa/s (50μs time resolution). The detection performance of the proposed embedded system is comparable with that of a state-of-art bench-top lock-in (Zurich Instruments).

4.3 Counting yeast cells

Final bio-screening experiments have been performed counting yeast cells (*Saccharomyces Cerevisiae*, strain BY4743) suspended in diluted PBS (conductivity 0.35S/m, corresponding to a 100kΩ channel resistance) at a concentration of 10^5-10^6cells/ml. As reported in Figure 8, the system enables automatic threshold counting on two independent channels. The recorded peak amplitude range is 0.1%-0.5% (Figure 8b) due to the broad distribution of yeast cell size (5-15μm). The input flow rate of ~1μl/min translates into a particle velocity of ~30μm/ms and a corresponding pulse duration of ~1ms. Thus, by applying a 650mV signal at 100kHz, a 2kSa/s sampling rate provides adequate SNR and a temporal resolution of 500μs, suitable to properly capture the peaks (Figure 8b).

Thanks to the selectivity of the lock-in demodulation technique, impedimetric yeast detection has been carried out while simultaneously using dielectrophoresis to manipulate the cells (steering them between the two outlets[8]) on the same microfluidic device ($9V_{pp}$ applied at 1MHz), thus demonstrating the feasibility of fully-electrical label-free sensing and actuation on cells.

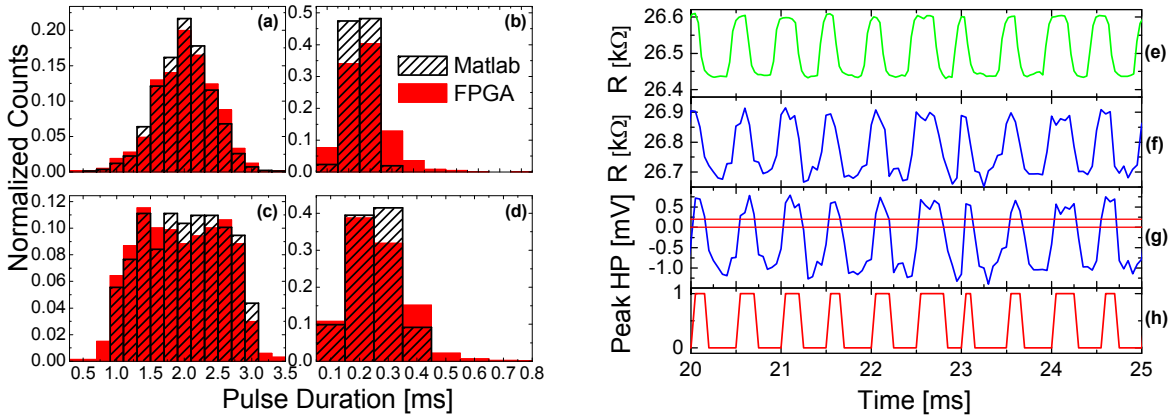

Figure 7. FPGA real-time peak detection algorithm matching the Matlab routine for Gaussian (a) 100/s and (b) 1000/s and uniform (c) 100/s and (d) 1000/s width distributions. Experimental comparison of dummy pulse detection (0.75%) with a bench-top lock-in instrument (e) and with the proposed system (f-g). HP is the high-pass filtered signal showing (h) error-free threshold counting at 2000pulse/s is demonstrated (SNR~9 with 200mV applied at 100kHz and 20kSa/s sampling rate).

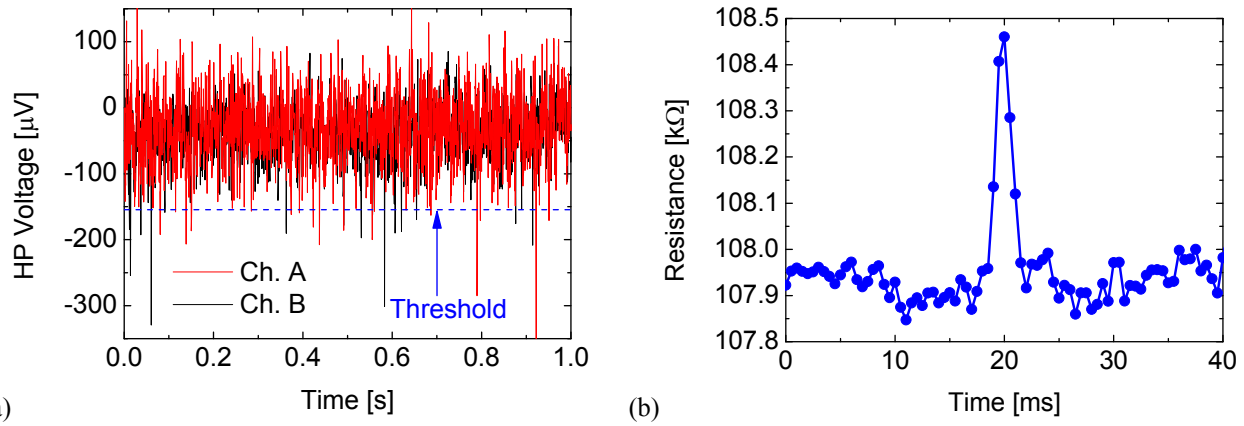

Figure 8. (a) Dual-channel automatic threshold detection of yeast cells flowing in diluted PBS at 20cell/s. (b) Detail of a single resistive peak (0.5% amplitude, 2.5ms width) sampled at 2kSa/s with an applied signal of 650mV at 100kHz.

5. CONCLUSIONS

We have presented the design and experimental characterization of credit card sized dual-channel impedance detection system able to reach a throughput of 2000 counts per second. It operates up to 1MHz with a resolution of 0.1%. Real-time peak-detection on the two simultaneous channels is performed by the embedded FPGA processing unit, thus representing a basic tool for any automated platform for high-throughput quantitative cell monitoring, analysis and closed-loop sorting. The combination of real-time digital processing and custom CMOS analog lock-in and sigma-delta converters enables unprecedented compactness and versatility.

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