Coaxial Recess Integration of InGaAs Edge Emitting Laser Diodes with Waveguides on Silicon Substrates: A Complete Solution to Laser Integration on ICs

by

Shaya Famenini

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

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Abstract

In this thesis, the first demonstration of the full integration of 1.55μm InGaAs/InP edge emitting platelet laser diodes with SiON/SiO_2 dielectric waveguides on a silicon substrate is presented. Small footprint laser platelets (300μm long by 150μm wide and 6.3μm high), are integrated and bonded in recesses etched in SiO_2 deposited on a Si substrate, and are coaxially coupled to the dielectric waveguides fabricated on the same wafer.

Lasers assembled in 6.5μm deep recesses are securely solder-bonded in place with a thin film Al/In bonding layer, which also brings the laser platelet back side n-contact to the wafer front side for measurements. The Al/In bonding layer composition and thickness are carefully optimized to provide highly reproducible vertical alignment to maximize the coupling of the laser output beam to the dielectric waveguide. Lasers are bonded into the recesses with this solder-bonding layer during a pressure assisted temperature cycle at 220˚C. The low temperature nature of the bonding phase makes this integration technique CMOS compatible.

The integrated lasers show lasing operation with threshold currents of I_{th}=17mA and I_{th}=19mA for pulsed and continuous wave drives respectively, at T=15˚C. The output spectrum shows single mode lasing near 1550nm, and a side mode suppression ratio of 25dB which is significantly higher than typical Fabry Perot cavity laser diodes. Furthermore, the integrated lasers have a characteristic temperature, T_0, of 76K which is improved from 60K for non-integrated lasers. Also the integrated lasers consistently show lower threshold currents compared to their non-integrated counterparts. The coupling loss between the laser and dielectric waveguide is extracted to be as low as 1dB, a value that can be further reduced by improved horizontal alignment and better matching the widths of laser stripe and dielectric waveguide.

Overall, this recess integration approach is CMOS compatible, is highly modular, compact and flexible, permits testing and selection of devices prior to integration, and allows integration of lasers emitting at different wavelengths on the same chip. It eliminates the need for wafer bonding III/V substrates to the host Si IC along with added complexity and cost it involves, and can be implemented using easily accessible technologies.

Thesis Supervisor: Clifton G. Fonstad
Title: Professor of Electrical Engineering

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First and foremost I would like to thank my adviser Prof. Clifton Fonstad, whose patience was iconic during the peaks and valleys of this project. His non-judgmental, professional and very stable character, in addition to his strongly motivational leadership skills, were quite empowering and enlightening to me and had a major impact in bringing this project to a success. I cannot possibly thank him enough for all I learned from him. Both through our discussions on optoelectronics and their integration, as well as the vast amount of very valuable management and life lessons I learned from him by just observing his balanced reactions to events and extremely healthy character. Such lessons, all learned implicitly, have a life time impact in helping me be a better leader, manager, and hopefully a better person in life. I feel blessed by having had the chance of working with such a great supervisor during these years and to learn so much from him, both academically and personally.

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Words come short of thanking my beloved dear late father, Parviz Famenini, for all this support and insightful advice which shaped my character and encouraged me to pursue success and excellence in life. My father's modest life, not giving in to social pressures to conform to what everyone else does, and his constant emphasis encouraging us to have a clear goal in life and to pursue it, have all had a profound impact in making me who I am and forming my ideals. I owe my independent way of thinking, resistance to illogical social pressures, strength of personality, and the constant quest in seeking meaning and goal of life endeavors all to my father and his deep impact on my personality. With that, I would like to dedicate this thesis to the fond memory of him and his pure soul which is deeply missed.

At last to lift the spirit of the reader by a jest, an academic one!, I'd like to conclude with a quote I liked from the book "My life as a Quant", by Emanuel Derman, where he describes his feelings upon graduation from Columbia University with a PhD in particle physics: "A large part of me was exhausted with physics and the seven-year struggle to shine. I consoled myself with a few sentences Einstein wrote in his autobiographical notes, composed at the age of 67, about aftereffects of his final examinations: "This coercion had such a deterring effect [upon me] that, after I had passed the final examination, I found the consideration of any scientific problems distasteful to me for an entire year.""

- My life as a Quant

Shaya Famenini

May 2012

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Chapter 1

Motivation and Approaches to Optoelectronic Integration

This chapter begins with a very short introduction to integrated circuits in general, followed by a review of the motivation behind photonic integration on silicon substrates. Different techniques that have been developed to achieve this goal will then be covered and the issues with each approach will be discussed. Finally our solution to the integration of III/V photonics on silicon substrates will be introduced, which relies on the coaxial integration of laser platelets with waveguides fabricated on Si substrates.

In the chapters that follow Chapter 1 the process of design, optimization, fabrication and implementation of this integration approach will be detailed, which in turn proves this technique to be a robust, modular, highly flexible solution for photonics integration. From the performance of laser diodes fully integrated with dielectric waveguides on Si substrate, we believe that this approach can provide a very promising solution for the integrated photonics industry and can be readily adopted and commercialized.

1.1. Integrated Circuits

The first working transistor was demonstrated in Dec. of 1947 [1], and 11 years later the invention of integrated circuits (ICs) started a new phase in electronics, communications and in an amazingly vast number of diverse other fields. Since integrated circuits provide an

insurmountable cost/performance/reliability advantage over discrete counterparts, industry has been keen to advance the IC technology ever since.

In 1965, Gordon Moore, an Intel co-founder, explained in a paper that in the time span between 1958 and 1965, the number of components per integrated circuit doubled every year and he expected the trend to persist for at least another 10 years. Whether it was his deep insight, luck, or the great inherent potential of the semiconductors microfabrication industry, this prediction turned out to be very true since then. Figure 1- 1 shows how on average the number of transistors on a CPU has doubled every 1.5-2 year since 1971 [2].

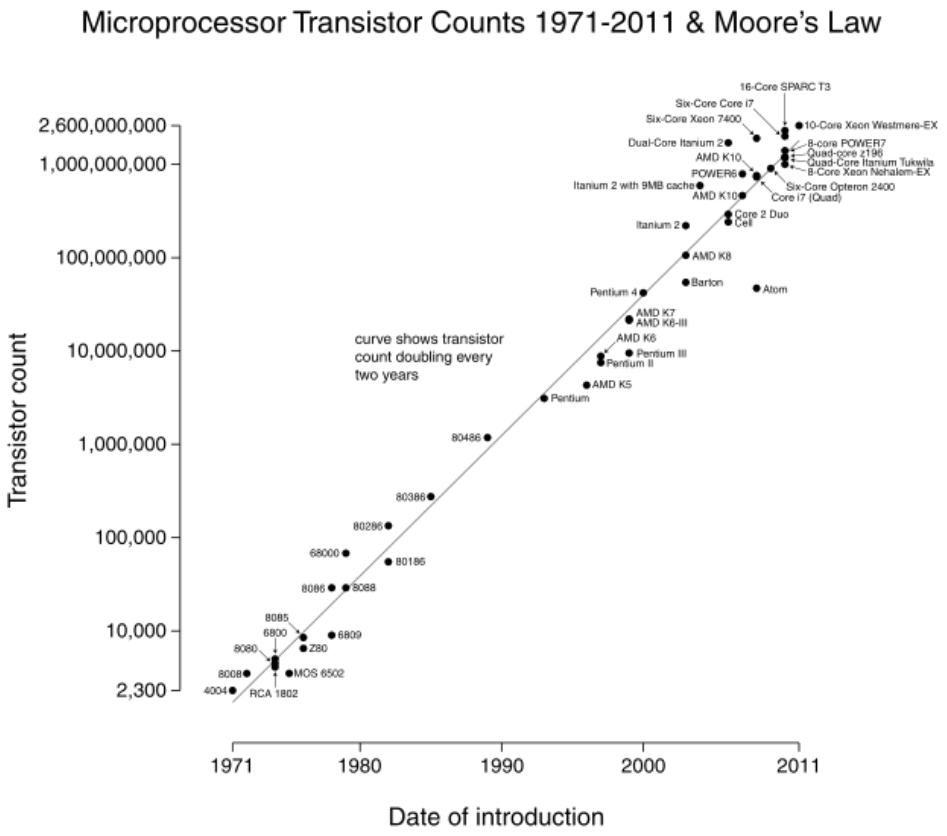

Figure 1- 1: CPU transistor count versus dates of introduction of the corresponding microprocessor. Notice the logarithmic vertical scale. The fitted line corresponds to exponential growth, with transistor count doubling every two years as the modified Moore's Law predicted.

With Moore's Law, the semiconductor industry has been setting up roadmaps for the next generations of microprocessors and memories, and has been pretty successful in meeting these milestones so far. Hence the mass production and large scale integration that such a trend puts forth resulted in stellar cost reduction and performance improvement of these electronic ICs. One might find it hard to believe that the first UNIVAC computer released in

1951 weighed 13 tons and occupied more than 35.5 square meters and had a clock speed of 2.25 MHz [3]. Sixty years later, a personal computer now is a thousand times faster and is light and compact enough that easily fits in a purse and is affordable enough that One Laptop Per Child (OLPC) campaign [4] has over 2.4 million of XO system deployments[1] as of April 2012 [5], [6].

All these make it clear how integration is the leading driver in the advances and wide-spread use of semiconductor components in the 20th and 21st centuries, which was made feasible by outstanding achievements in the technology and cost reduction simultaneously [7].

1.2. Optoelectronic Integration

The integration of optoelectronic devices with electronic circuits and systems has seen growing applications ranging from long haul to micro haul links. In fact this integration has been a concern and area of interest for the last 25 years, however until recently reliable approaches to the compact integration of photonic and electric components on a common substrate had yet to be developed, making optoelectronic integration a continuing challenge for the industry.

Increasingly higher bandwidth requirements for communication systems (from long haul to on-chip) have forced the drive for the integration of optoelectronics to access higher levels of signal processing and faster interconnection, with insight to cost and foot print reduction of the integrated circuits. As discussed earlier, the integration of CMOS electronics has followed the Moore's law trend and the number of transistors per chip has doubled every 1.5 to 2 years. This outstanding progress in the field of integration of transistors and scaling has resulted in having an astonishing number of 2.6 billion transistors integrated on a microprocessor chip commercially available in 2011, the Xeon E7 which is manufactured by Intel and has a clock rate of 1.73-2.67GHz with transistor gate lengths of 32nm and 4-10 cores per die [8]. This clearly shows the maturity of integration in silicon electronics, which is vastly ahead of photonics integration with CMOS. To address this photonics integration bottleneck, in this thesis we will talk about a novel technique to make the integration of active and passive photonics with silicon ICs feasible with a low cost, reliable, and reproducible approach.

[1] Specifically Southern American and African countries like Uruguay, Peru and Rwanda data is eye-catching.

First, we will look into why optoelectronic interconnects must (and most probably will) replace electrical interconnects in many applications.

1.2.1. Optical versus Electrical Interconnects

The limitations of electrical interconnects can be summarized as transmission line effects (high rise/fall time and channel attenuation for long channels), non-ideal effects at high frequencies such as the skin effect, frequency dependent dielectric loss, manufacturing variations, geometric issues like discontinuities, echo effect, crosstalk, and self coupling. Quite simply, electromagnetic interference and switching noise combined with higher power consumption pose serious issues with electrical interconnects when going at high bit rates over longer links.

It can be shown that for both RC limited and skin effect limited transmission lines, losses scale with the square of length in electrical interconnects [9]. This will result in frequency dependent distortion and ultimately reduces maximum achievable bit rate with inverse of the square of interconnect length.

Optical interconnects offer lower attenuation and distortion compared to their electrical counterparts, and are immune to crosstalk. As a result, optical links have become the selected choice for long haul communication. It is about a decade that optical WDM links with data rates of 5 Tb/s over 1000 km of single mode fiber without regeneration have been available commercially. In contrast, an electrical link would have a bit rate of only 0.05 b/s over the same distance. This makes it clear why optical communication has had an unbeatable triumph for long haul links. For Ethernet and LANs (local area networks) although the adoption of all optical links was slower historically, the increasingly overwhelming traffic in data centers and the need for higher bit rates has motivated the use of optical links in these applications as well.

Cho et al, compare the power consumption of optical interconnects to their electrical peers for 10cm to 1m range in [10], and the result is shown in Figure 1- 2. In summary, it is found that beyond a critical length, power optimized optical interconnects dissipate lower power compared to the state of the art high speed electrical signaling scheme. Also it is shown that at higher bit rates and lower BER, the critical length reduces and optics becomes more power favorable, which is intuitive. Consequently it is argued that these trends can be thought of as a tradeoff between optical interconnects downside of power loss in optical-electrical conversion (lower in all-optical systems) and their upside of lower attenuation and

noise (no crosstalk). Since the former is fixed and the later is length and bit-rate dependent, the optical interconnects become superior at longer lengths.

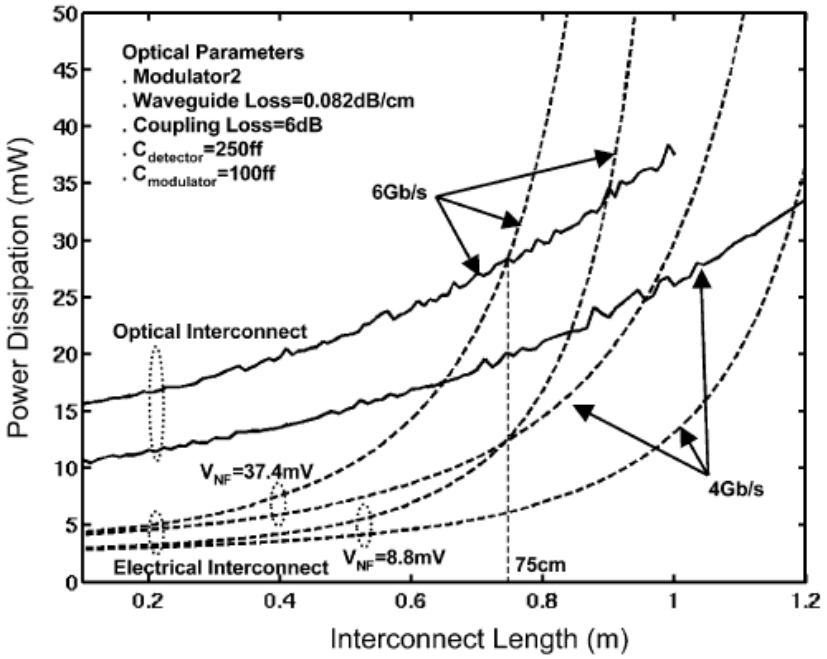

Figure 1- 2: Comparing the power dissipation of optical and electrical interconnects for different interconnect lengths.

In another effort to compare optical and electrical interconnects, Chen et al have looked into the critical lengths beyond which optical interconnects are advantageous based on delay, PDP and bandwidth density/delay in [11] and [12]. Figure 1- 3 shows the result of this comparison for different technology nodes. Consequently one can see that these critical lengths are well below the chip size with the recent technology scaling.

Therefore, even for on-chip communications, optical interconnects win over their electrical counterparts based on many different criteria.

In summary, although material research has provided improvements in electronic interconnects, such as the use of copper instead of aluminum and replacing SiO_2 with other insulators for higher performance interconnects, optical interconnects prevail in providing a high speed, low loss, low latency, massively parallel and cross talk resistant interconnection option [13] from on-chip and chip-to-chip all the way to LAN and long-haul communication applications. In Figure 1- 4 an example of high concentration of rack-to-rack fiber interconnects can be seen in the Barcelona Super Computing Center [14].

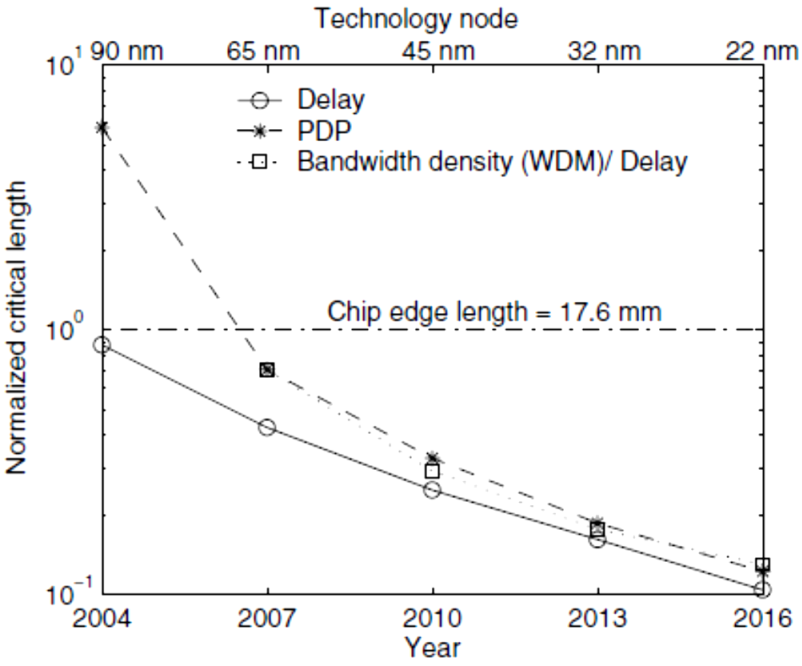

Figure 1- 3: Critical length for each recent technology node.

Figure 1- 4: Central switch racks, Barcelona Super Computing Center.

1.2.2. Evolution of Application of Optical Interconnects

Looking at the timeline of commercial deployment of optical interconnects (and thus copper displacement) [15] gives a good view regarding the history and roadmap of the trend of industry going from electrical to optical data transfer. Table 1- 1 summarizes this trend.

Year	1980's	1990's	2000's	>2012		
Range	Telecom	Datacom	Computer-com			
System	WAN, MAN	LAN	System	Board	Module	Chip
Application	Long-haul, metro	Campus, Companies	Inter-rack, intra-rack	Module-module	Chip-chip	On-chip buses
Distance	Multi-km	100's m	10's m	<1 m	< 10 cm	<20 mm
Integration	Cards	Card edge	Card edge or on card	Module	Chip to Chip	On Chip

Table 1- 1: Timeline of the introduction of optical interconnects to different range of systems, from long haul application all the way to on-chip busses [15].

While fibers showed their unbeatable superiority in 1980's in Telecom continental and metropolitan links, and a decade later found their place in LAN networks, it was around 2004-2005 that rack-to-rack fiber interconnects started to be used in super computers. In that time frame, IBM used a combination of copper interconnects for short distances of ≤10m and optical fibers for longer links (20-40m) in the ASCI Purple IBM Federation Switch (LLNL) [15]. The use of rack-to-rack optical links was extended in 2008-9 in IBM Roadrunner, and is a core element in realizing BlueWaters, one of the world's most powerful supercomputers, in a joint effort of IBM and University of Illinois with the goal of being capable of sustained performance of 1 peta flop on a range of real-world science and engineering applications [15], [16]. Figure 1- 5 shows optical fibers running not only rack-to-rack, but also connecting chips in one drawer in an IBM Power7 node network (to be used in BlueWaters system) in which 1.1 Tb/s hub switch and 1 T flop processor are noticeable [17], [18]. Of course there is no doubt that for 200-300 Gb/s speed of data transfer intra and inter drawers in such a system, optical lines are arguably the only solution.

Overall, although there is no doubt that Bandwidth × Distance product is much higher in optical links compared to copper interconnects, bringing in the former to on-chip links in commercial applications had been mainly limited by density and cost factors. However as it is argued in [19], mass production and high volume integration were the driving factors that have allowed today's affordable electronic gadgets to meet consumer budget. Without such a high volume integration, an accurate estimation of cost factor in on-chip optical interconnects is yet to be determined. Therefore, with current research and development cost estimate (i.e.

not having the advantage of high volume integration that VLSI systems have), it will be hard to judge if the cost factor will prevent the introduction of optical interconnects on chip.

Figure 1- 5: IMB Power7 IH node hub/switch network.

Needless to say that in order to drive these optical interconnects, having integrated sources is an absolute necessity. However currently most of sources are fabricated off-chip and drive the optical interconnects through suitable special packaging. Figure 1- 6 shows a recent instance of a 24-channel fiber coupled optical transceiver; in which VCSELs and photodetectors are packaged with the chip as well as a fiber array [15], [20].

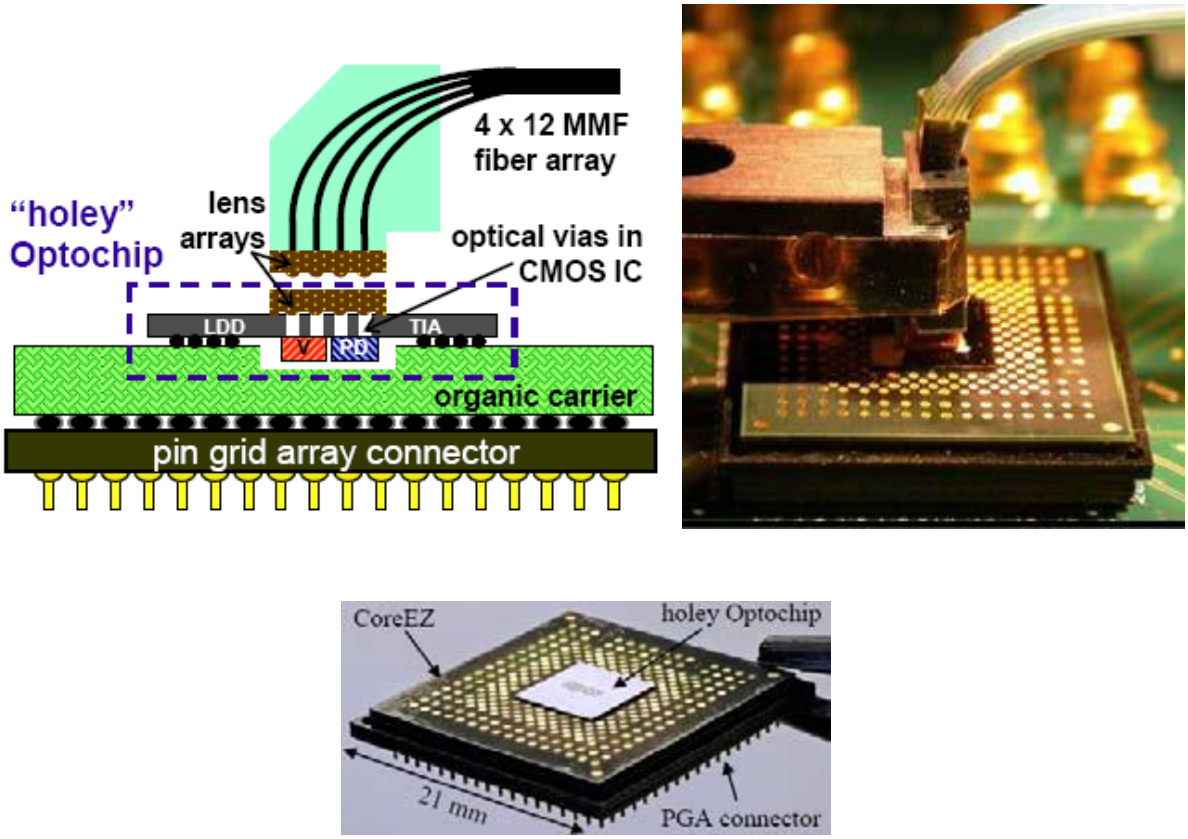

Figure 1- 6: A recent example of how VCSELs and PDs are currently packaged with fiber arrays on chip for a 300Gb/s transceiver made by researchers at IBM [20].

As the size of electronic devices continues to shrink and the usage of optical communication continues to grow, in addition to higher required data transfer rates and the greater need for higher density and more compact integration of components on chip, "monolithic" integration of electronic circuitry with photonic components (active and passive) has become increasingly desirable and necessary. In the next section, some of the pursued approaches to realize this goal will be presented and discussed with a brief focus on their strengths and weaknesses.

1.3. Approaches to Photonic Integration

Due to the importance of having integrated sources, different approaches have been adopted in order to realize lasers on Si ICs. Historically such integration had been primarily of a "hybrid" type, where by using the term "integration", essentially the careful packaging of off-chip fabricated lasers with the IC chip is intended. However this type of integration through packaging does not answer the need for monolithic integration of sources on Si and

thus other approaches have been investigated extensively. Among these attempts, trying to obtain lasing from Si itself, epitaxial growth of III/Vs on Si wafers, bonding III/V and Si wafers together, and in some cases with the removal of the III/V substrate afterwards, can be named. In the following subsections each of these techniques will be briefly reviewed.

Since giving a full breadth of all the attempts to photonic integration is beyond the scope of this introduction, a few examples of each integration approach are covered in each category, and their strengths and weaknesses will be discussed when applicable.

1.3.1. Hybrid-Packaging

Traditionally, one approach to integrate photonics with silicon integrated circuits had been "hybrid packaging" [13]. This method entailed manufacturing photonic devices separately and then the photonic chip was bonded to a board with the transceiver electrical circuitry, through wire bonds or bump bonds[2]. This method of integration revealed high parasitics which turned out to be unacceptable for high data rates. A more recent instance of such hybrid assembly and packaging is shown in Figure 1- 6 where VCSELs and PDs are integrated with the CMOS IC via a "holey" optochip [20].

As another instance of such hybrid approach in assembly/integration, researches in the MEMS arena have been interested to look into the integration of photonics on MEMS components, for instance in acoustic and vibration sensing. This can be achieved via interferometric techniques on light emitted from integrated laser components, in which the light path length is changed by an external stimulus like pressure or acceleration. Then this path length change will translate to an amplitude change in a photodetector through diffraction or interference. In [21] an implementation of such a sensor is illustrated using rudimentary assembly techniques. Although the emphasis in this work was not placed on developing a sophisticated small area integration technique, these prototypes put forth the broad area of applications for on-chip photonics when they accompany micro scale MEMS components, although their reliability and endurance should be investigated further.

1.3.1.1. Flip Chip Bonding

Flip chip or bump bonding is an approach for hybrid bonding of two material systems. This method (which can be categorized under hybrid packaging as well), has a number of drawbacks. First, it requires all the device electrical contacts to be brought to the front surface

[2] Since chip-to-chip wire bonds were unreliable, both chips were usually bonded to a board.

which is not usually the case for photonic devices made of III/Vs. This requirement will add to the fabrication steps, increases cost and reduces yield. Furthermore, since the III/V substrate is left on the top of the integrated device and it is absorbing, this poses a limitation when light needs to enter or exit the device vertically. Another significant drawback of this approach is the fact that the final chip will not be flip chip bondable to a system interconnection substrate since the thickness of III/V bonded substrate is much larger than standard bump bonds. One solution to this problem is to deep etch a recess for the III/V substrate on the mother system interconnect substrate, which adds to the complexity of the process and limits the electrical interconnection layout. Also having the III/V substrate prevents 3D stacking of multiple devices.

Removing the III/V growth substrate is advantageous in the sense that for most of active photonic devices, the active layers are in the grown epilayers and the original substrate is not functionally important. Removing the substrate is even beneficial since the back contacts get exposed and in certain applications there will not be a troublesome absorbing substrate present. However, in this approach the substrate removal step is followed by the bonding step (either bump bond or thinner metallization bond), therefore care should be taken not to affect the edges of both substrates; and eventually this approach suffers from some of the drawbacks of the bump bond approach as well.

In an attempt to the integration of optoelectronic components via this method, A. Fritze from Heriot-Watt University describes in his thesis the use of direct laser writing in making waveguides as well as a compatible polymer flip chip bonding [9]. Waveguides are polymerized with HeCd direct laser writing from an in-house-developed PMMA/diacrylate polymer base. With this approach taper writing and 45 degree angle mirrors are fabricated similar to the waveguides which function as interfaces to the external components. For the flip-chip bonding part, the fabrication of bumps and metallization masking is achieved with the same laser writing setup used for waveguides. The goal is to integrate these components with VCSEL lasers to make a fully integrated crosspoint switch. However this work had been the preliminary phases of this project as the testing of an assembled system was yet to be carried out at the time of writing the thesis in [9]. It might worth mentioning that waveguides and flip chip bonds were fabricated on glass substrates at this stage.

1.3.1.2. Planar Lightwave Circuits (PLCs)

Photonic integrated circuits (PIC) or planar lightwave circuits (PLC) have attracted a good amount of attention in the past decade, and have proven to be very promising in providing a low cost, reliable, and robust integrated photonic solution for industrial applications. PLCs are usually either silica-on-silicon or polymer based. Through this technology a wide range of photonic devices, such as couplers, filters, power splitters, can be integrated on a Si platform [118]. Photo detectors and laser diodes are also integrated on the same platform via flip-chip bonding techniques [119]. In the silica-on-silicon PLCs, the lasers are coupled to SiO_2 based waveguides which in turn couple to comparable dimension fibers that are packaged with the chip. As a result, hybrid integrated WDM transceiver modules have been fabricated for fiber-to-the-home applications based on the PLC silica-on-silicon technology [120]. The schematic in Figure 1- 7 shows this module where photodetectors and lasers, coupled to dialectic waveguides, are flip-chip bonded on the silicon platform. With polymer based PLC also, transceiver modules have been demonstrated [121]. In addition, spot-size converter semiconductor optical amplifiers have been integrated to make a Michelson interferometric wavelength converter on a PLC platform [122].

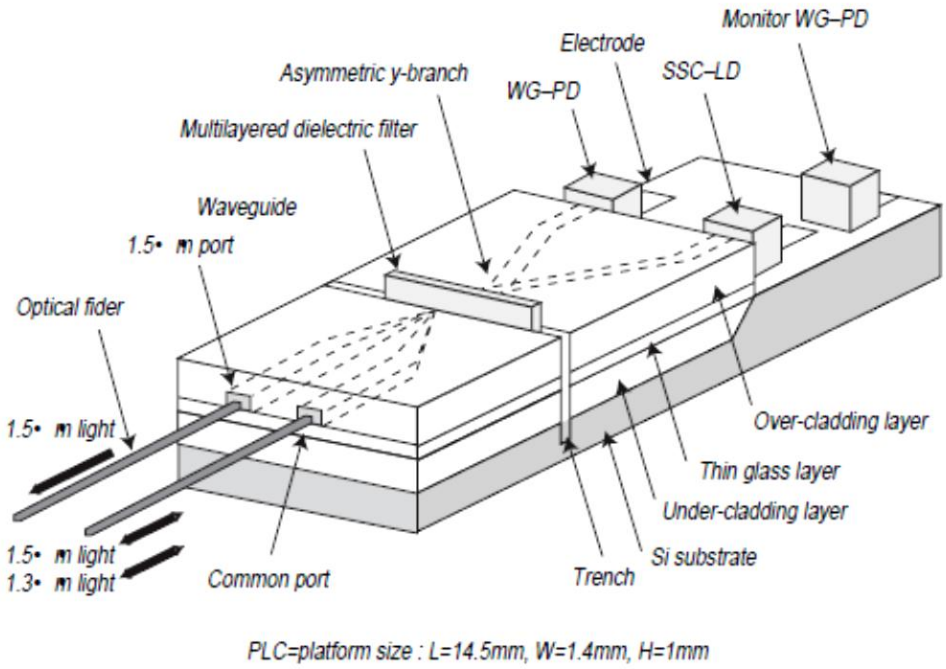

Figure 1- 7: Schematic of the silica-on-silicon PLC transceiver module, with a flip-chip bonded laser diode and photodetector [120].

Overall, although PLC technology is able to deliver low cost, fiber pig-tailed integrated photonic modules, it is basically a hybrid assembly method, mostly using flip-chip bonding to integrate lasers on a Si platform, and the dimensions and characteristics of it are far from the on-chip compact integration of laser sources on silicon ICs.

1.3.2. Si Based Detectors and Lasers

As an alternative to integration of III/V on Si, extensive efforts had been dedicated to fabricate optical components with Si itself, and thus remove the challenge for integration the first place. The photodetectors that are made on Si (mono material, thus no need for the integration of III/V components) mainly operate at short wavelengths (below 950nm) and suffer from low responsivity, low channel depth and slow speed. Introduction of Ge has brought the wavelength of the SiGe photodetectors to the telecom range and recently in-plane crystalline Ge detectors were developed [23] to increase responsivity and decrease material loss while being integrated on a CMOS chip.

Due to the indirect bandgap of Si (in contrast to the direct bandgap of GaAs and InP), light emission in Si has been a tough challenge. In order to detour this physical hurdle, a set of approaches had been suggested in order to emit light from Si, such as Raman lasers [24] and material engineered light emitting diode structures. In Raman lasers, pure Si crystal and an external laser source are required. In material engineering approaches, porous silicon [25], nano-crystalline silicon [26], SiGe quantum cascade structures [27], dislocation engineered Si [28], Erbium doped SiO_2 [29] and nano-pattering of Si [30] have been exploited for light emission. Most of these approaches need cryogenic temperatures to obtain lasing operation, and they do not fulfill the performance requirements of commercial applications like telecommunications and optical interconnects. Furthermore, lasing in Si, based on stimulated Raman scattering, requires an external optical pump source[3], which defies the purpose of compact integration of these lasers on IC chips. There has been recent progress in making Si/Ge room temperature lasers [31], but it is still work in progress.

In summary, having lasers made of Si (hence no need for integration), results in suboptimal components with non-optimized performances. In order to be able to separately

[3] The pump sources usually need to be high power, for instance 1.6W [32]. Such high pump powers not only increases power consumption which is a major concern in ICs, but also induces the nonlinear loss mechanism of two photon absorption (TPA). Introducing delay as well as using a short optical pulse had been helpful in reducing TPA [24].

optimize the performance of optics and electronics on a chip, it is very desirable to be able to optimize the photonic components based on III-V compound semiconductors independently from the Si CMOS VLSI circuitry.

Passive Si-based photonic integrated circuits are not of the main interest of this thesis, thus we only give one example of such integration. At McMaster University, M. Pearson, has shown monolithic integration of WDMs on Si in his PhD [33]. His work consists of design and fabrication of arrayed waveguide grating demutiplexers (AWG) on SOI, and SiGe MSM (metal-semiconductor-metal) photodetectors at 1.55μm, with a major emphasis on "low cost" feature of the developed fabrication technique. Three dimensional growth modes (undulating quantum well layers) where used to enhance the normally very low responsivity of SiGe photodetectors at 1.55μm. Finally the photodetectors are integrated with the waveguides as a demonstration of monolithic integration with any passive optical component. The cost effectiveness of the process primarily relies on the use of local oxidation of silicon (LOCOS) which enables Si microelectronics facilities to fabricate optical components with low change/cost. However optical sources hadn't been discussed in this work and thus this research still emphasizes the need for integration of III/V lasers to make a fully optically integrated circuit.

1.3.3. Epitaxial Growth of Compounds on Si Substrate

One widely explored approach to integrate optimized III/V optical devices on Si substrates is to heteroepitaxially grow optically active materials (e.g. GaAs), directly on top of Si. However, there are two fundamental issues with epitaxial growth of these optical materials on Si or Ge substrates. Firstly, heteropolar semiconductors, e.g., III-V's and II-VI's, are polar when grown along the (001) direction. This causes a polarity mismatch with the underlying group-IV substrate such as Si. Secondly, most existing optical materials and their alloys do not match the lattice constant of Si or Ge. Figure 1- 8 illustrates the bandgaps and the lattice constants for conventional semiconductor alloys that are used for optically active devices. It can be seen that most of the existing materials have either larger lattice constants or larger band gaps than of interest. They lie in the upper right-hand section of the graph. The desired region for viable compound materials for heteroepitaxial growth, on the other hand, is the intersection of the gray regions, to be lattice matched to Si (or SiGe) and to also provide operation at the wavelength of 1.5μm.

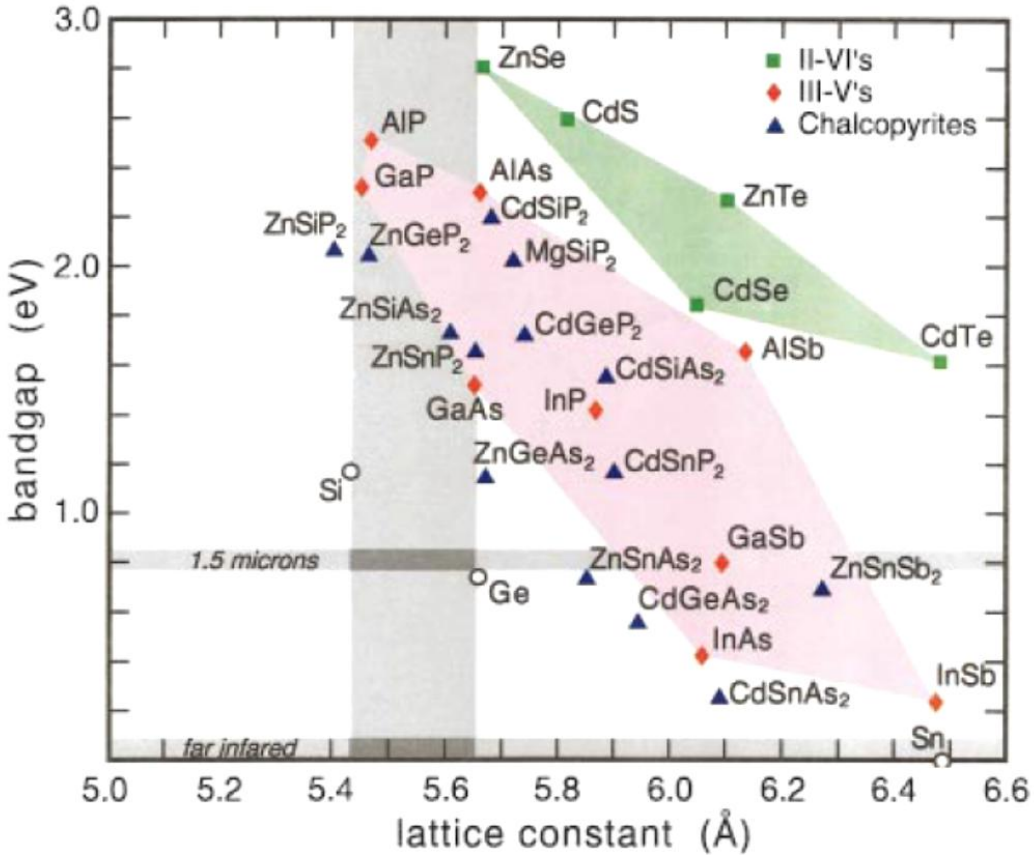

Figure 1- 8: Bandgaps and lattice constants for various traditional semiconductor materials. III/Vs are shown in red diamonds and II-VIs in green squares. The color shaded areas show possible alloyed materials and the gray regions correspond to lattice constants between Si and Ge, and bandgaps corresponding to wavelengths of 1.5μm and far infrared.

It can be observed from Figure 1- 8 that the III-V alloys that match the telecom operating wavelength (≈1.5μm) have lattice constants about 8% larger than that of Si[4], which makes it hard to grow these alloys defect free on Si substrates. This results in threading of misfit dislocation density of 10^8-10^{10} cm^{-2} when either of GaAs or InP are grown on Si [34]. Remedies like special surface treatment [35], low temperature buffers [36], growth on patterned substrates [37] and strained superlattices [38], [39] have been looked into to reduce dislocation density to about 10^5-10^6 cm^{-2}, which is still about two orders of magnitude higher than the case of epitaxial layers grown on native InP or GaAs substrates suitable for CW room temperature operation of III/V laser diodes.

More recently, SiGe [40] and GaSb [41] buffer layers have been employed to realize room temperature GaAs based CW laser diodes on Si, although their reliability remains to be

[4] More specifically compared to Si, GaAs and InP have 4.1% and 8.1% lattice mismatches respectively. Furthermore, the thermal expansion coefficient mismatch is 120.4% and 76.9% for these two materials versus Si.

a concern for practical applications [34]. Another promising approach is to exploit a strained Ge-on-Si layer, in which thermal tensile strain of Ge grown on Si makes the Ge bandgap closer to be direct and thus able to emit light through radiative recombination. Photodetectors [42], [43], [44], modulators [45], [46] and CW room temperature optically pumped Ge-on-Si lasers [31] were demonstrated using this technique. Further research is under way to fabricate an electrically pumped laser with the strained Ge on Si idea.

Although exciting research to realize optical gain on Si based substrates is underway, the problems of polarity and lattice mismatch make it very difficult to create optoelectronic integrated devices using heteroepitaxy.

Equally important as the problem of lattice mismatch of III/Vs and Si, is the different thermal expansion coefficient of these materials, which will persist even if layers with matching lattice constant are deposited on the Si substrate.

Therefore, in general the devices made with epitaxial growth of III/Vs on Si, suffer from short lifetimes and low efficiencies due to the problems mentioned above. In addition, the Si CMOS can get damaged by the relatively high temperature growth process [13].

Along the line of attempts to heteroepitaxially grow III/V materials on silicon substrates (the drawbacks of which were discussed earlier), Prof. Joannopoulos group at MIT has been looking into devising new material systems that address lattice mismatch and polarity issues of growing conventional III/Vs (GaAs, InP, etc.) on Si. In [47] they have shown that $(ZnSi)_{1/2}P_{1/4}As_{3/4}$ is a suitable compound that is lattice matched to Si and has a direct bandgap of 0.8eV, which corresponds to the canonical wavelength of 1.5μm, the desired wavelength in optoelectronic applications. They have shown the computational design of the material system and investigated its physical properties using both ab initio total energy and quasiparticle GW calculations.

Furthermore, O. Kwon had looked into the monolithic integration of III-V optoelectronics on Si in his PhD thesis [48] at Ohio State University. In his work he tried to overcome the obstacles of heteroepitaxial growth of III/Vs on Si substrate with the use of graded SiGe relaxed buffers. These buffers result in a low threading dislocation density for the relaxed Ge over large area Si substrate, which makes device quality GaAs components feasible on Si. Kwon first shows the implementation of a visible light QW LED made in GaAs on a Ge substrate. Also, quaternary alloy MBE deposition of the AlGaInP compound for wavelength of 600nm was studied, making fabrication of their second generation surface

emitting AnGaInP resonant cavity LEDs possible on a relaxed SiGe/Si substrate. And finally, stimulated emission was achieved in room temperature strained AlGaInP visible laser diodes on a relaxed SiGe/Si substrate, the third generation of devices in his work. Therefore, if hurdles of growing extremely high quality heteroepitaxial III/V layers and SiGe buffers can be overcome, Kwon's work has shown a potential for optoelectronics integration with this approach. One caveat here is the fact that such approach takes advantage of very close lattice constants of GaAs and Ge, however InP based compounds are not that easy to be integrated on Si with this method of epitaxial growth, as the lattice constant of InP is 3.9% different from GaAs and Ge[5].

1.3.4. Bonding III/V wafer to Si host IC

Another approach to photonic integration had been to bond a photonic III/V device wafer on a Si CMOS wafer in a post-fabrication integration step[6]. Wafer bonding is an option which uses high pressure and temperatures to bond the compound semiconductor wafer to the host Si substrate. One drawback of this technique is the mismatch of Si and III/V wafer sizes. A second issue arises since the required density of photonic elements is generally not the same as the one for Si integrated circuits. Therefore, only a very small fraction of the bonded III-V wafer is being used for making photonic devices, which translates to loosing the majority of the relatively expensive compound semiconductor wafer. These types of losses and costs are not tolerable for commercial low cost components and hence the industry would avoid such techniques to be put into production[7].

Based on this technique, a promising approach which is recently pursued with a great deal of enthusiasm, revolves around the bonding of an active region III/V wafer on top of a Si ridge waveguide fabricated on an SOI host wafer. Based on this Si-Hybrid idea, researchers at University of California Santa Barbara joint with Intel have developed a library of photonic active components from detectors to modulators and lasers [49]. Since this approach will be discussed in detail and its pros and cons will be looked into in Chapter 2, further details will not be repeated here and the reader is encouraged to follow the discussion regarding this approach to integration in the next chapter.

[5] Lattice constants of Ge, GaAs and InP are: a_{Ge} = 5.6461 Å, a_{GaAs} = 5.6533 Å, and a_{InP} = 5.8686 Å [50].
[6] This approach is also the essence of recently proposed Si-Hybrid integration technique developed by Intel/ UCSB for photonics integration.
[7] In Chapter 2, a full investigation of Si-Hybrid approach by UCSB/Intel will be detailed and the strengths and weaknesses of this integration technique will be discussed in depth.

Along the same lines of integration via III/V wafer bonding to a Si host wafer pursued by UCSB and Intel [49], researchers at Ghent University in Belgium have demonstrated a micro-disk laser integrated on Si with an adhesive bonding process using BCB (benzocycobutene) [51]. The schematic of the micro disk laser and the adjacent Si waveguide which carries out the evanescently coupled laser light is shown in Figure 1- 9. The Si waveguide is 500nm wide and has a thickness of 220nm. The laser disk is 580nm thick and 7.5μm or 10μm in diameter. Room temperature CW lasing operation with threshold current of 350μA is observed at 1554nm, and maximum coupled power to the outgoing fiber is measured to be 38μW with 4mA of drive current. Considering the efficiency of grating couplers placed on both sides of the Si waveguide, the maximum power coupled to the waveguide is estimated to be 120μW. Due to low thermal connectivity of the laser, excessive heating had been noticed in earlier generations of these micro-disk lasers and thus a thick (compared to the thickness of micro-disk itself) layer of gold (600nm) is deposited on the top contact of the micro-disk to function as a heatsink.

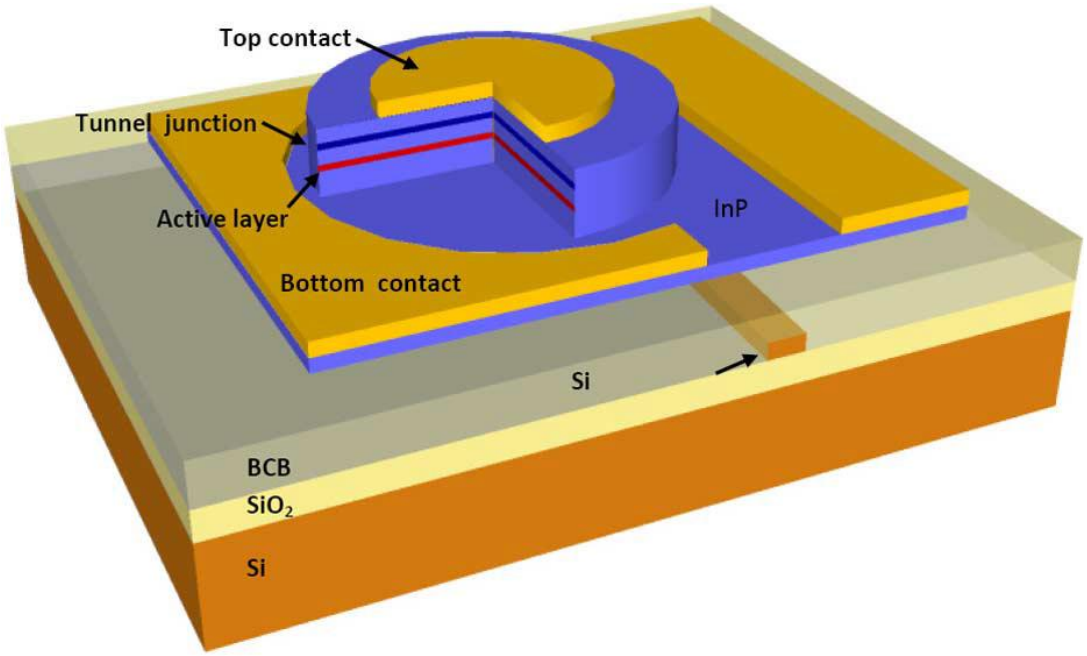

Figure 1- 9: Schematic of MDL (micro-disk laser) which is heterogeneously integrated with Si waveguide on an SOI substrate [51].

Also, in order to avoid InGaAs p-contact absorption losses and still achieve a good p-type contact in its absence, a tunnel junction is used instead. Quantum wells are made of InAsP and the epitaxial layer sequence is deposited on an InP substrate which is removed

subsequently. In another generation of these MDLs, for wavelength tuning purposes, a heater ring is fabricated around the laser disk with tuning rate of 0.31nm/mW.

Overall the output power of such micro-disk structures is quite low, and although the threshold currents are small, the power consumption per bit is about 400fJ/b [51] which needs to be further improved to reach the 100fJ/b target.

Similar to the micro-disk lasers discussed above, the research group at UCSB/Intel has also made micro-ring lasers [52], [53] with the same integration concept of bonding III/V to Si wafers. Figure 1- 10 show this micro-ring laser bonded on an SOI wafer and coupled to a Si waveguide which terminates with two integrated tapered photodetectors made with the same Si-Hybrid technology. These micro-ring lasers have InAlGaAs-based active region, InP claddings and have diameters ranging from 15µm to 50µm which allow compact integration of a large number of these lasers on chip [34]. In Figure 1- 11 the simulated mode distribution of same micro ring structure along with the adjacent Si waveguide shows that the mode is shifted to the outer area of the micro ring due to the presence of Si waveguide [34].

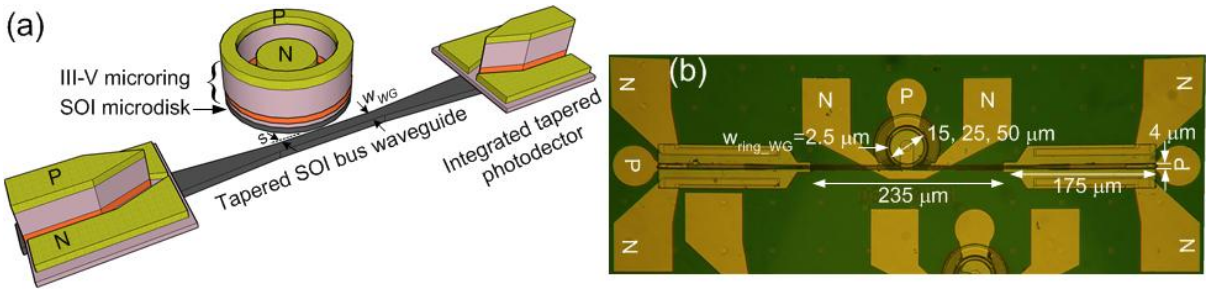

Figure 1- 10: (a) Schematic and (b) top-view microscopic image of hybrid silicon micro-ring laser with two integrated photodetectors [53].

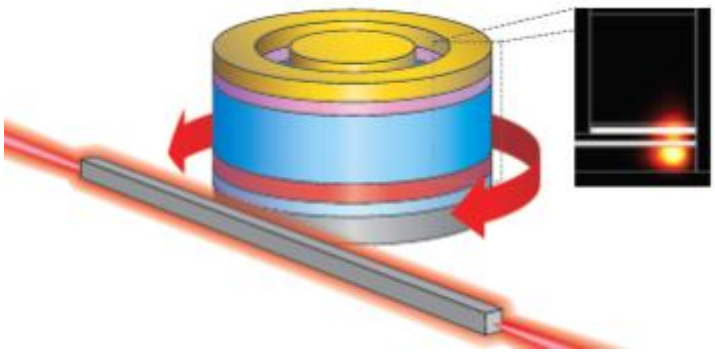

Figure 1- 11: Schematic of a Hybrid micro-ring laser with the adjacent Si bus waveguide [34].

A 50μm diameter micro-ring laser fabricated in this approach, and with a waveguide spacing of 250nm, shows CW lasing operation with minimum threshold of 5.15mA at 10˚C and with maximum operating temperature of 65˚C [53]. The Si-Hybrid approach will be further discussed in Chapter 2.

1.3.5. III/V Substrate Removal

Another possible approach is to remove the III/V substrate prior to bonding of the devices to the VLSI substrate (similar to the approach demonstrated in this thesis). The photonic devices are then aligned and bonded to the host substrate with various techniques such as transparent transfer diagram [54] or the pick and place assembly technique used in this thesis. Among the advantages of this approach are achieving a virtually "planar" hybrid integrated optoelectronic circuit as well as access to front and back device contacts, vertical scalability of stacked thin film devices, and the ability of mixing and matching the individually optimized multiple optoelectronic devices integrated with microelectronic circuits using the mainstream microfabrication processing techniques. The only drawback of this integration approach is that the cost is transferred to the assembly phase, which is more or less addressed by the semiconductor industry [13].

The following few examples are among other attempts to photonic integration, which did not perfectly belong to the subsections above. Therefore they are presented here separately.

Louderback et al have presented a monolithic VCSEL-based photonic integration on GaAs in [22]. Essentially, with the use of diffraction gratings, the suggested device structure enables the optical output of the VCSELs to be coupled to an internal horizontal waveguide, and the optical signal in the waveguide is tapered off to resonant cavity detectors. More specifically, as shown in Figure 1- 12, a waveguide is placed within the top DBR of the VCSEL structure and the thicknesses are chosen such that the waveguide layers are in phase with the vertical cavity. Then a diffraction grating is etched into the GaAs waveguide core to couple vertically oriented light bidirectionally into the horizontal waveguide. Therefore in Louderback et al work, by integration, mainly the conversion of VCSEL vertical light to horizontal optical waveguides is meant, and the substrate is GaAs, not a Si IC.

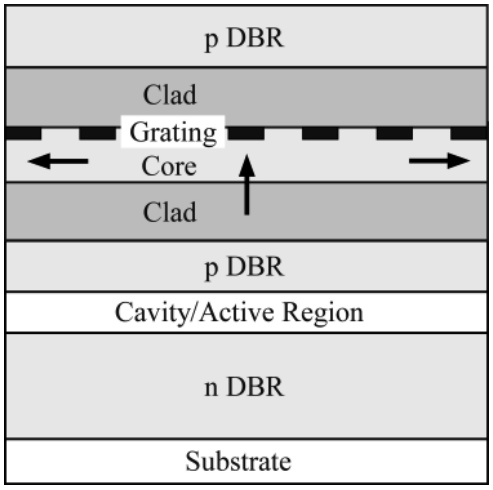

Figure 1- 12: Schematic of the structure of the waveguide-coupled VCSELs demonstrated in [22].

In an attempt to integrated photonic components on MEMs devices, a thin film double heterostructure AlGaAs/GaAs p-i-n diode is integrated on a polyimide micromachined platform on silicon by Wilkinson et al in [55]. The objective is that, having optoelectronic devices integrated on movable MEMS actuators can provide micro scale on chip active alignment when high precision alignment of optical emitters/detectors with the rest of the components is required.

In another set of efforts in this field, M. Adams at CalTech has devoted his PhD thesis [56] to use optoelectronics integration for biological and chemical sensing applications. In his work, the goal of achieving a lab-on-chip system, that replaces the cumbersome external interrogation microscope setup, is looked into. The system with the use of integrated lasers and detectors is capable of performing optical analysis both outside of the flow cell a well as directly inside the flow channel. In order to make the integration feasible, modeling, fabrication and the performance of different approaches like the use of CMOS imagers and spectroscopy, the effect of vertical cavity enhancement and photonic crystal lasers (also illustrated in depth in [57] from the same group) have been investigated. As other integrated microfluidic components, soft lithography which uses a silicone based elastomer had been used in fabricating the prototypes. As one may expect, the presence of an integrated light source is a key in making this lab-on-chip idea a reality. With that, the integrated CMOS circuitry not only can detect change of index of refraction of a flow, but also perform analysis on molecular level, as well as study other phenomena like multiphoton generation, optical trapping and Raman processes. Although the vertical cavity approach did not perform as

expected, the attempt shows a large range of applications of integrated optoelectronics in biofluidics as well.

Overall, as reviewed briefly here, the breadth and amount of effort that is devoted to photonic integration on Si demonstrates the importance and vitality of the availability of a reliable, low cost, and monolithic technology for integration of lasers on Si ICs. However, a robust and modular technique that fully answers the requirements of industry for commercial applications is yet to be developed. We believe that the coaxial recess integration approach that we're demonstrating in this thesis is a very promising solution to photonic integration on Si and while not suffering from the issues of other approaches, it is also modular, low cost, CMOS-compatible and has a small footprint on chip. In the following section the basics of this approach will be introduced.

1.4. Our Approach to Photonic Integration on Si

Considering the limitations of aforementioned approaches to photonic integration, we propose the coaxial integration technique which proves to be highly modular, flexible, and robust providing very compact, monolithic and planar integration of photonics on silicon ICs[8].

The schematic in Figure 1- 13 shows the general concept of this approach, in which emitted light from an edge-emitting laser diode is coaxially coupled to a dielectric waveguide fabricated on an integrated circuit chip.

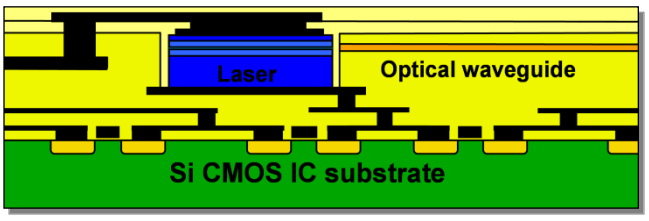

Figure 1- 13: Schematic of the coaxially coupled integration approach in which light emitted from a III/V laser bonded in a recess on chip is coaxially coupled to an outgoing waveguide.

[8] J. Perkins has demonstrated recess integration of VCSEL laser diodes on silicon Integrated Circuits [58] earlier in our research group. In the current thesis such recess integration technique is used for integrating in-plane laser diodes that are coaxially coupled to waveguides fabricated on Si chips.

More specifically, in this project the integration of 1.55µm InGaAs/InP in-plane edge-emitting laser diodes in recesses etched into the SiON/SiO_2 dielectric waveguides fabricated on silicon is demonstrated. The active region of the laser diode platelet is coaxially aligned with the silicon oxynitride waveguide core, to ensure the highest coupling between the two. The schematic in Figure 1- 14 depicts the idea of this integration approach, where light from III/V laser diode is coaxially coupled to on-chip optical waveguide on silicon. The laser back-side n-contact is brought to the wafer front side through a bonding layer that also ensures a strong mechanical bond of the laser platelet in its recess.

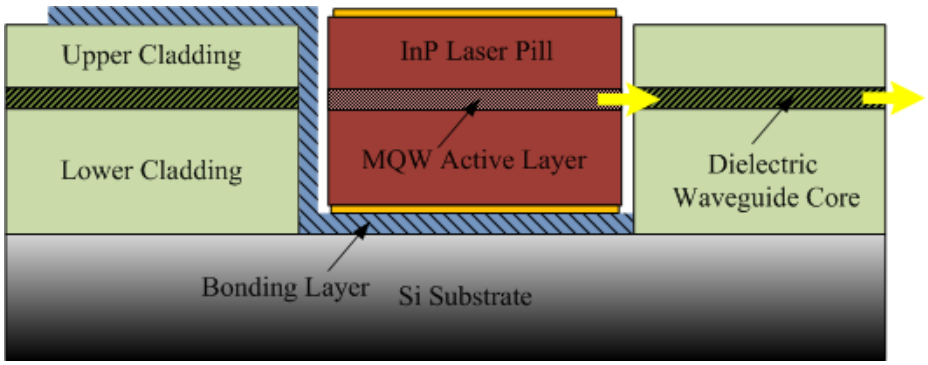

Figure 1- 14: Schematic showing the coaxial integration of edge emitting laser platelets in SiO_2 recesses on Si substrate.

In order to make the coaxially coupled integration approach feasible, previous PhD theses have solved different aspects of this integration. More specifically, E. Barkley has focused his PhD thesis [59] on the fabrication of SiON waveguides and etching the 6 to 7µm deep recesses in their path, and J. Rumpler made an impressive contribution by fabricating micro-cleaved edge emitting laser platelets with dimensions of 300µm×150µm×6.3µm, in his PhD thesis [60].

Having these two components on hand, in this thesis, the integration process is demonstrated and optimized.

1.5. Thesis Flow

In Chapter 1, the importance of optical interconnects and their gradual industrial adoption from long-haul all the way to rack-to-rack interconnects over that past few decades has been reviewed. With that view in mind, the importance of having on-chip monolithically

integrated sources to bring such application more into computer.com arena, is clear. Therefore, different approaches to realize integrated lasers on Si, ranging from Raman lasers to heteroepitaxial growth of III/V material on Si, and Evanescent-Si-Hybrid approach were presented and discussed. Finally, our proposed integration approach which we believe solves the issues with aforementioned methods was briefly described.

In Chapter 2, the promising integration approach of Evanescent-Hybrid-Si is discussed in further detail and a suggestion to reduce bend diameters in the large footprint race-track structure is made and its effect is simulated using the BeamPROP software. Then the Hybrid-Si and Coaxial integration approaches are compared and pros and cons of each approach are listed so that based on each application, the most suitable approach can be adopted.

In Chapter 3, design and optimization efforts to find the best dimensions and refractive index for dielectric waveguides used in our coaxially integration approach, as well as the optimized gap filling index is presented. Also, Distributed Bragg Reflectors (DBRs) were designed through three different methods of Finite Difference Time Domain (FDTD), Transmission Matrix Method and Bi-directional Beam Propagation Method (BPM) to provide higher reflectivity external mirrors for the laser cavity.

Since the integration method demonstrated in this thesis highly relies on the two key components of InGaAs laser platelets and dielectric waveguides fabricated on Si substrate, the fabrication of these two components which had been done by two former PhD candidates in our research group (E. Barkley [59] and J. Rumpler [60]), is discussed in Chapter 4 for ease of referencing on how these components were made.

In Chapter 5, the details of the integration process demonstrated in this thesis are explained. Also the process to accurately characterize the dimensions of the formerly fabricated dielectric waveguides is described, which is of paramount importance in ensuring best vertical alignment between laser active region and dielectric waveguide core. Furthermore, the bonding layer composition optimization, deposition and pattering is discussed. The discussion is followed by explaining the procedure for the assembly of laser platelets in recesses, as well as the pressure bonding mechanism. By the conclusion of Chapter 5, laser platelets are successfully integrated in recesses on a Si substrate, well aligned to dielectric waveguides, and are ready for measurement and characterization of the full integrated structure.

In Chapter 6, the detailed measurements of these integrated lasers for pulsed and continuous wave electrical drive is presented as well as IR images of the beam shape leaving

the chip. The spectrum of CW lasing of the integrated lasers is studied and a significant enhancement to mode suppression ratio is observed. A three-mirror cavity model is presented and good agreement between calculated MSR and the measurement results is achieved. Furthermore, external quantum efficiency and characteristic temperature for the integrated lasers are extracted from the measurement results. Finally, a number of explored approaches with the goal of quantifying the coupling losses in laser-waveguide facet are presented and the results are discussed.

Lastly, in Chapter 7, the discussion on the strengths and limitations of the coaxial integration approach is presented and suggestion are made on how to improve the current generation of the components, considering the desired features of single-mode operation, full CMOS compatibility, low cost, and being fab-less, which help in commercializing an approach by the industry.

Chapter 2

Assessment of Hybrid Evanescent Approach to III/V-Si Integration

As mentioned in the first chapter, one approach to photonics integration is to fabricate light emitting components in III/V or II/VI compound material systems and then integrate those active components on a Si substrate.

To achieve this integration step, there are a couple of approaches such as flip-chip bonding, coaxial coupling and vertical coupling of membrane devices[1]. Being concerned with the need for sub-micron alignment to ensure efficient coupling, and time and cost intensive nature of it, scientists at UCSB and Intel have proposed Hybrid Evanescent technology to address the requirement of sub-micron alignment of other integration approaches[2].

We were interested in understanding the Intel/UCSB approach and its strengths and weaknesses, particularly in comparison with the coaxial coupling approach being pursued in

[1] Hattori et al. have fabricated membrane disc lasers vertically coupled to a passive Si waveguide [123]. In this approach, alignment reduces to two dimensions, but still an important issue.

[2] In fact our proposed coaxial approach does not impose the need for costly active/passive submicron alignment. Since both laser pills and wells are 150μm in width, horizontal alignment is usually very well obtained. By the same token, there is no room for the lasers to have rotational misalignment either. As it will be discussed in Chapter 5, the bonding layer thickness is carefully optimized to ensure the best vertical alignment. The only remaining factor left for the human/automated assembler to care about is the gap length. Since the laser have a ±1.2 variation in length depending on where lasers cleave in the notch area using micro-cleaving approach, therefore in the experimental phase of this research a series of wells with various lengths were fabricated on chip, thus the user had flexibility to choose which well will fit the picked up laser the best. This can be efficiently done by either a human user or an automated process. Once the laser is assembled in the well, before breaking the vacuum, the micropipette (used for pick & placing the laser pills) can be used to slide the lasers to one facet of the recess for the highest coupling to that waveguide. Therefore the alignment issue is not a big hurdle by the nature of our approach.

our group at MIT. Therefore, through optical simulations with the BeamProp software, power losses due to evanescent coupling transitions were investigated. Our goal was to see how much scattering and reflection is caused when the optical mode inside a silicon waveguide is coupled vertically to a III/V gain stack, and when it couples vertically back to the silicon ridge waveguide. Our simulation results have shown that unless a well designed taper is used[3], an insertion loss of almost 20% in power is seen in the transition between Si/Hybrid/Si waveguides.

In addition to discussing the simulated results obtained using the beam propagation method to model insertion loss and scattering at Hybrid/Si interfaces, this chapter will also look into other pros and cons of Hybrid Evanescent Vertical Coupling approach. Finally, the two integration methods, i.e. the coaxial recess integration and Si-Hybrid approaches, will be briefly compared with respect to heat transfer, coupling loss, spatial footprint in chip, reliable manufacturability and mechanical endurance, aligning, monolithic integrability with other components on chip, and industry requirements on device characteristics like threshold current limit.

2.1. A Review of the Hybrid Evanescent Approach

Since the simulations presented later in this chapter are focused on characterizing the transitions in Hybrid Evanescent integration, it is essential to first give an introduction to the basics of this approach and the structure of the devices made using this technique. Therefore in the following, a review is given while trying to keep the content concise.

The idea behind the Hybrid Evanescent approach is that the optical mode inside a silicon ridge guide is evanescently coupled[4] to a III/V stack bonded on top of it and thus sees

[3] In further developments of the Hybrid Evanescent Coupling technique, an amplifier with integrated photodetectors was fabricated using this approach [70], in which tapers had been used to couple light from III/V active region to the passive Si-ridge area preceding the photodetector. In that case the taper loss is estimated to be in the range of 0.6-1.2dB, which is comparable to the 20%≈1dB loss that our simulations have shown for the reflection/scattering loss should an abrupt transition had been used. Thus the taper does not entirely address the problem of the mode's hardship in coupling back from high index III/V stack to lower index Si-ridge guide.

[4] While in initial publications on this technique, the term "evanescent" had been emphasized, it was dropped for later developments on the project. The latter seems to suit the reality of the structure more, as the mode shape is shared between the Si-ridge and III/V stack, with more concentration of the guided mode on either of these two

gain [61]. This technique has been used to fabricate the following range of devices [49] showing the flexibility of this approach in realizing a series of active photonic components.

- Optically pumped AlGaInAs-Si Fabry Perot laser [62]
- Electrically pumped AlGaInAs-Si Fabry Perot laser for λ=1550nm [63]
- Electrically pumped AlGaInAs-Si Fabry Perot laser for λ=1310nm [64]
- Hybrid Evanescent Photodetectors [65]
- Race-track laser for λ=1550nm integrated with two monitoring photodetectors [66]
- Fabry Perot mode locked laser (with saturable absorber region) for λ=1550nm [67]
- Race-track mode locked laser [68]
- Optical amplifier integrated with photodetectors [69], [70]
- Electroabsorption modulator [49]
- Microring laser [52], [53]
- AWG based multiwavelength laser [113]
- DFB laser array using quantum well intermixing [114]

Beside the initial introduction to the fabrication steps of this approach (which is mostly common among the devices above), when it comes to reviewing specific fabricated devices, the focus will be primarily on the lasers i.e. Fabry Perot cavity and race-track lasers since our major interest is in integrated laser diodes. The details about the rest of the devices listed above can be found in the corresponding references.

2.1.1. Fabrication Process in Hybrid Evanescent Approach[5]

In this technique an InP wafer[6] (containing AlGaInAs QWs) is bonded to an SOI wafer which includes Si ridge passive waveguides. Bonding is done via low temperature O_2 plasma assisted wafer bonding. The low temperature prevents two wafers from cracking due to the mismatch between the thermal expansion coefficients of Si and InP (i.e. direct wafer bonding at 600°C cannot be used).

The schematic in Figure 2- 1 helps in visualizing the sequence of layers and how the III/V and Si substrates are bonded to make an electrically pumped laser structure.

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depending on the width of the Si-ridge. Therefore one cannot really call the structure evanescently coupled (unless there are abrupt transitions like what we looked into later in this chapter), as in later publications the mere term of "Hybrid on Si" had been adopted. Nevertheless since this approach is mostly recognized in the photonic integration community with the initial "Hybrid Evanescent" title, the same term was used in this chapter.

[5] The material presented in this section has been adopted from references [61]-[63].

[6] In general the optimum size of III/V material to use depends on the required density of integrated active III/V devices on Si [72].

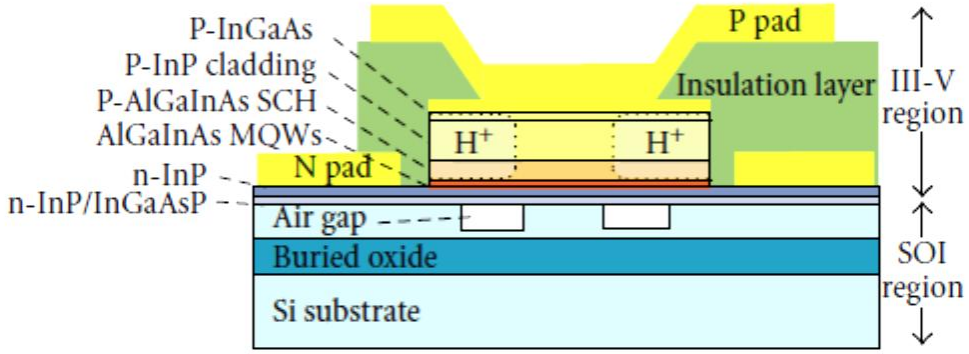


Figure 2- 1: Cross section of a Hybrid Evanescent device structure. Note that in the refined more recent developments of this approach, wide III/V mesas (12-14μm) are used for lasers and amplifiers to increase mechanical reliability of the bond and improve heat transfer, whereas narrow mesas (2-4μm) are used for detectors and modulators to decrease capacitance, for high speed performance [49].

In terms of processing, first a Si waveguide rib formation is done in RIE plasma of Cl_2-HBr-Ar where a thin layer of SiO_2 is used as hard mask. Then, both wafers are cleaned with Acetone, Isopropanol and DI water rinse followed by dipping in buffered HF for the SOI wafer and in NH_4OH for the III/V epitaxial wafer. Then the two wafers are bonded using Oxygen Assisted Plasma in which a very thin oxide layer (<5nm)[7] is generated (in the RIE chamber) whose surface is very smooth and chemically reactive. The wafers surfaces are then placed in physical contact at room temperature. The process is followed by a low temperature anneal (300°C), with applied pressure of 1.5MPa for 12 Hours. The low temperature bonding process is CMOS compatible and preserves the quality of the III/V material.

After the bonding is complete, the InP substrate is removed using HCl, and then the III/V mesa structure is defined using CH_4/H/Ar-based reactive ion etching of the p-type layers. Subsequent etching of the QW layers until the n-type layers is done with H_2O:H_2O_2:H_3PO_4 (1:1:38). Then the n-type (Ni/AuGe/Ni/Au) contacts are deposited and pattered on the exposed n-type layers, and the p-type contact (Pd/Ti/Pd/Au) is patterned on the center of the mesas. For electrically pumped laser and amplifiers, the p-InP mesa is implanted so that a 4μm current channel is formed at the center to prevent current spreading.

Finally, dicing, facet polishing, and characterization are performed and facets are coated with broadband high reflection coating (80%) consisting of three periods of SiO_2-Ta_2O_5.

[7] It is stated that "Bonding oxide at interfaces is so thin that does not alter the optical mode at 1.55μm" [61]-[63].

2.1.2. Layer Sequence in Hybrid Evanescent Structure

Regarding the layer structure (see the schematic in Figure 2- 2), a Si-ridge guide is fabricated on a lightly p-doped (<2×10^{15}) SOI substrate whose 1µm SiO_2 functions as the lower cladding for the Si waveguide. The dimensions of the Si ridge waveguide are D=0.6µm (ridge height), H=0.7µm (ridge plus substrate height), W=[1 to 5µm] (ridge width). The III/V stack consists of two periods of InP/1.1µm $In_{0.85}Ga_{0.327}As_{0.673}P$ superlattice (7.5nm thick alternating layers of InP-InGaAsP to inhibit the propagation of defects from bonded interface to the QW region), then a 110nm InP spacer, and a 50nm unstrained 1.3-µm $Al_{0.131}Ga_{0.34}In_{0.528}As$ SCH layer to increase pump power absorption and carrier flow into QWs followed by strain compensated AlGaInAs QWs (five 7-nm $Al_{0.055}Ga_{0.292}In_{0.653}As$ QWs with compressive strain (0.85%), 10-nm $Al_{0.089}Ga_{0.461}In_{0.45}As$ barriers with tensile strain (-0.55%)) (barrier bandgap:1.3µm)), 500nm of unstrained 1.3µm AlGaInAs SCH, and then an InP upper cladding layer.

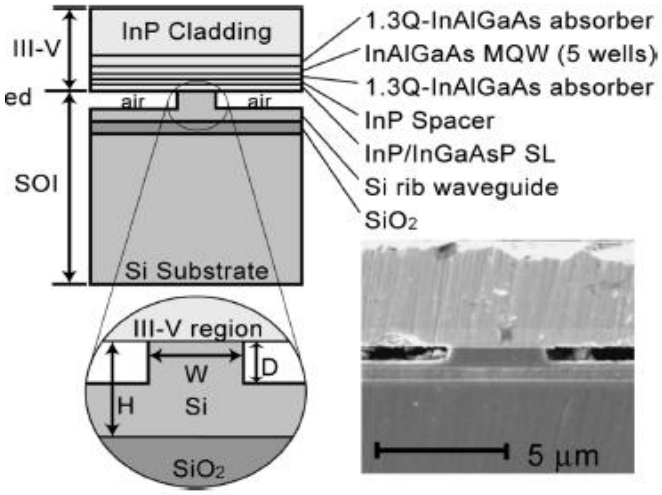


Figure 2- 2: Hybrid Evanescent technology laser structure (consisting of Si ridge waveguide and bonded multi layer epitaxial III/V stack on top) [62].

2.1.3. Optical Mode Distribution in Hybrid Evanescent Approach

In order to get a better understanding of the basics of Hybrid Evanescent technology, it is very useful to look into optical mode distribution vs. Si ridge waveguide dimensions. Essentially the larger the Si waveguide ridge the more concentrated the optical mode in the ridge becomes. Equivalently, as the Si ridge gets smaller, more and more of optical mode is coupled to the III/V stack. Having this effect in mind, there is a tradeoff in choosing the width of the Si ridge: a small width is preferred to deliver enough gain to reach lasing

threshold, while a large Si ridge gives the highest confinement of the optical mode in the Si waveguide for efficient coupling to incoming/outgoing passive Si waveguides.

In Figure 2- 3, the calculated mode profile is shown for several Si waveguide widths in fabricated devices. The waveguide height (H) is 0.7μm, the rib etch height (D) is 0.6μm and the waveguide widths are 1μm, 1.5μm, 2.5μm and 3μm. In Figure 2- 4, the measured optical profiles for different waveguide dimensions are depicted.

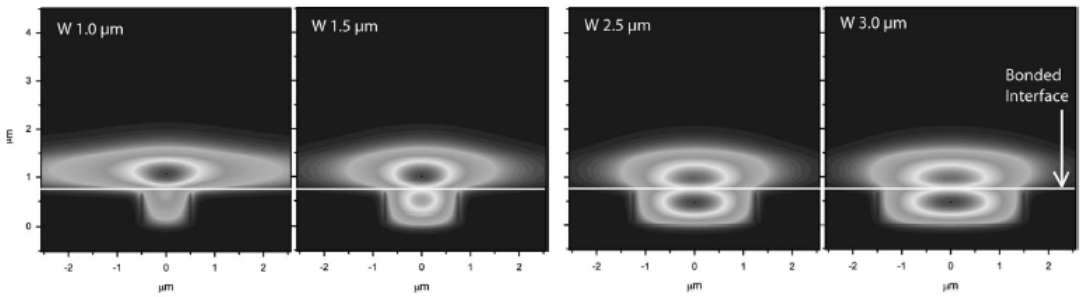


Figure 2- 3: Calculated optical mode profile [62].

(H=0.7μm, D=0.6μm for all cases, and W=1μm, 1.5μm, 2.5μm and 3μm from left to right.)

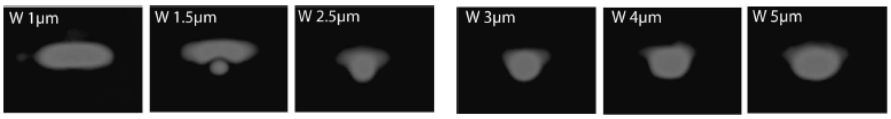


Figure 2- 4: Measured optical mode profile for W=1-5μm [62].

Confinement factors of the optical mode in the QW and Si waveguide were calculated with the BeamProp software. In Figure 2- 5, the relationship between Si-guide width and optical mode overlap with the Si-guide and QWs is illustrated. For dimensions of H=0.7μm, D=0.6μm and W=1-5μm, the confinement factors vary in ranges of Γ_{Si}=5% to 41%, and Γ_{QW}=5.1% to 4.1% for the different widths. The narrower the Si-guide width, the higher the coupling to the QW (thus higher gain) and the lower the mode overlap with the Si-ridge guide (therefore lower coupling to subsequent passive integrated devices on chip). This poses a tradeoff in choosing a suitable width for Si-ridge waveguide in this structure.

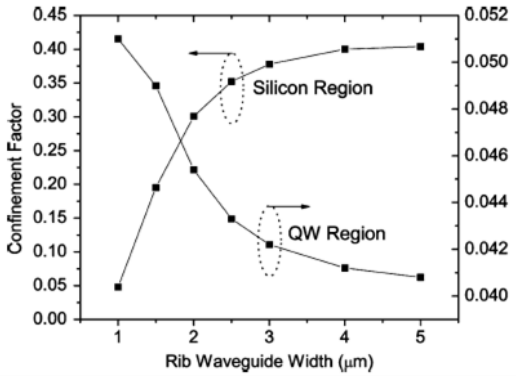


Figure 2- 5: Γ_{QW} and Γ_{Si} versus Si ridge widths [62].

The coupling from the fundamental mode of the Si passive waveguide to each mode of the Hybrid waveguide was calculated using FIMMWAVE [65]. The results are shown in Figure 2- 6. This information will be used later on to quantify the total insertion loss that the fundamental Si-guide mode sees in a Si-Hybrid-Si transition.

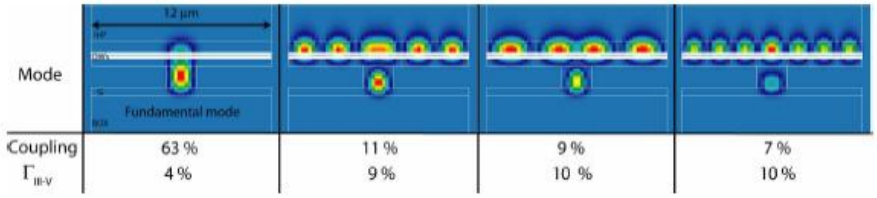


Figure 2- 6: Calculated coupling coefficient of the Si-guide fundamental mode to each of the Hybrid waveguides modes using FIMMWAVE [65].

Through fabricating optically pumped lasers with the Evanescent Hybrid approach [62], threshold variation with different Si-ridge sizes was observed (Figure 2- 7) which shows the tradeoff between the modal gain and loss for different ridge widths in these lasers. The reason is that material loss in Si is an order of magnitude less than the loss in III/Vs at 1.5μm. Therefore narrow stripes experience high gain but also high modal loss, while wider stripes experience less modal gain yet less modal loss. In such a tradeoff, a width equal to 4μm gives the lowest threshold power.

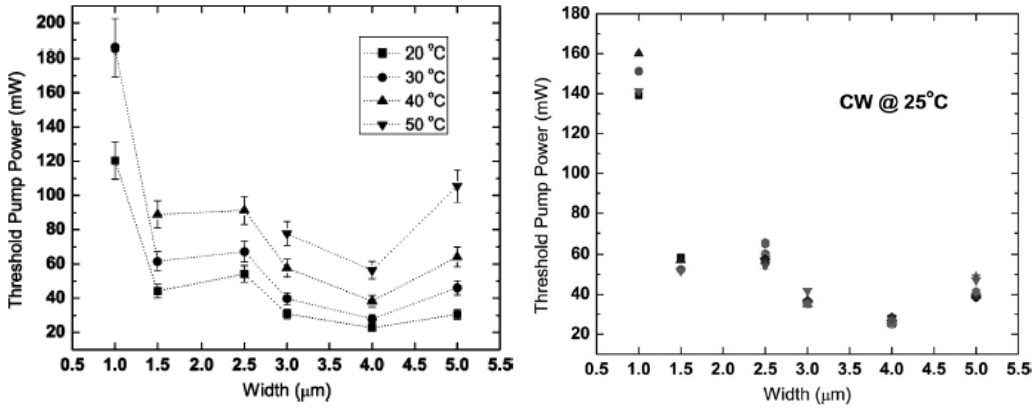


Figure 2- 7: Threshold pump power versus Si ridge guide width [62].

It is found that the yield of these devices has a direct correlation with the Si-ridge width in the fabricated devices [62]. Wider width ridge samples (≥2.5μm) have acceptable yields, whereas the yield is much lower for narrower stripes due to bond delamination during polishing [62]. This poses a major concern since smaller widths (≤2.5μm) are necessary to achieve single mode operation [63], [49].

2.1.4. Fabry Perot Cavity Electrically Pumped Laser

From the observations made from the optically pumped laser [62], an electrically pumped Hybrid Evanescent laser was fabricated [63], in which the Fabry Perot cavity is defined by dicing through the ends of the waveguides[8]. Again, the main idea is that the optical mode can obtain electrically pumped gain from the III/V region while being guided by the underlying Si waveguide. In Figure 2- 8, the evanescently coupled laser structure is illustrated in which carriers injected from the electrodes are recombined in the III/V active region and photons are emitted as a result. This will amplify the optical mode which is guided by the Si ridge waveguide underneath.

The laser structure is fabricated on top of a 2μm thick SOI layer and the Si guide has dimensions of H=0.76μm and W=2.5μm. Calculated overlaps of Γ_{QW}=3% and Γ_{Si}=75% are reported. The fabrication process is similar to what was reviewed earlier. The cavity of these lasers is defined by dicing through the Hybrid waveguides and then polishing the facets. Each laser has a length of 800μm. Figure 2- 9 shows an array of 36 lasers (left) and SEM image of the cross section of the laser (right). These fabricated lasers have shown CW operation with

[8] Therefore these Fabry Perot lasers are not integrable with other components on chip. In fact, this turns out to be a major issue with the Hybrid Si Evanescent Coupling approach. Only ring laser structures made with this technique [66] are integrable; although they propose their own issues of unstable mode hopping between clock wise and anti clockwise propagating modes in the laser loop for high currents above threshold.

I_{th}=65mA[9], $P_{out-max}$=1.8mW, η_d=12.7%, T_{max}=40°C, T_0=39K and a series resistance of 7.5Ω [63].

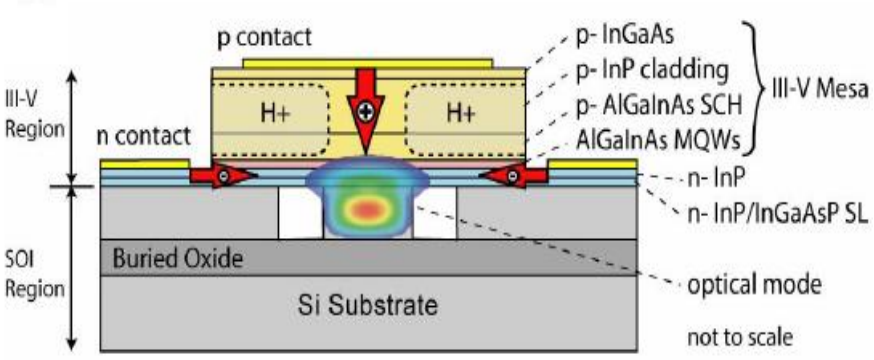


Figure 2- 8: Electrically pumped Hybrid Evanescent laser. Optical mode is mainly carried by the Si-ridge guide and is amplified by the stimulated recombination of pumped carriers in the III/V stack QWs [63].

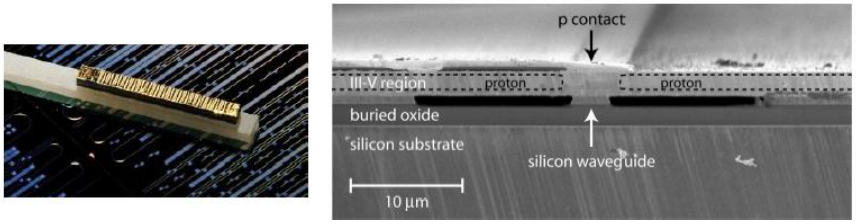


Figure 2- 9: Array of 36 lasers (left) and the SEM image of the cross section of a Hybrid Evanescent electrically pumped laser (right) [63].

In characterizing these devices, a modal loss of 15 cm^{-1} is measured and the modal group index is extracted to be 3.68. Spectral response has shown single mode operation close to threshold (70mA) where multi modes lase at 100mA. Single mode operation can be achieved with introducing a DBR into the structure or by using a ring resonator or smaller ribs instead of the current structure/dimensions.

It is found that waveguides with widths less than 2.5µm lase single mode. For these small widths, the yield is limited by waveguide chipping and bond delamination during dicing and polishing facets which occurs mostly in narrower guides. Such a problem can be addressed if a ring cavity [66] or gratings are used to enforce single mode operation for large waveguide dimensions.

[9] The threshold current of this laser is recalculated in Appendix I.

2.1.5. Hybrid Evanescent Race-track laser[10]

The race-track laser is another structure that was fabricated with Evanescent Hybrid technology in which by having the shape of a race-track, the need of dicing and facet polishing to define the cavity of an edge emitting laser is eliminated. Thus, this structure[11] is the only Hybrid Evanescent laser structure suitable for integration with waveguides and other active and passive optoelectronic and photonic devices.

With this laser, two monitoring on-chip hybrid photodetectors are also fabricated to which laser light will couple horizontally. In this structure, height, width and slab height of the Si-ridge guide are 0.69µm, 1.65µm and 0.5µm respectively. Γ_{Si} is calculated to be 64% and Γ_{QW} is 4.2%.

Reported results have shown CW operation at 1.59µm, threshold current of 175mA (which is high, and is recalculated in the Appendix I), maximum optical output power of 29mW and T_{max}= 60°C [66].

The schematic in Figure 2- 10 illustrates the race-track laser along with two monitoring photo detectors and Figure 2- 11 shows an SEM of the fabricated laser.

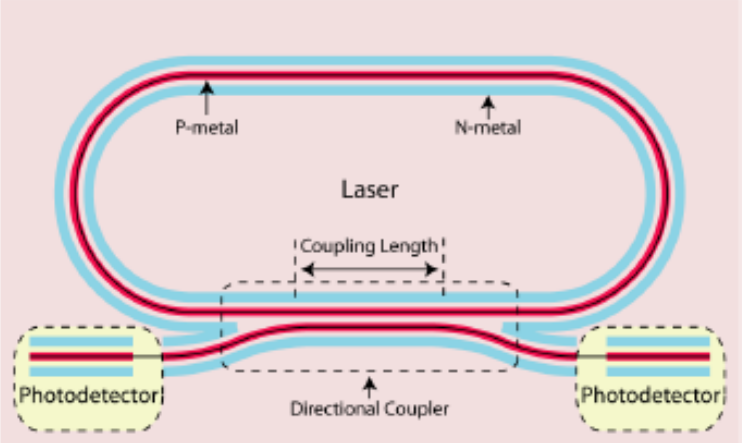


Figure 2- 10: Race-track laser structure with two monitoring photo detectors [66].

[10] Materials and figures in this section are mainly from [66].
[11] Along with the micro-ring laser which was fabricated at subsequent stages of Si-Hybrid project [52], [53].

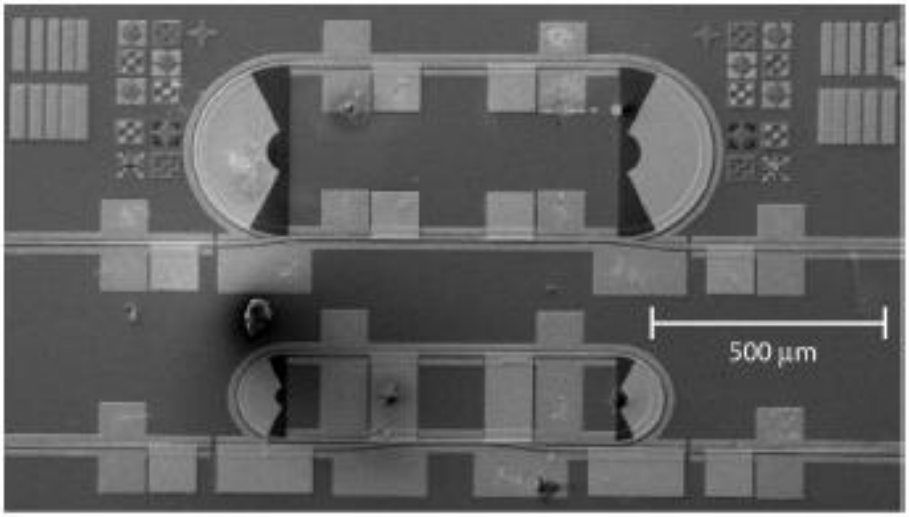


Figure 2- 11: SEM image of a fabricated race-track Hybrid Evanescent laser structure [66].

As visible in the SEM above, two versions of the structure are fabricated with bend radii of 100µm and 200µm and cavity lengths of 2656µm and 2028µm respectively. Table 2-1 shows characteristics of various versions of the fabricated race-track laser.

Radius	$L_{Interaction}$	P_{max}	η_d	I_{th}	T_{max}
200 µm	600 µm	29 mW	13%	175 mA	60 C
	400 µm	27.5 mW	17%	175 mA	60 C
100 µm	300 µm	3.1 mW	12%	200 mA	65 C
	100 µm	7 mW	4.3%	150mA	65 C

Table 2- 1: Characteristics of four fabricated laser track structures with corresponding P_{max}, η_d, I_{th} and T_{max} [66].

A limiting factor in reducing the size of the laser is bend loss. As seen in Figure 2- 12, bending loss increases dramatically for bend radii below 150µm.

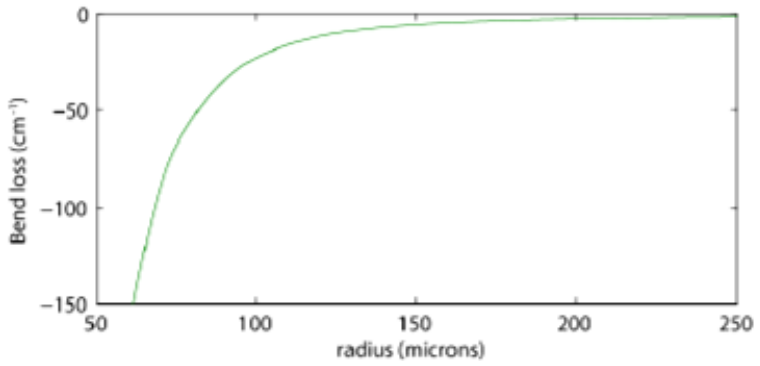


Figure 2- 12: Bend loss versus bend radius [66].

2.1.6. Suggestion to Improve the Race-track Laser Structure

This large bend radius requirement, i.e. r ≥150μm, should be compared to sub-10μm bend radius of Si ring resonators. The main reason that such a large bend radius is necessary here is the loosely guided mode characteristic of the Evanescent Hybrid technology. This in turn results in a very large device footprint and requires a significant amount of Si chip real-estate.

As one possible solution to solve this issue, we propose to remove the III/V stack on top of Si-ridge at the bend area, which makes the mode more confined and thus the bend can be less lossy with much smaller radius; as a result this will reduce the footprint of the device.

However this idea has two drawbacks. First, not having the gain medium in the bend area will reduce the modal gain. Second, such an idea will introduce four Si-guide↔Hybrid-guide transition interfaces. In the next section, the simulations we performed in order to study whether such interfaces pose a major loss due to reflections and scattering at the transition interfaces, will be discussed.

2.2. Assessment of Hybrid Evanescent Approach

In the race-track laser case, bends should be very large (>150μm in radius [66]), since the mode is weakly confined in the Si-guide in Hybrid Evanescent technology, therefore the mode sees a very high loss during a bend. As a result, the final structure is quite large and does not satisfy the small footprint requirement of high volume integration. Our suggestion to solve this issue would be to fabricate the bends from merely a Si-guide and not a hybrid one. In that case, since there is no III/V stack on top, the mode would be more confined and bends with much smaller radii (on the order of 10μm) can be achieved. However, with this approach one should look into the reflection and scattering the mode undergoes in the transition from Hybrid-guide to Si-guide and from Si-guide to Hybrid-guide at the interfaces going into and out of the bend (4 times in a race-track structure). The schematic in Figure 2- 13 shows the optical mode transfer in such transitions.

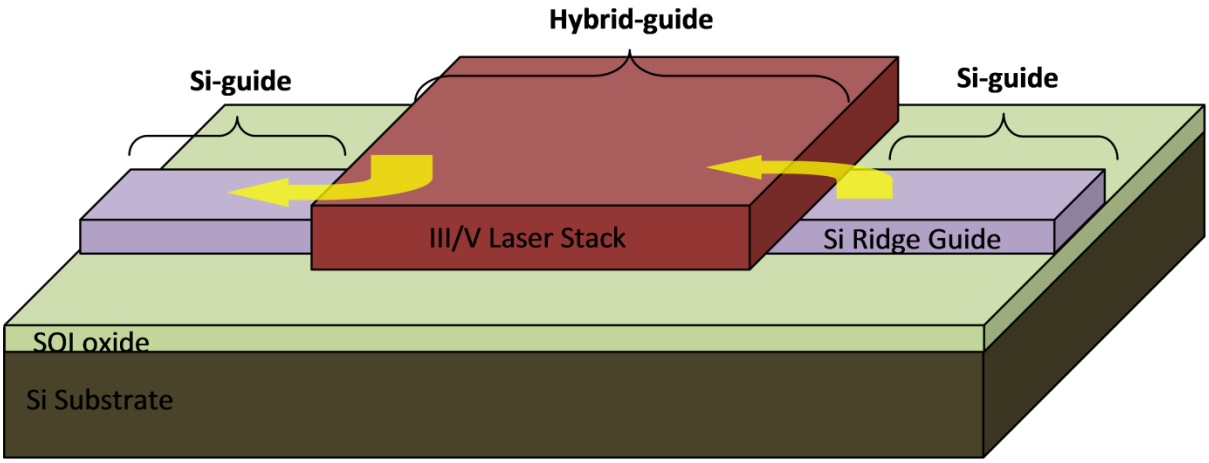


Figure 2- 13: Schematic showing the Si-guide to Hybrid-guide and Hybrid-guide to Si-guide transitions.

Using the BeamProp[12] software from RSoft, the reflection[13] and scattering caused at the transition interfaces between Si-guide and Hybrid-guide were studied. A three-dimensional structure was implemented and semi-vectorial simulations were performed. In order to define each layer, the Channel guide option was selected as the structure default waveguide type[14] and all the simulations were for the wavelength of 1.55μm[15].

Among the different kinds of input fields available in BeamProp, the rectangular launch and fiber mode launch were predominantly used, and the launched input waveform was positioned in the middle of the Si ridge waveguide.

In Figure 2- 14, the Hybrid Evanescent structure used in the simulations with BeamProp is depicted in x-y view (right) and in y-z view (left). The x-y view of the structure shows the special case of electrically pumped laser in which the slab height is zero. The SOI buried oxide has a thickness of 1μm (functioning as the lower cladding of the guided mode in Si-ridge), and the Si-ridge itself has a width of 2.5μm and height of 0.76μm, similar to the case of the fabricated electrically pumped laser in [63]. The figure on right shows the y-z

[12] Many thanks to the courtesy of Prof. Leslie Kolodziejski group that made the BeamProp software available to the author for simulations done on this topic.
[13] Before using BeamProp, we used the effective index method to assess the reflection at interfaces, however that approach undermines the basic requirement of effective index method which is the transitions should be smooth, gradual and not abrupt which is not the case in Hybrid-Si transitions by any means.
[14] Channel Guide waveguide type allowed for accurately positioning each layer of the structure as a channel guide in a shared background. Y positioning of layers was only available for Channel and Fiber guides in BeamProp and thus Rib/Ridge and Multilayer guides could not be used. Also the effective index method checkbox was deactivated since it reduced the dimensions of the structure from 3D to 2D and only works for Diffused and Rib/Ridge guides.
[15] Wavelength sweep simulations have also been performed to watch the optical mode distribution as frequency changes. However those results are not presented here.

view of such a structure. In this case the structure has a Si-guide to Hybrid-guide transition occurring at z=300μm.

Figure 2- 15 shows the computed fundamental mode for the Hybrid waveguide (left) and the Si-guide (right)[16].

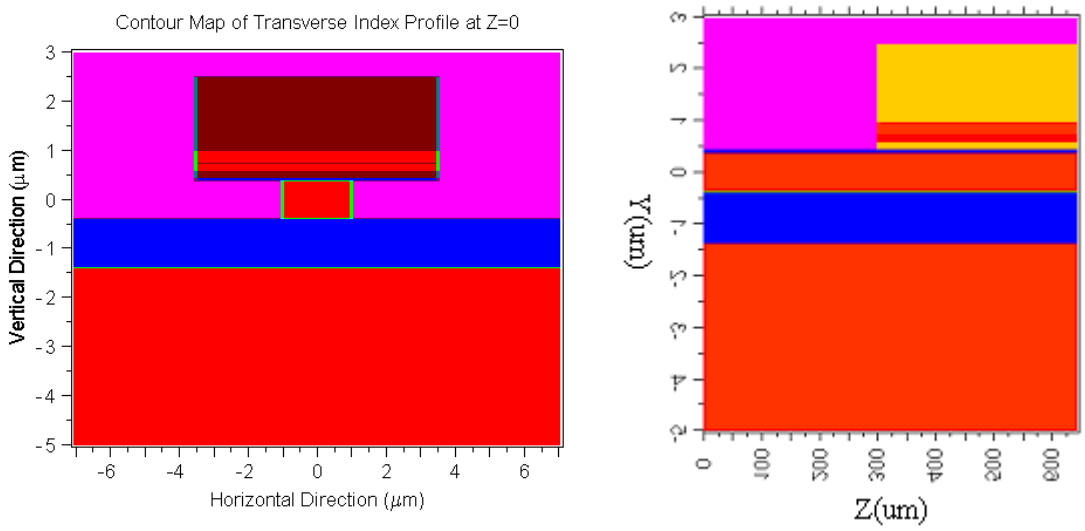


Figure 2- 14: Device structure used in BeamProp simulations. Left figure shows the x-y cross-section of the simulated structure (special case of zero slab height) where Si-ridge guide and III/V stack on top are recognizable. The figure on right shows the y-z view of the same structure. In this case the structure has a transition from Si-guide (<300μm) to a Hybrid-guide (>300μm) along z axis.

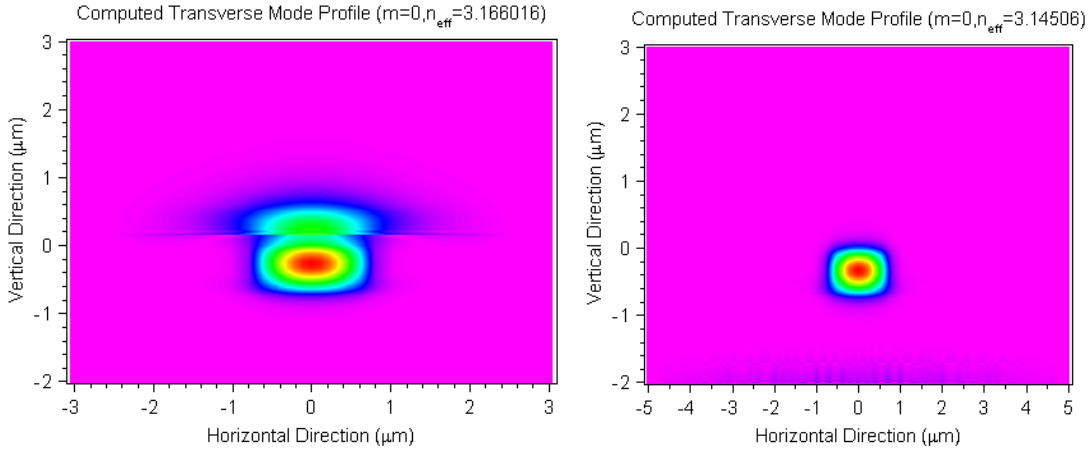


Figure 2- 15: Computed fundamental mode in Hybrid-guide (left) and Si-guide (right).

[16] Si guide dimensions are different in these two cases.

2.2.1. Structure Simulation Setup

The simulated structure has Si-guide dimensions of W=2.5µm, H=0.76µm and zero slab thickness[17]. The substrate (simulated domain) and III/V stack widths are 15µm[18] and 7µm respectively. Also, in order to include the bonding oxide layer between SOI and InP substrates, a thin layer of 6nm SiO_2 is included between the Si-guide and the III/V stack. Furthermore, since the three layers of Super Lattice (SL) + two n-InP layers all have the same refractive index, they are merged and treated as one layer in the simulated structure.

Two sets of discretizations are used throughout the simulations:

- Coarse grid simulation, with $\Delta y=0.01$, $\Delta z=1$, Monitor-z=5µm, and
- Fine grid simulation, with $\Delta y=0.005$, $\Delta z=0.5$, Monitor-z=1µm

Table 2- 2 summarizes different layers of the simulated structure, their material composition, height and corresponding effective index. In order to have flexibility to shift the whole structure up and down, a parameter called dH is defined and all layers' y-positions[19] (as well as launch mode y-position) are relative to dH (which is equal to 0.44 in the final results).

Layer Name	Material	Layer Height (hi) (µm)	Y-dH (dH=0.44 µm)	Effective Index
p-contact	$In_{0.53}Ga_{0.47}As$	0.1	-	-
p-InP (Upper Cladding)	InP	1.5	1.296	3.167
SCH	$Al_{0.131}Ga_{0.34}In_{0.528}As$	0.25	0.421	3.45
QW	$Al_{0.089}Ga_{0.461}In_{0.45}As$ 10 nm (9x)/ $Al_{0.055}Ga_{0.292}In_{0.653}As$ 7nm (8x)	0.146	0.223	3.53
n-InP	InP	0.15	0.075	3.167
Super Lattice	($In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$ / n-InP) (7.5nm each) 2x			
n-InP	InP			
Interfacial SiO_2	SiO_2	0.06	-0.03	1.45
Si rib	Si	0.76	-0.44	3.481
SiO_2	SiO_2	1	-1.32	1.45
Si Substrate	Si	5	-4.32	3.481

Table 2- 2: Simulated structure layers with their corresponding material composition, height, vertical position and effective index.

[17] Similar to the electrically pumped Hybrid Evanescent laser [63].
[18] Smaller domain width (e.g. 10µm) introduced high reflections at simulation domain boundaries.
[19] BeamProp puts Y position in the middle of each channel waveguide.

Figure 2- 16: Calculated mode for Si-guide structure along z direction.

Figure 2- 16 shows the calculated mode of the Si-guide structure along z direction, where the horizontal axis corresponds to x dimension in microns and the vertical axis is the z direction.

Different launch mode sizes have been simulated and compared with each other. More specifically, 3 cases of (W=2μm, H=0.6μm), (W=1.7μm, H=0.5μm) and (W=1.5μm, H=0.4μm) have been compared. The smaller the mode size, the lower the scattering to the Si-substrate and air, and much lower reflections from the boundaries are observed.

In addition, an important point about tracking powers was that each layer should have its own monitor positioned in the middle of that layer[20]. Also for the monitor type, Waveguide Power Monitor[21] was selected which integrates the power over the rectangular cross-section of the corresponding waveguide layer.

In the following simulation, the launch mode has a width of W=1.5μm and a height of H=0.4μm. The width of Si-guide is 2.5μm and the ridge height is 0.76μm. Figure 2- 17 shows one of preliminary results of the simulated optical mode propagation along the structure in both x-z and y-z views[22]. In this simulation a coarse grid size was used and thus the propagation results are not as fine as what will be presented shortly with finer discretization. By the same token, reflection from the boundaries can be seen in this case. Nevertheless, the general behavior of the propagated mode shape can be observed in x-z view on the left, and y-z view on the right. It can be noticed from the y-z view that the structure is initially a Si-guide only, and then at z=300μm it changes to a Hybrid-guide with the addition of the III/V stack on top of the Si-guide. Gradual coupling of the mode power to the III/V stack is observed in the y-z view, as well as lower power residing in the underlying Si-guide after the transition at z=300μm seen in x-z view.

[20] Meaning that layers cannot be combined and all share one monitor. Each layer should have its own monitor and at last, the recorded data must be manipulated manually to add powers in each group of layers.
[21] Monitor types available in BeamProp are: Fiber mode power/phase, Gaussian power/phase, Launch power/phase, WG power, Total power, Effective index, Field 1/e width/height and File power/phase.
[22] Since there was not much difference between Full TBC vs. Simple TBC, Full TBC was used as the boundary condition.

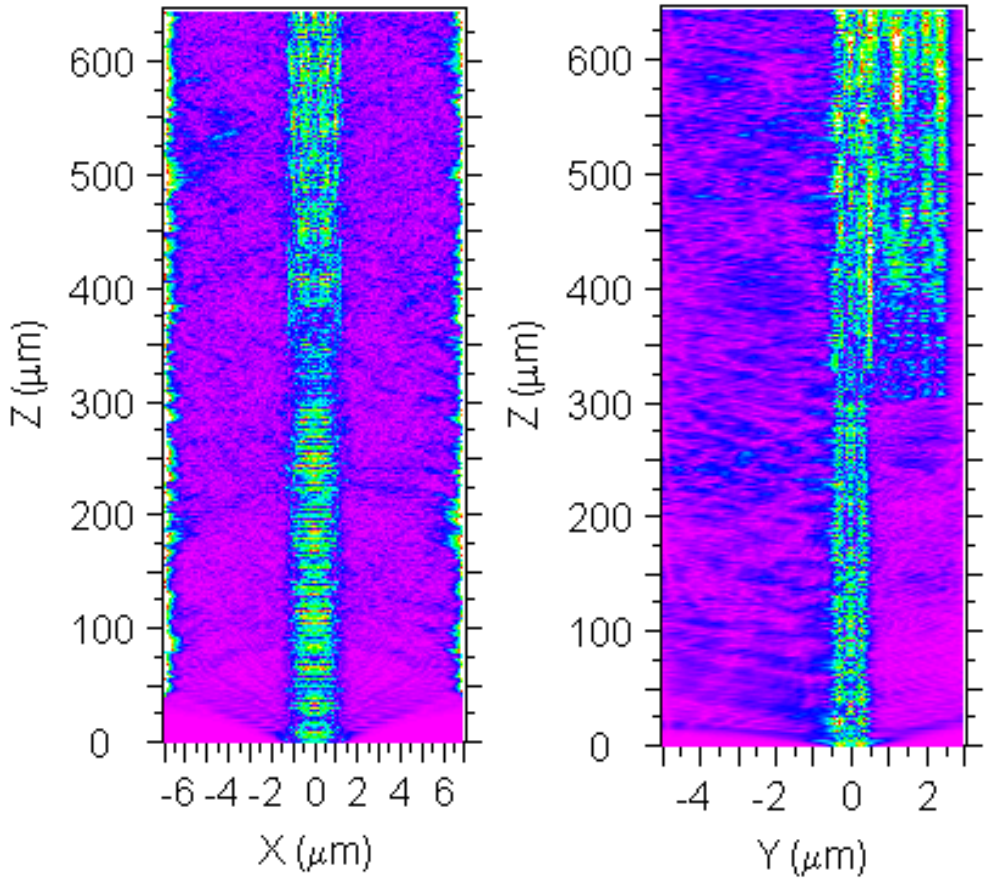


Figure 2- 17: Simulated optical mode distribution. x-z view is shown on left and y-z view is depicted on right. In this case, launch mode size is W=1.5µm and H=0.4µm, and the width of Si-guide is 2.5µm and the ridge height is 0.76µm.

2.2.2. Optical mode distribution in QW layer

In order to inspect the distribution of optical mode inside the QW layer, dH was changed from 0.44µm to -0.223µm so that the QW layer is positioned at y=0 (Figure 2- 18, right). The left graph in Figure 2- 18, shows the resulting mode distribution inside the QW layer. It is observed that due to the evanescent coupling nature of the structure and also the presence of thin bonding SiO_2, about 200µm of device length is needed to fully couple the optical mode to the QW layer and achieve the highest gain. This will increase the device length and results in a large final footprint of the device.

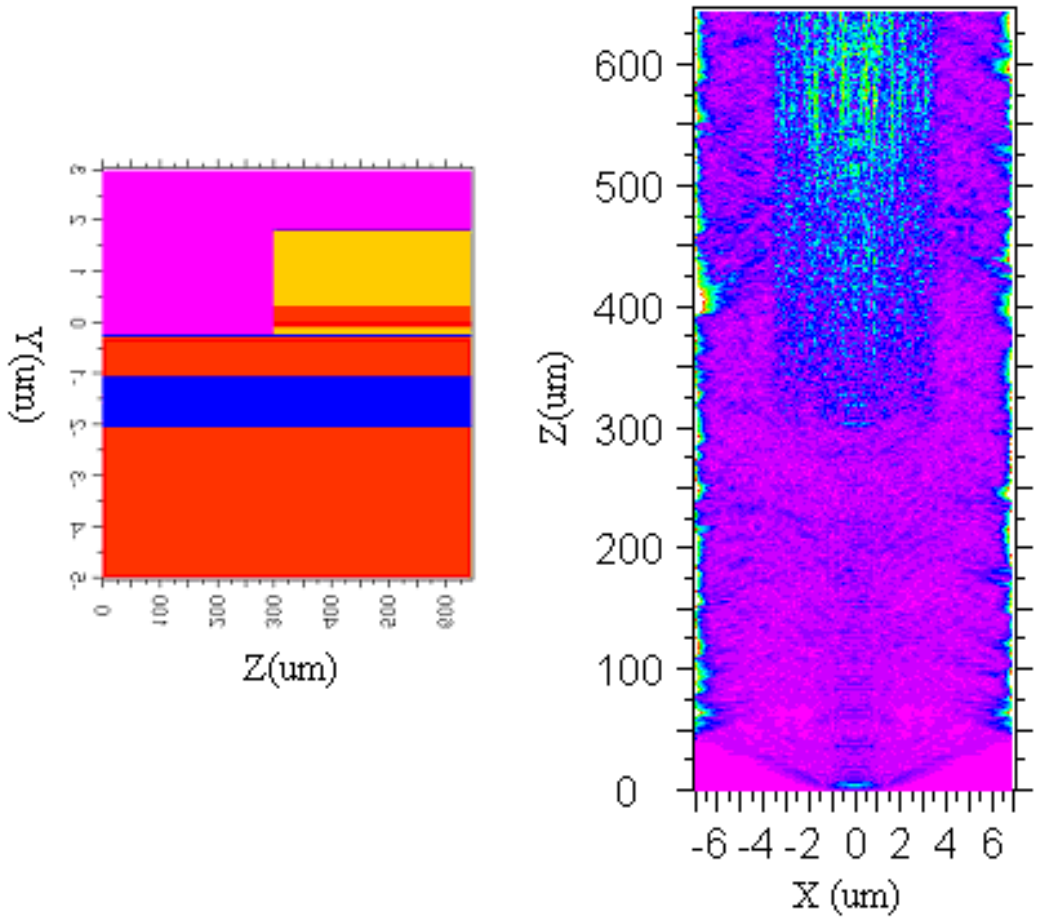


Figure 2- 18: Mode distribution at the QW level. The figure on left shows how the structure is vertically repositioned so that y=0 is aligned to the middle of the QWs and the figure on right shows the x-z view of optical mode distribution in QW layer.

2.2.3. Propagation Simulation Results

Figure 2- 19 and Figure 2- 20 show the fine discretization simulated results for mode propagation in a structure which consists of a Si-guide initially and then transitions to a Hybrid-guide at z=300µm. Launch fields have the dimensions of W=2µm and H=0.6µm and results for two cases of fiber launch and rectangular launch fields (same dimensions) are illustrated in fine discretization[23]. For each case, both x-z and y-z propagation profiles are depicted. Note that reflections from the simulated window boundaries (along the x dimension) are much lower in this case compared to coarse grid results of Figure 2- 17 and Figure 2- 18.

[23] Coarse grid simulations are not shown for the purpose of brevity.

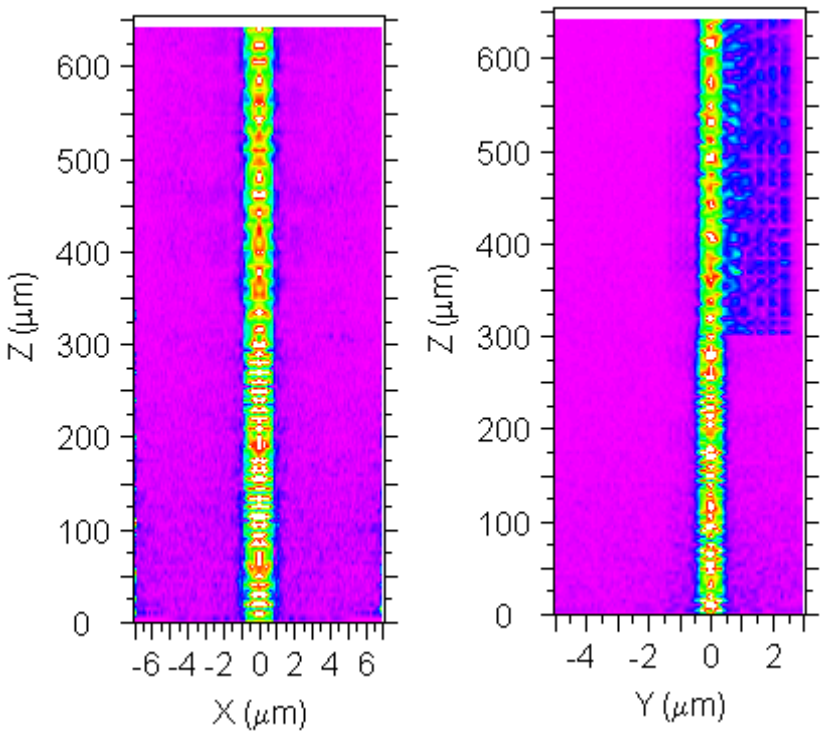


Figure 2- 19: Optical mode propagation results with fine grid discretization and a rectangular launch field; x-z view is shown on left and y-z view on right.

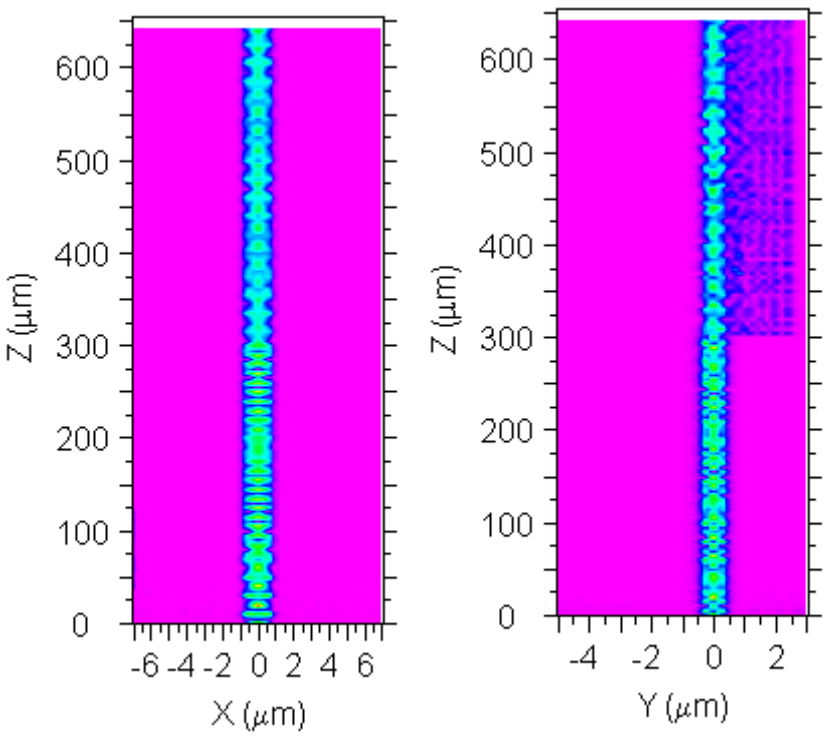


Figure 2- 20: Optical mode propagation results with fine grid discretization and a fiber launch field; x-z view (left) and y-z view (right).

Note that multi mode beating is observable in the x-z view (showing the Si-guide) of both Figure 2- 19 and Figure 2- 20, which is the result of large ridge width for the Si-guide (2.5µm) used in these simulations, which was selected to be similar to the fabricated Si-Hybrid electrically pumped Fabry Perot cavity lasers in [63].

2.2.4. Mode Spectrum Response

In order to confirm multimode beating observed in x-z propagation simulation results of Figure 2- 19 and Figure 2- 20, we looked into the modal spectrum of the structure.

In order to excite all modes supported by the structure, a proper field should be launched for instance any field launched off-center. Therefore the launch mode dx was set to W/2.

There are two possible approaches to simulate the mode spectrum of the structure: the iterative method and the correlation method. The iterative method is advised for standard waveguide structures and the correlation method is suggested for anti-guiding leaky cases. Experimenting with both approaches showed that the correlation method gives a more reasonable result for the fundamental mode. Figure 2- 21 shows the fundamental mode derived from the correlation method with a fiber mode launched at the center.

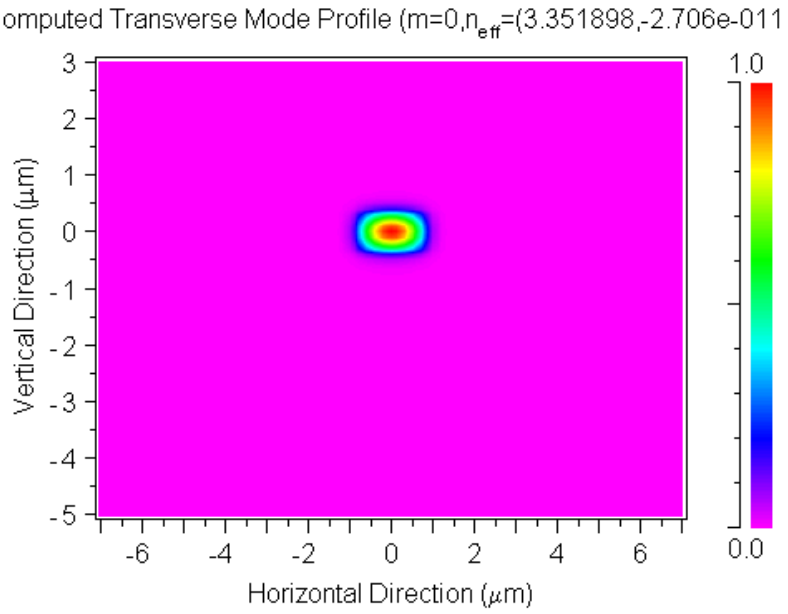
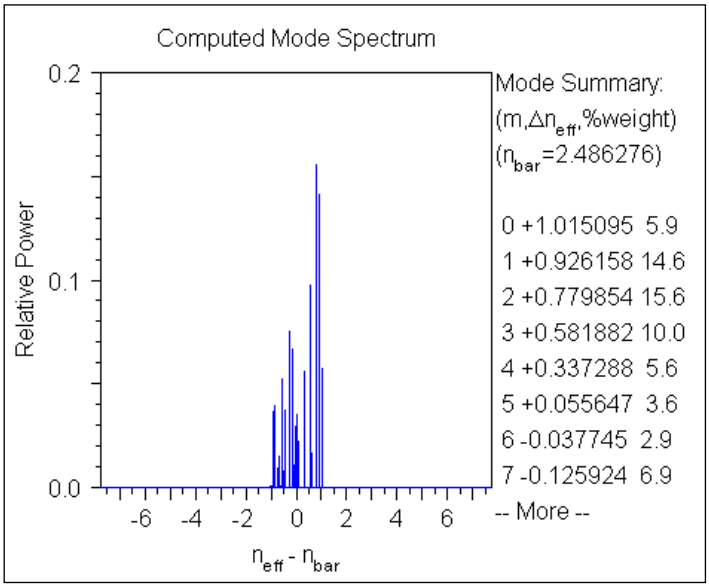


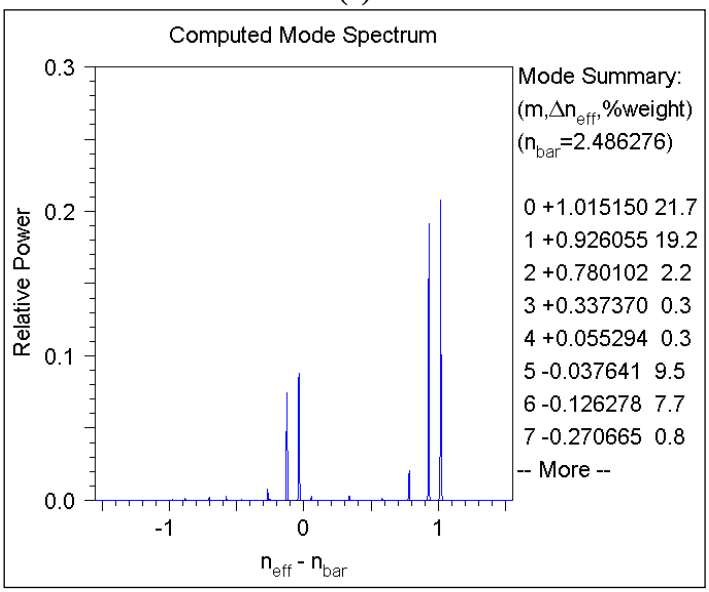
Figure 2- 21: Fundamental mode derived from correlation method. A fiber mode is launched at the center of the waveguide.

Since in the correlation method, the resulting mode spectrum represents the FFT of the correlation function (in which peaks show guided modes), the propagation length of the

structure should be long enough (to have better frequency resolution) and the sampling period (monitor steps) should be small enough to have a wider frequency spectrum. In Figure 2- 22, in the plot (a) the monitor step is set to 0.1μm where as in plot (b) it is set to 0.5μm (yielding an expanded view of the spectrum around $\Delta n_{eff}=0$). For both graphs the fiber launch mode is placed off center by dx=W/2. Modes supported by the structure are shown at each frequency ($n_{eff}-n_{bar}=(\beta-k_{bar})/k_{bar}$) with their relevant power listed in the sidebar of each graph.



(a)



(b)

Figure 2- 22: Mode spectrum response of the hybrid structure. Modes supported by the structure are shown at each frequency ($n_{eff}-n_{bar}=(\beta-k_{bar})/k_{bar}$) with their relevant power depicted in the sidebar of each graph. Fiber launch mode is placed off center by dx=W/2. In the upper graph, monitor step is set to 0.1μm and in the lower one it is set to 0.5μm (zoomed view in a sense).

2.2.5. Analyzing Simulation Data

In the following sections we will study the power flow in transitions between Si-guides and Hybrid-guides[24] from which the insertion loss of those transitions is calculated. First, we will analyze a Si-guide to Hybrid-guide transition, then a Si-guide to Hybrid-guide to Si-guide transition, and at last Hybrid-guide to Si-guide case is simulated.

In each case, when data from each simulation is extracted, monitors are added together to get the total power in the Si-guide, III/V stack, and Si substrate. More specifically, the following scheme was used:

- Si-guide Power = Si-guide + Thin (bonding) SiO_2
- III/V Stack Power = Lower InP + QW + SCH + Upper InP
- Sum = Si-guide Power + III/V Stack Power
- Power scattered to substrate = Thick SOI SiO_2 + Si-Substrate

- 2.2.5.1. Si-guide to Hybrid-guide Transition

For this transition, Figure 2- 23 shows the propagated mode shape along x-y and x-z views from a fiber launch case[25] (similar to Figure 2- 24), and the analyzed data is illustrated in Figure 2- 24 to Figure 2- 26. The structure simulated in this case has a Si-guide for the first 300µm (along z), which turns to a Hybrid-guide (III/V stack bonded on top) from 300µm to 645µm. In each plot, in order to get a better estimate of average power in the Si-guide and III/V stack, a moving average trendline is included as an overlay on each graph. The period of the moving average trendline is set to 50, meaning that an average of 50 data points is calculated to determine the trendline.

As seen from these figures and Table 2- 3, 20% of the optical power in the Si-guide would couple to the III/V stack on top in such a transition, and the remaining 80% continues to propagate in the Si-guide. By summing these two powers together, one can see that there is almost no loss in the total power (in Si-guide + III/V stack) after and before transition. Thus the insertion loss in a Si-guide to Hybrid-guide transition would be close to zero.

In fact to be more accurate, there is 3% increase in the sum of power in Si-guide and III/V stack after such transition, as can be seen in Figure 2- 25. This can be due to the Hybrid guide pulling up power that resides in the underlying substrate (in Si-guide section) by shifting up the propagated mode towards the III/V stack. In fact this hypothesis is reinforced

[24] Hybrid guide is a Si-ridge guide with the III/V stack bonded on top.
[25] Fine grid discretization was used in this simulation.

by looking at Figure 2- 26 where the yellow triangles show the power in the substrate decreasing right after the Si-guide to Hybrid-guide transition at z=300µm.

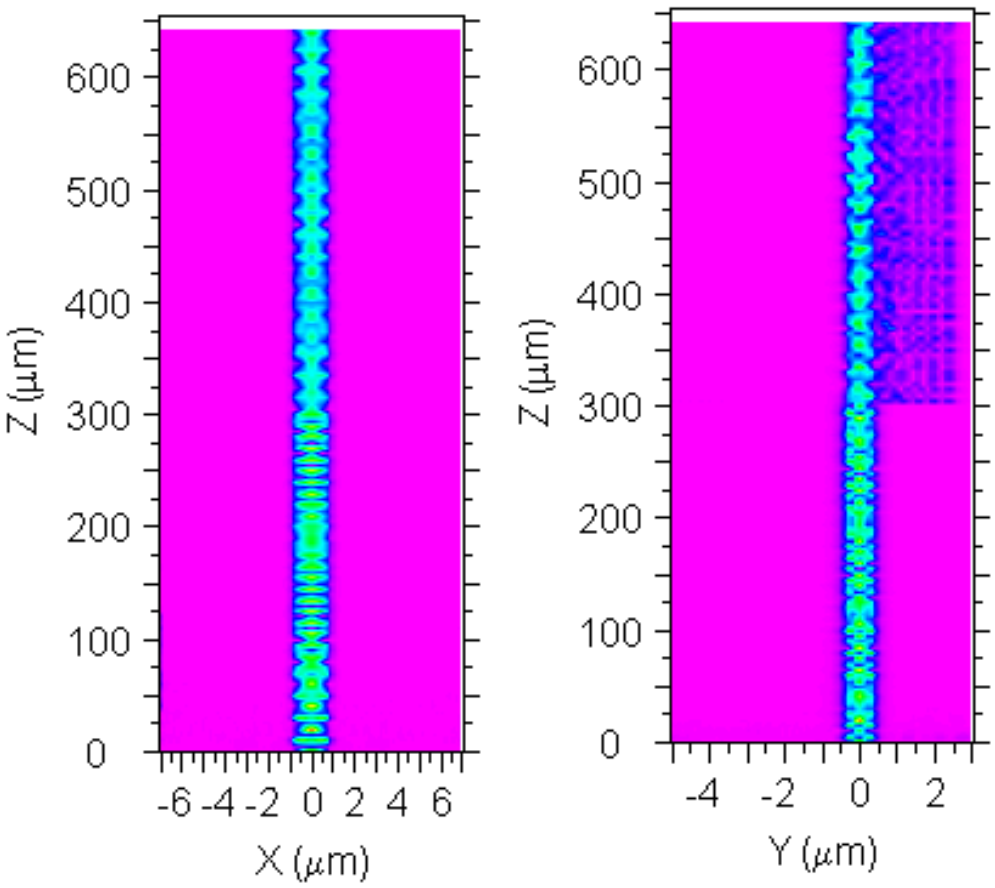


Figure 2- 23: Optical mode propagation results for fine grid discretization and fiber launch field. x-z view (left) and y-z view (right). The transition from Si-guide to Hybrid-guide occurs at z=300µm.

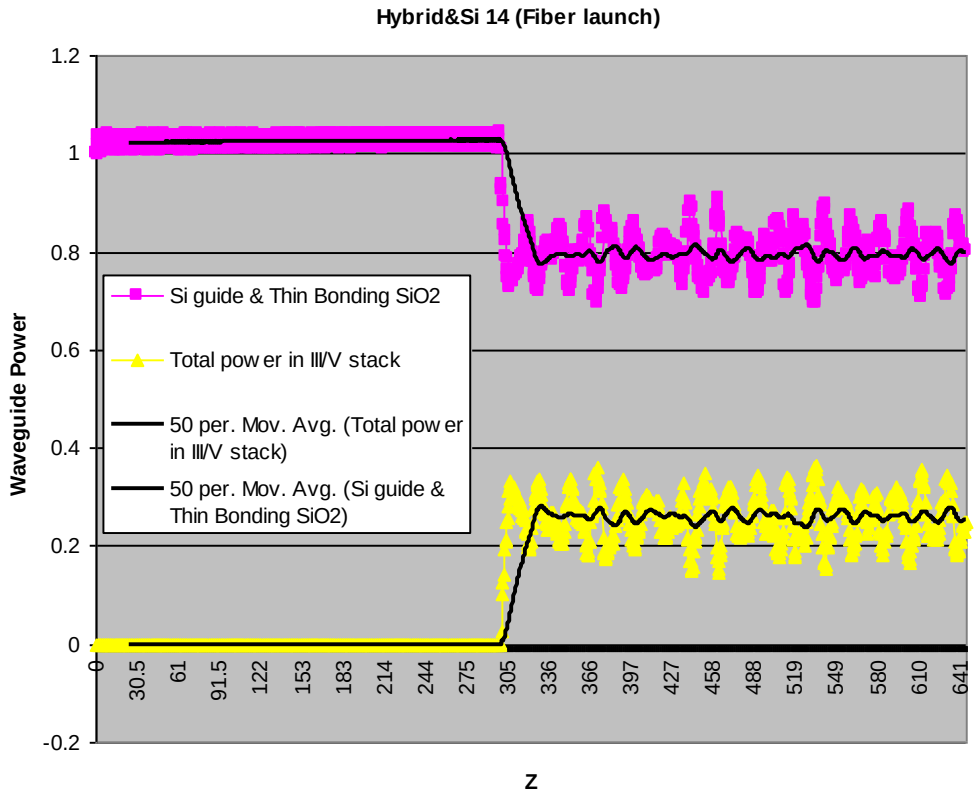


Figure 2- 24: Analyzed data for Si-guide to Hybrid-guide transition. The structure has a Si-guide for z<300µm and then a Hybrid-guide for 300µm<z<645µm. Pink squares show the sum of powers in Si-guide and the thin bonding oxide on it. Yellow rectangles show the sum of power in all layers of the III/V stack. It can be observed that 20% of the optical power in the Si-guide couples to the III/V stack on top in such a transition, while the remaining 80% continues to propagate in the Si-guide.

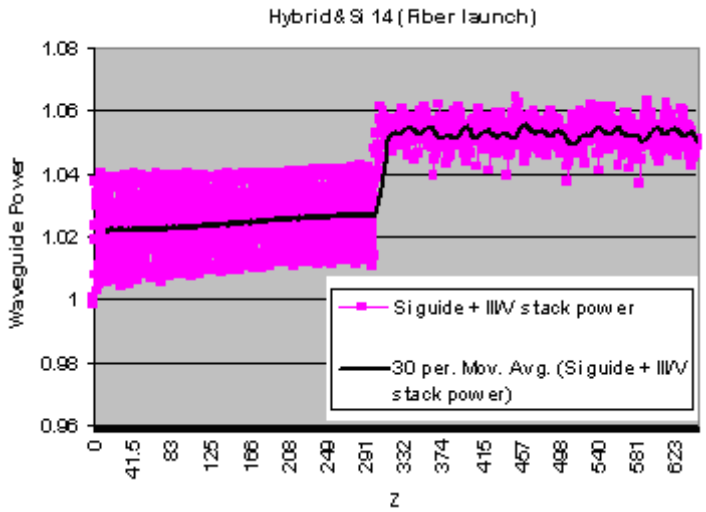


Figure 2- 25: By adding powers in Si-guide and III/V stack shown in Figure 2- 24, total guided power is depicted in this graph. It can be concluded that there is no loss in sum of powers of Si-guide and III/V section after and before transition, an instead about 3% increase is observed in this sum, indicating that power in the substrate is pulled up towards the III/V stack, in the Hybrid-guide. Therefore there is no insertion loss in Si-guide to Hybrid-guide transition.

Yellow triangles in Figure 2- 26 show the lost power in the Si substrate and SOI SiO_2 which is about 3%-4%. (Note that the Si-guide length is long enough to allow the unguided substrate modes to die out.) However, after the Si-guide to Hybrid-guide transition occurs, the power in the substrate falls to close to zero, and instead the sum of power in Si-guide and III/V stack is increased by about 3% pulling the power in the substrate upwards into the III/V stack. Selected points of the numerical simulation data for Si-guide to Hybrid-guide transition case are summarized in Table 2- 3 as a reference.

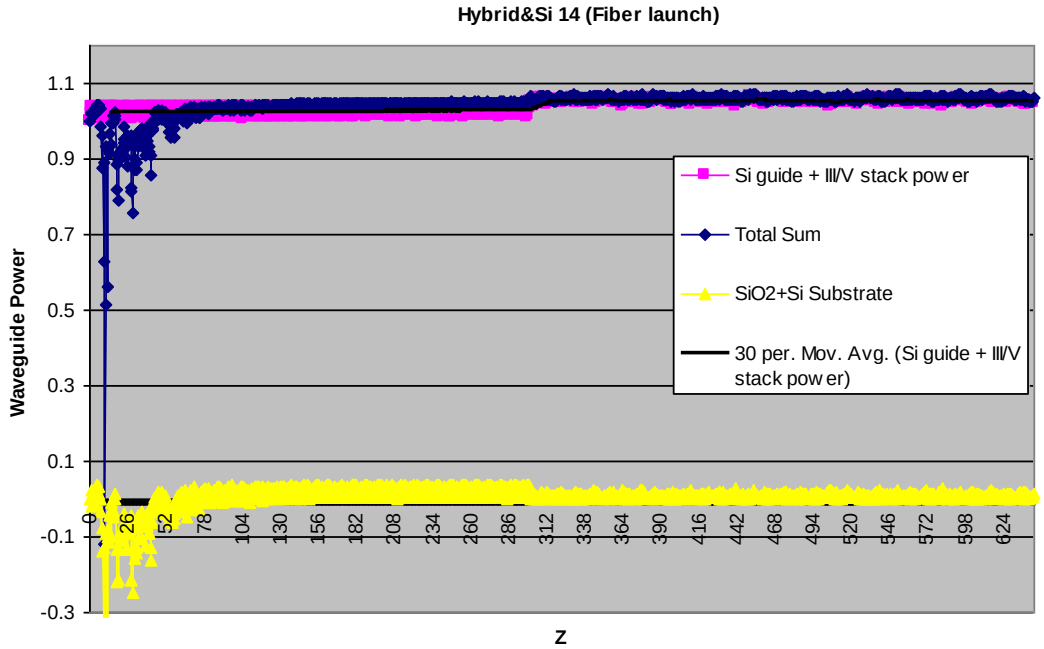


Figure 2- 26: Yellow data shows the dissipated power to Si-substrate and SOI SiO_2 which is less than 4% on average.

Z-position (µm)	Total power in III/V stack	Total power in Si guide & thin bonding SiO_2	Sum	SOI SiO_2 and Si substrate	Total sum
0	0	1	1	1.46338E-10	1
299.5	0	1.013499	1.013499	0.036759471	1.050259
300	0.0043656	1.043407	1.047772	0.004064115	1.051836
645	0.2487496	0.800554	1.049304	0.012741778	1.062046

Table 2- 3: Selected data points for Si-guide to Hybrid-guide transition simulation results.

- 2.2.5.2. Si-guide to Hybrid-guide to Si-guide Transition[26]

It was concluded in the previous section that 20% of the power is coupled to the III/V stack in Si-guide to Hybrid-guide transition. The next question will be whether this power will couple back to the Si-guide in a subsequent Hybrid-guide to S-guide transition. Therefore, in this section the simulated structure begins with a Si-guide ($z \in [0,300\mu m]$), then transfers to a Hybrid guide ($z \in [300\mu m,645\mu m]$), and at last transfers back to a Si-guide ($z \in [645\mu m,945\mu m]$). Such a structure would have two transition interfaces which will introduce reflections, scattering and turbulences in the mode propagation. Rectangular launch mode (coarse grid discretization) and fiber launch mode (fine grid discretization) are shown in Figure 2- 27 and Figure 2- 28 respectively.

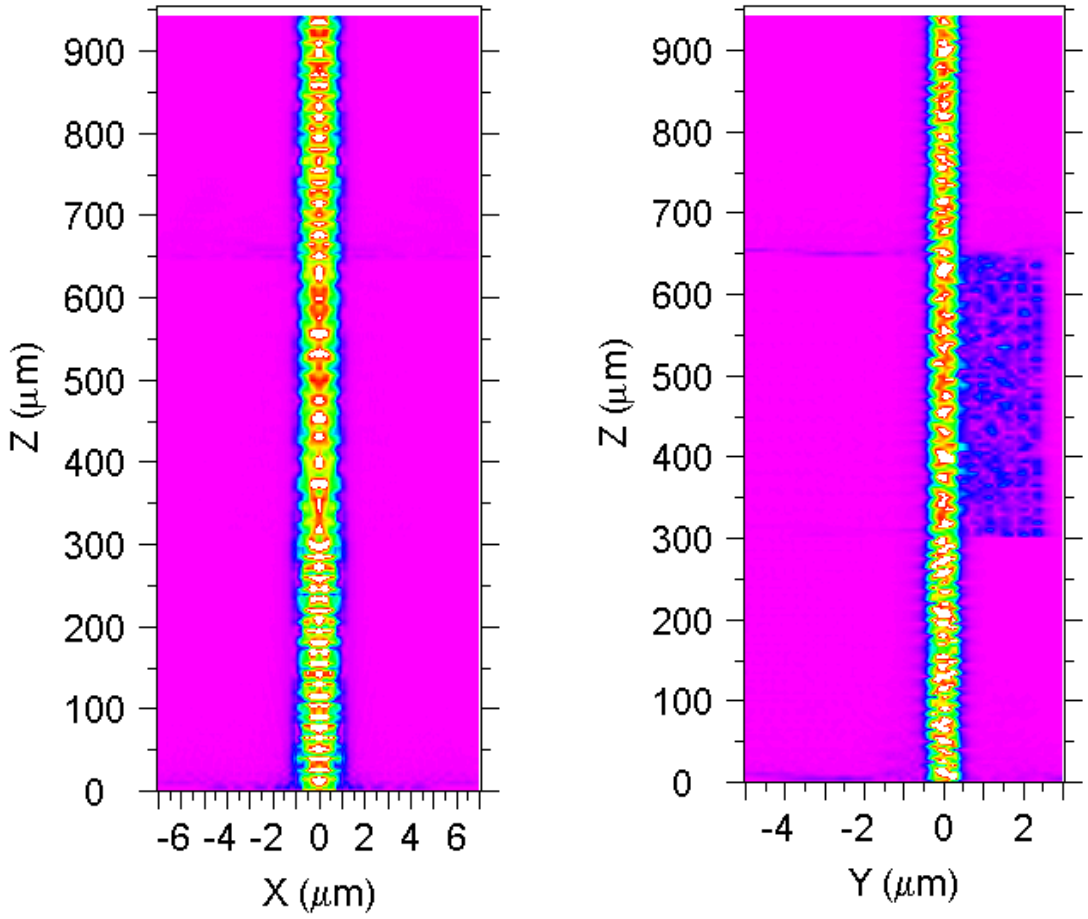


Figure 2- 27: Mode propagation in Si-guide to Hybrid-guide to Si-guide structure. Rectangular launch mode and coarse grid discretization are used here.

[26] Another version of the same Si-guide to Hybrid-guide to Si-guide structure is simulated in which III/V stack width is reduced from 7μm (in this case) to 2μm, the result of which is not presented here for the purpose of brevity.

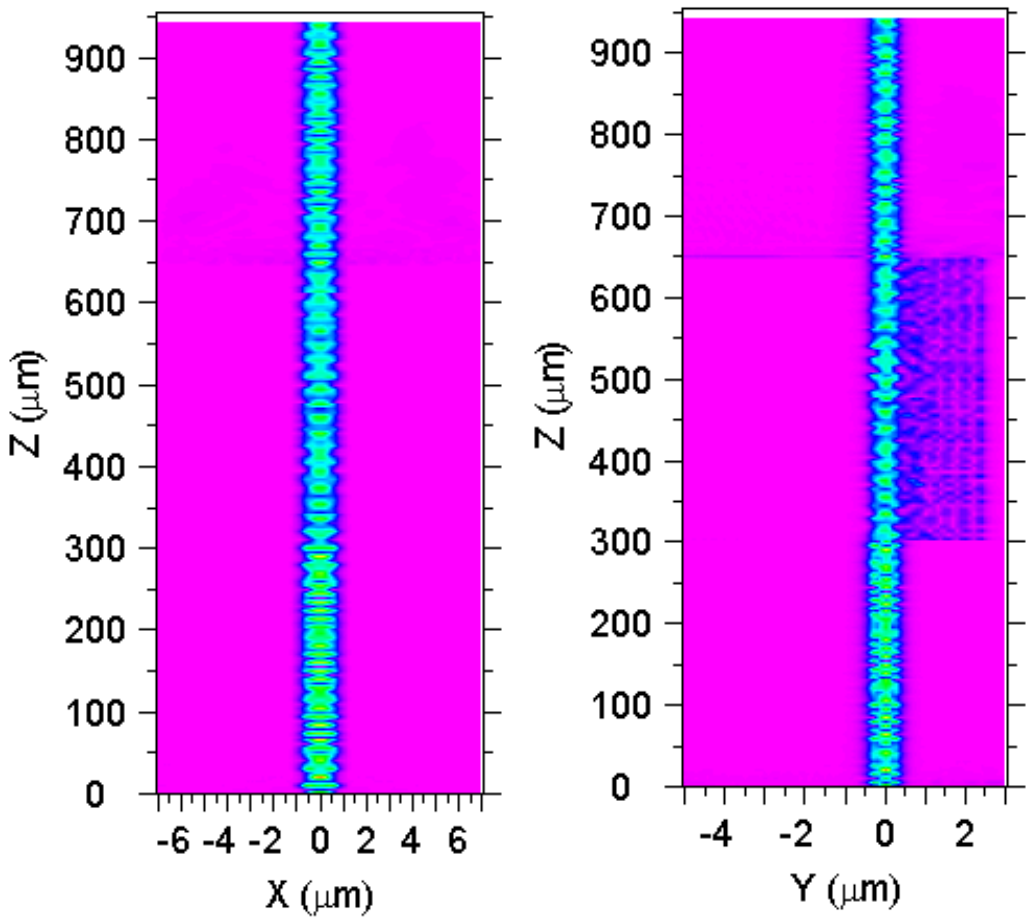


Figure 2- 28: Mode propagation in Si-guide to Hybrid-guide to Si-guide structure. Fiber launch mode and fine grid discretization are used.

Like the previous structure, the extracted data from the fine grid fiber launch simulation is plotted in Figure 2- 29 and Figure 2- 30. As it is seen from the analyzed data, the whole transition of Si-guide to Hybrid-guide to Si-guide introduces a 20% loss in the total power. Thus the insertion loss in this transition is $10 \times \log_{10}(0.794) = -1$ dB.

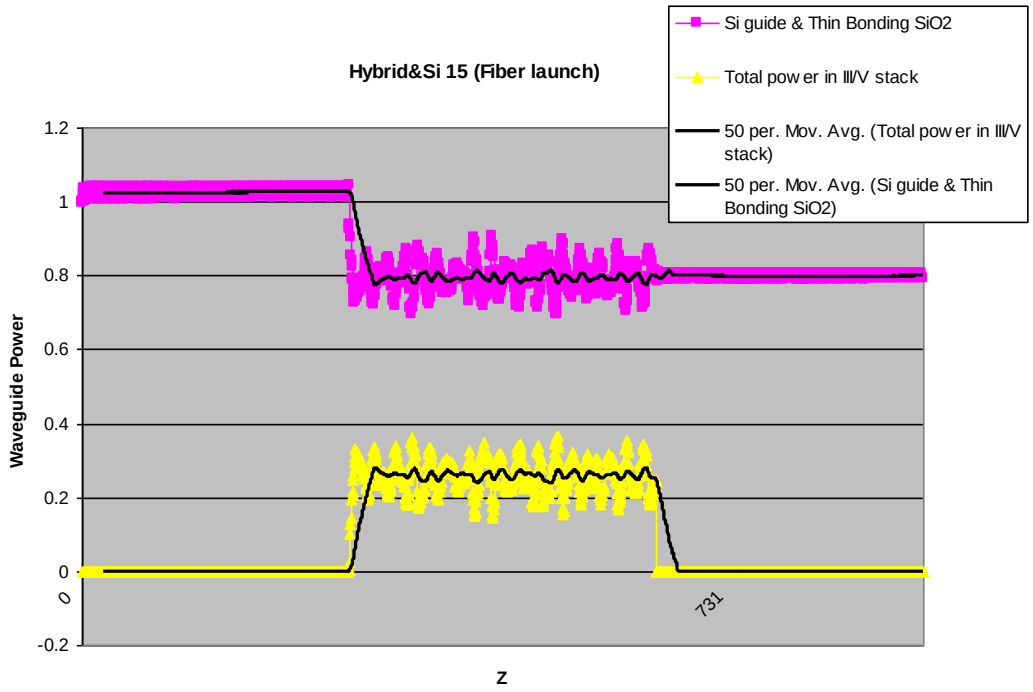


Figure 2- 29: Analyzed data for Si-guide to Hybrid-guide to Si-guide structure. Pink squares show the sum of powers in Si-guide and the thin bonding oxide on it. Yellow triangles show the sum of power in all layers of the III/V stack.

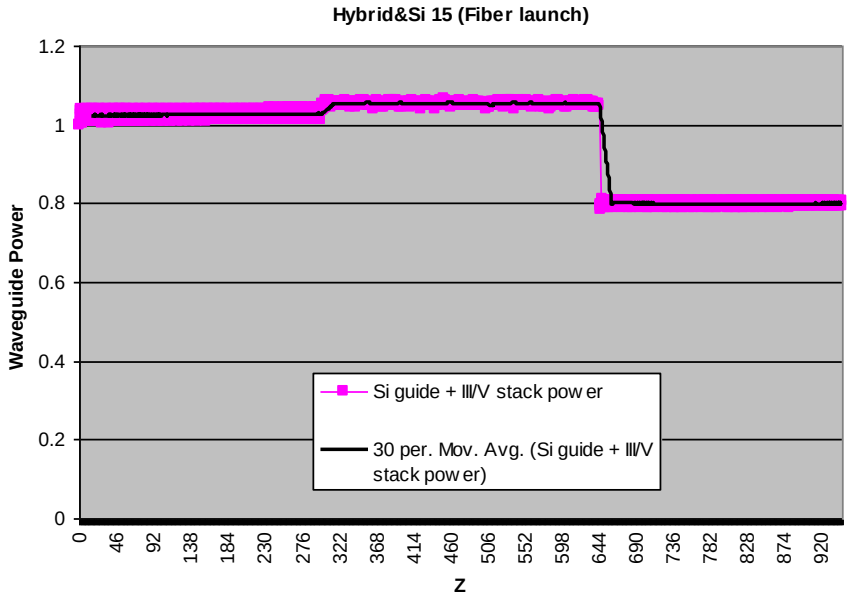


Figure 2- 30: Power in the Si-guide and III/V stack shown in Figure 2- 29 are added together to give the total guided power depicted in this graph. It can be observed that there is a 20% loss in this transition.

A selected point summary of numerical simulation data for the Si-guide to Hybrid-guide to Si-guide transition case is given in Table 2- 4.

Z-position (µm)	Total power in III/V stack	Total power in Si guide & thin bonding SiO_2	Sum	SOI SiO_2 and Si substrate	Total sum
0	0	1	1	1.46338E-10	1
299.5	0	1.013499	1.013499	0.036759471	1.050259
300	0.0043656	1.043407	1.047772	0.004064115	1.051836
644.5	0.2487496	0.800554	1.049304	0.012741778	1.062046
645	0	0.791858	0.791858	0.00931141	0.801169
645.5	0	0.795135	0.795135	0.000217298	0.795353
945	0	0.794029	0.794029	0.014507673	0.808536

Table 2- 4: Selected data points for Si-guide to Hybrid-guide to Si-guide transition simulation results, which shows about 1dB insertion loss.

2.2.5.2.1. Side note: Fundamental mode coupling loss in Si-guide to Hybrid-guide to Si-guide transition:

By looking at the simulations done by Intel/UCSB group for the photodetector case [65] and data presented in Figure 2- 6, there is 63% coupling between the fundamental mode of the Si-guide and the fundamental mode of the Hybrid-guide. This leads to $(63\%)^2$=37% coupling efficiency in a Si-guide to Hybrid-guide to Si-guide transition in a structure that has only a single mode. In other words, in such a transition, there is 63% (2dB) insertion loss based on fundamental mode overlaps shown in Figure 2- 6 and calculated by Intel/UCSB group.

However, since in the beam propagation method used in our simulations here, multi mode propagation along the waveguides and their interaction is allowed, the insertion loss is found to be 1dB, which is lower than the 2dB implied by considering only the overlap of fundamental modes of the two guides as discussed above. Since the multi mode nature of such propagation was confirmed earlier in this chapter, this observation is consistent with expectation.

- 2.2.5.3. Hybrid-guide to Si-guide Transition

In order to confirm the loss that was observed in the Si-guide to Hybrid-guide to Si-guide results of previous section, another structure was simulated with a Hybrid-guide to Si-guide transition. The structure starts from the Hybrid guide ($z \in [0,345\mu m]$) and then it is transferred to a Si-guide ($z \in [345\mu m,630\mu m]$). Like before, both coarse and fine grids were simulated for fiber and rectangular launch modes (Figure 2- 31 and Figure 2- 32). For the

fiber launch and fine grid case, the extracted data was analyzed and shown in Figure 2- 33 and Figure 2- 34.

From the data shown in Figure 2- 33 and Figure 2- 34, one can conclude that, from the total power of the launched mode, 20% is coupled to the III/V stack while 80% remains in the Si-guide. However in the Hybrid-guide to Si-guide transition 20% of the total power is lost (1dB insertion loss) due to reflections and scattering to air and SOI substrate caused at the Hybrid-Si interface. Selected points of numerical simulation data are summarized for this transition in Table 2- 5 and confirm this conclusion.

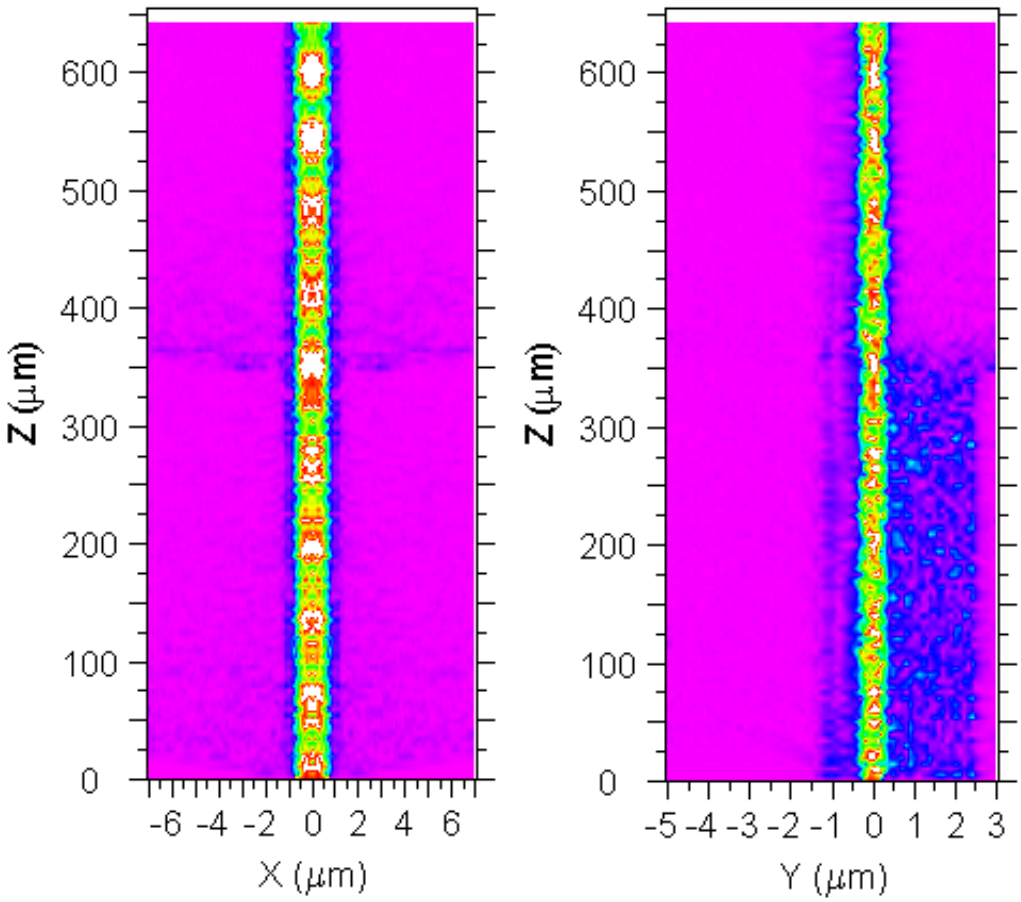


Figure 2- 31: Mode propagation in Hybrid-guide to Si-guide structure.
Rectangular launch mode and coarse grid discretization are used here.

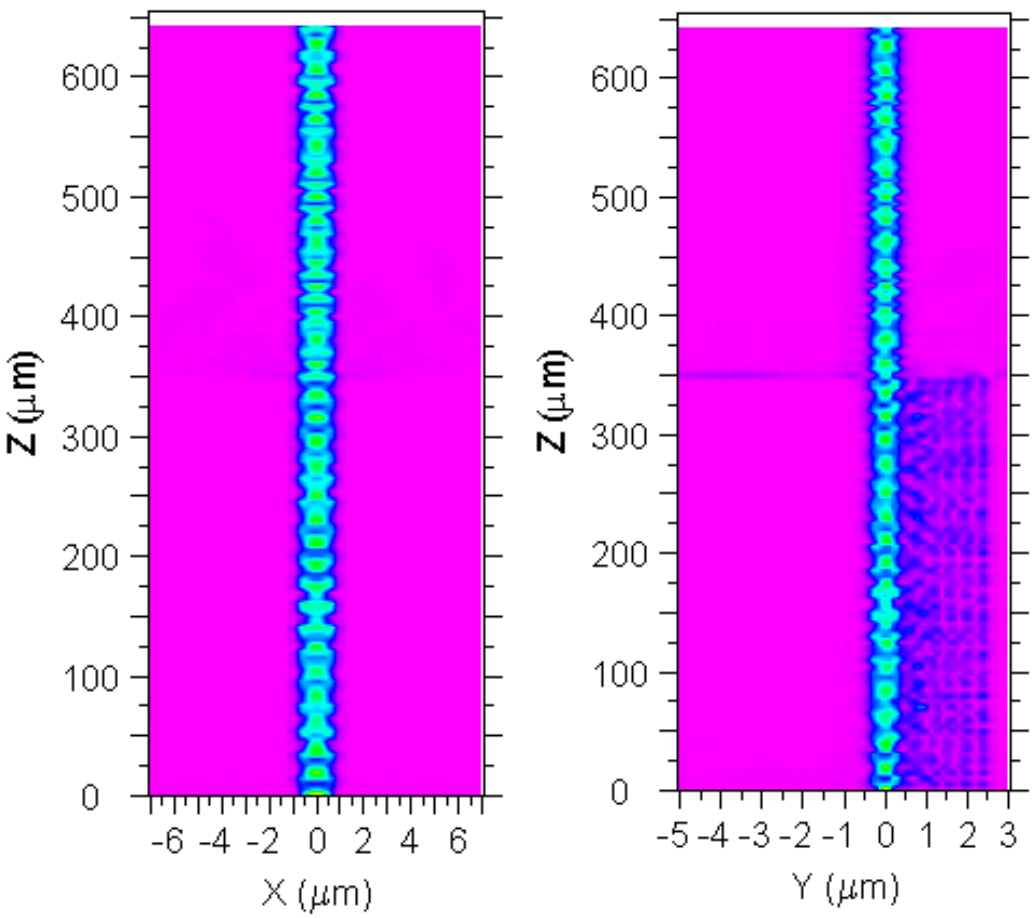


Figure 2- 32: Mode propagation in Hybrid-guide to Si-guide structure.

Fiber launch mode and fine grid discretization are used.

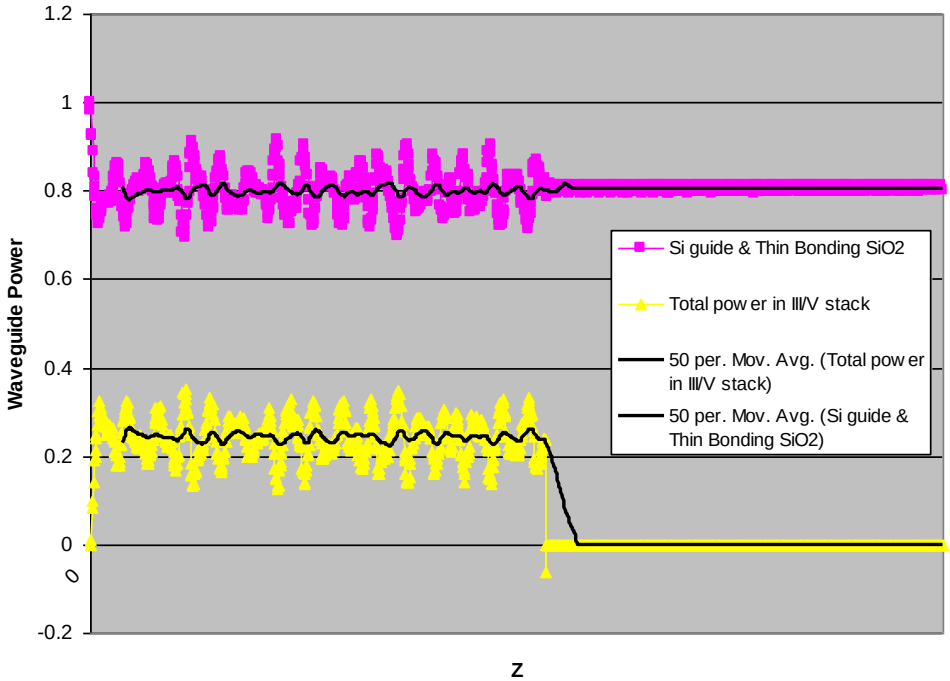


Figure 2- 33: Analyzed data for Hybrid-guide to Si-guide structure. From the total power of the launched mode, 20% is coupled to the III/V stack while 80% remains in the Si-guide.

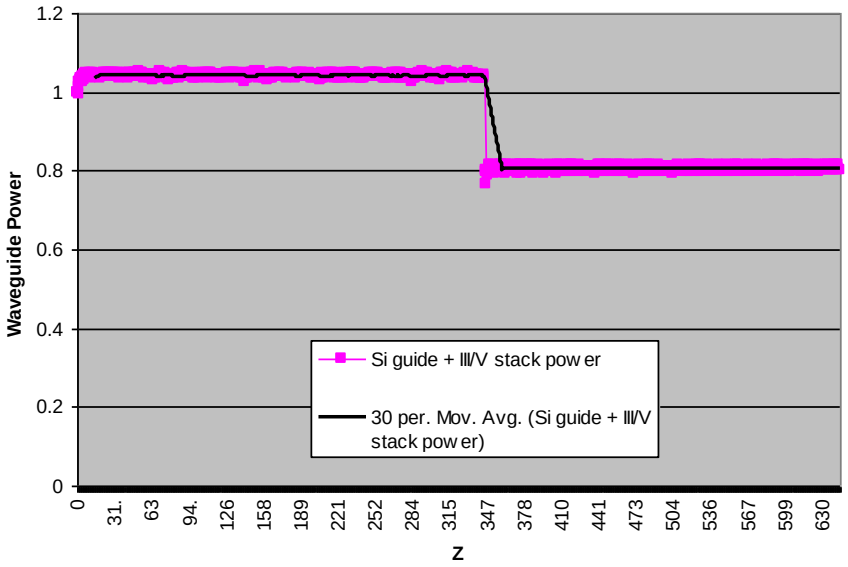


Figure 2- 34: In the Hybrid-guide to Si-guide transition, 20% of the total guided power is lost (1dB insertion loss).

Z-position (µm)	Total power in III/V stack	Total power in Si guide & thin bonding SiO_2	Sum	SOI SiO_2 and Si substrate	Total sum
0	3.632E-13	1	1	1.46338E-10	1
345	-0.062138	0.827887	0.765749	0.01437198	0.780121
345.5	0	0.800649	0.800649	0.006050691	0.8067
630	0	0.809812	0.809812	0.005081597	0.814894

Table 2- 5: Selected data points for Hybrid-guide to Si-guide transition simulation results, which shows about 1dB insertion loss.

2.2.6. Summary

According to the simulations above, one can conclude that the Si-guide to Hybrid-guide transition does not introduce a significant loss in power, while the Hybrid-guide to Si-guide interface produces a 20% loss in total power (about 1dB insertion loss).

This observation is interesting and is further confirmed when one recalls the fact that optical mode tends to couple better to higher index layers. In fact this is exactly the idea behind starting with lower index layers and going to higher refractive index layers as we elevate in height in the Twin Waveguide Technology. This wise strategy is based on the knowledge that light couples more easily from lower index layers to higher index layers, thus they start with lower index ones at the bottom of the multi-layer structure and fabricate higher

index layers on top. This will maximize the coupling efficiency in each vertical layer transition in the Twin Waveguide Technology.

By the same token, our simulations have shown that going to higher index waveguide (Si-guide to Hybrid-guide) does not introduce significant loss while going to lower index waveguide (Hybrid-guide to Si-guide) introduces about 1dB insertion loss.

At this stage, one might wonder how this observations play in the fabricated devices by the UCSB/Intel research group. In fact neither the fabricated race-track laser [66] nor the Fabry Perot cavity laser [63] do not posses such Hybrid-guide to/from Si-guide transitions. For both cases we believe that the entire cavity is Hybrid type. In the Fabry Perot laser case [63] the cavity is defined by cleaving the facets.

For an SOA[27] made with Si-Hybrid technology, such transitions of Si-guide to Hybrid-guide and reverse are unavoidable and the results we found here for Si-guide to Hybrid-guide to Si-guide transition can be of critical importance in an amplifier operation. In fact if the power generated in the III/V stack fails to couple back to the Si-guide, as observed here for the passive simulations, such an SOA design would fail to function, unless carefully designed tapers are used as shown in the pre-amplifier design of [70].

Alternatively, if the loss experienced in Hybrid-guide to Si-guide transition is in the form of reflection back into Hybrid-guide (some of it will be lost due to scattering at the transition), then assuming the power reflection of 20%, it could in fact function as a mirror and be used to define the cavity for lasing operation, rather than having the need to cleave that facet which renders the device as non-integrable. Further studies are required to verify these conclusions.

2.3. Conclusion

In the Hybrid Evanescent approach, only the race-track/ring cavity lasers have the utmost important integrability feature, as the cavity for Fabry Perot counterpart needs to be defined by dicing through the waveguides. The race-track structure needs to have large bends due to the loosely coupled nature of the mode. We suggested in order to reduce the footprint of the laser, Si-guides may be used instead of Hybrid-guides in the bend area to provide a confined mode which would have from lower loss, and thus bend radius can be much smaller.

[27] SOA stands for Semiconductor Optical Amplifier.

However, according to the simulations done in this study, we observed that each Hybrid-guide→Si-guide→Hybrid-guide transition introduces about 20% (1dB) insertion loss in optical mode. A race-track structure should have two of those transitions in order to make the bend curvature small. This results in about 2dB insertion loss in total. It is worth mentioning here that work by E. Barkley in our group has shown that the coaxial coupling loss from a SiON waveguide to a III/V guide can be as low as 1dB for gaps filled with air and will be lower for gaps filled with a higher dielectric constant material [59]. Thus in terms of losses, coaxial approach is comparable to, and potentially better than, the evanescent approach.

2.3.1. Coaxial vs. Evanescent Coupling Integration Approaches: Strengths and Limitations

Limitations of the Hybrid-Evanescent approach can be summarized in distinctive categories of: coupling loss (already discussed), heating, footprint, bond delamination, limited wavelength range, integration with electronics, reflection/scattering at Si-Hybrid transition interfaces, and threshold currents.

- **Heat Transfer**

Regarding the heating issue, in the Hybrid-Evanescent structure, the III/V active region is cooled via the relatively narrow Si-ridge-guide underneath it. Thus the heat sinking of the active region is rather poor and the structure will experience heating roll-off in the L-I curve of the laser relatively quickly. Therefore, the maximum operating temperature will be reduced, as seen experimentally where T_{max} is about 40-45˚C for Hybrid Evanescent Fabry Perot cavity laser [63], [49]; while the industry requirement for commercial laser diodes is the operation up to at least 70˚C.

As expected, the low maximum temperature of 40°C is caused by poor heat extraction of the active region and heat generation in series resistance of thin n-InP layer. Analyzing L-I roll off and I-V curve has shown thermal resistance of 40°C/W for the structure. Reducing the buried oxide thickness, heat sinking top of the laser, and moving the n-contact closer to the center might decrease the thermal resistance of the structure, but probably not significantly.

It's worth mentioning that lasers made by J. Rumpler [60] for the purpose of coaxial integration, show maximum operating temperature of 85°C which is well in range with the commercial requirement.

- **Heating in Carrier Paths**

Another issue is high loss due to very thin lateral carrier pathway to n-ohmic contacts. Also finite element thermal modeling of the structure [71] has shown that the heat generated in the p-InP region is even higher than the heat generated in the active region.

- **Modal Loss**

In the Hybrid Evanescent approach, the optical mode sees n-InP and this increases optical loss, which leads to an increase in the threshold current.

Furthermore, as our simulations have shown, there is significant insertion loss at the Hybrid-Si transition interfaces.

- **Footprint**

Our simulations have implied that a minimum length of 200μm is needed so that the mode is fully coupled to the QW layer of III/V. This will increase the length of the laser, while large footprint is not welcome in ultra high volume integration in ICs today.

Due to the bonding of InP and Si substrates, the fabrication yield will decrease during facet polishing of edge emitting structures. Meanwhile, in race-track structure (the only Hybrid-Evanescent laser structure that is suitable for photonics integration), where no facet polishing is needed, large bend diameters are essential which make the footprint of the structure very large. The large bend diameter (>150μm) requirement is mainly due to the loosely guided nature of mode inside the hybrid structure.

Also due to the evanescently coupled nature of Hybrid Evanescent approach, modal gain is low (due to smaller (about one third[28]) quantum well overlap), and thus the foot print of the device would be larger in return.

Comparing the 800μm length of the electrically pumped laser in Evanescent approach [63] with 300μm edge emitting lasers made by Joseph Rumpler [60], shows about 3 fold

[28] Refer to Appendix I for this estimate.

difference in foot print. Moreover, the race-track structure (which is integrable) has a foot print of about 1250×500 μm^2 which is quite large.

Apart from using up the real-estate on IC surface due to a large footprint, having a long device will increase the threshold current of the laser[29] and increases power consumption which is definitely not welcome in integrated circuits.

- **Threshold Current**

Due to low overlap with active region and large device footprint, I_{th} is quite high in lasers made with Hybrid Evanescent approach. Industry requirement for commercial laser diodes is I_{th}<20mA, where as Fabry Perot laser has I_{th}=65mA [63] and the race-track laser has I_{th}=175mA [66]. In the coaxial coupling approach, since these two issues are not present, I_{th} of 17mA and 19mA were observed for pulsed and CW operation (see Chapter 6 of this thesis), which satisfy the commercial requirement on threshold currents.

- **Wavelength Restriction per Bonded III/V Substrate**

The Hybrid Evanescent technology restricts the operating wavelength of a laser structure due to the requirement of bonding one separate III/V stack to the Si substrate for each wavelength. This poses a problem where multi wavelength array of integrated lasers is essential. QW intermixing can address this issue to some extent but it cannot achieve a wide wavelength sweep. If a wider range of wavelength tuning is required in a transceiver chip, multi-layer bonding techniques must be employed in order to bond different stacks of III/V material systems on one Si substrate.

- **Use of SOI Silicon and Issue w/ Integration with Electronics on Chip**

Another major issue arises when Hybrid Evanescent structures are to be integrated with electronics on a chip. Since CMOS transistors on SOI will have microns of height, and in Hybrid Evanescent approach ridge structure of the Si-guide is made at the same layer of transistors, mesa etching is needed and significant difficulties with non-planar wafer bonding will rise.

[29] See Appendix I for threshold current calculation of this race-track laser.

- **Single Mode Operation Tradeoff vs. Bond Delamination**

Dicing and polishing the facets in Fabry Perot lasers made with this approach reduces the yield considerably if the Si-ridge is narrow (≤2.5μm) due to bond delamination. However in order to achieve single mode operation ridge width needs to be ≤2.5 μm. This tradeoff in yield will pose a hurdle in reliable manufacturing of devices in this approach, unless a race-track structure is used.

Overall, the Hybrid Evanescent approach is promising and has a potential for photonics integration. However in certain areas like heat transfer, footprint, flexibility in selecting a wide range of wavelengths for various devices to be integrated on a single chip, planarity, ease of integration with CMOS electronics on chip, and the robustness of manufacturing process, we believe the coaxial approach is quite strong and seems a great solution for lasers integrating on Si ICs.

Chapter 3

Design and Optimization Simulations

Before embarking on the fabrication of coaxially integrated structures[1], an extensive amount of effort[2] was dedicated to design the components of this structure. More specifically, the dielectric waveguide dimensions and refractive index were to be optimized, as well as the refractive index of the filling material of the gap (between the dielectric waveguide and III/V ridge waveguide, as shown in Figure 3- 1). Then design and optimization of a Distributed Brag Reflector (DBR) as part of the dielectric waveguide structure was explored. The use of such a DBR structure can compensate for the higher Fabry Perot cavity mirror loss, α_m, in the case that higher refractive index filling is used for the gaps. DBRs can also help in ensuring a single mode beam at the output facet of the chip, if their bandwidth is narrow enough to filter the adjacent cavity axial modes.

[1] It is worth reminding that in the coaxially integrated structure demonstrated in this thesis, a SiON/SiO_2 dielectric waveguide (fabricated on the Si substrate) is end-fire-coupled (via a gap) to a III/V (InGaAs/InP) ridge waveguide edge emitting laser. For the case of an SOA version of this structure, the amplified optical mode, at other end of the III/V gain component sees the same gap and is coupled back to another SiON waveguide.

[2] The material that is presented in this chapter discusses the simulations that were performed by the author of this thesis.

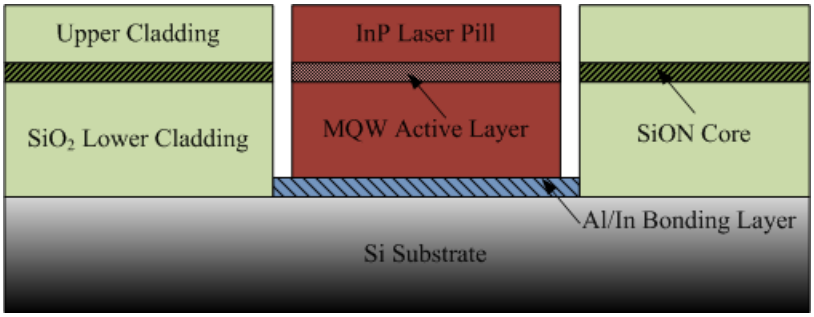


Figure 3- 1: Schematic showing the coaxial recess integration approach, where a laser platelet is integrated in a recess etched out of SiO_2 and is coaxially coupled to SiON/SiO_2 waveguide via a gap.

In this chapter, first in order to find the optimum gap filling material to achieve highest transmission (and lowest reflection subsequently), simulations were carried out via 2D FDTD, the results of which are presented in Section 3.1. Next, Section 3.2 discusses the motivation for using a Distributed Bragg Reflector (DBR), followed by Section 3.3 where the results of FDTD simulations to design such a DBR structure on the dielectric waveguides of this project are presented. The inflexibility of this 2D FDTD solver, made us to look into other modeling approaches, for instance the Transmission Matrix Method (TMM) which proved to be quite flexible and adjustable for our optimization purposes. In Section 3.4, through simulations based on TMM, the transmission and reflection frequency spectrum were looked into and used for the grating design. A sensitivity analysis was carried out to measure the sensitivity of the reflection spectra to fabrication variations (e.g. grating pitch length variation) and the results are described. Finally, in Section 3.5, the DBR design was more rigorously optimized using bidirectional BPM simulations via BeamProp from Rsoft. Section 3.6 concludes this chapter with a summary of the findings, as well the discussion of the application of the designed DBRs in the coaxial integration project.

3.1. Waveguide and Gap Filling Optimization: Dimensions, and Refractive Indices

As discussed earlier, the first set of optimization attempts were geared towards maximizing the coupling between the dielectric and III/V waveguides. Such optimization entails finding the best dimensions for each waveguide and the best filler material for the air gap between them. For instance, initially the simple 1D vertical mode profile of the two guides were compared as shown in Figure 3- 2. The core height and waveguide core and cladding refractive indices used in these simulations are listed in Table 3- 1.

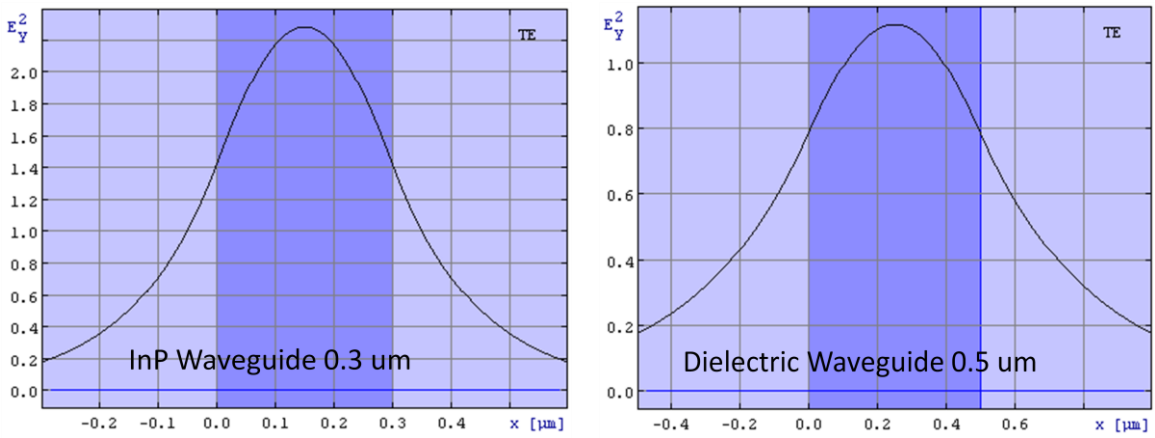


Figure 3- 2: One dimensional mode shapes found for laser and dielectric waveguides with core heights of 0.3µm and 0.5µm respectively.

	Dielectric Waveguide	III/V Laser Waveguide
Core Height (µm)	0.5	0.3[3]
Core Material	SiON	InGaAsP/InGaAs
Cladding Material	SiO_2	InP
Core Refractive Index	1.6	3.43
Cladding Refractive Index	1.45	3.14

Table 3- 1: Waveguide parameters used for finding the mode shapes shown in Figure 3- 2.

[3] This corresponds to the 0.27µm height of active region in the MQW layer structure of the laser diode discussed in Chapter 4.

In order to quantify the coupling between the two waveguides based on the height of the dielectric waveguide core and its refractive index, as well as the gap refractive index, Finite Difference Time Domain (FDTD) simulations were used.

For the end fire coupling between SiON and III/V waveguides, there is an inevitable gap[4] across which the photonic mode would propagate unguided. Therefore in order to optimize for the maximum coupling of the SiON waveguide - gap - III/V waveguide structure, the gap filling is an important component. A 2D FDTD simulator[5] was used for this purpose. The input to this solver is a text configuration file describing the position and refractive index of dielectric objects present in the simulation window, as well as the descriptions of a source wave. For the source, a Gaussian pulse at 1.55μm center wavelength and pulse width of 150fs was used, whose shape is matched with the fundamental mode of the input waveguide. Since the simulation is done in the time domain, it needs to run long enough so that the source wave propagates all the way through the initial SiON waveguide, scatters in the gap, and then gets coupled to the III/V waveguide. Absorbing boundary conditions were used to avoid reflections from the edges of the limited simulation window dimensions. The FDTD simulations done with this script have three output results, T (transmission coefficient), R (reflection coefficient) and time varying snapshots of the propagated optical fields[6]. The T and R coefficients are based on the coupling to the fundamental mode of the second and first waveguides respectively. The sequence of field snapshots in Figure 3- 3 shows one example of how the source wave propagates through the SiON waveguide, passes the gap unguided, and then couples to the III/V waveguide. Parameters used in this case are the same as before (Table 3- 1), except that the dielectric waveguide core height is 0.7μm, and the gap filling as well as the background refractive index are the same as the dielectric waveguide cladding i.e. $n_{gap} = n_{background} = n_{clad}=1.45$. The dielectric waveguide is on the left and the III/V is on the right of the simulated structure. The incident vertically-Gaussian field is propagating from left to right, i.e. it couples from the dielectric waveguide to the III/V guide[7]. Note that images start from the left hand side, and by

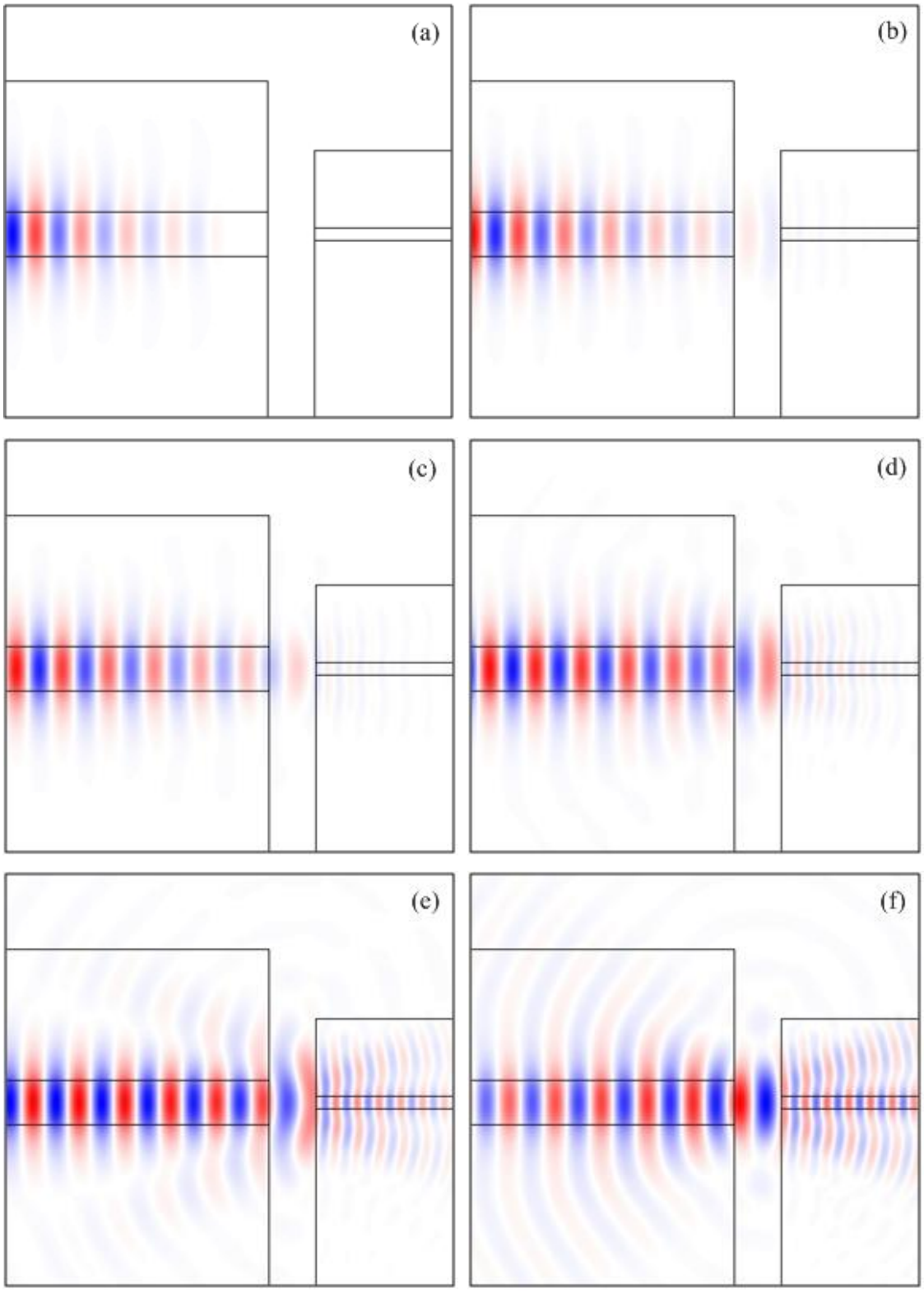
[4] Depending on what recess lengths are used to assemble the laser pills, this gap length varies. However it was observed that on average, a gap spacing of 1-2μm is typical, with the range from 0 to 7-9μm.

[5] The script for this simulator had been developed by Christina Manolatau and Milos Popovic in Prof. Ippen's research group at MIT and was generously shared with us.

[6] The snapshots are displayed for the electric field for TE, and the magnetic field for TM simulations.

[7] The reverse direction of coupling is shown in the upcoming simulations; however the expectation is that since the coupling integral is mutual and does not depend on the direction of propagated wave, the results should be close. This strictly holds for the case of end-fire coupling without any gap between the two waveguides. However when a gap is present, the scattering due to unguided nature of gap will make the transmission/reflection results different in the two cases of Si guide → III/V versus III/V guide → Si guide.

following the sequence, propagation along the dielectric guide, reflection from SiON facet, propagation in air gap, and coupling to III/V guide are noticeable.



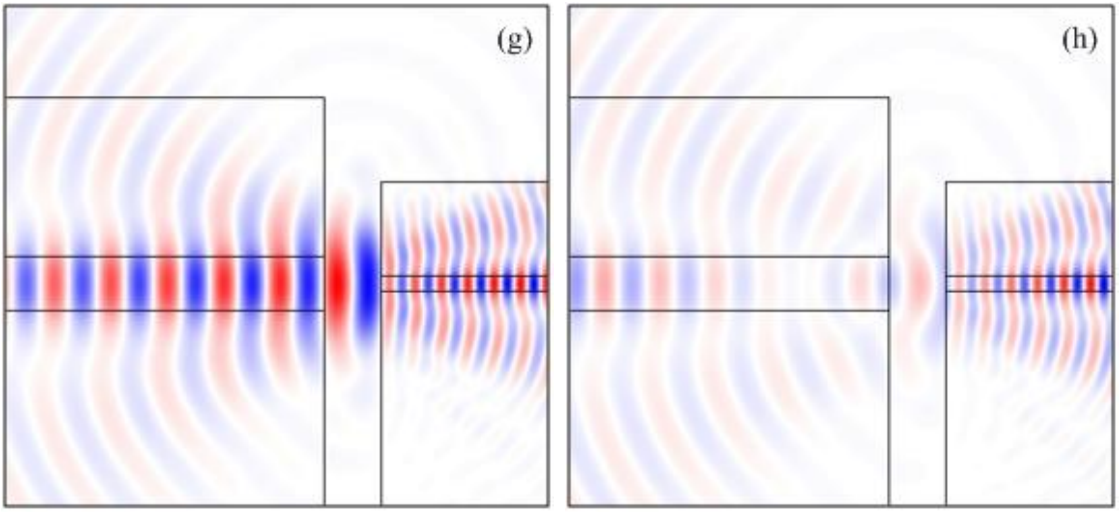


Figure 3- 3: FDTD snapshots of the field being launched from SiON waveguide on left (a), propagating along the dielectric waveguide (b,c), seeing the gap and getting reflected (d,e,f), and coupling to the laser waveguide on right (g,h).

To find the optimized dimensions and gap filling material index, a set of joint simulations were carried out. For the dimensions, three cases for the dielectric waveguide and two cases for the semiconductor waveguide have been looked into as summarized in Table 3-2. For the dielectric waveguide, the three options of B_1, B_2 and C were chosen based on the available refractive indices of SiN, SiON and SiO_2 (n=2.2, 1.6, 1.45 respectively). The core height was varied from 0.2µm, a close match to the thin laser active region, to a thicker case of 1µm. For the laser waveguide, since the MQW layer structure was rather fixed as it was ordered from an outside vendor, A_1 and A_2 differ only slightly in core height.

Type	Tag	Core Height[8]	n_{Core}	$n_{Cladding}$
Dielectric Waveguide	B_1	0.2µm	2.2	1.6
	B_2	1.0µm	2.2	1.6
	C	0.5µm	1.6	1.45
III/V Waveguide	A_1	0.2µm	3.43	3.14
	A_2	0.3µm	3.43	3.14

Table 3- 2: Simulated dielectric and laser waveguides with different core heights and refractive indices.

[8] Since these FDTD simulations are 2D, "h" stands for the core height of the waveguides.

Using the above waveguide options, FDTD simulations of coupling in the cases of $C \rightarrow A_1$, $C \rightarrow A_2$, $B_1 \rightarrow A_1$ and $B_2 \rightarrow A_2$ have been performed and transmission and reflection coefficients were derived.

Gap filling indices of n_{gap} = [1, 1.45, 1.6, 2.2, 3.14] were simulated with each waveguide combination, and the gap length was changed from 0.5μm to 4μm.

As an instance of the results, transmission and reflection for the case of $C \rightarrow A_2$ (which is exactly the case that was eventually selected and fabricated for the final structure) for different gap filling indices is depicted in Figure 3- 4.

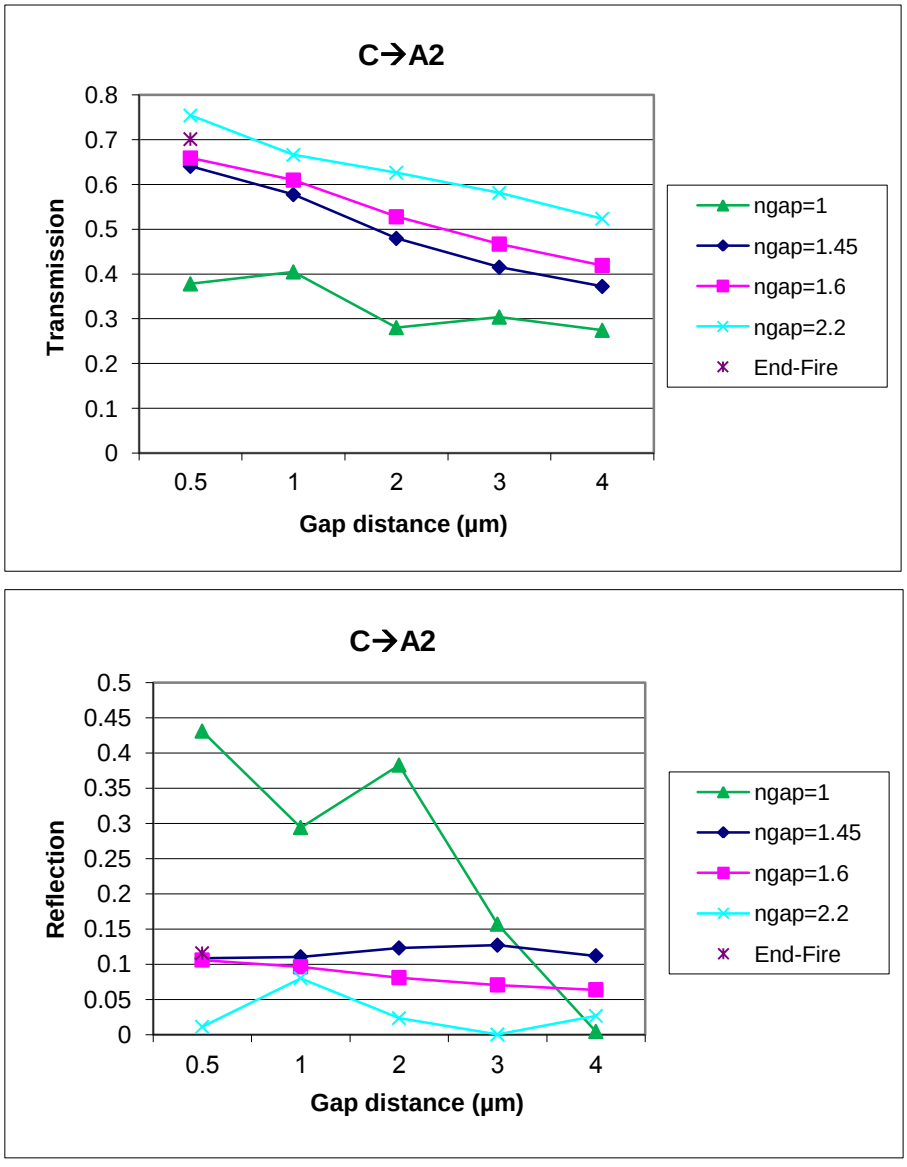
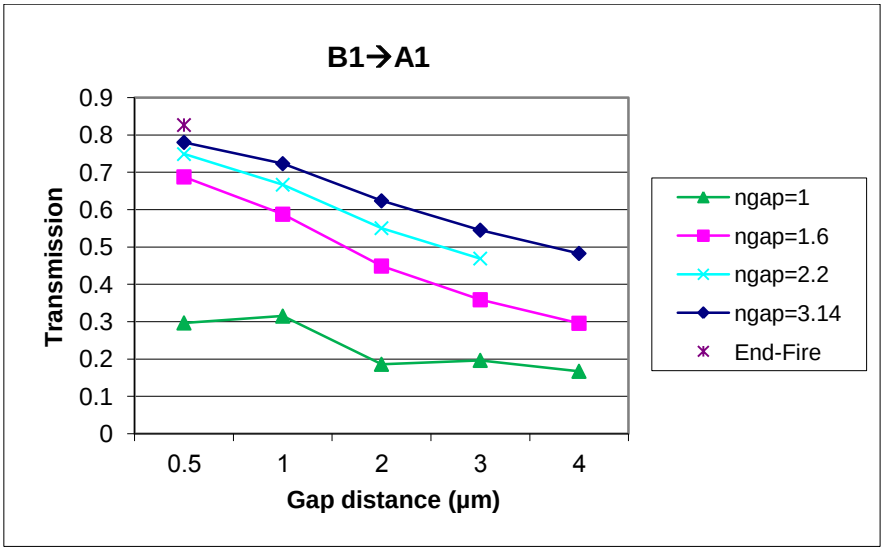


Figure 3- 4: Transmission and reflection coefficients found for different gap filling indices, for the case of $C \rightarrow A_2$ for dielectric and laser waveguide pair.

As the results above show, the higher the refractive index of gap filling, the higher the transmission and the lower the reflection. This trend was observed for all the cases of $C \rightarrow A_2$, $B_1 \rightarrow A_1$ and $B_2 \rightarrow A_2$ (as seen in Figure 3- 5 and Figure 3- 6).

It is worthy to note that no filling (air with $n_{gap}=1$) shows the highest reflection, which is the case for the current state of our integrated structures discussed in Chapters 5 and 6. Therefore an enhancement of performance and higher coupling efficiency is expected if a higher refractive index gap filling material is added in the spacing between the dielectric $SiON/SiO_2$ waveguide and the InGaAsP/InP semiconductor guide.

The transmission and reflection coefficient results for the two other cases of $B_1 \rightarrow A_1$ and $B_2 \rightarrow A_2$ waveguide pairs are shown in Figure 3- 5 and Figure 3- 6, in which the dielectric waveguide has higher core and cladding refractive indices (2.2 and 1.6 respectively). In these simulations an even higher gap filling with $n_{gap}=3.14$ was added for the comparison. The same trend of highest transmission for the highest gap filling index, and worst transmission for an air gap is observed here as well. However, since the refractive index step of $n_{gap}=3.14$ with $n_{core}=2.2$ is high, the reflection in this case is not the lowest necessarily; instead $n_{gap}=1.6$ gives the lowest reflection since it is the closest to the core index, consistent with what is expected from the Fresnel reflection coefficient that depends on the difference between the refractive indices of the two materials at an interface.



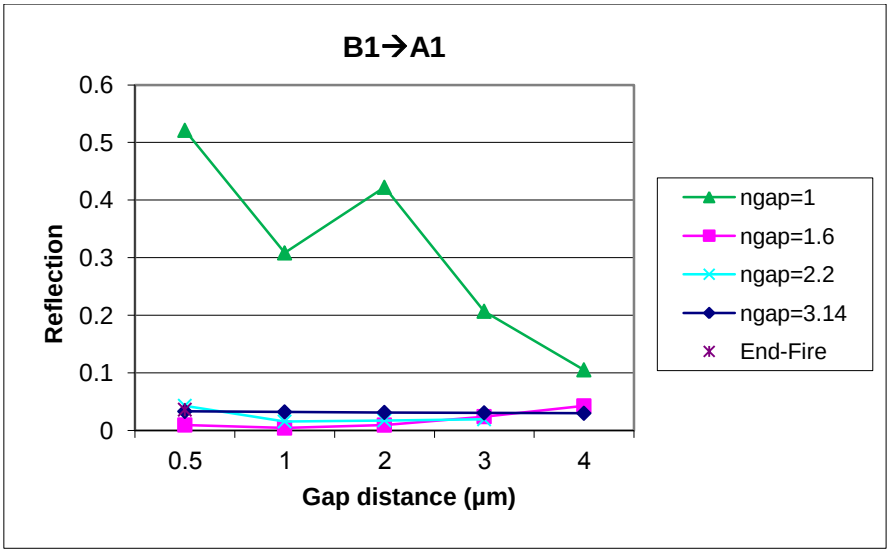
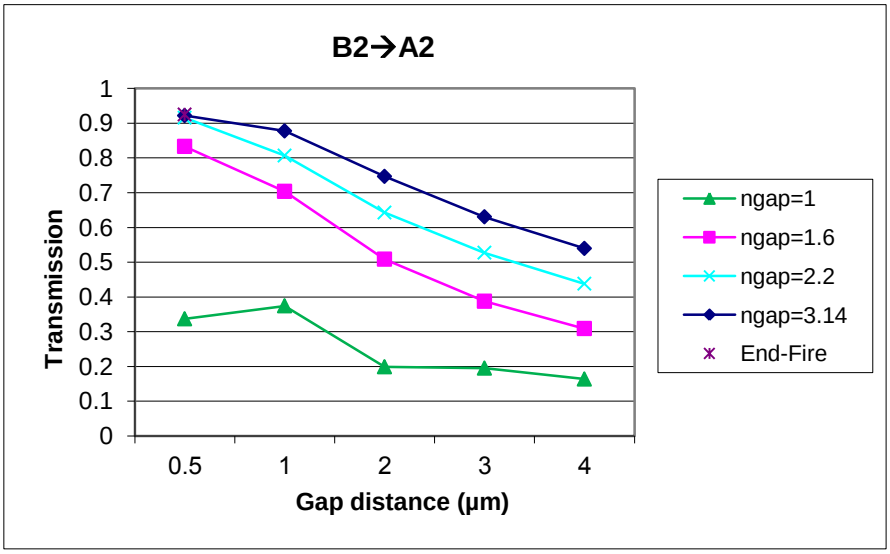


Figure 3- 5: Transmission and reflection coefficients derived for the $B_1 \rightarrow A_1$ coupling case.



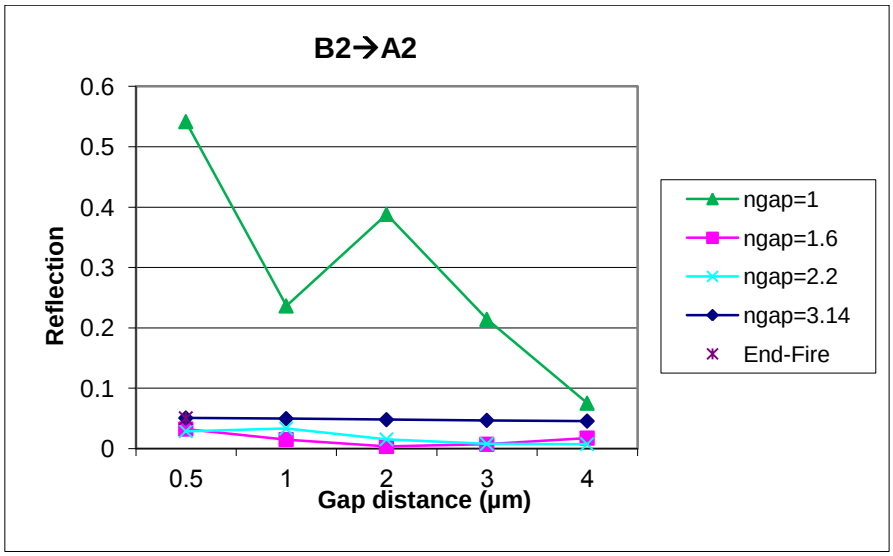
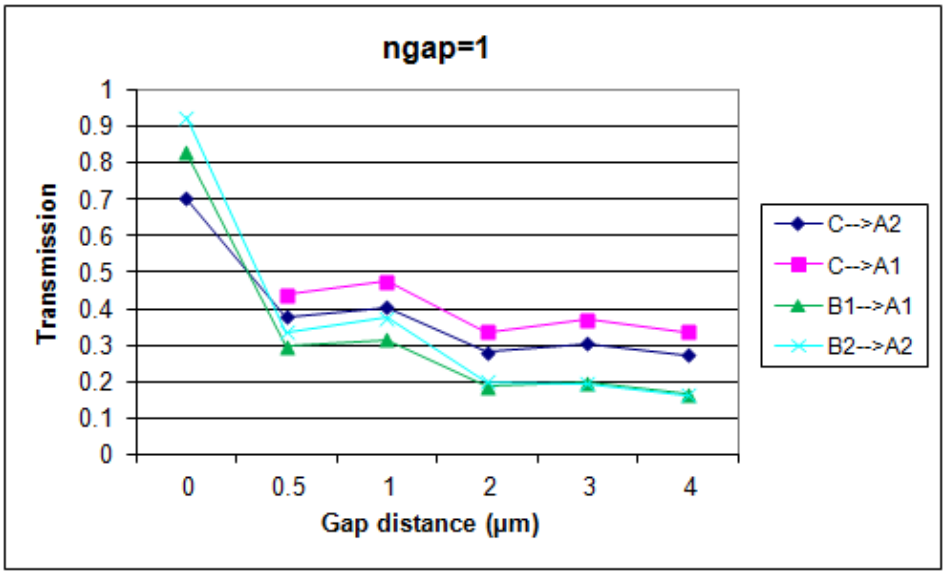
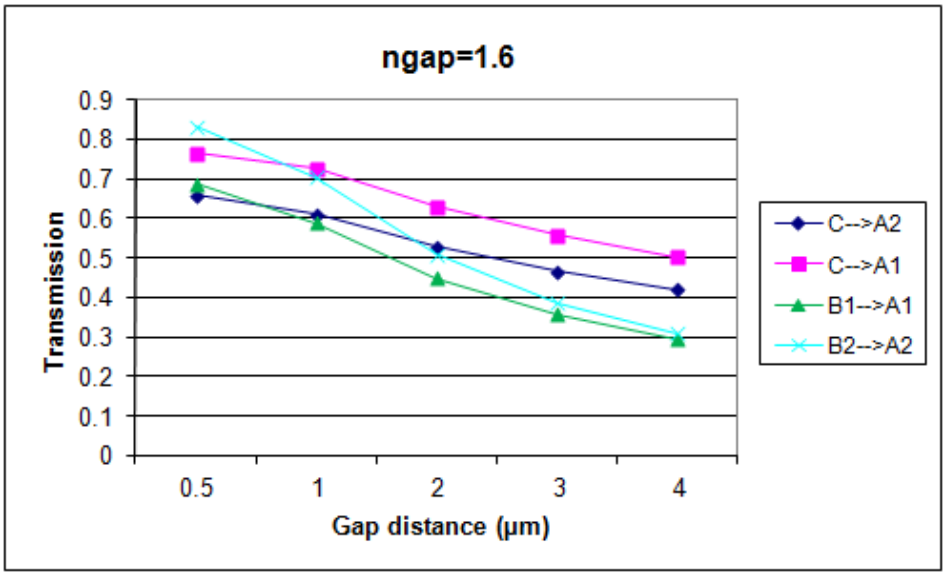


Figure 3- 6: Transmission and reflection coefficients derived for $B_2 \rightarrow A_2$ coupling case.

In order to decide which waveguide combination gives the highest coupling, for each gap filling the transmission coefficients are compared as shown in Figure 3- 7. The coupling transmission coefficients suggest that C→A_1 gives the highest coupling for all gap fillings for practical gap lengths (>0.5µm)[9]. It might not be redundant to recall that C is the lower index dielectric waveguide (core: n=1.6, cladding: n=1.45) rather than the higher index cases of B_1 and B_2 (n_{core}=2.2, $n_{cladding}$=1.6). In fact, based on these results, this lower index option for the dielectric waveguide was selected for fabrication, and thus the dielectric guides in this project have the cladding of SiO_2 with n=1.45 and core of SiON with n=1.6.





[9] The core height of the laser active region is 0.27µm and is closer to A_2 rather than A_1. However since laser epitaxial structure was purchased from an outside supplier, A_2 core dimension was available and hence was used in the fabrication and integration process.

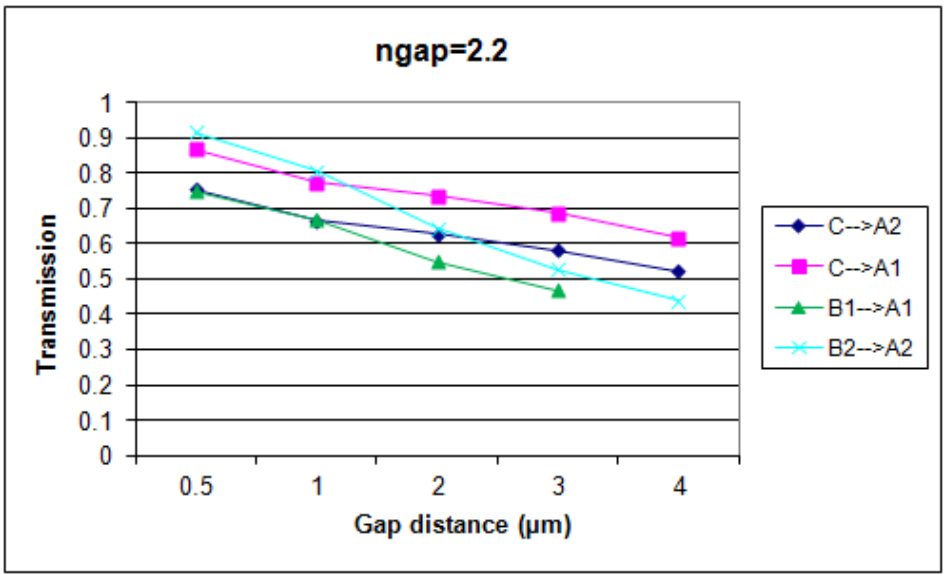


Figure 3- 7: Transmission coefficient found for four coupling pairs of C→A_2, C→A_1, B_1→A_1 and B_1→A_2, for different gap filler indices of n_{gap}=1, 1.6 and 2.2.

Since the C→A_1 case of coupling seemed optimal, we also looked into the reverse coupling of A_1→C to investigate the behavior of coupling back from the semiconductor waveguide to the dielectric one. This comparison can also investigate the reliability of FDTD results and see if they are relatively compatible[10] with the theoretical expectation of same coupling values from overlap integrals, which is proven to be the case as shown in Figure 3-8[11].

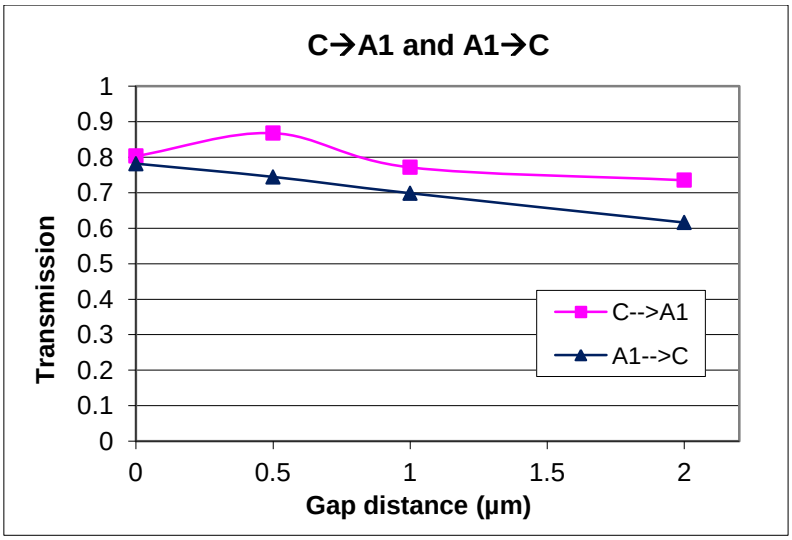


Figure 3- 8: Transmission coefficient derived for C→A_1 transition as well as the reverse case of A_1→C coupling.

[10] As discussed before, the unguided mode shape spreading in the gap area makes the case different from completely similar coupling that the coupling integral formulation suggests.

[11] It was found that if the distance of launch field and dummy field is kept constant, the results are more reliable compared to a case that dummy position is fixed.

In summary, in this section the optimization of dielectric waveguide and gap filling index was illustrated. Based on these results, a SiON/SiO_2 dielectric waveguide with n_{core}=1.6 and $n_{cladding}$=1.45 is selected for the final structure. Using a higher index gap filling (e.g. n=1.45) would increase the coupling efficiency compared to the natural air gap that is currently present in the integrated structure.

In the next sections, design and optimization simulations to include a DBR structure with these dielectric waveguides will be discussed using FDTD, TTM and BPM methods.

3.2. DBR Motivation

The idea behind Distributed Brag Reflectors (DBRs) is that many small reflections add up constructively at a certain frequency and thus the structure gives a large net reflection coefficient. Therefore, such a grating structure has an important application in both vertical cavity and in-plane laser diodes, but for slightly different purposes.

For in-plane lasers (the lasers used in this thesis), the axial modes are closely spaced since the Fabry Perot cavity is ≥100μm. Therefore a number of them fall in the positive gain part of the active region gain/loss spectrum. This results in multi-mode[12] lasing of these in-plane edge emitting lasers, which is often not desirable.

In general, to ensure single mode lasing, the following options exist:

- Reducing L in the Fabry Perot cavity so that $\Delta\lambda$ gets larger and only one mode falls in the positive part of the gain spectrum (e.g. VCSELs)
- Making α_m a strong function of λ (e.g. with using DBR or DFBs)
- Making the width of the gain spectrum narrow so that only one cavity mode falls in the positive section of the gain spectrum. (i.e. Quantum dots and gas lasers)

Therefore, for an in-plane edge emitting laser, the introduction of a DBR structure to its external cavity is a great solution to achieve single mode operation. Essentially a well designed grating will introduce a large reflection (small α_m) for one axial mode near the gain maxima, and will filter out the rest of the nearby axial modes by imposing a smaller reflection (thus larger mirror loss (α_m)), resulting in a single mode operation.

[12] Note that these multi modes are axial/longitudinal modes due to the Fabry Perot cavity. They should not be confused with waveguide transverse modes, which can be limited to single mode if the transverse dimensions of the waveguide are designed to be small enough.

Figure 3- 9 shows an instance of the inclusion of a DBR structure in a GaAs based in-plane laser diode [73].

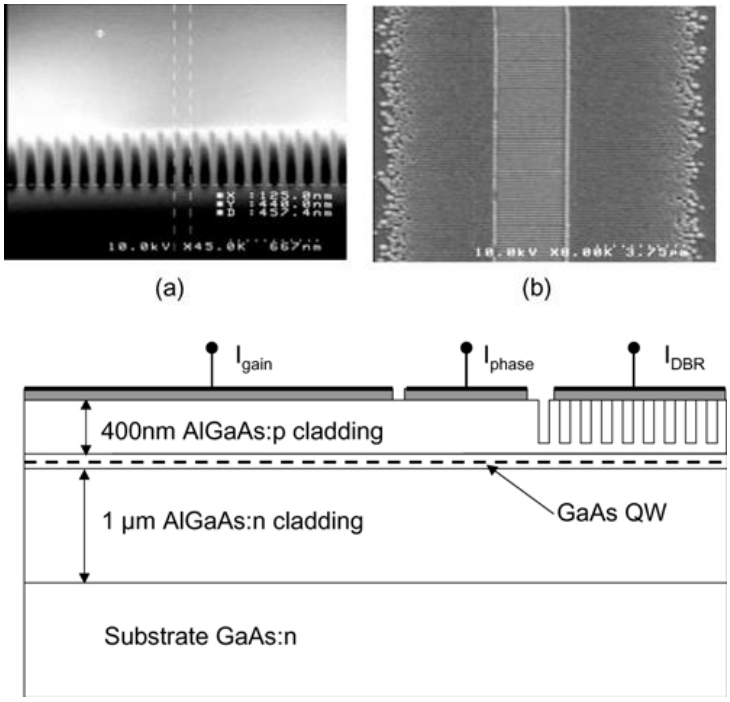


Figure 3- 9: SEM image of the (a) top view and (b) cross section of a DBR grating. The schematic diagram shows structure of the asymmetric-cladding DBR laser diode.

Conversely, in VCSELs the cavity is relatively short thus axial modes are well spaced from each other and most of the times only one falls in the positive gain spectrum of the active region. Therefore in VCSELs multi mode operation is less of a concern. However since the vertical cavity is quite short in VCSELs, it is of paramount importance that losses are minimized to be able to reach lasing for a low enough threshold current. Two factors contribute to the cavity loss, α_i (material intrinsic loss) and α_m (the mirror loss), where:

$$\alpha_m = \frac{1}{L}\ln\left(\frac{1}{R}\right)$$

In the equation above R is the intensity reflection coefficient of the ethalon, $R= r_1r_2$ where r_1 and r_2 are field reflection coefficients at each facet of the Fabry Perot cavity. With these losses, the condition that needs to holds for lasing is: $\Gamma g_{th} = \alpha_m+\alpha_i$.

For VCSELs α_m needs to be small and thus the mirror reflections need to be very large. Since the natural Fresnel reflection is relatively low, the introduction of a DBR in the vertical cavity is employed to achieve a high mirror reflection needed for lasing.

Overall, for each application, an extensive amount of work is dedicated to the design these DBR structures. For example, T. Murphy has dedicated his PhD thesis at MIT to the design and fabrication of these integrated gratings [74], and other instances of this type of detailed work in the design and optimization of DBRs are numerous in the literature. By the same token, we saw the need to optimize such a structure for our specific application of integrated in-plane laser diodes and thus the studies in the following sections were motivated.

More specifically, the structure we are dealing with in this thesis is an edge emitting in-plane Fabry Perot cavity laser, therefore for the reasons discussed above, in order to ensure single mode operation and suppress the rest of axial modes that see positive gain and tend to compete with the winning mode, we decided to adopt a DBR structure in the external cavity of the laser. Furthermore, the presence of such a DBR structure in the external cavity compensates for the higher mirror loss, α_m, if a higher index material is used for filling the air gaps. Essentially as shown in Figure 3- 10, a grating is to be fabricated on a section of the SiON/SiO_2 dielectric waveguide that is getting coupled to the laser ridge waveguide via a gap.

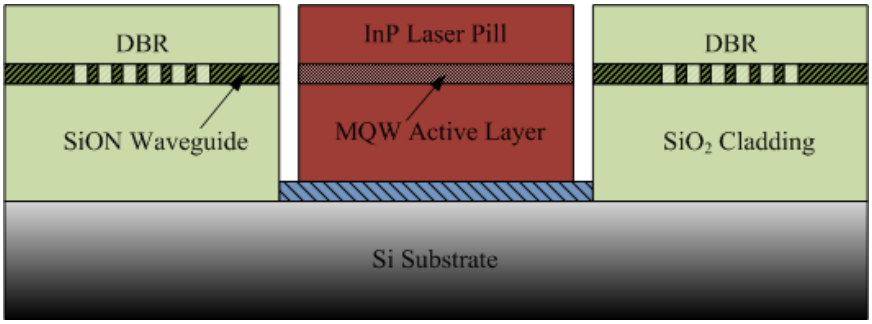


Figure 3- 10: Schematic showing the introduction of a DBR on a section of the SiON waveguides.

In order to design this DBR structure, three approaches were adopted in chronological order. First, the same 2D FDTD script that was used for optimizing dielectric waveguide dimension and gap refractive index was used to design the DBR structure. Since the input script for this solver was not user friendly and became exponentially complex when handling more advanced structures, the Transmission Matrix Method (TMM) was adopted next. This technique proves to be quite flexible and was used to optimally design a DBR in the complicated structure of SiON_guide → DBR → SiON_guide → Gap → III/V_guide → Gap →SiON_guide → DBR → SiON_guide , for different gap fillings, and various pitch heights and refractive indices in the DBR section. Furthermore, a sensitivity analysis was carried out to see how the spectral response varies with fabrication inaccuracies in pitch definition and

patterning. Finally, the Bi-directional Beam Propagation Method (BPM) was also used to design these DBRs. In the following sections the results of these three approaches are explained.

3.3. DBR Design via FDTD

As mentioned before, having a grating in the SiON waveguide provides a very high external cavity reflection at the Bragg frequency which ideally coincides with one axial mode of the laser cavity that sits near the active region gain peak, and thus single mode lasing is ensured.

For looking into the effect of such DBR, the first attempt was via FDTD (same script as the one used in Section 3.1), and Bragg gratings were introduced in the SiON waveguide only. It is important to bear in mind that simulations in this section do not see the semiconductor waveguide due to the limitations of the simulator. In subsequent sections, the results of simulations with better and more sophisticated methods will be presented.

To design a DBR one can recall that in order to have constructive reflections at Bragg frequency, the Bragg condition dictates that pitch period (Λ) for m^{th}-order grating needs to be:

$$\Lambda = \frac{m\lambda_0}{2n_{eff}}$$

Since for the first order Bragg grating, the diffraction efficiency is strongest, usually first order gratings (i.e. m=1) are preferred unless fabrication limitations require larger pitches and thus higher order gratings. Hence, for first order gratings, the pitch period is:

$$\Lambda = \frac{\lambda_0}{2n_{eff}}$$

And pitch lengths, as illustrated in Figure 3- 11, are:

$$L_1 = \frac{\lambda_0}{4\, n_{1\,eff}}$$

$$L_2 = \frac{\lambda_0}{4\, n_{2\,eff}}$$

where λ_0=1.55µm for the center lasing frequency that the InGaAs/InGaAsP MQW active region of the laser diode has been designed for.

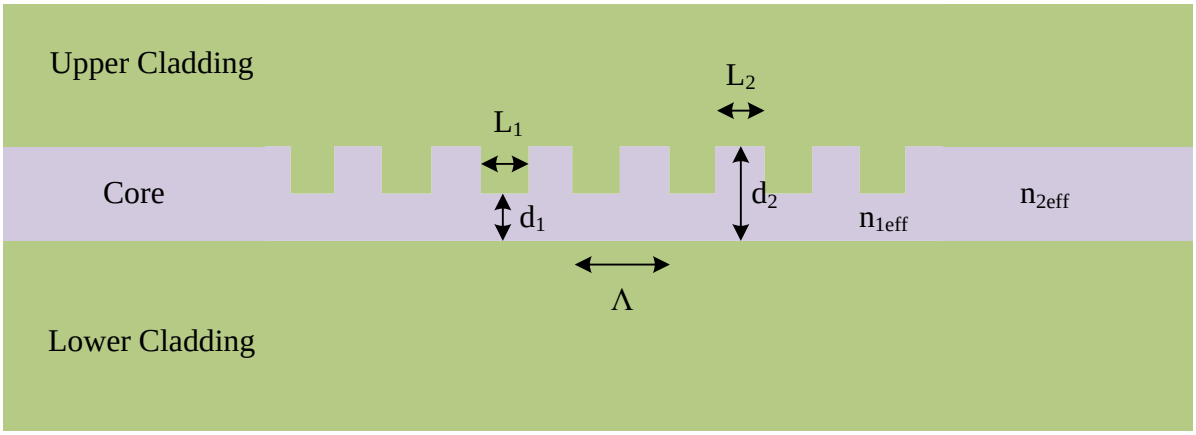


Figure 3- 11: Schematic clarifying the convention used here in referring to low pitch and high pitch parameters in DBR design. This structure is mostly identical to the simulated structure B (shown with pink squares in the upcoming graphs) where low pitch area has the same filling as the high pitch core (n=1.6) and d_1=0.3µm, where d_2=0.7µm.

Having these basics in mind to select the pitch length, the DBR on the SiON waveguide was structured in the FDTD input file and simulations were carried out to find reflection, transmission and scattering with different numbers of gratings (1 to 7). Regarding DBR pitches, the four cases listed in Table 3- 3 were simulated.

For all the four cases, d_2=0.7µm, $n_{2(core)}$=1.6 and $n_{2(cladding)}$=1.45, similar to the actual SiON/SiO_2 dielectric waveguides that were eventually fabricated by E. Barkley for this project. With these, the effective index of the high pitch region (denoted as #2 here), is n_{2eff}=1.5172, and thus L_2= 0.2554µm.

Regarding the L_1 dimension, first n_{1eff} is determined and then $L_1=\lambda_0/(4\times n_{1eff})$ is calculated. For instance, for the case D, n_{1eff} is simply 2.2 (due to the large height of the pitch in this case), and thus L_1= 0.1761µm, or for the case A, n_{1eff}=1.5 and thus L_1=0.2672µm.

DBR Tag	Color	Shape	d_1 (µm)	n_1
A	Blue	Diamonds	0	1.45
B	Pink[13]	Squares	0.3	1.6
C	Red	Squares	8	1.75
D	Green	Triangles	8	2.2

Table 3- 3: Four DBR designs with different pitch/grating filler refractive index and height.

[13] This case is most similar to the schematic illustrated in Figure 3- 11.

For each case videos were created showing time domain propagation of waves along the DBR structure. Figure 3- 12 shows the snapshots of FDTD wave propagation for three cases of DBRs listed in Table 3- 3 as A, B and D. (Note that the structure of C looks like D, only the pitch filler index is higher.)

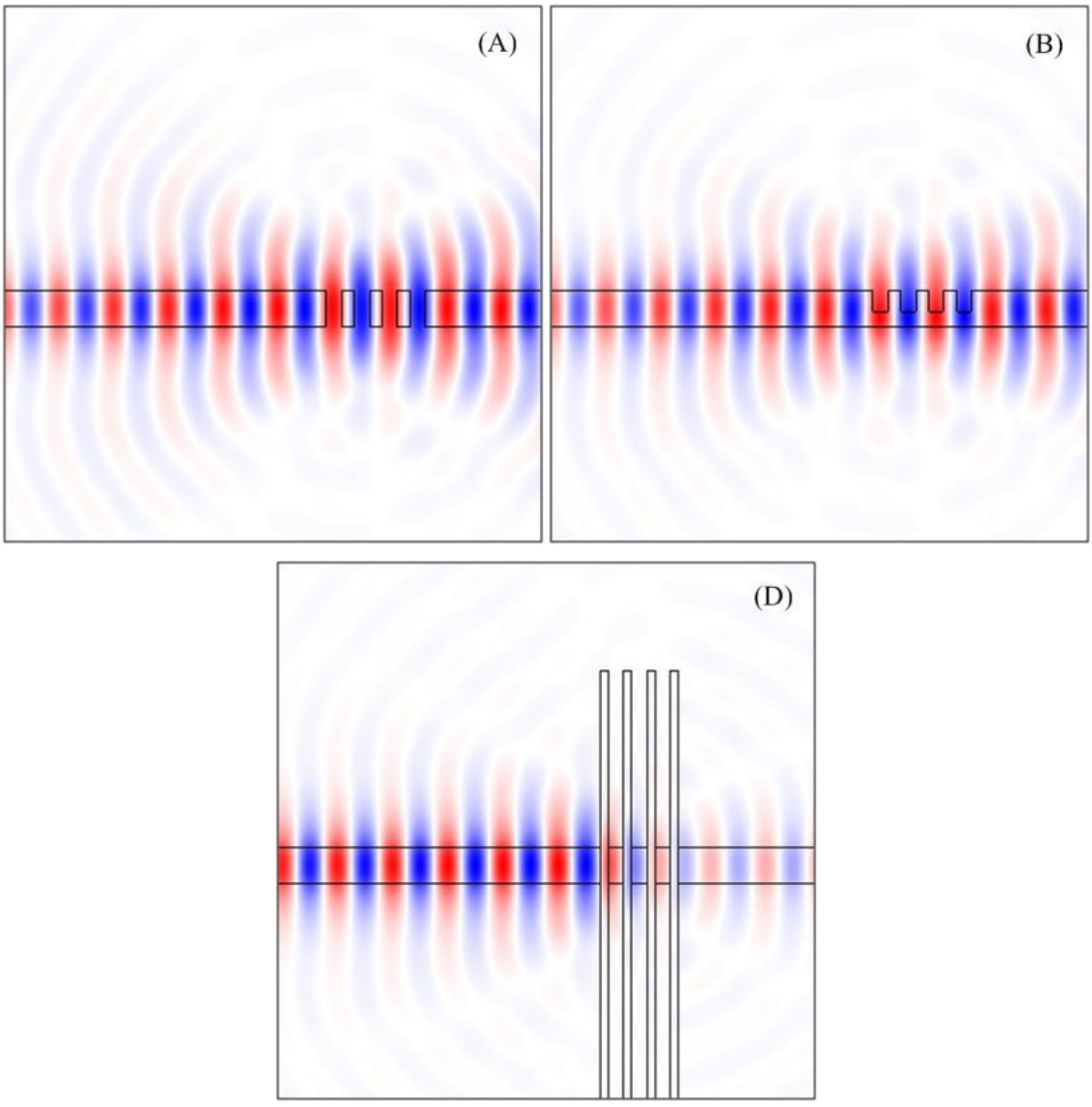


Figure 3- 12: FDTD field propagation snapshots for three different DBR design cases of:

Case A, where d_1=0.0μm, n_{core}=1.6, $n_{cladding}$=1.45

Case B, where d_1=0.3μm, n_{core}=1.6, $n_{cladding}$=1.45

Case D, high index pitch filling, d_1=8μm, n_1=2.2

In Figure 3- 13, the reflection and transmission coefficient output[14] of these FDTD simulations are given for different numbers of gratings for the cases of A and B designs (abrupt (d_1=0) and non-abrupt (d_1=0.3µm) gratings respectively). It is noticeable that for the case A (blue graph, abrupt gratings), fewer numbers of periods are needed for a same desired reflection coefficient which is expectable due to higher refractive index contrast per pitch.

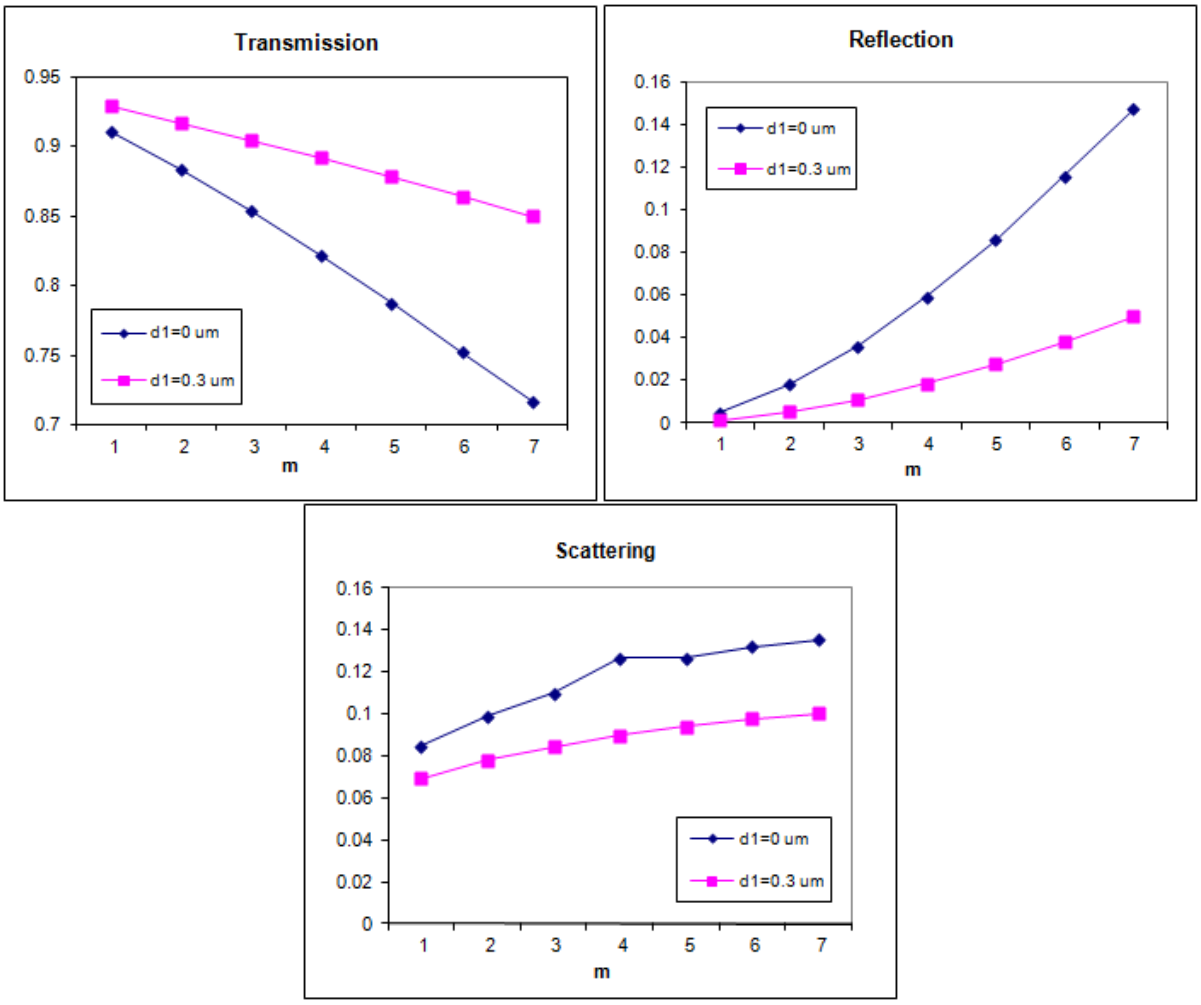


Figure 3- 13: Reflection, transmission and scattering results for two different cases of A: (blue diamonds) abrupt gratings (d_1=0), and B: (pink squares) non-abrupt (d_1=0.3µm); while d_2=0.7µm for both cases.

As simulations suggest, the abrupt DBR structure gives higher reflection for lower numbers of gratings. Then the next question is what index should be used for the grating fillings. To address this question, another set of design optimization reflection-transmission curves for different DBR pitch fillings is shown in Figure 3- 14, for the cases of A: n_1=1.45, C: n_1=1.75, and D: n_1=2.2 versus the numbers of gratings. Since the SiON waveguide has

[14] Scattering is defined by S=1-T-R.

refractive indices of n_{core}=1.6 and $n_{cladding}$=1.45, it is expected that the highest grating filling index (D: n_1=2.2) gives the highest reflection increase for each incremental number of gratings. The results compared in the graphs below strongly support this expectation; and this high index pitch filling proves to give the highest reflection for each number of gratings. Also, as 1.75 and 1.45 are equally different from 1.6, those two cases show a similar incremental drop in the transmission with increasing m (numbers of gratings). However, the lower index case of n_1=1.45, does generally have less transmission and reflection but more scattering, due to lower effective refractive index and thus opening up the mode.

In general, through these types of design curves one can choose the right number of grating periods and the filling material for a desired reflection coefficient based on details of the Fabry Perot laser diode dimensions and gain/loss parameters.

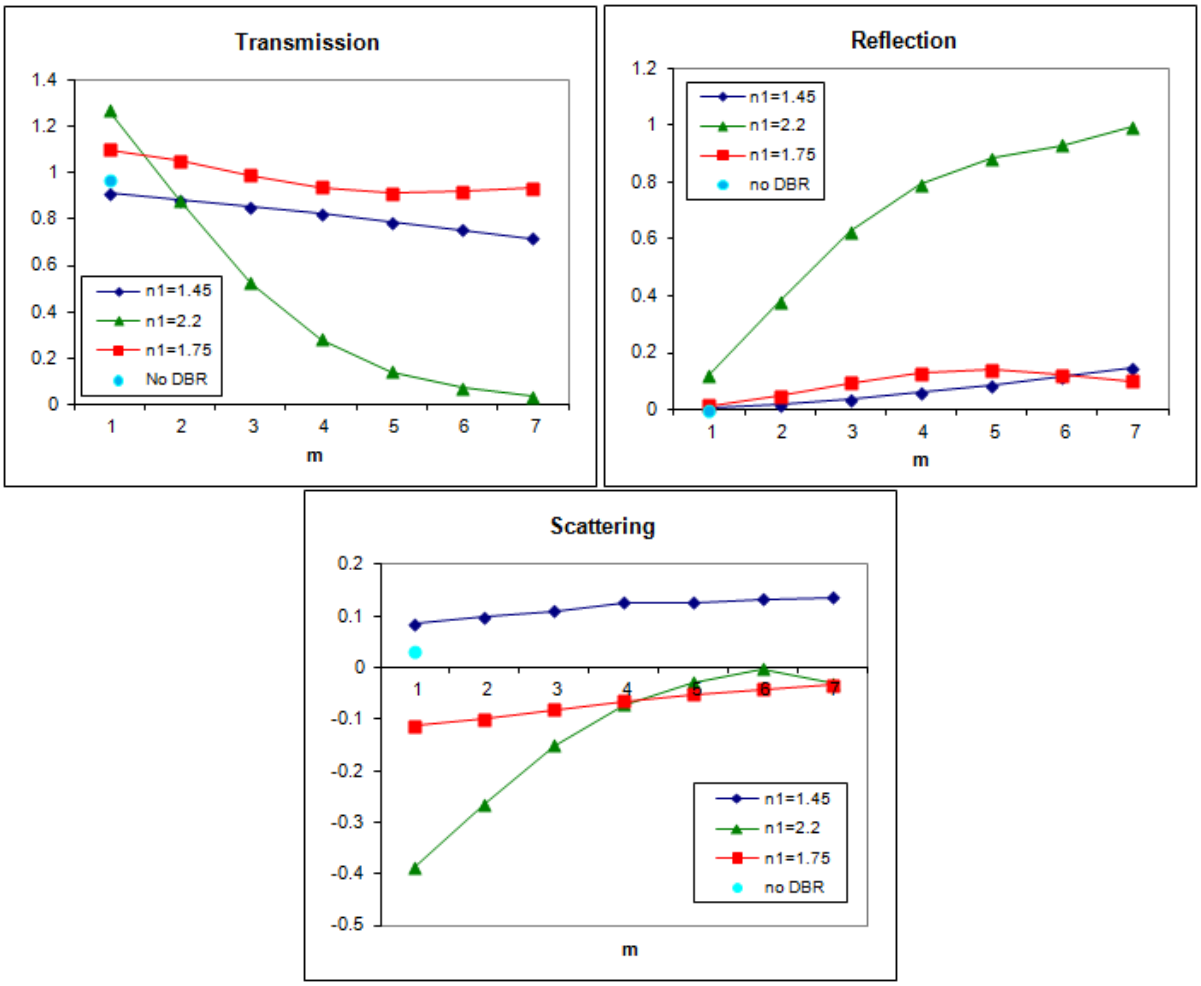
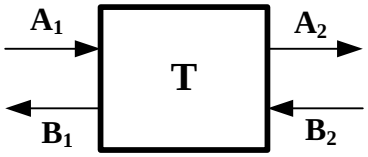


Figure 3- 14: Reflection, transmission and scattering vs. different numbers of grating periods (m) for three different cases of abrupt gratings, all with d_2=0.7um and n_2=1.6, (n_{2eff}=1.5172) and various pitch fillings: A: Blue diamonds: Low index, n_1=1.45 (same as background/cladding), d_1=0, C: Red squares: Medium index, n_1=1.75, d_1=8um, D: Green triangles: High index, n_1=2.2, d_1=8um.

3.4. Transmission Matrix Method: Design and Optimization Simulations

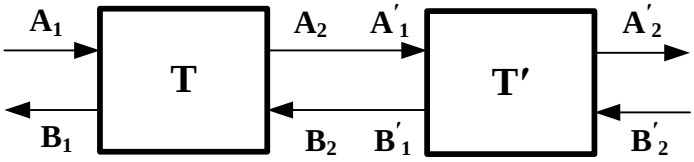
Although the preliminary DBR designs were done through FDTD, as discussed in the previous section due to the very limited capabilities of the solver, the structure was simple and composed of a single SiON waveguide. Adding other segments of the real structure such as the coupling gap, III/V laser cavity guide and another coupling back to a dielectric waveguide through a gap, was too complex to be handled in the FDTD solver that we had on hand. Therefore, Transmission Matrix Method (TMM), coded via MATLAB, was chosen as a better, more flexible and robust alternative approach for modeling the introduction of DBRs to the integrated structure of "SiON guide + gap + III/V guide + gap + SiON guide". In fact through this setting, a range of diverse cases have been looked into.

In Transmission Matrix Method, each structure segment is simulated by its two port transmission matrix representation.



$$\begin{bmatrix} A_1 \\ B_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} A_2 \\ B_2 \end{bmatrix}$$

Then all the structure sections are put in tandem with each other, as the transmission matrix of a series of components is the multiplication of each transmission matrix in their order in the physical structure, as described by equations below. This feature of the TMM gives excellent flexibility to the method as additional sections can be added quite easily without increasing the complexity of problem.



$$\begin{bmatrix} A_1 \\ B_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} A_2 \\ B_2 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} T'_{11} & T'_{12} \\ T'_{21} & T'_{22} \end{bmatrix} \begin{bmatrix} A'_2 \\ B'_2 \end{bmatrix}$$

This useful property of TMM was utilized to modify the initially simulated "SiON guide + gap + III/V guide + gap + SiON guide" structure to include DBRs in the SiON waveguides as an external cavity mirror for lasing operation, hence having the more sophisticated structure of "SiON guide + DBR + SiON guide + gap + III/V guide + gap + SiON guide + DBR + SiON guide".

Each segment was modeled by its equivalent transmission matrix. For instance the frequency dependent T matrix formulation for a general dielectric segment and a DBR can be found in [75] and [76] respectively.

With this benchmark in place, the spectrum of reflection and transmission were simulated for various gap fillings, number of gratings, and pitch depths. Next, a sensitivity analysis on the Bragg length variation was carried out using the same method. In the following subsections, the results of these simulations will be reviewed.

Figure 3- 15 gives a 3D representation of reflection coefficient from a single DBR structure for different numbers of gratings over different wavelengths.

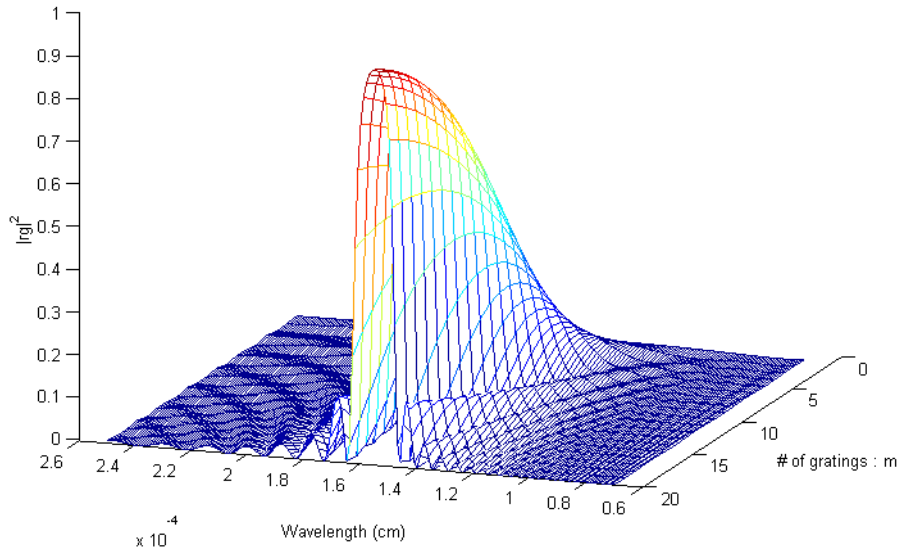


Figure 3- 15: Reflection spectrum of a DBR structure with respect to different numbers of gratings.

To determine the required number of gratings for a given reflectivity, simulations at the Bragg frequency (λ_0=1.55μm) were carried out for different numbers of grating periods for various designs options. The design options cover a range of 0-0.6μm for the shallow pitches of the grating (d_1 in Figure 3- 16).

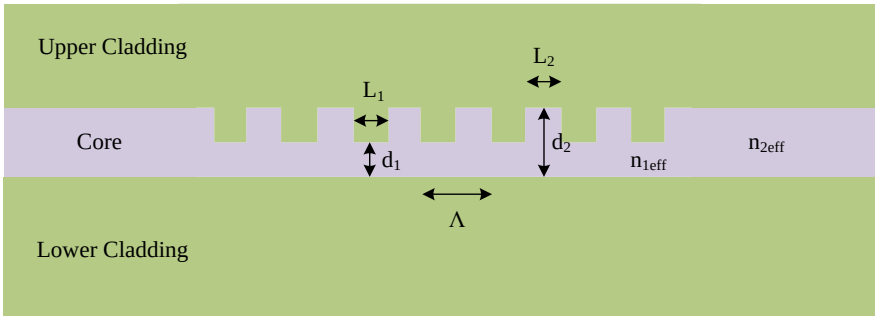


Figure 3- 16: Schematic showing grating d_1 and d_2 pitch heights, L_1 and L_2 pitch lengths, and Λ for the pitch period.

For all cases, d_2=0.7μm, n_{core}=1.6 and $n_{cladding}$=1.45, therefore n_{2eff}=1.5172. Table 3- 4 summarizes n_{1eff}[15] for different values of d_1 that are going to be demonstrated in the design graph of Figure 3- 17.

Core height (μm)	$\mathbf{n_{eff,\ TE}}$	$\mathbf{n_{eff,\ TM}}$
0.1	1.4528899	1.4519732
0.2	1.4607531	1.4575872
0.3	1.4717251	1.4660274
0.4	1.4839058	1.4762267
0.5	1.4959545	1.4871510
0.6	1.5071428	1.4979923
0.7	1.5171762	1.5082282

Table 3- 4: Effective refractive indices for TE and TM modes, for various core heights.

With the parameters discussed above, a set of design curves for the reflection coefficient versus the different numbers of gratings and for various structure options with different abruptness of gratings, is presented in Figure 3- 17.

From this graph it can be noted that for an abrupt grating (i.e. d_1=0μm), at about m=40, power reflection of R=90% is achievable. If less sharp grating pitches are used (d_1 increased), the reflection per pitch is lower, and thus a higher number of gratings is needed to achieve the same aggregate reflection at the Bragg frequency of the DBR.

[15] Effective indices here were calculated through a simple 1D mode solver [79]. However later on, specifically in Chapter 6, mode analysis is done with a more sophisticated full vectorial 2D solver, developed by Milos Popovic.

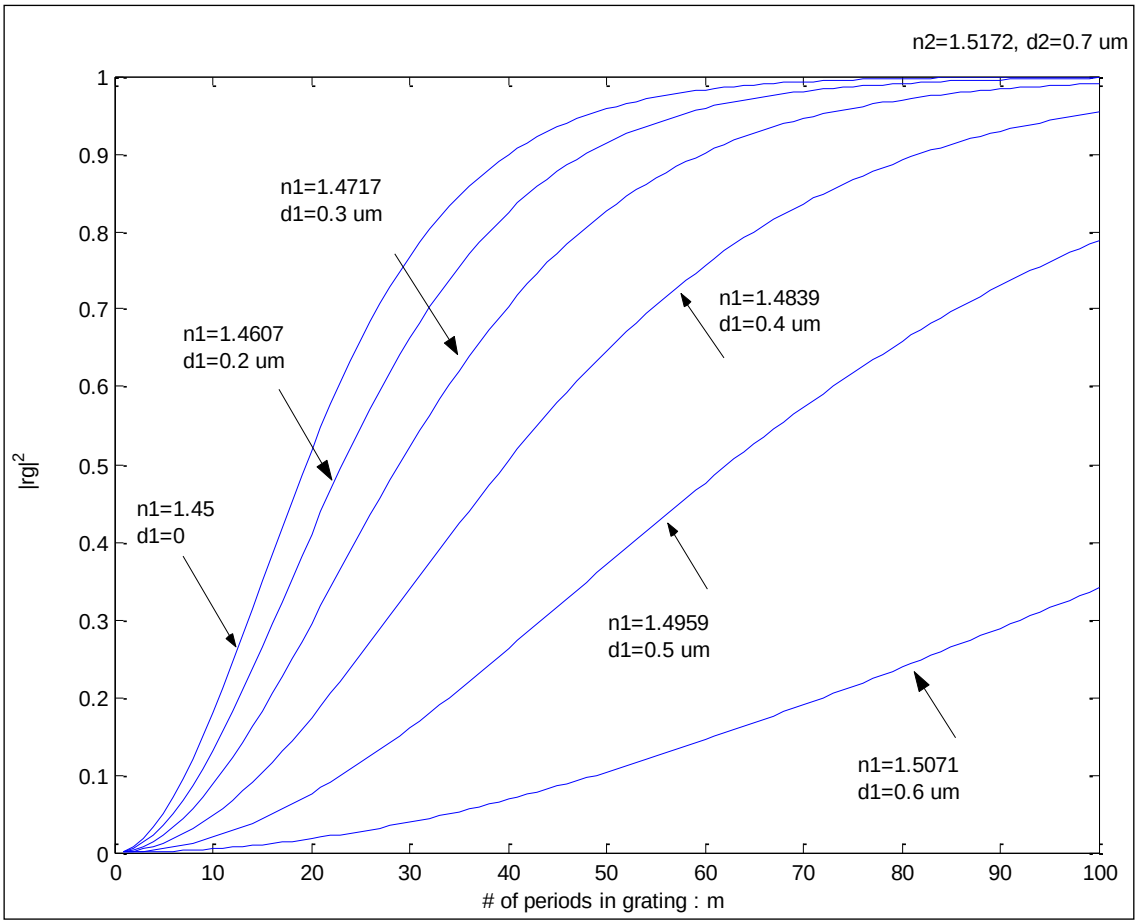


Figure 3- 17: DBR design curve showing the reflection for different grating options (height of grating pitches) and numbers of gratings.

Next, using TMM, the added effects of gaps, SiON waveguide sections, and DBR to the initial InP cavity are simulated. With these sections put in a cascade order, their transmission matrices are multiplied to give the aggregate transmission matrix of the complete structure. Figure 3- 18 to Figure 3- 22 show this trend in which initially the spectrum of a 300µm InP cavity by its own is given in Figure 3- 18, then two 2µm gaps are added to the sides of laser cavity in Figure 3- 20. Next in Figure 3- 21, two sections of SiON waveguide are added to the previous gap-laser-gap structure, and finally in Figure 3- 22 two DBR segments are added to the two ends of the structure.

When the single 300µm laser cavity is simulated, a zoomed view of the spectrum is depicted in Figure 3- 19, and shows the longitudinal mode separation of 1.25nm.

In general, for a Fabry Perot cavity, the axial mode spacing is given by

$$\Delta\lambda = \frac{\lambda_0^2}{2L * n_{eff}}$$

Using λ_0=1.55μm, L=300μm and n_{eff}=3.2072[16] for III/V guide, mode spacing for this laser platelet cavity is found to be $\Delta\lambda$=1.248nm, which is exactly the same as what can be read from the zoomed graph of Figure 3- 19 and serves as a sanity check.

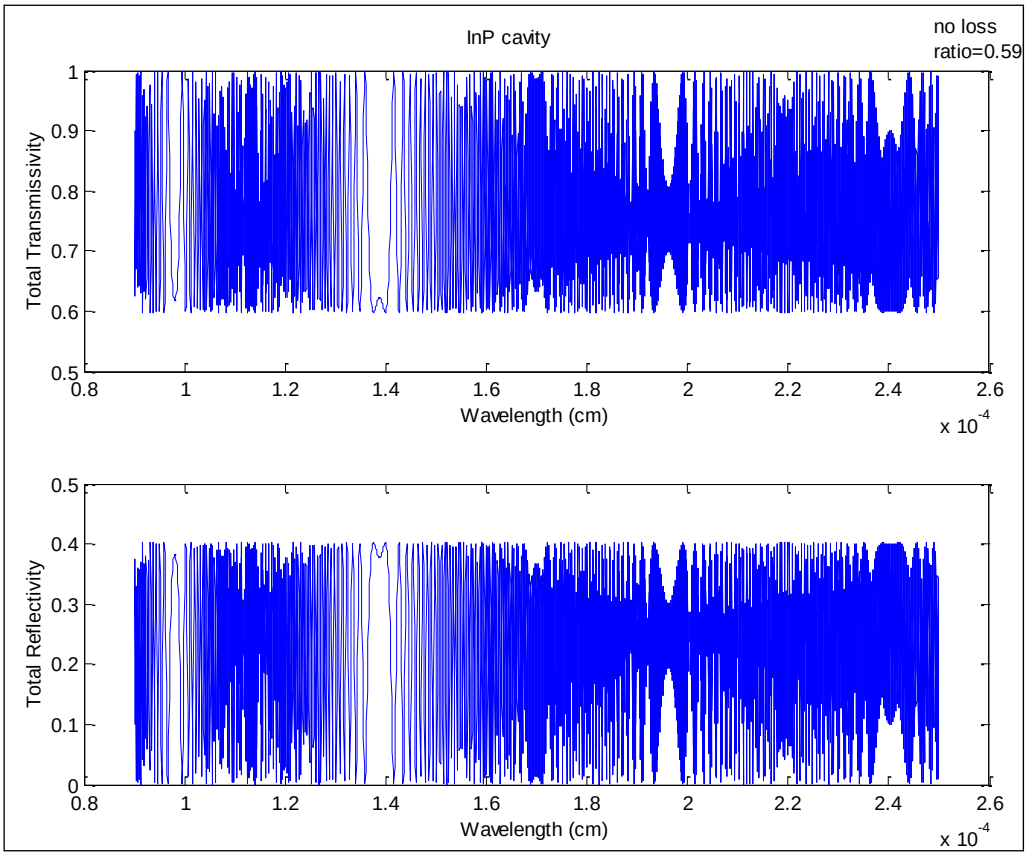


Figure 3- 18: Spectrum derived from transmission matrix of a single 300μm InP laser cavity.

[16] This is obtained by a 1D analysis, however it is close enough to what the 2D fully vectorial analysis used in Chapter 6 gives i.e. n_{eff}=3.1944 for the 1st TE mode, for the laser ridge waveguide with fabricated dimensions.

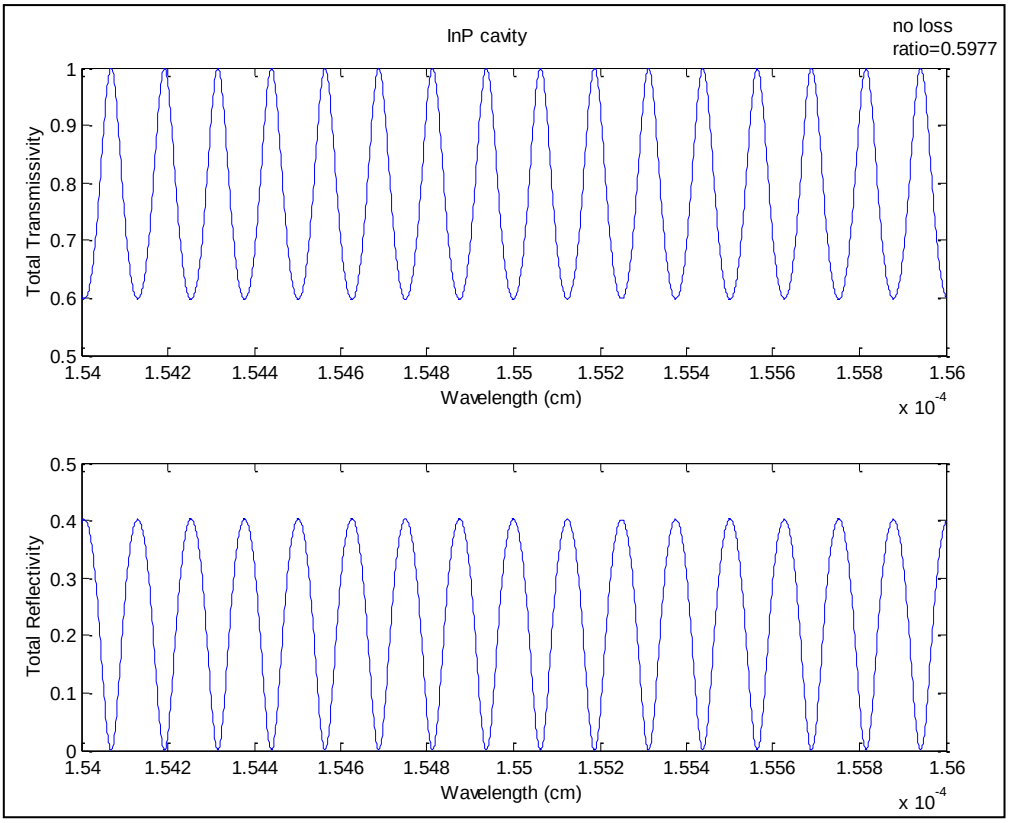


Figure 3- 19: Zoomed view of Figure 3- 18 shows $\Delta\lambda$=1.25nm, which is consistent with theory.

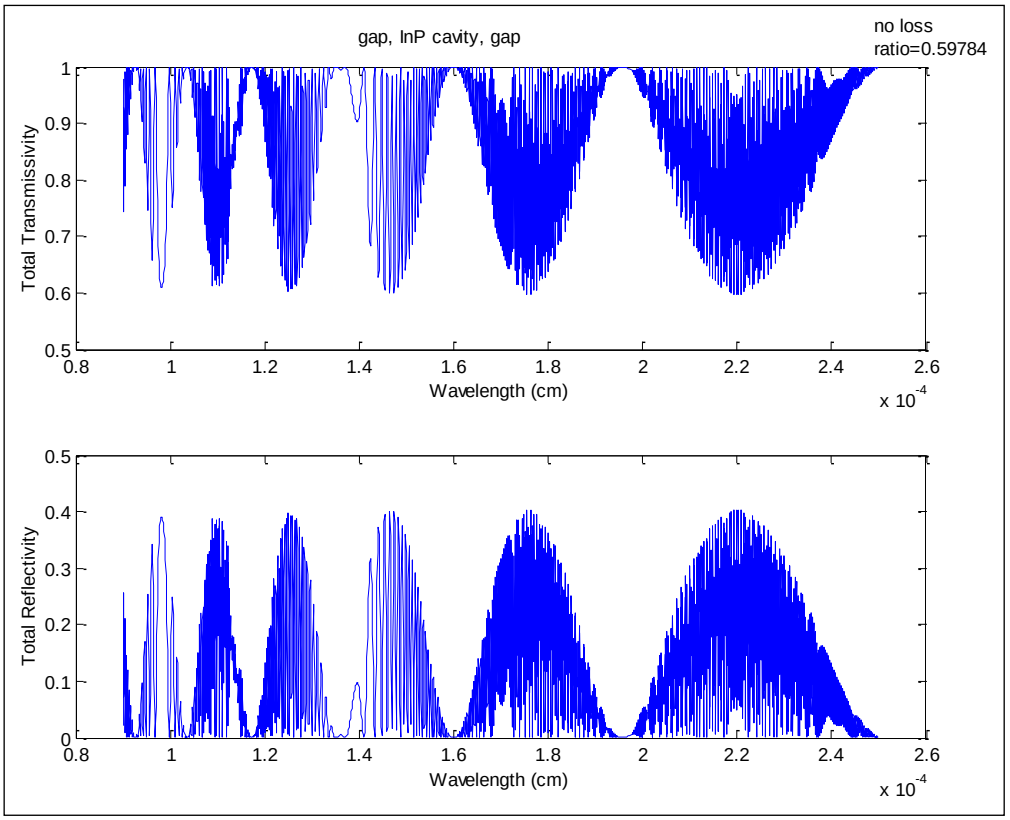


Figure 3- 20: Spectrum of "gap - InP cavity - gap" structure with 2μm of air gaps at both ends of the laser cavity.

When the SiON waveguide sections are added, the spectrum shown Figure 3- 21 is obtained. This is in fact the fully integrated structure composed of "SiON waveguide + gap + InP cavity + gap + SiON" sequence.

The parameters used in these simulations for core, cladding and effective refractive indices, as well as core heights of SiON and laser waveguides are listed in Table 3- 5.

Waveguide	n_{core}	$n_{cladding}$	n_{eff}	h_{core}
SiON	1.6	1.45	1.5172	0.7µm
Laser	3.43	3.14	3.2072	0.2µm

Table 3- 5: Refractive indices and dimensions for dielectric and III/V waveguides used in TMM simulations here.

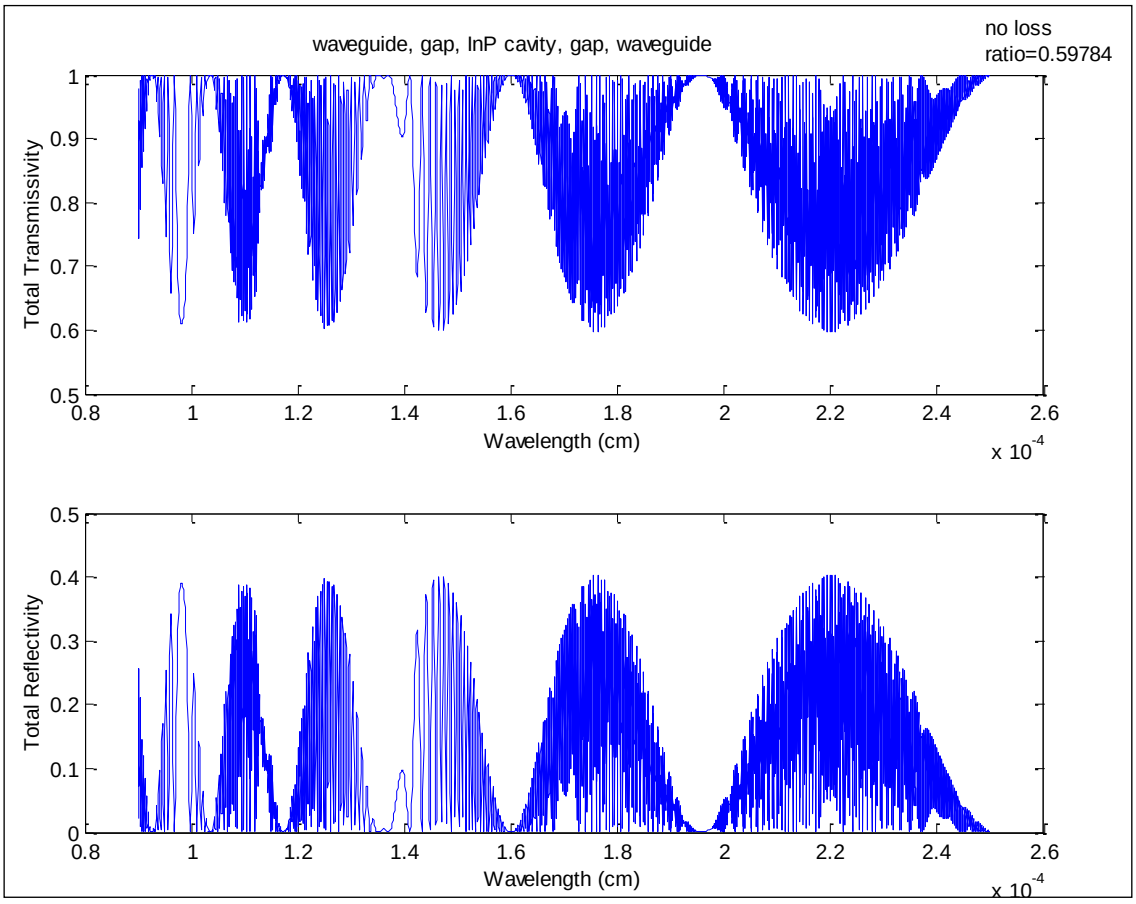


Figure 3- 21: Spectrum of "SiON waveguide+gap+InP cavity+gap+SiON waveguide" structure.

Finally, two DBR segments are added to the two ends of the structure. The two DBRs are placed 5µm away from the SiON dielectric waveguide facet that faces the laser waveguide via a gap. The effect of the introduction of such DBR with m=30 (number of

gratings) on the spectrum of the structure is shown in Figure 3- 22, where its significant impact in adding a very strong reflection (-19dB in transmission) at the Bragg frequency (designed to be at λ=1.55μm) is noticeable.

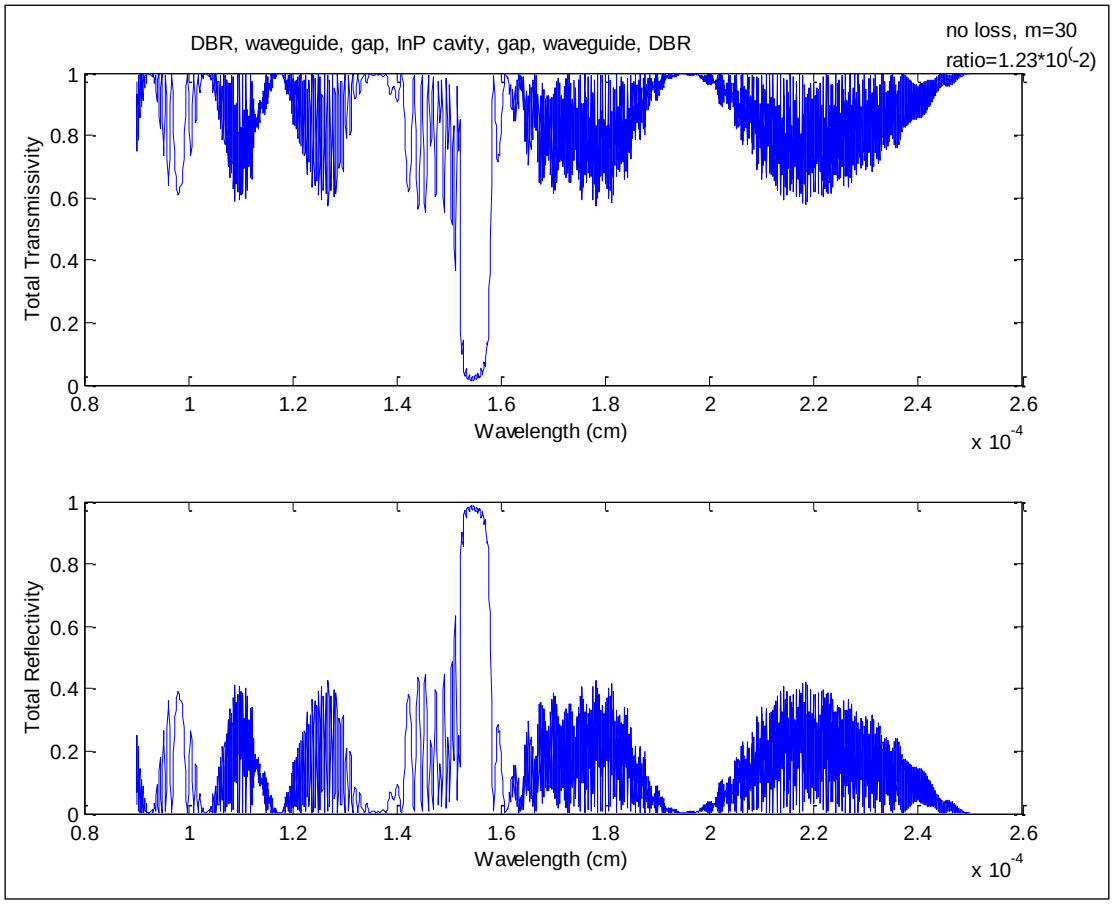


Figure 3- 22: Spectrum of the integrated structure where two DBRs are incorporated at both ends (in SiON waveguides), with number of gratings=30. Efficient filtering characteristic of the DBR is visible, which was designed to happen at λ=1.55μm.

It is expected that the filtering impact of the DBR depends strongly on the number of gratings used. In Figure 3- 23 and Figure 3- 24, the spectrum for m=10 and m=100 are depicted to show this strong dependency. The maximum reflectivity for m=10 is R_{max}=76%, while for m=30 it reaches R_{max}=99%, and for m=100 R_{max}=100% effectively. This type of information can be used by a designer to select the required number of gratings based on what reflection coefficient the application demands.

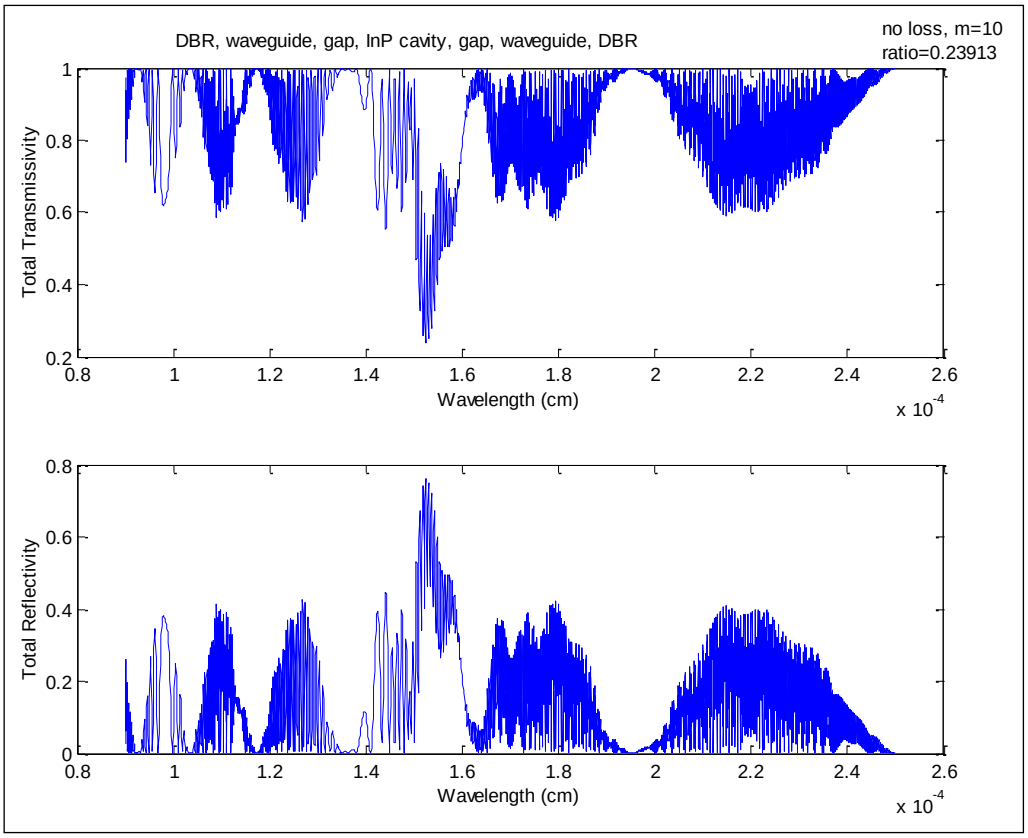


Figure 3- 23: Spectrum of the aggregate structure where the DBR has m=10 gratings.

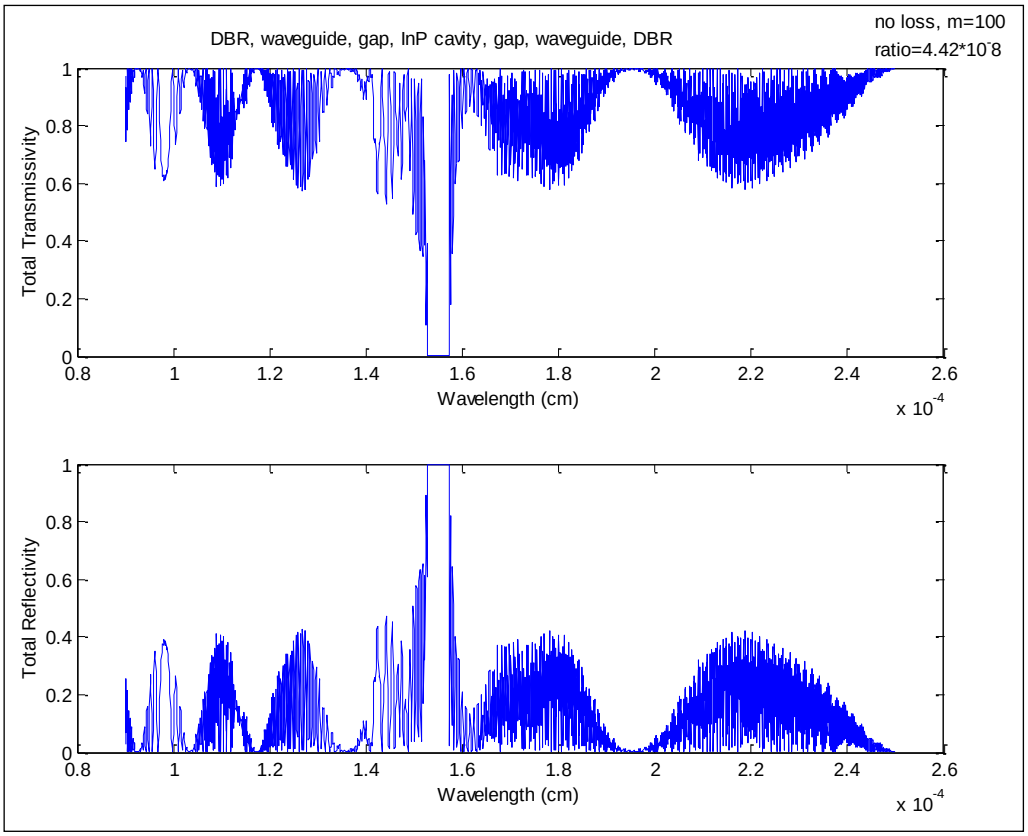


Figure 3- 24: Spectrum of the entire structure with a DBR with m=100 gratings.

Since fabrication variations might impose a limit on how accurate and consistent the grating pitches can be fabricated, we also looked into the sensitivity of the spectrum response with respect to fabrication inaccuracies, specifically for pitch length variations.

In order to implement the effect of pitch length inaccuracies, the pitch period $\Lambda=L_1+L_2$ was kept constant. Ideal pitch lengths are as before:

$$L_1 = \frac{\lambda_0}{4\, n_{1\,eff}}$$

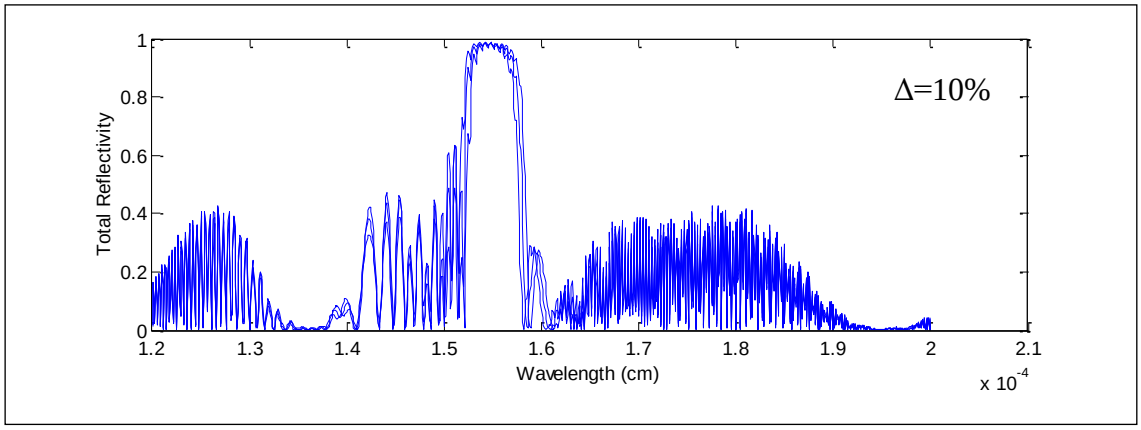
$$L_2 = \frac{\lambda_0}{4\, n_{2\,eff}}$$

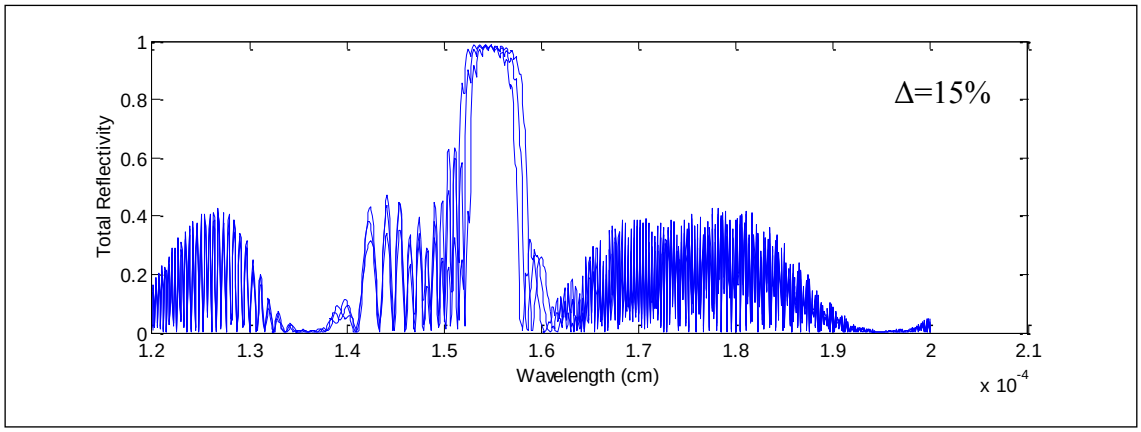
For each variation of $\Delta \in [5, 10, 15, 20, 30, 40, 50]$ %, three cases with length values below are compared.

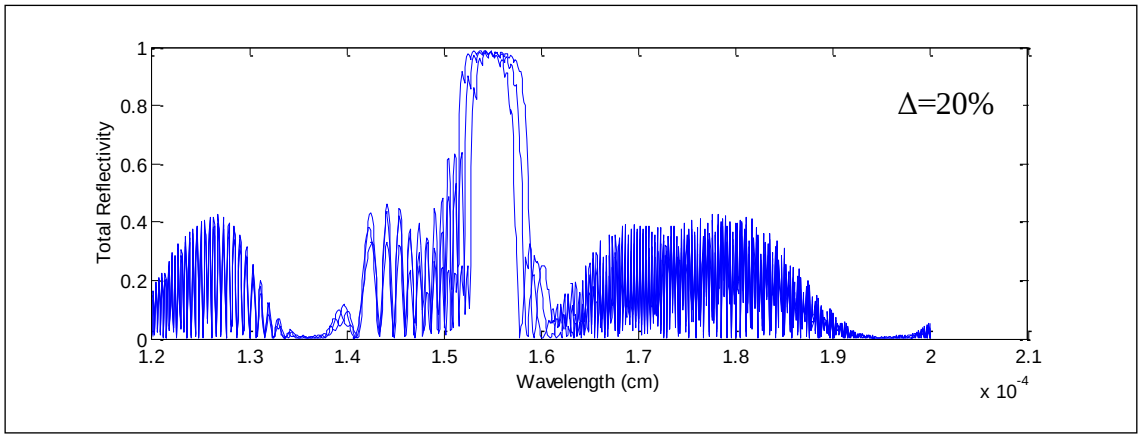
$$\begin{cases} a)\ L_1\ ,\ L_2 \\ b)\ L_1 + \Delta L_1\ ,\ L_2 - \Delta L_2 \\ c)\ L_1 - \Delta L_1\ ,\ L_2 + \Delta L_2 \end{cases}$$

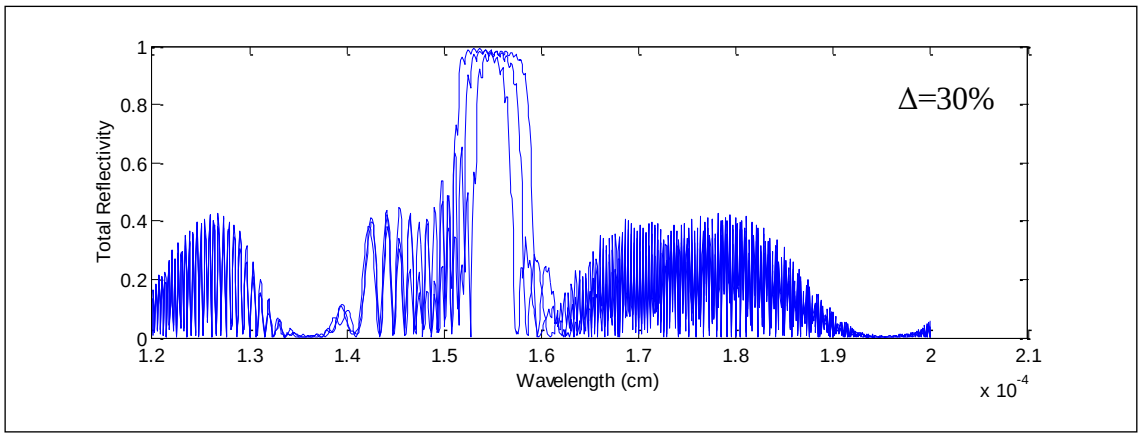
The simulations gave reflection and transmission for the whole system consisting of: "waveguide + DBR + waveguide + gap + laser cavity + gap + waveguide + DBR + waveguide", and the number of periods in the DBR is m=30 for all cases. The effective refractive indices for the DBR pitches are n_{1eff}=1.45 (d_1=0µm) and n_{2eff}=1.5172 (d_2=0.7µm). It was observed that the case c) experienced shifting of the reflection peak to lower wavelengths (blue shift) and b) experienced red shift (to higher wavelengths).

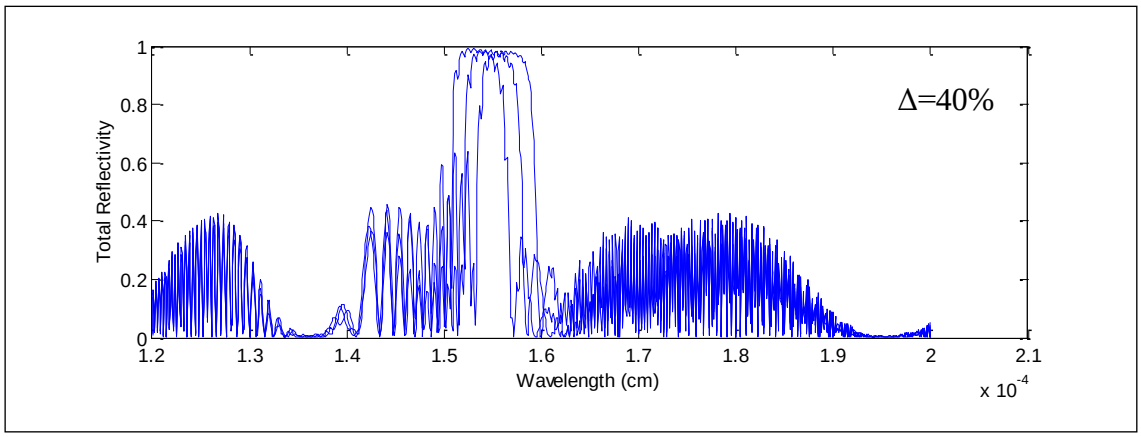
A series of examples for such a variation analysis of the full integrated structure of "waveguide + DBR + waveguide + gap + laser cavity + gap + waveguide + DBR + waveguide" is shown in Figure 3- 25, where for brevity, only reflection graphs are shown.




Δ=15%
Total Reflectivity
Wavelength (cm)
x 10^-4


Δ=20%
Total Reflectivity
Wavelength (cm)
x 10^-4


Δ=30%
Total Reflectivity
Wavelength (cm)
x 10^-4


Δ=40%
Total Reflectivity
Wavelength (cm)
x 10^-4

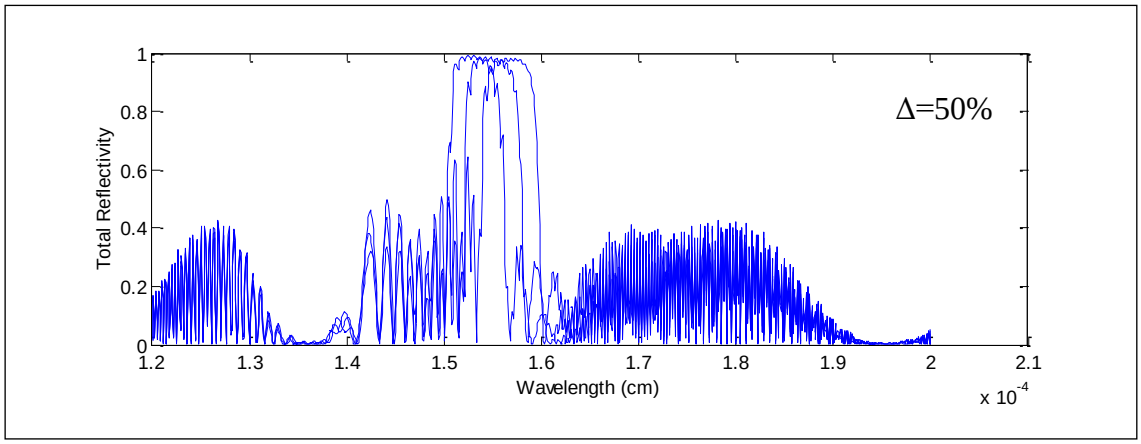


Figure 3- 25: Sensitivity analysis due to DBR pitch lengths variation ranging from 10% to 50%.

The wavelength shifts of the Bragg filter were determined from the plots in Figure 3-25 and are listed in Table 3- 6 for various length variations Δ. Based on this table, and depending on the acceptable tolerance for the shift of the stop-band wavelength, one can decide which minimum fabrication accuracy is required to ensure efficient operation of the DBR structure.

Δ (%)	**λ_{shift} (nm)**
10	3.3
15	6.1
20	7.9
30	10
40	11.7
50	18

Table 3- 6: Stop-band shift of the DBR filter in the aggregate structure. λ_{shift} for each length variation Δ is derived from the corresponding plot in Figure 3- 25.

It was noticed in the FDTD simulations in the previous section that if the pitches in the DBR gratings are filled with a high refractive index material e.g. n_1=2.2, a high reflection is attainable with a lower number of gratings. Therefore, the effect of such high index pitch filling (n_1 in Figure 3- 11) is further studied here with Transmission Matrix Method as well.

Figure 3- 26 compares the reflectivity at the Bragg frequency using a high index pitch filling versus a lower index one. It can be noticed that for n_1=2.2, with a small number of gratings (e.g. m=6) a very high reflectivity is achieved, which would make the DBR segment compact and reduces the consumed area on chip. Deviating from the Bragg frequency, Figure 3- 27 shows how a smaller DBR behaves in the high index pitch filling case (n_1=2.2).

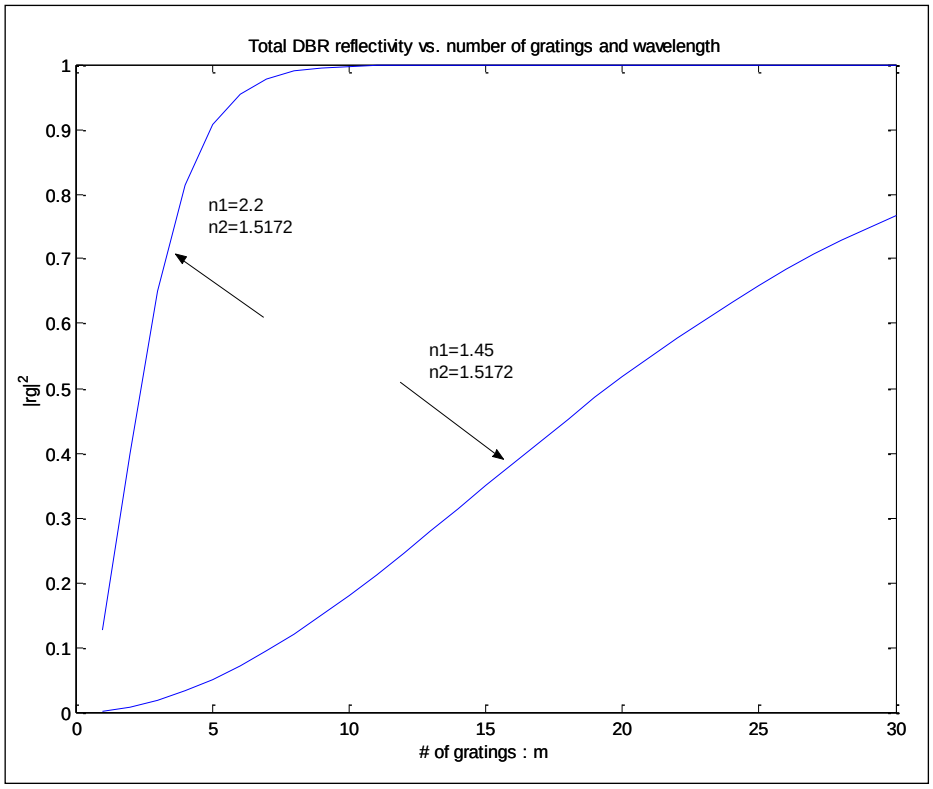


Figure 3- 26: Reflectivity of a DBR for two cases of low and high pitch refractive index, at the Bragg wavelength.

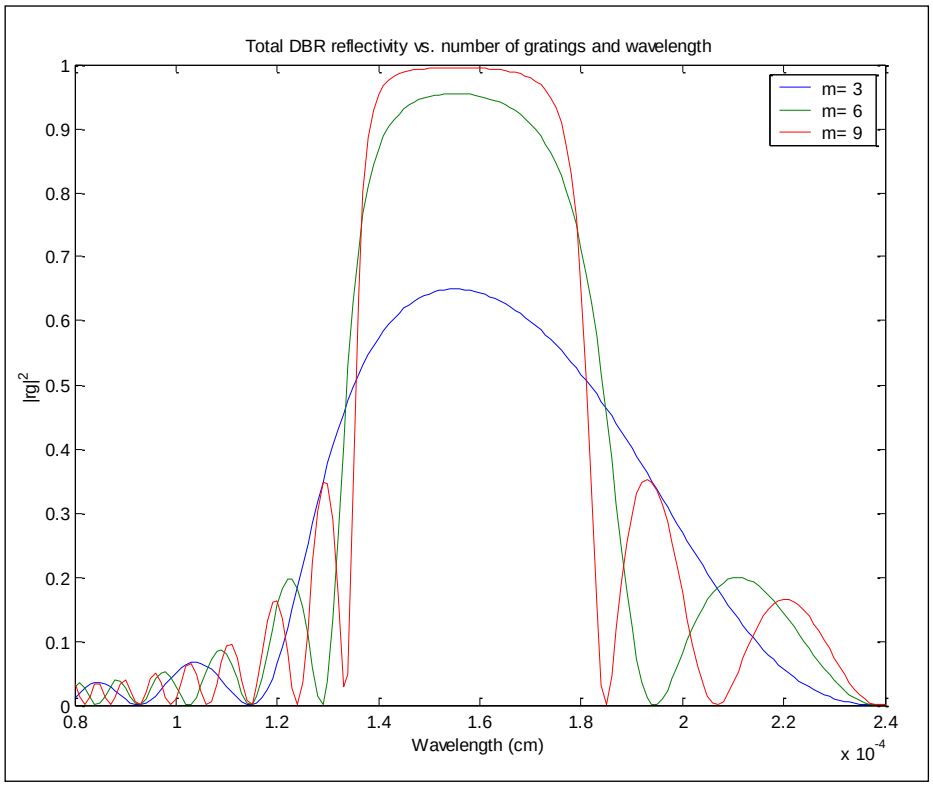


Figure 3- 27: DBR reflectivity spectrum for high index pitch fill (n_1=2.2) for m=3,6,9.

If such a DBR is introduced to the entire structure of "waveguide + DBR + waveguide + gap + laser cavity + gap + waveguide + DBR + waveguide", the transmission and reflection spectrum is shown in Figure 3- 28 and Figure 3- 29 for m=6 and 4 respectively.

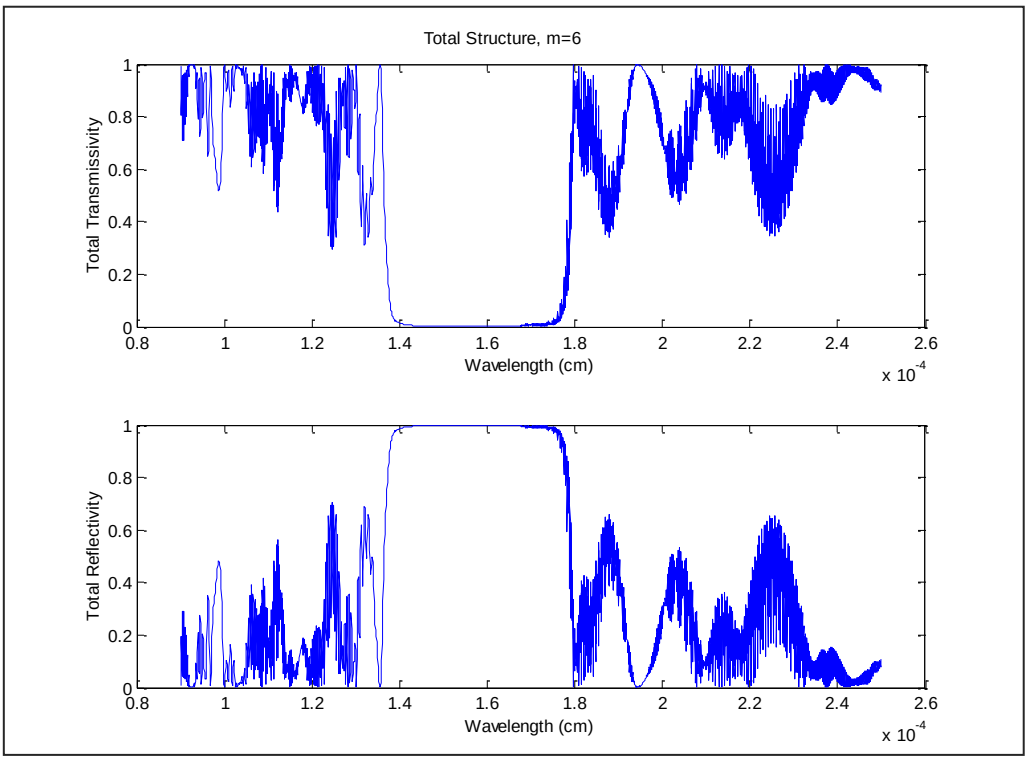


Figure 3- 28: Spectrum of the entire structure with high index DBR (n_1=2.2) and m=6.

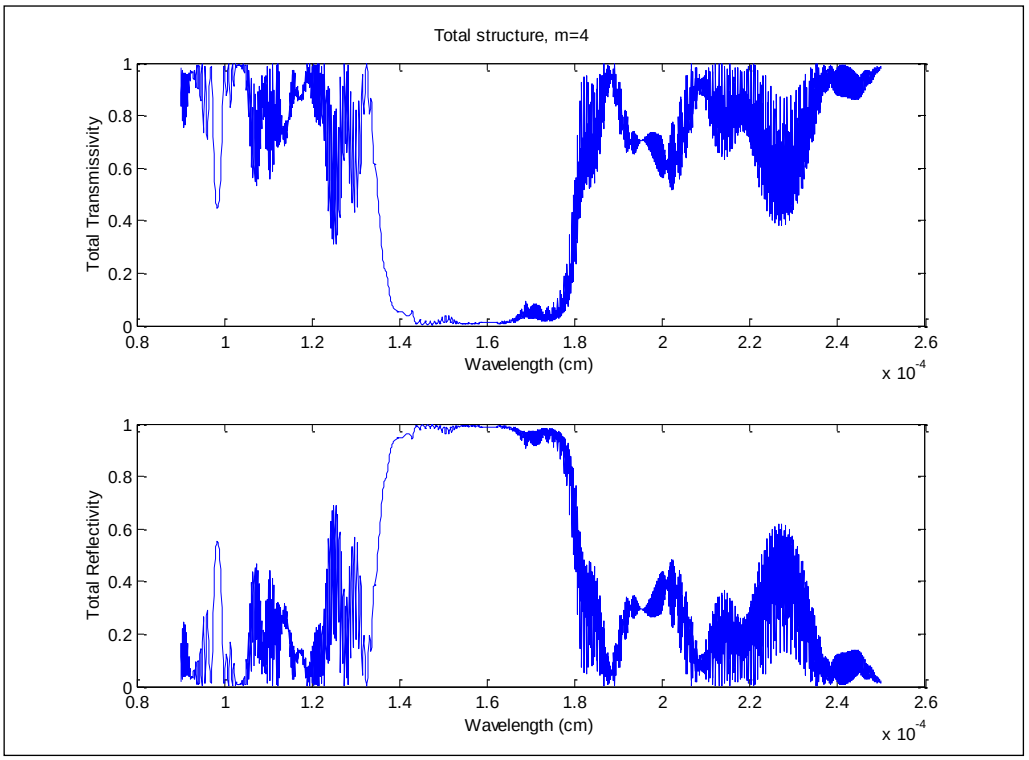


Figure 3- 29: Spectrum of the entire structure with high index DBR (n_1=2.2) and m=4.

Since in this high index DBR the reflection bandwidth is quite wide when compared to the designs we discussed earlier, a 15% pitch length variation in the fabrication process very well covers the target λ=1.55μm range, as shown in Figure 3- 30. However, if the DBR is used to enhance single frequency operation of the integrated laser structure, this wide bandwidth would not be desirable, as many modes would see the high reflection and thus be motivated to lase. In such a case, a lower index pitch filling which results in a narrower stop-band is preferred.

Note that if a DBR is used to enhance mirror reflectivity of a Fabry Perot Laser cavity, usually one mirror is designed to have a very high reflection (e.g. 100%), while the other mirror has a lower reflectivity letting the stimulated emitted light out of the laser.

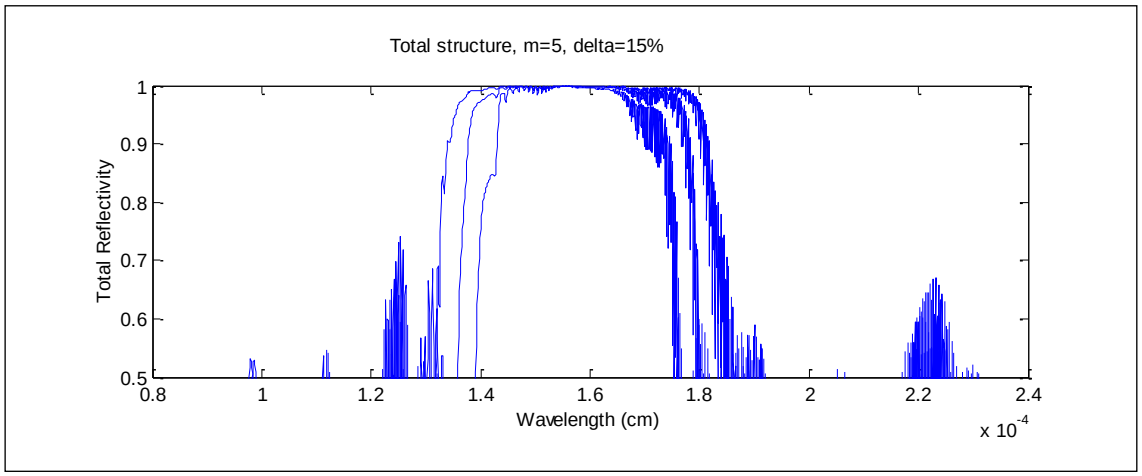


Figure 3- 30: Sensitivity of the structure spectrum with length variation of Δ=15%, when the DBR has high index pitch fill (n_1=2.2) and grating periods of m=5.

3.5. DBR Design via BeamProp: Bidirectional BPM

3.5.1. Introduction to BPM

The Beam Propagation Method (BPM) was formulated in 1970, and since then has contributed significantly in simplifying the modeling and simulations of photonic circuits.

In basic terms, the most accurate way of solving for field distributions and wave propagation in Electromagnetics is to solve the fully vectorial Maxwell's equations with proper boundary conditions. However, this approach turns out to be quite taxing and

computationally overwhelming for photonic structures, due to their high transverse versus axial aspect ratio. More specifically, the transverse axial dimensions of a photonic structure are on the order of a few microns, whereas the propagated wave is simulated to propagate axially over lengths on the order of centimeters. Therefore, discretization and field storage turn out to be a huge burden on CPU performance and memory allocation.

In order to address this bottleneck, approximations to the full Maxwell's equations have been widely used. For instance, in many applications the scalar wave equations are sufficient in modeling mode propagation. Also the fact that the phase front of guided modes in photonic waveguides is close to planar, makes paraxial approximations a viable approach. If the refractive index changes along the propagation axis are small and slowly varying, the reflections will be minimized. In such a case, the non-paraxial wave equation can be reduced to paraxial wave equation.

The paraxial wave equations have the luxury of being initial value problems rather than boundary condition problems. This means that in contrast to solving for the full field distribution in full Maxwell formulation, here knowing the initial condition in space (e.g. at z=0), one can find the propagated field at any z along the propagation axis. Not being a boundary-value problem makes the Beam Propagation Method computationally highly efficient.

However, since the refractive index needs to be slowly varying and strong reflections are not allowed in BPM, the application of this method is limiting for scenarios with abrupt axial changes of structure. To address this issue, modifications to BPM, such as bidirectional BPM have been suggested [77], which are suitable for the design of gratings as they do not satisfy the slow varying prerequirement of traditional BPM.

3.5.2. DBR Design with Bidirectional BPM

In an effort to utilize the capabilities of BPM, the design of gratings in dielectric waveguide used in the integrated structure of this project was also studied using beam propagation method provided by the BeamPROP™ software from RSoft [78].

Initially, the conventional BPM method was used; however since the main idea behind DBRs is the constructive reflections of waves at discontinuities, unidirectional BPM was not proper for gratings design. Therefore, the focus was changed to use Bidirectional BPM simulations in BeamPROP, where both $e^{+j\beta z}$ and $e^{-j\beta z}$ components of the propagating wave are included, and the solution is found by iteration, hence structures like gratings can be

modeled. In the bidirectional BPM mode of BeamProp only 2D simulations were possible in the available release of the software. Since this feature of the software was a work in progress and thus not highly robust for complex problems, care must be taken to select the right order of Pade solver, the imaginary parameter used in the Pade solver interface (to dump artificially evanescent waves generated), and the proper type of iterator, from the options available.

The launch field used in the simulations presented here was Slab Mode and the selected power monitors were Forward Major (blue) and Backward Major (green). The convenient grating feature of BeamPROP had been used to define the structure, where pitch Δn is defined (compared to background refractive index) as well as the numbers of gratings and their period (Λ). The index profile of a structure with m=40 (number of gratings) for low index pitches[17] (n_1=1.45)) is shown in Figure 3- 31. For this filling, the pitch period is $\Lambda = \lambda_0/4\times(1/n_{eff1}+1/n_{eff2})=0.5226$, with n_{eff1}=1.45 and n_{eff2}=1.5172 for the SiON dielectric waveguide.

As mentioned before, 2D Bidirectional BPM was chosen as the solver for these sets of simulations in semi-vectorial, and the waveguide width is 4μm. Through experimentation it was found that when operator is set to "Local", the Pade order to "Propagation order" or (1,1) and the iterator to "BF-Auto" or "Matrix", the solution failed to converge. However if a higher order Pade solver e.g. (3,3) is used in conjunction with an imaginary parameter ϵ [0.4-0.8], and the iterator is set to "Matrix", the solution converged very well after about three iterations. The corresponding forward (blue) and backward (green) power monitor results are shown in Figure 3- 32, where the gradual reflection of the incident beam as a result of constructive interference of reflections from each grating pitch is observed, and the beam strength decays towards the end of the grating along the z-direction.

[17] Since the background refractive index (including claddings) is also 1.45 for these dielectric waveguides, Δn=0 for the grating pitches. Conversely Δn=0.15 for the waveguide core where n=1.6 for SiON.

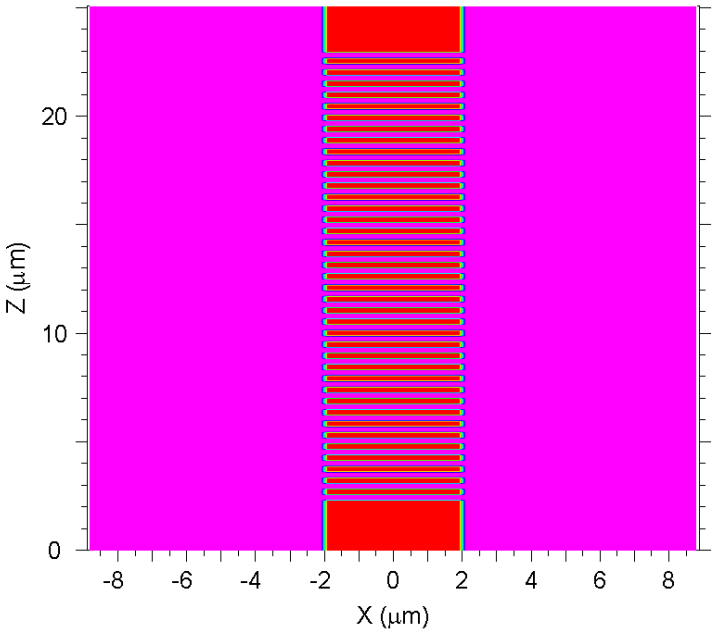


Figure 3- 31: Grating with m=40 and low index gap filling (n_2=1.45).

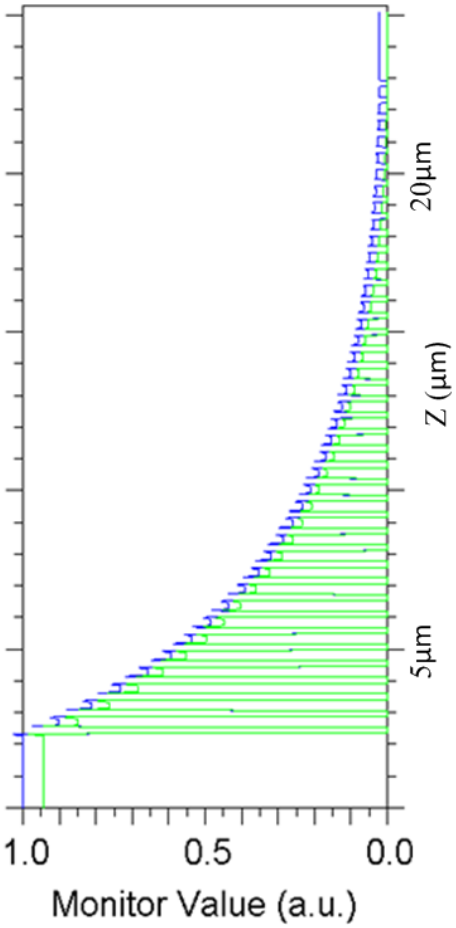


Figure 3- 32: Simulated beam propagation along the gratings for m=40 and low index gap filling (n_2=1.45). Bidirectional solver: Pade (3,3) and imaginary parameter:0.6. The blue curve corresponds to the forward power monitor while the green one represents the backward wave power monitor.

Having the solver converged, other numbers of grating periods were also looked into to see what reflection can be achieved in a more compact structure. For instance, with m=10 and m=5 (and still a low index gap filling of 1.45), the following results, shown in Figure 3-33 and Figure 3- 34, were obtained for an imaginary parameter[18] of 0.4 and 0.6 respectively.

In addition, since high index gap filling had been of interest in the previous sections, a filling of n_1=2.2 was simulated here as well, with different numbers of gratings, as shown in Figure 3- 35 (m=40), and Figure 3- 36 (m=10). Since the refractive index step is larger in this case, the solver only converged when "Matrix-3" iterator was used (along with Pade (3,3) and an imaginary parameter[19] of 0.6). In this simulation Δn=0.75, therefore $n_{grating\text{-}pitch\text{-}filler}$= 1.45+0.75=2.2 and thus the period $\Lambda = 1.55/4 \times (1/1.5172 + 1/2.2) = 0.43154\mu m$.

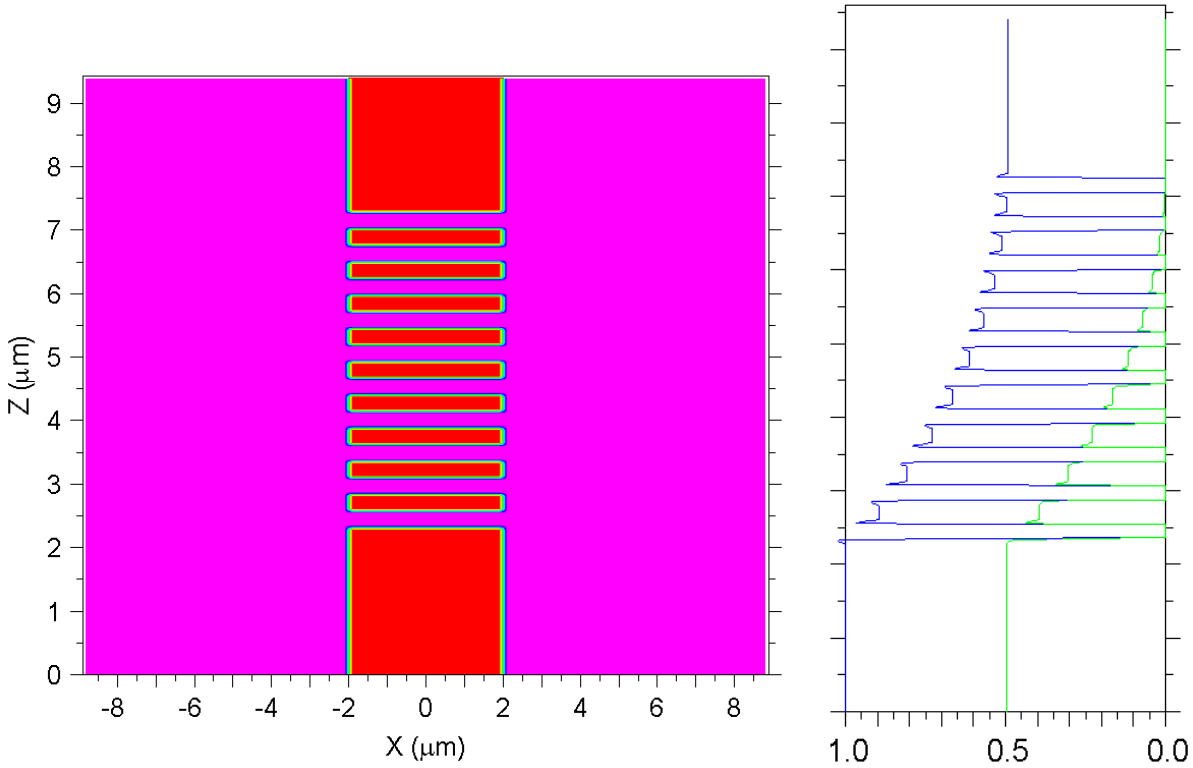


Figure 3- 33: Grating with m=10 and low index gap filling (n_2=1.45). The grating structure is shown on left and forward and backward beams propagated along the gratings are illustrated on right.

[18] Overall the imaginary parameter had better be kept as low as possible since with a high value the true solution also gets affected. Generally the range for this parameter is [0,1] and 0.6-0.8 is suggested for a high Δn problem in conjunction with Pade (2,2) or (3,3).

[19] In this case with a small imaginary parameter of 0.2 the solver fails to converge. As mentioned earlier for a higher refractive index, a higher imaginary parameter on the order of 0.6-0.8 is required.

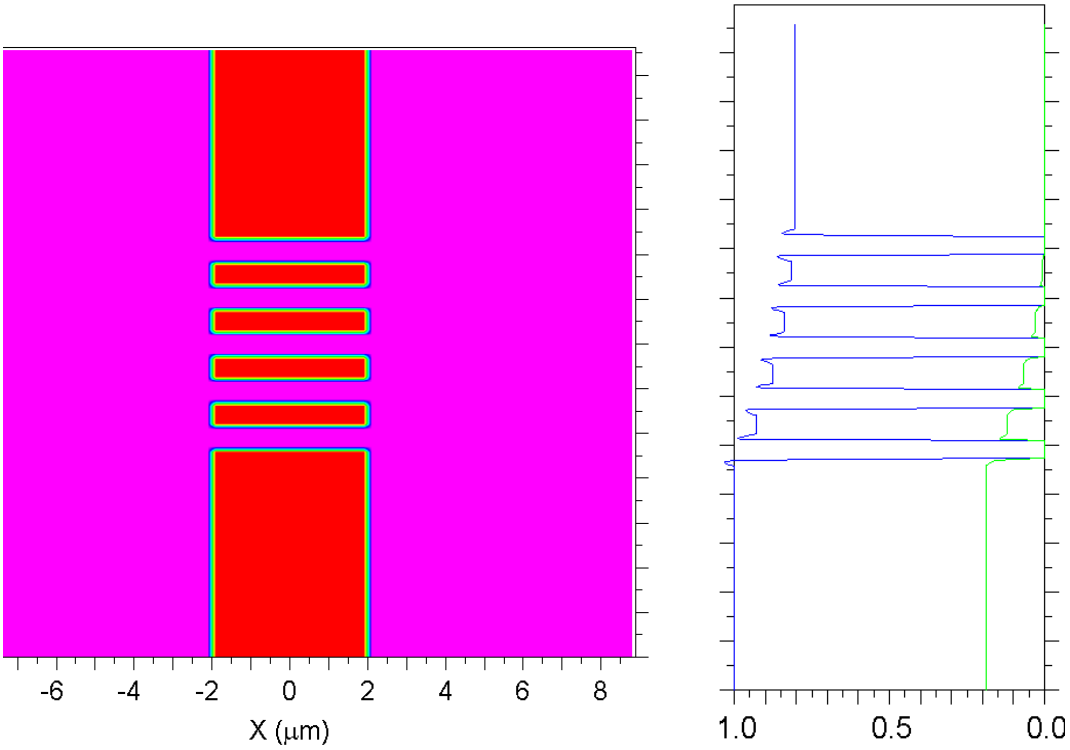


Figure 3- 34: Grating with m=5 and low index gap filling (n_2=1.45). The grating structure is shown on left and forward and backward beams propagated along the gratings are illustrated on right.

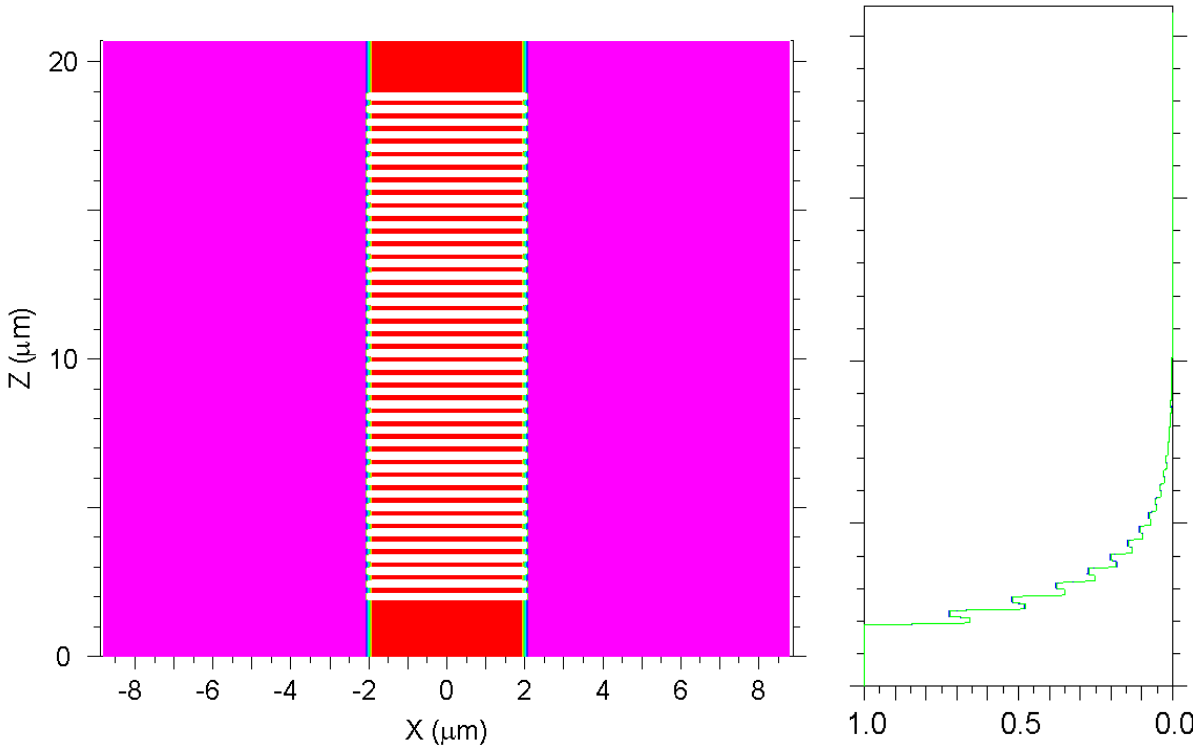


Figure 3- 35: Grating with m=40 and high index gap filling (n_2=2.2). The grating structure is shown on left and beam propagated along the structure is shown on right.

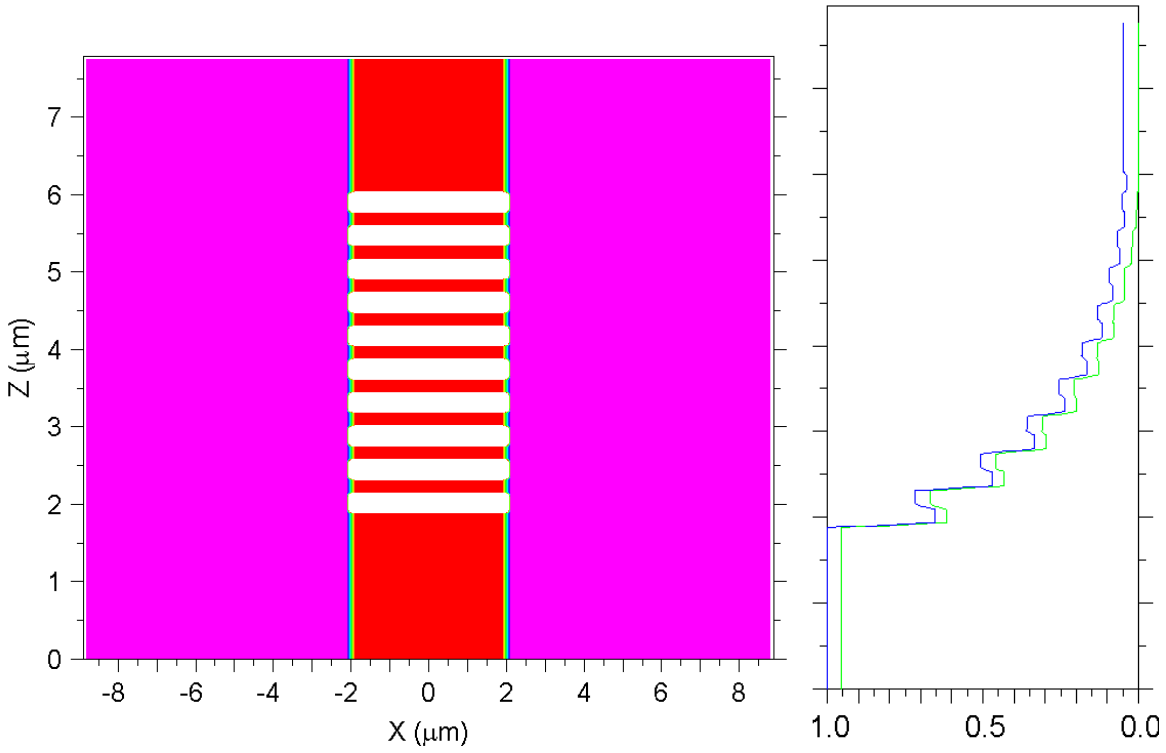


Figure 3- 36: Grating with m=10 and high index gap filling (n_2=2.2). The structure is shown on left and propagated beam along the grating is shown on right. A significantly higher reflection is observed here compared to the low index filling case shown in Figure 3- 33.

Having achieved a stable solution for each structure at the Bragg frequency, in the next step the spectrum of each case was looked into for different gap fillings and numbers of gratings.

Since the wavelength sweep feature of the software is not very stable and at times fails to solve for a certain wavelength and aborts the process, the resolution in the frequency response had to be limited using the then-available version of BeamPROP, since instead of the automatic sweep, a manual simulation for each wavelength separately needed to be adopted. Hence, the power reflection and transmission coefficients were extracted and plotted versus wavelength for two cases of low and high index pitch filling (n_1=1.45 and 2.2) and three numbers of gratings (m=5,10 and 40), as shown in Figure 3- 37 and Figure 3- 38. It can be noticed that for both pitch filling indices, the extinction ratio of the DBR filter increases for higher number of gratings and the stop-band width decreases as well.

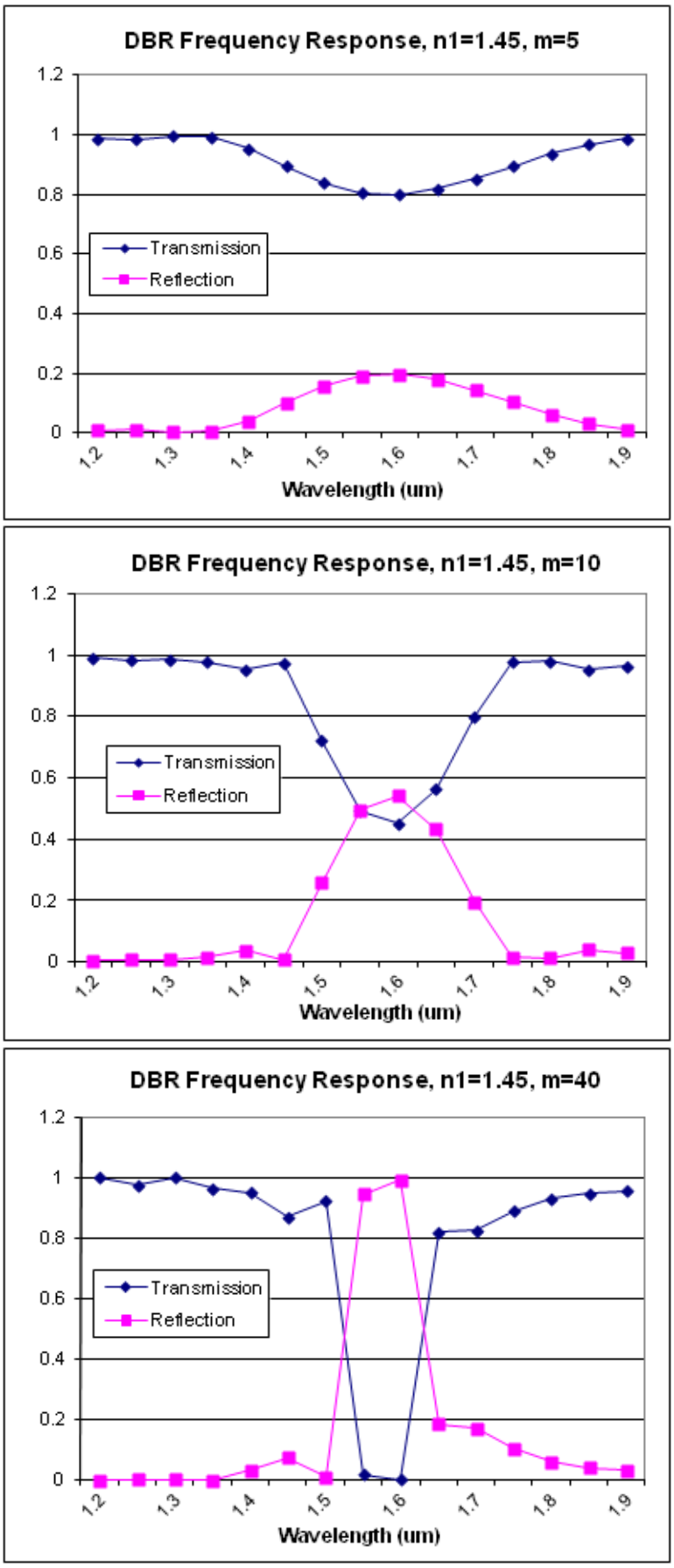
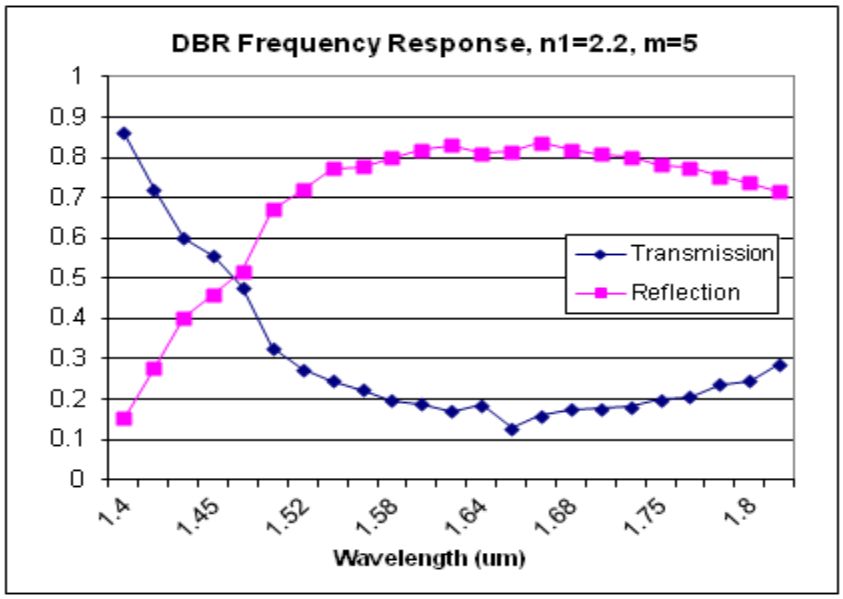
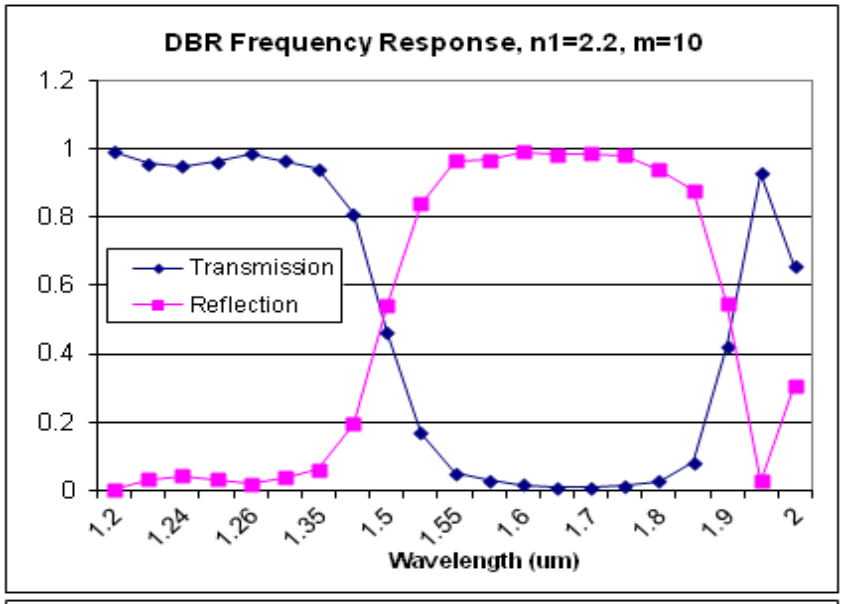


Figure 3- 37: Spectrum of grating, for pitch filling index of n_1=1.45, and m=5,10,40.





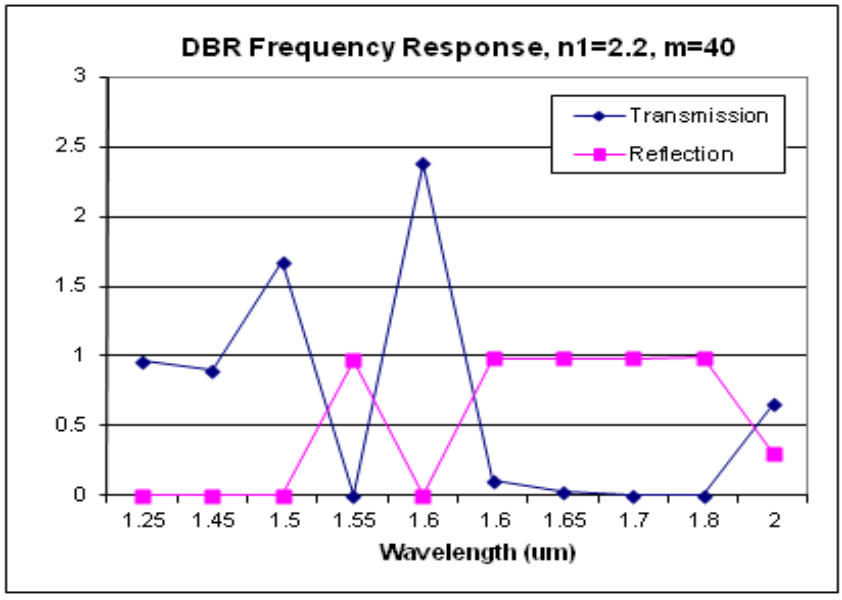


Figure 3- 38: Spectrum of grating, for pitch filling index of n_1=2.2, and m=5,10,40.

The case of high index pitch filling shows a considerably larger stop-band width, which is consistent with the results of transmission matrix method detailed in previous section. Also since Δn is larger for this case, Bi-directional BPM is not as robust as the previous case and more difficulty in converging to the final solution for each wavelength had been faced here. Specifically the spectrum with n_1=2.2 and m=40 shows unstable behavior and thus should not be used for design purposes. Furthermore, the graphs convey that center wavelength of the filtered region is not at λ=1.55μm. This is due to the fact that n_{2eff} had been assumed to be 2.2, consistent with FDTD simulations that were carried out earlier. In the FDTD case, the low pitch height was assumed to be very large, therefore $n_{2eff}=n_2$=2.2. However, BeamPROP treats grating pitches differently and thus the more realistic value for n_{eff2} deviates from the 2.2 that had been used to calculate the grating period (Λ). This results in a shift in Bragg frequency (i.e. center wavelength) of the grating.

Finally, away from Bragg frequency, a standing wave pattern was seen in the designed DBR structure, whereas at Bragg wavelength, strong reflection is observed, as expected. Figure 3- 39 compares these two cases for λ=1.7μm (left) and λ_{Bragg}=1.55μm (right) in a DBR structure with n_1=1.45 and m=40.

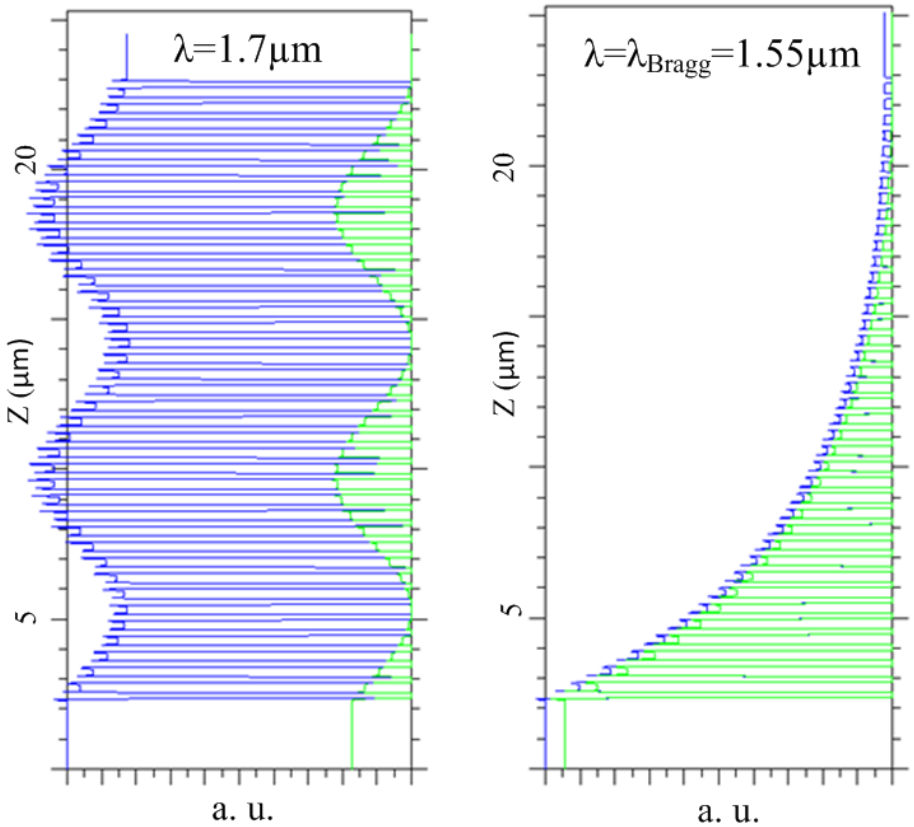


Figure 3- 39: Standing wave (left) at λ=1.7μm, versus strong reflection (right) at λ_{Bragg}=1.55μm in the DBR structure with n_1=1.45 and m=40.

At this stage, the reader might wonder how the results of the bidirectional BPM simulations carried out in this section compare to the transmission matrix method results of the Section 3.4. Comparing Figure 3- 26 with the reflection graphs of Figure 3- 37 and Figure 3- 38, it is seen that BeamProp is consistently overestimating the reflection for low index pitch filling (n_1=1.45). For the higher index fill (n_1=2.2) the discrepancy is smaller, as in both cases reflectivity reaches 100% with a few numbers of gratings. However, BeamProp is not very stable for high index contrast of n_1=2.2 and thus its results for m=40 are unreliable in that case.

3.6. Summary and Discussion

The motivation that triggered the design of DBRs in our project, changed over time as the fabrication steps proved to be successful. For instance, prior to fabrication, there had been uncertainty about the success of the micro-cleaving approach (discussed in Chapter 4 and [60]) that aims to define crystalline laser facets. In case that novel approach proved to be not working, the idea was to use conventionally cleaved lasers (that have rough facets), and fill in the air gap with a high index material, as well as placing the laser at an angle to the dielectric waveguide to minimize the reflection. The idea is to avoid defining a cavity when the conventionally cleaved facets are rough. Therefore the cavity was to be defined elsewhere i.e. through two DBRs fabricated on the dielectric waveguide section. Hence the initial purpose of the DBRs was to define the laser cavity.

However, with the successful fabrication of the micro-cleaved laser platelets, the Fabry Perot of the laser cavity was defined on its own with quality facets. Although with air gaps, the reflection is low (R=27.37%), there was not an immediate need for an external high reflection mirror such as a DBR. Also threshold currents are low enough that a DBR based higher reflection mirror was not essential for that goal.

The single frequency lasing application of DBRs could be very useful in our application, since from the results presented in Chapter 6 one can see that at higher currents above threshold, multi (longitudinal) modes start to lase. Having a mirror loss (α_m) with strong and sharp frequency dependence would have helped to filter them out and ensure single mode lasing. However, a look at the DBR frequency spectrums that were designed in this chapter show that the DBR bandwidth is on the order of a few hundred nanometers (for the case of n_1=1.45 and d_1=0), whereas the spacing between cavity modes is on the order of

nanometers. Therefore, a much narrower bandwidth DBR needs to be designed if single frequency operation is the goal. We expect that if the DBR gratings had smaller reflection per pitch (i.e. increasing d_1 so that it gets closer to d_2 or n_1 closer to n_2), the bandwidth would be narrower, thus it will be more effective in filtering the closely spaced axial cavity modes that compete for lasing.

Another application of including a DBR segment in the SiON waveguides in the coaxial integration approach is to decrease the mirror loss, α_m, when a high index material is used to fill the air gaps. The high index gap filling is desirable both in increasing the coupling between the laser and III/V waveguide as well as removing the sensitivity of the structure to gap length[20]. When a higher index gap filling is used, the Fresnel reflection from the laser cavity facets will be lower, resulting in a high mirror loss which will in turn increase the threshold current. Therefore having a DBR in the external cavity can compensate for such higher mirror loss and result in reducing the threshold current.

Furthermore, if angled configuration of laser ridge and waveguides are adopted (similar to semiconductor optical amplifiers (SOAs)), to reduce the sensitivity of the structure to the frequency dependent effective reflection[21] from the air gap and dielectric waveguide facet, then the required reflection to reach lasing can also be provided by an external cavity DBR made on a segment of the SiON waveguide.

In summary, in this chapter first the optimization of dielectric waveguide refractive index and dimensions as well as gap filling refractive index has been presented. Then the design of a possible DBR structure to be fabricated on the SiON dielectric waveguide was discussed. Such grating structure was designed to function as a stronger mirror/filter in the laser external cavity. The DBR design simulations were carried out using three different approaches of FDTD, TMM and Bidirectional BPM. The results will help us to select the appropriate number of gratings and pitch filling index based on the application requirements, if these DBR structures are going to be included in the next generation of dielectric waveguides fabricated for the coaxial integration approach demonstrated in this thesis.

[20] The effect of gap length on mode suppression ratio observed in the spectrum of integrated lasers is studied and modeled in Chapter 6.

[21] This effective reflection will be modeled in Chapter 6 based on three-mirror cavity model.

Chapter 4

Integration Components: Lasers, Recesses and Dielectric Waveguides

The research described in this thesis focuses on demonstrating the feasibility and advantages of the coaxial integration approach, implemented through nearly planar monolithic integration of edge emitting 1.55μm InGaAs/InP laser diodes in recesses on Si wafer, and coaxially coupled to dielectric waveguides fabricated on the same substrate.

The components used in this project for the demonstration of coaxial integration approach were fabricated through two other PhD theses in our group. Specifically laser platelets have been fabricated by Joseph Rumpler [60] and recesses and dielectric waveguides by Edward Barkley [59].

In this chapter, the fabrication of these three components (dielectric waveguides, recesses and laser platelets) is reviewed in order to have a thorough view about the fabrication details of the aggregate structure.

4.1. Passive Components: Dielectric Waveguides and Recesses

As one of the major components for the monolithic integration of photonic components on silicon using the coaxial integration technique, Edward Barkley focused on

the fabrication of SiON dielectric waveguides in his PhD thesis [59]. These waveguides perform the intra-chip routing of the optical signal to and from the integrated III-V photonic devices that are going to be recess mounted on the silicon integrated circuit.

4.1.1. Design of Dielectric Waveguides

For the structure of the dielectric waveguides, a buried rectangular channel guide structure was chosen[1] as it provides a high confinement. In these dielectric waveguides, the buried rectangular core of SiON is surrounded by SiO_2 upper and lower claddings all fabricated on a Si substrate.

SiON, favored by researches as a material suitable for low-loss waveguides and compatible with Si processing, was selected for the core of waveguides. Furthermore, SiO_xN_y provides a range of refractive indices from n=1.46 (for SiO_2) to n=2 (for Si_3N_4) depending on the ratio of oxygen and nitrogen present in the PECVD chamber. This flexibility of refractive index was desirable in the design phase of this project. In addition, considering the ease of fabrication of this material system[2], the SiON/SiO_2 had been selected for the core/cladding material choice in these waveguides.

Regarding designing the waveguides, it was concluded in Chapter 3 that the optimum dielectric waveguide has n_{core}=1.45, $n_{cladding}$=1.6, and core_height=0.5µm, for gaps larger than 0.5µm between the laser and dielectric waveguides.

For single-mode operation, the maximum waveguide widths were found to be 1.7µm for the dielectric waveguide and 2µm for the laser ridge waveguide [59]. However these dimensions differ from what was fabricated in reality for these two devices. Actual waveguide width dimensions are 1.7µm for dielectric guides and 6.8µm for the fabricated final laser ridge guides.

An analytical formulation [80], [81] was used to calculate substrate coupling loss versus different lower cladding thicknesses to choose a minimum lower cladding height. Based on this calculation, lower cladding thicknesses[3] greater than 3.3µm met the target of substrate coupling loss below 1dB/cm (pp. 79 of [59]), for core refractive indices ranging from 1.5 to 1.65.

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[1] The laser waveguides have a ridge structure.

[2] Notice that if the higher refractive index contrast of SiO_2/Si : cladding/core structure was used, waveguides had to be made much smaller in order to preserve single mode operation, which would have made the fabrication more challenging.

[3] In Chapter 5, different lower cladding heights used for fabricating different batches and their corresponding required bonding layer thickness will be discussed.

The effect of misalignments between the axis of laser and dielectric waveguides were also considered by E. Barkley. For instance, a vertical misalignment of 300nm was simulated to increase the loss by 0.5dB for a gap width of 3μm. However, for smaller gap widths, the vertical misalignment will be more important in increasing the coupling loss as shown in Figure 4- 1. This is expected, considering the ability of the mode to spread and cover more area of the second waveguide in the case of the presence of a gap. Also, the effect of angled sidewalls (resulting from the etch process) on the coupling was studied. A slope of 12˚ (a typical value for the fabricated waveguides) was shown to introduce another 0.5dB of loss.

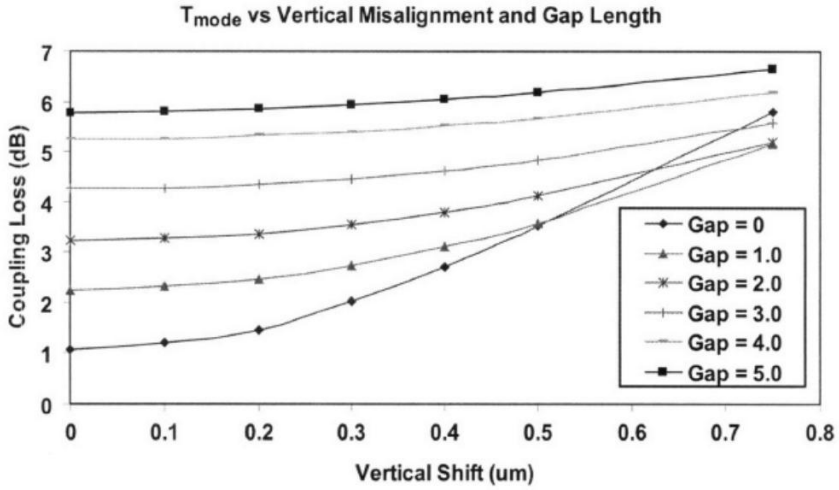


Figure 4- 1: FDTD simulation results: normalized T_{mode} versus vertical displacement for six different gap lengths (normalized $T_{mode} = T_{mode}/(1-R_{mode})$ and was used to remove the resonance introduced by the presence of the gap), pp. 109 of [59].

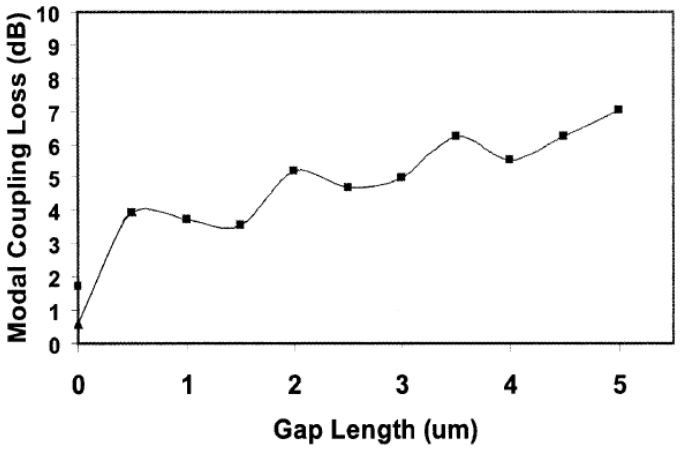


Figure 4- 2: FDTD 2D simulation, T_{mode} vs. gap length. n_{core}=1.55, pp. 103 of [59].

Overall, it was concluded that for the case of a large gap of 5μm the total worst case coupling loss would be 17dB. This includes 7dB loss due to the gap (seen in Figure 4- 2), in

addition to a 0.5dB loss for vertical misalignment, 0.5dB for non-vertical sidewalls, and 4dB for horizontal misalignment contributed (although this has been done with a 2µm guide for laser which is quite far from the 6.8µm reality of the fabricated ridge width). The total loss of 17dB can be decreased significantly for silicon rich nitride gap fill (n=2.2) and better alignments.

Also it is worth mentioning that the accuracy of deposited dielectric layers in this work is about 0.05µm which is highly consistent with the 50nm variation of the profilometer measurements described in Chapter 5.

In general, the simulations done in Chapter 3 of [59] are two dimensional only and mostly served as a preliminary workout to tackle the design questions. Furthermore the parameters used differ from the actual fabricated structures. More importantly, in [59] the coupling from dielectric waveguide to laser waveguide is studied only. However in the integrated laser, the coupling occurs in the reverse direction (from laser ridge guide to dielectric waveguide), which with the presence of air gap does not necessarily equate the coupling from dielectric waveguide to laser waveguide. All these limit comparing the results of simulations done in [59] to the measurement results obtained in Chapter 6 of this thesis.

In the following sections, the details about the fabrication of these waveguides along with the etched recesses will be discussed.

4.1.2. Fabrication of Dielectric Waveguides

The SiON optical waveguides[4] consist of a silicon-oxynitride core (n=1.6) with height of 0.7µm and a silicon dioxide cladding (n=1.45). The waveguide layers were deposited through Dense Chemical Vapor Deposition (DCVD) and the core was patterned by reactive ion etching (RIE).

For the deposition of the silicon dioxide claddings, silane (SiH_4) and oxygen (O_2) gases were used. Nitrous oxide (N_2O) was added to the gas mixture for the deposition of the SiON core. The waveguide stack was annealed once after the lower cladding and core were deposited and then again with the whole stack.

[4] These dielectric optical waveguides can replace the copper interconnects in the all optical integrated circuit systems.

Two issues were encountered in the fabrication of the dielectric waveguide stack. First, the compressive stress (intrinsic and thermal) of the deposited waveguide layers made the wafer bow. This issue was addressed through the deposition of same waveguide stack at the back of the Si wafer, to neutralize the stress. The second issue was the unwanted hydrogen content in the deposited layers. Since the vibrational mode of N-H bonds is matched with the 1.55μm wavelength, the presence of hydrogen in the deposited dielectric induces propagation losses if not treated. In E. Barkley's work, the high temperature anneal (at 1050˚C for 4 hours[5]) was used as a solution, although other CMOS compatible techniques can avoid deposition with hydrogen containing precursors and are suggested for future developments of the process[6].

For patterning and etching of the waveguide core, RIE had been used with a 1:1 combination of CHF_3:CF_4, trading off etch selectivity for desired vertical sidewalls[7].

4.1.3. Characterization of Dielectric Waveguides

Optical characterization of these fabricated waveguides with core width of 1.7μm has shown a 7.3 dB/cm average propagation loss[8]. At the final stage when passive (unstimulated) lasers were assembled into the wells, a loss of 17.75 dB was measured[9], comparable to the 18.5 dB loss obtained from FDTD simulations.

[5] Annealing at longer periods and higher temperatures has proven to reduce the hydrogen based propagation loss even further.

[6] For instance sputtering from a silicon-nitride target is one of those hydrogen-free precursor options.

[7] Here since the core is less than a micron, high selectivity wasn't a concern. Therefore higher composition of CF_4 (1:1 of CHF_3:CF_4) was chosen to make the sidewalls vertical. Later, for the etching of recesses, it was seen that increasing the CHF_3 is essential to achieve high enough selectivity that can preserve the mask for the deep well etch. Therefore the chemistry of 3:1 of CHF_3:CF_4 was used for that case.

[8] Propagation loss of 7.3dB/cm is quite high compared to reported very low loss on the order of 0.01dB/cm for SiON waveguides [82]. However it is not too far from the reported propagation losses of 0.1dB/cm [82] to 5dB/cm [83] where the primary goal of the research wasn't achieving ultra low-loss waveguides. The processing method used in these cases is very similar to the fabrication method used here by E. Barkley [59]. Also the propagation losses reported above are mainly for about twice the width of waveguides fabricated here. For wider waveguides, the loss is lower since the mode sees less of the sidewalls roughness of the etched core. Furthermore annealing the waveguides at higher temperatures than what was used here reduces the propagation loss considerably [84].

[9] As mentioned earlier, these measurements are for the case that the III/V edge emitting lasers were simply put in the wells and were not pumped. Thus only the passive transmission loss in SiON_guide - gap - III/V laser (passive) - gap - SiON_guide structure was looked into, without any attempt to optimize the vertical alignment of the waveguides, nor to bond the lasers in recesses.

4.1.4. Fabrication of Recesses

In the next step, a deep well (7-8µm) is etched in the path of the SiON waveguide, in which the III-V photonic device, in this case the edge emitting InP/InGaAs laser diode, will be assembled. The size of the recesses ranges from 135µm to 150 µm in width, and from 293µm to 312µm in length as shown in Figure 4- 3. Thus, only some of these wells would provide a suitable fit for laser pills with nominal dimensions of 150µm in width and 300µm in length. Zoomed in top-view image of one of the etched recesses with dimensions of 303 µm×150 µm is shown in Figure 4- 4 , where the SiON waveguide aligned with the center of the recess can also be seen. Upon integration, the ridge of laser platelet is coaxially aligned with the core of this SiON waveguide.

The wells are etched through the waveguide stack until the silicon substrate is reached. The well depth theoretically[10] ranges from 6µm to 7.2µm, corresponding to lower claddings thicknesses in the range of 3µm to 4.2µm for the different fabricated batches listed in Table 4- 1, and a constant 3µm thickness for upper claddings. Therefore, in order to achieve a high enough selective etch (to be able to etch a well 8µm deep) a 1.5µm polysilicon hard mask deposited by LPCVD was used[11]. Similar to patterning the waveguides, recess etching was done with RIE using a CHF_3:CF_4 mixture but now with 3:1 ratio for higher selectivity[12].

It is worth mentioning that in the SiO_2 recess etching phase, over-etching into the Si substrate was possible but ignored in [59]. A more careful study of this factor will be presented in Chapter 5.

[10] Later on in Chapter 5 we will see that these theoretical dimensions are different from the actual dimensions in the fabricated components; for instance, see Tables 5- 3 to 5- 6.
[11] In order to pattern this polysilicon hardmask, an oxide layer was deposited and patterned, which served the role of the photoresist that was not a patterning mask option due to the thickness of the polysilicon.
[12] The higher selectivity is at the expense of less vertical sidewalls of about 80˚ angle.

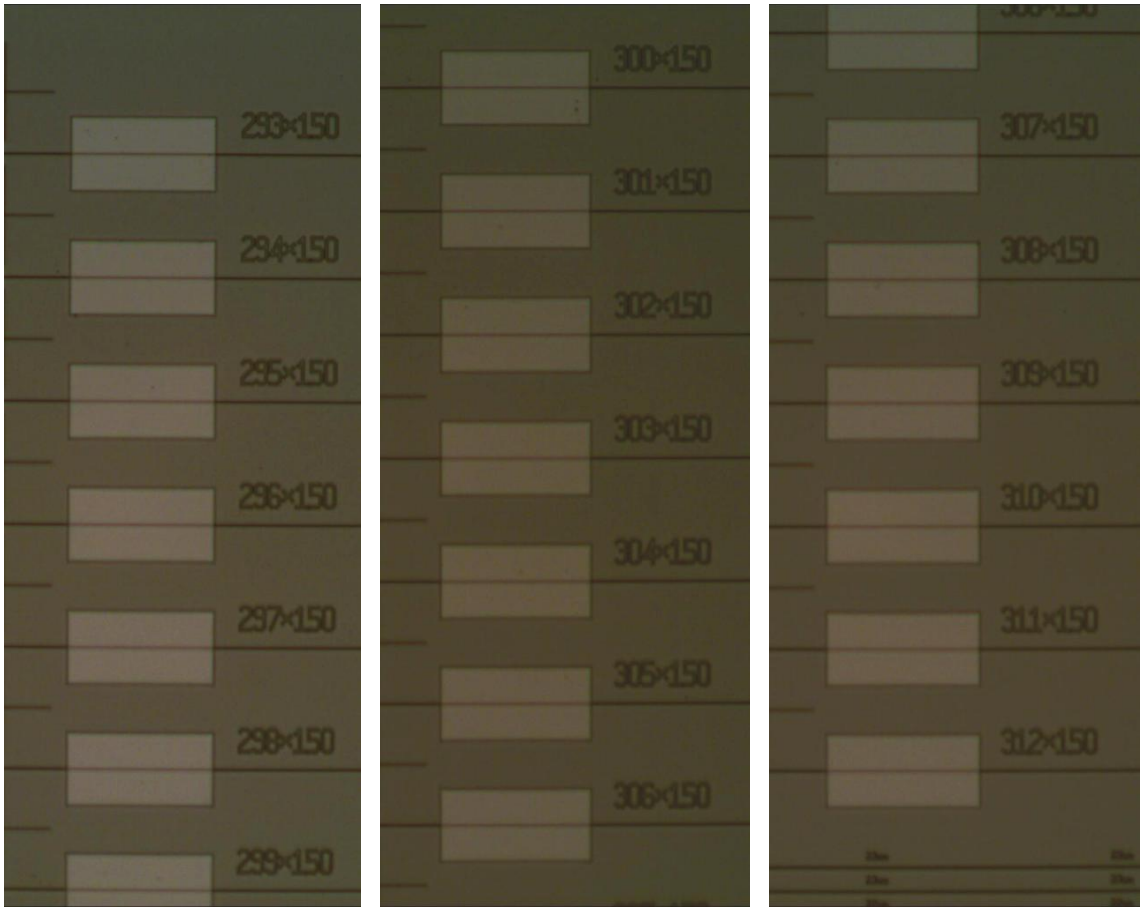


Figure 4- 3: Recesses of various lengths etched into the SiO_2 dielectric stack on Si substrate. The SiON dielectric waveguides aligned with the center of recesses are also noticeable in these images.

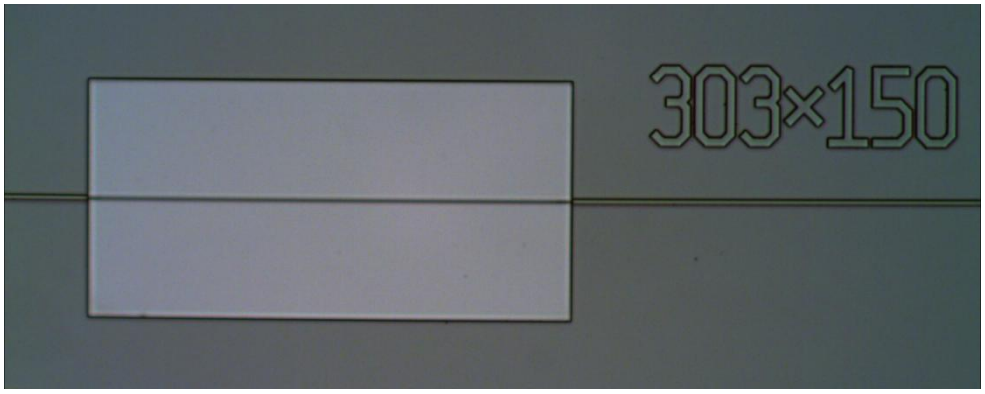


Figure 4- 4: Zoomed in top-view image of an etched recess with dimensions of 303µm×150µm.

Batch #	Expected Lower Cladding (µm)	Expected Well Height (µm)
B6-13	4.2	7.2
B6-10	3.9	6.9
B6-7	3.6	6.6
B6-4	3.3	6.3
B6-2	3	6
B6-1	3	6

Table 4- 1: List of fabricated dielectric waveguide batches with different lower cladding thicknesses, thus various expected recess heights.

4.1.5. Die-saw Assisted Cleave

Finally, when the waveguides are deposited and recesses are etched, a die-saw assisted cleave is used to separate the dies for further processing steps, namely the assembly of laser pills into the wells, bonding and characterization.

The motivation behind the die-saw assisted cleave is to decrease the facet roughness that results from cleaving through the thick silicon wafer. Facet roughness contributes significantly to the scattering from the facet and thus decreases coupling. Since the waveguide stack is amorphous, its facet will be much rougher after the cleave, than the crystalline silicon facet underneath. To address this issue, a die-saw assisted cleave technique was used, in which the wafer is partially sawed from the backside[13], but not all the way through. About 100µm of the front side is left intact, which will cleave with the application of a gentle pressure[14]. For cleaving, the sample was placed between two aluminum blocks with backside facing up, and the die-saw cut point sticking out. Then, a torque was applied to the tip of sample using a razor blade, which cleaves the sample along the partly-die-sawed line.

At this point, the chips with the dielectric waveguides and etched recesses are ready for the next steps of integration process described in Chapter 5.

[13] The frontside is facing down and is protected from contact with the die-saw tape through a protective resist layer.

[14] Ideally the dies had better not cleave during tape removal, as when this happens the facet quality becomes quite poor. Therefore it is preferred (although hard to achieve) that dies stay uncleaved during tape removal and then get cleaved by applying a torque afterwards.

4.2. Active Component: Edge Emitting InGaAs MQW Platelet Laser Diodes

As discussed before, the integration of room temperature edge emitting laser diodes is one of the most important steps in this demonstration of achieving the full integration of optoelectronics on silicon integrated circuits. The InGaAs/InP laser platelets will be assembled and bonded in recesses made on a Si substrate. In order to cleave these thin (6μm) platelet lasers, a novel micro-cleaving process has been developed in [60][15].

In the following sections, first the performance characteristics of the fabricated InGaAs MQW ridge lasers are summarized and then the detailed processing steps for fabricating these laser diodes are explained.

4.2.1. Characterization of Fabricated InGaAs/InP Edge Emitting Laser Diodes

According to J. Rumpler's thesis [60], 300μm long MQW InGaAs laser diode platelets simply placed on a Si substrate have shown continuous-wave lasing at temperatures as high as 55˚C, and pulsed lasing to at least 80˚C. The output power of these lasers was as high as 26.8mW (at T=10.3˚C) with differential efficiency of 81% and threshold currents as low as 18mA. For these lasers placed on a Si substrate, the characteristic temperatures T_0 and T_1 were measured to be 43K and 85K respectively. Also the performance of these laser diodes placed on the Si substrate was compared to those on their native substrate of InP and it was found that the former outperforms the latter[16] in terms of thermal characteristics, output power and differential efficiency.

In the following sections, the details regarding the fabrication of these laser diodes will be reviewed.

[15] Besides reaching crystalline cleaved facets, the micro-cleaving technology also provides a vehicle to precisely define laser cavity length of the order of 300μm ±1.25μm.

[16] The same result that was also achieved and confirmed in the VCSEL project done by J. Perkins [58] in our group.

4.2.2. Fabrication of Edge Emitting Platelet Laser Diodes

- 4.2.2.1. Epitaxial Layer Structure of MQW InGaAs Laser Diodes

Instead of growing epitaxial layers of edge emitting lasers in house, Landmark Optoelectronics [85] 1.55µm wafers with epitaxially grown MQW heterostructure on InP were used in fabricating the laser platelets. Table 4- 2 shows the layer sequence of these wafers.

Layer #	Material Type	Doping	Function	Thickness	λ (µm)
9	$In_{(1-x)}\ Ga_x\ As$	P^+	Ohmic Contact	200nm	-
8	InP	P	Ridge	1.5µm	0.92
7	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	P	Etch Stop	7nm	1.3
6	InP	P	Upper Cladding	200nm	0.92
5	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Upper Core	110nm	1.25
4	$4 \times In_{(1-x)}\ Ga_x\ As$	U	QW	6nm each	1.75
	$3 \times In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Barriers	9nm each	1.25
3	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Lower Core	110nm	1.25
2	InP	N	Lower Cladding	2.8µm	0.92
1	$In_{(1-x)}\ Ga_x\ As$	N^+	Backside Etch Stop	500nm	-
0	InP substrate	N	Native Substrate	350µm	0.92

Table 4- 2: InGaAs/InP 1.55µm MQW laser epitaxial layer structure fabricated by Landmark Optoelectronics Corp.

The substrate is an n-type InP wafer and is highly doped with S to $N_D=2.8\times10^{18}\ cm^{-3}$. Next, as we required, the supplier added a 500nm of n-type $In_{0.53}Ga_{0.47}As$ layer, lattice matched to InP, to their generic structure. This layer serves two purposes, forming a low resistance n-type ohmic contact for the bottom of the laser pill, and providing a reliable etch stop in subsequent fabrication steps in which the substrate is completely etched away to release the individual laser platelets from the substrate.

The next layer is a 2800nm n-type InP layer, which again has the dual purpose of a lower cladding (with lower refractive index than the core), and also being the electron rich injecting region in forward bias. As a side benefit, this layer also isolates the optical mode in the core from the lower InGaAs high refractive index contact layer.

Above the lower cladding, a 271nm[17] stack of undoped InGaAs/InGaAsP MQW layers forms the active region where stimulated emission takes place, in which due to its higher refractive index the optical mode is also confined. The MQW stack consists of four 6nm InGaAs quantum wells (λ=1.75μm) separated by three 9nm InGaAsP barriers (λ=1.25μm), and finally the stack is sandwiched by two 110nm thick InGaAsP layers (λ=1.25μm).

On top of the MQW stack, a 200nm p-type InP layer serves as the upper cladding. Then a very thin (7nm) InGaAsP layer provides an etch stop used in defining the ridge waveguide in the subsequent ridge-formation etching step[18].

The 1500nm InP upper cladding layer on top works similar to the 2800nm lower cladding, with the mere difference that being highly doped p-type, it also provides a source for injecting holes into the active region.

Finally, a 200nm thick highly doped $N_A=2\times10^{18}$ cm^{-3} p-type InGaAs layer (similar to its n-type counterpart at the bottom) makes the formation of the top ohmic contact feasible.

- 4.2.2.2. Front End Processing of Conventionally Cleaved Laser Diodes

- Initial Top Ohmic Contact

The front end processing of edge emitting laser diodes starts with the deposition and lift-off a 300nm p-type Ti/Pt/Au ohmic contact[19] on top of the wafer, patterned[20] to the stripes of the ridge width. When the lift-off step is complete, in order to reduce the contact resistance, rapid thermal anneal (RTA) at 385˚C for 30s in forming gas (95% N_2, 5% H_2) environment is performed[21]. One other significant benefit of this annealing step is to increase the adhesion of the metal contact layer, which had been a serious issue as the metal stripes peeled off during the ridge wet etch in samples that did not undergo the annealing step.

[17] The 271nm of active region core (used also in subsequent simulations) includes two 110nm of upper and lower cores, 4 quantum wells, each 6nm, and 3 barriers, each 9nm.
[18] HCl proves to be a great etchant candidate in this case since it etches InP at a high rate and stops at the InGaAsP etch stop layer.
[19] The exact composition of this p-type ohmic contact for InP or InGaAs is: Ti(300Å) /Pt(200Å) /Au(2500Å), where the Ti serves as the adhesion layer, Pt prevents the diffusion of Au into the semiconductor and out diffusion of In from the substrate at increased temperatures, and finally Au on top is the low resistance inert metal contact.
[20] Close care was taken to align the stripes with the [011] cleavage plane of [100] substrate so that the cleaving step results in mirror smooth facets.
[21] This annealing step alloys the Ti-InGaAs interface.

- **Semiconductor Ridge Waveguide Formation**

In order to etch the ridge waveguide on top of the active region, which gives horizontal confinement of the guided optical mode as well as electrical carrier flow, the Ti/Pt/Au ohmic contact stripes serve as a self aligned etch mask. Initially the top 200nm p-type InGaAs is etched at room temperature by a 20:1:1 mixture of H_2O:H_2O_2:H_2SO_4 which stops at the InP layer. Then concentrated HCl (37%) is used to etch the 1.5µm upper cladding InP layer, which selectively stops at the InGaAsP 7nm etch stop layer.

- **Device Planarization**

Since the Ti/Pt/Au ohmic contact is only on the narrow ridge area (2-3µm[22]), it is not sufficient for low contact resistance, and not convenient when it comes to probing the devices. Therefore a large area contact pad is required, for which the device should be planarized, i.e. the 2µm deep hollow area outside the ridge will be filled with a dielectric (e.g. BCB) and then the large area contact is deposited on the planarized surface on top.

The planarization dielectric used in this project is Cyclotene, by DOW Chemical, and is primarily composed of B-staged bisbenzocyclobutene-based (BCB) monomers, a strong insulator with large break down field (5×10^6 V/cm), and low refractive index (n=1.54).

As shown in the schematics of Figure 4- 5, the planarization process steps are as follows: First a layer of Cyclotene is spun on the wafer, followed by curing at 210˚C for 40min in an annealing furnace[23]. After the first curing step, the second coat of Cyclotene is applied and the sample is cured once again at 250˚C for 60min.

The sample is almost planar at this stage, however a thin layer of Cyclotene is covering the ohmic contact thus shielding the electrical connection. Therefore, an etch-back step is required to expose the metal ridge contact once again. This etch-back step is done in RIE (Plasmatherm) with a 6:1 mixture of O_2:SF_6 at a relatively high pressure (200 mtorr) and low RF power (150 W). In fact, due to process variations, an over etch was usually performed, in which the low RF power prevented out-sputtering of the exposed metal contact. The end point detection of the etch-back step was done manually by frequent inspection of the sample under microscope between etch steps.

[22] In final fabricated lasers, ridges are 6.8µm in width, thus noticeably larger than the ideal value of 2µm.
[23] During this annealing step, care is taken to prevent oxidation of the BCB film, through flushing the chamber with nitrogen 30min before as well as through the curing step.

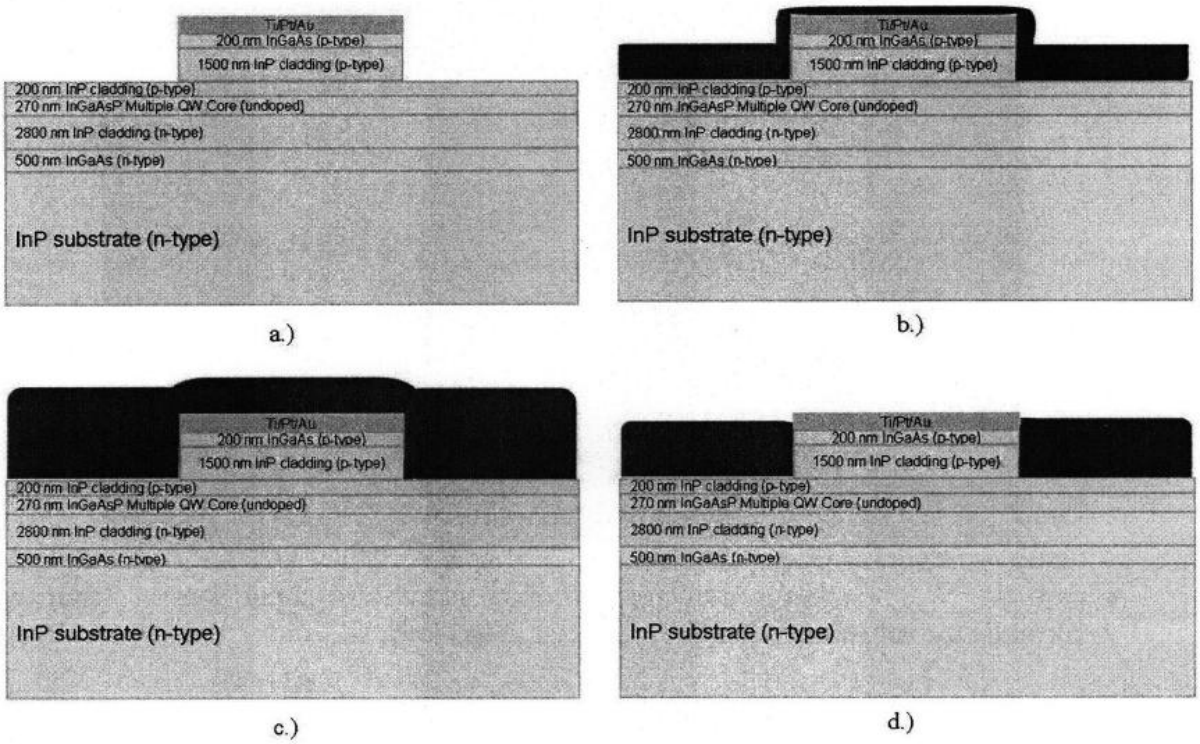


Figure 4- 5: Schematic of dielectric layer deposition and planarization steps: a) Initial structure after ridge formation, b) First coat of Cyclotene and the subsequent cure, c) Second coat of Cyclotene and cure, d) Cyclotene etch-back step. (Schematic from pp. 96 of [60])

- **Large Area Top Electrical Contact**

At this stage, the laser ridge structure is planarized with Cyclotene and the ohmic contact covering the ridge top is exposed via the etch-back step. Therefore the device is ready for large area top contact metallization, which consists of a Cr adhesion layer followed by few hundred nm of Au[24].

Having the top metallization deposited and patterned through lift-off, the front side processing is concluded. In the next section we will review the back side processing steps for these lasers.

[24] This large area contact pad is essential not only due to probing mechanics, but more importantly for achieving a low resistance contact which is important in reducing the voltage drop between two probe points; a fundamental initial problem that prevented the whole length of the laser getting biased above threshold and thus the emission would be merely spontaneous and the stimulated emission would not occur.

- 4.2.2.3. Back Side Processing of Laser Diodes

After the completion of front side processing of the lasers, the back end processing is started, in which first the substrate is thinned from the back side so that the cleave step results in mirror smooth facets, and then the back side n-type ohmic contact is deposited.

- Substrate Thinning

The InP substrate on which the laser expitaxial layers are grown, is 350µm thick initially. For conventionally cleaved lasers, in this step, approximately 100-150µm of the substrate thickness will be removed from the back side. Although CMP (Chemical-Mechanical Polishing) is one possible approach for this purpose, HCl wet etching was used instead. In order to protect the front side of the wafer (which houses the processed lasers), a layer of thick photoresist (AZ4620) is spun on the front side, and then with Apiezon™ wax adhesive is mounted on a Si carrier substrate. Now the sample is ready for HCl back side wet etching with an approximate rate of 6µm/s.

- Back Side n-type Ohmic Contact

After the thinning of the substrate, backside n-type ohmic contact of Ni(50Å)/Au(100Å)/Ge(600Å)/Au(900Å)/Ni(300Å)/Au(1750Å)[25] is deposited by e-beam evaporation.

When the back side ohmic contact deposition is complete, the sample is placed in TCE (trichloroethylene) which dissolves the Apiezon™ wax while leaving the devices intact. Then the dies are scribed to shorter bars which undergo an annealing step at 385˚C for 30s to reduce the back side n-type contact resistance.

- 4.2.2.4. Micro-Cleaved Process vs. the Conventional Cleave Approach

Note that what was described so far pertains to the conventionally cleaved laser process. Instead, the final laser platelets that were used for integration (in this thesis), were fabricated through a novel Micro-Cleaving technique developed in our group by J. Rumpler

[25] While the Ni layer is mainly used for adhesion purposes, it is suggested that Ni enhances the diffusion of Ge into InP. Ge adds to the doping of InGaAs layer and thus a better quality ohmic contact forms (reinforced by subsequent annealing step). And finally Au is used for its very low ohmic resistance.

[60]. Here, instead of going through the whole process, which is in part similar to what was already described in previous section, only the differences of two processes are highlighted[26].

- 4.2.2.4.1. Front End Processing in Micro-Cleaved Case

The idea behind micro-cleaving is the to-be-cleaved facet is narrowed to a few tens of microns. Since the laser platelet is released from the InP substrate, such a thin platelet can easily cleave along the [011] crystalline plane, if the facet notch is made narrow enough (which is the motivation behind making the notches small compared to the 150µm width of the platelet). Once the laser platelets with these narrowed notches are released from the substrate[27], ultrasonic agitation will help them cleave along the crystalline facet and produce a smooth facet.

- Initial Top Ohmic Contact

The ridge metal contact[28] in the micro-cleaving approach is similar to the conventionally cleaved case discussed earlier, with one difference that the pattern is not continuous as before. Instead, the ridge metal is discontinuous where the cleaving is to happen. This was adopted through experience that any presence of amorphous/non-crystalline material along the to-be-cleaved facet, hampers the quality of cleave noticeably. Therefore, modifications to the mask sets were made so that no contact metal or Cyclotene is present in the micro-cleaved facets.

The SEM image in Figure 4- 6 shows this problem encountered when the metal ridge pattern was continuous, where the non-crystalline metal does not cleave along the facet and either gets peeled off from the ridge or leaves an unstable tail behind, similar to this SEM.

[26] Another option was to only review the micro-cleaved approach in this chapter. However since that process is rather complicated, the author thinks the process flow will be easier to comprehend if initially the conventionally cleaved approach is described and then the complexities of the micro-cleaving method is built upon that prior knowledge.

[27] At this stage there are bars of lasers in which individual lasers are still connected together via the notch areas.

[28] The deposited Ti/Pt/Au contact resistance was measured by TLM and has shown to have a resistance of 6×10^{-4} $\Omega.cm^2$, which is an order of magnitude higher than industry standards. System limitation of high vacuum pressure before and during deposition is considered to be the contributing factor in this process.

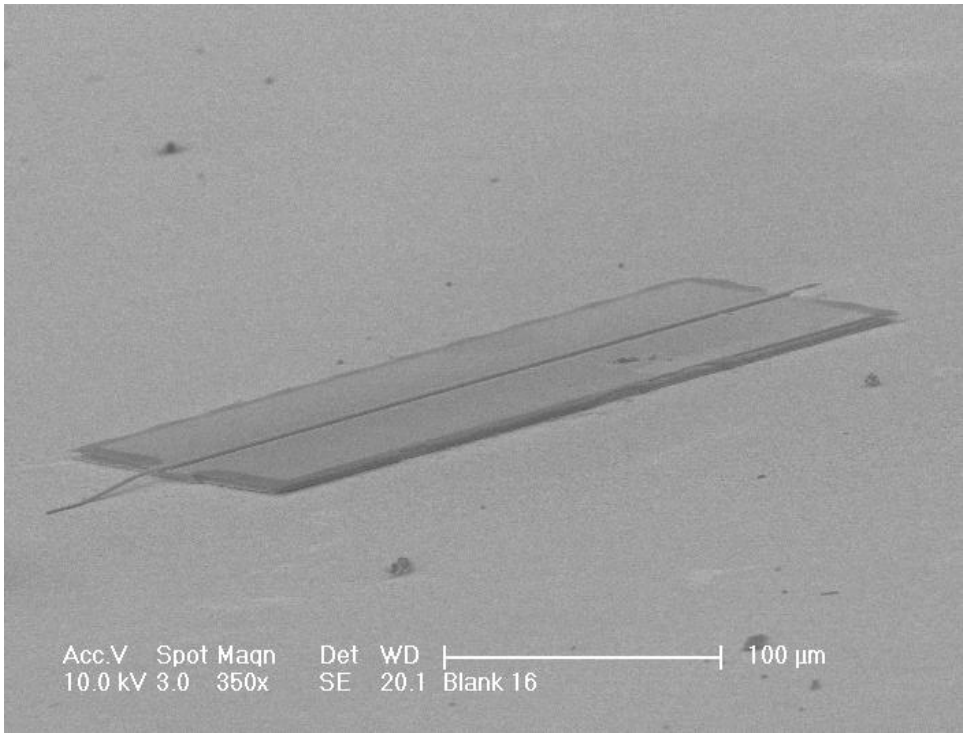


Figure 4- 6: SEM image showing the problem faced with continuous pattern of ridge metal which being non-crystalline, does not cleave along the facet edge and either peels off from the ridge or leaves an undesirable tail behind [60].

As discussed earlier, to address this issue a modified pattern for ridge metal had been adopted which is shown in the schematic of Figure 4- 7. The discontinuities correspond to notch regions where micro-cleaving will eventually happen.

Figure 4- 7: Schematic showing ridge metal pattern for micro-cleaving approach, pp. 107 of [60].

- **Semiconductor Ridge Etch**

Since the metal contact pattern has discontinuities, it cannot be used as a self aligned mask in the ridge formation step. Therefore an additional photoresist mask covers the discontinuities and an etch step is performed as before using HCl.

- **Device Planarization and Large Area Top Electrical Contact**

The Cyclotene coat and etch-back, as well as top large area contact deposition and patterning are similar to what was reviewed in the conventionally cleaved case, with one difference that the pattern is modified such that Cyclotene and metal contact are removed from the to-be-cleaved notch area, due to the same reason that motivated modifying the pattern of ridge metals discussed earlier.

- **Micro-Cleave Patterning and Etch**

Each individual laser platelet area needs to be defined to its 150µm×300µm size. In fact, this definition will make the release of the platelets feasible when the substrate is etched from the backside in subsequent steps. The schematic in Figure 4- 8 shows the pattern that defines these bars of lasers that are connected with to-be-cleaved notches.

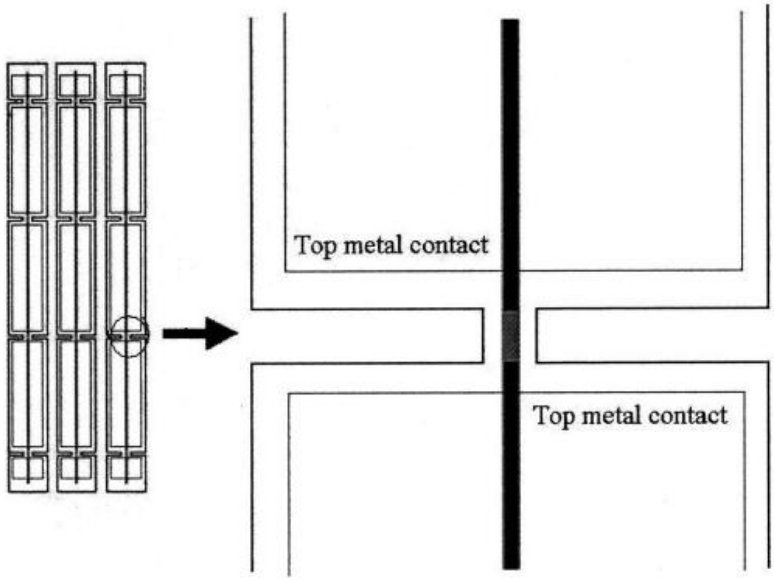


Figure 4- 8: Schematic showing the Micro-Cleave laser platelets pattern, and how it is aligned with the ridge and planar top large area ohmic contacts. Modified image from pp. 112 of [60].

The semiconductor etching with this pattern is done by a SAMCO Inductively Coupled Plasma (ICP) Etching system at Lincoln Laboratory. A hardmask of SiO_2 is used to ensure that the mask will bear this etch step. SEM graphs in Figure 4- 9 show preliminary results[29] of the vertical sidewalls achieved in this step using the micro-cleave pattern.

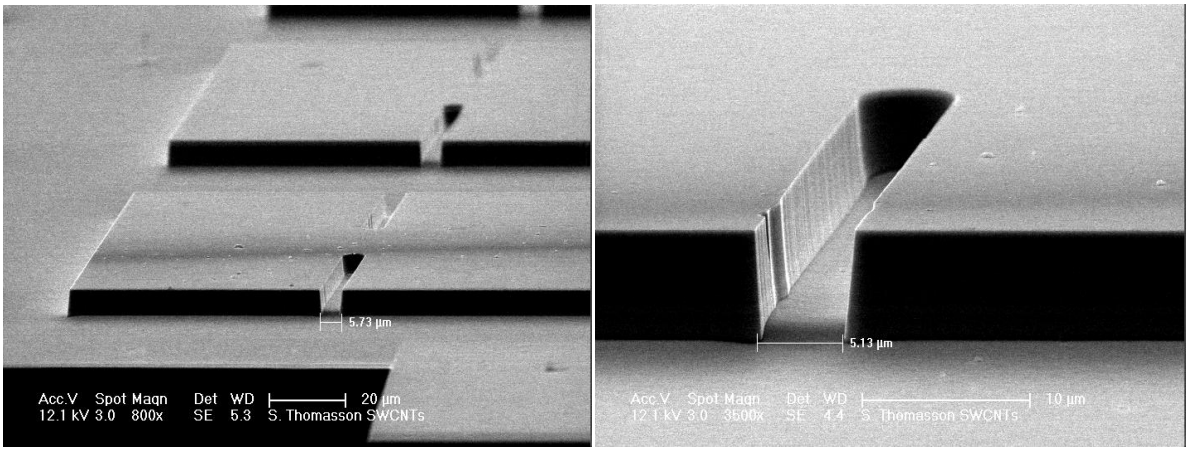


Figure 4- 9: SEM images of initial attempts to laser platelet definition, where vertical sidewalls can be seen in this micro-cleaving pattern [60].

The etched height in actual samples is about 3.5µm and goes halfway through the (backside etch stop) InGaAs layer[30] as the chemistry ($SiCl_4$ (0.5sccm) and Ar (10sccm) at 250W), used in this dry-etch is not selective[31] to InGaAs.

- 4.2.2.4.2. Back Side Processing in Micro-Cleaved Case

At this stage the front side processing of the lasers is concluded. The backside processing entails substrate removal and backside ohmic contacts deposition, which will be discussed in the following subsections.

- InP Substrate Removal

First a protective layer is deposited on wafer's front side, and the wafer with its frontside facing down is mounted on a Si carrier wafer. Then, the backside InP substrate is removed in a wet etching step that stops at the backside InGaAs etch stop layer.

[29] These images are from dry-etching trials and the samples did not have metallization or ridge formation.
[30] This etching through InGaAs layer becomes handy later when trying to do the patterning of backside n-contact metallization rectangles.
[31] Wet etches selective to InGaAs turned out to be incompatible with Cyclotene used for planarizing the top surface.

The challenge in this step is that later on the backside metallization layer needs to be patterned to platelet shapes, whereas in the conventionally cleaved case a uniform backside metallization sufficed without any further patterning.

In order to choose a proper protective/adhesive material, five different options were considered: photoresist, Brewer ProTex™, Apiezon® Wax, photoresist + Apiezon®[32] and Bewer WaferBOND™. The layer needs to be resilient to the wet-etch acid chemistry (HCl) and acetone used in lift off process, it needs to be planar for backside photolithography, and must be easily removable without leaving clutters sticking laser platelets together. Through careful study of each option, it turned out that only Bewer WaferBOND™ meets all these requirements.

- **Backside Ohmic Contact Formation**

After InP substrate is removed through a wet etch, the InGaAs layer is thinned by about 300nm. Care was taken not to remove all of the InGaAs, as it is helpful in formation of a good ohmic contact. The reason for thinning this layer comes from the need to align the backside ohmic contact metallization pattern (rectangles) to the front side laser bars and to-be-cleaved notches. Since the InGaAs under the laser platelets is thicker compared to outside the platelets (remember that in the front side processing, the exposed InGaAs was also thinned a bit), punches could be made through the wafer in the areas surrounding the bars in order to make the front to back side patterning possible[33].

Then through lift off, the backside ohmic contact of Ni(50Å)/Au(100Å)/Ge(600Å)/ Au(900Å)/Ni(300Å)/Au(1750Å) is deposited and patterned[34]. The schematic in Figure 4- 10 shows the structure at this stage, where the backside contact is patterned and the front side is still faced down and protected in WaferBOND™. Notice the alignment of the backside contact with the front side ridge definition, planarization, and front side large area ohmic contact.

[32] This combination was used in the conventionally cleaved case, however in the micro-cleaved case, the front side was non planar with this combination, an issue for the backside photolithography.
[33] Note that even a front&back side double aligner would not have helped in this case, since front side is covered by the adhesive and a carrier wafer.
[34] This contact has a resistivity of 1×10^{-5} $\Omega.cm^2$, which is an instance of the easier formation of good n-type ohmic contacts than p-type ones on InP. To alleviate this issue a lattice matched layer of InGaAs deposited on p-type InP becomes helpful.

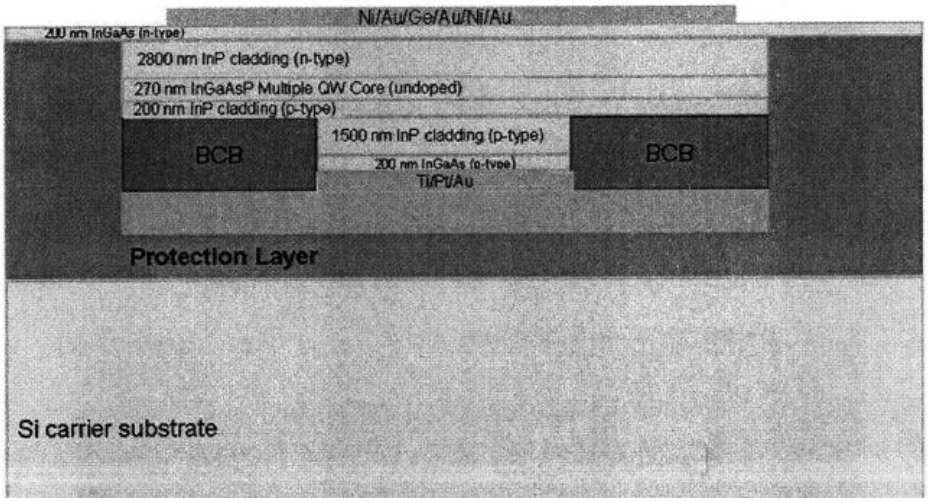


Figure 4- 10: Schematic showing back side metallization of the laser platelets aligned and patterned to the front side contact, while front side is being held by WaferBOND on a carrier Si substrate [60].

- **Laser Platelets Release**

Now that the backside metallization is finalized, the backside processing is concluded and the WaferBOND™ protective layer is removed using the manufacturer's solvent for this purpose. Hence, long laser bars are released (still connected in the to-be-cleaved notches in a form of a long bar) sitting on a Teflon substrate. The solvent is removed with care, and laser bars are cleaned[35] with a series of acetone and methanol rinses while care is taken not to disturb the low weight released laser bars in the solution. Finally the laser bars are rinsed with isopropanol and then dried at 115˚C for 30min. The SEM image in Figure 4- 11 shows two of these released and to-be-cleaved laser bars.

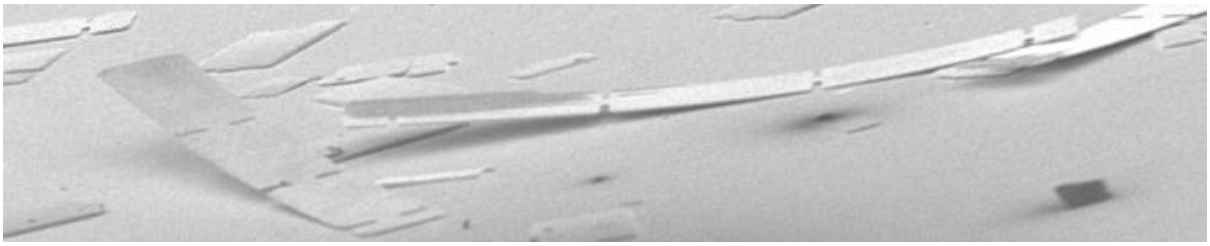


Figure 4- 11: SEM image of released laser stripes [60]. In the next micro-cleaving step, individual laser platelets will release as they preferentially cleave along the notches with ultrasonic agitation.

[35] Well rinsing the lasers from WaferBOND™ remover solvent is essential as Cyclotene BCB is not very compatible with the solvent remaining residues, which will make the top contact fragile.

- 4.2.2.5. Micro-Cleaving

The laser bars floating in an isopropanol container are ultrasonically agitated, causing them to cleave preferentially at the notch regions and along the [011] crystalline surface. As seen in the SEM image in Figure 4- 12 the facets are very smooth, which shows the success of the micro-cleaving idea.

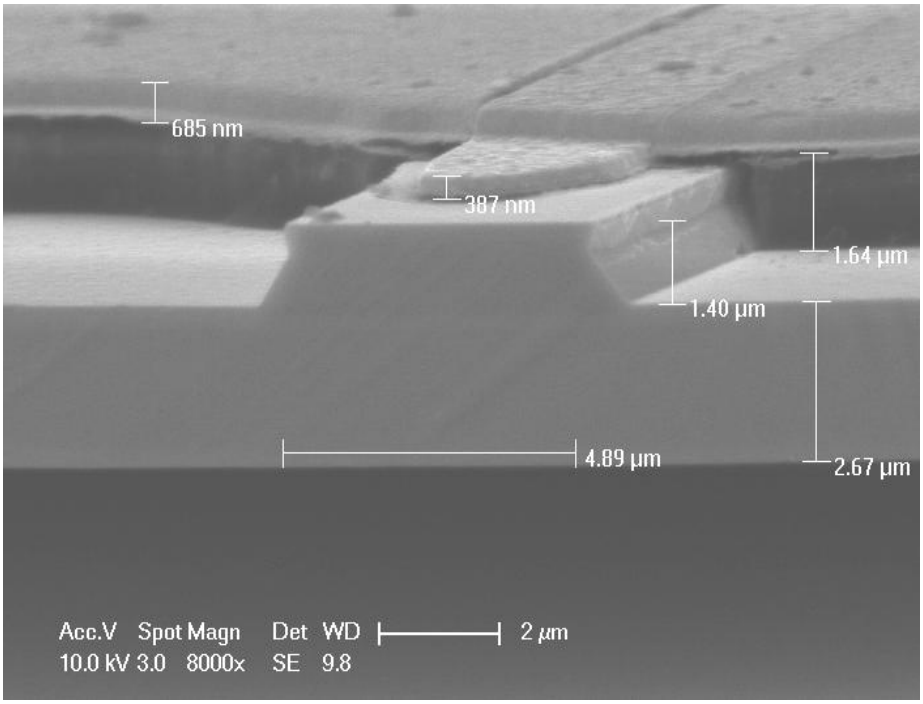


Figure 4- 12: SEM image showing the micro cleaved facet of a released laser platelet [60].

Figure 4- 13 shows another SEM image of a laser platelet looking at the front facet. Top view photographs of these laser platelets are shown in Figure 4- 14 and Figure 4- 15, and Figure 4- 16 depicts an image of a laser with backside facing up showing the patterned backside n-contact of these laser platelets.

At this point, the laser platelets are released, finalized and are ready to be integrated, which will be detailed in the next chapter.

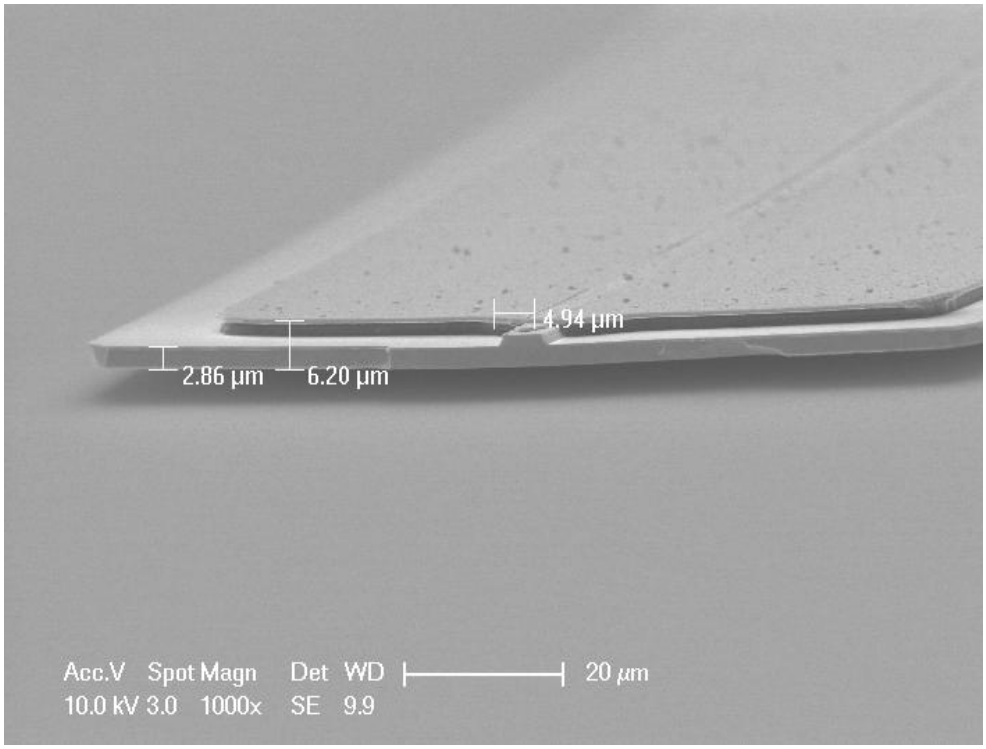


Figure 4- 13: SEM image of a released laser platelet [60]. The planarized top contact and high quality micro-cleaved facet at the notch area are noticeable.

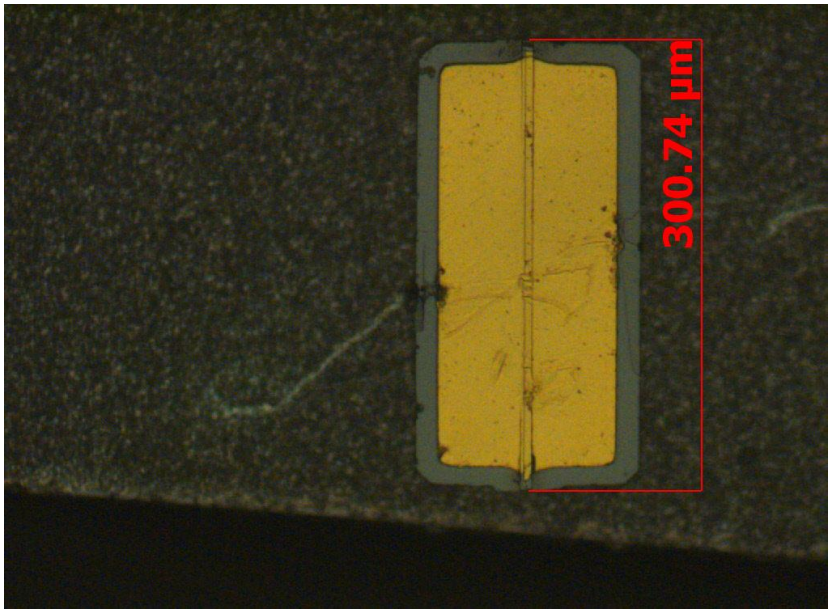


Figure 4- 14: Top-down photograph of micro-cleaved ridge laser (MC6) sitting on silicon [86].

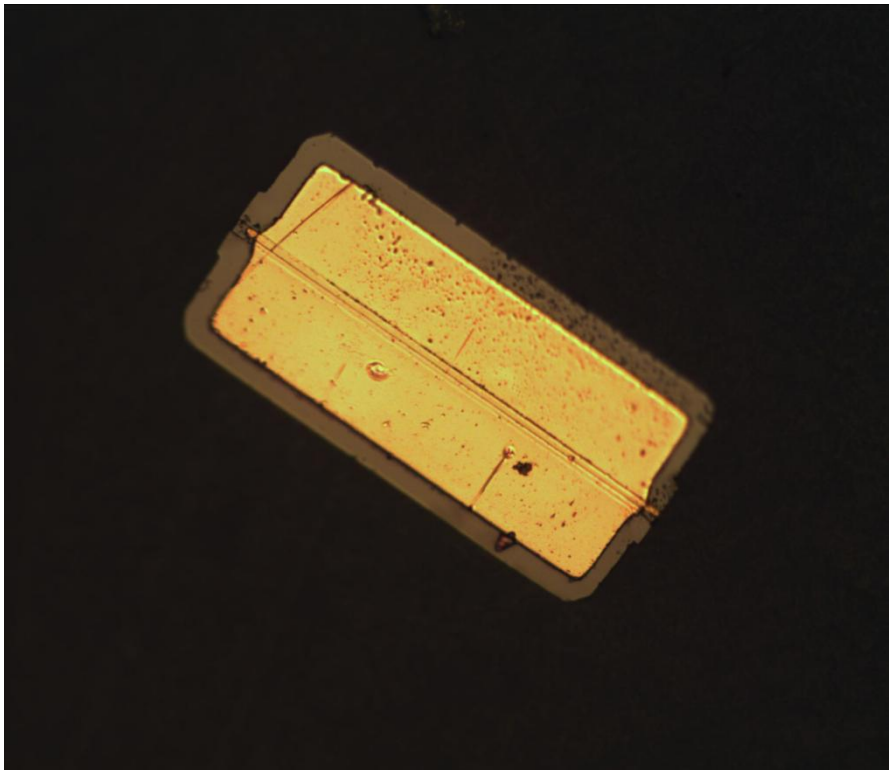


Figure 4- 15: Photograph of the front side of a released laser platelet ready to be integrated. The ridge structure on the topside p-contact is also visible.

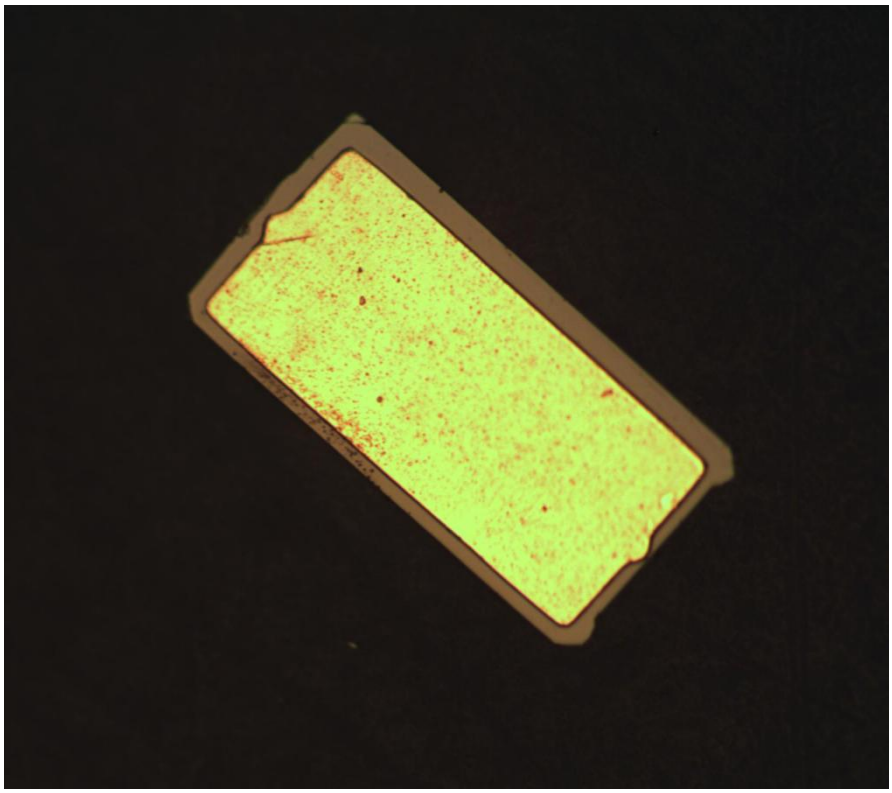


Figure 4- 16: Image of the backside of a laser platelet showing the patterned backside n-contact.

Chapter 5

Integration Process

In this chapter the process of integrating laser platelets in recesses etched out on the silicon chip is discussed. First, the integration process steps are reviewed leading to the discussion about the features of bonding layer and its patterning. Then, the assembly phase and the bonding steps are described. Given the importance of vertical alignment of two guides in our coaxial integration approach, the results of a study to optimize the thickness of the bonding layer based on the on-hand lasers and dielectric recesses is presented. Finally, micrographs of the integrated laser platelets in recesses are shown, as the finalized devices ready for measurements whose results will be discussed in Chapter 6.

5.1. Integration Steps

In this section, the detailed fabrication process to integrate the edge emitting laser platelets in the recesses and aligned with the waveguides on the Si chip is described.

As discussed in Chapter 4, having the recesses, dielectric waveguides and free standing laser diode platelets fabricated separately (by previous PhD candidates in our group), the components are ready for integration, which is a 3-step process consisting of:

a) Optimization, deposition and patterning of the bonding layer
b) Assembly of the laser diode pills in the recesses etched to intersect the SiON waveguides on the Si substrate
c) Solder-bonding the lasers in the recesses

5.2. Bonding[1] Layer

For this integration, thin-film solder-bonding was selected in contrast to other integration methods like wafer bonding or metal-to-metal pressure bonding. In solder-bonding, melting and resolidification of the solder metal occurs and provides a good mechanical bond between the two structures.

Therefore, an important part of this integration process is to bond the laser platelets in recesses and thus the following section will discuss the details about the importance of this layer, how the material composition was selected and the deposition methods that were employed.

5.2.1. Significance

The bonding layer has a number of very important roles in this process. Firstly, it needs to provide a mechanically strong bond to hold the assembled photonic component in the recess etched on chip. Secondly, the bonding temperature needs to be low enough that no damage is done to the laser or the Si IC electronics. Thirdly, the bonding layer also brings the laser backside n-contact to the front side of the wafer in this work, for ease of drive probing and measurements. For this reason, it is very important that the bonding layer has good continuity over the sharp and rather vertical sidewalls of the wells. And lastly, the height of the bonding layer is a very helpful tool for optimizing the vertical alignment of the SiON core of dielectric waveguide and the MQW active layer of the InGaAs laser diode. Since various batches of the waveguides with a range of lower cladding heights of 3 to 4.2µm have been fabricated on the Si substrate, and laser height is fixed, the bonding layer height provides a handy tool in optimizing for the perfect alignment for each batch. Furthermore, the height of this layer should be consistently reproducible and change the least during the pressured heated bonding phase.

5.2.2. Composition

The three roles of the bonding layer discussed above have been carefully taken into account in order to choose the most proper bonding layer composition and processing

[1] The term "bonding" might not be the most accurate term for this process, as it usually refers to the bonding of two wafers. A better phrase is "solder-bonding" which entails the melting and resolidification feature of the bond used in this project. However for ease of referencing, from now on the abbreviated term of "bonding" will be used instead of more accurate term of thin film solder-bonding.

scenario. For the composition of the bonding layer, a sequence of aluminum and indium (referred to as Al/In layer here after) was chosen.

The reason for this selection is as follows: indium (In) [2] is a rather soft metal with a low melting point of 156.6˚C [87], ideally suited to keep the integration thermal phase as low temperature as possible and make the process CMOS compatible.

Initially, we intended to have the bonding layer to be entirely indium. However, further study of the properties of this layer and its fluidity and softness made us realize that the pressured bonding phase will compress and push out the bonding indium layer, making its height unreliable and not reproducible. Since the vertical alignment of two waveguide cores is critically important in the coaxial integration, one will appreciate how important it is to have a deterministic height for the bonding layer that is well optimized. With this in mind, we decided to add aluminum to the metal sequence, which has a higher melting point and thus remains rigid in the bonding phase. It also has a good conductivity, is CMOS compatible, is widely used in integrated circuit processes, and can be easily deposited and patterned.

Thus Al was chosen as the base of bonding layer, composing most of the required thickness of the bonding layer. For instance for batch B6-4, the required bonding layer thickness is found to be 975nm[3], for which 855nm of Al and 120nm of In were deposited.

It is worth mentioning that there is another criteria that determines the minimum In thickness, since it functions as the primary bonding agent. Previous studies performed in our group [88] have shown that in order to ensure a strong and reliable mechanical bond, there is a minimum required height for the In layer of about 80nm. Hence 120nm of In thickness was chosen to have a safety margin above this minimum[4].

The SEM image in Figure 5- 1 shows a peeled off Al/In segment, in which the sequence of these two layers can be observed.

[2] Fun Fact: The name of Indium comes from the indigo blue line in its spectrum, which gave the first indication of existence of this metal in Zinc ores (still the major source of In) in 1863.
[3] The process of calculating the optimum bonding layer height to ensure the best vertical alignment of the cores of laser and dielectric waveguides is presented later in this chapter.
4 Which primarily comes from the spreading of In of about 60nm with a pressure of 20psi in the bonding stage.

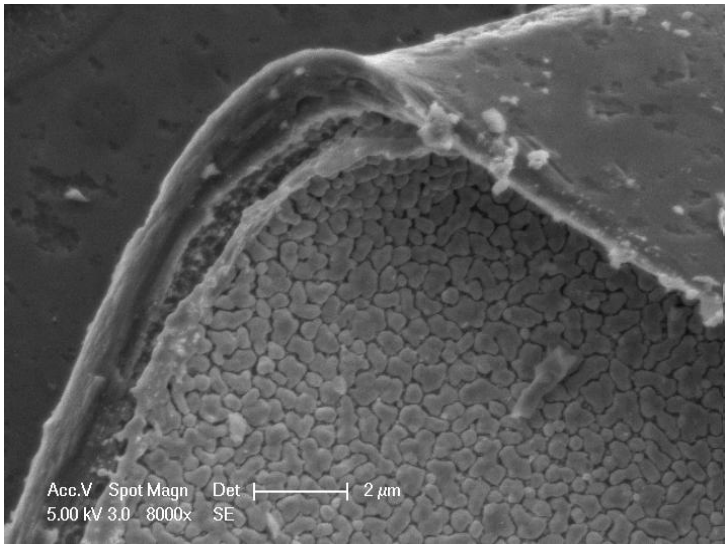


Figure 5- 1: Peeled off and rolled bonding layer which shows two deposited layers of Al and In. Indium grains are also visible on the outer surface.

5.2.3. Intermetallic Compounds Formed in Solder-Bonding Layer

Regarding the choice of material for the bonding layer, difference sequences were considered initially, one of which was Au/In sequence, because of the high melting temperature (1064˚C) and low resistivity of gold. However, this choice was dismissed since studies such as [89], [90], [91] have shown that gold and indium interact and form an alloy of primarily $AuIn_2$ at fairly low temperatures.

Having such a bi-metal compound is not desirable for the solder-bonding layer in this project and thus Au/In layer sequence would not have been a good fit for this application. Figure 5- 2 shows the Au/In alloys that form at different temperatures [89].

In [90] it is found that the diffusion of Au and Ag in In is several orders of magnitude higher than self diffusion rate of In. In [91] the morphology of intermetallic compounds formed during the soldering reaction of liquid In on Au-deposited substrates is studied and it is concluded that two types of $AuIn_2$ compounds form: the continuous wavy crystalline type and the floating island type, and the wettabily of In on an Au-coated surface is calculated.

In an application note from AIM [92], a global supplier of tin-lead and lead-free bonding systems, it is argued that indium-lead solders are superior to tin-lead solders in applications where the solder layer is in contact with gold. The reason is that tin dissolves 18% by weight of gold at moderate temperatures of 225-250˚C, whereas that dissolution is 2-4% for indium. Less dissolution is more desirable because less intermetallics will form and the solder flow on the Au surface will improve. For the case of tin-lead solders, it is argued

that over time tin dissolves gold by solid state diffusion and degrades the electrical contact [92]. However, if indium-lead could not be used for applications that need to be lead-free for environmental concerns, a gold/tin alloy is recommended in either Sn90/Au80 217˚C eutectic or Au80/Sn20 280˚C eutectic forms.

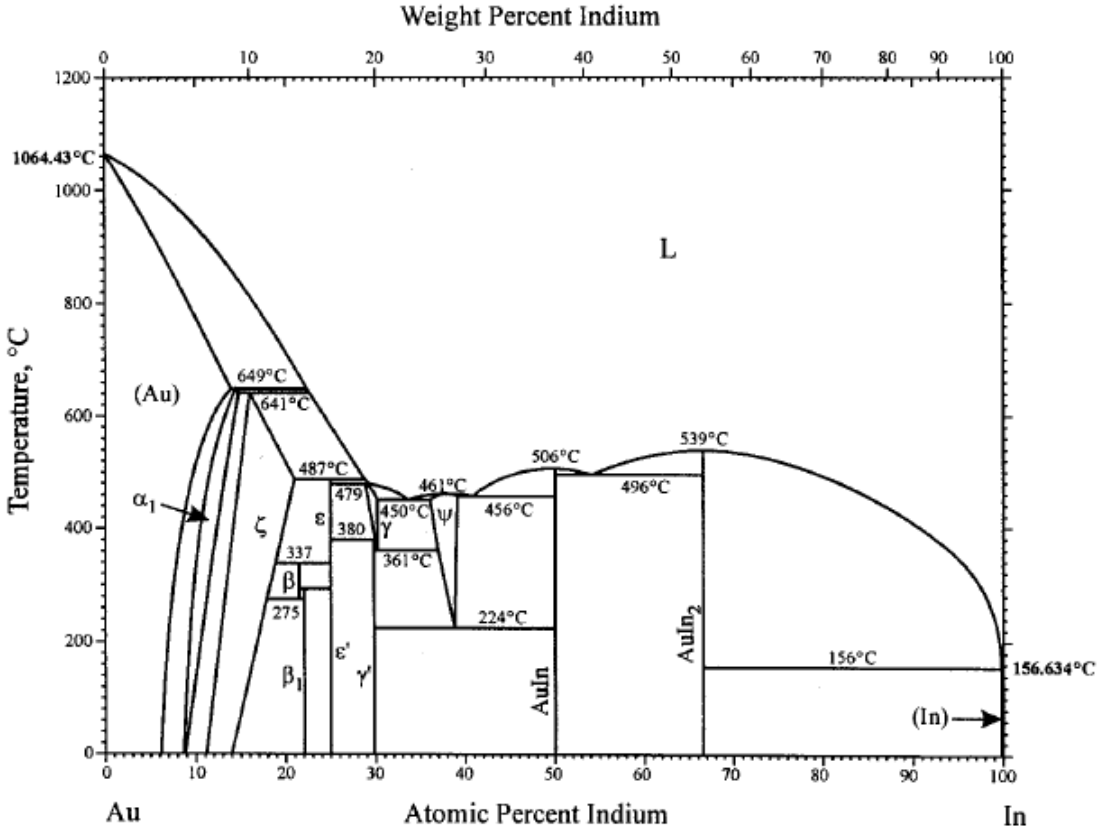


Figure 5- 2: Calculated phase diagram of Au-In binary system [89].

Having dismissed Au as a choice for the support layer in our solder-bonding layer sequence, we looked into the case of Al/In sequence.

In [93] the diffusion of Al in In (as well as Ga) is studied and the diffusion coefficients of Al in In at 620˚C is found to be $D=8.4\times10^{-5}$ cm^2s^{-1}, while in [94] the diffusion of indium in Al is estimated be $D=9.8\times10^{-8}$ cm^2s^{-1} at 626˚C. In [95] in addition to the Al-In-Sn ternary, the Al-In binary is studied in detail and it is shown that this binary is of great interest due to its large miscibility gap[5]. The upper limit for solubility of In in Al is given to be 0.05 atomic percent and the melting point of the eutectic composition is indistinguishable from 156˚C of pure In melting point, indicating very low Al presence in the compound.

[5] Range of compound percentage and temperatures that the two materials do not mix well in liquid phase.

Therefore, since Al does not tend to diffuse in In (and vice versa), the Al/In sequence was a great low temperature choice for the solder-bonding layer to be used for our application of coaxially integrating laser platelets in SiO_2 recesses.

It is worth mentioning that another drawback of the Au/In sequence would have been the high cost of depositing a thick layer of Au and more importantly the problem with patterning it. Since in order to cover the sidewalls of the recesses, the chips are placed at an angle during the bonding layer deposition, lift off is not a viable option. Therefore, another very desirable attractive feature of the Al/In sequence is that it can be patterned in one step and even in one etch, which simplifies the processing.

5.2.4. Deposition

Two methods have been used for the deposition of the Al/In bonding layer. One method used eBeam evaporation of both layers in the EML-MTL facility, while the other was carried out in Prof. Bulovic's lab, in which aluminum was RF sputtered and indium was thermally evaporated[6] due to the material limitations of that lab.

The motivation behind using the second facility was to ensure a low vacuum in the range of 10^{-7} torr, to prevent oxidation of sensitive layers like indium. For the same goal, due to system limitations, the EML eBeam system was put to overnight vacuum to reach a 10^{-6} torr range. Overall, both sets of samples were used in the integration phase.

The finish of thermally evaporated or eBeam deposited Indium is not metal shiny and instead it is non-reflective, appearing almost white especially when it comes into contact with resist developers during the patterning phase.

As discussed at the beginning of this section, another criterion for the bonding layer is to provide sound electrical connectivity from the bottom of wells to the top of substrate. Therefore to ensure this, the samples deposited with eBeam evaporation were positioned at a systematic angle of about 15˚ during deposition so that at least one of the long well sidewalls is continuously coated with the bonding layer[7].

[6] In this case samples were transferred between the two chambers in an interconnected vacuumed line.
[7] Initially we decided to put samples off-center in eBeam deposition chamber in order to cover the sidewalls. However it was observed that the deposited thickness varies a lot in those off-center areas, and thus optimizing the layer thickness would turn out to be non ideally reproducible. Hence, we decided to position the samples at center to have the most consistent layer thickness and at an angle to ensure sidewall coverage.

5.2.5. Patterning of the Bonding Layer

The bonding layer needs to be patterned, since at least one of the facets needs to be clear of any opaque layer to allow coupling of the lasing light from the laser diode to the dielectric waveguide. Experimentation showed that patterning with a thin conventional resist (OCG825:1μm), does not work for this high-aspect-ratio structure (7μm step) and fails to cover and protect the bonding layer on the sidewalls. Figure 5- 3 depicts how the bonding layer on the edges is exposed and attacked in the subsequent etching phase using a thin resist for patterning.

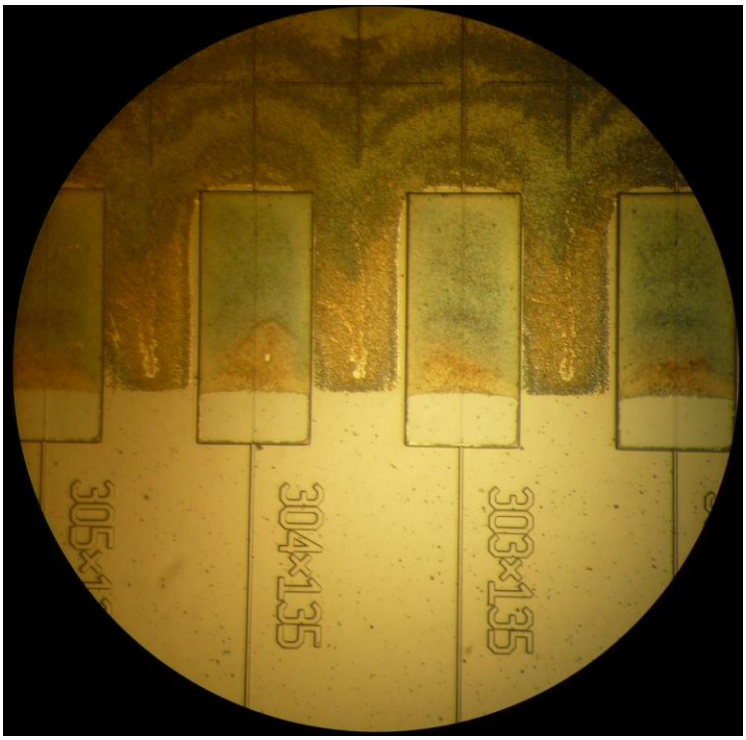


Figure 5- 3: Failure in patterning In on a substrate with wells using thin resist. It can be noticed that along the sidewalls the thin resist has failed to give adequate coverage and the Al/In bonding layer is etched away.

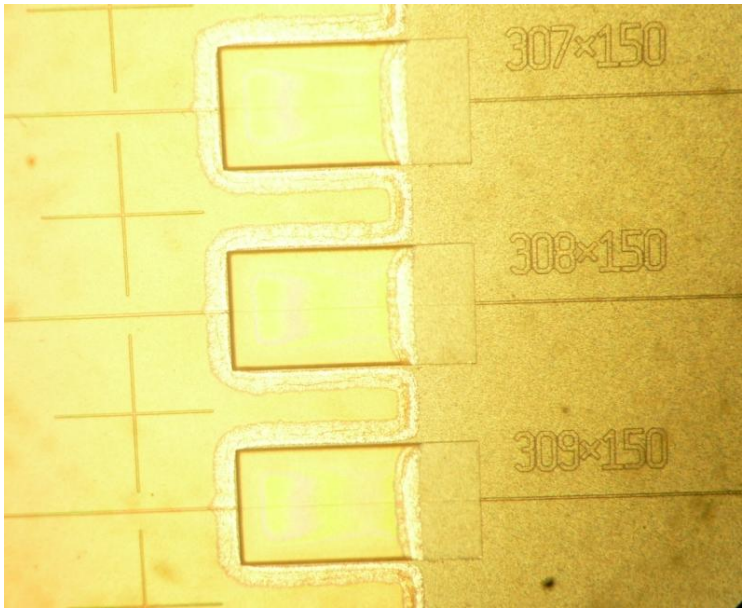
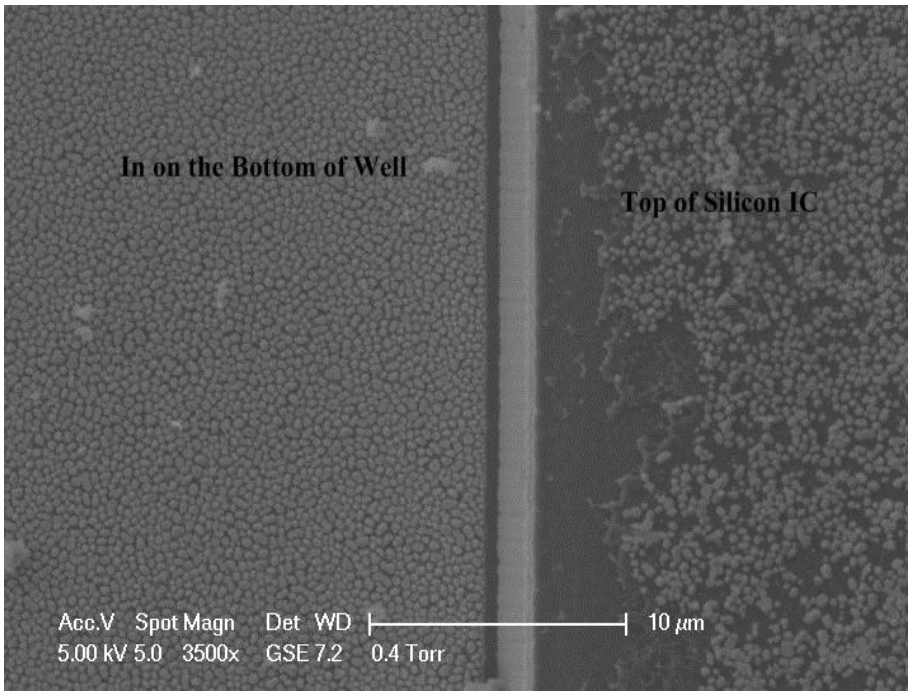


Figure 5- 4: Another image of the Al/In layer patterned with thin resist (OCG825:1µm). Discontinuities on the sidewall edges are noticeable due to the lack of complete coverage with this thin resist.

The SEM images in Figure 5- 5 also confirm what was optically visible in Figure 5- 3 and Figure 5- 4, that on the sidewall edges indium grains are attacked and removed due to the lack of proper coverage by the thin resist.



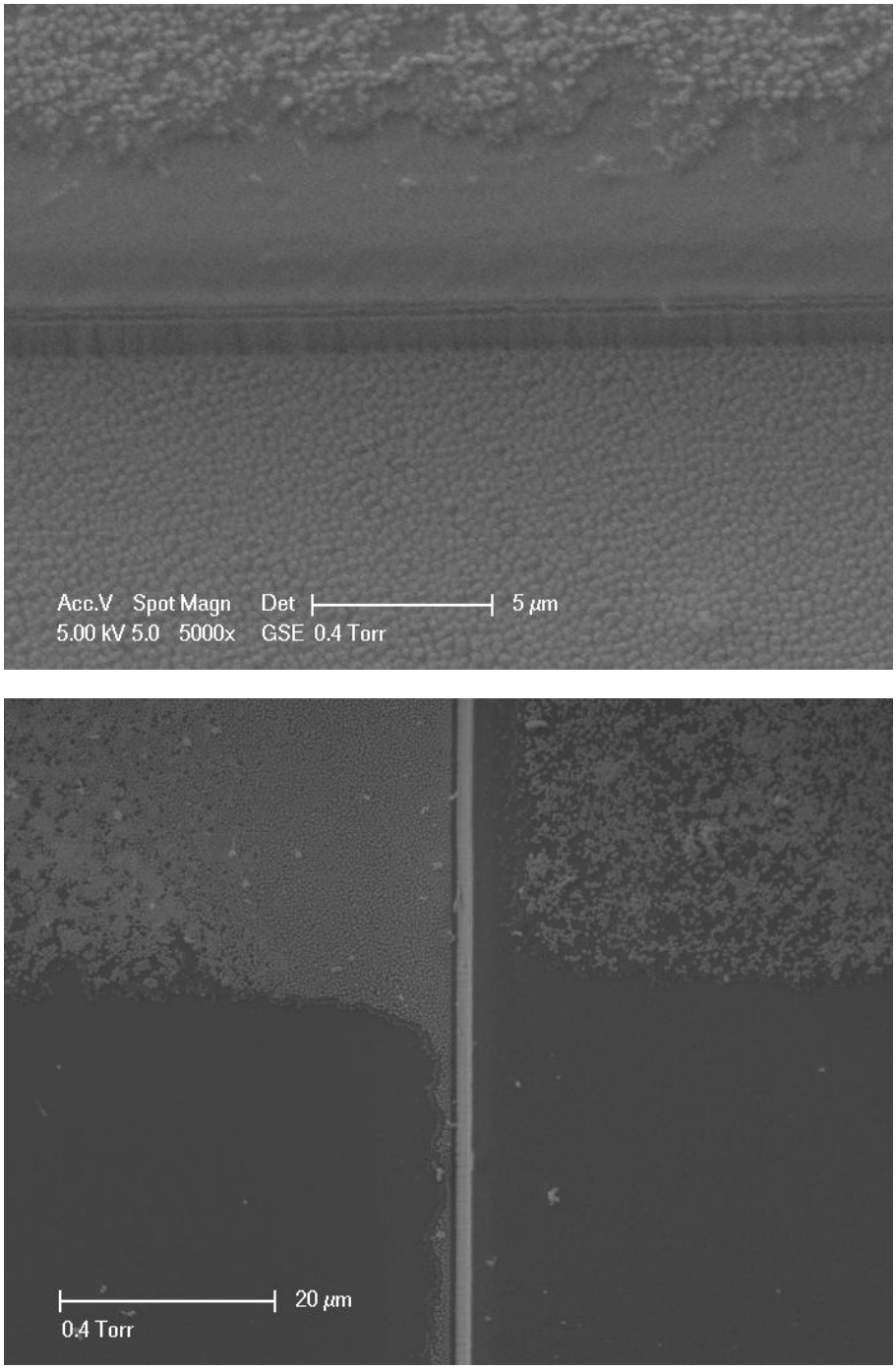


Figure 5- 5: SEM images showing the discontinuity of indium grains at the sidewalls when OCG thin resist was used for patterning.

In order to address the issue faced with thin resist patterning, the thick AZ4620 resist (6-8μm depending on coating rpm) was adopted instead, which solved the aforementioned problems of thin resist's lack of coverage. Figure 5- 6 and Figure 5- 7 show the improved patterning outcome when this thicker resist is used.

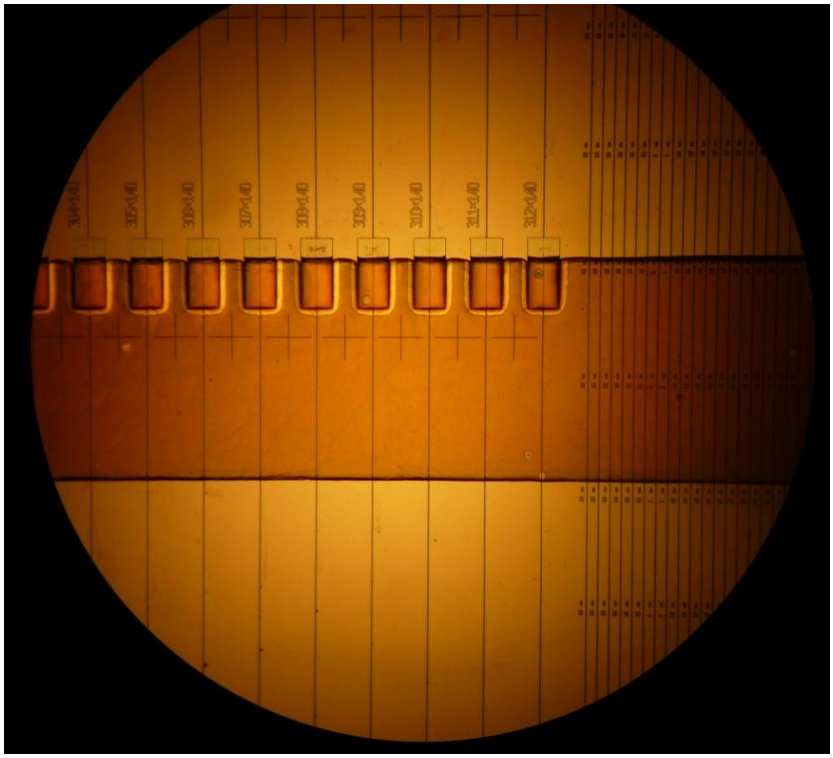


Figure 5- 6: Successful patterning with AZ4620 resist. Here the thick resist covers the deep recess sidewalls very well resulting in a flawless Al/In pattern.

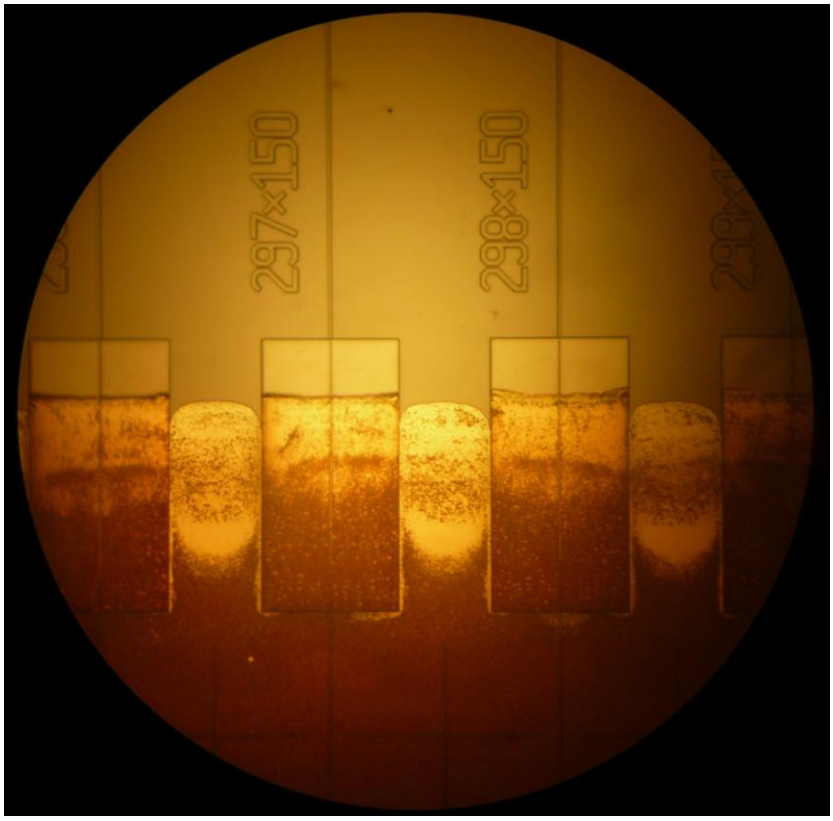


Figure 5- 7: Zoomed in image of Al/In layer patterned with thick resist (AZ4620). With this resist good coverage of the high-aspect ratio recesses step is achieved.

5.2.6. Morphology of the Bonding Layer

During process development, it was noticed that KOH based resist developers attack the surface of indium aggressively (AZ400K for example), and a study was carried out to determine at what stage of the process, the indium surface is attacked the most. OCG developer, Microstrip, acetone, heat and the combined effect of each were compared to a control sample using SEM imaging, and the results are shown in Figure 5- 8, where all the SEMs have the same 5000x magnification.

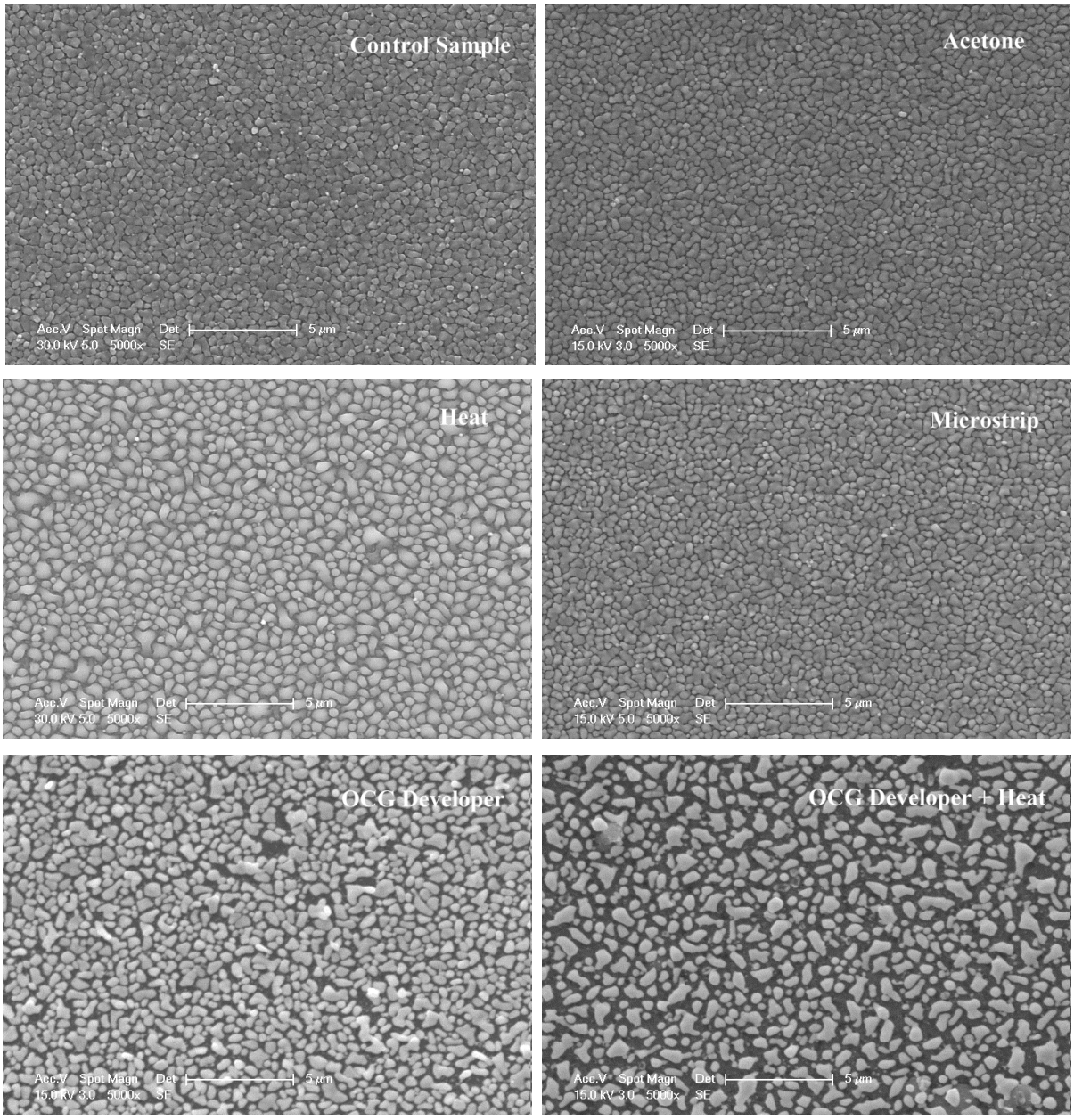


Figure 5- 8: Morphology study of the impact of heat and different solvents on the In surface. All images are taken at the same magnification of 5000x.

It was concluded that KOH based developers cause the most of the harm by attacking indium grains, which get even sparser during the subsequent heat treatment in the bonding phase. Therefore, a Metal Ion Free (MIF) developer such as AZ405MIF was adopted instead.

After the resist was patterned, the Al/In layer was etched and patterned with standard Al-etch etchant[8] (Type-A from Transene, with an etch rate of 100Å/s at 50˚C). One advantage of the Al/In layer sequence is that both layers can be easily etched in a single step using this etchant, which will naturally stop at the underlying SiO_2 layer.

The SEM images of Figure 5- 9 and Figure 5- 10 show a laser platelet bonded on a patterned flat bed of sparsed Al/In layer when KOH based developer was used (which attack the Al/In layer as discussed earlier). The second SEM is a zoomed in image at the micro-cleaved facet of this laser platelet and it shows the very smooth crystalline facets resulted from the micro-cleaving technique used for cavity definition of these platelets.

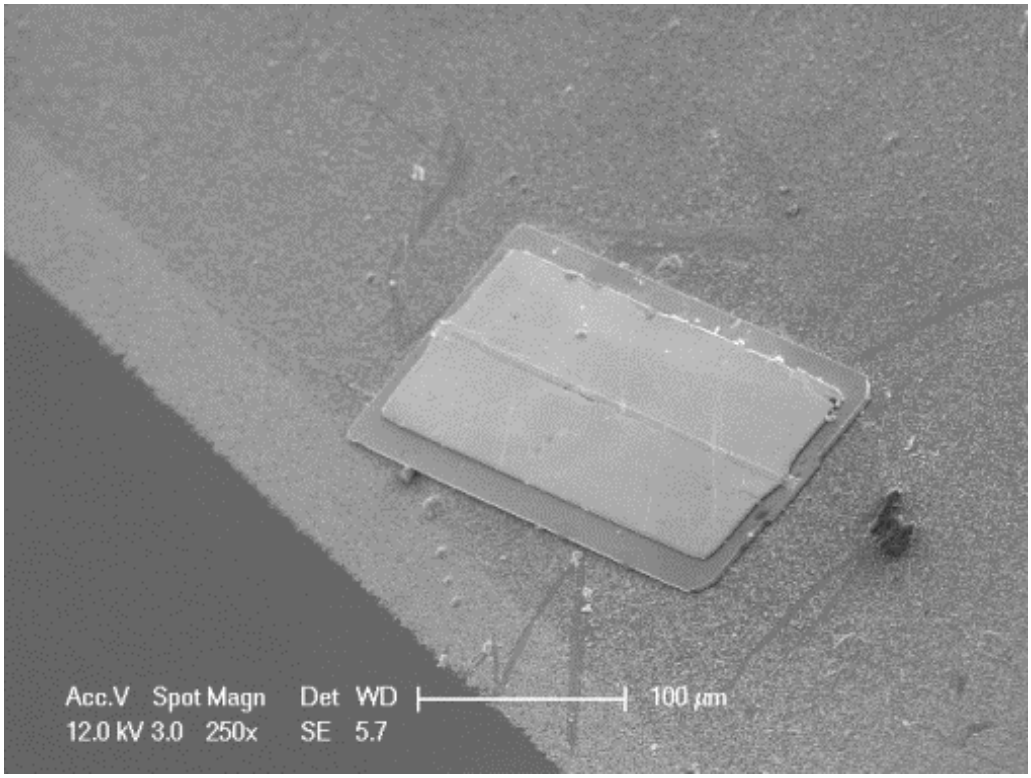


Figure 5- 9: Laser platelet bonded on a strip of Al/In bonding layer on a flat substrate. In surface is sparsed due to the effect of initially used aggressive solvents and heat treatment.

[8] Aluminum Etchant Type A contains 80% Phosphoric Acid, 5% Nitric Acid, 5% Acetic Acid, and 10% Distilled Water. It is an industry standard for Aluminum etching on Si devices, and does not attack SiO_2 or Si_3N_4. [110]

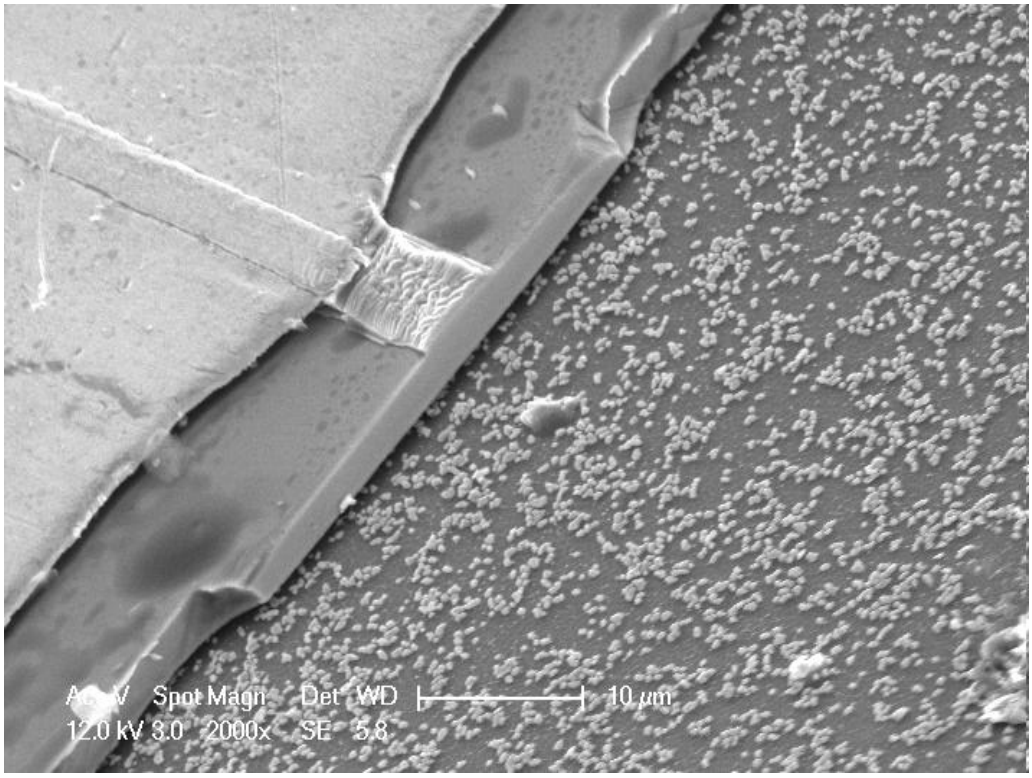


Figure 5- 10: Zoomed in SEM image of the previous laser platelet bonded on Al/In layer. The highly smooth facet of the laser platelet is the result of micro-cleaving, which induces cleaving along a crystalline facet.

5.2.7. Other Concerns in Patterning Al/In with AZ4620

Since there are hollow steps of about 7µm of recesses on the wafer surface, the Al/In does not pattern as smoothly as it would on a flat substrate using the thick AZ4620 resist. The problem is that the surface tension of the resist and probably its interface with indium, make it pull back from the surface, leaving a curved pattern as one can see in Figure 5- 7. Although this curving was tolerable for the straight stripe of bonding layer pattern, later on when we liked to remove the SiON waveguide at one end in order to measure the coupling loss with a single laser[9], it turned out to be a major issue, severely rounding the square patterns, as can be seen in Figure 5- 11. The wrinkles that can be seen at the bottom of the wells in a zoomed out image of the patterned resist on these Al/In coated wells, shown in Figure 5- 12, strengthens this theory of resist pull-back during patterning.

[9] The motivation and mask pattern for this goal will be discussed in more details in Chapter 6.

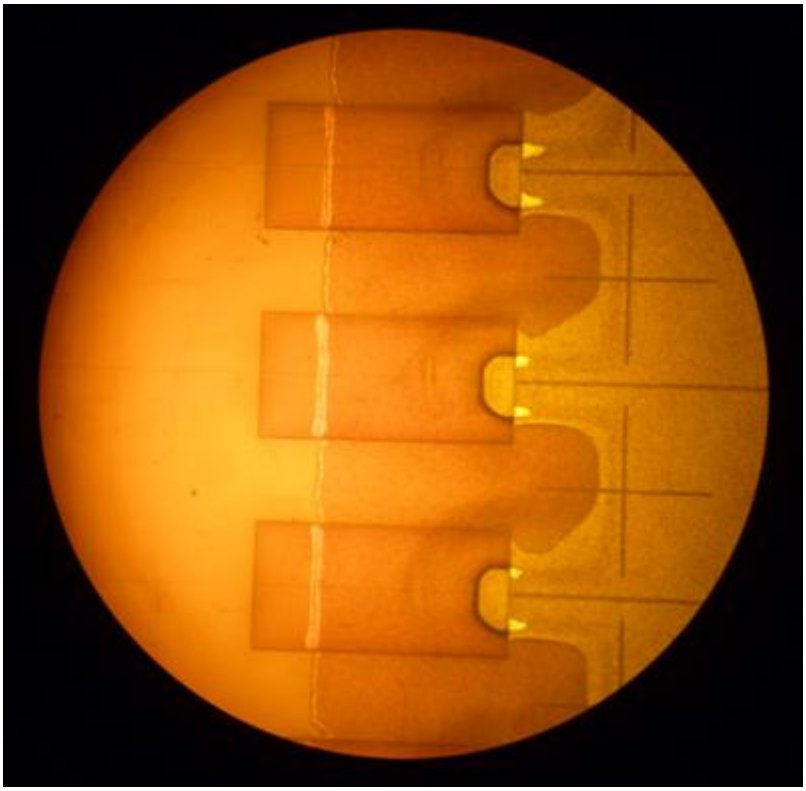


Figure 5- 11: Failure in patterning AZ4620 on an In coated sample. Square patterns are rounded due to the pull back of resist during development.

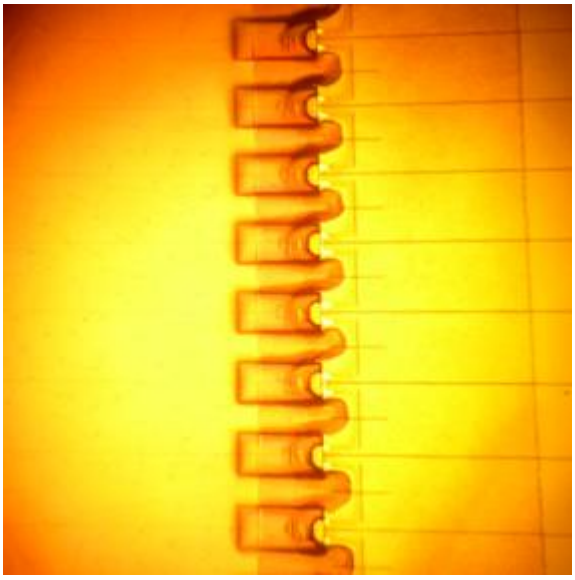


Figure 5- 12: Zoomed out image of Figure 5- 11, showing the resist's wrinkles at the bottom of wells post-development, which strengthens the assumption that the development failure is due to the resist's surface tension on an indium coated surface.

For comparison, it might be helpful to show how the resist patterns on the same non-planar recess surface with the same recipe when no Al/In coat is present. Figure 5- 13 shows the same pattern on such a bare recess surface, in which the squares in the pattern have turned

out quite sharp, as shown in Figure 5- 11, and without any rounding effects that occurred patterning the resist on an Al/In coated surface.

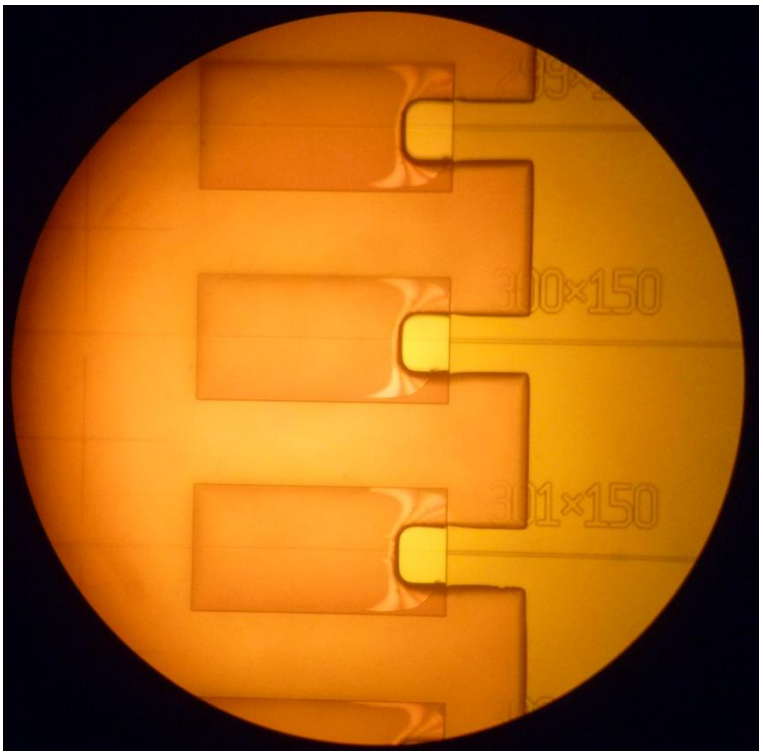


Figure 5- 13: AZ4620 patterning had no issues when no indium coating was present on the sample. Thus the issue shown in Figure 5- 11 is specific to the interaction of In and AZ4620.

Since we speculated that the rounding of AZ4620 patterns on an In coated non-planar surface was due to the surface tension and pull-back of the resist, one possible solution is to make the resist more firm during the bake step. In fact, this solution proved to work very well when the resist pre-bake time was increased by 50%-100% from 5min to 8-10min. Figure 5-14 shows a sharp rectangular patterned resist resulted from this modified recipe, which is further noticeable in the zoomed view of Figure 5- 15. Therefore, the modified recipe with longer bakes was adopted whenever a pattern was to be developed on an In coated surface using AZ4620.

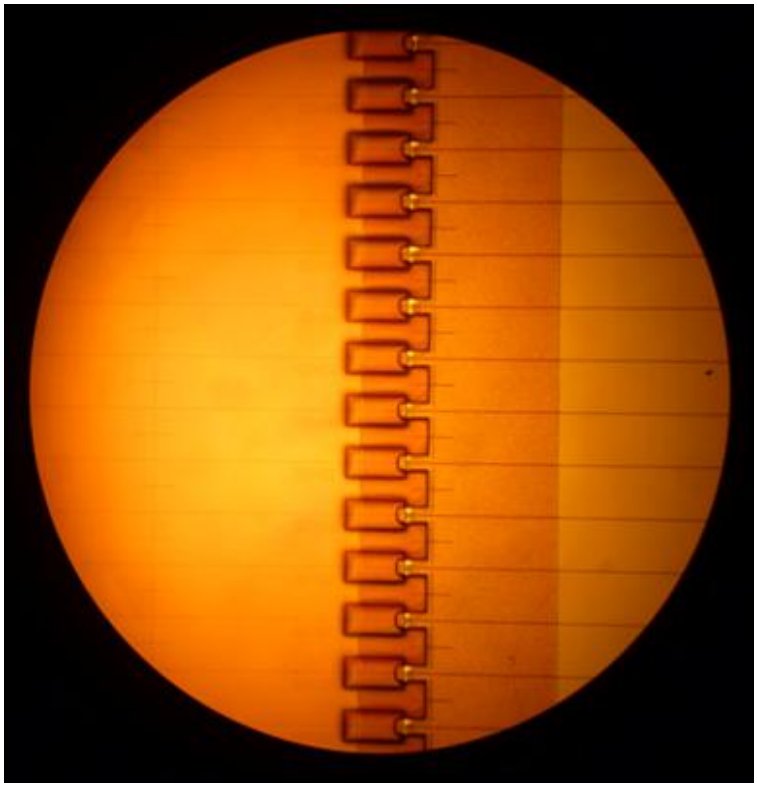


Figure 5- 14: Successful AZ4620 patterning on an indium coated surface, with longer bakes that helped solidify the resist more and prevent it from rounding and pull back during the development.

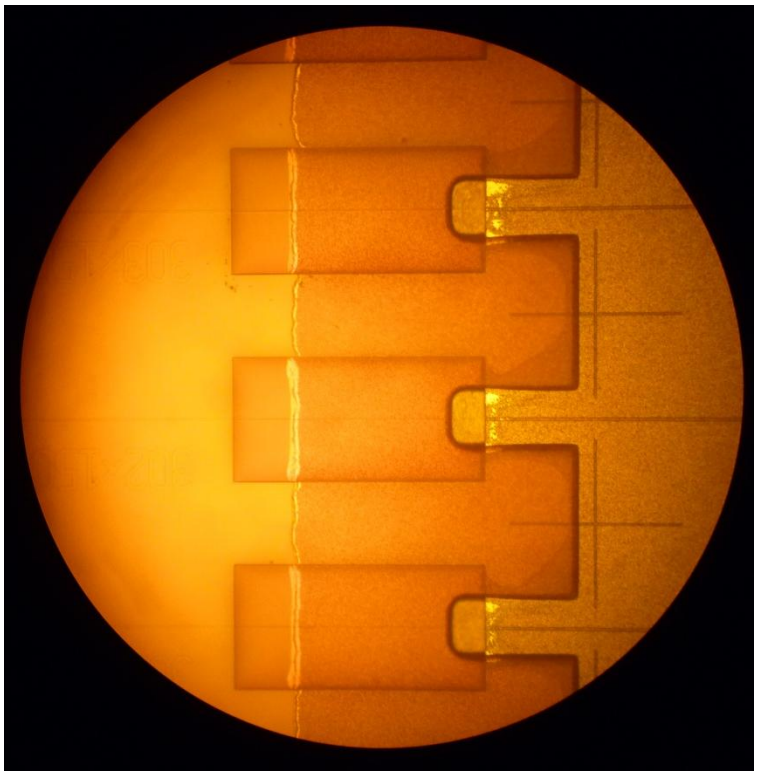


Figure 5- 15: Zoomed in image of Figure 5- 14, showing that the rounding problem of Figure 5- 11 is addressed by solidifying the resist through longer bakes.

5.3. Substrate Cleaving and Facet Polishing

Once the bonding layer is patterned and etched, the substrate needs to be cleaved through the output waveguides (since their pattern had been such that they terminate before the larger die edge), followed by polishing of the output facets.

In order to protect the sensitive Al/In on the front side during these two steps, a coat of thick AZ4620 resist is applied to the substrate front side and is pre-baked. Cleaving of the dies is carried out by scribing through the backside, so that the frontside dielectric facets turn out smoother[10].

Since the thick dielectric stack (6-7µm) is amorphous, the cleaved facet is always rough, especially in the dielectric waveguide area. Therefore, polishing is essential to minimize scattering loss from the outgoing waveguide facet.

Polishing of the cleaved die facets has been carried out manually, by pressing the sample against a rotating surface with 1µm grit, with low rpm and constant flow of DI water. Finer grid polishes[11] are expected to give smoother facets and less scattering losses from the outgoing waveguides.

After the polishing is done, samples are cleaned with a sequence of isopropanol, acetone and DI water, making the substrates ready to receive the laser diode platelets with the pick and place assembly step, details about which will be discussed in the next section.

5.4. Assembly Process

As the second step of the integration process, the laser platelets need to be placed in the recesses that are etched into the SiO_2 stack deposited on the Si substrate. In this pick and place assembly phase, a vacuumed pipette is used to pick up each laser one-by-one and place them in the wells. Figure 5- 16 shows the pick and place assembly setup as well as a zoomed view of the pipette. As can be seen, a XYZ micro-positioner helps in maneuvering the

[10] Aggressive pressure from scribing on the frontside, damages the dielectric waveguides, as well as making a rougher facet due to the amorphous layer of dielectric seeing the scribe first. Instead when scribing from the backside, Si wafer ideally cleaves along a crystalline plane resulting in a smoother facet. Nevertheless, waveguide stack facet is always much rougher than the underlying Si substrate no matter what method is used for cleaving the dies.

[11] In the basic polisher machine we had access to, polishing with grits finer that 1µm required applying a Alumina abrasive liquid on a rotating fine cloth, with which the initial attempts to polish the substrate facets were not as successful as the straightforward 1µm polishing grit. Nevertheless, the polishing process is an industry standard and through using a more advanced polishing system, the problem faced here can easily be addressed and smooth finely polished facets can be achieved.

pipette. Also the sample sits on a heavy chuck moving on a thin layer of greased surface, therefore it also can be moved smoothly and easily by the assembler. The micro-pipettes were made to have a 45˚ beveled tip so that they can land flat on the laser platelet surface. The other end of the pipettes is connected to a vacuum pump through a valve which is opened by the assembler when the pipette is ready to pick up a platelet, and is closed to let the laser pill rest in its final position in the recess if the fit and alignment is desirable. Once the lasers are well positioned in the wells, care must be taken in transferring the die to the bonding setup. Static electricity is a hazard in this process and therefore plastic Petri dishes should be strictly avoided, as static charge built-up on them attracts the light laser platelets to the sidewalls of the dish, making the careful assembly effort in vain. Fortunately, by using glass Petri dishes instead, this issue is addressed very well.

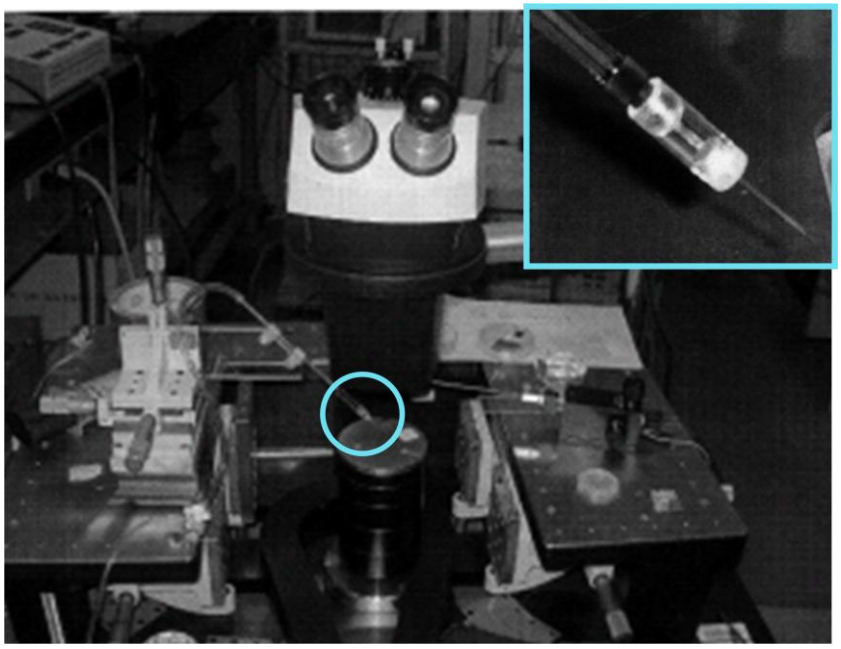


Figure 5- 16: Vacuum assisted pick & place assembly setup. The micro-pipette that picks up the laser platelets with an applied vacuum is shown in the inset.

It is worth noting that picking up the lasers and placing them in wells involves a certain amount of delicacy. During the development of the assembly process, it was noticed that lasers were difficult to lift up, and it was quite challenging to make the pick up phase work. One important contributor to this problem was the Teflon carrier surface that lasers were initially sitting on. Experiments revealed that the electrostatic charge buildup between the laser platelet and the Teflon surface was too high for the vacuum pipette to be able to overcome the electrostatic attraction and lift the pill. To address this, adding humidity to the

operating chamber was tried to enhance electrostatic discharge of the components. We found that a better vacuum pump and especially a larger pipette diameter were needed so that the upward force from the vacuumed area of the laser top, can overcome the downward force of built-up electrostatic attraction[12].

Furthermore, from the TriboElectric data[13] shown in Table 5- 1, it can be seen that the charge affinity of paper is 1/19th of Teflon. In the last column, the strength and type of the charge accumulated on the insulator when rubbed against a metal is also given. For paper, the electrostatic charge buildup is weak, whereas for Teflon it is strong and the same sign (normal) as the usual negative charge on Teflon due to the strongly electronegative nature of surface fluorine atoms. Therefore, from the information in Table 5- 1, it can be concluded that if the Teflon substrate is replaced by paper, electrostatic attraction between the laser platelet and the carrier will be much lower and thus vacuum pipettes with the sizes on hand (e.g. 35µm in diameter) can lift the laser platelets. When this change was made in the assembly process, it was observed that the platelets were much more easily lifted by the vacuumed pipette.

Insulator	Charge Affinity [nC/J]	Metal Effect
Paper	+10	- Weak
Teflon	-190	-Normal

Table 5- 1: TriboElectric table with charge affinities of paper and Teflon.

In terms of other difficulties in assembly, often times when a laser pill was sitting face down on the carrier, it had been challenging to turn it over. One can try to lift one edge up by inserting the pipette under the pill and lifting it, but that effort often ends up in tossing the laser to somewhere around on the carrier (and luckily one could hope on the front side is now facing up). Of course such difficulties like turning over pills or lifting them can be well addressed with a more sophisticated industrial system and the outcome will be a much faster and more robust process.

Overall in the assembly phase, care and expertise were administered to ensure the best fit of lasers in recesses and the highest horizontal alignments of the two waveguides. These can also be well optimized in an automated process, which optically measures the laser

[12] Calculations have shown that the laser platelet weight is negligible compared to the electrostatic attraction to the carrier substrate.
[13] TriboElectric series [111] are used to determine the charge buildup when two different materials are in contact or rubbed against each other [112].

dimensions and picks the best fit to each recess, as well as easily pushes lasers to one edge of the well, for highest coupling to the outgoing waveguide.

5.5. Bonding Step

Following the assembly, the bonding step takes place in an in-house-developed pressured bonding chamber [96] in a forming gas environment at 220˚C for 7min.

Figure 5- 17 shows a schematic and image of this bonding system. The setup has an outer chamber in which N_2 will flow to pressurize the membrane pushing it down and pressing the lasers to the bonding layer[14], and an inner chamber in which a graphite heating element and sample reside. The forming gas (H_2:20%, N_2:80%) flow[15] in the inner chamber prevents oxidation of the metal layers during the heating cycle.

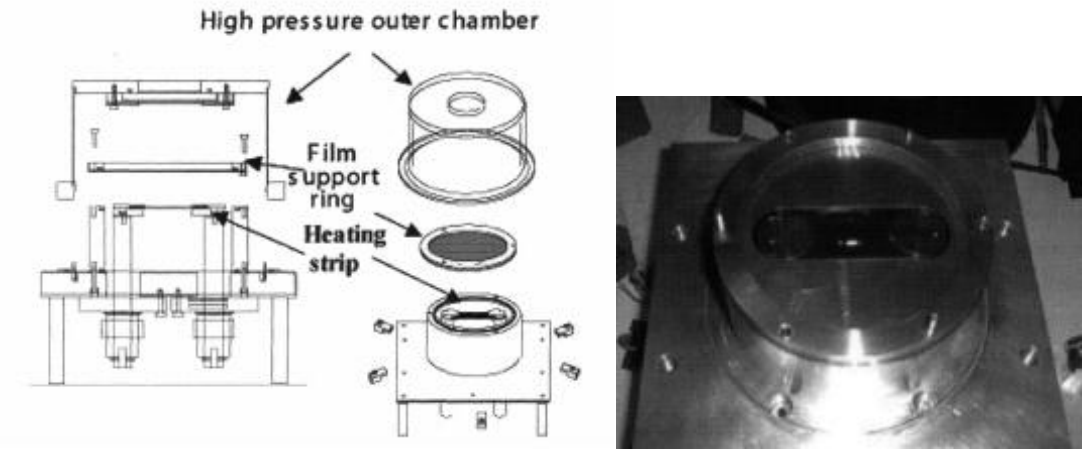


Figure 5- 17: Bonding setup. The sample sits on the heating stripe in the inner chamber through which a flow of forming gas is applied to avoid the oxidation of In throughout the bonding phase. The outer chamber is pressurized forcing the membrane down which will apply pressure on the laser platelets against the bonding layer to form a strong bond during the bonding phase above melting point of In.

One concern during the bonding phase is the presence of oxygen in the chamber, which must be avoided to prevent indium oxidation when it is melted. Another concern is that since the laser pills can stick to the membrane[16] and get dislocated from their recess, care must be taken to keep the membrane pressured down at all times and not let it move up and down during the heating/cooling of bonding sequence. This latter concern was a limitation

[14] Initial experiments revealed that temperature sequence on its own does not make a solid bond and the presence of pressure is vital in this bonding phase.
[15] Forming gas outlet of the inner chamber goes to a bubbler filled with vacuum pump oil, to avoid the back flow of ambient oxygen into chamber.
[16] Although the lasers mounted in wells have less tendency to be lifted by the bonding chamber membrane compared to lasers that were to be bonded on flat Al/In surfaces.

that prevented us from pumping down the chamber to remove the oxygen content before flowing in the forming gas. In such a sequence the membrane would have come down with vacuum and stick to the lasers, and with the inflow of forming gas the membrane would lift, picking up the lasers with itself and dislocating them. Instead, the inner chamber was purged for a long time before the outer chamber was pressurized.

Keeping all these in mind the following sequence was selected for the bonding step:

1. Mount the sample and tightly close both the inner and outer chambers.
2. Purge the inner chamber with forming gas for 45min, to remove ambient oxygen.
3. Pressure down the membrane with 20psi of N_2 in outer chamber.
4. Run the heating sequence, which aside from the ramp up/down steps, has a 7min hold time at 220˚C in which the indium melts and the bonding takes place.
5. Let the system cool down to about 40˚C. (To make sure In has solidified in the forming gas environment and the system is ready to be opened.)
6. Close nitrogen inflow to the outer chamber.
7. Close forming gas inflow to the inner chamber.
8. Slowly open vent of outer chamber.
9. Open both chambers and take out the bonded sample.

By following this process and having optimized the bonding pressure to ensure the mechanical strength of the bond (without breaking the graphite heating element), the bonding phase is successful if the lasers are well placed in the recesses and were not dislocated by or attached to the membrane. At this stage the integrated system is ready for measurement and characterization.

5.6. Optimization of Bonding Layer Thickness

As discussed earlier, it is of paramount importance to find an optimum thickness for the Al/In bonding layer, to ensure that the dielectric waveguide core and the laser active region are vertically well aligned so that coupling between the two is maximized, as depicted in Figure 5- 18.

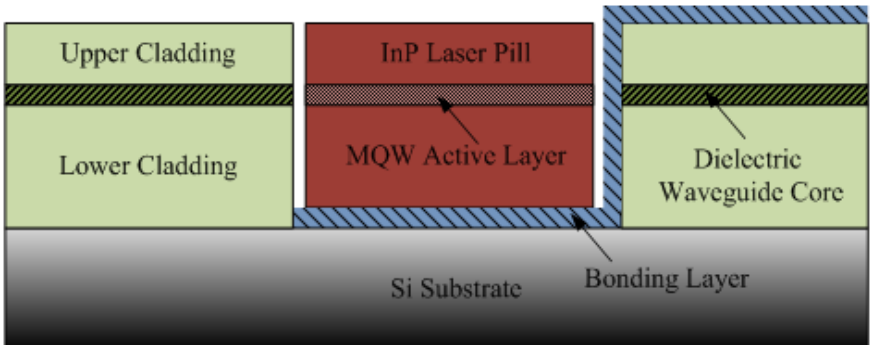


Figure 5- 18: Schematic showing the importance of the height of Al/In solder-bonding layer in ensuring the best vertical alignment of laser active region and SiON core of dielectric waveguide.

Therefore, two important factors should be known with a good accuracy: a) the vertical position of the laser active region from the back of the platelet (y_L), and b) vertical position of dielectric core from the bottom of the well (y_W). Their difference (hopefully negative) gives the required bonding layer thickness to bring both to the same height.

The height of the active layer is known from the reliable material description given by the wafer manufacturer[17] and knowing that the deposited backside n-contact thickness is 0.37µm. Table 5- 2 lists the different layers of the laser, and shows that the mid-point of the active region is located at y_L=3.605µm above the bottom of the laser platelet. (Note that the InP substrate is etched away in the fabrication of individual micro-cleaved laser platelets.)

Layer #	Material Type	Doping	Function	Thickness
9	$In_{(1-x)}\ Ga_x\ As$	P^+	Ohmic Contact	200nm
8	InP	P	Ridge	1.5µm
7	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	P	Etch Stop	7nm
6	InP	P	Upper Cladding	200nm
5	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Upper Core	110nm
4	$4 \times In_{(1-x)}\ Ga_x\ As$	U	QW	24nm total
	$3 \times In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Barriers	27nm total
3	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Lower Core	110nm
2	InP	N	Lower Cladding	2.8µm
1	Thinned $In_{(1-x)}\ Ga_x\ As$	N^+	Backside Etch Stop	300nm
0	Backside metallization	-	n-contact	370nm

Table 5- 2: InGaAs/InP laser platelet layer structure.

[17] Landmark Optoelectronics

However, finding the position of the waveguide core, i.e. factor y_W described earlier, turns out to be more difficult than simply adding the lower cladding height to half of the core thickness. For instance ideally for the case of batch B6-4, lower cladding was supposed to be 3.3µm which added to half of the core expected thickness of 0.7µm, will yield y_W=3.3+0.35= 3.65µm. Subtracting y_L from y_W, results in 45nm of Al/In bonding layer thickness to reach the vertical alignment of the cores. However, as it will be discussed in detail soon, a careful study of the deposited waveguide/recess system showed that there are more elements into the story which were initially not considered at the time of the fabrication of these structures. Therefore the required Al/In layer thickness is actually 975nm instead of 45nm that the naive approach above suggests. The following section describes how these subtleties were identified and the dimensions characterized.

5.6.1. Determining Actual Dimensions of Dielectric Stack/Recesses

Dektak profilometry gave us the first indication that the reported/expected dimensions in the preparation of dielectric waveguide/recess [59] were not precise. In fact, the discrepancies were of significant value. Table 5- 3 shows expected and actual well depth measurements for different batches (that differ in lower cladding height as listed in the table). The expected upper cladding and core heights were 3µm and 0.7µm for all batches.

Batch #	Expected Lower Cladding (µm)	Expected Well Height (µm)	Averaged Dektak Well Measurement (µm)
B6-13	4.2	7.2	6.86
B6-10	3.9	6.9	6.46
B6-7	3.6	6.6	6.52
B6-4	3.3	6.3	6.48
B6-2	3	6	7.29
B6-1	3	6	6.19

Table 5- 3: Expected and actual recess heights for different fabricated batches.

With such a discrepancy, which would have hampered a good vertical alignment of the guides, further investigation to determine the actual dimensions was essential in order to get an accurate estimate for the required bonding layer thickness.

For this analysis, first the entire waveguide stack was etched away though HF wet-etching, where it was noticed that the recess patterns had been etched into the Si substrate wafer as well. This new piece of information was an important factor that should have been included in the well height estimation. Table 5- 4 shows the amount of Si-Over-Etch per

batch #. Note that the over-etching is on the order of 1-2µm which is quite significant for the total well height of 6 to 7µm.

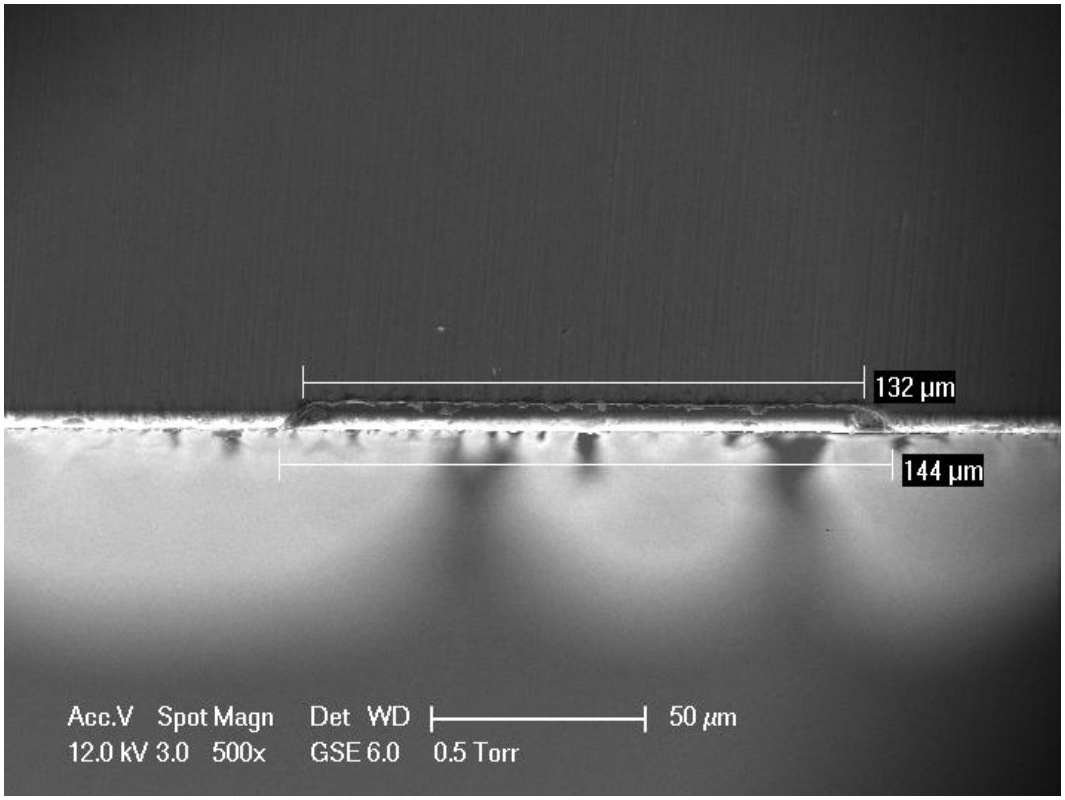
Batch #	Si-Over-Etch
B6-13	1.46
B6-10	1.26
B6-7	1.3
B6-4	1.3
B6-2	n/a
B6-1	n/a

Table 5- 4: Over-etch into the Si substrate occurred at the end of recess etching phase.

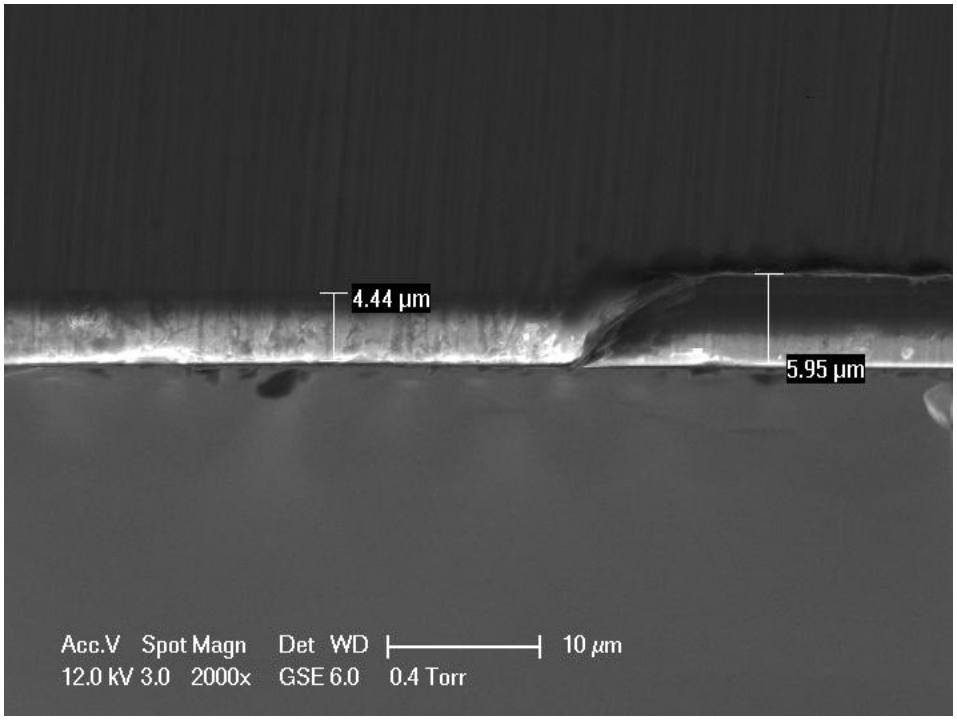
One might suspect that this over-etch could have happened in the deep recess etching RIE phase (with the gas mixture of CHF_3:CF_4 3:1). However that would have been unlikely since a poly-silicon hard mask was used and the chemistry has a low Si etch rate and high selectivity[18]. Instead, most probably, this recess Si-over-etch has happened during the RIE removal of the 1.5µm Poly-Si hardmask (using Cl_2:HBR_3 3:1) which served as a mask in the recess etching phase. In fact the amount of Si-over-etch concluded in Table 5- 4 is very much consistent with the thickness of that poly-silicon hardmask, making this hypothesis the more probable one.

The SEM images in Figure 5- 19 have been taken from a cross-section of a polished sample cleaved through a recess, and clearly show the Si-over-etch, since Si and SiO_2 can be differentiated visually in these SEMs. (The wells are upside down in both images.)

[18] Si:SiO_2 selectivity with this etch chemistry is expected to be about 1:6.



(a)



(b)

Figure 5- 19: SEM images of a cross section of a 145µm wide recess (a), and the zoomed view of it at the left edge (b). The sample was positioned upside down. The different shades for SiO_2 stack and Si substrate are observable, and confirm over etching inside the Si substrate.

Also note that although care was taken to select a tailored etch chemistry for the recess etch step to ensure vertical sidewalls, the sidewalls etched in the Si are very much slanted, as seen in Figure 5- 19. This could have been a concern in integration if the lasers were to sit directly in the bottom of the wells, as the width of recesses gives a tight fitting to the laser platelets. However, since the Al/In layer is deposited on the bottom of the wells, it removes this concern. For instance for batch B6-4, the required Al/In thickness is about 1µm and Si-Over-Etch is 1.3µm, therefore the bonding layer masks most of curved sidewalls and thus it is not an issue for the well-sitting of the lasers in these recesses[19].

Going back to the original question of how to optimize the Al/In layer thickness, and the discrepancies observed from the expected to actual dimensions, it was noticed that including the Si-Over-Etch factor is still not sufficient to make the equations consistent and there must be other factors in place as well. One possibility was that in defining the SiON core, the lower cladding SiO_2 got over etched and thus the total height of the stack is less than expected. The schematic shown in Figure 5- 20 illustrates these factors that play a role in getting the best vertical alignment of guides.

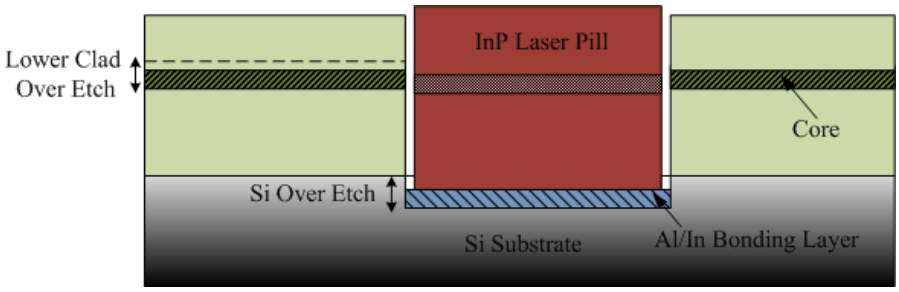


Figure 5- 20: Schematic depicting the two additional factors of over-etch into Si substrate and SiO_2 lower cladding over-etch during the formation of SiON core.

Therefore, the next goal was to determine the amount of over etch of the lower cladding that occurred during defining SiON core. SEM imaging of cross sections seemed an option, however since the refractive index of SiON core (n=1.6) and SiO_2 claddings (n=1.46) are quite close in value, the normal ESEM (environmental SEM (with H_2O low pressure)

[19] In fact another concern that the bonding layer addresses very well is the issue with bumps in the middle of the bottom of recesses (left from the increased height of the waveguide passing through the middle of well, and when RIE etched, still a trace of it is left behind.) These bumps have been measured to be about 700nm in height. Should the lasers sit directly on the bottom of well, the nonlinearity due to these bump would have been a serious issue. However, now the Al/In layer covers most of that bump, making the resulting bump height of about 100nm.

used for non-conductive samples), was not giving a differentiation between core and cladding layers in the cross sectional image. Figure 5- 21 shows this lack of differentiation in the dielectric stack layers with normal SEM.

To solve this challenge, Back-Scattered ESEM was tried and provided a good differentiation between different dielectric layers, if the right brightness/contrast setting was used along with a relatively high voltage (compared to voltages used with normal GSE detector).

Figure 5- 22 shows Back-Scattered ESEM image taken from the cross section of the front side of a sample in which the SiON core is nicely differentiated visually from the sandwiching SiO_2 cladding layers.

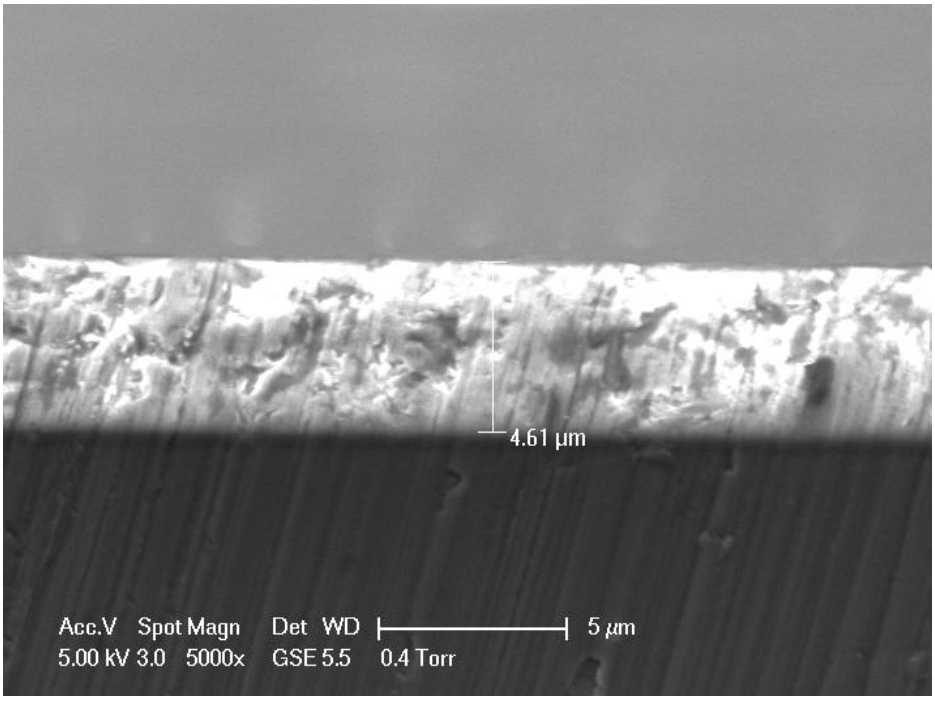


Figure 5- 21: SEM image taken from the cross section of the front side of a substrate. Note that SiON core and SiO_2 claddings are not distinguishable due to their small refractive index difference.

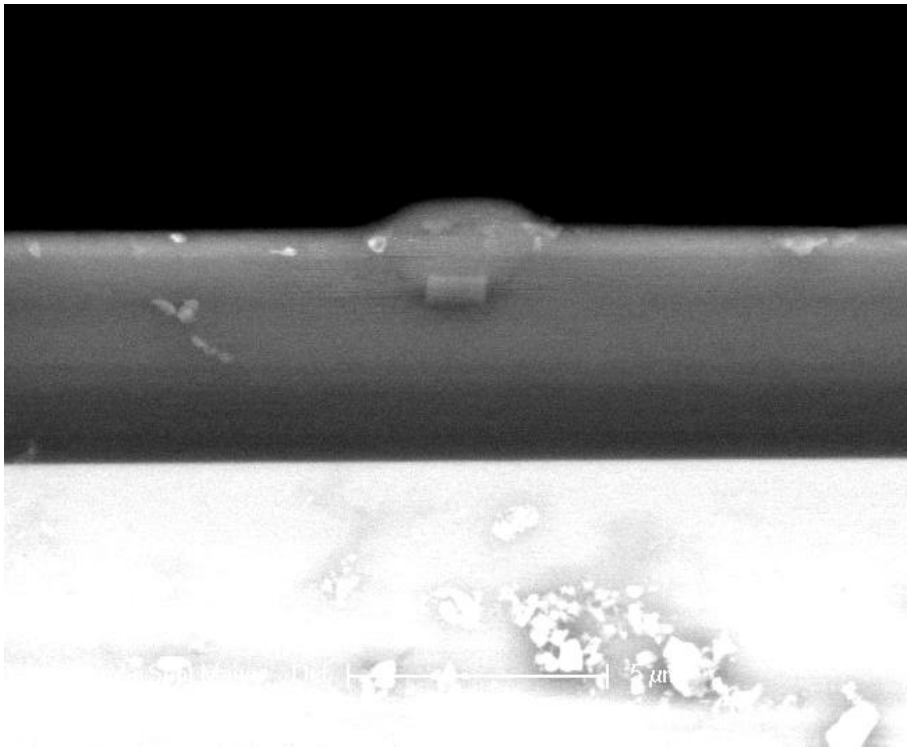


Figure 5- 22: Back-Scattered ESEM image of the cross section of the wafer front side. SiON core is noticeable being embedded in SiO_2 claddings all fabricated on a Si wafer.

Another very helpful and important factor that made the calculations feasible was the fact that in order to cancel the stress on the Si wafer from the deposited thick dielectric stack, the same exact layer sequence deposited on the front side of wafer, was also deposited on the backside as well. We made the assumption that since the same recipe and durations were used for the front and backside depositions when these waveguides were fabricated by E. Barkley, the layers have the same thickness and the backside can be used as a reference to find the unknowns of the front side layers. The Back-Scattered ESEM image in Figure 5- 23 shows the layer differentiation of lower clad, core, and upper cladding on the backside of wafer for a sample from batch B6-13. Note that the lower cladding on the backside (which had no core defining step and thus was safe from any over-etching) is about 4.2μm as expected for this batch. Also note that the core height is 0.5μm rather than 0.7μm that was reported in [59].

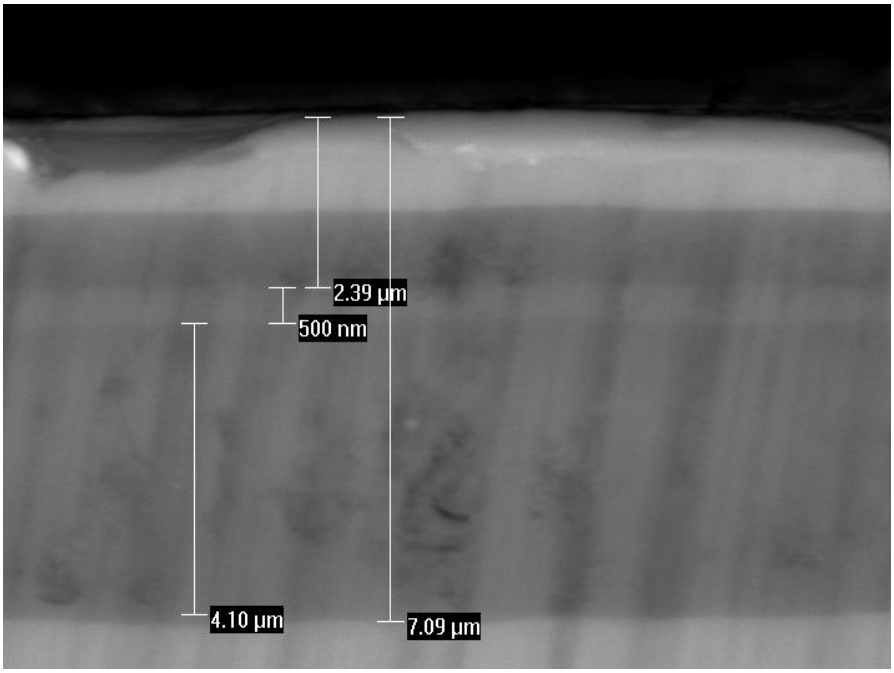


Figure 5- 23: Measurement of core and claddings layer thicknesses at the cross section of the backside of batch B6-13 wafer (note that core is not patterned here). This image is taken with a Back-Scattered ESEM detector, which makes it possible to differentiate between layers with close refractive indices.

By performing the same measurements on the front side of the wafer, one can determine the lower-cladding over-etch for each batch. The image in Figure 5- 24 shows the front side dimensions of a sample from batch B6-4.

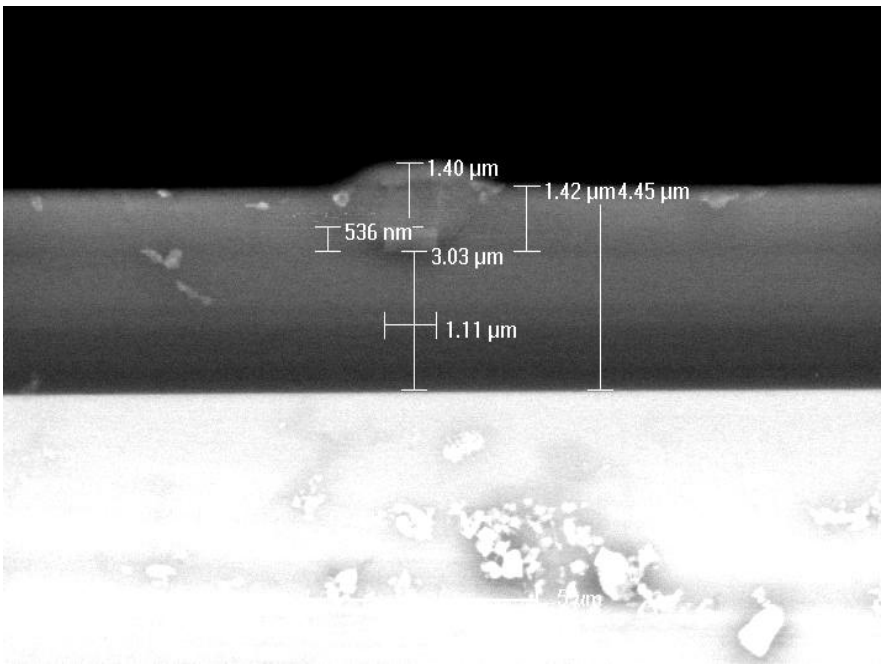


Figure 5- 24: Measurement of core and cladding dimensions from Back-Scattered image taken from the cross section of the front side of a batch B6-4 wafer.

With the collected information from the techniques described above, there are two methods to find the unknowns.

1. Method I: Front_dielectric_height = LC - LC_OE + UC
   For LC and UC backside dimensions were used, Front_dielectric_height was measured from front side and LC_OE is the unknown.
2. Method II: LC_OE = UC + LC + Si_OE - Dektak_Well_Depth

where LC stands for lower cladding, LC_OE for lower cladding over-etch, UC for upper cladding, and Si-OE for over-etch into the silicon substrate.

Between the two options, Method II proved to be more robust since it uses more information from the measurements, including the measured Si_OE. Therefore, method II was adopted and then the optimized thickness of required Al/In layer for perfect vertical alignment is found through[20]:

Required Al/In = Core/2 + LC (Actual_Lower_Cladding) + Si_OE - 3.605

where 3.605 is the vertical position of laser active region measured from the bottom of laser platelet, factor y_L as discussed before. The actual core thickness of 0.5µm was used in this calculation.

From the schematic shown in Figure 5- 25, the rationale behind equations above might become clearer. Essentially, the Dektak measurements do not see the core height if the sweep does not go over a waveguide. However, the lower cladding over-etch is factored in the well height measurement results. Therefore, Well_Depth = (LC - LC_OE) + UC + Si-OE. Rearranging the terms yields the equation presented for method II. Conversely, as seen in Figure 5- 25, in Al/In thickness calculation, the lower cladding over-etch is not a determining factor since the core is sitting on top of the intact section of lower cladding with as-deposited thickness, hence the equation for Al/In layer thickness results.

Table 5- 5 summarizes the lower-cladding over-etch found through calculations above. Based on the actual lower cladding thicknesses and over-etch into Si substrates, the optimum required Al/In layer for each batch is listed in Table 5- 6.

The reason behind the n/a entries for batches B6-1 and B6-2 is that they had a cover layer (probably the poly-silicon hardmask was not removed) which prevented the dielectric stack removal that enabled finding Si_Over_Etch, a factor that was actively used in calculations to find the required height of the bonding layer .

[20] Note that since the core is sitting on top of the intact lower cladding, actual lower cladding thickness is used for Al/In height calculation. The lower cladding over-etch factor comes on stage, when measuring recesses etched depths.

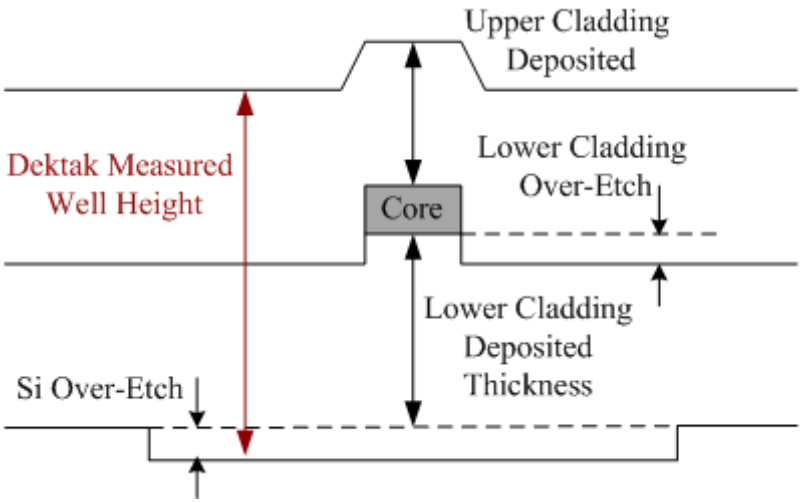


Figure 5- 25: Schematic showing how the Dektak profiler does not see the core thickness and instead measures Si_OE + (LC - LO_OE) + UC. Also note that in finding the required Al/In thickness, the lower cladding over-etch is not included in the equations, since the core is sitting on top of the intact deposited lower cladding.

Batch #	Expected LC	Actual LC	M II: LC Over Etch
B6-13	4.2	4.1	1.09
B6-10	3.9	3.48	0.44
B6-7	3.6	3.23	0.63
B6-4	3.3	3.03	0.83
B6-2	3	2.86	n/a
B6-1	3	2.84	n/a

Table 5- 5: Summary of findings for actual lower cladding thicknesses and over-etch into SiO_2 lower cladding (in µm) for each batch #.

Batch #	Actual LC	Si Over Etch	Al/In Required (µm)
B6-13	4.2	1.46	2.205
B6-10	3.9	1.26	1.385
B6-7	3.6	1.3	1.175
B6-4	3.3	1.3	0.975
B6-2	3	n/a	n/a
B6-1	3	n/a	n/a

Table 5- 6: Optimum required Al/In layer thickness derived based on actual lower cladding thickness and over-etch into Si substrate. (All dimensions are in µm.)

Overall, batch B6-4 was selected for subsequent integration given the reasonable required Al/In thickness that the Table 5- 5 indicates for this batch.

In summary, the study described in this section enabled us to carefully and accurately optimize the bonding layer thickness and maximize the vertical alignment of laser active layer to achieve optimum coupling. For batch B6-4, the required Al/In layer was 0.975μm for which 850nm of Al was deposited (either with RF Sputtering or eBeam evaporation) followed by 120nm of In (either with thermal evaporation or eBeam evaporation in the two deposition methods used). In both cases, the actual deposited thickness was measured[21] to be about 1.1μm due to non-exact tooling factors used in the deposition systems.

This over deposition was in fact desirable, as previous studies [88] had shown that indium on a flat surface undergoes about 60nm of immersion/spreading in the bonding phase. Comparing the height of the Al/In layer on the bottom of adjacent recesses on the same wafer for the two cases of: recesses with a laser platelet bonded in them and then got debonded through probing (for instance see Figure 5- 26), and recesses that no laser was bonded in them, showed the height of Al/In layer is about 100nm different in the two cases. Hence, the spreading of In might be more or less in that range, which also incorporates the smoothening of surface roughness of as-deposited In when laser platelet presses on it during pressured bonding.

Therefore, with 1.1μm minus 100nm, the post-bonding layer will be very close to the desired Al/In thickness of 975nm for batch B6-4, given that Dektak results had about ±50nm accuracy in well height measurements. Therefore, the accuracy of Al/In layer thickness is about ±50nm, hence the vertical alignment accuracy, which is tolerable given the height of the two waveguides[22].

[21] Due to the softness of indium, Dektak pin scratches it during the scans. Therefore, in order to get a more accurate measurement of the In height, Dektak probe pressure was reduced to its minimum i.e. 1mg rather than the normal profiling with 5mg setting.

[22] Another advantage of using low index contrast of SiON/SiO_2 system for dielectric waveguide (rather than high index Si) is the fact that core can be larger in diameter and still be single mode. This larger diameter of the dielectric core provides more room for vertical misalignment and recess depth variations on a wafer scale based on the RIE/deposition systems we had on hand. In an industrial process, these variations can be minimized, thus an even better vertical alignment of the two waveguides can be ensured.

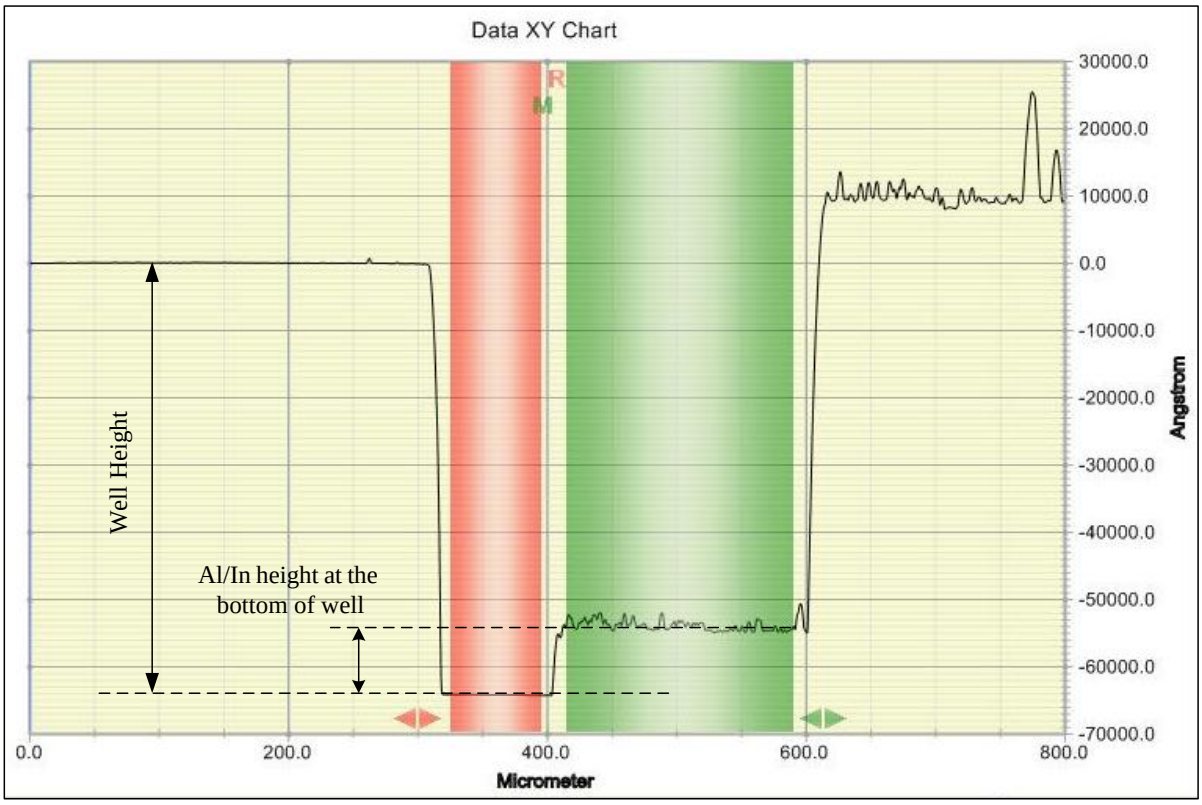


Figure 5- 26: Sample Dektak profilometery results, going over the length of a recess. The average height difference between the green and red bands is 1.03µm which corresponds to the Al/In height at the bottom of the well in this case. Note that a laser was bonded in this well and got debonded during measurements. Comparing the height of the Al/In layer in a series of wells with debonded lasers and wells that did not have lasers assembled in them, gives the immersion of In, which was compensated by increasing the pre-bonding deposition thickness.

5.7. Integrated Structure

With all that was discussed in this chapter, and depositing the optimized thickness of the Al/In layer, assembly of platelet lasers in recesses and executing the bonding phase, the integrated structures were obtained and are shown in the SEMs of Figure 5- 27 to Figure 5- 32.

Specifically, Figure 5- 27 to Figure 5- 31 show two lasers assembled in adjacent recesses of 311µm and 312µm in length, and the zoomed SEMs from the front and end facets show great horizontal alignment of the laser ridge to the dielectric waveguides on the Si wafer. SEMs in Figure 5- 32 depict the snug fitting of the platelet edges to its recess.

In the next chapter, the measurement results of the optical characterization of these integrated lasers will be discussed.

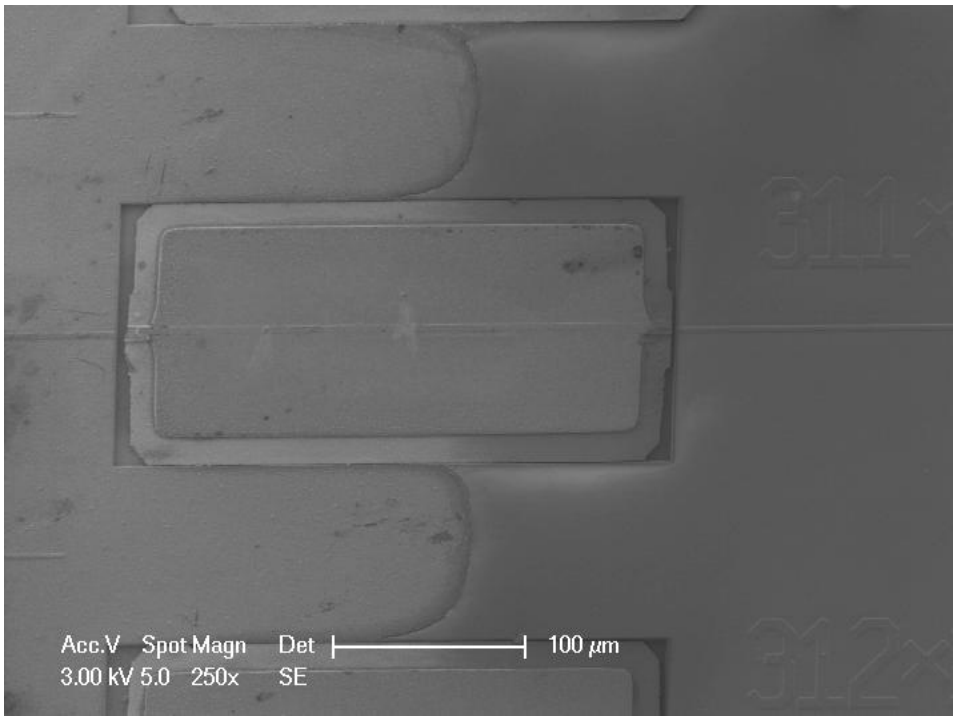
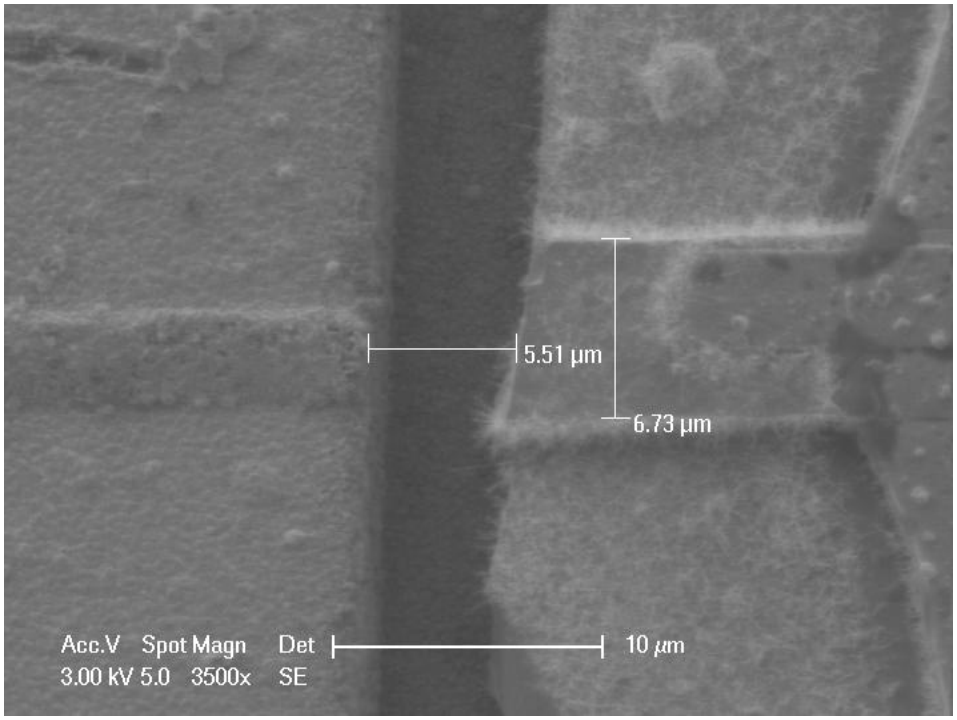
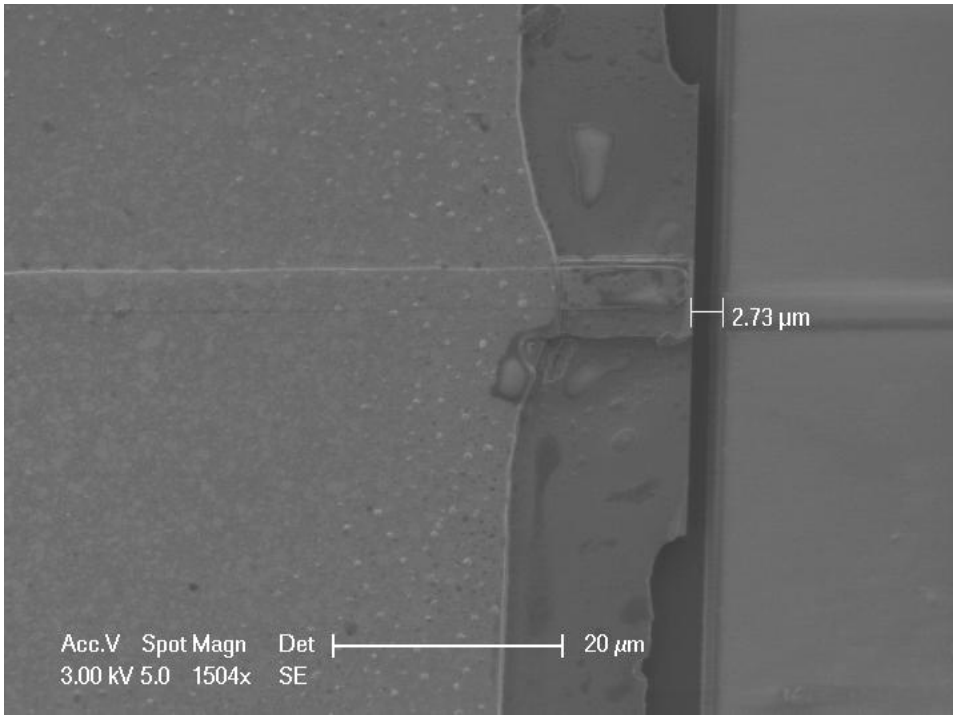


Figure 5- 27: SEM image of integrated and bonded laser platelet in a 311µm×150µm recess.



(a)



(b)

Figure 5- 28: Zoomed in SEM images of (a) left and (b) right laser - dielectric_waveguide facets for the integrated laser platelet shown in Figure 5- 27.

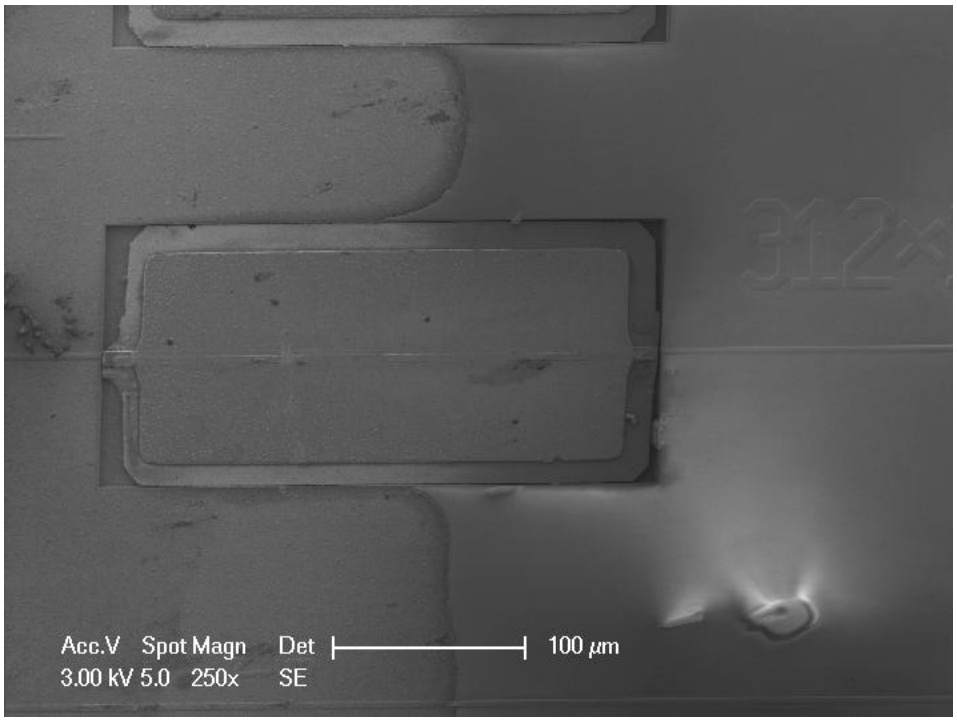


Figure 5- 29: Another instance of an integrated laser, here in a 312µm×150µm recess.

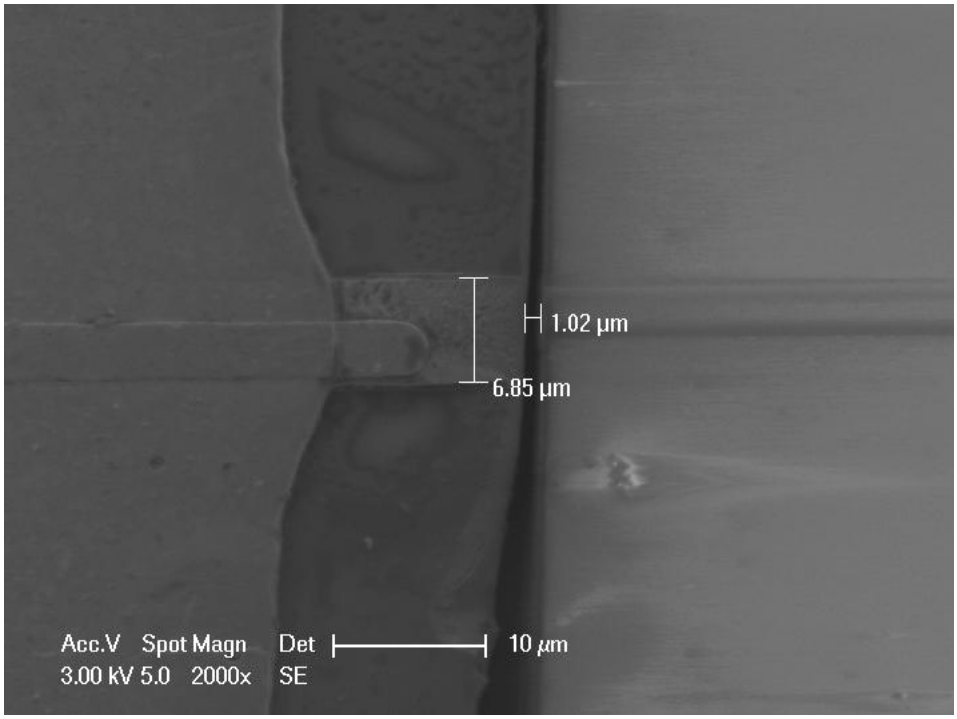


Figure 5- 30: Zoomed in SEM image looking at the right facet of integrated laser shown in Figure 5-29. This facet has a gap width of about 1µm and shows good horizontal alignment of the laser ridge and dielectric waveguides.

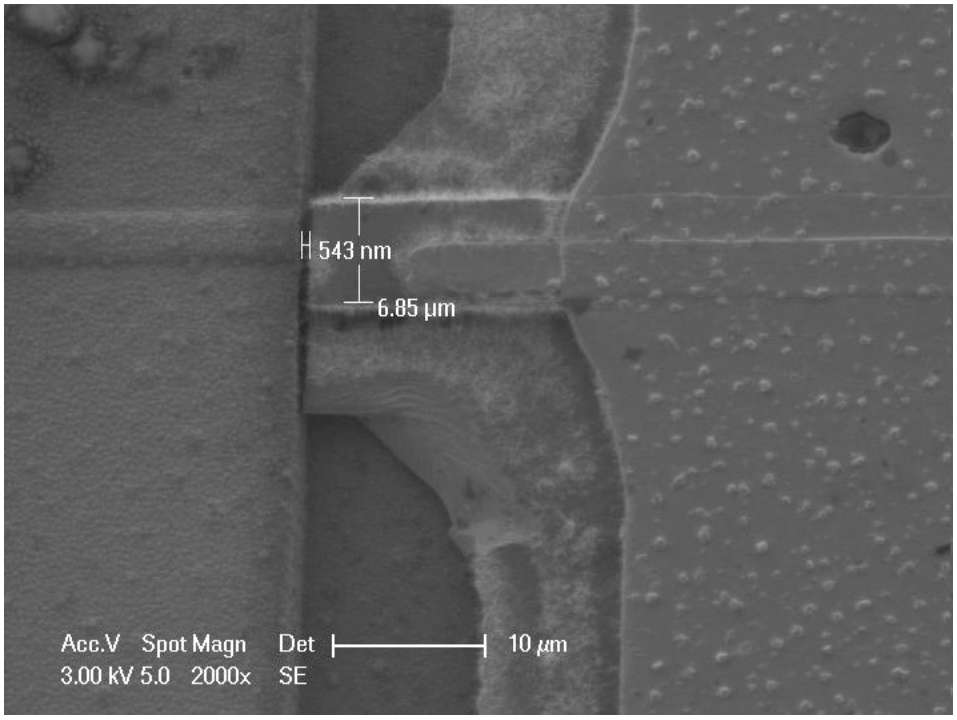
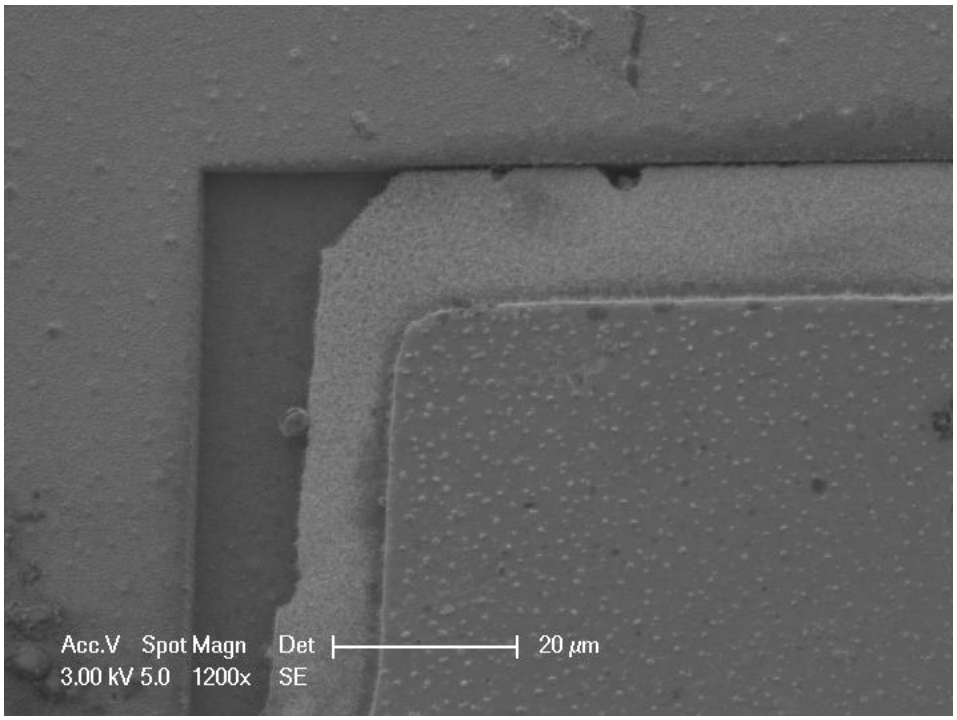
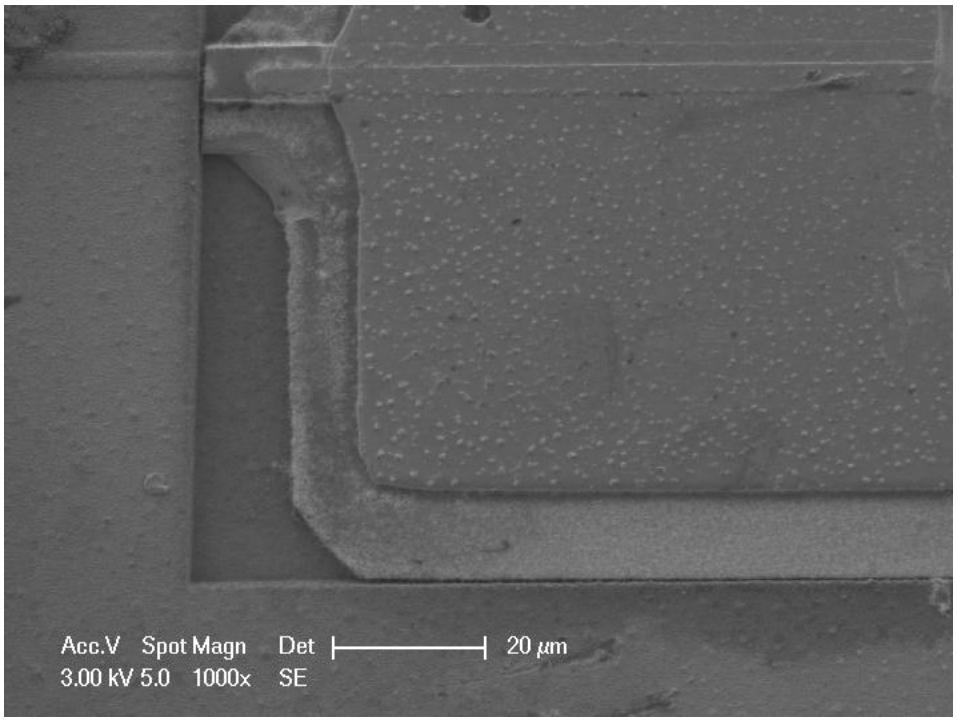


Figure 5- 31: Zoomed in SEM image looking at the left facet of the integrated laser shown in Figure 5- 29. This facet has a gap width of about 0.5µm and like the left facet has great horizontal alignment of the laser ridge and dielectric waveguides.



(a)



(b)

Figure 5- 32: SEM images of integrated laser platelet of Figure 5- 29 looking at the tight fitting of the laser with recess sidewalls. Such a snugly fit will eliminate the possibility of rotational misalignment.

Chapter 6

Measurements and Results

In Chapter 5, the details about the integration process of InGaAs/InP laser platelets in SiO_2 recesses fabricated on Si substrates were discussed, and methods used to achieve a good vertical alignment of laser platelets active region and dielectric waveguides SiON core were presented. Having the lasers fully bonded and integrated in the recesses and the chips cleaved and polished, the integrated structures are ready for measurements and characterization.

In this chapter, measurement results of the integrated laser platelets with SiON waveguides will be presented. The lasing operation of integrated lasers with both pulsed and continuous wave drives at room temperature is characterized, and threshold currents are determined for each laser. Next, IR images from the output facets of the integrated structures are demonstrated. Complementary simulations to determine the fundamental modes of the laser ridge and dielectric waveguides are carried out and the overlap integral of fundamental modes is calculated, as well as the divergence angle of the output beam from the integrated chip. Furthermore, the frequency spectrum for CW lasing operation is studied, from which mode switching with the increase of drive current and temperature is investigated and the effective cavity length is derived. Since the integrated lasers show a significant enhancement in mode suppression ratio (MSR) compared to their non-integrated counterparts, three-mirror cavity model is described and calculations to estimate the MSR of the integrated lasers are presented. Also, external quantum efficiency and characteristic temperature factors are extracted. Finally, various methods to estimate the coupling loss between the laser and dielectric waveguides are discussed and the results are analyzed. The discussion about the future work and possible improvements to components and fabrication steps in the coaxial integration approach will be presented in Chapter 7.

6.1. Measurement Setup

The integrated structure with lasers bonded in recesses and coupled to the SiON/SiO_2 dielectric waveguides is electrically pumped for pulsed and continuous wave measurements. As shown in the cross section schematic of Figure 6- 1, two probes deliver the electrical drive. One of the probes sits directly on the laser platelet surface (the top p-type ohmic contact) and the other probe is placed on the patterned Al/In coated area on the wafer surface, which is continuous along the sidewalls of the recess and is in contact with laser's backside n-type ohmic contact. The fact that in this integrated structure, the Al/In solder-bonding layer also brings the laser's backside contact to the front surface of the chip is an advantage and provides ease of contact and probing.

As a reminder, as can be seen in Figure 6- 1, the laser output beam is coaxially coupled to the SiON core of the dielectric waveguide fabricated on the Si substrate and after propagating through the waveguide, it can be measured with a photodetector or fiber, at the output facet of the chip.

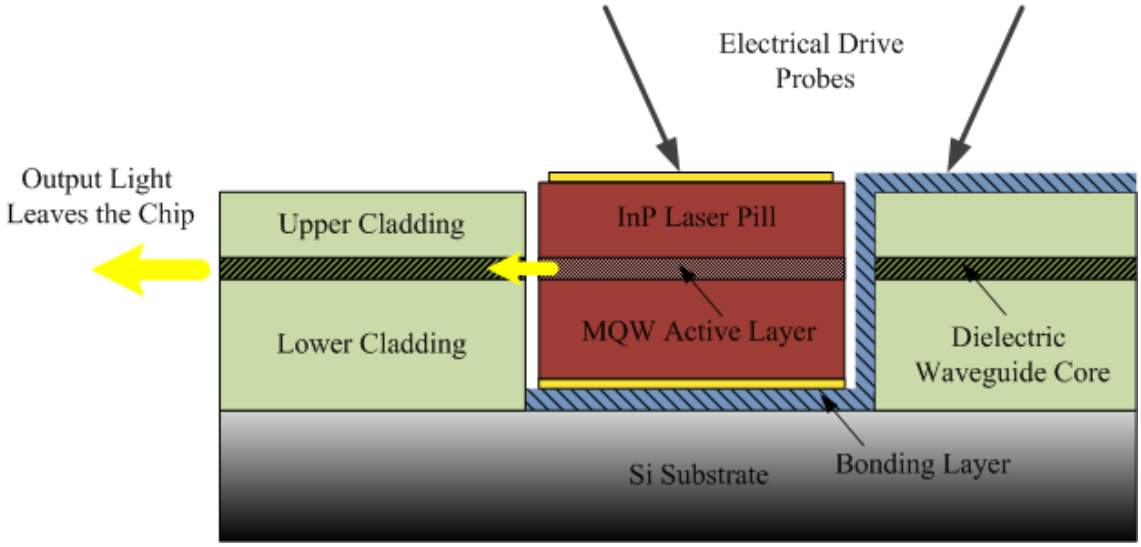


Figure 6- 1: Schematic illustrating the cross section and measurement of an integrated laser in a recess, which is coupled to dielectric waveguides fabricated on a Si substrate. Probes make contact to laser's top n and bottom p gold contacts, both on the frontside of wafer.

To maintain temperature control during the measurements, the integrated wafer is placed on a thermoelectric cooler (TEC) mount connected to an LFI-3751 Thermoelectric Temperature Controller from Wavelength Electronics. Figure 6- 2 shows an image taken of the measurement setup, where the chip with laser platelets integrated in recesses is being electrically driven by probes, and the output is measured by a small area InGaAs infrared photodetector. The stripes that can be seen on the wafer are the patterned Al/In solder-bonding layer.

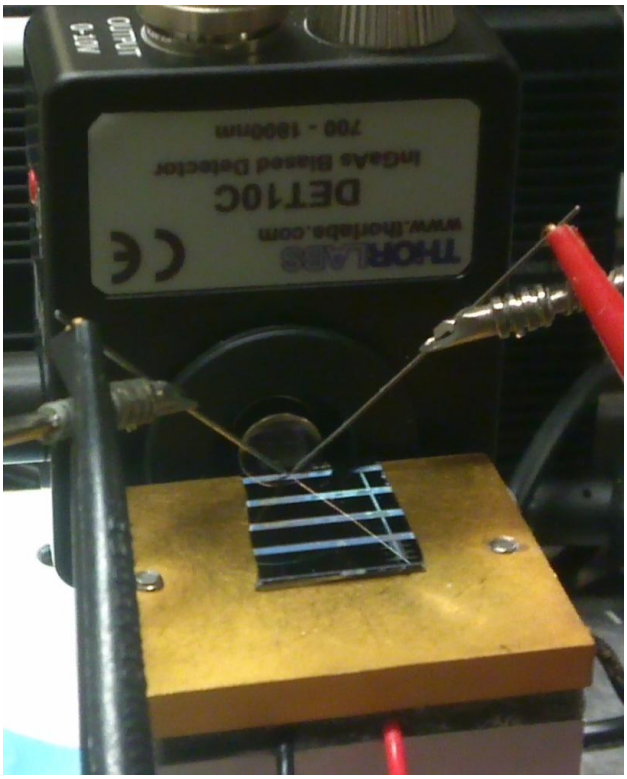


Figure 6- 2: Photograph taken from the measurement setup, showing the integrated chip sitting on a TEC mount, driven by probes and its output is measured by an IR photodetector.

A list of equipments that were used for the measurements is found in Table 6- 1, along with some of their important specifications. The large area Ge and small area InGaAs photodetectors (PD) used here had an output voltage and were connected to an oscilloscope (for pulsed measurements) or a voltmeter (for continuous wave measurements). The large area Ge PD had a gain of 0-70dB and could be loaded with 50Ω or Hi-Z loads. The small area InGaAs PD did not have any gain; however due to a simpler circuitry, it had a more clear and tractable time domain response in pulsed operation when compared to the more complex response dynamics observed from Ge PD due to its higher order filter and gain circuitry.

Since these two detectors both had voltage outputs that needed to be calibrated to derive the actual emitted lasing illumination power, another InGaAs power head detector (OMH-6708B) was also used to measure the output of the lasers directly in watts. This detector from ILX Lightewave had an integrating sphere, and its output was measured by OMM-6810B multimeter from the same manufacturer which provided a very sensitive reading from 10nW all the way to 100mW. The calibrated reading from the Ge PD and this InGaAs power head detector were in good agreement as will be presented in the measurement results. However, the InGaAs power head detector could only be used in CW operation, as for the pulsed case, its analog output was modulated by another signal making in not suitable for accurate pulse response reading. Therefore, for pulsed operation, mostly the Ge photodetector was used and the results had to be calibrated to derive the actual optical power at the output. The process of such calibration is discussed in Appendix II.

Type	Product #	Mat.	Collection Area	Bandwidth (nm)	Vendor	Gain
PD	PDA50B	Ge	19.6mm^2 D=5mm	800-1800	Thorlabs	Yes (0-70dB)
	DET10C	InGaAs	1mm^2	700-1800	Thorlabs	No
	OMH-6708B	InGaAs	D=6mm	800-1600	ILX Lightwave	OMM-6810B Multimeter
Imager		InGaAs	-	IR	Sensors Unlimited	Exposure Time
		Ge	-	Visible - IR	Nobel Peak Vision	-
Fiber	Multimode	-	250µm	-	Photonik	-
	Single Mode Lensed	-	4.3µm	1550	Photonik	-

Table 6- 1: List of detectors, imagers and fibers used in the measurement and characterization of integrated laser diodes.

Since the lasers emitted light output was strong enough, the detectors were able to measure the response directly and there was no need to use a lock-in amplifier[1].

For the pulsed and continuous wave drives, two current sources had been used. For pulsed measurements, ILX Lightwave Pulsed Current Source (LDP-3840B) was used and for continuous wave, Newport Laser Diode Driver (M5005) was employed.

In the following chapters the LI measurements done with the photodetectors with both pulsed and CW drive will be presented.

6.2. Pulsed LI Measurements

6.2.1. Non-integrated lasers

It is usually the best practice to first measure the IV response of a laser diode before performing the LI measurements, as most of the problems with the laser or measurement circuitry can be detected if the laser diode does not show the typical IV curve of a diode. These IV curves, as shown in Figure 6- 3, had been measured with an HP4145 Semiconductor Parameter Analyzer,.

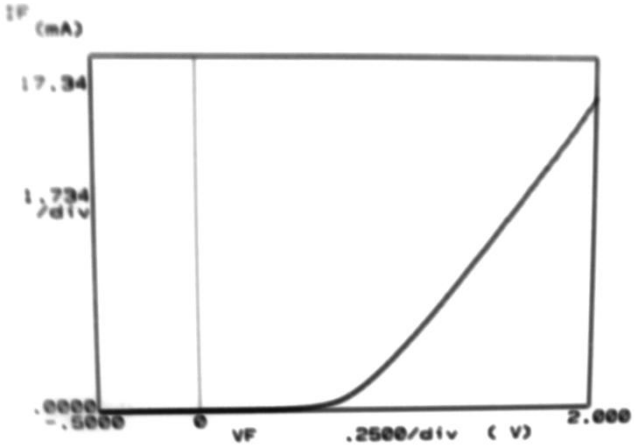


Figure 6- 3: IV characteristic of an integrated laser, showing a typical diode response and confirming that probes have made a proper contact with the n and p contacts of the laser diode.

[1] Nevertheless a lock-in amplifier was also used in initial measurements for pulsed operation. However it was noticed that the loading of the locked-in amplifier on hand was significant on the PD output voltage, dropping the response to very low values, probably due to not-sufficient buffer at the output of PD circuitry and low input impedance of the lock-in amp. When a buffer that accompanied the amplifier was added to the circuit, the high 60dB gain of the buffer, made the lock-in reading to overload. As mentioned earlier since the output of lasers are high enough and detectors used had enough sensitivity, the use of lock-in amplifier was not required in the measurements.

After confirming the health of the contacts by observing a typical IV diode characteristics, the lasing response was measured in pulsed drive first, as heating is less compared to CW and the chances of lasing is higher as a result.

Figure 6- 4 shows the LI pulsed lasing response measured from a non-integrated laser bonded on a flat Al/In covered surface. The emitted light of the laser is measured with the large area Ge photodetector and a gain of 40dB was used. Furthermore, the input pulses were set to have a pulse width (PW) of 1μs with the percent of pulse repetition interval (%PRI) of 0.6%[2], which means that pulses have a period of PW/PRI=1μs/0.6%=166.7μs or f=6kHz. The TEC temperature was set to 15˚C and the response shows successful lasing with a threshold current of I_{th}≈22mA.

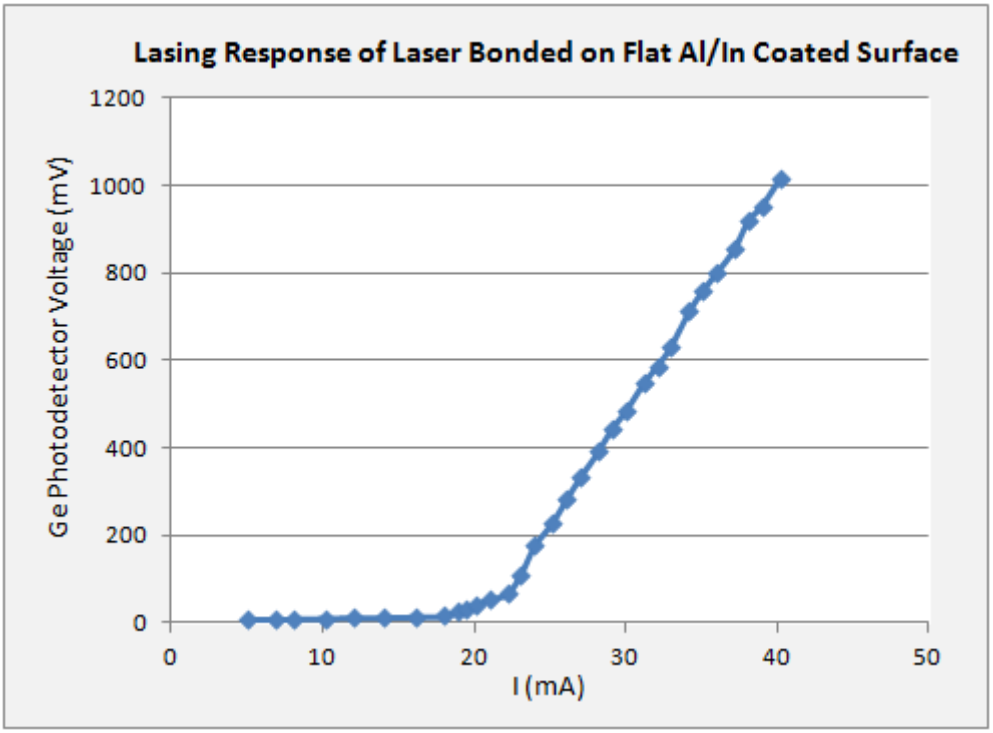


Figure 6- 4: LI pulsed response of a non-integrated laser, bonded on a flat Al/In layer.

The LI response of another laser of the same type (i.e. bonded on a flat Al/In coated surface) is shown in Figure 6- 5, with pulse parameters of PW=1μs and %PRI=0.5% (i.e. f=5kHz).

[2] In this specific measurement PRI was 1% initially and was reduced to 0.6% after 18mA not to heat up the lasers. However for subsequent measurements the drive parameters other than the current were kept constant throughout LI measurements.

One can notice that the output reading of the photodetector is higher for this laser[3]. One reason might be the inherent difference between the emitted optical power of lasers, but also it can be due to the difference in the alignment of the photodetector or the positioning of the probes resulting in different series resistances in the path of the drive circuit. In Figure 6-6 such a difference in the LI response of a same integrated laser diode but with two different probe and detector positions is illustrated. The exact reason of why changing probe positions results in such different light emission levels when the drive is a current source, is not entirely clear to the author and is currently under investigation.

Nevertheless, for this laser I_{th}≈22mA as well, which is similar to the laser whose response is shown in Figure 6- 4. In fact this trend of very close and repeatable measured threshold currents was consistently observed among the integrated lasers as well.

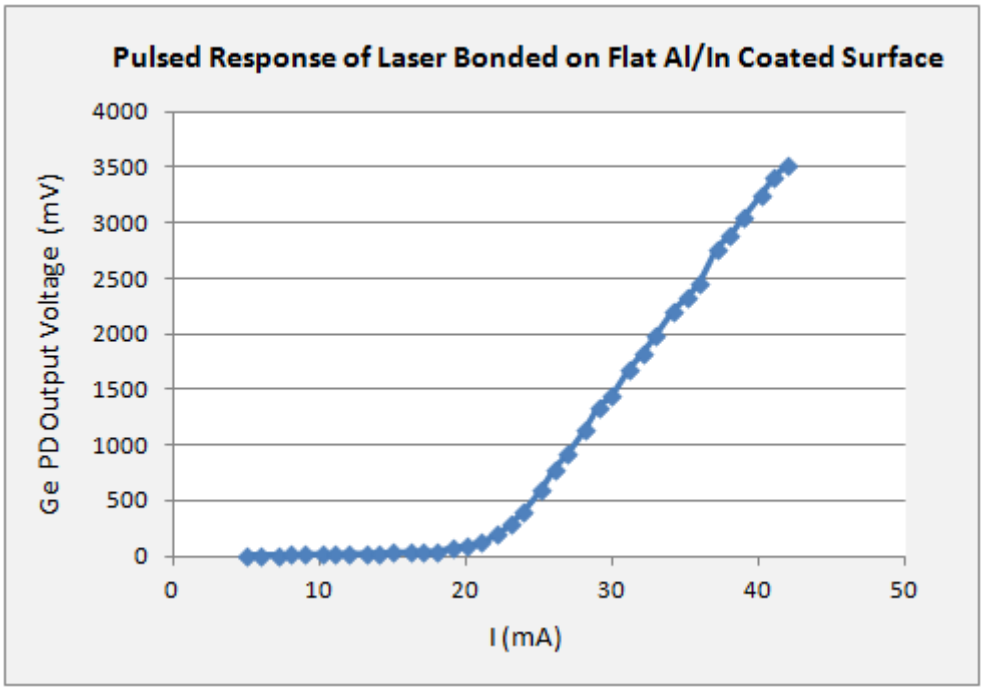


Figure 6- 5: LI pulsed response of another laser bonded on a flat Al/In coated surface. (%PRI=5%). Same threshold current compared to the laser with a response shown in Figure 6- 4 is noticeable while the read voltage varies due to individual laser differences as well as probe positions and detector alignment variation.

[3] Later in this chapter, the conversion of Ge PD output voltage to optical power in watts will be presented.

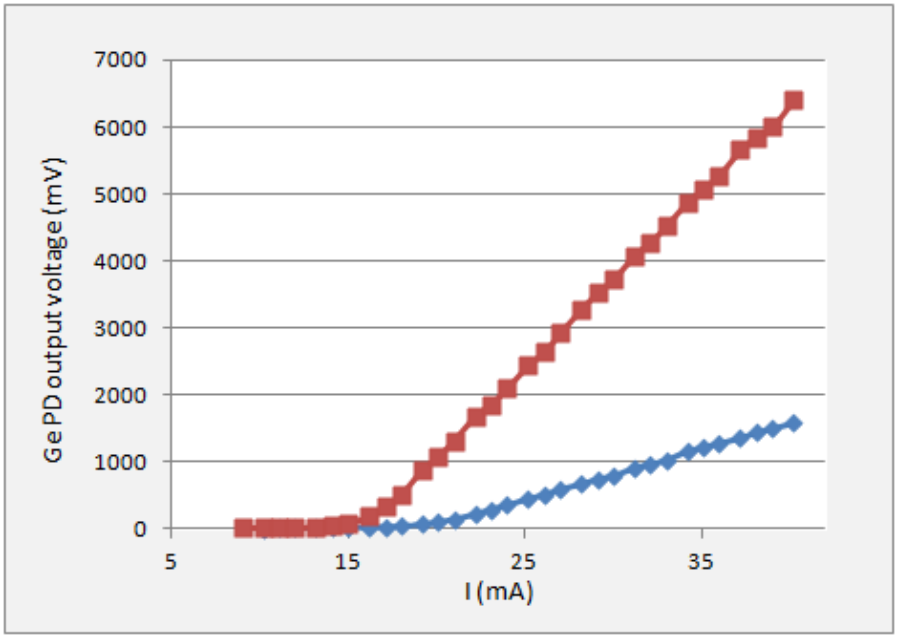


Figure 6- 6: Two LI pulsed responses of one integrated laser bonded in a 308µm recess. Probe positions (probably the quality of contacts) and photodetector alignment had been different between the two cases. Output readings from the PD are quite different whereas I_{th}s are the same[4].

6.2.2. Integrated Lasers

Having confirmed the lasing operation with a pulsed drive and for the non-integrated lasers, the same measurements were carried out for integrated lasers in recesses and coupled to the SiON dielectric waveguides. The details about assembly and bonding these laser platelets into SiO_2 recesses fabricated on Si substrates were discussed in Chapter 5.

Figure 6- 7 shows the lasing response of a laser platelet bonded and integrated in a 312µm recess. The inset in the graph illustrates the SEM image of this laser, where the patterned Al/In bonding layer on the top surface is also noticeable which brings the backside n-contact of the laser platelet to the front of wafer surface for probing and measurements. The drive had PW=1µs, %PRI=0.5% (f=5kHz), and TEC temperature was set to T=15˚C. Furthermore, the Ge PD had a gain of 30dB in this measurement, and the readings were based on peak-to-peak pulsed voltage response of the photodetector (as a result of the pulsed drive). The threshold current of this pulsed lasing is at I_{th}=17mA, consistent with other integrated lasers whose responses are shown in Figure 6- 8, Figure 6- 9 and Figure 6- 10, corresponding to the lasers bonded in 306µm, 311µm and 308µm recesses, respectively. In all these

[4] In order to accurately determine I_{th} of the lower output case (the blue color in graph), it was plotted separately to have a zoomed view of the advent of lasing.

measurements, the drive and Ge detector parameters are similar to what is listed above for the laser integrated in 312µm recess, although lasers might belong to different fabricated chips.

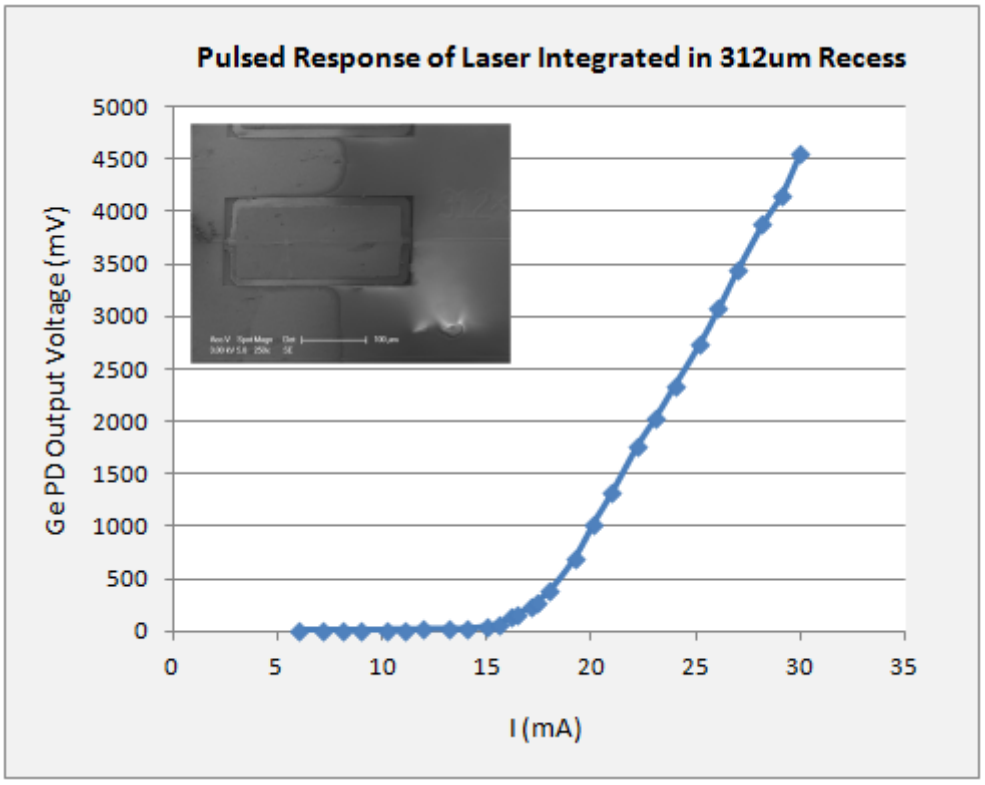


Figure 6- 7: LI pulsed response of the integrated laser in a 312µm recess, showing I_{th}=17mA. The inset image is an SEM taken from this integrated laser in its recess.

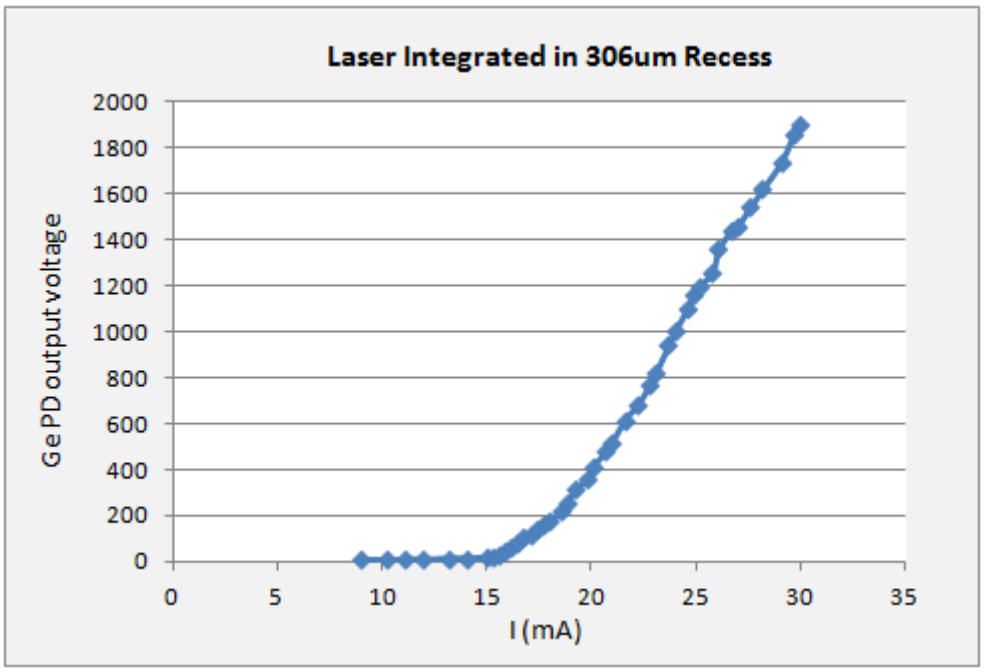


Figure 6- 8: LI pulsed response of the laser platelet bonded in a 306µm recess showing I_{th}=17mA.

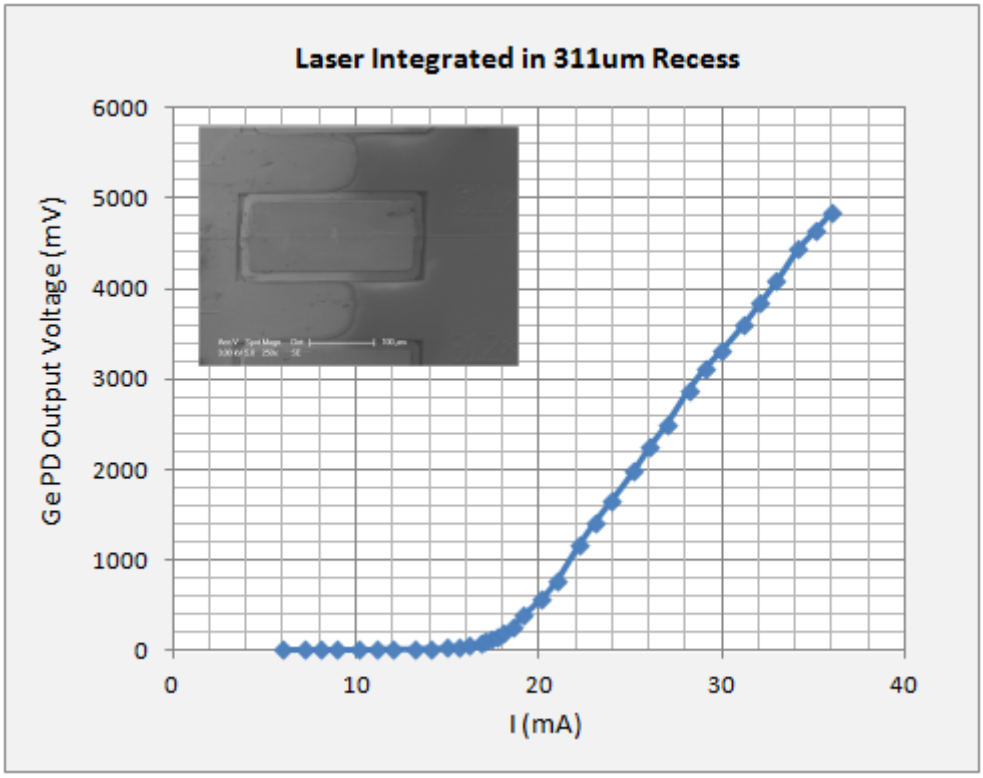


Figure 6- 9: LI pulsed response of the laser platelet bonded in a 311µm well. I_{th}=17mA similar to other lasers measured with pulsed drive. The inset shows the SEM image of this integrated laser.

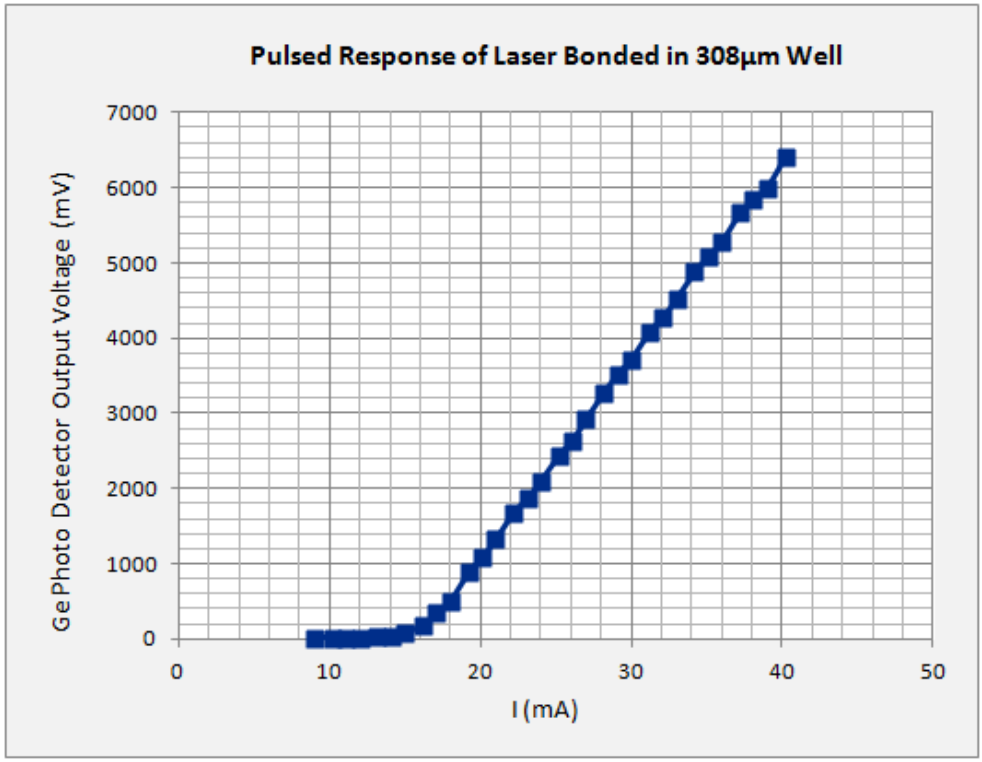


Figure 6- 10: Pulsed LI response of the laser integrated in a 308µm recess, I_{th}≈17mA.

6.2.3. Calculating Optical Power from Detector Output Voltage

Since the Ge PD used in the pulsed measurements has a voltage output, calibration needs to be carried out to translate the voltage signal to an actual optical power. Appendix II explains the process of such calibration, which reveals that in order to convert voltage to optical power for this detector, the calibration factor for the 30dB gain, i.e. $A_{30dB\text{-}adjusted}$, is derived to be:

$$A = V / W \rightarrow W = V/A$$

$$A_{30dB\text{-}adjusted} \approx 3.47 \times 10^3$$

Hence, in the case of the pulsed response of the integrated laser in a 308µm recess (whose LI response in shown in Figure 6- 10), the PD has a peak-to-peak pulse voltage of 6.4V for I=40.2mA. Based on the calibration factor above, the optical power leaving the output facet of this integrated chip can be calculated as:

$$W_{308um\_laser\ 30dB\text{-}adjusted\ @\ 40.2mA} = V/A = 6.4 / (3.47\times10^3) = 1.844\ mW / facet$$

The output power derived from the calibrated gain factor presented here is consistent with the readings from InGaAs PD used with an optical multimeter, which has internal calibrations and directly shows the output power of the emitted light. This agreement verifies that the adjustment value is in fact needed to be incorporated into the gain factor of this Ge PD, as discussed in Appendix II.

The laser integrated in the 308µm recess is a fairly bright laser compared to its counterparts (Figure 6- 7 to Figure 6- 10). Table 6- 2 summarizes the derived output power from the output facet of the SiON dielectric waveguides to which laser platelets couple to. Input current of I=30mA, detector gain=30dB, PW=1µs and %PRI=0.5% were common for all the measurements. Based on calculations in Appendix II, the conversion factor of $A_{30dB\text{-}adjusted} = 3.47\times10^3$ had been used to calculate the output optical power from the PD voltage response. Like before, the lasers are differentiated by the length of the recess they had been integrated into, for the purpose of clarity and tractability.

Table 6- 2 conveys that the output power of the integrated structure is around 1mW for modest current levels above threshold. Note that going higher in current will also increase the output power above what is listed in the table above, for instance for free standing lasers, output power as high as 25mW was measured at a high current level of I=160mA by J. Rumpler in [60].

Recess Length of Integrated Laser Platelet	Detector Output Voltage (pk-pk) @ I_{drive} = 30mA	Calculated Optical Output Power (W)
306 μm	1.9 V	548 μW
311 μm	3.32 V	957 μW
312 μm	4.56 V	1.31 mW
308 μm	3.72 V	1.07 mW

Table 6- 2: Calculated pulsed power seen from the SiON output waveguide, to which laser platelets are coupled to. Measurements are done with Ge PD and $A_{30dB\text{-}adjusted} = 3.47\times10^3$ was used.

6.3. Continuous Wave LI Measurements

So far all the presented LI lasing responses were with pulsed excitation. In general, due to lower heat generation and thus lower Auger recombination, lasing is more easily achieved in pulsed operation compared to CW. However lasing at CW and room temperature is essential for commercial applications of laser diodes. Therefore, after confirming that lasers do in fact lase in pulsed operation, the continuous wave operation was examined. Figure 6- 11 shows the CW LI response of the laser platelet integrated in a 308μm recess. The threshold current is seen to be $I_{th}\approx19$mA for this integrated laser.

The measurements were carried out with a TEC temperature of 15˚C and in a dark environment. The direct optical power in watts could be measured, since the integrating sphere InGaAs power head photodetector (OMH-6708B) from ILX Lightwave was used in conjunction with an optical multimeter (OMM-6810B) from the same supplier. In fact, the use of this multimeter was essential since the voltage output of this detector had been quite noisy and voltmeters could not detect the signal from noise. This might be due to the integrating sphere nature of this photodetector, which attenuates the signal significantly and thus a calibrated sensitive multimeter is needed to retrieve it. A Newport Laser Diode Driver Model 5005 was used for the continuous wave current source which provided fine and accurate current steps. Due to xyz positioner issues, the detector had been placed at a slant in this measurement, in contrast to the suggested placement of this detector where its aperture needs to be perpendicular to the incoming light beam. This slanted position of the detector head, might translate to a lower reading of the output power, but the effect is not expected to be significant.

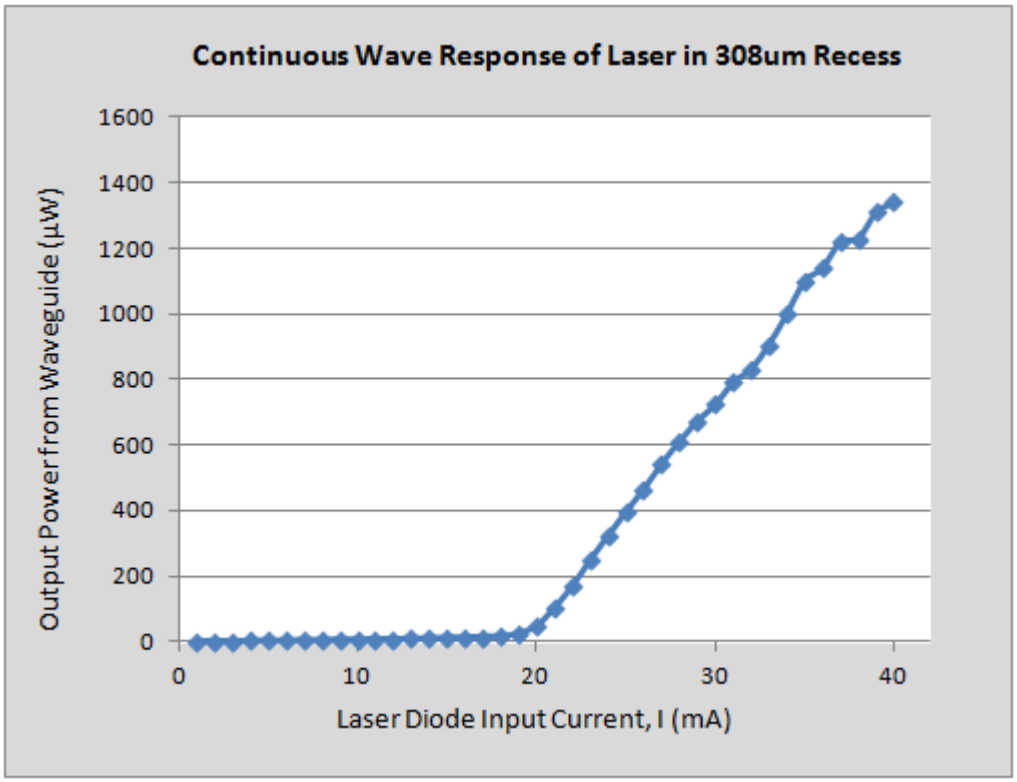


Figure 6- 11: Continuous wave LI response of the laser integrated in 308µm recess.

6.4. Output Optical Mode Shape

The optical output mode shape leaving the integrated chip is of interest for two reasons. First, we want to make sure that the laser's emitted light is actually coupled to the SiON core and is guided through it, rather than through the claddings or air. Second, knowing the output mode shape is helpful for coupling purposes to an outgoing lensed fiber, for instance.

Initially, in order to verify guiding of SiON/SiO_2 waveguides, a visible red source was used. As shown in Figure 6- 12, the beam of a red laser is being focused through a lens onto one facet of the chip. The sample is imaged by a camera, and it is held in place by a vacuumed tip. The user can focus the beam on the facet of the chip by seeing the setup from above with a microscope. In Figure 6- 13, the result of this experiment is shown, where the red beam spot guided by the SiON waveguide that opens to a recess is noticeable in the image. This confirms visible mode guiding by these waveguides.

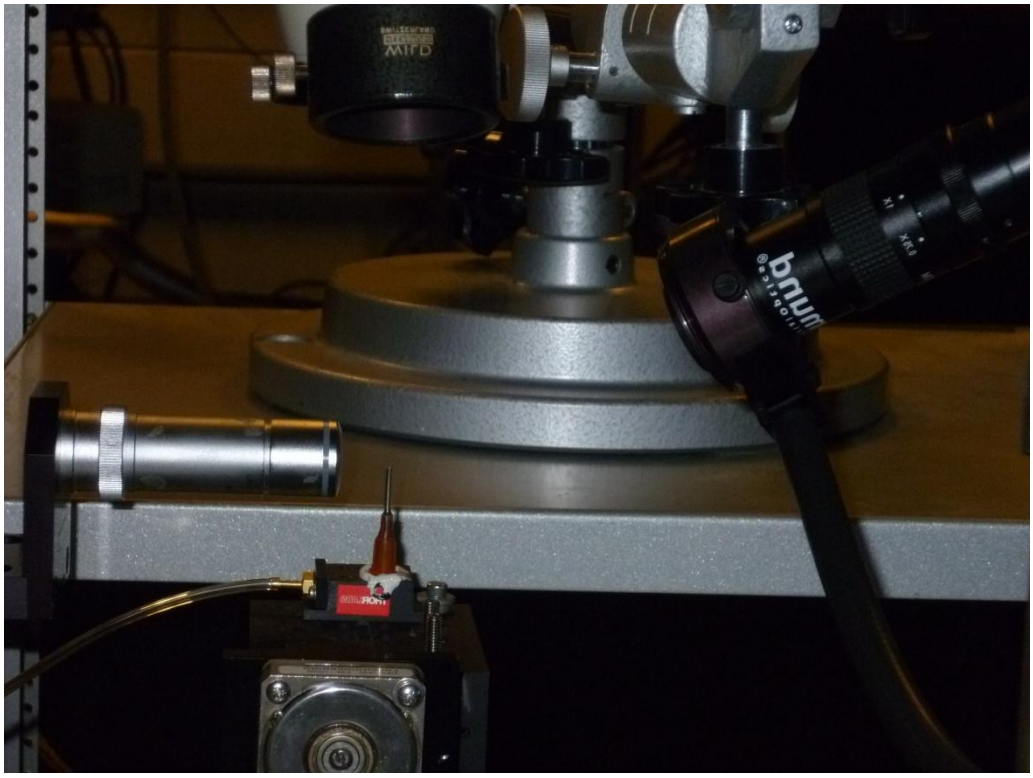


Figure 6- 12: Setup used to verify the guiding of SiON waveguides with a visible red source.

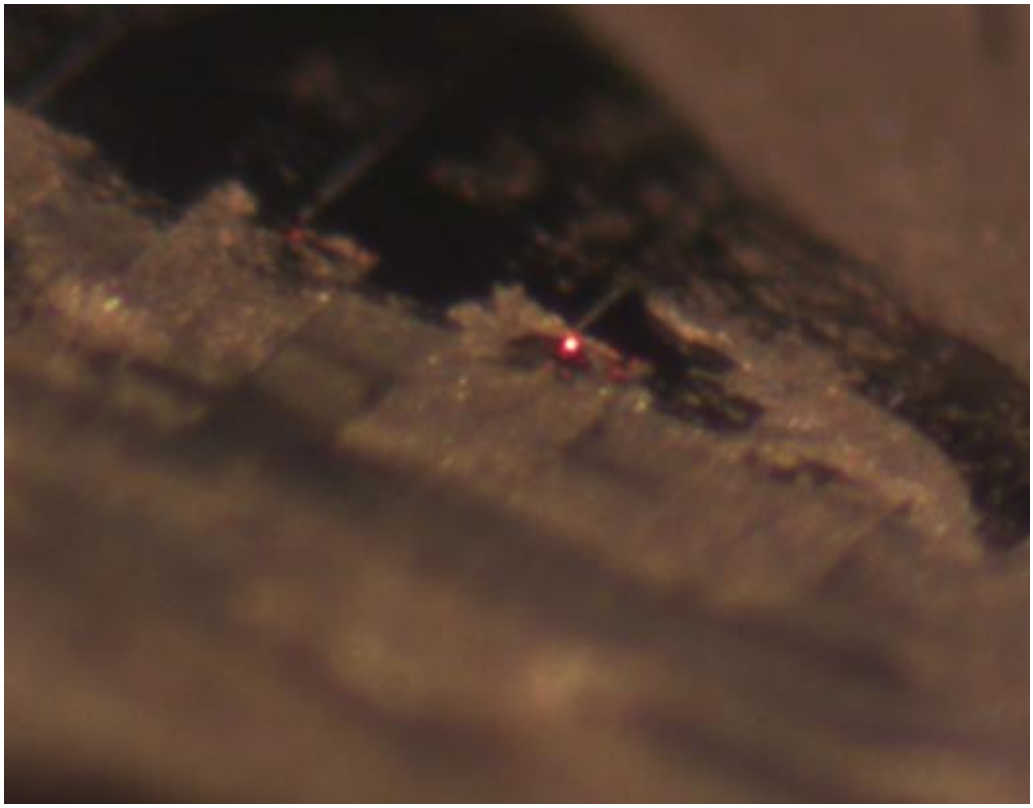


Figure 6- 13: Image taken with setup shown in Figure 6- 12, illustrating the SiON waveguide that opens to a recess, guides the visible red beam that was shined on the chip facet.

In this experiment care was taken to ensure that the laser beam was blocked from being directly imaged by the camera. This was achieved through mounting and silver-paste gluing of a wafer piece vertically on the chip under test, so that only the guided mode in the waveguide is seen by the camera.

Once the mode guiding in visible range was verified, IR imagers were used to see the emission of laser platelets at λ=1.55μm.

6.4.1. IR Images of Output Beam

Using a Ge camera[5] that is wide band enough to be able to image infrared as well as visible simultaneously, Figure 6- 14 was taken. Note that the device under test is the thin square wafer sitting on the thick temperature controlled substrate, and the two probes that provide the drive current are also noticeable in the image. More importantly, the IR lasing beam leaving the output facet of the chip is also seen in this image.

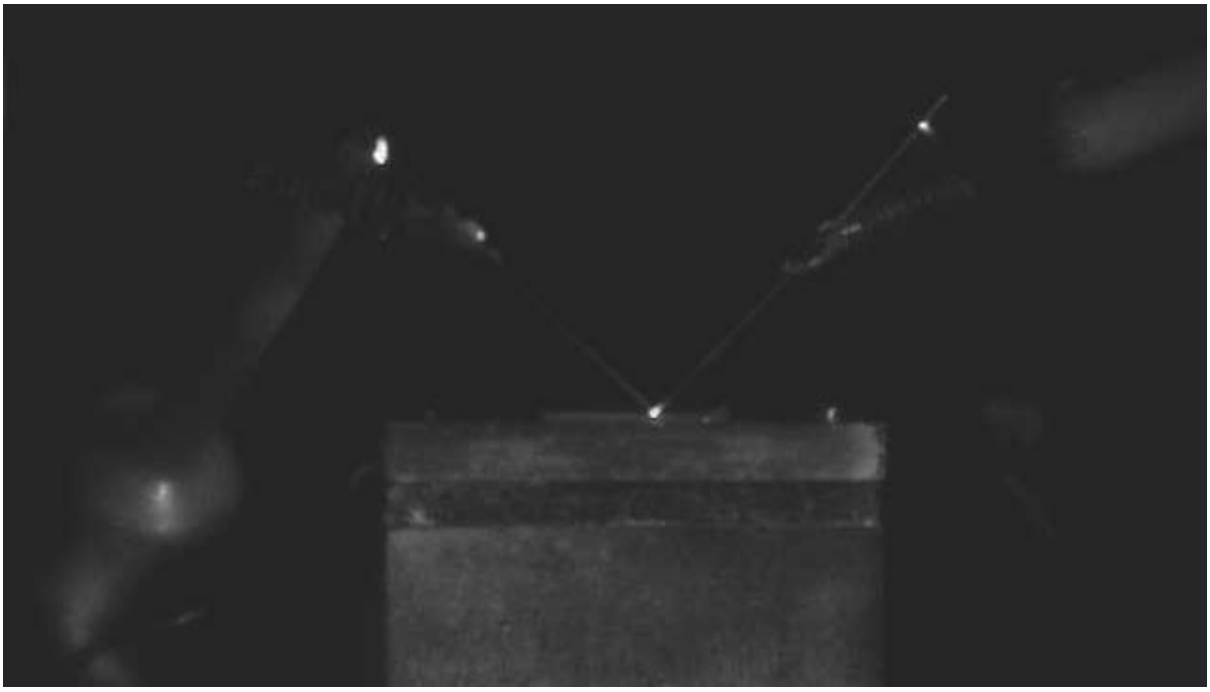


Figure 6- 14: Image taken by Ge camera showing the chip under test, lasing beam, drive probes and the mount on which the chip is sitting.

The image in Figure 6- 14 was taken with a low magnification setting of the lens that accompanied this imager. In order to get a better view of the output beam emitted from the

[5] Dr. Connor Rafferty has kindly lent us this Noble Peak Vision Ge imager.

chip, the close up image of Figure 6- 15 was obtained using the highest magnification setting. Here, the lasing beam can also be noticed as well as the drive probes. There is also slight reflection from the edge of the mount seen at the bottom of lasing beam.

In this image, an incandescent light source was used to add some ambient light to the image, otherwise only the bright laser beam would have been visible as a bright spot against a black background. Adding the wide bandwidth light source helps to see the passive components of the setup, including the chip and the probes, and also helps in getting a good focus on the beam itself.

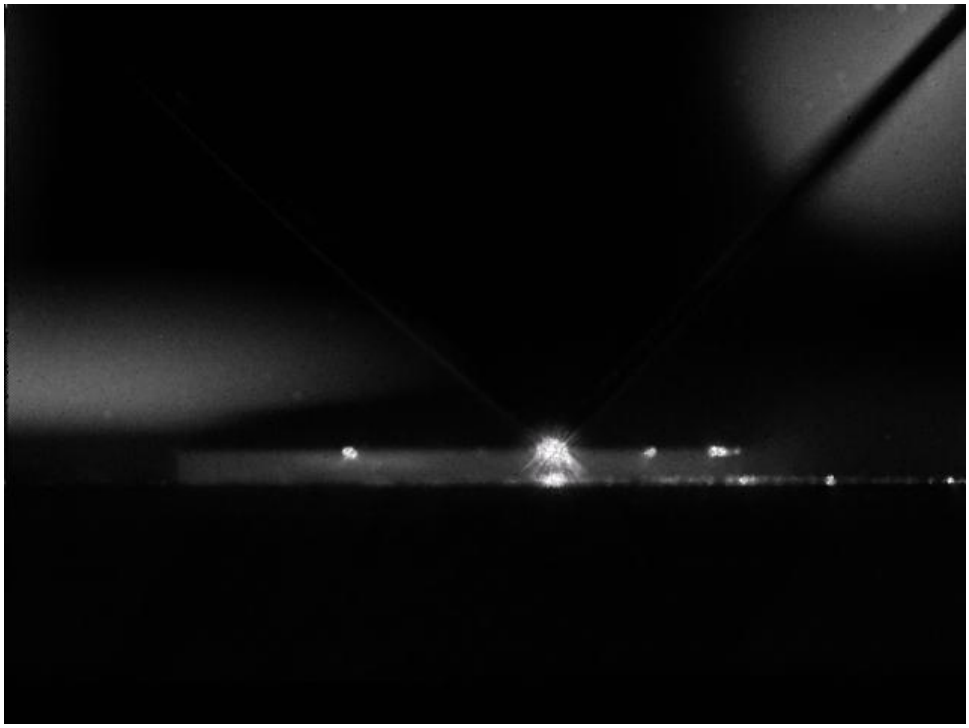


Figure 6- 15: Zoomed image taken by the Ge imager. The lasing beam is obvious as well as the chip and drive probes. There is also a slight reflection from the mount seen at the bottom of chip.

Although informative images could be taken with this Ge camera, due to unknown reasons to the author, extra optics could not be used with this imager since a sharp focus was unattainable adding extra lenses and only blurry images would result. Therefore, in order to be able to view the output beam more clearly and with a better focus, an infrared InGaAs imager was used. Figure 6- 16 shows the setup with this camera. Note that a 40x lens is used to get a higher magnification of the image. This lens had a long enough focal length which allowed it to be placed at a safe distance from the sample, avoiding hitting it during focusing efforts. Since one of the probes sits on the laser surface, such disturbances to the setup could translate to breaking, de-bonding and thus loosing a working laser platelet.

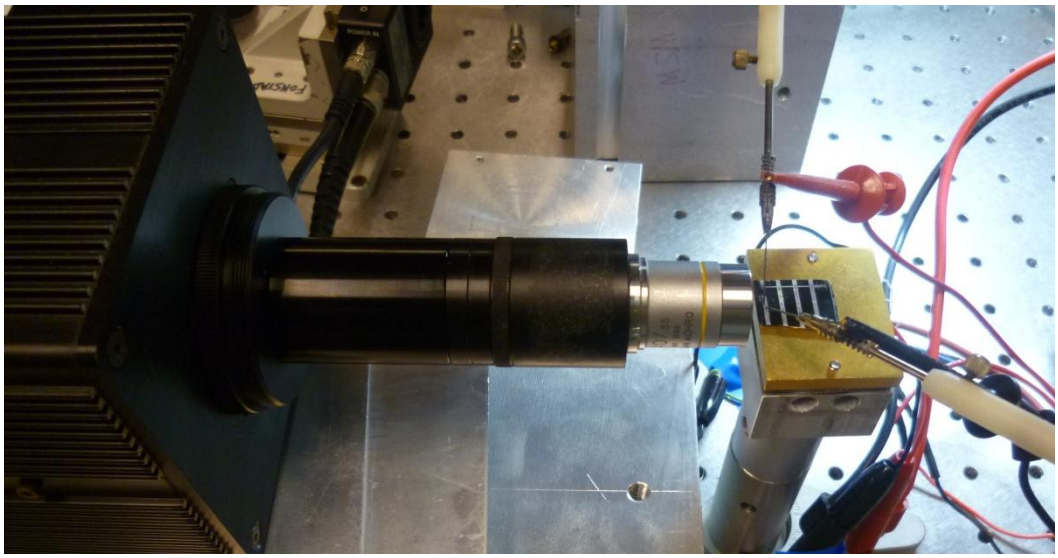


Figure 6- 16: Image of the setup where the output beam from the chip is collimated by a 40x lens and is cast on the IR imager located at the end of the tube on left. The black box is the InGaAs camera.

With this InGaAs infrared camera, at first images were taken without additional lighting, and Figure 6- 17 shows one of the images obtained. Not knowing exactly what was being looked at in this image, adding an extra light source with a wide bandwidth (including infrared) seemed essential. For that purpose, an incandescent microscope light source was used to add ambient illumination to see what the IR image of Figure 6- 17 corresponds to. (Note that for a more sophisticated setup, a beam splitter would direct the image seen from the device under test to two cameras: an IR one that captures the infrared beam of the laser, and a visible range camera to allow the user to monitor the physical location.) With this addition to the setup, the image shown in Figure 6- 18 is obtained and clarifies that Figure 6- 17 is indeed taken from the facet that laser platelet emitted light is being coupled to the dielectric waveguide.

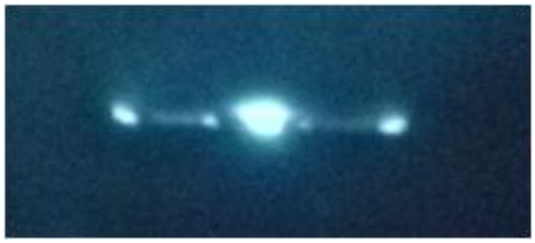


Figure 6- 17: Image taken by InGaAs camera. Later investigation shows this image is seen at the laser/waveguide coupling facet, as shown in Figure 6- 18.

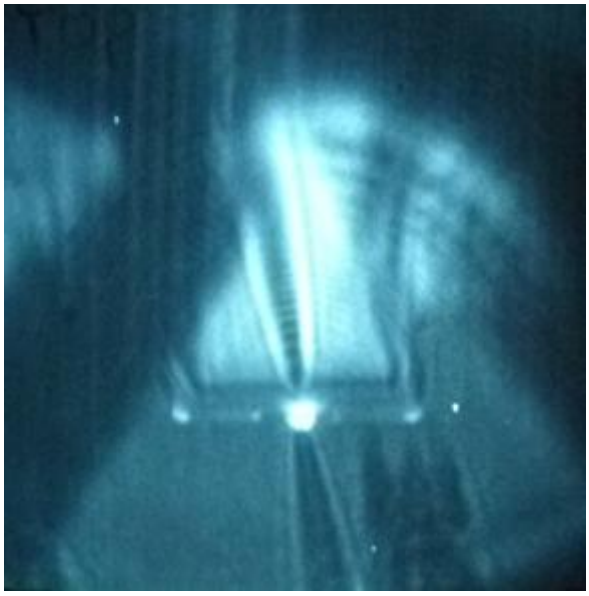


Figure 6- 18: IR image taken with the same focus of Figure 6- 17 but with the addition of wideband light source, revealing that Figure 6- 17 is actually looking at laser platelet's facet.

It is worth mentioning that the relative position of the incandescence light source and its angle to the camera changes the appearance of the image taken. Also note that in Figure 6-18, the point of focus is the laser/waveguide facet. That type of focusing affects how the waveguide appears in the image as well, i.e. at the focus point, it looks like the point of a taper. By changing the rotation or elevation of the light source, the angle of such taper seen in the image would change.

Now that with the help of wideband light source one can verify where the imager is focused at, Figure 6- 19 was obtained through moving the focus point further to the edge of the chip. Note again the taper at the focus point as a result of the angle and position of the light source.

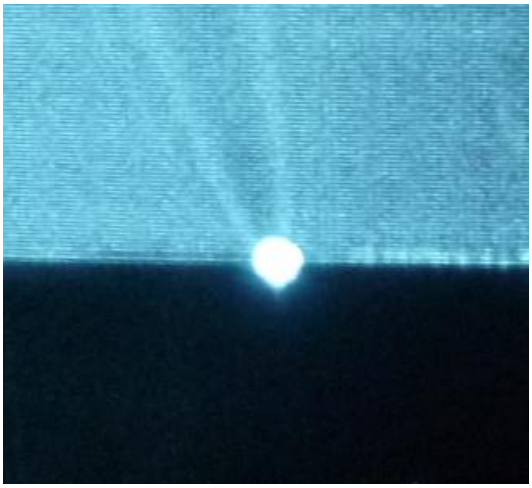


Figure 6- 19: IR image of beam leaving the chip, i.e. at the end of SiON waveguide.

Regarding adjusting the images brightness, for each image the exposure time factor (changeable at the back of camera) was adjusted to prevent over flooding of the images. Also it should be noted that these images had been taken from a VCR display connected to the InGaAs imager, since at the time of the experiment the computer setup used to record imager results was not available.

Nevertheless, these images are sufficient to confirm that the beam is guided through the SiON core and not through air above or lower SiO_2 cladding, nor the Si substrate.

Finally, in order to get a better sense of where the IR images had been taken, Figure 6- 20 shows an overlay of the InGaAs infrared images over the top view of measured structure shown in Figure 6- 32.

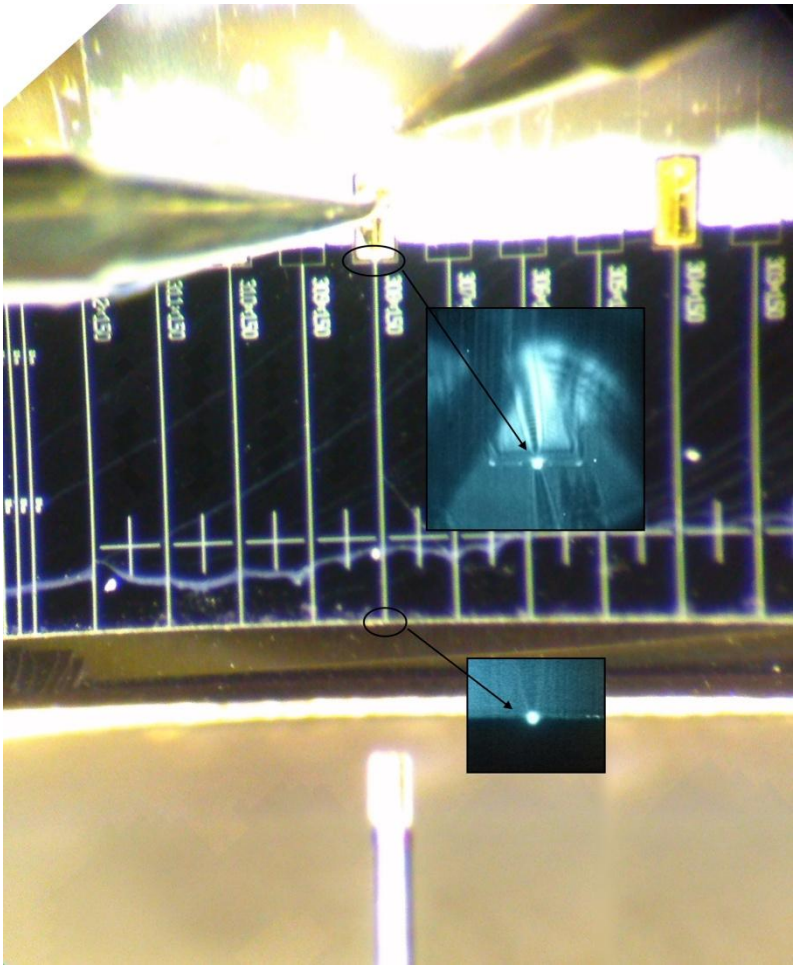


Figure 6- 20: IR images used as insets on a photo taken from the top-view of an integrated device under test, depicting where the infrared images were taken from.

6.5. Mode Shape Simulations

In order to determine the output mode shape as well as effective refractive indices, 2D vectorial FDTD simulations were carried out for laser diode and dielectric waveguides. For these simulations the mode solver software developed by Milos Popovic during his PhD at MIT was used, which was kindly shared with our group by Dr. Popovic [97].

In the following subsections, first the laser diode ridge waveguide modes are simulated and displayed. Then, the same will be carried out for the SiON/SiO_2 waveguide. At last, the first fundamental mode of the dielectric waveguide is propagated in air to find the mode shape that photodetector or fibers see, and by that the beam divergence angle is calculated.

6.5.1. Laser Ridge Waveguide Modes

In order to simulate the guided modes of the laser ridge waveguide, refractive indices for InGaAs and InGaAsP layers were derived from compound material data base graphs, for their corresponding E_g and being lattice matched to InP for the unstrained layers. Unknown mole fractions of the layers were derived in the same manner. For strained layers of QW and the barriers, the same refractive index of the upper and lower InGaAsP core was used. Table 6- 3 shows the layer sequence, the function, and the refractive index used for each layer in the simulations here. The resulting simulated structure is shown in Figure 6- 21 where ohmic contacts are neglected and layers with similar refractive indices are lumped together and treated as one. Also, the palanarization BCB layer is included similar to the fabricated lasers[6].

[6] Simulations both with and without the BCB planarization layer were carried out and did not show significant difference in the results. Since the presence of BCB layer is closer to the actually of the laser platelets, the results of this case only will be shown here.

#	Material Type	D	Function	Thickness	λ (μm)	Eg	x,y	n
9	$In_{(1-x)}\ Ga_x\ As$	P^+	p-contact	200nm	-	-	x=0.53	3.166
8	InP	P	Ridge	1.5μm	0.92	1.35	-	3.167
7	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	P	Etch Stop	7nm	1.3	0.95	x=0.27 y=0.58	3.384
6	InP	P	Upper Clad	200nm	0.92	1.35		3.167
5	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Upper Core	110nm	-	-	x=0.23 y=0.52	3.352
4	$4 \times In_{(1-x)}\ Ga_x\ As$	U	QW	24nm total	1.75	-	-	
	$3 \times In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Barriers	27nm total	1.25	0.99	-	
3	$In_{(1-x)}\ Ga_x\ As_y\ P_{(1-y)}$	U	Lower Core	110nm	1.25	0.99	x=0.23 y=0.52	
2	InP	N	Lower Clad	2.8μm	0.92	1.35	-	3.167
1	Thinned $In_{(1-x)}\ Ga_x\ As$	N^+	Etch Stop	300nm	-	-	x=0.53	3.166
0	Backside metallization	-	n-contact	370nm	-	-	-	-

Table 6- 3: Summary of laser layer sequence and extracted refractive index for each layer.

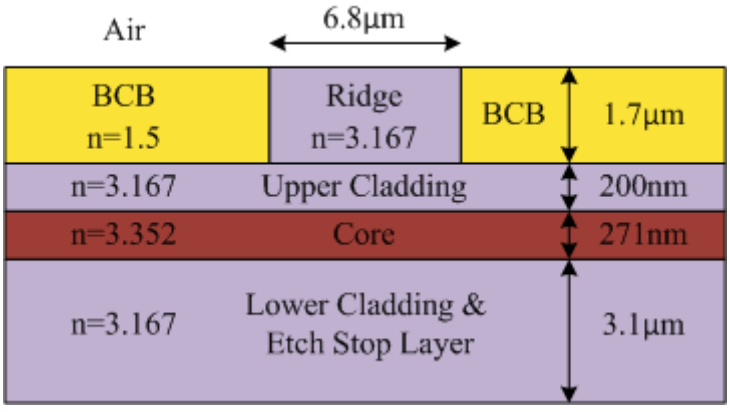


Figure 6- 21: Simplified simulated laser ridge structure based on the layer sequence of Table 6- 3.

All the simulations in this section are done for λ=1.55μm. For the laser ridge guide, 30 modes were simulated and 10 were graphed. Figure 6- 22 and Figure 6- 23 depict the first two modes of the laser ridge structure of Figure 6- 21. In each graph, the top left hand side of the image shows the refractive index profile of the structure, and the three other subplots show the real part of E_x, E_y and imaginary part of E_z. Modes 1 to 6 are confined under the

ridge, however from mode 7 above the mode is dispersed beyond the ridge as well, as shown in Figure 6- 24. It might be tempting to relate this to what was observed in Figure 6- 17, as the area outside the ridge is also illuminated. However this might also be due to reflection by the shiny edges of the laser platelet as can be seen in the two left and right corner edges of Figure 6- 17.

Also it is noticed that the propagation constants of the first four simulated modes do not differ up to 4 decimal points if the BCB layer is present in the simulated structure or if it is replaced by air. This verifies that including the BCB layer for the purpose of planarization does not affect the optical mode shape under the ridge. From the propagation constants of each mode, effective refractive indices were extracted and shown in Table 6- 4 for the first four modes. Note that n_{eff1} from this table will be used later on for the calculation of effective cavity length based on the spacing of axial modes of the laser Fabry Perot cavity.

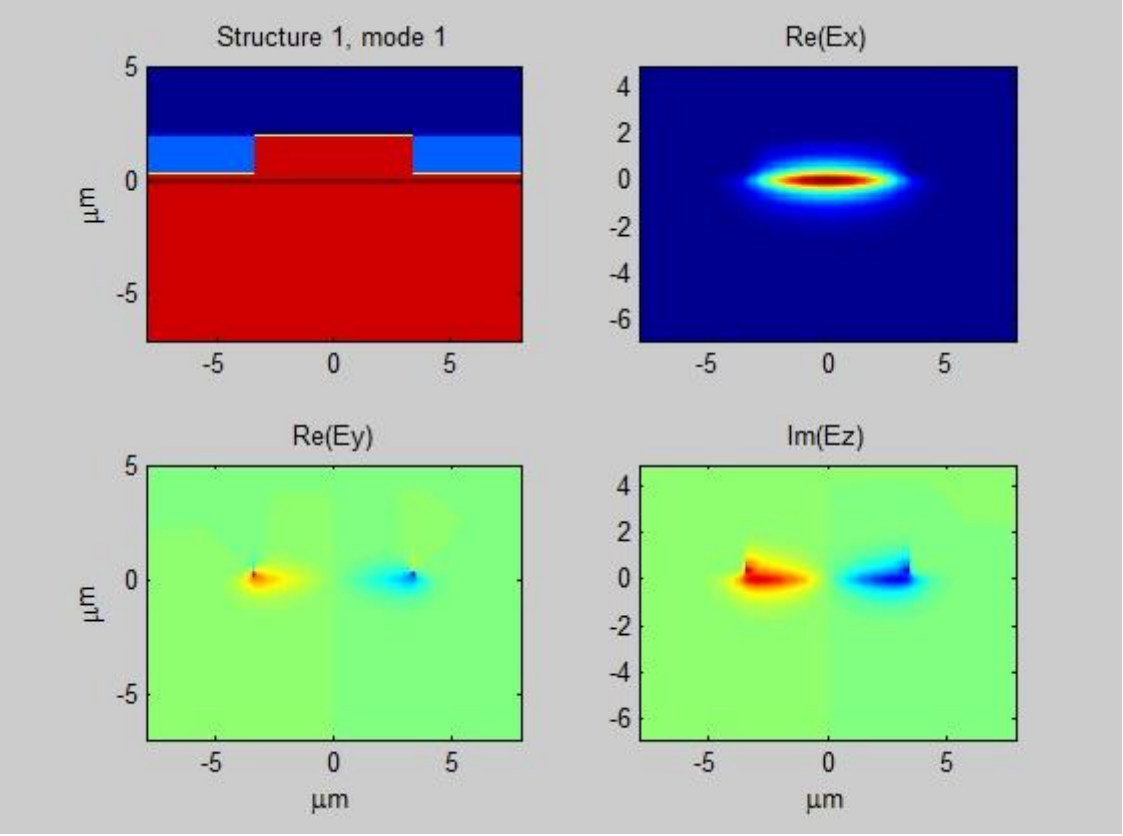


Figure 6- 22: Simulated first mode of the laser ridge structure with a strong E_x component.

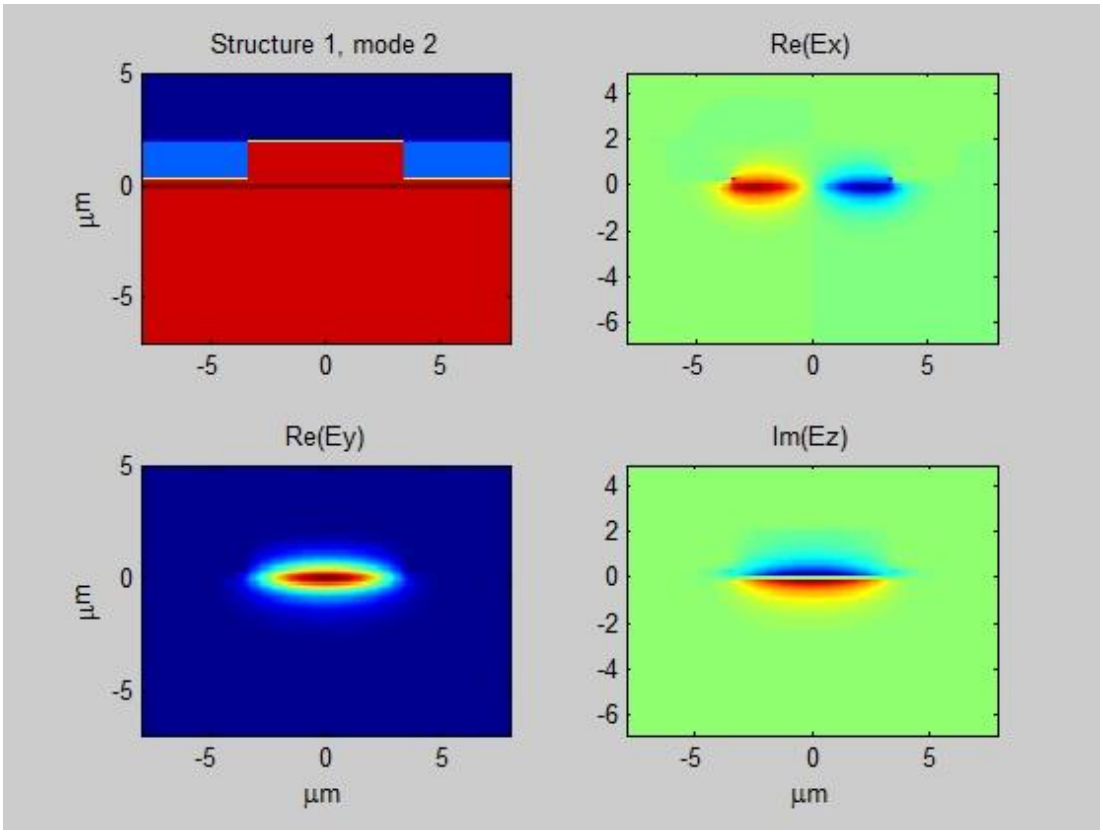


Figure 6- 23: Simulated second mode of the laser ridge structure with a major E_y component.

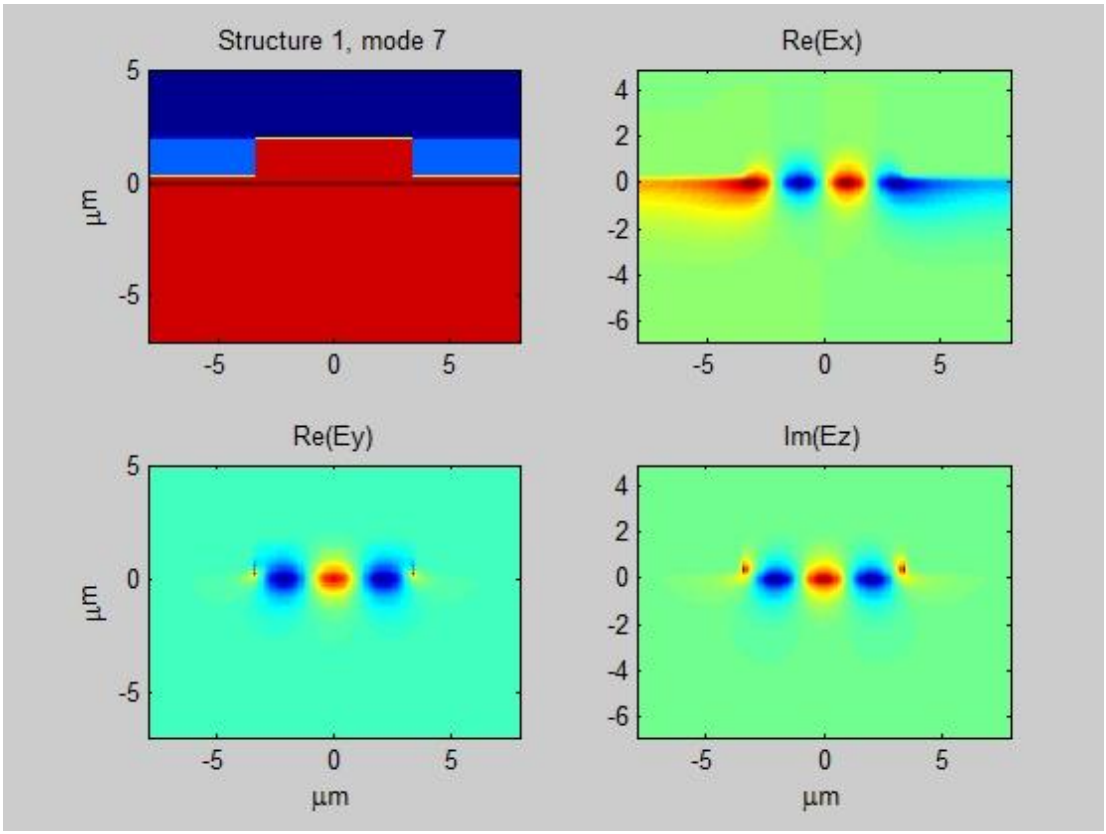


Figure 6- 24: Simulated mode #7 of the laser ridge structure. From this mode above, the light is not confined under the ridge anymore.

Mode #	n_{eff}
1	3.1944
2	3.1919
3	3.1897
4	3.1870

Table 6- 4: Effective indices calculated for the first 4 modes of the laser ridge waveguide.

6.5.2. Fundamental Modes of Dielectric Waveguide

Simulating the real structure of the dielectric waveguide i.e. including the Si substrate had proven to be challenging since due to the high refractive index of silicon (n=3.43), the calculated modes have their most significant field strength in the substrate rather than in the SiON core as shown in Figure 6- 25. However this would not be the case in reality since the guided modes of the structure are being calculated without any regard to the launch field. Since for the actual SiON/SiO_2 waveguides, their input field is provided by the vertically aligned laser ridge waveguide, the SiON core will see the input mode and thus the excited modes will guide through it and not the substrate, which is not excited by any input launch. Therefore, in order to find the fundamental modes of the dielectric waveguide, the Si substrate was ignored and the substrate was assumed to be the same as the lower cladding. Figure 6- 26 shows the simple structure of the dielectric waveguide simulated here, where the core has w=1.7µm, h=0.55µm and n_{core}=1.6, upper and lower claddings have h=3µm (for B6-4 batch used in integration) and $n_{cladding}$=1.46. The mode shape of the first two fundamental modes (TE and TM polarizations) is depicted in Figure 6- 27. Again, by having the calculated propagation constants, effective refractive indices can be calculated with:

$$\beta = \frac{2\pi}{\lambda_0 / n_{eff}} \quad \rightarrow \quad n_{eff} = \frac{\lambda_0 \beta}{2\pi}$$

Table 6- 5 shows the effective refractive indices for the first two fundamental modes of this waveguide.

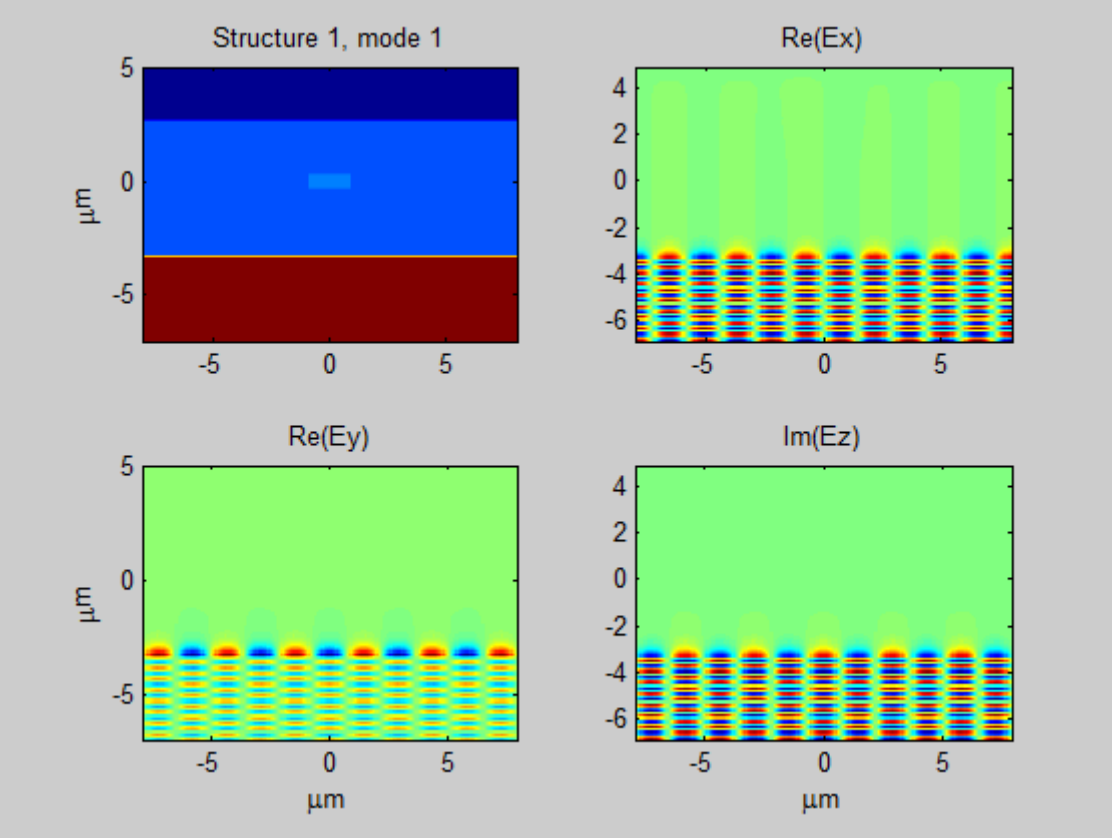


Figure 6- 25: The calculated first mode of the dielectric waveguide when high index Si substrate is present.

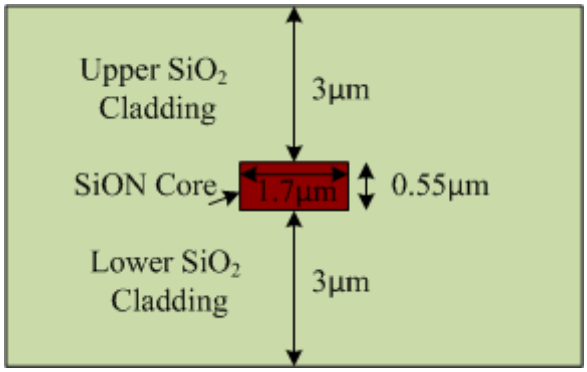


Figure 6- 26: Simulated dielectric waveguide structure.

Mode #	**n_{eff}**
1	1.4868
2	1.4824

Table 6- 5: Effective refractive index for dielectric waveguide modes.

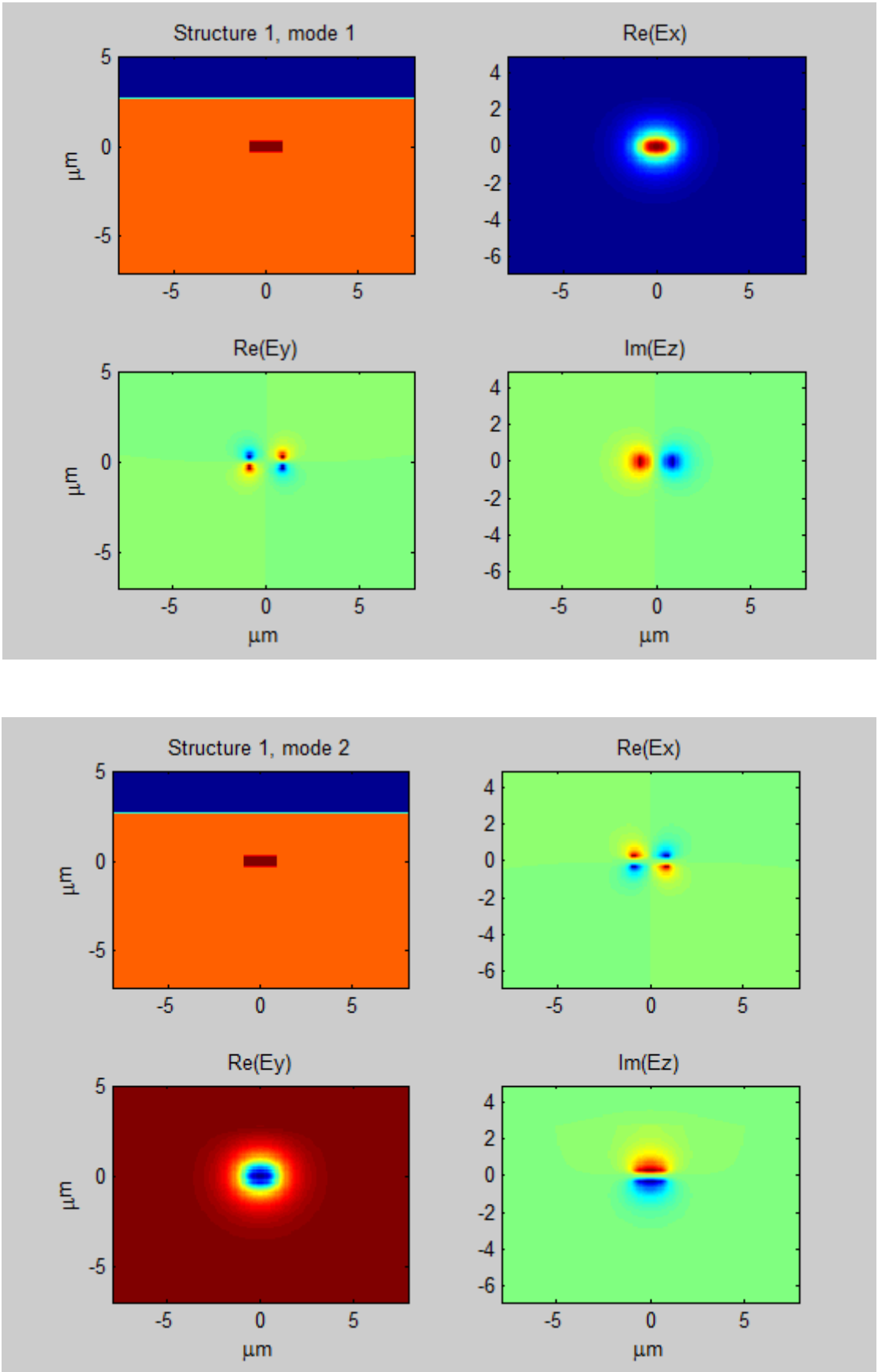


Figure 6- 27: Simulated fundamental modes of the SiON/SiO_2 dielectric waveguide.

6.5.3. Fundamental Modes Coupling Integral of Two Waveguides

Once the major modes of the laser ridge waveguide and dielectric waveguide are calculated, the E_x and E_y components of each mode are stored and through a separate script their overlap integrals are calculated. This process is shown in Figure 6- 27, where the first mode is shown in the left column and the second mode in the right column. In each column the first image is the dielectric waveguide mode shape, the second image shows the laser ridge waveguide mode and on the third row these two modes are multiplied to give an overlap field. Then the norm of this overlap is calculated and is divided by the norm of dielectric waveguide and laser waveguide fields, resulting in the overlap integral for two modes.

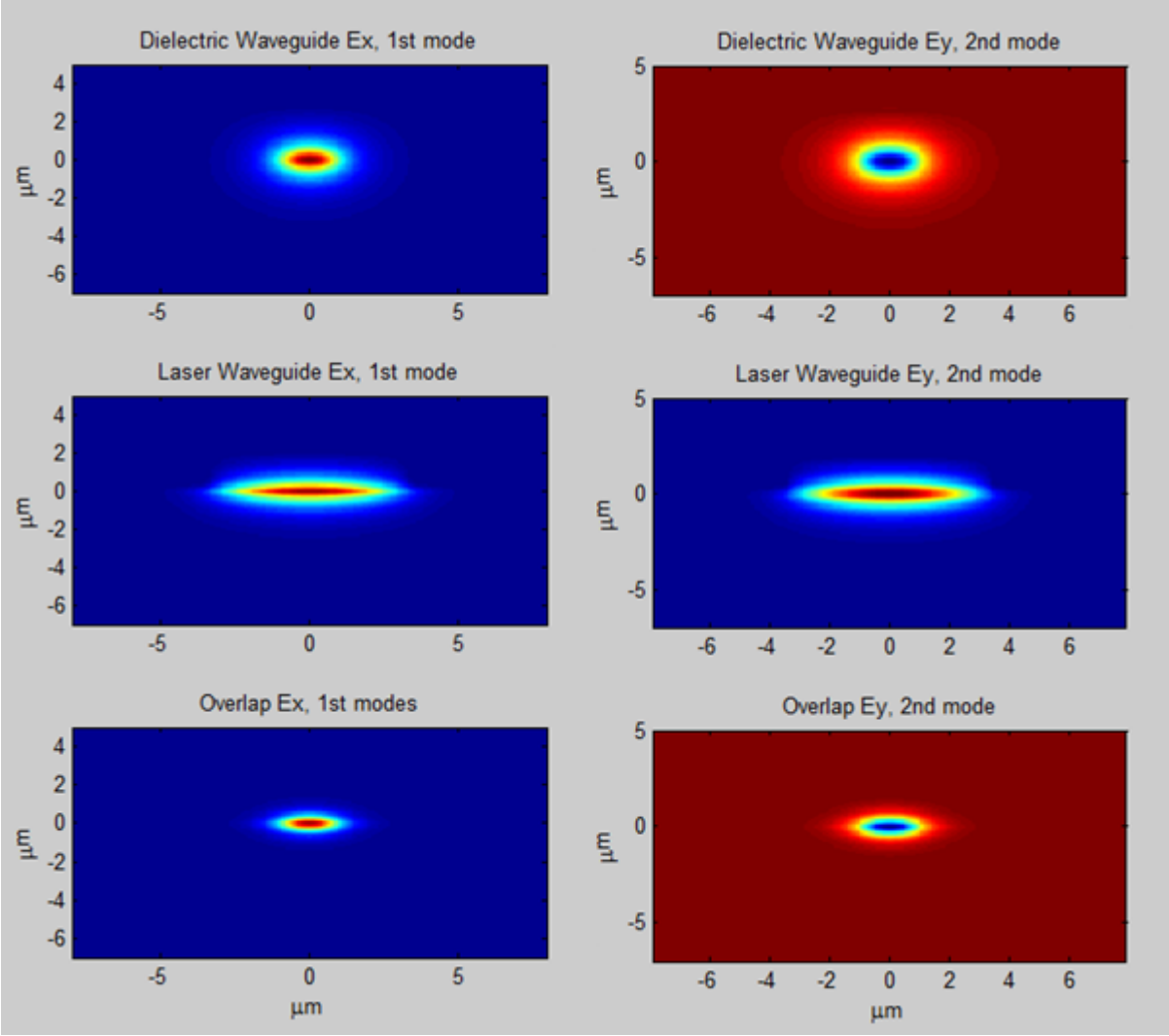


Figure 6- 28: Field overlap of dielectric guide and laser guide mode shapes. The first column corresponds to the first mode of the two guides with strong E_x component, and the second column corresponds to the same process done for the second mode with dominant E_y.

The overlap integral calculated for the first mode (E_x) is 0.0413 and for the second mode (E_y) it is found to be 0.0386.

It is clear that such a small overlap of the fundamental modes comes from the fact that the widths of laser ridge guide and dielectric waveguide are quite different in the current generation of fabricated components, i.e. 6.8μm and 1.7μm respectively. In the next generation of devices, the width of the laser ridge will be made smaller which not only would help in the increased mode shape match with the dielectric waveguide fundamental modes, but also would be beneficial in limiting the transverse modes that the laser ridge structure supports, in order to achieve single mode operation while lasing.

Also, the ≈4% value of overlap integral calculated here implies about 14dB coupling loss between the first fundamental mode of the laser and the dielectric waveguides, which is dramatically higher from the 0.5-6dB losses that were seen experimentally, as shown in Table 6- 6, for different lasers with various horizontal alignments. This discrepancy implies that inter-coupling of higher order transverse mode takes place as well, and that the simple overlap calculations between the fundamental modes of the two guides does not give a full picture of what is happening in reality. Furthermore, the coupling integral found here is for the end-fire coupling case. We believe that the presence of the gap helps the laser guide mode to open vertically and have a better overlap with the larger height of the dielectric waveguide. Therefore, in order to compare the results of the simulations carried out here to the measurement data, one should let the output mode of the laser propagate in air for various gap widths, which will model the actual device in a better way.

6.5.4. Far Field Output Mode Shape

Another motivation in finding the fundamental modes of the dielectric waveguide is to find the mode shape that a photodetector or output fiber sees. Specifically, knowing the size of the output beam helps in determining whether the large area PD is collecting most of the beam or not. Furthermore, the beam divergence angle derived in this section will be used in coupling loss estimations later in this chapter.

For this purpose, the fundamental mode shape of the dielectric waveguide was saved and then through non-paraxial propagation formulation, its Fraunhofer far field distribution is found. Essentially for $Z>2D^2/\lambda$ (where D is the largest dimension of the source), far-field or Fraunhofer diffraction applies. For far field, the wave amplitude attenuates with 1/r and the power with $1/r^2$. Since the beam emitted by laser diodes and similar dimension dielectric

waveguides is quite divergent, paraxial approximation is not valid when calculating free space propagation of the fields. Instead the following exact non-paraxial formulation must be used:

$$U(x,y,z) = 2D \iint U_0(x_0,y_0,z_0) \times h(x-x_0, y-y_0, z-z_0)dx_0dy_0$$

$$h(x-x_0, y-y_0, z-z_0) = \frac{j}{\lambda r} e^{-jkr}$$

$$r = \sqrt{(x-x_0)^2 + (y-y_0)^2 + (z-z_0)^2}$$

In scripting this formulation, the fundamental mode of the dielectric waveguide found earlier is used as U_0 and is propagated for z=5mm. Again, as before, λ_0=1.55µm and the grid discretization for far field calculation is 25µm[7]. The resulting far field mode distribution after z=5mm of propagation is shown in Figure 6- 29. The near field is compared side by side to the far field in Figure 6- 30.

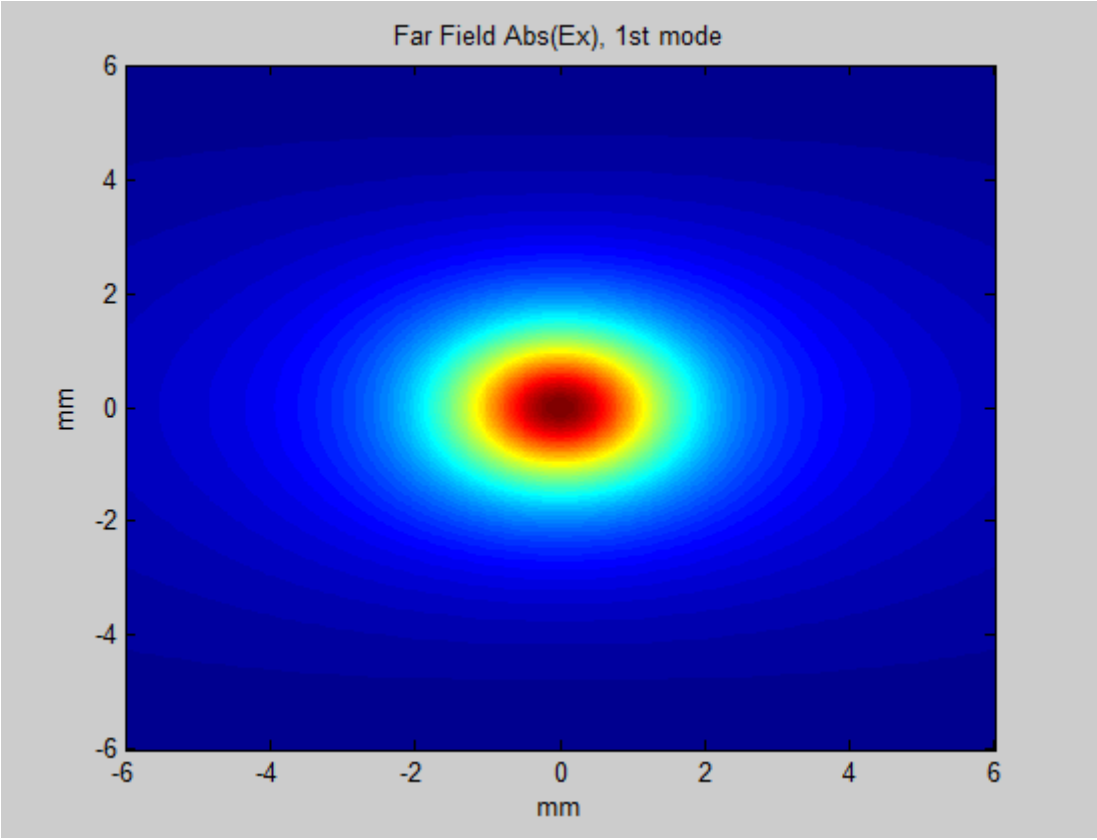


Figure 6- 29: The far field mode shape of the output beam from the dielectric waveguide after z=5mm of propagation.

[7] Simulating this propagation with 25µm discretization takes about an hour, in contrast to 100s when 100µm grid size is used.

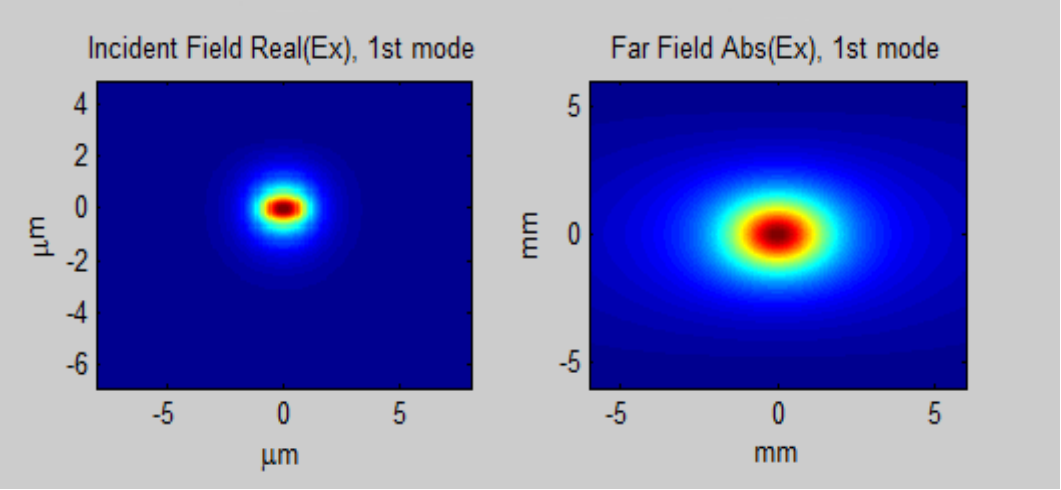


Figure 6- 30: Near field and far field distributions. For incident field, the fundamental mode of SiON dielectric waveguide is used and the far field shows the distribution that a detector/fiber placed at 5mm from the output facet of the chip will see.

From the far field mode shape, the divergence angle of the integrated structure can be calculated. Usually for laser diodes and comparable size waveguides, the half-angle-beam divergence is reported and is calculated through $\theta = \arctan(y/z)$, as shown in Figure 6- 31.

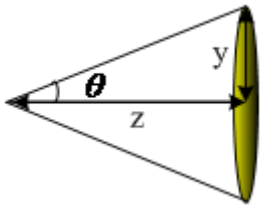


Figure 6- 31: Schematic showing how half-beam-divergence angle is calculated.

From Figure 6- 29, it can be concluded that $\theta = \tan^{-1}(3.5\text{mm}/5\text{mm}) = 35^{\circ}$, which is highly consistent with the typical divergence angle of 30° that is reported for laser diodes or waveguides of micron size. With such divergent beam, collimating lenses with wide numerical aperture should be used to collect the output light of these devices.

Since the Ge PD used in the measurements in this chapter has a large collection area with a diameter of D=5mm, a collimating lens was not used with it. From the calculations above it was concluded that after 5mm of propagation through air, the beam has a diameter of about 3.5mm×2=7mm, therefore most of the beam is collected by the large area Ge PD.

6.6. CW Spectrum of Integrated Lasers

Once the CW lasing for integrated lasers was verified, the output light was collected through a multi-mode fiber connected to an optical spectrum analyzer (OSA).

Figure 6- 32 shows a top-view photograph of this structure where the two integrated lasers in recesses are noticeable through their gold top contacts. Also two electrical probes that provide the drive current can be seen. One of the probes is on the laser platelet's top p-contact, and the other sits somewhere on the Al/In bonding layer which is connected to the laser's backside n-contact at the bottom of the recess. The laser emitted light is coupled to the SiON dielectric waveguide and at the end of the waveguide the emitted light from the chip is collected by a multimode fiber shown at the bottom of the image.

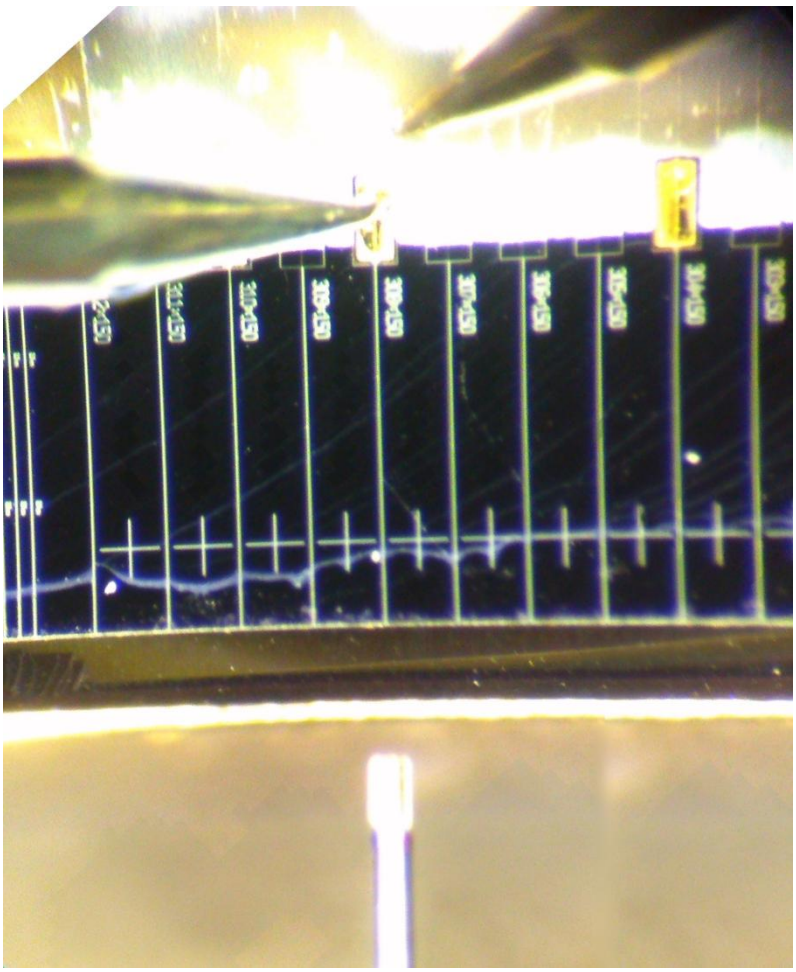


Figure 6- 32: Photograph of the top-view of the measurement setup, showing probes driving the laser integrated in a 308µm recess, the dielectric waveguide that it is coupled to and finally the fiber that collects the light emitted from the chip.

Below threshold (I=10mA) no lasing mode is seen as shown in Figure 6- 33. However as the input current is raised, right at threshold (I=19mA) a single mode starts to win over the rest of modes as shown in Figure 6- 34 with the wavelength of λ=1543.6nm.

As the current is increased above threshold, the winning mode gets stronger, increasing MSR (e.g. Figure 6- 35) until it reaches a steady value. However, through increasing the drive, at certain currents two significant modes compete for lasing as shown in Figure 6- 36. Increasing the current further favors one of these modes, the laser becomes single mode again (see Figure 6- 37) and stays so for some current span (Figure 6- 38), before the lasing becomes consistently multi-mode at higher current levels above 31mA. As an example of such double-mode lasing Figure 6- 39 was measured with I=40mA ($I/I_{th}\approx 2$) where two modes consistently lase with wavelengths of λ_{peak1}=1554.8nm and λ_{peak2}=1554.2nm.

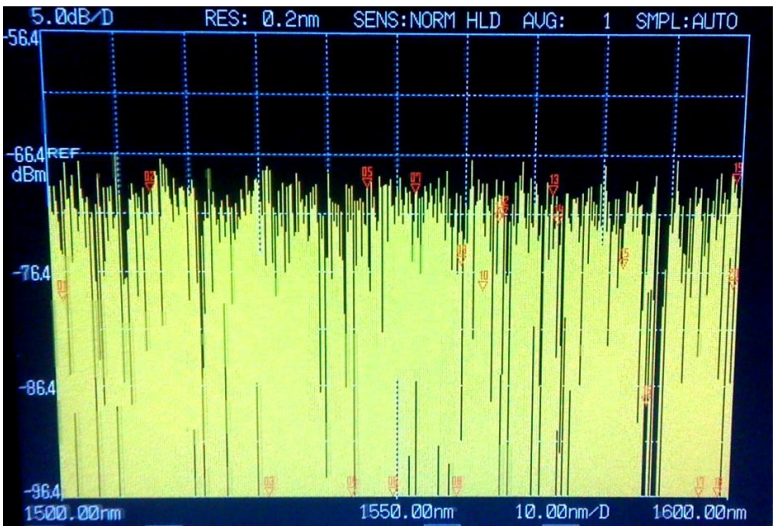


Figure 6- 33: OSA spectrum snapshot for below threshold (I=10mA).

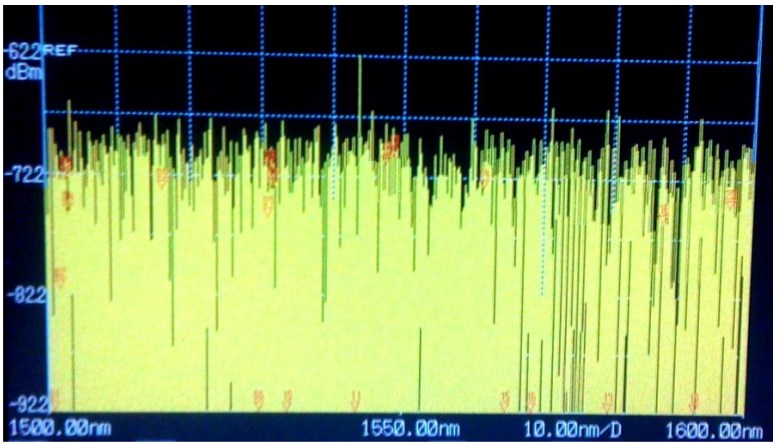


Figure 6- 34: Lasing spectrum right at threshold (I=19mA). A winning mode starts to show face with λ_{peak}=1543.6nm.

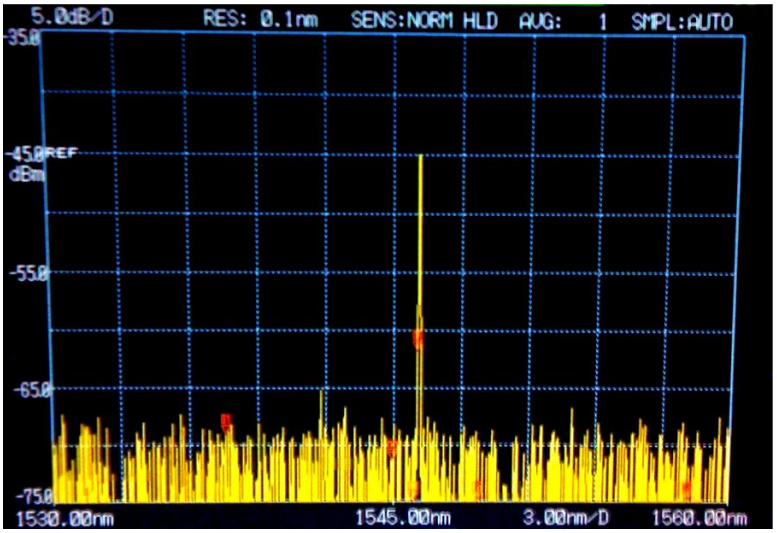


Figure 6- 35: CW spectrum at I=24mA, winning mode wavelength is λ_{peak}=1546.1nm.

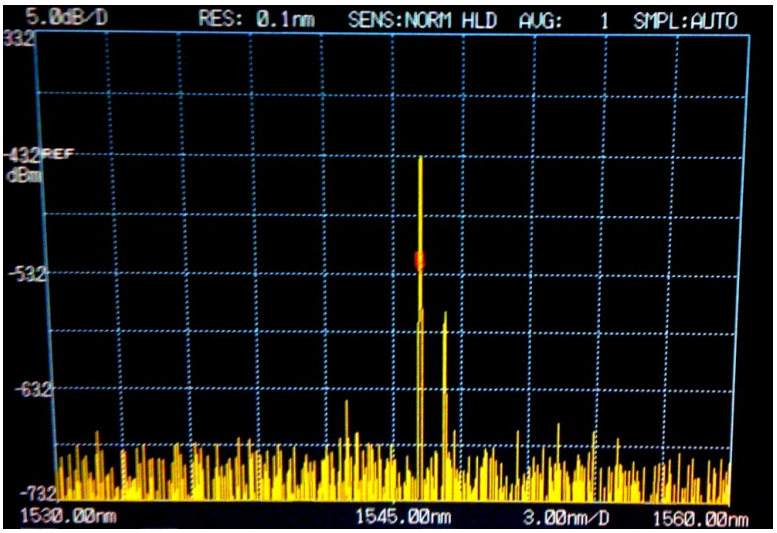


Figure 6- 36: Multi modes compete in lasing for certain currents, for instance here at I=25mA. Wavelength peaks of the two significant modes are λ_{peak1}=1546.2nm and λ_{peak2}=1547.2nm.

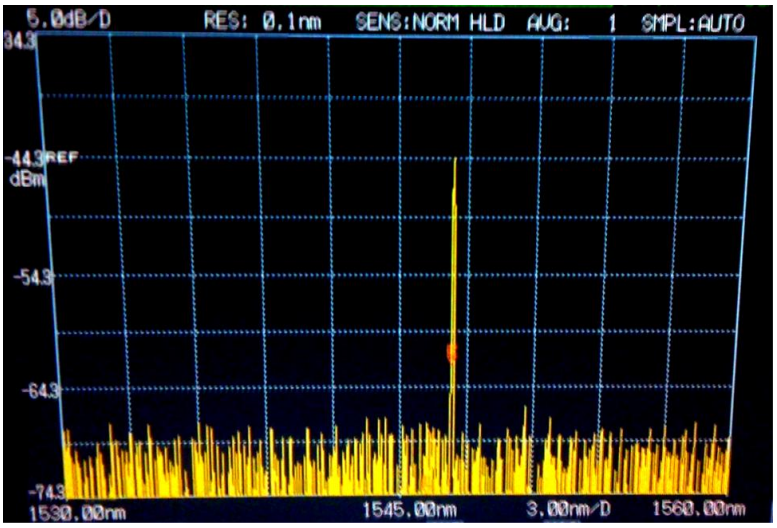


Figure 6- 37: Lasing becomes single mode again at I=26mA (and stays so until I=31mA). Here λ_{peak}= 1547.3nm.

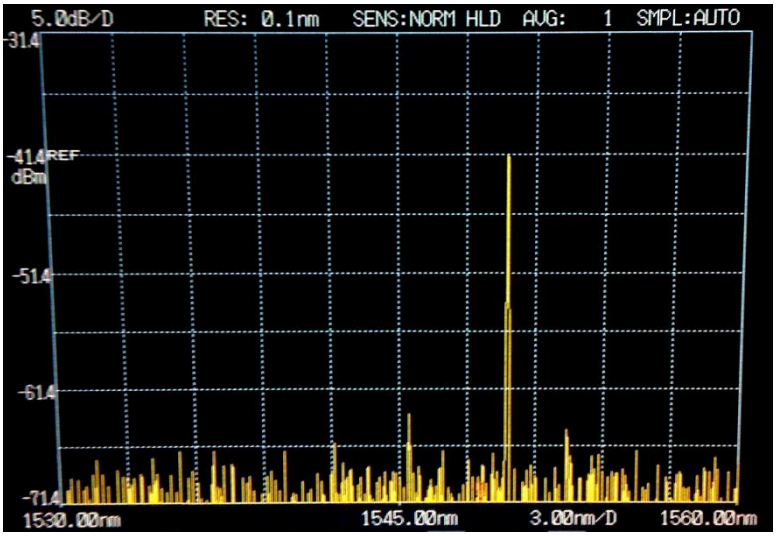


Figure 6- 38: Single mode operation at I=30mA with MSR≈25dB and λ_{peak}=1549.7nm.

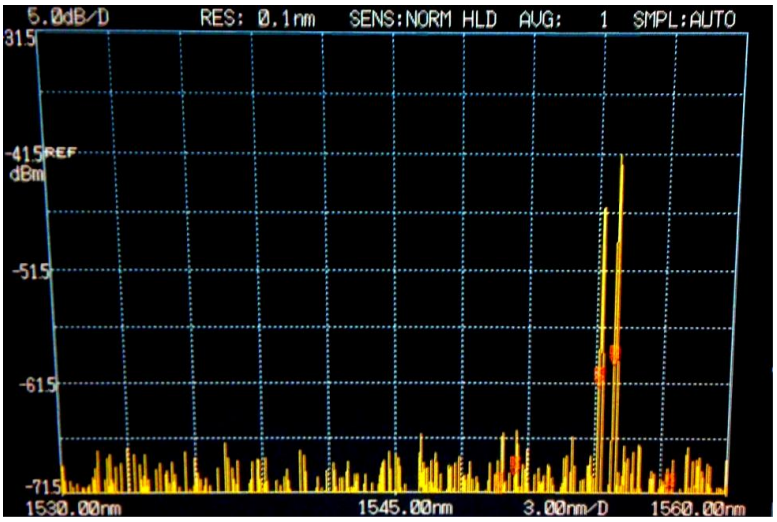


Figure 6- 39: Two modes lasing in high above threshold current of I=40mA with wavelengths of λ_{peak1}=1554.8nm and λ_{peak2}=1554.2nm.

6.6.1. Fabry Perot Cavity Mode Hopping vs. Current

In order to capture all the information of modes that pop up competing for lasing, later get suppressed down, and their wavelength shift, the wavelength of the significant modes are plotted together versus current as shown in Figure 6- 40. Modes within 15dB of the strongest mode were included in this plot.

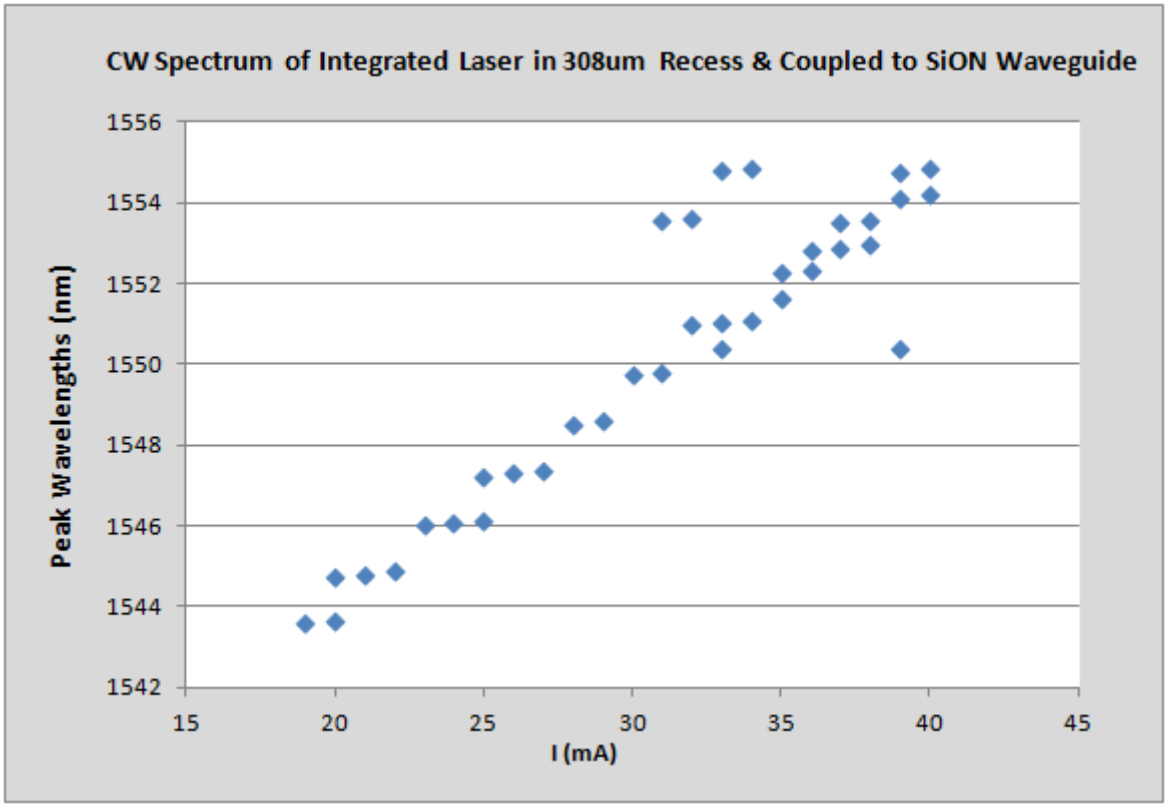


Figure 6- 40: Lasing wavelengths at each CW drive current showing mode hopping behavior.

Figure 6- 40 is in fact quite interesting since it shows modes shifting in straight lines slanted slightly upward, and then hoping to the next line up. Understanding these two behaviors gives valuable insight to mode-hopping phenomena observed and well-understood in Fabry Perot lasers. Basically, the shift along one slanted straight line seen in Figure 6- 40 is due to thermal expansion of the Fabry Perot cavity which slowly shifts the longitudinal cavity modes. Along with this phenomenon, another effect takes place as well, which is due to the larger reduction of the bandgap of the MQWs and barriers as a result of heating, which results in the relatively more rapid red shift of gain spectrum. At some point the gain curve shifts to a degree that another cavity mode sees higher gain and is favored over the previous lasing mode and thus a hop happens to the next higher slanted line. And the same process repeats. Of course this description only concerns longitudinal modes due to the Fabry Perot cavity length. If the laser ridge and dielectric waveguide support multiple transverse modes, there will be various propagation constants based on the longitudinal and transverse mode number for each existing mode, which might get a chance of lasing at higher currents.

It might be also helpful to see in Figure 6- 40 which modes are primary, having the highest power, and which are secondary at each wavelength. In Figure 6- 41 the primary modes are shown in blue diamonds and secondary modes are shown in red triangles.

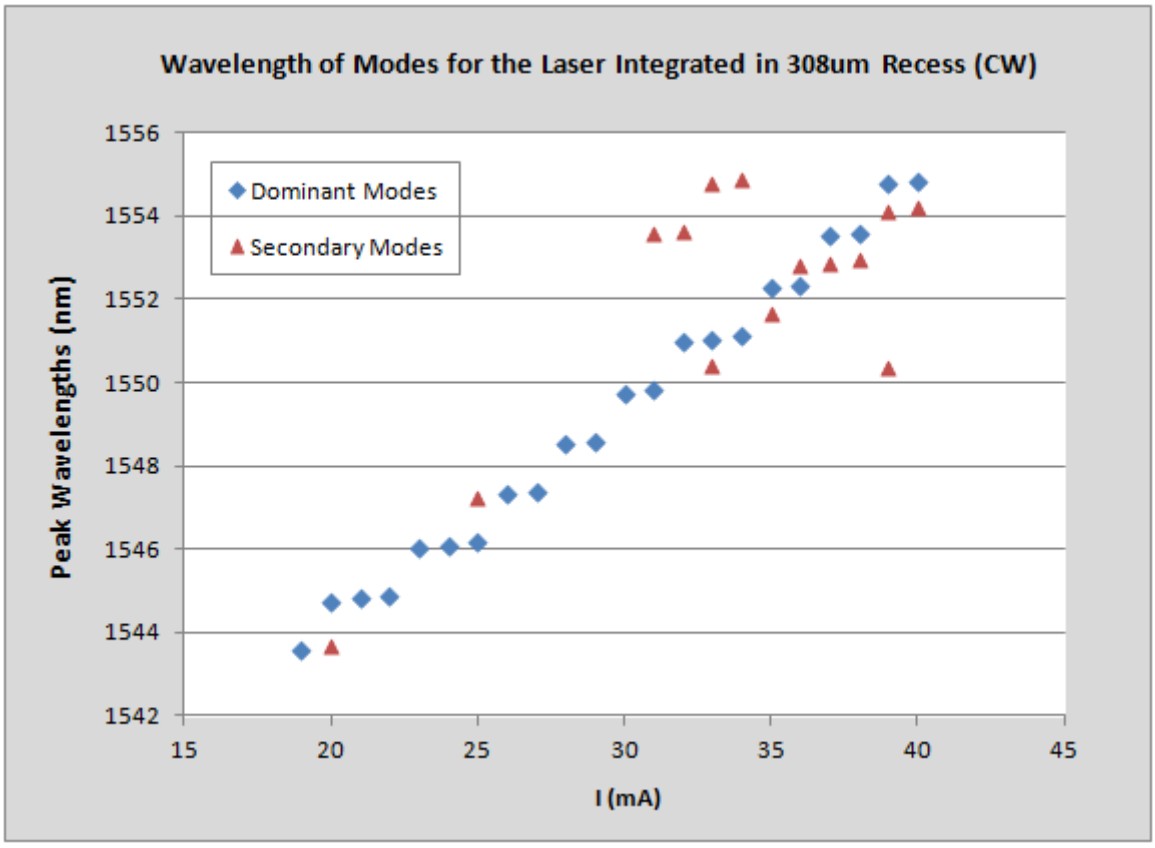


Figure 6- 41: Primary and secondary modes competing to lase at each current.

As mentioned before, one factor that contributed to a mode moving along a slanted line seen in Figure 6- 41 is mode shift due to cavity thermal expansion. And when the gain curve shifts enough due to red shift from heating, another longitudinal mode is selected which accounts for a jump between the two lines. Such a jump can be noticed for instance at I=20mA or I=25mA. At I=25mA for instance, the primary mode is the previous axial mode, while the secondary mode (the next axial mode seeing enough gain to lase) is popping up as the secondary mode. Increasing the current to I=26 or 27mA, this new mode becomes the single mode shifting with cavity expansion.

This pattern of wavelength shifting along clean slanted lines and hopping to one next holds until about I=30mA. Above 30mA, a new family of modes starts to compete for lasing as seen in Figure 6- 41. These new modes can correspond to higher order transverse modes of the laser ridge waveguide. The verification of the nature of these extra modes needs further study.

6.6.2. Effective Cavity Length

One more piece of very useful information that can be derived from Figure 6- 41 is the effective cavity length[8], which can be extracted from the wavelength spacing between the lines that modes jump to. For instance, at I=25mA, the spacing between the two lines (i.e. $\Delta\lambda$ between the primary and secondary modes), can give the effective length, L_{eff}, of the cavity. Specifically at I=25mA, the two modes have wavelengths of λ_1=1546.155nm and λ_2=1547.245nm resulting in $\Delta\lambda$=1.09nm.

Based on the constructive interference of a mode with its roundtrip propagated version, the wavelength spacing of cavity modes can be found as:

$$\Delta\lambda = \frac{\lambda_1\lambda_2}{2nL_{eff}} \qquad \text{(Equation 6- 1)}$$

The calculated fundamental mode of the laser ridge waveguide has an effective refractive index of n_{eff1}=3.1944, which using Equation 6- 1, with yield L_{eff}=343.5µm. This value for the effective cavity length is quite large and calls into question the accuracy of n_{eff} and the precision of $\Delta\lambda$.

With a 0.1nm variation[9] in the reading of $\Delta\lambda$, a 29-35µm variation in L_{eff} results (specifically, $\Delta\lambda$=1.09+0.1nm → L_{eff}=314.7µm and $\Delta\lambda$=1.09-0.1nm → L_{eff}=378.2µm). Furthermore, if the group propagation index of n_g=3.6 is used for n in Equation 6- 1, which is the value extracted from the mode spacing of a non-integrated conventionally cleaved laser in [60], then the effective length becomes L_{eff}=304.8µm, which is well in range with the 305µm laser cavity length with 1µm and 2µm air gaps integrated in the 308µm recess.

Because of the strong sensitivity of L_{eff} to refractive index and $\Delta\lambda$, both of these factors need to be more accurately estimated to achieve a more precise value for L_{eff}. For instance, using a finer resolution OSA is necessary for a more precise spectral measurement to achieve a better estimate of $\Delta\lambda$.

In that case, Equation 6- 1 can be refined further to include the different propagation constants in the active and passive sections of aggregate cavity [98] as:

$$\Delta\lambda = \frac{\lambda_1\lambda_2}{2(n_aL_a + n_pL_{p,eff})}$$

[8] Knowing the effective length will help us to determine if the micro-cleaved laser platelet cavity dominates the mode spectrum, or if the recess walls and/or some of the waveguide are part of what the lasing mode sees in its round trip pass inside the composite cavity. It is anticipated that the first possibility is more probable, however this needs to be confirmed, and modes spacing in the spectrum can provide a good estimate to determine L_{eff} for that purpose.

[9] The resolution of SOA in these measurements has been 0.1nm.

where L_a and n_a correspond to the active part of the cavity (i.e. the laser platelet), and n_p and L_p refer to the passive part of the cavity (here the air gap and SiON dielectric waveguide). One complexity is the passive section of the external cavity has two segments (gap and waveguide) each with a different refractive index. Therefore one can modify the equation above by replacing ($n_p \times L_{p,eff}$) term with ($n_g \times L_{g,eff} + n_{wg} \times L_{wg,eff}$) in order to incorporate the effect of both segments of the passive external cavity in this application; where subscript g stands for gap and wg stands for waveguide.

6.7. Mode Suppression in Integrated Lasers

From the spectrum of continuous wave operation of laser integrated in 308µm recess, with a drive current of I=30mA, the Mode Suppression Ratio (MSR) is about 25dB as seen in Figure 6- 42.

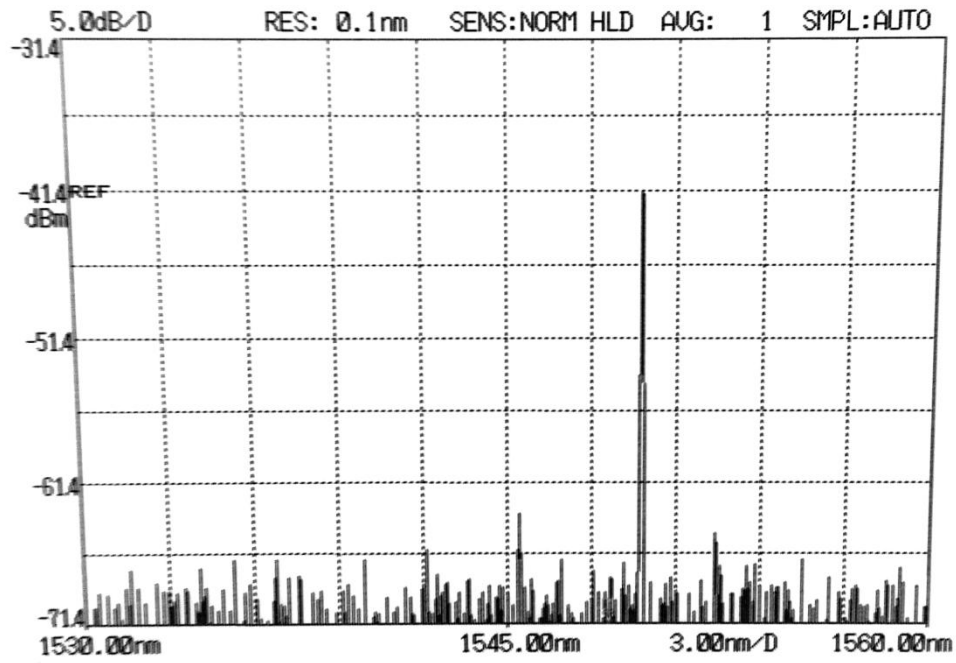


Figure 6- 42: MSR≈25dB seen from the CW spectrum of the laser integrated in the 308µm recess, at I=30mA.

Observation of this level of MSR (25dB) is indeed interesting, as Fabry Perot lasers usually have much lower side mode suppression ratios on the order of 10dB [99].

In fact the spectrum of the non-integrated conventionally cleaved counterparts of the laser platelets used in this project have been measured by J. Rumpler in pp. 153 of [60] and the resulting spectrum for two different current levels is illustrated in Figure 6- 43 and Figure

6- 44. Since the threshold of this conventionally cleaved laser is 25mA, the spectrum at I=35mA shown in Figure 6- 43 is comparable to the one in Figure 6- 42, which is measured 11mA above threshold. One can see that the MSR of this non-integrated (and conventionally cleaved) laser is very small and at most 1dB. Therefore, the enhancement of MSR≈25dB seen in Figure 6- 42 is quite significant. By increasing the current above threshold, the MSR improves but it is still in the range of 10-15dB as shown in Figure 6- 44, which is measured well above threshold. Therefore it will be instructional to understand the source of the MSR improvement in the integrated lasers structure.

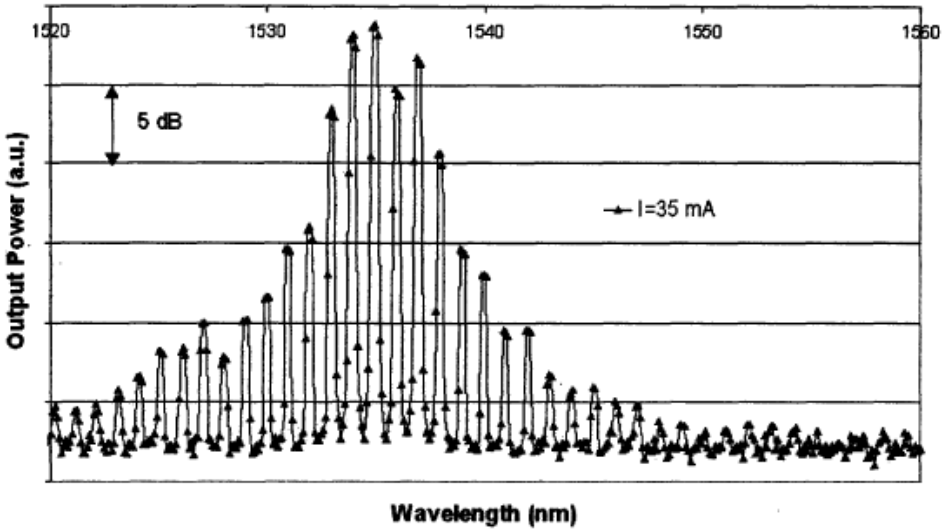


Figure 6- 43: Spectrum of a conventionally cleaved non-integrated laser at 10mA above threshold, pp. 153 of [60]. The spectrum shows a very limited MSR of about 1dB.

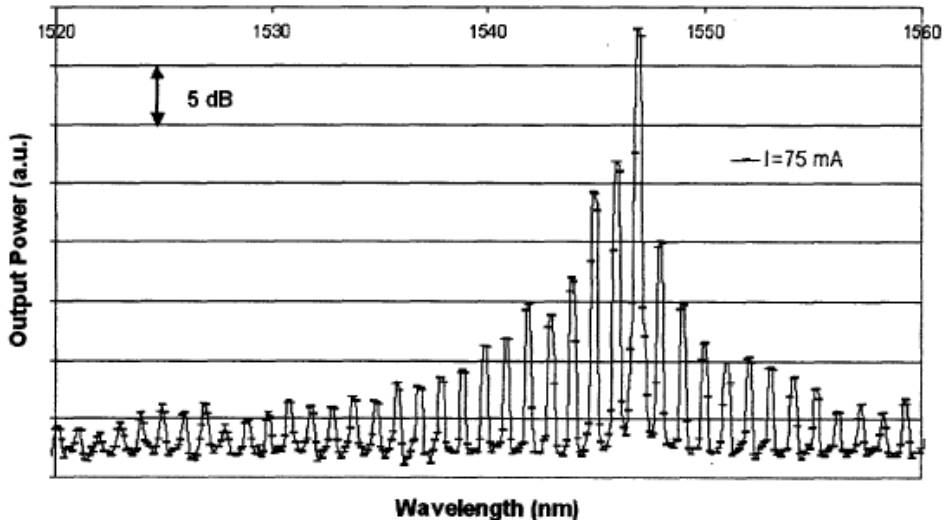


Figure 6- 44: Spectrum of a conventionally cleaved laser well above threshold, showing an upper limit of MSR≈10dB for these non-integrated lasers.

One theory that can explain the enhanced MSR in integrated lasers considers the frequency dependence of mirror loss, $\alpha_m(\lambda)$, that the Fabry Perot laser cavity sees looking into the external cavity of the gaps and SiON waveguide. In order to model this dependence, a three-mirror cavity model can be used. The implications of such a model on the mirror loss and therefore MSR will be explained in the following subsection.

6.7.1. Three Mirror External Cavity Model

One possible way to model the effect of air gap and reflection from the SiON waveguide on the effective reflection seen by the laser Fabry Perot cavity is to use a relatively simple three-mirror cavity model [101]. The schematic shown in Figure 6- 45 illustrates this model, in which the active laser cavity with a length of L_a, sees a Fresnel reflection r_2 from the passive section, i.e. the air gap as shown in Figure 6- 47. By the same token, a Fresnel reflection of r_3 is seen going from the air gap to the SiON dielectric waveguide. The advantage of the three-mirror cavity model is that all the effects of the external cavity can be lumped into one effective reflection, r_{eff}, that is seen at the active-passive segments facet, as shown in Figure 6- 46.

Based on this model, the effective reflection seen from the laser active segment looking into the passive segment is

$$r_{eff} = r_2 + \frac{t_2^2 r_3 e^{-2j\beta_p L_p}}{1 + r_2 r_3 e^{-2j\beta_p L_p}} \qquad \text{(Equation 6- 2)}$$

where the strong frequency dependent nature of r_{eff} is evident (from the term β_p). Consequently, the magnitude of r_{eff} yields the mirror loss for the composite cavity through

$$\alpha_m = \frac{1}{L_a} \ln \frac{1}{r_1 \, | r_{eff} |} \qquad \text{(Equation 6- 3)}$$

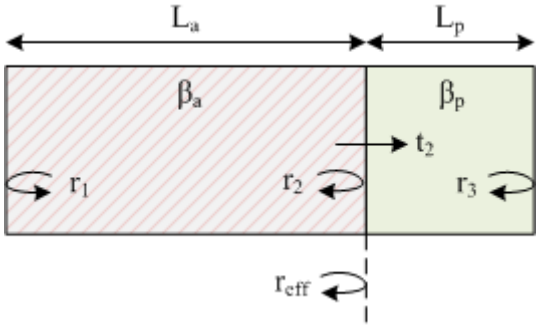


Figure 6- 45: Schematic showing the three mirror cavity model.

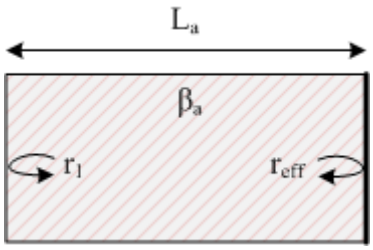


Figure 6- 46: The three-mirror cavity is simplified to one cavity with an r_{eff} modeling the impact of the external passive segment.

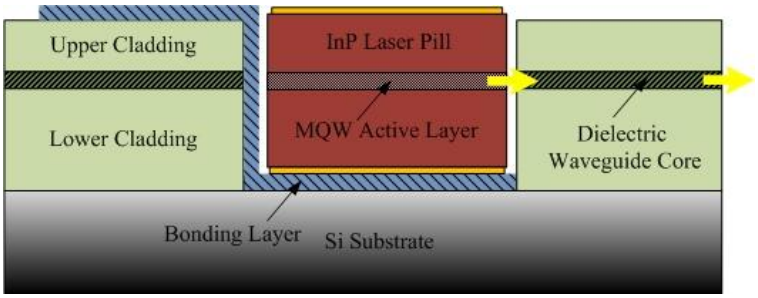


Figure 6- 47: Schematic of integrated laser platelet illustrating the fact that r_{eff} is only seen on the right side of the laser cavity, whereas on the left side all the emitted light from the laser is scattered by the rough surface of Al/In bonding layer covering that facet, and thus it is effectively not reflected back.

Note that the effective reflection model is only used at one side of the cavity where the light is coupled to the SiON dielectric waveguide (the right side of laser platelet in Figure 6- 47). For the other side of the cavity, since the emitted light from the laser reaches a fact that is covered by a rough Al/In layer surface (especially due to the In grains), it is expected that the beam is scattered and not reflected back, which is equivalent to assuming the air gap is infinite in this facet. Therefore, on the left facet of Figure 6- 47, basic Fresnel reflection coefficient of the laser beam opening to air, r_1, is used. In fact, this asymmetric nature of the integrated laser cavity will be used again in the calculation of the coupling loss, and is an important factor to take into consideration in the fabricated integrated structures.

6.7.2. MSR with Frequency Dependent Mirror Loss

In order to see how the frequency dependence of r_{eff} and thus α_m affects MSR, the gain and loss spectrum overlap with the cavity axial modes is shown in Figure 6- 48. It illustrates how the loss margin, $\Delta\alpha_m$, can significantly help in suppressing the next axial mode to the primary lasing mode which is preferred by the gain curve. Therefore the enhanced new MSR is given by

$$MSR(dB) = 10\log_{10}(\frac{\Delta\alpha + \Delta g}{\delta_G} + 1) \qquad \text{(Equation 6- 4)}$$

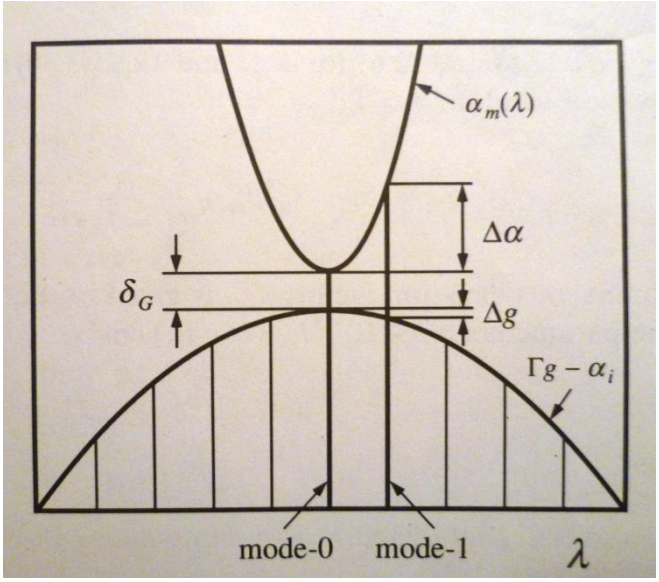


Figure 6- 48: Gain and loss spectrum with their overlap with Fabry Perot cavity axial modes [115].

In Equation 6- 4, $\Delta\alpha$ is the difference of mirror loss, α_m, between primary and secondary modes and Δg is the same difference but for the gain curve[10]. The gain defect, δ_G, is the difference of gain and loss for the primary mode can be found through

$$\delta_G = (\alpha_i + \alpha_m)\beta_{sp}\eta_r(\frac{I_{th}}{I - I_{th}}) \qquad \text{(Equation 6- 5)}$$

where β_{sp} is the spontaneous emission factor, and as shown in [116], it is given by

$$\beta_{sp} = \frac{\Gamma_c \lambda^4}{8\pi V n^2 n_g \Delta\lambda_{sp}} \qquad \text{(Equation 6- 6)}$$

Furthermore, the radiation efficiency, η_r, can be extracted from the spontaneous emission in the sub-threshold LI response [117] through

$$P_{sp} = \eta_i \eta_r \frac{h\nu}{q} I \qquad \text{(Equation 6- 7)}$$

6.7.3. Calculating MSR Numerical Value

For the numerical values in determining the mirror loss with the effective reflection from the external cavity, the effective refractive indices of the fundamental modes were used for laser and dielectric segments, i.e. $n_a = n_{eff\_laser\_guide} = 3.1944$, $n_p = 1$ for the air gap and n_{eff-}

[10] Here $\Gamma g - \alpha_i$ which is gain - intrinsic loss is referred to as effective gain curve and is shown in Figure 6- 48.

$_{waveguide}$=1.4868 for the dielectric waveguide segment. Therefore, $r_1=r_2=(n_a-n_p)/(n_a+n_p)$= 0.5232, t_2=0.8522 and r_3=-0.1958. For the length of the cavity segments, L_a=305μm and L_p=1μm were used for the laser cavity and gap length[11] respectively.

Since the goal is to find the MSR from Equation 6- 4, in order to calculate δ_G, first the total loss should be determined. Using Equation 6- 2, the effective reflection from the three-mirror cavity model yields $|r_{eff}|$=0.585 at λ=1.55μm and with r_1=0.5232. From Equation 6- 3, the mirror loss at the center wavelength is α_m=38.82 cm^{-1} and knowing α_i=25.1 cm^{-1} [60], the total loss at λ=1.55μm becomes $\alpha=\alpha_m+\alpha_i$=63.92 cm^{-1}.

For the spontaneous emission factor, β_{sp}, using Equation 6- 6 and Γ_c=0.04, Δλ=1nm, n_g=3.6, $n=n_{eff}$=3.1944 and V=0.271μm×300μm ×7μm, yields $\beta_{sp}=4.4\times10^{-4}$.

Regarding the radiation efficiency, η_r, from the CW response of this laser, shown in Figure 6- 11, at a current below threshold e.g. I=10mA, P_{sp}=6.05μW, and with η_i=87.6% and q/hν=1.25, from Equation 6- 7, radiation efficiency of $\eta_r=8.4\times10^{-4}$ is extracted[12].

Using the values for the loss, β_{sp}, and η_r derived above, and I=30mA with I_{th}=19mA, $\delta_G=4.2\times10^{-5}$ is obtained. In order to find Δg, one can use an MSR=1dB, seen in Figure 6- 43 for the non-integrated laser. Using Equation 6- 4 and assuming Δα=0 for the conventionally cleaved Fabry Perot laser, $\Delta g=0.259\times\delta_G$. To determine Δα, the difference of α_m for Δλ=1nm is calculated at λ=1550nm, and it is found to be Δα=0.03.

Now that all the components in evaluation of MSR are derived, the mode suppression ratio of the integrated laser can be calculated from Equation 6- 4, to be MSR=715.5= 28.5dB, which is very close to the approximate value of 25dB that is seen in Figure 6- 42.

The calculation presented in this section shows that the frequency dependence of the mirror loss can be an important contributing factor in enhancing the MSR in the lasing spectrum of integrated lasers. However, to verify this observation we need to run experiments with lasers of various gaps lengths and see if the model is able to explain the MSR of them, since $|r_{eff}|$ has inevitable strong dependence on the gap length in the current structure with non-angled laser facets and air gap.

In fact if this frequency dependence of α_m proves to be an uncontrollable factor in the recess integration approach, as shown in Figure 7- 2, the lasers and waveguides can be fabricated at an angle (similar to SOA structures) to avoid the reflection from coupling back

[11] This 1μm gap length is not the required resonance length of L_p, and thus can be an issue in using the model explained in Figure 6- 48.

[12] This value for radiation efficiency is quite low, however one must bear in mind that lasers are usually not very efficient LEDs.

to the laser cavity and induce a variable mirror-loss for different lasers seeing different air gaps.

6.8. External Quantum Efficiency

From the LI responses of integrated laser platelets, most of their parameters can be derived and studied. One factor of interest in lasers is external quantum efficiency, η_d, which represents the number of photons emitted per injected carrier (thus is unit-less). Therefore η_d can be found through the slope of LI curve above threshold from:

$$\eta_d = \frac{q}{h\nu}\frac{dL_{total}}{dI} = 2\frac{q}{h\nu}\frac{dL_{one\ facet}}{dI}$$

From Figure 6- 11 in which the continuous wave LI response of the laser integrated in 308µm recess is plotted (measured by an InGaAs detector), a line is fitted to the above threshold segment as shown in Figure 6- 49, and its slope is found to be 66.593×10^{-3} mW/mA. With q/hν=1.25 for free space and wavelength of λ=1.55µm, this results in η_d=16.6%.

Note that this η_d is derived for the integrated laser. For non-integrated lasers, J. Rumpler has seen η_d of 73% to 81% for 20˚C to 10.3˚C respectively, as well as a low η_d of 23% for less bright lasers [60].

There are two factors that hamper the external efficiency of the measured integrated lasers in this project. One is the coupling loss factor which naturally introduces some loss to the laser output before it can be measured at the dielectric waveguide output with a PD. Second, there has been a few years gap between the fabrication of these laser platelets and their integration in this project. Since the lasers had not been designed and packaged well for long lasting shelf life, their performance deteriorates over time. The three contributing factors, i.e. individual laser differences, coupling loss, and aging, cannot be differentiated robustly here.

Nevertheless, η_d=16.6% and η_d=70% have 6.25dB difference in value which is about 5dB larger than the coupling loss estimates, and is the result of both the aging of these lasers, and individual laser differences. Even in the lasers that J. Rumpler measured [60], there were instances of much lower η_d=23% as mentioned above.

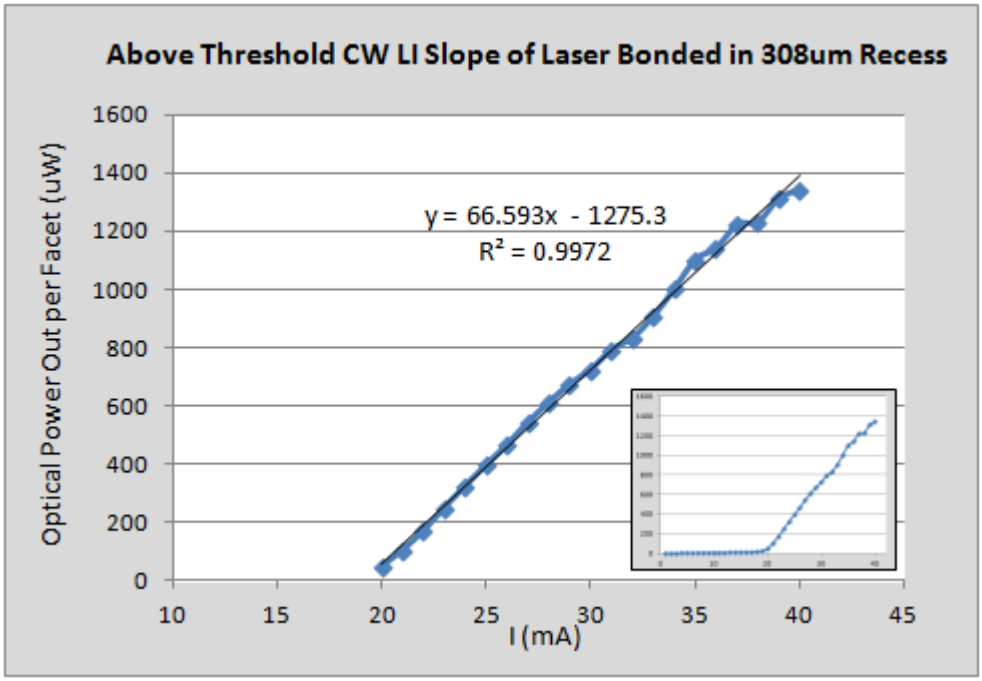


Figure 6- 49: Fitted trendline to the above threshold LI response of the laser integrated in 308μm recess and measured with InGaAs power head detector.

One might notice that an important problem about the above comparison is that the integrated lasers in this project are being compared to non-integrated lasers in [60]. The reason that such comparison is not exact is the fact that the integrated and non-integrated lasers see different mirror losses (α_m). A better approach would be to use the intrinsic efficiency, η_i, derived from the conventional cleaved lasers on their native InP substrate, and with the new facet reflectivities find an expected value for η_d in the integrated case.

The reason that η_i can not be estimated with laser platelets is the fact that various length of lasers are needed for a reliable estimation of η_i. Thus the data from conventional cleaved lasers made on their native InP substrate should be used as demonstrated by J. Rumpler in pp.151 of his thesis [60]. The values he found were η_i=87.6% and α_i=25.1 cm^{-1}.

External and internal quantum efficiencies, η_d and η_i respectively, are related through [100]:

$$\eta_d = \frac{\eta_i \alpha_m}{\alpha_i + \alpha_m}$$

Since, the mirror loss is given by:

$$\alpha_m = \frac{1}{L}\ln\left(\frac{1}{R}\right)$$

Therefore

$$\frac{1}{\eta_d} = \frac{\alpha_i}{\eta_i \ln(1/R)} L + \frac{1}{\eta_i}$$

With the estimated vales for α_i and η_i from [60], we should be able to get an estimate of η_d for the integrated lasers (excluding coupling loss) once the mirror reflections are known.

For integrated lasers, the three-mirror cavity model is employed as explained in Section 6.7.1. Thus, from the details discussed in Section 6.7.2, the effective reflection from the external cavity is $|r_{eff}| = 0.585$ for one facet, and simple Fresnel reflection[13] of r=0.5232 for the other facet of the laser Fabry Perot cavity. Note that the power reflection coefficient (R) is related to the amplitude reflection coefficient (r), with $R = r^2$.

Therefore, for integrated lasers, $R=|r_{eff}|\times r=0.585\times0.5232=31\%$ compared to R=24% for non-integrated lasers. Hence, for integrated laser with a cavity length of 300µm, $\alpha_m=39.5cm^{-1}$ (in contrast to $\alpha_{m\text{-non-integrated}}=43.2cm^{-1}$), and with $\alpha_i=25.1\ cm^{-1}$ and $\eta_i=87.6\%$, η_d can be calculated as:

$$\eta_d = \frac{\eta_i \alpha_m}{\alpha_i + \alpha_m} = 53.6\%$$

Comparing this expected value for external efficiency with the measured $\eta_d=16.6\%$, will convey a coupling loss of 5.1dB if the assumed η_i was valid and lasers had not aged.

If $|r_{eff}|=58.5\%$ is used for both laser facets, $\alpha_m=35.7cm^{-1}$ and thus $\eta_d=51.4\%$, and compared to experimental value of $\eta_d=16.6\%$, conveys the coupling loss of 4.9dB. However both of these values are much larger compared to the 1.23dB coupling loss estimation of Table 6- 6 for this integrated laser in the 308µm recess, and therefore η_i value for this laser must have been quite smaller than the ideal 87.6% that was reported for the best conventionally cleaved lasers in [60].

6.8.1. Aging of Laser Platelets

To get a better sense of the aging of these laser platelets, the LI response that J. Rumpler obtained from CW operation of the best free standing laser platelets he has measured, is shown in Figure 6- 50. From this it can be noticed that at 15˚C and I=40mA, the output power is P=5.7mW. Unfortunately, in the current project a non-integrated laser that manages to lase CW had not been found; otherwise, that would have provided a great criteria to measure the aging effect in these lasers. Only the CW operation of integrated lasers was observed and could be measured. This might be due to a better heat transport in the integrated structure, less heating and thus less Auger recombination. Or it might be due to the decreased

[13] As discussed in Section 6.7.2. this is due to the scattering caused by the rough surface of Al/In layer that is covering one facet of the recess, in the current implementation of coaxial integration.

mirror loss as a result of the presence of external cavity, and thus lower required gain to reach threshold. In any case, the CW LI response of an integrated laser showed P=1.34mW which includes individual laser differences, ageing factor, and coupling loss when it is compared to P=5.7mW seen from Figure 6- 50.

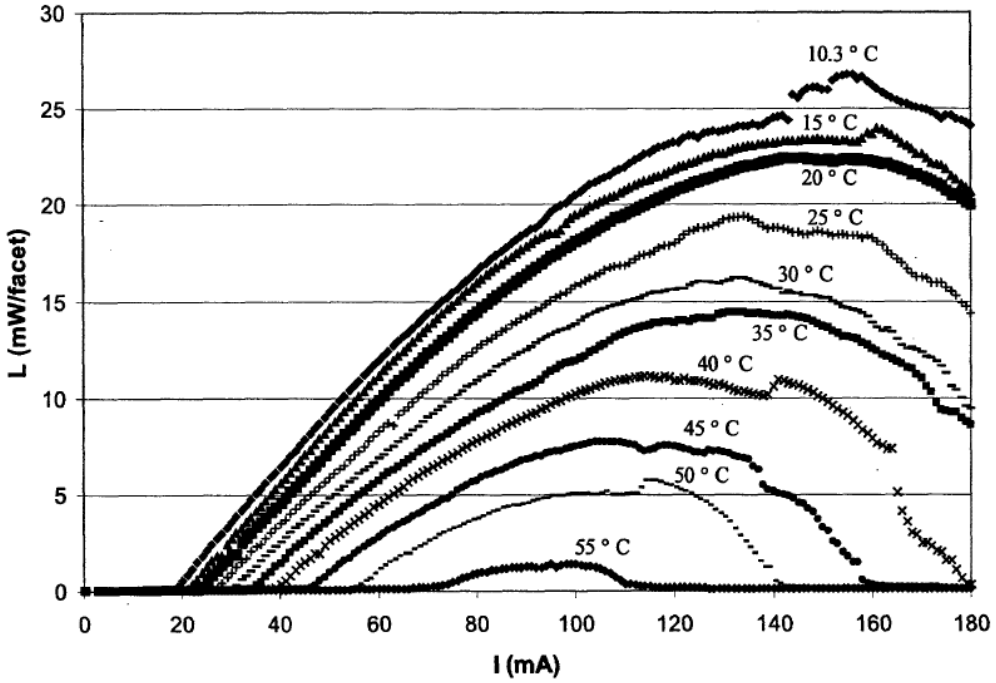


Figure 6- 50: LI characteristic of a CW operation of a non-integrated laser platelet measured by J. Rumpler, pp. 163 of [60].

6.9. Characteristic Temperature

From the pulsed LI measurements presented in Section 6.2, it was seen that integrated lasers have a consistently lower threshold current compared to non-integrated lasers. Such trend is verified by comparing the threshold currents of an integrated and a non-integrated laser over a range of stage temperatures as shown in Figure 6- 51.

The lower threshold for integrated lasers can be due to two factors. One is the higher effective reflectivity seen at one of the facets and thus lower mirror loss of the integrated laser, resulting in a lower threshold current. However, the more important contributing factor is the different heat transfer mechanism in the two structures and thus the sensitivity of threshold currents on temperature.

In fact, the dependence of threshold current on temperature can be modeled by an exponential term as

$$I_{th} = I_{th0} e^{T/T_0} \qquad \text{(Equation 6- 8)}$$

Based on Equation 6- 8, T_0 is the characteristic temperature and shows the sensitivity of the threshold current on temperature increase. Higher T_0 is preferred which implies a lower sensitivity of I_{th} on temperature. In order to find T_0, Equation 6- 8 can be rewritten in the logarithm form of

$$\ln(I_{th}) = \ln(I_{th0}) + T/T_0 \qquad \text{(Equation 6- 9)}$$

Therefore if the natural logarithm of I_{th} is plotted versus temperature (in Kelvin), as shown in Figure 6- 52, the inverse of the fitted line slope will yield the characteristic temperature T_0. As it is seen in Figure 6- 52, the significant R-squared factors in the linear fit of $\ln(I_{th})$ versus T shows that exponential model of Equation 6- 8 describes the temperature dependence of I_{th} very well. The inverse of the slope of the fitted lines gives the characteristic temperatures of T_0=60K for the non-integrated laser and T_0=76K for the integrated laser.

The increased characteristic temperature for the integrated lasers is an indication of better heat transfer in the integrated structure.

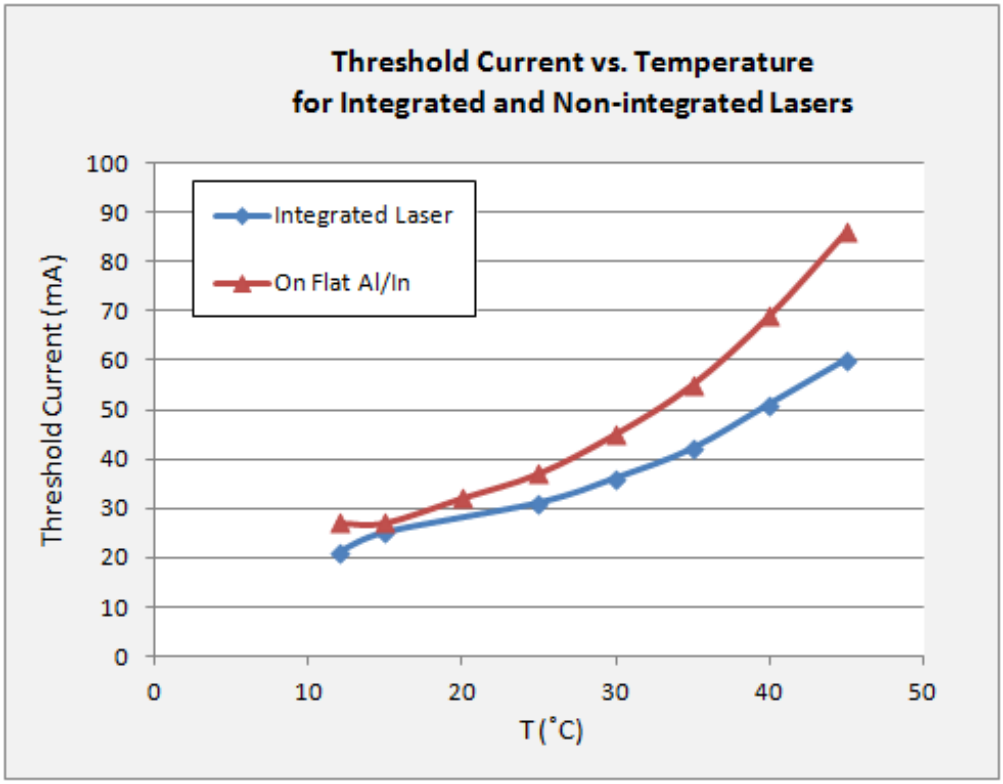


Figure 6- 51: Threshold current versus stage temperature for integrated and non-integrated lasers. The consistent trend of higher threshold current for the non-integrated laser is observable.

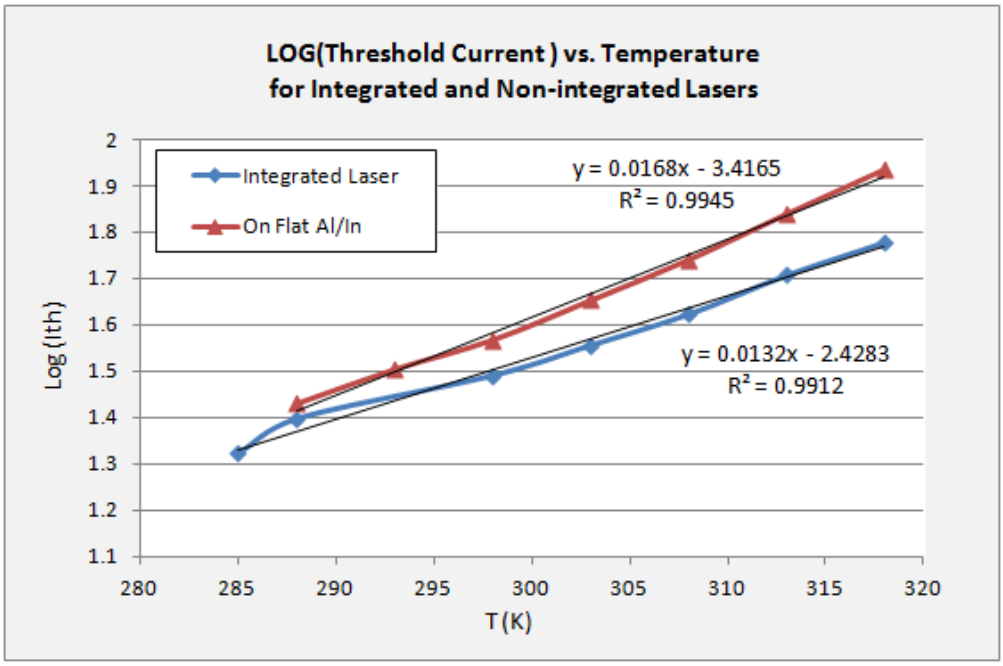


Figure 6- 52: Extracting the characteristic temperature from the inverse of the slope of $\ln(I_{th})$ versus T.

6.10. Determining the Coupling Loss

Determining the coupling loss addresses an important question in the coaxial integration approach demonstrated in this project. However, as important as this question is, finding a reliable answer is rather challenging. One complexity involved is the variation between the laser platelets themselves. Among those that lase (the majority), some have high output power and some have lower emitted optical power. This variability factor makes the derivation of coupling efficiency by comparing an integrated laser on chip with another laser bonded on flat surface, not completely accurate. Also the alignment of the detector and the quality of the contact that the probes make is another factor that changes the response even for a single laser.

With these factors in mind, a reliable way to derive the coupling loss is to measure the output of one single laser in two integrated and non-integrated states and compare the response of the two.

In order to achieve this, it was tried numerous times to retrieve a laser that was initially integrated in a recess and had been characterized, and then after it became debonded from the well, bond it back on a flat Al/In coated surface and measure its response in this non-integrated state for the purpose of comparison mentioned above. However due to yield

issues and loosing the laser platelets in bonding phase (e.g. they frequently became stuck to the thermo-plastic membrane on top), this solution did not work out in those attempts.

6.10.1. Open-Ended Recess Method

Another possibility to estimate the coupling loss, would have been to integrate a laser platelet in a recess on a chip that has been cleaved through one end of recesses, as shown in Figure 6- 53. Therefore at one side (left in this schematic), the laser's emitted light is coupled to the SiON waveguide and represents the similar output of an integrated laser-waveguide structure (P_2), and on the other output (right side here), due to the cleave, the recess edges and thus SiON waveguide and SiO_2 stack are all removed, thus the direct output of the laser can be measured (P_1). Assuming two similar detectors with the same alignment to the chip, make the readings of P_1 and P_2, the coupling loss can be derived as:

$$\text{Coupling Loss} = -10\ \text{Log}_{10}\ (P_2/P_1)$$

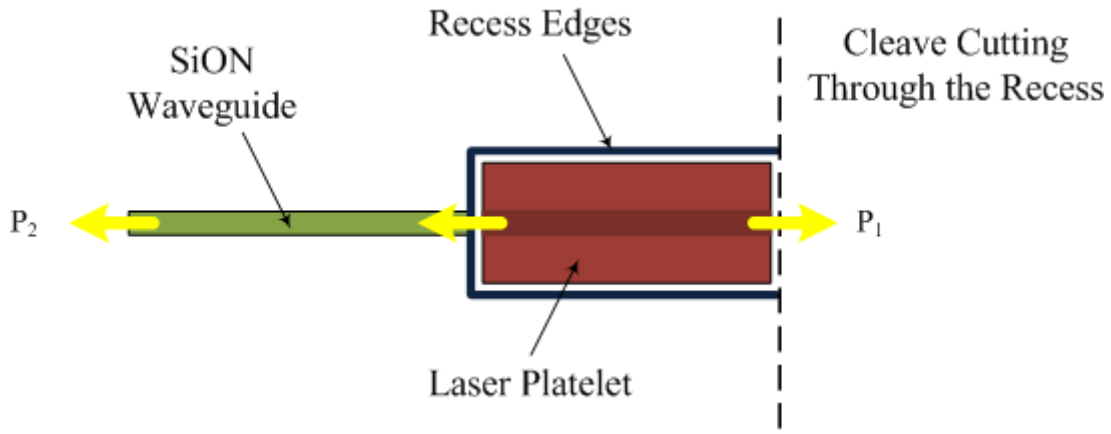


Figure 6- 53: Schematic illustrating a possible method to derive laser-waveguide coupling loss in the coaxial integration technique, by cleaving through one end of recesses and thus accessing the direct output of laser. Comparing P_1 and P_2, the coupling loss could be derived.

Although this idea seemed very promising at the beginning, in practice, it turned out that due to the loose holding of laser platelets in an open-ended recess in the structure of Figure 6- 53, it was very difficult to hold laser platelets in such a well post assembly and while the chip was being transferred to the bonding setup and during its placement on bonder heating stripe. When this transfer was successful, the laser was picked up by the electrostatic attraction either to the holder edges or the thermo-plastic membrane of the bonding setup. Hence, the need to devise other ways to estimate the coupling loss emerged.

6.10.2. Estimating Coupling Loss from Two Different Lasers

Since the aforementioned two approaches with the goal of comparing the output of a single laser in integrated and non-integrated states were not easily feasible considering the yield of the current process, another possible approach was pursed which is based on estimating the coupling loss by comparing the output power of two different lasers, one integrated and one non-integrated. The idea is that if this is done for enough number of trials, a statistically reliable estimate can be made if variation between lasers is not too large.

For this purpose the pulsed response of a non-integrated laser[14] (bonded on a flat Al/In coated surface) is compared to the integrated lasers mentioned in Table 6- 2. For reference the pulsed LI response of the non-integrated laser is given in Figure 6- 54. Note that this measurement had been done with slightly different pulse frequency i.e. %PRI=1%[15] compared to %PRI=0.5% of the integrated lasers whose response was presented in Section 6.2.2. However since pulse widths had been 1µs for both cases, the difference in %PRI does not matter, because the assumption is lasers do not heat up much in pulsed operation. However, one factor that will affect the result is that the Ge photodetector gain had been 40dB here. Therefore the calibration factor needs to be derived for this gain as well. With the data shown in Appendix II, Figure AII- 2, it was concluded that A_{40dB}/A_{30dB}= 35.2/29 = 1.214, thus using $A_{30dB\text{-}adjusted} = 3.47\times10^3$ gives $A_{40dB\text{-}adjusted} = 4.21\times10^3$. With this, the optical output of the non-integrated laser shown in Figure 6- 54 can be calculated as:

$$P_{non\text{-}integrated} = V/A_{40dB\text{-}adjusted} = 5.96V/ (4.21\times10^3) = 1.42mW \quad @ \ 30mA$$

With this derived output power for the non-integrated laser, an estimate of the coupling loss can be made comparing it with the pulsed response of integrated lasers at the same current[16] (i.e. 30mA), as listed in Table 6- 6.

[14] In fact this laser has the legacy of being the first laser, with which lasing was observed in this project. The laser had been extremely bright, that the output beam could be visually "seen" by an IR sensitive disk.
[15] PRI% stands for percent in Pulse Repetition Interval, meaning the ratio of pulse width to the period of pulses.
[16] Due to threshold difference of typical integrated and non-integrated lasers, it would have been more accurate to compare the output at same current value above threshold, i.e. $(I\text{-}I_{th})$=constant. However since the specific laser measured in Figure 6- 54 shows I_{th} close to the integrated lasers, same current had been used in estimating the coupling loss.

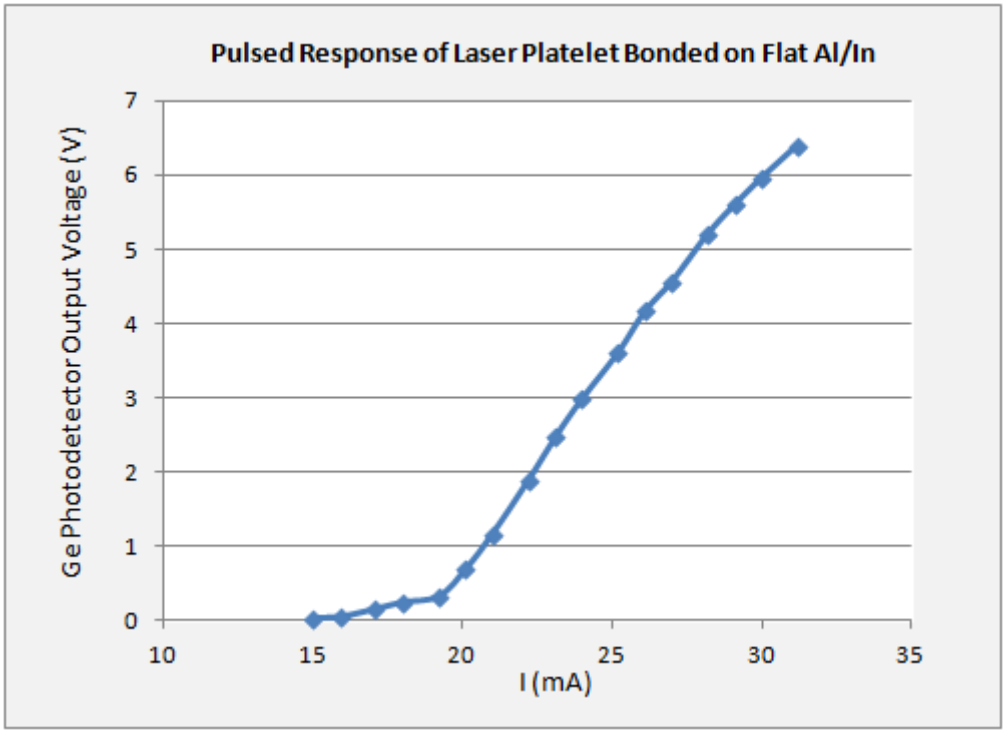


Figure 6- 54: Pulsed response of the first non-integrated laser measured.

Recess Length of Integrated Laser Platelet	Output Power @ I =30mA	Coupling Loss
306 µm	548 µW	4.12 dB
311 µm	957 µW	1.71 dB
312 µm	1.31 mW	0.35 dB
308 µm	1.07 mW	1.23 dB
304 µm	369 µW @ 35mA	5.85 dB
Non-integrated Laser	1.42 mW	-

Table 6- 6: Coupling loss derived from comparing the pulsed response of different non-integrated and integrated lasers.

As seen from the results derived from comparing different integrated and non-integrated lasers, the coupling loss has a range of 0.3dB to 6dB. One of the factors contributing to the different coupling losses derived is the difference in the lasers individually, however more important is the different horizontal alignment and air gap that each integrated laser has, based on its assembly and bonding in its corresponding recess. For instance, the zoomed SEM image of the laser-waveguide coupling facets of two integrated lasers in 312µm and 311µm recesses is shown in Figure 6- 55 and Figure 6- 56 respectively.

Note that the left facet of the recess is covered with the Al/In bonding layer; therefore lasing emission is coupled to the right SiON dielectric waveguide only, thus the right facet is of interest here.

In fact, comparing the results of Table 6- 6 with these two SEMs is quite interesting. Note that the coupling loss for the 312µm laser is 0.35dB while it is 1.71dB for the 311µm recess laser. It is observed from the close up SEMs of the coupling facets that the 312µm laser has a gap width of only about 1µm, while gap length of 311µm laser is about 2.7µm. Since increased gap length makes the non-guided optical mode propagating in the air gap expand and thus reduces the coupling efficiency between the two waveguides, the increased coupling loss of the 311µm laser compared to 312µm laser is consistent with expectation.

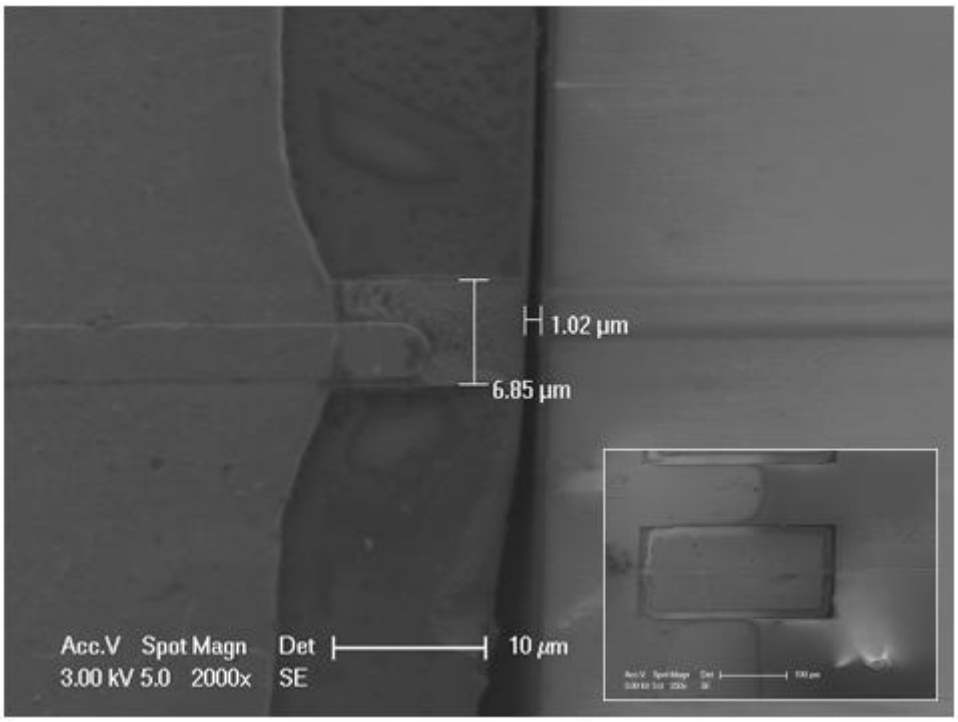


Figure 6- 55: SEM image of the right coupling facet of laser integrated in 312µm recess (the inset). This facet has a very good horizontal alignment of the waveguides and small gap width of 1µm.

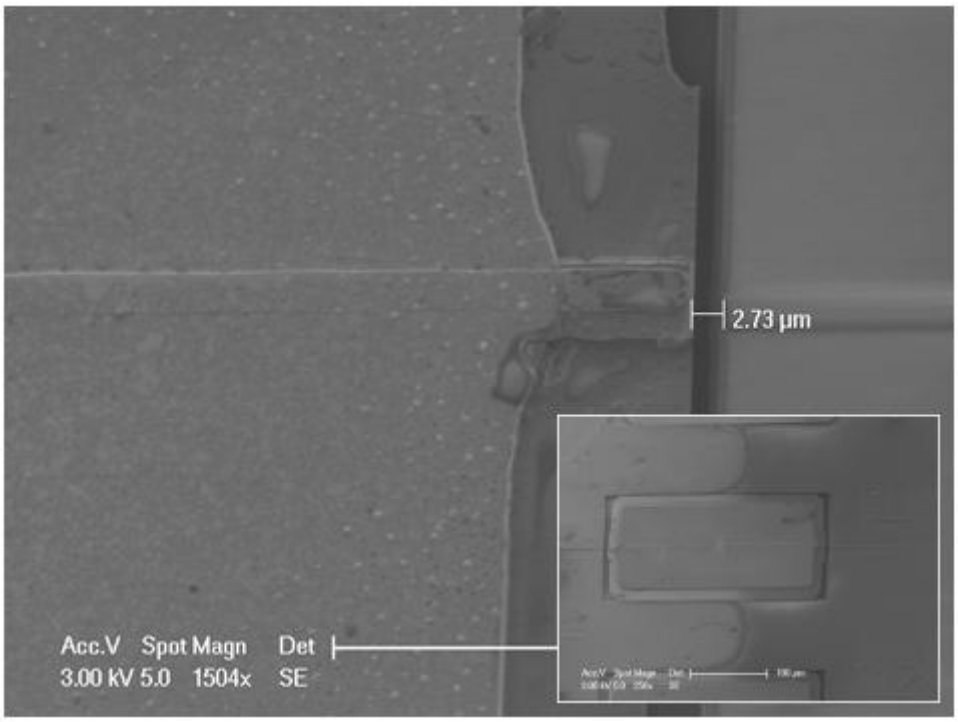


Figure 6- 56: SEM image of the right hand coupling facet of laser platelet integrated in 311µm recess (the inset image). The increased gap width of 2.73µm in this case increases the coupling loss.

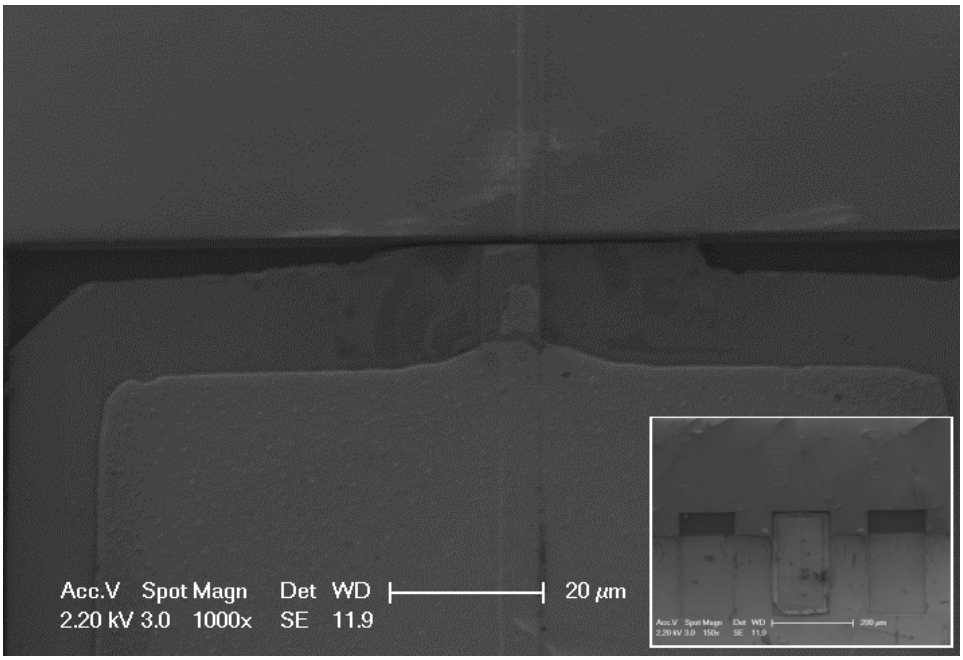


Figure 6- 57: SEM image of the laser platelet integrated in a 308µm recess. Gap width is measured to be less than 1µm, however as noticed from this SEM, there is a lateral shift between the center of waveguides.

Figure 6- 57 shows the SEM taken from the laser platelet integrated in a 308µm recess. Although the gap width is about and less than 1µm, since there is lateral shift between

the center of two waveguides, coupling loss is 1.23dB which is more than 0.35dB of 312μm laser with a comparable gap length.

Another interesting case is the laser bonded in a 304μm recess. Figure 6- 58 shows the measured pulsed response of this laser. Note that the threshold current for this laser is I_{th}=22mA, in contrast to the rest of the lasers of this sort which showed I_{th}=17mA for pulsed operation. Since the threshold current is about 5mA above the rest of lasers, its response at I=35mA is used in the corresponding entry at Table 6- 6. For I=35mA, Ge PD voltage=1.28V, which with $A_{30dB\text{-}adjusted} = 3.47\times10^3$ results in output power of P=396μW which is quite low compared to the rest of integrated lasers. Comparing this with the output of non-integrated laser as listed in Table 6- 6, the coupling loss is about 6dB, which is quite high compared to the rest of the measured integrated lasers. Looking at the SEM image of the laser-waveguide facet of this integrated laser, shown in Figure 6- 59, one can explain the reason of such a low coupling. For this laser, there is a significant amount of lateral shift between the laser ridge and the SiON dielectric guide. Therefore, essentially only a small fraction of the laser's emitted light gets coupled to the waveguide and is measured by the photodetector, therefore the coupling loss is much higher than the case of e.g. laser in 312μm recess which had excellent horizontal alignment of the two guides and thus a very low coupling loss.

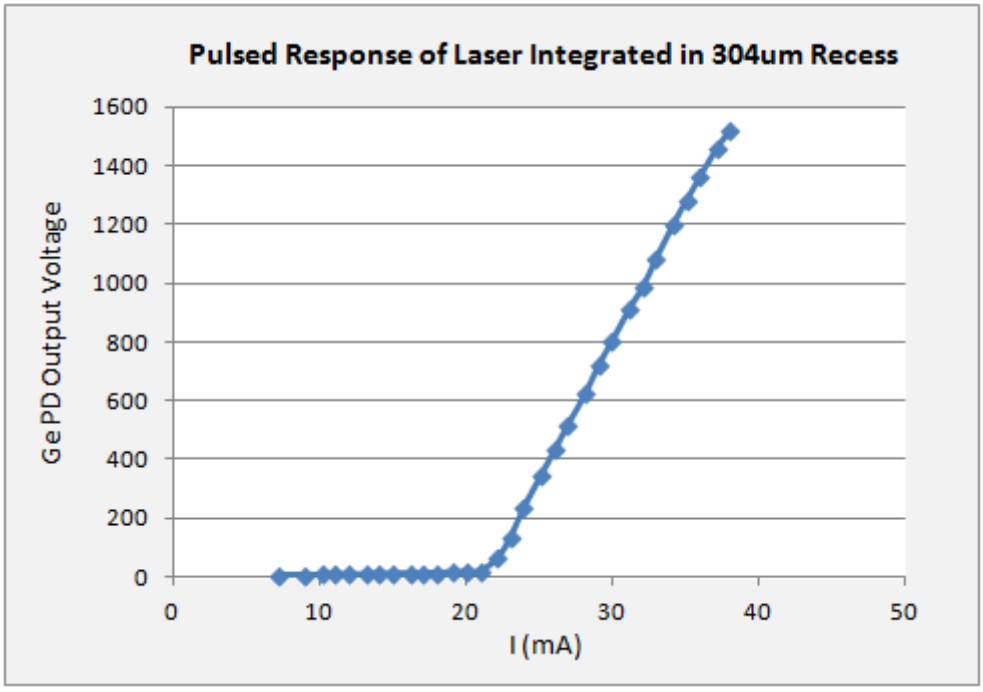


Figure 6- 58: Pulsed response of laser integrated in 304μm recess.

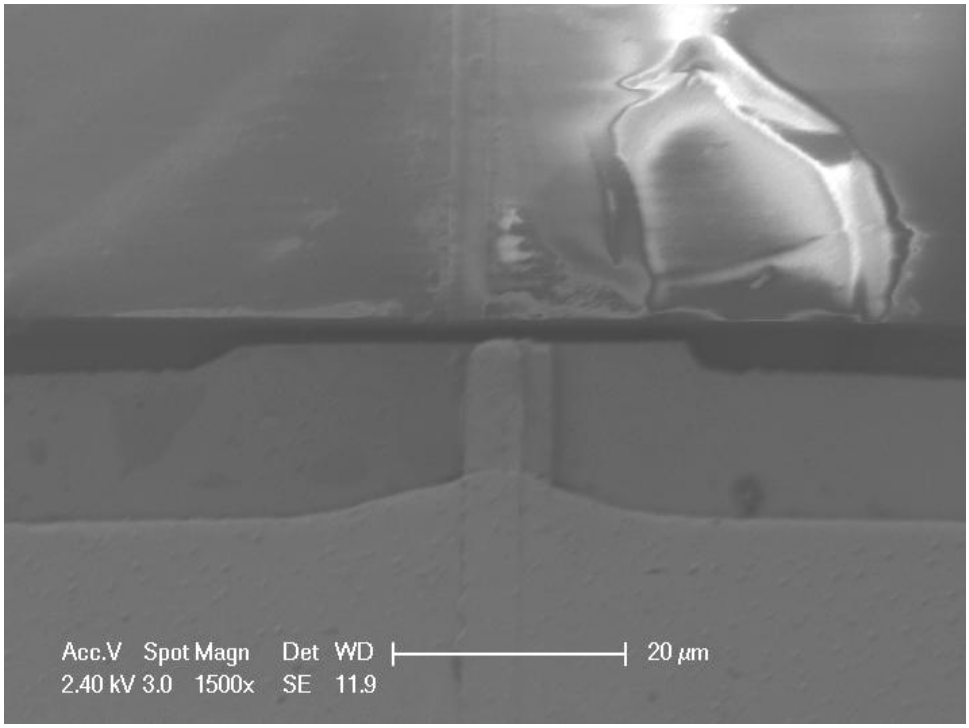


Figure 6- 59: SEM image of laser-waveguide facet for the laser integrated in 304µm recess. Note the major horizontal misalignment of the two guides. (The bright area on the upper corner of the image is due to SiO_2 getting charged by the electron beam, as this SEM image was taken in Hi-Vac SEM rather than ESEM which is more suitable for non-conducting samples.)

6.10.2.1. Comparison of Experimental Coupling Loss with FDTD Simulations

It is helpful to know how the coupling loss measurements of Table 6- 6 in addition to the knowledge of gap widths presented in Figure 6- 55 and Figure 6- 56, compare with theoretical simulations.

E. Barkley, in his PhD thesis [59] has done a series of 2D FDTD simulations looking at the transmission (thus the coupling loss) between laser and dielectric waveguides. The result of his findings for air gap filling is presented in Figure 6- 60.

It is noticed that the measured losses are consistently less than what these simulations convey. For instance for a gap width of 1µm, Figure 6- 60 suggests a 4dB loss whereas from the measurements shown in Table 6- 6, about 1dB of loss was extracted.

One reason for such a discrepancy is due to the fact that in these simulations the input mode is launched at the SiON waveguide and then is coupled to the laser ridge waveguide. Conversely, in the actual integrated structure the lasing beam is coupled from the laser waveguide to the dielectric one. Although for a zero gap width (i.e. end-fire coupling), the

coupling integral is symmetric and thus will not depend on the order of waveguides, however due to mode spreading in the air gap, such symmetry will not necessarily hold. It is expected that when the mode is getting coupled from the narrow laser core (0.27µm), the presence of the air gap helps to widen the mode for a better matching with the dielectric core (0.55µm in height). However, in the reverse case, the SiON mode is already larger in height compared to the laser mode and when propagates through the gap it widens even more, thus it sees less overlap with the fundamental mode of the laser guide. Therefore, it is expected that the results of Figure 6- 60 are consistently higher than the measurement results of Table 6- 6.

Another point to consider is the limitations of the 2D FDTD simulations that were carried out to derive Figure 6- 60. For instance, the length of the waveguides might not have been long enough to de-embed the shape of launch field and reach the true modes of each waveguide.

E. Barkley has also investigated the effect of lateral shift of the two waveguides on coupling loss [59]. However since those simulations use a width of 3µm for the laser ridge, the results cannot be used for the actual current lasers that have a ridge width of 6.8µm.

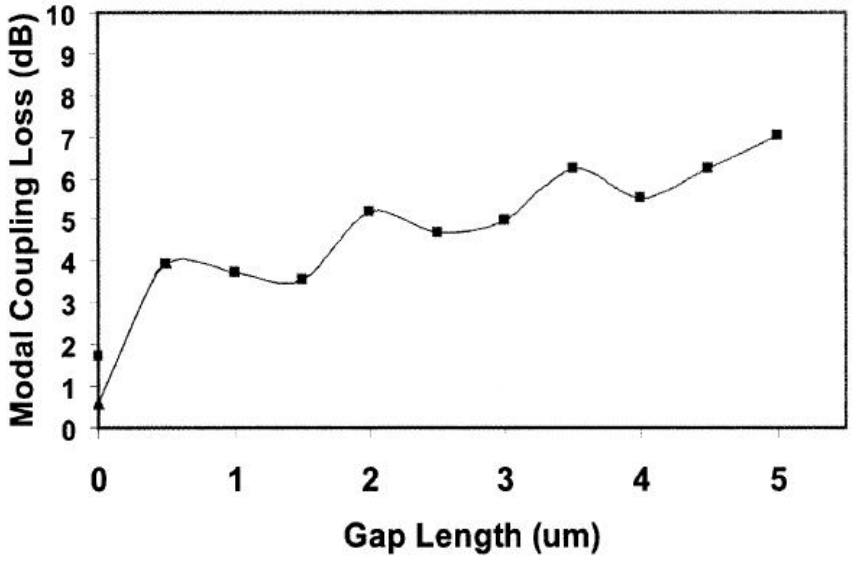


Figure 6- 60: 2D FDTD simulations to determine coupling loss between laser and dielectric waveguides for the different lengths of air gap.

6.10.3. Determining Coupling Loss through Surface Temperature Analysis

Since getting an accurate estimate of coupling loss is not highly robust when different lasers are compared, the characterization of such loss is challenging for lasers in integrated systems. To address this concern in general, K. Pipe and Prof. Rajeev Ram at MIT have developed a technique [102], [103] that is able to give an estimate of a laser radiation, through a simple thermal analysis model.

- 6.10.3.1. Theory

Figure 6- 61 shows the essence of this approach where three temperature readings of $T_{laser\text{-}surface}$, $T_{heatsink}$ and $T_{ambient}$ make it possible to determine Q_{rad} above threshold. Basically in this analysis, the input-output power balance is preserved as shown in Equation 6- 10, which translates to Equation 6- 11.

$$Q_{in} = Q_{conduction} + Q_{convection} + Q_{radiation} \qquad \text{(Equation 6- 10)}$$

$$IV = \frac{\Delta T}{Z_T} + A_{eff} \times h \times \left(T_{surf} - T_{amb}\right) + Q_{rad} \qquad \text{(Equation 6- 11)}$$

In this model, below threshold the weak spontaneous radiated power is ignored and thus the slope of ΔT ($=T_{surf}$-$T_{heatsink}$) versus input power (IV) gives the thermal impedance of the chip, accounting for the conduction term in the input-output power balance of Equation 6-10.

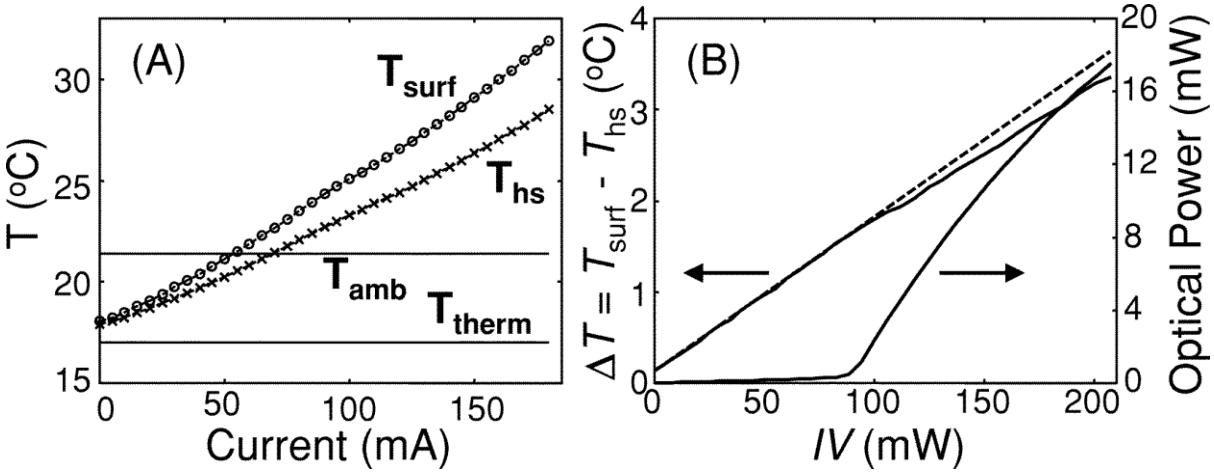


Figure 6- 61: Graphs describing the surface temperature analysis method used to determine laser radiation power. [102]

Once Z_T is determined through below-threshold ΔT/(IV) slope, the convection term in this thermal analysis (second term in Equation 6- 11) can be determined from the I=0 point, resulting in:

$$A_{eff} \times h = \frac{\Delta T_0}{Z_T \times (T_{amb} - T_{surf})_0} \qquad \text{(Equation 6- 12)}$$

Having both the Z_T (accounting for conduction) and A_{eff}×h (accounting for convection) terms derived, one can use Equation 6- 11 to determine Q_{rad} above threshold. Note that here $IV = IV' - I^2R_{series}$, where V' is the output voltage of power source and R_{series} is the resistance of wires. Therefore ohmic heating in the contact path is already de-embedded in Equation 6- 11.

- 6.10.3.2. Implementation

In order to apply this method to our coaxially integrated lasers, a set of fine and sensitive thermocouples are required. Initially for ease of handling and gaining experience in using fine thermocouples, 75µm and 50µm tip T-series[17] unshielded thermocouples from Omega [104] were used.

Since the laser platelets have dimensions of 300µm×150µm, and an electrical probe also sits on the laser top p-contact surface, 75µm or larger thermocouples were not suitable for this application. Furthermore, large tip thermocouples enhance the cooling of laser top surface through conduction via the thermocouple metal, a factor that is not captured in the model used here. Therefore, the choice of 25µm[18] is the best regarding the footprint of the thermocouples needed for surface temperature measurements. However, in this case the wires are extremely fine and make the assembly and handling quite challenging. Hence, utmost care must be taken when removing the thermocouples from their manufacturer sheet, and taping the tip on a probe. Probes are used here since they could be maneuvered with micro-positioners. Half a centimeter above the soldered tip of the thermocouple it is taped to a probe. The fact that these thermocouples are unshielded[19] adds to the complexity and challenge of handling them. Thus in their placement on the setup and during measurements care must be taken to make sure that the copper and constantan wires do not cross. However

[17] T series thermocouples are copper and constantan type.
[18] 25µm is the minimum dimension of fine thermocouples that Omega offers.
[19] There are fine 20µm shielded thermocouples available from other suppliers. However it turned out that unshielding them for contact and micro-soldering the tip is a challenge of its own, over which the unshielded Omega thermocouples were preferred in this project.

with practice the user can securely mount and use the fine 25µm thermocouples for surface temperature measurements.

With the use of two 25 T-type thermocouples from Omega, and continuous wave (CW) drive, the preliminary result of surface temperature analysis of the laser bonded in 304µm recess is presented in Figure 6- 62. Consistent with Figure 6- 61, below threshold ΔT vs. IV relationship is linear giving Z_T=196.8 ˚C/W, and from I=0, A_{eff}×h=0.01 can be derived. However, above threshold ΔT deviates from the extrapolation of Z_T×IV, and through Equation 6- 11 Q_{rad} can be calculated. For instance, at I=35mA, the coupling loss is found to be 5.8dB which is comparable to 5.85dB found before for the pulsed operation of this laser as shown in Table 6- 6.

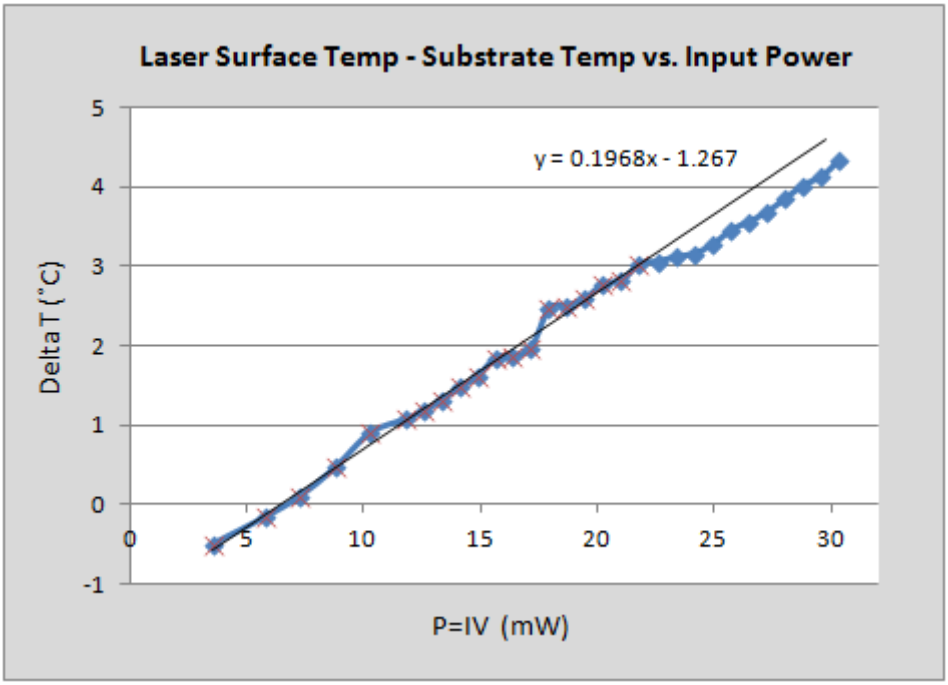


Figure 6- 62: Initial results of surface temperature analysis of the 304µm laser with CW drive.

In spite of the close match of these results, it should be kept in mind that Figure 6- 62 reflects the initial attempts to use the surface temperature analysis method for estimating coupling loss and many unstable factors were present which need to be corrected/stabilized for more robust measurements. For instance, the thermoelectric cooler that was used in this measurement is different from what was used in past pulsed and CW measurements and due to reaching its current limit was not able to provide enough temperature control for the laser. This resulted in a threshold current of 30mA for this case which is much higher than I_{th} of other lasers of this type that were measured before. Furthermore, due to air conditioning of

the lab environment, convection might have been more significant than what the 1D model used here can capture. More importantly, the temperature reading was not stable and made an accurate estimate more difficult. Along with fluctuations of temperature, voltage measured by the current source also had instabilities, therefore reading of voltage and thus power had been not very reliable either, hence a diode model was used instead. Finally, in this measurement ΔT is measured as a difference of temperature from the top of the laser and the top surface of the wafer (on the Al/In layer). However, the formulation of [102] defines ΔT as T_{surf}-T_{hs} thus the second thermocouple should have been placed on the heatsink rather than the top of the sample. With all these, more robust measurements need to be carried out for a more reliable estimation. However the technique, approach and resulted graph will be essentially similar to what was presented here through these preliminary results.

6.10.4. One-Waveguide-Removed Approach to Estimate Coupling Loss

Since the variation between individual lasers output power prevents a robust estimation of coupling loss, the need to measure the loss more directly and with one single laser resurfaces again. The issue with the suggested method of cleaving along a recess edge, discussed in Section 6.10.1 and shown in Figure 6- 53, was the lack of enough support to hold the assembled laser in the well while it was being transferred to the bonding system. This caused the laser to fall out of the recess it was assembled to, making the recess-cleave idea impractical.

However, this issue can be addressed by keeping the edges of the recess intact, thus providing enough holding support for the laser platelet to stay in place, and only removing the SiON/SiO_2 waveguide stack on one facet, so that the laser output can directly be measured without seeing any coupling loss. Simultaneously, from the facet on the other side (which has the SiON/SiO_2 waveguide intact), the coupled light to the dielectric waveguide can be measured. By comparing these two outputs, the coupling loss can be robustly estimated for one single laser. The schematic in Figure 6- 63 illustrates this idea, where the light emitted from the left facet of the laser platelet gets coupled to a SiON dielectric waveguide, while on the right, the SiON/SiO_2 is removed by a deep dry etch. This allows the emitted light to be directly measured by the photodetector without suffering from any coupling loss. As before, dividing these two output powers will give a good estimate of the coupling loss for this integrated laser.

The advantage of the structure proposed in Figure 6- 63 over the earlier idea of cleaved recess in Figure 6- 53 is that the edges of the well remain intact thus there is sufficient physical support to hold the laser platelet in place until it gets securely bonded in its recess. Therefore better success is expected to result with this approach.

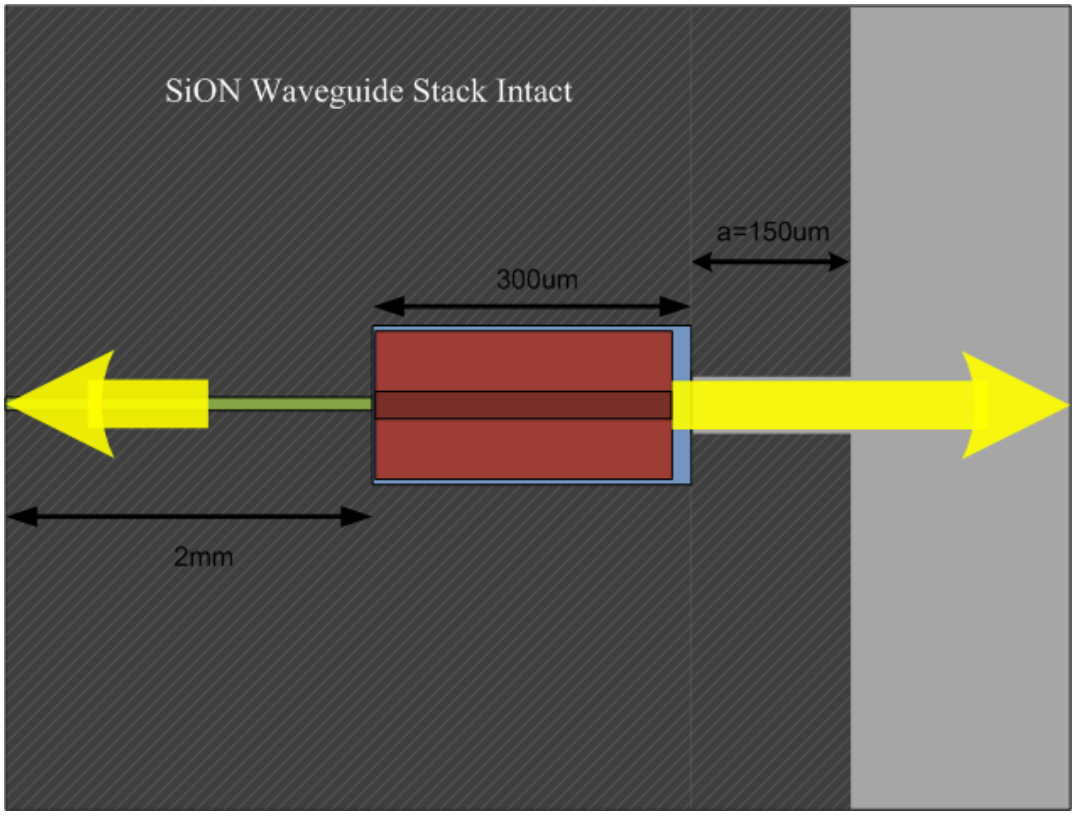
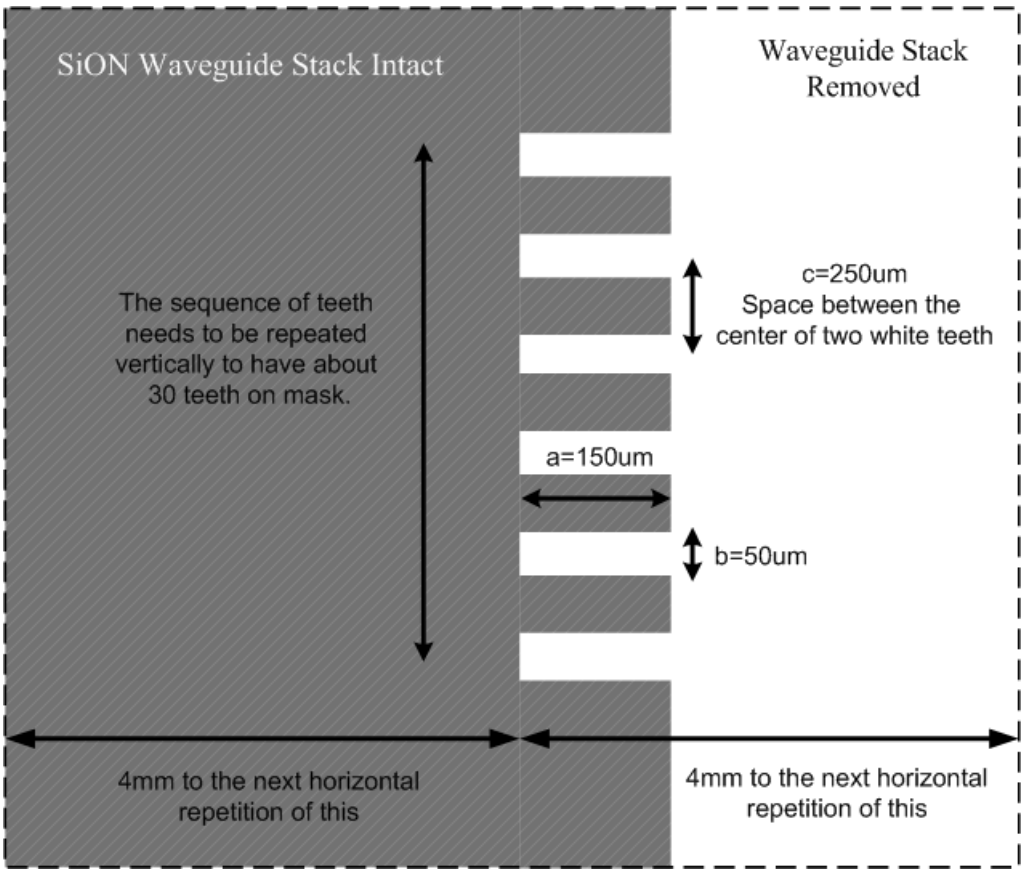


Figure 6- 63: Schematic showing the one-waveguide-removal idea to measure coupling loss more robustly.

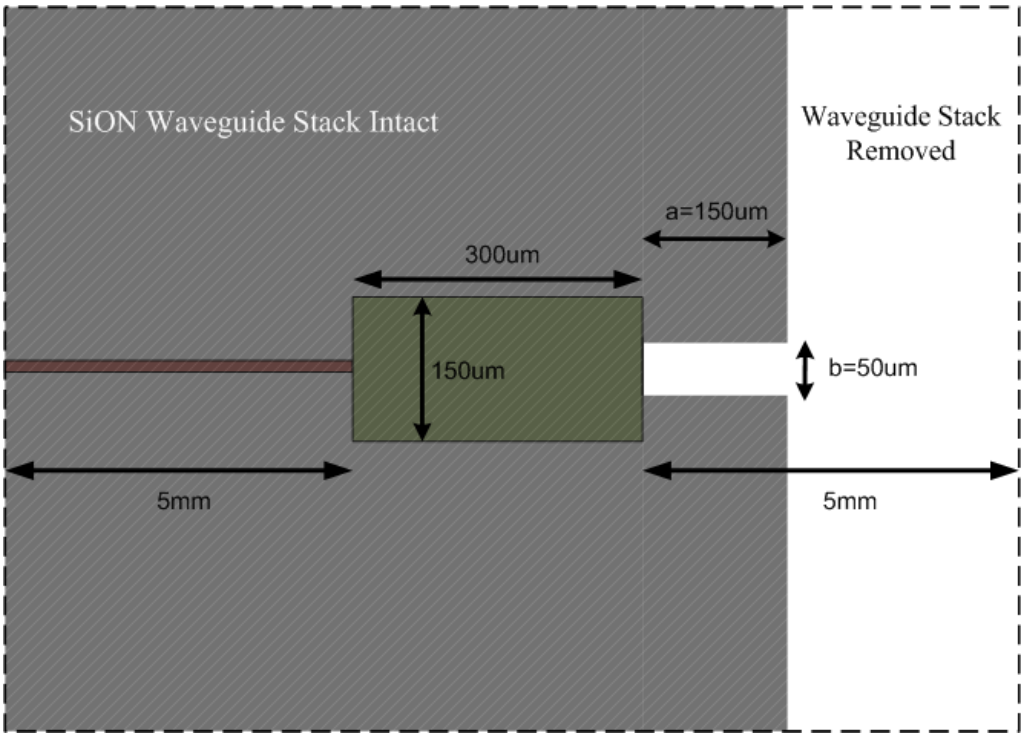
In order to remove the SiON/SiO_2 on the right side of the recesses, a mask with the pattern shown in Figure 6- 64 was employed. Figure 6- 65 shows the AZ4620 resist patterned with such a mask using the modified recipe that was discussed in Chapter 5, Section 5.2.7.

Figure 6- 65 also shows that the Al/In solder-bonding stripe covers most of the right side of recesses, while leaving the left facet clear for coupling of the light out to SiON waveguide for coupled measurements.

In order to fabricate this structure there are two possibilities. One can either etch the SiO_2 stack first and then deposit and pattern the Al/In solder-bonding layer, or alternatively do this in reverse. Initially the second method was selected because samples with already deposited Al/In layer were on hand. However, for the subsequent generation of samples the first option was adopted as it provides a wider Al/In bonding layer on the top surface.



(a)



(b)

Figure 6- 64: (a) Mask layout sketch used to etch SiON/SiO_2 at the right side of recesses in order to measure coupling loss. (b) How one of the teeth shapes in the layout of (a) is aligned to a recess.

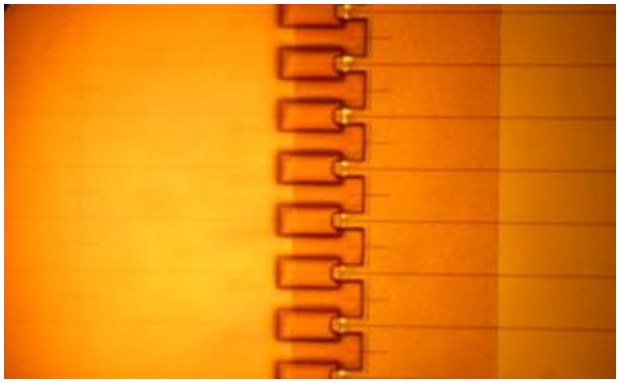


Figure 6- 65: Patterned AZ4620 resist with the mask layout of Figure 6- 64, in order to remove the $SiON/SiO_2$ stack partly at the right side of recesses. The stripe seen here is patterned Al/In solder-bonding layer.

To etch the thick $SiON/SiO_2$ stack, either wet or dry-etching can be used. Because the thickness of this layer where the waveguide core is present is about 7µm, the mask should be able to endure the long etching process.

Initially wet-etching was tried. Etching such a thick layer takes about 50min with BOE. Concentrated HF very quickly under-etches the edges of the pattern and destroys it. The reason for such aggressive result relies not on the reaction of HF and SiO_2 but from how HF etches Al extremely fast. Therefore, even for a brief exposure to HF, the underlying Al of the Al/In layer is etched away and thus the edges of the pattern get undercut and destroyed.

Overall, since BOE is very slow to etch the thick $SiON/SiO_2$ stack, and even the thick resist mask might not be able to endure such a long etch, an RIE dry etch was selected instead. Although a recipe used in another facility was on hand, it could not be exactly followed due to the limitations of the MTL EML's RIE system. Therefore, a modified recipe was developed for this system so that it etched 7µm of SiO_2 faster than the 6µm of AZ4620 resist used as the mask for this process. Based on power and gas flow limitations of this RIE system, the following flow rates were used with a power of 350W, Ar: 20sccm, CHF_3: 45sccm, CF_4: 15sccm, with a resulting etch rate of 11Å/s.

If higher powers levels were possible, the etch rate would have been higher. However 350W was the maximum tunable power available in this RIE system. Another factor that dropped the etch rate was cooling the substrate through a He flow to prevent the chip from over-heating and burning the resist (which was observed in the initial etch trials without the substrate cooling flow). Using the substrate cooling feature, and with an etch rate of 11Å/s, it takes about 106min to complete this deep etch. For longer etches of about 115min, the resist almost holds up to the end, although due to surface roughness, pinholes etched through the

resist reach the protected area of SiO_2 and made its surface rough in the first substrates etched with this process. Since the 3μm upper cladding SiO_2 is thick enough, it is expected that such surface roughness will not have an impact on the buried SiON core of the dielectric waveguide and therefore the results will not be affected. For future generations of samples, a thicker coat of the resist or a different RIE system that allows a higher etch rate and more selective etch recipe can be used to address this concern.

After the RIE etch is completed, the residual resist is removed in hot Microstrip. Acetone in addition to swipes with a cotton swab can also be used to help remove any burnt and solidified resist. Then the Al/In bonding layer is deposited and patterned as before, while attention is given so that it only covers the edge of the recess whose $SiON/SiO_2$ was removed by RIE. The other recess sidewall should be clear so that laser beam can couple to the intact $SiON/SiO_2$ waveguide on the other side to give a comparison of integrated versus non-integrated structure outputs. Then, the chips are cleaved and polished, and the lasers are assembled in the recesses followed by the bonding step.

In the measurement setup, since the chips in this specific implementation are cleaved on both edges, they tend to be narrow and therefore the mount needs to be similarly thin. The reason is since changing probe positions, changes the emitted output power, in this specific measurement it is of critical importance that the probe positions are kept constant when the output power of with-waveguide and without-waveguide sides of the chip are being measured. Therefore, the mount needs to be narrow so that without changing probe positions, the large area Ge detector can measure the with-waveguide output power once and then be brought to the other side of the mount to measure the without-waveguide side power. An image of the modified setup to meet these requirements is shown in Figure 6- 66. Note that the mount used in this setup does not provide any temperature control and therefore the threshold currents are higher than usual.

Figure 6- 67 shows the microscope-zoomed top view image of this integrated laser under measurement, where the intact dielectric waveguide runs diagonally up and the side with the removed $SiON/SiO_2$ layer is at the bottom of the photo. The probe on the Al/In layer is positioned on the side of laser diode so that it does not block the emitted light from the $SiON/SiO_2$ removed facet.

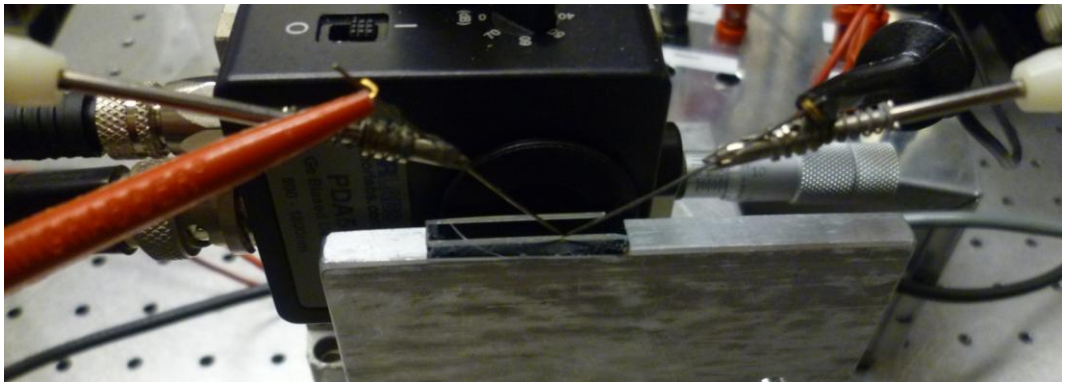


Figure 6- 66: Setup with narrow mount used for measuring one-side-waveguide-removed chips in order to estimate coupling loss, without changing probe positions.

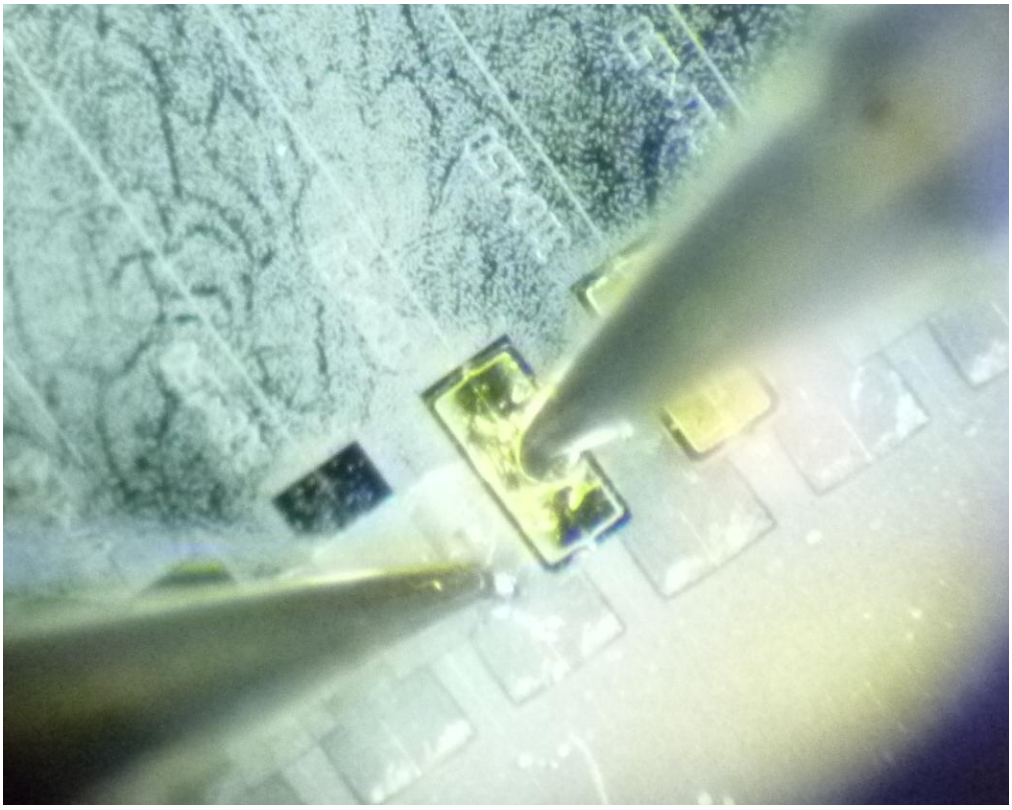


Figure 6- 67: Top view microscope-zoomed photograph of measuring the integrated laser in a recess with one end waveguide removed. On the upper half of the graph, the waveguides are intact.

Using the setup shown in Figure 6- 66 and measuring the pulsed LI response of a laser platelet integrated in a 309μm recess, from both the with-waveguide and without-waveguide sides (without any change to probe positions), the two LI responses shown in Figure 6- 68 are measured. By averaging the ratio of two powers above threshold, it is concluded that the power measured from the with-waveguide side is 0.56dB lower than the power measured from the without-waveguide side.

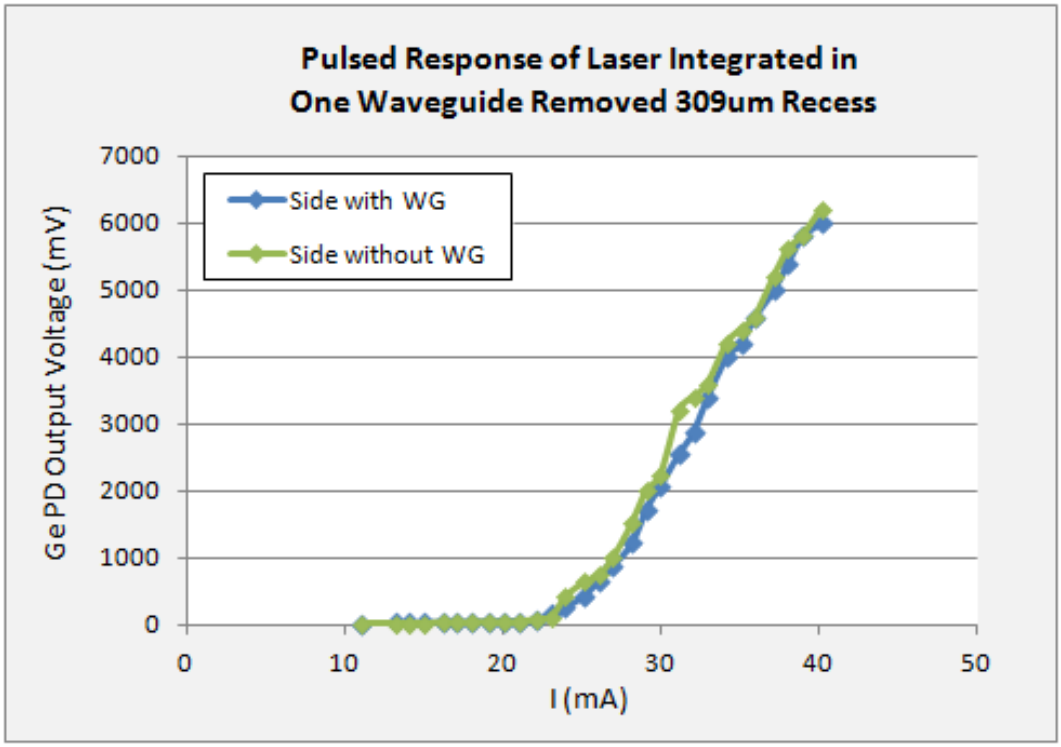


Figure 6- 68: Pulsed LI response of measuring with-waveguide and without-waveguide sides of the chip prepared for estimating coupling loss.

One might conclude that the coupling loss is simply the above measured average difference of 0.56dB. However by taking a closer look at the device under test in this configuration, one can realize that there are other contributing factors in this measurement that need to be taken into account. The schematic shown in Figure 6- 69 illustrates these factors, where P_1 represents the power that leaves laser facet at the waveguide-removed side of the integrated laser, and P_2 is the emitted power on the with-waveguide side of the recess.

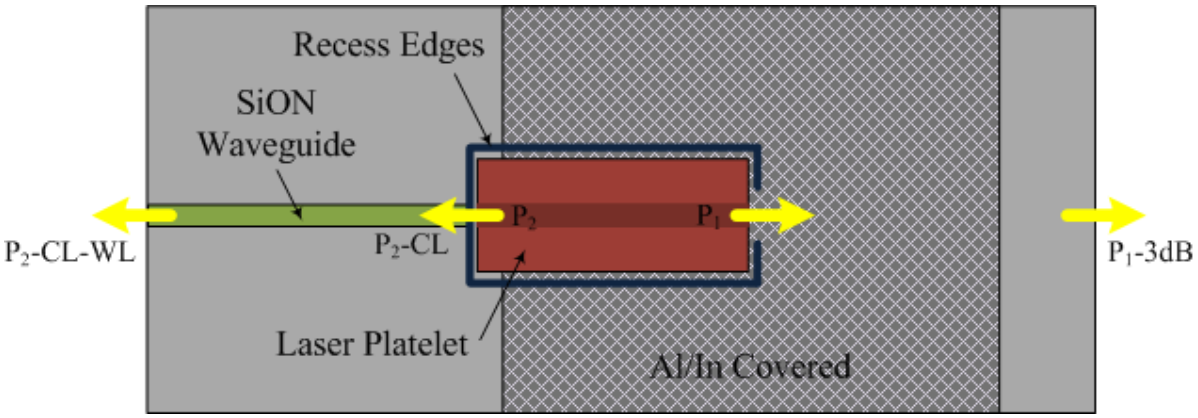


Figure 6- 69: Schematic showing the other contributing factors in the power readings from the two sides of one-side-waveguide-removed structure.

As it is illustrated in Figure 6- 69, due to the coupling loss (CL) between the laser and dielectric waveguide, P_2-CL enters the dielectric waveguide on the left. Since the waveguides on this chip are longer than before, the waveguide loss (WL) should be taken into account as well. Therefore, the power that leaves the with-waveguide side of the chip is P_2-CL-WL. On the other side of the wafer, P_1 leaves the laser platelet, but since the divergence angle is quite wide (half-divergence angle=35˚ as simulated in Section 6.5.4), the lower half of the beam hits the Al/In covered surface on chip. Since the In finish is rough, it is expected that the all of this lower half portion of the beam gets scattered. Therefore, the power that reaches the edge of the chip is P_1-3dB, accounting for the scattered lower half of the beam. Hence, from the 0.56dB averaged difference of the two output powers measured in Figure 6- 68, one can write:

$$P_2 - \text{Coupling Loss} - \text{Waveguide Loss} + 0.56\text{dB} = P_1 - 3\text{dB} \qquad \text{(Equation 6- 13)}$$

For a 2mm long dielectric waveguide and using 7.3dB/cm loss that was extracted in [59] for these fabricated waveguides, WL=0.2×7.3= 1.46dB.

Also one more interesting subtly in this structure is the asymmetric nature of the cavity, where two facets see different reflections and thus P_1 and P_2 are not equal. In fact based on effective reflections from each facet, the ratio of powers leaving a Fabry Perot cavity is given by

$$\frac{P_1}{P_2} = \frac{t_1^2 r_2}{t_2^2 r_1} \qquad \text{(Equation 6- 14)}$$

where $r_1=r_{\text{without-waveguide}}$ = 0.5232 and thus t_1=0.8522. On the with-waveguide side, effective reflection should be calculated from Equation 6- 2, which for a 1μm gap, gives $r_2=|r_{eff}|$= 0.585, and t_2=0.811. Using Equation 6- 14, P_1/P_2=1.2346=0.92dB. Including the waveguide loss, Equation 6- 13 becomes

$$P_2 - \text{Coupling Loss} - 1.46 + 0.56\text{dB} = P_2 + 0.92\text{dB} - 3\text{dB} \qquad \text{(Equation 6- 15)}$$

from which a coupling loss of 1.18dB is concluded.

This estimated value of coupling loss of about 1.2dB is in range with what was concluded comparing two different lasers shown in Table 6- 6. Unfortunately the laser integrated in the one-waveguide-removed structure measured here, got debonded by the strike of a probe before SEM images of its facets could be taken. Therefore information on the horizontal alignments of the two waveguides in this case is not available more than what the

microscopic images similar to Figure 6- 67 convey. In these photos, it can be seen that the two waveguides have a reasonable alignment. Overall, the laser platelet integrated in the 309µm recess here is a typical integrated laser, without any special efforts to pick the best aligned laser. Therefore the extracted low coupling loss of 1.2dB shows a typical value of the low loss that is easily achievable in this integration, given the coarse assembly setup available and human sight limitations. Therefore with an automated process, much better alignments and even lower coupling loss values can be easily achievable.

6.11. Summary

In this chapter the measurement results of the integrated laser platelets with dielectric waveguides were presented and analyzed for both pulsed and continuous wave operation. Infrared imaging verified the guided nature of the mode through the SiON dielectric waveguide. In addition, simulations were carried out to determine the effective refractive index of the fundamental modes of the two guides, their mode shapes, overlap and finally the far field mode distribution seen from the chip. Furthermore, from the CW lasing spectrum of these lasers, single mode lasing around λ=1.55µm was observed, and the effective length of the cavity was quantified through the spacing of axial modes. The significantly increased mode suppression ratio of the integrated structure over typical Fabry Perot cavity lasers, confirms the impact of external cavity in these integrated structures. Three-mirror external cavity model was employed to get an estimate for the MSR of the integrated lasers. External quantum efficiency and characteristic temperatures were also extracted for the integrated lasers. Finally, a series of methods to determine the coupling loss between the laser and dielectric waveguides in the integrated structure were presented and discussed. Based on these results it was found that the coupling between the laser and dielectric waveguides is quite good and the loss is very low for a typical integrated laser.

Chapter 7

Conclusion and Suggestions

In this final chapter, first we will summarize and review the attractions of coaxial integration approach, followed by the main contributions and findings of this thesis research. The third section will present the recommendations for further research to extend our understanding of several aspects in the design and optimization of recess integrated micro-cleaved laser platelets. Then, the recommendations for enhancements that can be made in the recess integration process will be discussed, and will be followed by conclusions.

7.1. Coaxial Recess Integration Approach

In this thesis, for the first time, coaxial integration of III/V laser platelets with waveguides on Si substrates is demonstrated. The innovative recess integration approach that was used is highly modular and results in a wafer that is essentially planar. It provides a very flexible solution for the long-standing problem of how to integrate photonic sources and amplifiers on silicon integrated circuits. This coaxial integration approach allows for device testing and selection prior to integration, and is very cost effective since it is not constrained by the need to bond a whole III/V wafer on a Si host substrate. Furthermore, the bonding phase is carried out at low temperatures and thus the integration is CMOS compatible. The modularity of the process allows the integration of lasers with different wavelengths, as shown in the schematic of Figure 7- 1, without the need to be confined to the limitations of quantum well intermixing. The planarity of the final integrated structure is also highly desirable for the subsequent packaging of the IC chip. In addition, in this integration technique the footprint of integrated lasers is very small and the impact on the density of

circuits on chip is further minimized by the fact that the recesses created for them are made in back-end processing steps on the upper surface of a processed IC chip or wafer.

Overall, we believe that this recess integration approach is quite promising in making on-chip optical interconnects feasible to meet the increasing bandwidth and speed requirements of the next generation of super computers and data centers. Equally important, it also enables the integration of a variety of optoelectronics, sensors, neurological probes and modules that cannot be realized now using the currently available technologies.

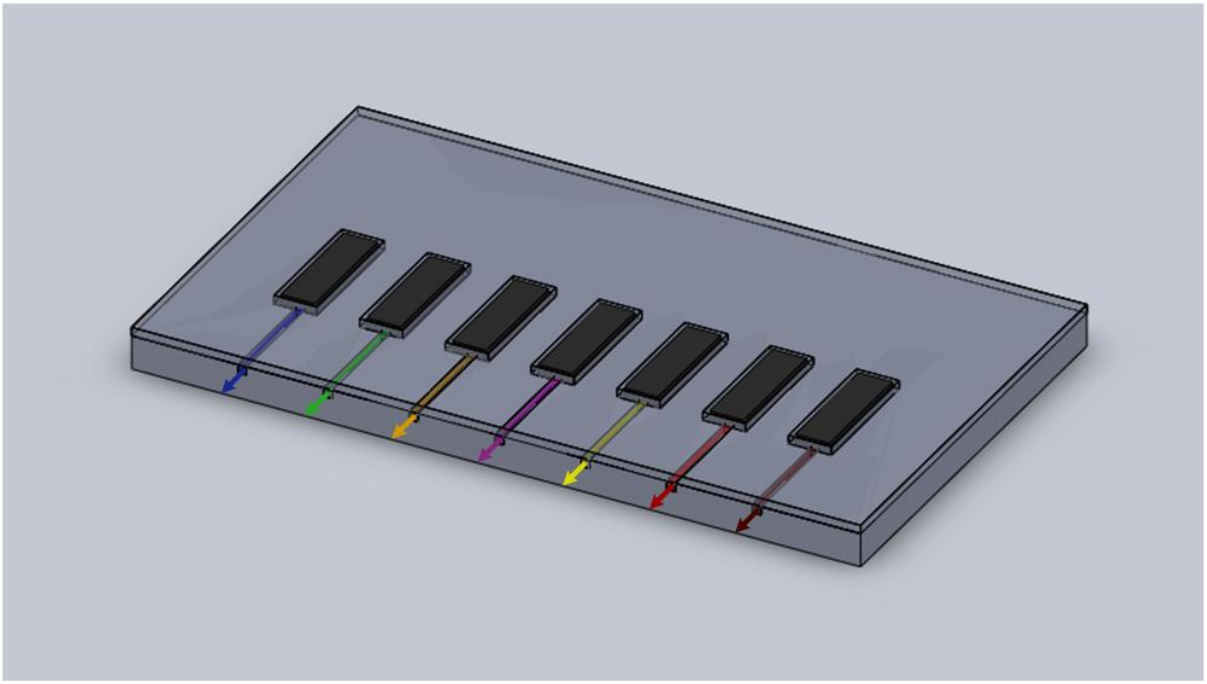


Figure 7- 1: Schematic showing the modularity of the recess integration approach, in which lasers at a diverse range of wavelengths from orange and blue in visible all the way to infrared are compactly integrable on one chip without any added complexity or cost to the process.

The coaxial recess integration technique does not suffer from the draw backs of older integration approaches like BGA bonding of the optochip onto the Si IC, heteroepitaxial growth of III/Vs on Si, Si-base lasers or the more recent Si-Hybrid approach (that involves bonding a III/V wafer on Si and the shared nature of the guided mode between the two), as discussed in Chapters 1 and 2. Therefore, based on its modularity, low cost and flexibility, the coaxial integration technique has the potential to provide the ultimate solution to efficient integration of laser sources on silicon.

Since the Si-Hybrid integration approach pursued by UCSB/Intel research group, has shown the most success compared to other attempts in realizing quality lasers on Si, in order to provide a side-by-side comparison of our coaxial recess integration approach with the Si-Hybrid integration method, Table 7- 1 provides a summary of the important criteria and the strengths and advantages of each method. For each criterion, a green square shows the strength of the corresponding approach whereas a red circle shows its relative weakness. Since the detailed discussion of each factor is already presented in Chapter 2, they will not be repeated here and Table 7- 1 serves as a summary of all the comparison presented there. Based on this comparison the more suitable method can be adopted by the industry based on the requirements of each specific application.

Criteria	Si-Hybrid Approach UCSB/Intel	Coaxial Recess Integration MIT
QW Overlap	●	■
Heat Transfer	●	■
Bond Delamination	●	■
Diversity of Devices	■	■
Integrability	●	■
III/V Material Waste	●	■
Footprint	●	■
Threshold Current	●	■
Device Footprint	●	■
Si waveguides	■	●
Planarity	●	■
Modularity	●	■
Very High Volume Integration	■	●
Pre-testing Lasers	●	■
Sensitive to Horizontal Alignment	■	●
Sensitive to Gap Length	■	●
Wavelength Range	●	■

Table 7- 1: Side-by-side comparison of the Si-Hybrid approach presented by UCSB/Intel and the coaxial recess integration approach pursued by our group at MIT. Green squares show a strength, while red circles show a relative weakness of each approach based on the corresponding criterion.

7.2. Achievements of This Research

In this thesis the first demonstration of the recess integration of InGaAs/InP laser platelets coaxially coupled with SiON/SiO_2 waveguides is illustrated. The lasers have the dimensions of 300µm×150µm×6.3µm, and are mounted and bonded in deep-etched recesses in a thick SiO_2 layer deposited on a Si substrate. A carefully optimized solder-bonding thin film sequence of Al/In is used for the purposes of providing a strong mechanical bond as well as bringing the backside contact of laser platelet to the front side of chip. The height of this layer is optimized for the best vertical alignment of the active region of the laser platelet with the SiON core of the dielectric waveguide, in order to reach the best coupling between the two waveguides.

The integrated lasers show threshold currents of 17mA for pulsed operation and 19mA for continuous wave (CW) operation[1] at T=15˚. In CW operation, the spectrum of the integrated structure shows single mode lasing at λ=1549.7nm with I=30mA. A mode suppression ratio (MSR) of 25dB is observable in the spectrum of these lasers, which is about 10-15dB higher than typical Fabry Perot lasers. From the three-mirror cavity model it is expected that the increased MSR is the result of the frequency dependent mirror loss, which is in turn due to the presence of external cavity composed of air gaps and SiON waveguide. Furthermore, using infrared imaging, the output beam shape of the integrated lasers was investigated and guiding through the SiON waveguide was confirmed.

In addition to external quantum efficiency, the characteristic temperature of integrated lasers is extracted to be T_0=76K compared to T_0=60K for the non-integrated lasers. Higher characteristic temperature is desirable and shows the lower sensitivity of the threshold current to temperature increase, and can be the result of enhanced heat transfer to the substrate for the integrated lasers. Finally a very low coupling loss of about 1.2dB is estimated to occur between the laser and dielectric waveguides for a typical integrated laser, which can be even further reduced by more precise horizontal alignment of the waveguides and a better match of their dimensions.

[1] These threshold currents meet the industry requirement of I_{th} to be lower than 20mA.

7.3. Future Work

7.3.1. Effect of External Cavity

One of the important factors that requires further study is the effect of the external cavity in the integrated structure. The external cavity is composed of the gap and the SiON waveguides that the laser is coaxially coupled to. The implications of the presence of such external cavity and how it affects the lasing operation, threshold current, mode suppression ratio and coupling loss, need to be further studied.

For instance, the measured side mode suppression is significantly higher than what would be expected for a typical cleaved-cavity laser diode, and a simple three-mirror cavity model suggests that such an MSR enhancement can be due to the frequency dependent effective reflection from the external cavity composed of gaps and dielectric waveguide. Further study is required to fully understand the effects of the gap length and its refractive index on this effective reflection, and its subsequent impact on MSR and threshold current.

By developing a better understanding on the effect and role of the external cavity, it might be possible to achieve an even higher side mode suppression ratio from the current MSR=25dB. In fact, for single mode operation of a laser diode, MSR=30dB is required. The enhanced value for MSR can be achieved by introducing a loss section or a DFB structure on the laser platelet, but it might also be feasible to reach the 30dB target through engineering the gap length or its refractive index.

Initial simulations have been carried out with Laser Matrix software to understand the effect of such external cavity on the MSR and other parameters of the integrated laser structure, however the results need more refinement at this stage, since although an MSR of about 30dB is derived from these simulations for the integrated structure, with gaps and SiON waveguides, the software results in MSR=0 for a bare Fabry Perot laser cavity even well above threshold, which makes the simulated results from this software unreliable at this stage.

7.3.2. Gap Filling

It was concluded in the simulations of Chapter 3 that a higher index gap filling material will enhance the coupling efficiency between the laser and dielectric waveguides. However, a higher index gap will also mean a lower facet reflectivity and thus a higher mirror loss, which will increase the threshold current. Therefore experiments need to be

carried out to optimize this tradeoff resulting from the refractive index of the gap filler material. Furthermore, the gap filling index will affect the frequency dependant $|r_{eff}|$ seen by the laser cavity looking into the external segment of the cavity, i.e. gap and SiON waveguide, which will in turn affect $\alpha_m(\lambda)$ and MSR. Study of integrated lasers with various gap lengths, gap filler refractive indices and the effect of these on the laser threshold current, coupling loss and MSR, will help us develop a better understanding of the integrated structure composite cavity, and therefore be able to optimize the refractive index of the gap filler material.

7.3.3. Removing Gap Sensitive Reflection

Since $|r_{eff}|$ is highly dependent on the length of the gap between the laser and dielectric waveguides, and the fact that the gap length may not be consistently similar among the various integrated lasers in recesses, it might be desirable to remove this sensitivity and its effects on I_{th}, MSR, and lasing spectrum of the integrated lasers.

In order to remove the effect of the reflecting beam coupling back to the laser cavity, the facets can be made at an angle, similar to semiconductor optical amplifiers (SOAs). Then an external DBR fabricated on the SiON waveguide will provide the required mirror reflection to achieve lasing. The schematic shown in Figure 7- 2 illustrates the idea of using angled facets in addition to external cavity DBRs for this purpose.

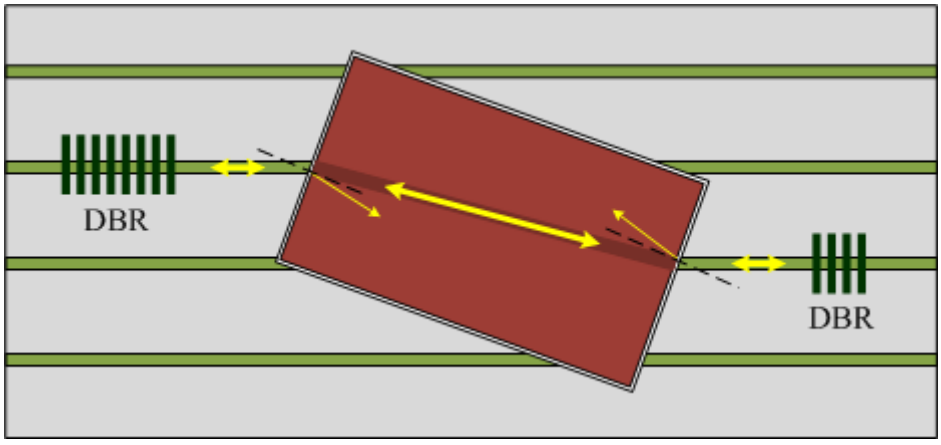


Figure 7- 2: Schematic showing a laser platelet with angled facets in order to remove the reflection from the air gap back to the laser cavity, and avoid its consequences. Instead the DBRs fabricated on the SiON waveguide provide the required mirror reflection for lasing.

7.4. Suggested Improvements

Overall, at this stage the success of the coaxial integration process is fully demonstrated. However, there is a range of enhancements that can improve the current generation of integrated devices. Since these structures have multiple components, in the following section, the suggested improvements regarding each component will be discussed separately. In general, there are not fundamental bottlenecks in this process that would prevent incorporating any of the suggested improvements. Therefore they can be employed with minimal added complexity and cost to this integration process. In the following, a set of these possible improvements will be discussed grouped by each device or process step.

7.4.1. InGaAs/InP Platelet Lasers

An important improvement in the laser platelets fabrication is the reduction of the laser ridge width. In the currently fabricated lasers, the ridge width is about 6.8µm and thus supports multi transverse modes. For very much desired single mode operation of lasers, it is critically important that the ridge width is reduced to below 3µm.

With a smaller ridge, alignment of the narrow ohmic contact on top will be marginally harder, but not a major issue. However, the more important impact of ridge width reduction will be in the increased sensitivity of horizontal alignment to the dielectric waveguides when the laser platelets are integrated in recesses. In fact, when the ridge width is reduced to below 3µm, a more accurate assembly setup is vital. With our current pick and place assembly setup, the magnification of the microscopes on hand had not been high enough to be able to very clearly see the state of horizontal alignment of the two waveguides (laser and dielectric). Should the setup have a higher magnification inspection tool, a finer and more accurate assembly is possible for ensuring a better alignment of smaller ridge lasers. Of course, when the process is automated, precision alignment is possible, which will remove the limitations of human visual microscope inspection and manual micro-positioning.

Reducing the laser ridge width will decrease the number of supported transverse modes, but it cannot reduce the axial multiple modes of the Fabry Perot laser cavity. At high enough currents, the gain curve provides enough gain to two or more of these axial modes and thus multimode lasing occurs for instance at I=40mA under CW operation.

Incorporating DBRs on the SiON/SiO_2 section of the structure is one solution to filter out some of the axial modes. However, from the preliminary simulations presented in

Chapter 3, it was seen that the designed DBRs have a very wide stop-band width that would not work in filtering the closely spaced ($\Delta\lambda \approx 1$nm) axial modes of the cavity. Therefore, the best solution to address the multi-axial modes with Fabry Perot planar lasers is using a DFB structure for the laser platelet. Such a structure is capable of providing single mode operation over a wide enough current range, and is a robust solution to the demand for single mode operation of the integrated lasers.

Another important improvement that can be made in the fabrication of laser platelets concerns their variation in length due to how they get micro-cleaved along the etched notches. The length of the laser platelet not only affects the Fabry Perot cavity definition and spacing of axial modes, but it is far more important in the mechanical fitting of laser platelets in recesses in the assembly phase. Contrary to the R&D nature of the first demonstration of this approach in this thesis, in commercial applications it is not feasible to make different length recesses on chip and thus having options to mount the lasers in the best fitting recess. Of course the best fitting laser to the fabricated recess on chip can be selected from a pool of released laser platelets. However, this search process adds to the cost and complexity of the assembly in this integration technique. If the length variation of laser platelets could be made smaller than 1µm, it would have been very beneficial in increasing yield and the consistency of gap lengths.

The length variation of the laser platelets can be reduced by making improvements in the notch design (discussed in Chapter 4). These notches provide a guideline for the subsequent micro-cleaving that takes place in ultrasonic agitation. If the notch pattern is made narrower, or in a taper form, there will be more restriction on where the micro-cleave can happen. Hence the length of released laser platelets will have less variation. This improvement can definitely be incorporated in the next generation of the micro-cleaved lasers for coaxial integration on Si ICs.

7.4.2. SiON/SiO_2 Waveguides

One important aspect of the coaxial integration approach that we demonstrated in this thesis is the fact that the integration phase is CMOS compatible, since the bonding temperature at 220˚C is below the 400˚C limit for CMOS circuits.

However, in the current generation of fabricated devices, the waveguides undergo a high temperature anneal (1050˚C for 4 hours) to remove the hydrogen atoms trapped in the waveguide core during DCVD deposition, which uses a hydrogen based curser (SiH_4). In

fact, not going to a high enough temperature and long enough anneal, these waveguides exhibit a high loss of 7.3dB/cm which is significantly higher than the 0.01dB/cm that has been reported [82] for $SiON/SiO_2$ waveguides[2].

In order to address the issue of loss introduced due to the presence of N-H bonds in the CVD deposited $SiON/SiO_2$ waveguides, and thus eliminate the need to high temperature anneal, non-hydrogen based pre-cursers can be used, such as sputtering from SiO_2 and co-sputtering from Si_3N_4 targets. In fact J. Sandland from Prof. Kimerling's group at MIT has devoted her PhD [106] to the material study of sputtered SiON for microphotonics applications. Also, Agnigotri et al reviewed the possible techniques to realize low loss SiN passivation layers and waveguides at low temperatures [107]. In [108] although the main-stream PECVD deposition technique has been used, Hoffman et al have achieved a low loss of below 0.4dB/cm for $SiON/SiO_2$ waveguides at 1.55μm by increasing the refractive index contrast of core and cladding and reducing the dimensions of the core. They claim that such a reduction in dimension will make the mode propagate more in the nearby SiO_2 cladding which has a very low loss, and thus the aggregate loss of the waveguide will be low. The process temperature in this case is below 400˚C and thus is CMOS compatible.

Therefore, in general the need for low temperature low loss $SiON/SiO_2$ waveguides has been the interest of many in the integrated photonics field, and reliable techniques have been developed to achieve this goal. These methods can be employed in the next generation of dielectric waveguides used in the coaxial integration technique discussed in this thesis, and their low temperature nature will make the whole process CMOS compatible.

Another improvement that can be made in fabricating the $SiON/SiO_2$ waveguides in this project is to achieve more vertical sidewalls with lower surface roughness for the SiON core during dry-etching step. Especially the surface roughness is important when waveguide dimensions are small, in order to support single transverse modes only. (Note that axial modes will be present even if the waveguide and laser both have single transverse modes. Axial modes can be filtered with a DFB structure for the laser platelet.)

Another concern is about the planarity of the final integrated structure. One attractive feature of coaxial integration approach is its potential for a planar final chip which is very desirable in the integration and packaging of ICs. However, in the current demonstration in this project, the final chip is not 100% planar. The height of laser claddings, recesses, and

[2] Although these reported low losses had been mainly for almost twice the width of the waveguides fabricated in this project. Having a wider waveguide reduces the losses due to core sidewall roughness caused during the definition of the core, therefore the waveguide width should also be taken into account comparing the losses.

dielectric waveguide lower claddings have been such that the final integrated laser, has about 1µm profile above the surface of the SiO_2 surface of the chip. A completely planar structure is achievable by modifying the InP lower cladding of laser platelet and SiO_2 lower cladding of dielectric waveguide accordingly. Alternatively one can use a polymer like BCB to planarize the wafer surface and also fill in the gaps.

7.4.3. Recesses

One immediate improvement that needs to be made in the next generation of recesses is to make sure the Si substrate is not etched in any phase of recess formation by avoiding the polysilicon hardmask. In fact a thick coat of a resist like AZ4620 can endure the deep well etch, as it was demonstrated in Chapter 6, and there is no need to use polysilicon hardmask (and the SiO_2 hardmask to pattern the polysilicon), which will avoid the complexity and the etched substrate consequences of it. As it was discussed in Chapter 5 and shown through cross sectional SEM images, although the recess dry-etch is nearly vertical in SiO_2, it is very much angled in Si. Such slanted circumference of the recess will prevent laser platelets from sitting well in the recesses. In the current implementation, the Al/In bonding layer is thick enough that it covers the 1µm over etch in the Si substrate and thus angled lower edges of the sidewalls were not an issue in this work, however this can be easily prevented in the next generation of devices.

Another factor that can be changed for recesses is their shape. If instead of rectangles, the corners of recesses and laser pills are patterned to be angled, the horizontal alignment of two waveguides might be enhanced.

7.4.4. Solder-Bonding Layer

The choice of Al/In as the solder bonding layer was suitable since it allowed bonding to happen at low temperatures (220˚C) and because it also was easily patterned in one process step. However, other metal sequences can also be used, for example Au/Sn, although the cost of depositing a thick layer of gold (about a micron) might make this material choice less attractive. Overall any layer sequence that meets the criteria for the bonding layer might be a candidate here and can be explored.

An important improvement that can be made in the bonding layer is to have a bright metal finish. Then, it could function as a good mirror for the side of cavity that is covered by the bonding layer to bring the laser platelet backside contact to the front side of the chip.

Currently the finish of indium is white which implies its surface roughness. This was confirmed by the granular appearance of deposited indium in SEM images and the profilometry surface roughness prior to bonding[3]. Therefore the indium that is covering the sidewalls is rough and will not effectively reflect most of the light back to the laser cavity from the covered recess sidewall. The assumption is that half of the laser output light is lost this way. Therefore if a bonding layer with a bright finish and thus high effective reflection could be used, it would be beneficial in reducing the mirror loss, and threshold current as a result.

7.4.5. Assembly Setup

Automation of the pick and place assembly phase is the major step to the commercial adoption of the coaxial integration approach. We believe that if this step is successfully automated, there would only be very small lead time until the full adoption of this technique for commercial applications. With such a system, precision assembly and accurate horizontal alignment of the waveguides is achievable. With the current manual assembly, such precision is severely limited by the small magnification of microscope lenses and by the user experience in assembling the platelets in recesses. The automated system can also perform a scan, and pick the best fitting laser platelet for a corresponding recess that has been fabricated on chip.

7.4.6. Bonder Setup

Yield can be highly increased if the bonding and assembly setup could be consolidated into one system, and sample transfer between the two was omitted, since prior to bonding, the assembled laser platelets are very prone to get dislocated out of their recesses during the transfer between the two setups. For an automated system, having the two functionalities in one setup is possible, and it is desirable for increasing the efficiency of the integration process.

One more immediate issue with the current bonding setup is the laser platelets sticking to the thermo-plastic membrane when the membrane is lifted from the chip surface at the end of the bonding phase. Lasers are also in the danger of getting attracted to the membrane before the bonding sequence gets started, if electrostatic charges build up on the

[3] Post bonding, the surface roughness is decreased at the bottom of recesses where lasers sit and pressure the molten In during bonding.

membrane. Such charges can be depleted by cleaning the membrane with a moist fab wipe and letting it dry with air or dry nitrogen. Any sweeping of the membrane with paper, gloves or wipes will build significant amount of electrostatic charge on the membrane and will attract light laser platelets to it, rendering the assembly effort in vain. One solution for this concern might be to coat the area of the membrane that gets in contact with samples, with a conductive layer.

Also it has been noticed that for bigger chip sizes of about an inch, samples tend to crack and break from the middle when pressured during the bonding phase. The pressure cannot be reduced further, as it is already close to the minimum value required to reach a strong mechanical bond. We believe the breaking of large samples in half is due to the curvature of the heating stripe, and can be addressed by adding more support to make sure the stripe does not bend down when the outer chamber is pressurized.

Furthermore, since the melting point of indium is 156˚C, the maximum temperature of bonding step does not need to be as high as 220˚C (as is in the current process). Therefore, bonding temperature can safely be reduced to 180˚C if the thermocouple controlling the heating stripe temperature is placed near the sample and has an accurate reading of the actual temperature that the sample feels.

7.4.7. Gap Filler Material

Simulations of Chapter 3 indicated that coupling between the laser and dielectric waveguides will be enhanced by a gap filler with a higher refractive index than air. Although simulations have indicated that n_{gap}=2.2 provides the best coupling advantage, filling the gap with a material with this refractive index (i.e. Si_3N_4) may not be straight forward considering the tight opening of the gap (1µm or even less) and its high depth (6 to 7µm). However the simulations of Chapter 3 also suggested that n_{gap}=1.5 still provides a significant improvement over the air gap, and does not differ vastly from the coupling enhancement that a higher index filler with n_{gap}=2.2 gives. Since filling the gap with BCB for instance is easier, and because it has the refractive index of n=1.54 [109], this options seems to be simpler to implement in the next generation of integrated lasers with a gap filler other than air.

However, having a higher index gap filler also reduces Fresnel reflection from laser facets and thus increases mirror loss of the laser cavity. This might result in higher threshold currents or may even prevent lasing. In such a case the introduction of a DBR (as designed in Chapter 3) on one of SiON waveguides might help to decrease the effective mirror loss and

compensate for lower reflection that the lasing mode sees in the laser Fabry Perot cavity due to higher refractive index of the gap filler compared to air.

Therefore, as discussed in Section 7.3.2, the effect of such gap filler material needs further study and experimentation to optimize considering its tradeoff in coupling between the two waveguides and the mirror loss of the laser cavity.

7.4.8. Si Waveguides

In the current demonstration of coaxial integration approach, $SiON/SiO_2$ waveguides have been used. Since Si waveguides are gradually becoming the preferred choice in the photonic integration industry, in the next generation of coaxial integration, Si waveguides can be used instead of the $SiON/SiO_2$ dielectric waveguides. Since the refractive index of Si is higher than SiON, the cross section of a Si waveguide is smaller (a few hundred nm) to sustain a single transverse guided mode. In case such smaller waveguide dimensions pose a difficulty in achieving a great horizontal alignment of the two waveguides, a spot converter taper can be used, in which initially the Si guide has a larger cross section and then through a well-designed taper, turns to a smaller cross section desired for a single mode Si waveguide. The vertical and rotational misalignments can be easily avoided by careful optimization of the thin film solder-bonding layer height, as it was demonstrated in this thesis, and the shape of the recesses.

7.5. Conclusion

In summary, in this project the successful coaxial integration of laser platelets with dielectric waveguides on a Si substrate is demonstrated. We believe this recess integration approach is highly modular and flexible, and has a very promising potential to meet the need of the industry for efficient integrated sources on chip. The foot-print of the integrated lasers is also very small, which is an important criterion for on-chip integration of laser sources on ICs. Furthermore, this integration approach is CMOS compatible, low cost, and allows very compact integration of lasers of different wavelengths on the same chip. With further improvements to the process, such as the automation of the assembly phase, this integration approach has a high potential to be adopted by the industry for high performance commercial applications.

Appendix I

Calculation of Hybrid Evanescent Device Specifications

In this appendix, photodetector responsivity and threshold currents for Fabry Perot cavity and race-track lasers made with Si-Hybrid approach (discussed in Chapter 2) are calculated, as well as checking the typical QW overlap value in these structures.

AI.1. Photodetector Responsivity Derivation

Photodetector fabricated in Hybrid Evanescent technology has the following reported parameters [65]:

$\eta_{\text{internal QW}}$ = 90%, Γ_{QW}= 4%, Γ_{Si} = 63%, L=400μm, h_{QW}=0.146μm, W_{mesa} = 12μm

$\alpha_{\text{absorption}}$ = 1596 cm $^{-1}$, Internal Responsivity= 1.1 A/W

$$I = \frac{P_0}{h\nu} \times \eta_{QW} \times q$$

$$R = \frac{I}{P_0} = \frac{\eta_{QW} \cdot q}{\int \bar{h}\omega}$$

where R stands for responsivity. For simplicity we take into account only one wavelength in which the detector absorbs light (central wavelength of absorption spectrum: 1.5μm):

$$R = \frac{I}{P_0} = \frac{0.9}{1.24/1.5} = 1.088$$

(For photon energy, approximate formula of $E = \frac{1.24}{\lambda}$ was used.)

Thus the calculated responsivity is 1.09 A/W, which is a very close match to the reported responsivity of 1.1 A/W [65].

AI.2. Edge Emitting Laser Threshold Current Calculation

Edge emitting laser fabricated in Hybrid Evanescent technology has the following reported parameters [63]:

R=80% (power reflectivity, with high reflection coating), L=800μm, η_d=12.7%, α_i=15 cm^{-1} (modal loss), Γ_{QW} = 3%

Assuming η_i=70% (from race-track laser case), g_0=1500 cm^{-1}, N_0=1.85*10^{18} (for AlGaInAs QWs), will yield:

$$\alpha_m = \frac{1}{2L}\ln(\frac{1}{R_1 R_2}) = 2.79cm^{-1}$$

$$\Gamma g = \alpha_m + \alpha_i = 17.79cm^{-1}$$

Since Γ_{QW}=3%, $g_{th} = \frac{17.79}{0.03} = 592.98cm^{-1}$, the threshold electron density will be:

$$N_{th} = N_0 e^{g_{th}/g_0} = 1.85*10^{18} * e^{59298/1500} = 2.75*10^{18}cm^{-3}$$

And thus

$$\frac{I_{th}}{V_{ac}} = \frac{1.6*10^{19}}{0.7}(0.8*10^{-10}(2.75*10^{18})^2 + 3.5*10^{-30}(2.75*10^{18})^3) = 1.55*10^8[A/cm^3]$$

$$V_{ac} = h_{QW} \cdot W_{mesa} \cdot L_{mesa} = 0.146*4*800*10^{-12} = 4.672*10^{-10}$$

$$I_{th} = V_{ac} * 1.55*10^8 = 0.072[A] = 72[mA]$$

Therefore the calculated threshold current is 72mA which is close to the measured and reported I_{th}=65mA [63], where the discrepancy mainly resides in the inaccuracy in selecting N_0 and g_0 for this material system.

AI.3. Race-track Laser Threshold Current Calculation

Race-track laser fabricated in Hybrid Evanescent technology has the following reported parameters [66]: R=80% (with high reflection coating), L=2656μm, α_i=15 cm^{-1} (modal loss), η_i =70%, g_0=1500 cm^{-1},

Assume: Γ_{QW}= 4%, $N_{0(AlGaInAs\ QWs)}$=$1.85*10^{18}$, B=$0.8*10^{-10}$ [cm^3/s], C=$3.5*10^{-30}$ [cm^6/s].

In the race-track structure, there is no facet thus, $\alpha_m = 0$, and hence: $\Gamma g = \alpha_m + \alpha_i = 15cm^{-1}$

which leads to $g_{th} = \frac{15}{0.04} = 375cm^{-1}$, and therefore threshold electron density would be:

$$N_{th} = N_0 e^{g_{th}/g_0} = 1.85*10^{18} * e^{375/1500} = 2.38*10^{18} cm^{-3}$$

Then

$$\frac{I_{th}}{V_{ac}} = \frac{q}{\eta} \cdot (B \cdot N_{th}^2 + C \cdot N_{th}^3) = \frac{1.6*10^{19}}{0.7}(0.8*10^{-10}(2.38*10^{18})^2 + 3.5*10^{-30}(2.38*10^{18})^3)$$

$$= 1.14*10^8 [A/cm^3]$$

$$V_{ac} = h_{QW} \cdot W_{mesa} \cdot L_{mesa} = 0.146*4*2656*10^{-12} = 1.55*10^{-9}[cm^3]$$

$$I_{th} = V_{ac} * 1.14*10^8 = 0.177[A] = 177[mA]$$

Hence, the calculated threshold current is 177mA which is very close to the measured and reported I_{th}=175mA [66], where the discrepancy can be corrected by a better selection of B, C and N_0 parameters for this material system.

AI.4. Quantum Well Confinement Factor Reality Check

Intel/UCSB papers have reported Γ_{QW}=4%. Typical laser diode QW overlap per QW is about 1.5%. Since in the hybrid structure there are 8 wells and 9 barriers, n_{QW}=8 and thus Γ_{QW}= Γ_{QW}/well×n_{QW}=0.0115×8=0.12. Thus a typical laser diode structure would have 12% overlap while the hybrid structure gives 4% overlap. This 3 fold reduction from the typical value is attributed to the evanescent coupling characteristic of the hybrid-evanescent technology and low overlap of the guided mode with the III/V gain layer bonded on top.

Appendix II

Calibrating Ge PD Output Voltage

In order to translate the voltage output of the Ge photodetector to the actual optical power seen from the outgoing facet of the integrated structure, initially the datasheet of the PD was consulted. According to Thorlabs PDA10B manual [105], R(λ), the spectral responsivity, of this detector peaks at λ=1550nm, as shown in Figure AII- 1, with R(λ=1.55μm)≈0.85. For each gain, the transimpedance gain (V/I) of the detector can be found according to Table AII- 1, which is presented for a Hi-Z load. If the detector is terminated with a 50Ω load, the response will be halved since the PD has an output resistance of 50Ω.

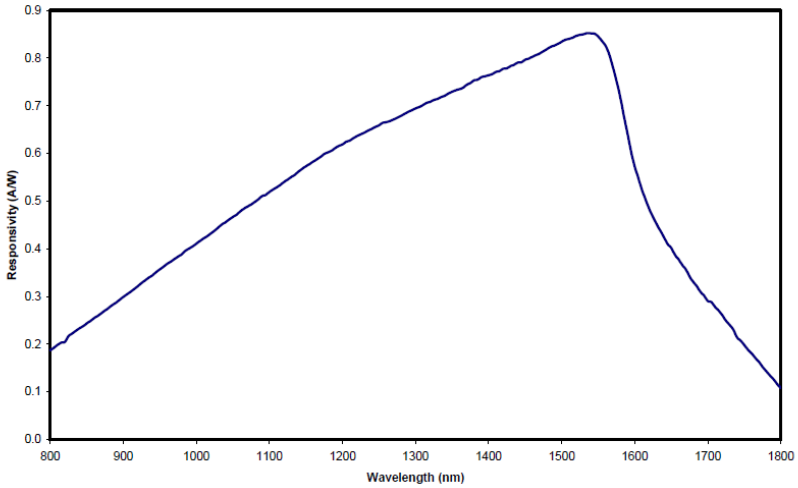


Figure AII- 1: Spectral responsivity of Ge PDA10B, which peaks at λ=1550nm.

Gain	Transimpedance Gain (V/I)
0 dB	1.51×10^3
10 dB	4.75×10^3
20 dB	1.5×10^4
30 dB	4.75×10^4
40 dB	1.51×10^5
50 dB	4.75×10^5
60 dB	1.5×10^6
70 dB	4.75×10^6

Table AII- 1: Ge PD V/I response for different gains, based on the product manual for a Hi-Z load.

Therefore the voltage-to-light conversion of this detector output will ideally be as follows:

$$A = \text{Output [V/W]} = \text{Transimpedance Gain [V/A]} \times R(\lambda)\ \text{[A/W]} \times \text{Scale Factor}$$

The scale factor is the due to the voltage division between the load and the output resistance of the photodetector (which is 50Ω). Therefore if a Hi-Z load is used, scale factor is 1 and for the case of R_{load} = 50Ω, the scale factor will be 0.5.

Therefore, for the gain of 30dB used in the pulsed measurements presented in Chapter 6, responsivity of R (λ=1550nm) = 0.85, and scale factor = 1 for the Hi-Z input impedance of oscilloscope used to read the peak to peak values of the pulsed output response,

$$A = \text{Output [V/W]} = 4.75 \times 10^4 \times 0.85 \times 1 = 4.04 \times 10^4$$

However, further investigation of the gained response of this Ge PD, shows that Table AII- 1 mentioned in specs is not perfectly accurate. In fact, as depicted in Figure AII- 2, the response does not by any means change exponentially when the PD gain is changed from 0dB to 70dB, keeping the input current constant at 20mA. In fact by a closer look one can conclude that the gain at 30dB is only 3 times compared to the case of no gain (0dB). In this measurement the PD output was connected by a BNC cable to the oscilloscope (i.e. R_{load}=1MΩ), therefore PD sees a Hi-Z load. The same trend was observed using R_{load}=50Ω with the only difference that the output voltage was halved in that case[138].

[138] Contacting the product support of Thorlabs regarding this issue, they suggested a 50Ω load should be used. However using such load did not change the trend and only cut the response in half consistently for various gains.

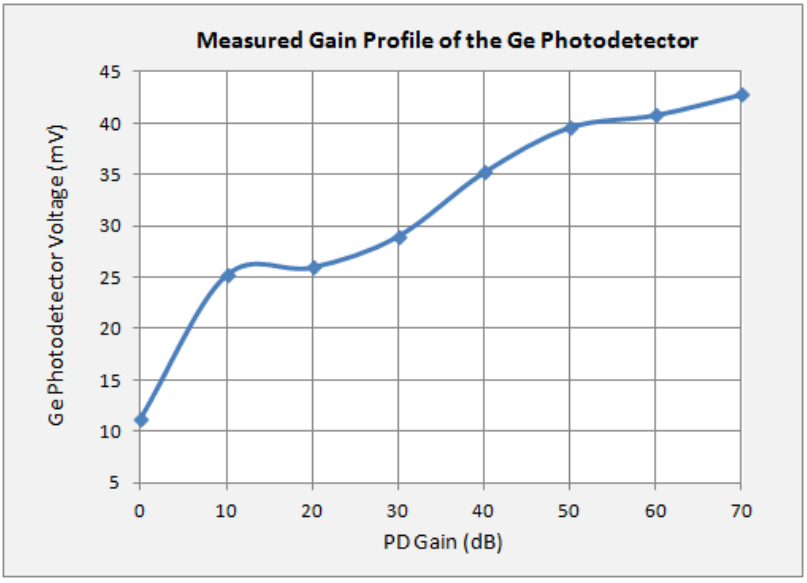


Figure AII- 2: Measured gain profile of Ge photodetector with constant I=20mA. A rather linear trend is observed, which is in contrast to the exponential expectation from product datasheet.

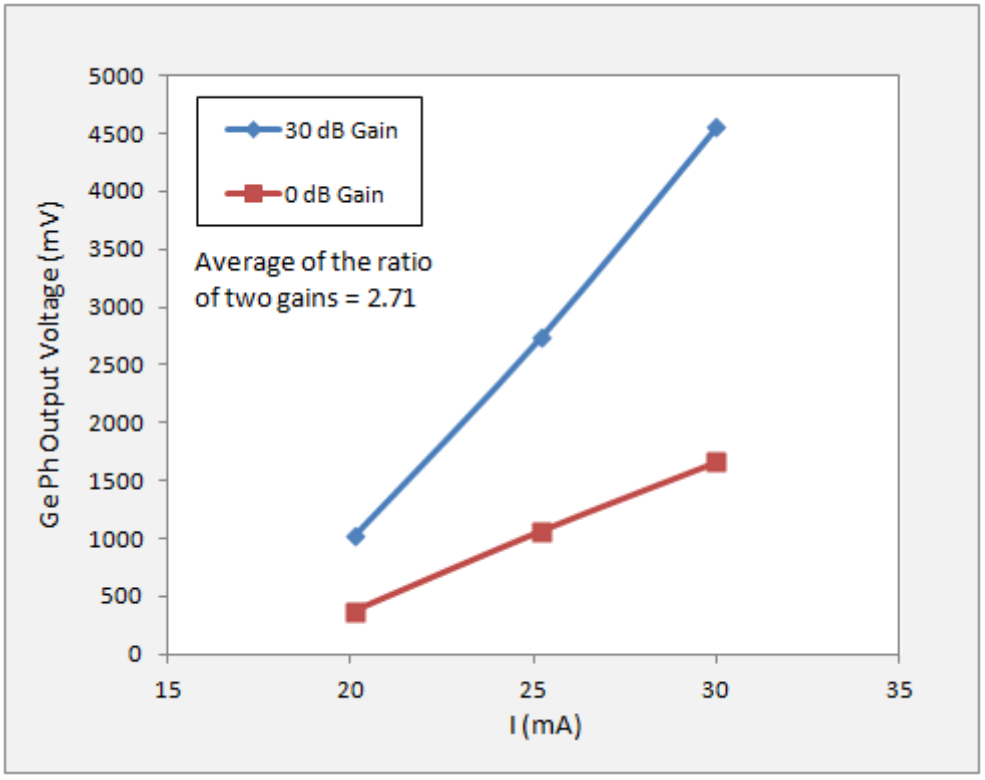


Figure AII- 3: Output response of the Ge PD for pulsed lasing operation of the laser bonded in 312µm recess. Two gains of 30dB and 0dB were used and the ratio of detector output voltages was calculated for each input current. The ratios averages to 2.7 in contrast to 31.5 expected from Table AII- 1.

To verify this observation that the gain at 30dB is about three times of the response at 0dB gain, with this Ge PD and Hi-Z oscilloscope load, another set of measurements were carried out for the laser integrated in 312μm recess, whose response was depicted in Figure 6- 7. Through dividing the PD output voltage for 30dB and 0dB gains (see Figure AII- 3), an average ratio of 2.7 was derived, which is considerably different from 31.5 ratio expected from Table AII- 1.

This approximate calibration factor of 2.7 is used in calculating the actual optical output based on the voltage readings from this Ge PD.

Hence, the calibrated output optical power is calculated as follows:

$$A = V / W \rightarrow W = V/A$$

$$A_{30dB\text{-}adjusted} = \text{calibrating factor} \times A_{0dB}$$

$$A_{30dB\text{-}adjusted} \approx 2.7 \times 1.51 \times 10^3 \times 0.85 \times 1 = 3.47 \times 10^3$$

This calibrated factor is used in Chapter 6 to derive the optical output power from the voltage reading of the Ge PD with 30dB gain.

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