Design of Low-voltage, High-bandwidth Radio Frequency Power Converters

by

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Abstract

The mass and volume required for power electronics circuitry is a dominant obstacle to the miniaturization and integration of many systems. Likewise, power electronics with greater bandwidth and efficiency are becoming vital in many applications. To realize smaller and highly responsive power electronics at low voltages, this thesis explores devices, circuits, and passives capable of operating efficiently at very high frequencies (VHF, 30-300 MHz). Operation at these frequencies enables reduction of the numerical values and physical size of the passive components that dominate power converters, and enables increased bandwidth and transient performance which is valuable in a multitude of low-voltage and low-power applications.

This thesis explores the scaling of magnetic component size with frequency, and it is shown that substantial miniaturization is possible with increased frequencies even considering material and heat transfer limitations. Moreover, the impact of frequency scaling of power converters on magnetic components is investigated for different design criteria. Quantitative examples of magnetics scaling are provided that clearly demonstrate the benefits and opportunities in VHF magnetics design.

It is shown to utilize the advantages of frequency scaling on passive component size that system losses and other limitations must be considered. One such area that is examined is semiconductor device requirements, where through a combination of device layout optimization for cascode structures and integrated gate drive designs on a 0.35-um CMOS process, converter performance (i.e., loss and bandwidth) can be significantly improved in the VHF regime.

In this thesis a dc-dc converter topology is developed that is suitable for low-voltage power conversion and employs synchronous rectification to improve efficiency. The converter is also comprised of a high-bandwidth and high-switching-frequency inverter topology that can dynamically adjust the output power from one-quarter to full power, while maintaining good efficiency. Furthermore, with its inherent capability of gate-width switching, the inverter can further reduce gating loss by one-half resulting in substantial performance improvements at light load operation.

A major contribution of this thesis is the development of a synchronous rectifier operating in the VHF regime. VHF power conversion is especially challenging at low voltages due to poor efficiency resulting from rectification loss. To overcome diode rectification loss, the benefits of synchronous rectification are discussed in the context of a 100MHz class-E resonant rectifier, which results in a 2.5× overall converter efficiency improvement. The culmination of the developed design techniques in passives, semiconductor devices, and circuit topologies is an experimental prototype of a miniaturized 100MHz, 1W power converter utilizing synchronous rectification.

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Chapter 1

Introduction

THE SIZE of power conversion electronics is a dominant obstacle to achieving further miniaturization and integration of many modern mobile and communication systems. Moreover, power electronics having higher efficiency and control bandwidth are important for reducing the overall energy consumption of communications electronics.

In spite of the need for smaller and better dc-dc power converters, it is difficult for many existing conventional power converter designs to provide wide operation range while maintaining high efficiency and a small volume. Furthermore, while switched mode power supplies (SMPS) have taken advantage of scaling trends in the form of improved semiconductors and higher integration, the bulk energy storage (comprising most of the volume) required at contemporary switching frequencies of a few megahertz and below has not scaled to the same degree, leaving most commercial converters with a not-so-subtle footprint. Shrinking passive component volume at constant numerical component value and energy storage is one obvious way to target the needs for a smaller converter. However, fundamental scaling issues that bring efficiency down beyond acceptable limits make this approach impractical.

An alternative method to resolve the tradeoffs between small size and high efficiency is to reduce the required energy storage and passive component values by increasing the switching frequency [2]. The numerical values and energy storage requirements of energy storage elements (e.g., inductors and capacitors) required to achieve a given conversion function vary inversely with switching frequency (see, e.g., [2, Chapter 6]). Moreover, a higher switching frequency and reduced intermediate energy storage enable faster response to load transients and reduce the size of ancillary filter components (e.g. output capacitors). Higher switching frequencies can considerably widen converter control-loop bandwidth, which is typically limited to about a tenth of the switching frequency.
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The advantages of increasing switching frequency suggest that this method may hold the key to achieving designs that can meet all the demands of the next generation mobile and communication systems. This, in fact, has been an ongoing pursuit in power electronics since at least the 1970's [3] as switching frequencies have risen from tens of kilohertz to a few megahertz.

To design power converters at radically increased switching frequencies that attain significant reduction in passive component size requires leveraging semiconductor device technology, novel circuit topologies, and unconventional system architectures. Such designs also benefit from increased integration of devices (especially including integrated circuit technology), improved passive components, and better packaging. This thesis will develop design techniques for high-performance, low-voltage dc–dc power converters. Design of suitable switching circuits and integrated gate drivers in CMOS technology will be explored, along with improved controls and their application in various circuit topologies and functions. Together, these approaches will address design challenges associated with high-efficiency and high-bandwidth power conversion at low voltages. The new architectures, circuits and controls considered are expected to enable substantial miniaturization and improve response speed of inverters and dc–dc converters, and to permit improved performance in multiple applications.

1.1 Challenges of Increasing Converter Switching Frequency

A typical switched-mode power stage consists of semiconductor devices and passive energy storage elements. While losses are distributed among the active and passive components in the power stage of a converter, the bulk of the system mainly resides in the volume of the passive elements. Increasing operating frequency can significantly improve the size, cost and transient response of the system. However, increasing power loss at higher operating frequency in conventional converters places an upper bound on the switching frequency.

Switching power MOSFETs have experienced tremendous improvements in the last twenty years, yielding devices with lower on-state resistance and smaller packages. However, under high frequency operation, switching loss (including loss associated discharging the output capacitance and overlap loss), instead of conduction loss, becomes the dominant loss
1.1 Challenges of Increasing Converter Switching Frequency

mechanism in a conventional hard-switched converter. This has imposed a upper limit on acceptable switching frequencies in such converters.

Another loss mechanism closely related to the characteristics of switching devices such as MOSFETs is gating loss, which results from charging and discharging the device input capacitance, $C_{iss}$. For both lateral and vertical MOSFETs, gating loss has a linear dependency on the switching frequency [4, 5]. In the case of a conventional hard-switched converter, the gating loss is described by the following equation:

$$ P_{GATE} = Q_{GATE} V_{GATE} f = C_{GATE} V_{GATE}^2 f $$

(1.1)

For a typical commercial 20V vertical MOSFET having a 2A current rating with effective gate capacitance of 200 pF operating at a switching frequency of a few megahertz, the loss is measured from hundreds of milliwatts to over a watt, which makes the efficiency unacceptable for low-voltage, low-power designs.

In addition to the conduction loss, switching loss and gating loss associated the semiconductor devices, frequency-dependent losses resides in the magnetic components are yet another loss mechanism eating away efficiency. Inductors, incorporating conventional magnetic materials may operate fine at low frequency. However, As the frequency is scaled up, core losses, captured by the Steinmetz equation 1.2, imposes a fundamental operating frequency limit of these materials. For conventional cored inductor, this frequency limit doesn't usually exceed a few megahertz, beyond which magnetics loss increases substantially.

$$ P_s(t) = k f^a B^b $$

(1.2)

Altogether, these major loss mechanisms associated with conventional converter designs suggest that alternative design methods must be exploited to improve converter performance if we are to increase switching frequency to reduce the volume of modern switch mode power supplies.
Introduction

![Class E Inverter](image)

Figure 1.1: Class E Inverter

1.2 Very High Frequency Resonant Power Conversion

The predicted poor performance of conventional hard-switched converters at high frequency, exacerbated in the case of low-power converters, suggests that resonant power conversion may be a more viable candidate as the switching frequency moves beyond a few megahertz.

Efficient power conversion at high frequency has been achieved using switched-mode RF inverters taking advantage of zero-voltage switching (ZVS) [3–19]. Inverters like the Class E inverter [6–8], Figure 4.4, have been popular in various applications. By utilizing reactive elements to shape the voltage and current waveforms, resonant power conversion can eliminate the significant amount of switching loss faced by traditional hard-switched converters at higher operating frequencies. Taking the advantages of resonant network one step further, gating loss can also be significantly reduced when a resonant network recycling a portion of the gate energy each cycle is utilized to drive the gate [4,5,18–24].

However, resonant power conversion has its own challenges, which limits its range of use. Reactive elements in resonant topologies are usually tuned to provide desirable ZVS performance (and high efficiency) at a single operating point. However, as the load moves away from the nominal load value, with which the resonant topology is tuned, converter performance can plummet. Furthermore, designing a suitable control method is also a non-trivial issue. Duty ratio control becomes difficult (if not impossible) to implement for resonant converters at high frequencies. Controlling power by varying switching frequency yields varying component stresses and efficiency reductions across load control limitations become yet another drawback for high frequency resonant converters.
Burst mode control \[4,15,18,24,25\] has been shown to address the control challenges above, by separating the control function from the power stage operation of the converter, Figure 1.2. The converter cell is switched on and off at a modulation frequency, often much lower than the converter switching frequency, to control the average power delivered to the output. When the converter is on, it delivers a fixed power maintaining ZVS characteristics and good efficiency. When off, no power is delivered and there is no associated resonating loss. A particular implementation of this on/off control method \[26\], enables fast transient response and efficient light-load operation while providing controlled spectral characteristics of the input and output waveforms, which makes this control method suitable in a variety of applications (such as communication systems). In addition, a hysteretic override technique may further allow the converter to reject load disturbances with a bandwidth much greater than the modulation frequency, limiting output voltage disturbances to within a fixed value. Such operation allows the network to be tuned to enforce ZVS at one particular operating point. The result is maximum efficiency, better dynamics, and higher achievable operating frequency. The fact that this mode of operation allows much higher switching frequency is self-reinforcing—high frequency means less energy storage so the converter can be started and stopped more rapidly and achieve a wider load range.

1.3 Contributions and Organization of the Thesis

As suggested in the previous discussion, VHF resonant power conversion is a suitable design method for low power converters to meet the two major concerns of future portable electronic systems, namely, efficiency and volume. Utilizing air-core inductors with rea-
Introduction

Reasonable $Q$s in the range of 60-120 operating at VHF regime can completely eliminate the frequency-dependent core losses. For capacitors, VHF operations reduce the total required capacitance value, leading to much smaller volume.

The primary goal of this thesis is to develop designs and techniques suitable for high-bandwidth RF power conversion at low voltages. There are three major areas that this thesis work will focus on: passives, devices, and circuits. The following chapters will address the topics in turn.

Chapter 2 explores magnetics design tradeoffs and scaling in VHF dc-dc converters, and examines how the physical sizes of magnetic components change with increasing frequency for different design options. We provide quantitative examples of magnetics scaling, and also point to opportunities in VHF magnetics design.

Chapter 3 examines methods to improve upon performance achievable via commercial off-the-shelf semiconductors for use in VHF applications. The variety and quality of discrete commercial MOSFETs with breakdown voltages lower than 20 V are very limited. Even the available ones are generally optimized for hard-switched applications. One can thus realize substantial performance improvements by designing customized devices in an integrated CMOS process. With custom design, one can attain significant reduction in switching, conduction and gating loss via modifying device layout, device packaging and extending safe operating area (SOA) in a low-voltage CMOS process. However, even when an optimal device geometry (for a given design) has been determined, driving the input capacitance of such a device at tens to hundreds of MHz is not a trivial issue. Integrating gate drivers on the same process introduces even more opportunities to achieve better performance.

Through the magnetics scaling analysis, the most desirable range of operating frequencies can be determined. From which, a device geometry can also be reached via the device optimization algorithm along with a low-power gate driver design. Chapter 4 explores various circuit topologies as a means to leverage the optimized device/gate drive design in the tens to hundreds of MHz operating regime. Specifically, a inverter topology operating at hundreds of MHzs that can dynamically adjust the output power from full power to 1/4 of the full power level is introduced. Furthermore, this topology allows for an alternative gating scheme that further cuts down the gating loss by half, which directly translates to substantial performance improvements at light load. This topology operates at fixed


1.3 Contributions and Organization of the Thesis

frequency and duty ratio. It eliminates the need for bulk inductors and provides excellent transient response. Compared to its counterparts, this design is specifically optimized to address the unique challenges of high-bandwidth low-voltage low-power designs.

Chapter 5 presents a full dc-dc converter utilizing the inverter topology discussed in Chapter 4. Advantages of synchronous rectification at low voltages is discussed in the context of a 100MHz class-E synchronous rectifier. The culmination of the developed design techniques in passives, semiconductor devices, and circuit topologies is an experimental prototype of a miniaturized 100MHz, 1W power converter utilizing synchronous rectification.

Resonant power conversion at VHF regime has proven its merits in the context of a low-power, low-voltage, high bandwidth dc-dc converter. Chapter 6 summarizes the design considerations for VHF resonant power conversion and suggests direction for continued work in this area.
Chapter 2

Magnetics Scaling

As introduced in Chapter 1, power electronics operating at very high switching frequency (e.g., 10-100 MHz) are important in many applications including resonant inverters for heating, plasma generation, imaging and communications [6,10,27-31] and resonant dc-dc converters [7,17,28,32-35]. Magnetic components play an important role in these applications for intermediate energy storage, impedance transformation, and filtering. These magnetic components should have a high quality factor and low loss in order to achieve highly efficient power conversion.

In this chapter, we explore frequency scaling of power converters, and examines how the physical sizes of magnetic components change with increasing frequency for different design options. We provide quantitative examples of magnetics scaling, and also point to opportunities in VHF magnetics design. Based on several key assumptions in Section 2.2, different magnetic design tradeoffs (cored vs. air-core; conventional magnetic material vs. RF low-permeability materials) are studied and compared. The results from this chapter can help to give a quantitative sense of the scaling of magnetic component size with frequency.

2.1 Background

Consider how a power converter could be redesigned to preserve the voltage and current waveform shapes, but with the waveforms scaled in time and amplitude to yield a new frequency and power level. Treating the system as a switched linear network, and defining scaling factors $k_v$, $k_i$, and $k_f$ for circuit voltages ($v$), currents ($i$), and frequency ($f$):
Magnetics Scaling

\[
\begin{align*}
    v_{new} &= k_v \cdot v_{old} \\
    i_{new} &= k_i \cdot i_{old} \\
    f_{new} &= k_f \cdot f_{old}
\end{align*}
\] 

then it is straightforward to show that the circuit powers and component values scale as:

\[
\begin{align*}
    p_{new} &= k_v k_i \cdot p_{old} \\
    C_{new} &= \frac{k_i}{k_v k_f} \cdot C_{old} \\
    L_{new} &= \frac{k_v}{k_i k_f} \cdot L_{old} \\
    R_{new} &= \frac{k_v}{k_i} \cdot R_{old}
\end{align*}
\] 

Following this scaling for all circuit elements, the waveform shapes scale as desired in amplitude and time, and circuit efficiency remains unchanged. For operation at the same voltage and current levels but at a factor \( k_f \) higher in switching frequency, circuit resistances remain unchanged, while capacitor and inductance values scale inversely with frequency (by a factor \( 1/k_f \)). This inverse scaling of passive component values and energy storage with switching frequency, along with the proportionate increase in achievable control bandwidth, clearly motivate use of higher switching frequencies. What is less clear and what we examine as part of this work, is how the achievable sizes of the passive components change with frequency when practical constraints are taken into account. We focus on magnetic components, as they are the most challenging to scale to high frequencies and small sizes, and because they typically dominate the size of power electronic systems. Moreover, we restrict our discussion to scaling of ac inductors (e.g., for resonant operation), both because this is representative of scaling in many magnetic components, and because resonant circuit designs using such magnetics are often suited for operating at extreme high frequency and for achieving superior transient performance, which are the key applications addressed by the scope of this thesis work.
2.2 Magnetics Scaling Design Considerations

When inductance values are scaled inversely with switching frequency, the effective impedance levels provided remain unchanged as a design is scaled. How the size of an appropriate magnetic component scales, however, is a much more complex question, encompassing the dependence of winding loss [36–40], core loss and permeability [28, 39–45], and heat transfer [34, 44, 46] on size and frequency. Size and frequency scaling of magnetic components has been considered in a variety of works: [39] considers how the quality factor of an inductor at a given frequency scales with linear dimension for various loss cases. Reference [40] examines scaling of transformer parameters and performance with size and frequency under heat transfer limits, while [46] shows how achievable transformer size varies with frequency under efficiency and heat transfer limits. Reference [47] provides a transformer design algorithm including core loss and simplified winding loss, and explores via a design example how transformer size scales with frequency. Reference [44] explores power density limits of inductors vs. frequency, considering core loss and heat transfer limitations. These references reveal that there are often limitations in scaling down the size of magnetic components, even if frequency is increased arbitrarily. Nevertheless, as illustrated below, considerable reduction in the size of magnetic components is possible through frequency scaling if appropriate materials and designs are employed.

We examine how the size of ac (e.g., resonant) inductors scale with operating frequency considering both efficiency (e.g., quality factor) and temperature constraints. We focus on single-layer-winding designs, and consider use of high-permeability ferrite materials, low-permeability rf materials, and coreless designs. In addition, in order to make the problem tractable, we only consider inductor design under a limited set of conditions. Nevertheless, these conditions are both very reasonable and practical for inductor scaling analysis at very high frequency. The key assumptions we are making here are:

1. Switching devices are not the limiting factor in operating frequency. As will be described in Chapter 3, semiconductor characteristics and packaging inductance can be one of the key limiting factors in moving up converter switching frequency while maintaining acceptable efficiency. However, for the simplicity of this analysis, we will explore the operating frequency limit due to the magnetic component itself only.
2. As the operating frequency scales up, the converter time-domain waveforms are merely compressed. Often times, as we move up in switching frequency, the packaging parasitics have a larger effect on the overall performance of the system, changing the overall system impedance, and distorting waveshapes of the original system. For the purpose of analysis, we assume all waveforms preserve their original waveshapes and they are merely compressed in the time-domain, as per the scaling analysis described above.

3. The optimal geometry and structure of an inductor does not change with frequency. In other words, we will scale an inductor geometry by changing all dimensions by linear dimensional factor $\varepsilon$. This has been found to be the case in single-layer-wound toroidal RF inductors, for example [48,49].

2.3 Magnetics Scaling Method and Procedure

Given a constant magnetic component impedance and a set of operating conditions, the key question to be addressed under the aforementioned assumptions is how magnetics volume scales with frequency.

2.3.1 Numerical Analysis Procedure

Figure 2.1 illustrates the proposed scaling analysis procedure for a magnetic-core inductor design. Firstly, we decide some basic parameters from power electronics design requirements including the inductance ($L$), the AC current amplitude ($I_{AC}$), a loss budget ($Q$), and a maximum temperature rise limitation. Secondly, we create a frequency scaling matrix (inductances vs. frequency while maintaining constant impedance) with corresponding set of new inductance at each frequency to keep the $\omega L$ product. Then, we start with a given core design, and create a set of core sizes with each dimension scaled according to the assumptions stated in Section 2.2. Then, for each given frequency and each possible core size, we design a new scaled inductor and calculate its scaled core loss $P_{core}$, winding loss $P_{winding}$ and temperature rise. Finally, for each frequency, we search the entire design space (the scaled core dimension matrix) for the smallest inductor that meets with both the loss
budget (Q) requirement and the temperature rise requirement. Numerical simulation script is included in Appendix A.

2.4 Magnetics Scaling Analysis

2.4.1 Cored Inductor Scaling

There are two major loss mechanisms associated with a cored resonant inductor, core loss and winding loss. We model core loss \( P_{\text{core}} \) using the classical power law or Steinmetz model:

\[
P_{\text{core}} = V_{\text{core}} C_M f^\alpha B_{ac}^\beta
\]

(2.3)

where \( V_{\text{core}} \) is the core volume, \( f \) is the operating frequency, \( B_{ac} \) is the sinusoidal ac flux density in the core and \( C_M, \alpha \) and \( \beta \) are parameters chosen to fit the model to measured loss data. For typical ferrite materials, \( \alpha \) is in the range of 1.4-2.0 and \( \beta \) is in the range of 2.4 - 3.0 where specific parameters may need to be selected for a particular frequency range [50]. For a single-layer winding in the skin-depth limit we use a simple model for winding loss \( P_w \):

\[
P_w = \frac{1}{2} I_{ac}^2 R_{ac} = \frac{1}{2} I_{ac}^2 \frac{\rho l_w}{w_w \delta} = \frac{1}{2} I_{ac}^2 \frac{l_w}{w_w} \sqrt{\pi \rho w_w f}
\]

(2.4)

where \( I_{ac} \) is the sinusoidal ac current amplitude, \( \rho \) is conductor resistivity, \( l_w \) is the length of the winding, \( w_w \) is the effective width of the conductor, and \( \delta \) is the skin depth, which is inversely proportional to frequency. In this model, we neglect gap fringing effects [21, 51]. Consider how the achievable size of a resonant inductor scales with frequency when the inductive impedance is held constant and equivalent ac series resistance is held constant. This results in a required inductor quality factor Q (and loss) that is independent of frequency. In carrying out our scaling experiment, we start with an inductor having an optimized design for a given frequency (winding, core geometry and gap). To scale the design in size, we
Figure 2.1: Cored inductor scaling analysis procedure. Matlab script implementing this procedure is provided in Appendix A.
allow the core geometry to change proportionally in all linear dimensions (keeping the core geometry constant), including the gap, but allow the number of turns to vary (distributed in a single layer in the scaled winding window, thus changing $w_w$). In scaling to a new frequency we seek the smallest design that meets both the impedance and quality factor requirements. If the size is held constant while frequency is increased by a factor $k_f$, the winding loss could be held constant by decreasing the number of turns by a factor $k_f^{-0.25}$, based on (2.4). If we adjust the gap to keep the inductive impedance constant, flux density scales down by $k_f^{-0.75}$. Core loss then scales as $k_f^{-0.75 \beta}$. If $\alpha < 0.75 \beta$, core loss, and thus total loss, decrease. We can see that it is then possible to reduce the size, which will incur a loss penalty, and return to the original total loss. Ideally the gap length and number of turns would be re-optimized at the same time to maximize the size reduction.

However, if $\alpha > 0.75 \beta$, core loss increases if frequency is scaled up and impedance and winding loss are held constant. In this case, size needs to be increased in order to maintain the original total loss. In principle, the size can either scale up or down with frequency, depending on the material parameters. In practice, the values of $\alpha$ and $\beta$ that provide a good fit to core-loss data vary as a function of frequency: $\alpha$ becomes larger at high frequency and $\beta$ stays approximately constant or decreases [50]. Thus, at sufficiently high frequency, the improvements from scaling frequency cease and then reverse, so there is a limit to the amount that frequency scaling can be used to reduce inductor size.

### 2.4.1.1 Cored Inductor Design Examples

To demonstrate this effect, we carry out a numerical design experiment. The resonant inductor design to be scaled realizes an impedance of 62.8 $\Omega$ (i.e. 100 $\mu$H at 100 kHz) at $Q = 100$ for 1A peak ac current. We use a numerical search to optimize designs based on 3F3 core material starting with scaling RM7 core with 800$\mu$m air gap. The optimization is based on the assumptions introduced above, but additionally limits core flux density to below 0.3 T and considers only integer numbers of turns. The $Q$ limited curve of Figure 2.2 shows the numerical optimization results and inductor box volume vs. design frequency. Note that box volume, as illustrated in [42], is the volume of the smallest box that the inductor could fit inside. The scaled inductor design achieves its minimum size at around 300 kHz, and beyond which the inductor volume increases drastically, with its minimum volume being
Magnetics Scaling

Figure 2.2: Numerical Optimization results of inductor "box" volume vs. design frequency for an example resonant inductor approximately 0.2 cm$^3$. Figure 2.3 illustrates the two loss mechanisms of cored-inductors, and their behaviors across the scaled frequency range. At low frequencies, winding loss contributes to a large portion of total loss, with flux density constrained primarily by saturation limits. However, at high frequencies, core loss increases significantly and the inductor core area must be increased to reduce flux density in order to maintain constant total loss and $Q$ (loss budget). At frequencies where core loss is a factor limiting flux density (as opposed to flux density determined only by saturation limits), one ends up with flux density derated from the saturation limits by an amount that yields approximately equal core and winding loss.

Also shown for comparison (Figure 2.4 are results for a separate CAD optimization which uses discrete, standard RM cores, wire sizes and gaps (with 3F3 material), incorporates multi-layer windings, and accounts for skin and proximity effect and core thermal limits, the inductor implemented here realizes an impedance of 157 $\Omega$ (i.e. 250 $\mu$H at 100 kHz) at $Q = 100$ for 1 A peak ac current. We use a numerical search to optimize designs based on 3F3 core material. Results from this alternative optimization match well given differences in the design limits, and yield identical conclusions. We note that these results are qualitatively similar to those found for transformers in [46,47], underscoring the limitations of frequency scaling in cored designs.
2.4 Magnetics Scaling Analysis

Figure 2.3: Core loss and winding loss of an optimized resonant inductor vs. design frequency for a set of inductors realizing a constant impedance of 62.8 Ω (i.e. 100 µH at 100 kHz) at \( Q = 100 \) for 1 A ac current. Numerical simulation files are included in Appendix A.

Figure 2.4: Numerical optimization results of inductor "box" volume (including discrete designs) vs. design frequency for a set of inductors realizing a constant impedance of 157 Ω (i.e. 250 µH at 100 kHz) at \( Q = 100 \) for 1 A peak ac current. Numerical simulation files are included in Appendix A.
2.4.1.2 Temperature Constraint

It should be noted that there are also other constraints in miniaturization under frequency scaling. In the previous discussion, it is assumed that the inductor loss budget is the limiting factor for achieving a minimum volume. In addition to meeting a quality factor requirement, imposing a temperature rise limit on a given inductor may further increase its minimum achievable volume. In order to study how the volume of an inductor scales with a temperature rise constraint, a thermal model is first developed. Among the three heat transfer mechanisms (convection, conduction and radiation), the heat flow is proportional to surface area (of which the units are linear dimension squared) for convective and radiative heat transfer, whereas the heat flow through conduction is proportional to linear dimension if the dimensions of all structures are scaled together, (2.5). To form a conservative estimate at small scales, it is safe to assume that heat flow is at least proportional to the surface area and temperature rise, which corresponds to a constant heat flux limit for a given temperature rise, (2.6).

\[ q_{\text{convection}} = hA\Delta T \propto \varepsilon^2 \]
\[ q_{\text{conduction}} = \frac{A\Delta T}{l_{\text{PTH}}} \propto \varepsilon \]
\[ q_{\text{total}} = (k_1\varepsilon^2 + k_2\varepsilon)\Delta T \]

By matching the thermal resistance vs. surface area for this constant heat flux model with discrete data points for RM type ferrite cores and an empirically-fitted curve for toroidal Micrometals cores [52], as shown in Figure 2.5, we arrive at a heat flux limit of 6.7mW/(°C·mm²). This thus represents a thermal model which is quite conservative at small scales.
With this thermal model, a temperature limit of $40^\circ C$ is imposed on both previous inductor designs (i.e. $157\Omega$ and $62.8\Omega$ at 1 A ac current on a scaled RM core using 3F3 material). This $\Delta T$ limited curve of Figure 2.4 and Figure 2.6 plot the minimum size of an inductor that meets this temperature requirement without consideration of $Q$. As shown in Figure 2.4 and Figure 2.6, both loss and temperature constraints are important, with an allowed design being on the maximum of the two curves.

### 2.4.1.3 RF Low-Permeability Materials

As shown in Figure 2.6, resonant inductors constructed with conventional high permeability MnZn and NiZn ferrite materials, such as 3F3 and 3F4, are typically effective only up to a few megahertz, beyond which the volume must increase drastically to meet a given quality factor requirement. Introduction of low permeability rf materials (with several examples explored in [48,49,53]) extends the frequency range for which cored inductors are useful up to many tens of megahertz. However, core loss still imposes a fundamental frequency limit in minimizing size in resonant cored inductors built with rf materials, and there still exists an optimal frequency beyond which the inductor size increases in order to stay within a loss constraint. To demonstrate the efficacy of low-permeability RF materials, we simulate and optimize inductor designs for the same requirements ($62.8\Omega$ inductive impedance, 1 A ac current, a minimum $Q$ of 100 and a maximum temperature rise of $40^\circ C$), using toroids.
Magnetics Scaling

Figure 2.6: Numerical Optimization results of inductor “box” volume vs. design frequency for an example resonant inductor with temperature limitations for a set of inductors realizing a constant impedance of 62.8 Ω (i.e. 100 μH at 100 kHz) at $Q = 100$ for 1 A ac current. Numerical simulation files are included in Appendix A.

of P-type material ($\mu = 40$) from Ferronics. The inductors designs are optimized based on a polynomial fit to the available core loss data [53] for P material and various toroidal core sizes [50]. Figure 2.7 illustrates that the box volume for inductors designed with P material is minimized near 30 MHz, with an achievable minimum size of ~1.5 cm$^3$. Unlike the previous case, the minimum size in this example is limited by temperature rise. Figure 3 shows that, compared to designs with a conventional high-permeability material (i.e., 3F3), designs using an RF material (P) enables an approximate 40% reduction in volume to be achieved, along with a reduction of energy storage and increase in frequency by a factor of ~100. In other cases (e.g., higher temperature rise designs) the relative advantage of the rf material would be even much larger.

2.4.2 Coreless Inductor Scaling

Core loss imposes fundamental frequency limits associated with minimizing size in cored resonant inductors. Since winding loss is the only major loss mechanism for a coreless design, coreless designs may offer a much better tradeoff between a given loss budget and volume at higher frequencies. In general, the inductance of a tightly-coupled magnetic structure can be expressed as being proportional to a linear dimensional scaling factor $c$
2.4 Magnetics Scaling Analysis

Figure 2.7: Resonant inductor volume comparison. The use of the rf material enables a ~40% reduction in volume as compared to using 3F3 material for this scaling example.

\[ L = \frac{N^2 \mu A_l}{l} \propto N^2 K \epsilon \]  \hspace{1cm} (2.7)

Consider a single-turn inductor: its inductance is directly proportional to the linear dimension factor \( \epsilon \) (6), and its dc resistance is inversely proportional to \( \epsilon \) (7):

\[ L = K_1 \epsilon \]  \hspace{1cm} (2.8)

Figure 2.8: Magnetic Dimension Scaling
Magnetics Scaling

\[ R_{DC} = \frac{\rho l}{A_w} = \frac{K_2}{\varepsilon} \]  \hspace{1cm} (2.9)

For ac resistance in the skin depth limit, the dependency on linear dimension is exchanged for a dependence on the square root of frequency:

\[ R_{AC} = d_{\delta} R_{DC} = K_3 \sqrt{f} \]  \hspace{1cm} (2.10)

For a closely-linked N-turn inductor, inductance, dc resistance and ac resistance are all merely scaled by number of turns squared.

\[ L = N^2 K_1 \varepsilon R_{DC} = \frac{N^2 K_2}{\varepsilon} R_{AC} = N^2 K_3 \sqrt{f} \]  \hspace{1cm} (2.11)

In order to scale an inductor design across frequency maintaining constant impedance and constant loss, we can first find the dependence of the quality factor on the linear scaling factor \( \varepsilon \) and on frequency

\[ Q = \frac{2\pi f L}{R_{AC}} = \frac{2\pi f N^2 K_1 \varepsilon}{N^2 K_3 \sqrt{f}} = K_4 \varepsilon \sqrt{f} \]  \hspace{1cm} (2.12)

The quality factor is directly proportional to \( \varepsilon \) and to the square root of frequency. Thus, to achieve a given impedance and quality factor as frequency is varied, an inductor’s linear dimension can be scaled as \( f^{-1/2} \), which in turns means that the volume of the inductor scales as \( f^{-3/2} \). If quality factor were the only limiting factor, the required volume of a coreless inductor could be continuously reduced as \( f^{-3/2} \) as frequency increases. However, as the inductor volume (and surface area) gets smaller and smaller for a given loss, the inductor will eventually encounter its thermal (temperature rise) limit. From the thermal model developed in the previous section, imposing a temperature limit is equivalent to limiting heat flux through the inductor surface. Under this model, there are two ways through which the temperature rise can be decreased: reducing the loss and/or increasing the surface area. From (2.12), the quality factor is shown to be proportional to the linear
2.4 Magnetics Scaling Analysis

![Diagram of a single layer coreless solenoid inductor]

Figure 2.9: Single layer coreless solenoid inductor

scaling factor. If the thermal model is combined with (2.12), the volume of a coreless inductor under a heat flux limit scales with \( f^{-1/2} \):

\[
\Delta T = k \cdot \frac{P_{\text{diss}}}{\text{Area}_{\text{Surface}}} = k \cdot \frac{I_{\text{RMS}}^2 Z}{\text{Area}_{\text{Surface}}} = k_2 \frac{I_{\text{RMS}}^2 Z}{\epsilon^2 \sqrt{f}}
\]  

(2.13)

Therefore, even in the heat flux (thermally) limited case, the volume of an air-core inductor can still be made smaller with increasing frequency. Furthermore, the quality factor of the inductor in the heat-flux-limited scaling actually improves as \( f^{1/3} \). This scaling can be maintained so long as at least one turn or more is required for the desired impedance at the specified scale. (Scaling can still be achieved beyond this point in some cases, but necessitates changes in geometry.)

2.4.2.1 Coreless Inductor Design Example

For a single layer coreless solenoid inductor, a good empirical model is available based on Medhurst’s work [54-57]. In Medhurst’s model, quality factor \( Q \) is directly proportional to the diameter of a solenoid, square root of frequency and another factor \( \Psi \), where \( \Psi \) is a function of length \( l \) to diameter \( D \) of the solenoid and wire diameter to wire spacing:

\[
Q \approx 7.5 D \Psi \sqrt{f}
\]

\[
\Psi_{\text{optimum}} \approx 0.96 \tanh(0.86 \cdot \sqrt{\frac{l}{D}})
\]

(2.14)

\[
\frac{l}{D} = 5, \Psi_{\text{optimum}} \approx 0.88
\]
Figure 2.10: Numerical Optimization results of inductor "box" volume vs. design frequency for an air-core resonant inductor with temperature limitations (40°C) for a set of inductors realizing a constant impedance of 62.8 Ω (i.e. 100 μH at 100 kHz) at Q = 100 for 1 A ac current. Numerical simulation files are included in Appendix A.

To achieve maximum Q for a solenoid inductor, this model maintains the aspect ratio of the length to diameter of the inductor to be at least 5, which is consistent with our assumption of maintaining an optimal design by holding the relative geometry constant as we scale designs. A CAD optimization of solenoid inductors based on Medhurst's formulation is shown in Figure 2.11 compare to illustrate how the coreless resonant inductors scale with frequency, with the associated MATLAB script in Appendix A. The same operating conditions (an impedance of 62.8 Ω (i.e. 100 μH at 100 kHz) at Q = 100 for 1 A ac current) are applied as were used for the cored resonant inductors. Initially, when temperature rise is not a limiting factor, we see that the inductor box volume scales as $f^{-3/2}$, and once the temperature rise becomes the major constraint, the inductor volume falls off at a slower rate, with $f^{-1/2}$, which is precisely what the previous analysis predicts, figure 2.10.

Figure 2.11 also shows the previous simulation predictions for inductor box volumes with the conventional high permeability magnetic material (Ferroxcube 3F3), and the low permeability RF material (Ferronics P) and a coreless structure under the same operating conditions and constraints. This comparison is somewhat limited by the fact that the solenoid design is magnetically unshielded, while the other two designs are largely shielded. Nevertheless for a given maximum loss budget and temperature rise limit, there is always a frequency beyond which a coreless inductor will outperform any cored inductor. What design strategy
2.4 Magnetics Scaling Analysis

Figure 2.11: Comparison between conventional magnetic material (3F3), RF material (P) and coreless inductor volume for a set of inductors realizing a constant impedance of 62.8 \( \Omega \) (i.e. 100 \( \mu \)H at 100 kHz) at \( Q = 100 \) for 1 A ac current. Numerical simulation files are included in Appendix A.

is best depends on the design specifics, but it is clear that both low-permeability designs and coreless designs can be advantageous, and that at sufficiently high frequencies, a coreless design will provide the lowest loss.

2.4.3 Magnetics Scaling Summary

From the above analysis, we can see that cored ac inductors always have a frequency limit in terms of achieving miniaturization with increased operating frequency. Nevertheless, it is shown that significant improvements in size can be achieved by moving to VHF frequencies if low-permeability RF magnetic materials are employed. It should be noted that the design of magnetic components with low-permeability RF magnetic materials is relatively poorly understood as compared to design with conventional materials. This represents a significant opportunity for improved designs at VHF frequencies. Moreover, the above analysis indicates that with coreless designs we can always achieve significant benefits in size, required energy storage, and magnetics loss by scaling up in frequency, provided sufficiently high frequencies can be obtained within other constraints. Likewise, there is opportunity to gain still greater benefits through improved design and fabrication of coreless magnetic
structures and with magnetic structures better suited to extreme high frequencies (e.g. [29,58]).
Chapter 3

Integrated Device and Gate Drive Design

Achieving a high-bandwidth, low-voltage VHF power converter across a wide operating range requires addressing a number of obstacles. One of the major building blocks for implementing such a converter is the semiconductor switches themselves. As compared to using discrete devices, designing devices on a low-voltage process provides the flexibility and freedom to customize the size of the device and optimize its layout, in addition to integrating its driver on the same die to avoid additional losses associated with packaging parasitics.

In this chapter, we examine methods to improve upon performance achievable via commercial off-the-shelf semiconductors for use in VHF applications. As was found in the previous chapter, air-core magnetics provide a much better tradeoff in terms of size and loss compared to its cored counterparts (for the application range under consideration), provided that other limitations such as semiconductor losses are dealt with. To address these device limitations, this chapter explores opportunities in integrated device and gate driver designs. Device geometry optimization on a CMOS low-voltage process is discussed, and opportunities in extending voltage range via a cascode device structure are explored. Furthermore, an integrated gate drive design is also studied, which can sidestep challenges (especially at hundreds of MHz operating frequency) associated with utilizing their discrete counterparts. These design approaches together with careful considerations given to device packaging issues lead to a integrated design much suited for resonant VHF power conversion at low voltages.
3.1 Background

Generally, the achievable transistor characteristics, including lower parasitic capacitance and on-state resistance, get better with lower breakdown voltage. Unfortunately, choices are very limited when it comes to commercial off-the-shelf devices with 20V or lower breakdown voltage. Furthermore, the relative magnitudes of various device losses associated with VHF resonant power conversion are significantly different from that of hard-switched operation. Available (discrete, vertical) devices do not get much better once the breakdown voltage gets below 30V. In part this is because of the nature of vertical power MOSFET designs, and in part because most commercial switches are designed with conventional power converters in mind and, therefore, are not intended to be used in VHF resonant applications [59]. For example, RF power MOSFETs intended for use in linear power amplifier are optimized for their use in linear operation, which doesn't correlate to best performance in power conversion; devices designed for hard-switched converters are optimized for extremely low on-state resistance and capacitance levels suitable for low frequencies, which is not compatible with VHF operation. This has led to devices that are very good for these applications, but not to providing the full potential of achievable performance that a particular IC process may realize in the VHF regime. In this work, optimization is accomplished for the set of device losses that result when soft switching is employed to attain very high switching frequencies.

At low voltages, CMOS processes offers tremendous opportunities in terms of achievable device switching speed, which makes them an attractive alternative for semiconductor device design in the VHF range. However, one major challenge associated with doing resonant power conversion on a low-voltage CMOS process is its very limited voltage range. Resonant power conversion utilizes resonant networks to ring the drain-to-source voltage across its switching device up and down to achieve characteristics such as ZVS to reduce switching losses at high frequencies. For instance, if we consider a class-E inverter design, where the peak device voltage stress on a given device is over 3.5× its input voltage, employing a 3.3V CMOS device which then sets the theoretical maximum dc input voltage to sub-1V. If the additional ringing caused by lossy packaging and layout parasitic inductances are considered, the operating input voltage range is further reduced, substantially limiting the application space where these CMOS devices may be utilized.
3.2 Device Design

In addition, designing a low-loss gate drive is not a trivial issue at VHF, especially for low-power applications and low-voltage CMOS devices. In CMOS devices, gate drive losses can often exceed switching loss due to output capacitance discharge, because the gate voltage swing is on the same order as the output voltage swing (unlike at higher voltages). Gate driver loss can easily become a significant portion of total loss, and deteriorate the overall converter efficiency tremendously. Furthermore, in the VHF operating regime, parasitic inductance associated with off-the-chip driver designs can tremendously impact the timing of the gate drive signal, which has prevented synchronous rectifiers (especially suitable for low output voltage operations) from being implemented in the hundreds of megahertz. Merits of resonant gating techniques at VHF have been demonstrated in [3,4,6,10,16–18,60–65]. The complexity of tuning a resonant drive can be high and the number and the size of components required can be large (especially in the CMOS case, where the driver components may be on the same order size as the power stage components). This suggests that an integrated driver may offer a much more attractive alternative at low voltages, considering its size, simplicity, loss and accurate timing control.

3.2 Device Design

Optimizing a device for efficient operation at VHF requires an understanding of the three major loss mechanisms (conduction loss, switching loss and gating loss) which are directly related to characteristics of a switching device. Achieving a balance between these loss mechanisms is necessary to attain optimum performance. A simple device model, figure 3.1 is used when determining the optimum device parameters that need to be considered in a VHF converter [59,66].

The device models shown in the figure above are selected because they are the most relevant parameters in determining the semiconductor loss in a converter design [59,66]. In this simplified model $C_{GD}$ and $C_{GS}$ lumped together to form an equivalent capacitor $C_{ISS}$, which is a reasonable assumption since in a soft-switched converter, the drain voltage is ideally at zero when the gate voltage rises (provided that $C_{GD}$ is small enough that it does not introduce significant overlap loss). Similarly, $C_{DS}$ and $C_{GD}$ together form a single capacitor $C_{OSS}$. In addition, for soft-switched resonant applications, the transistor is not
operated outside the triode region, which leads to the on-state behavior of the transistor modeled merely as a variable resistor.

For a CMOS soft-switched converter in the VHF regime, conduction loss behavior is similar to that of hard-switched converters, \( P_{\text{COND}} = R_{\text{DS,ON}} l_{\text{cond,RMS}}^2 \), which is not dependent on the switching speed of a converter. By contrast, while the off-state conduction loss is negligible for hard-switched converters, it can be significant for soft-switched designs due to the large circulating current loss through the device output capacitance and output resistance. As frequency increase, the branch current through the \( R_{\text{OSS}} \) and \( C_{\text{OSS}} \) leg rises linearly as the capacitor impedance falls, leading to a square-law dependency on frequency terms in the corresponding loss mechanism: \( P_{\text{DISP}} \propto C_{\text{OSS}}^2 R_{\text{OSS}} f_{\text{SW}}^2 \). Furthermore, as seen in converter designs in [4,16–18,60,65], additional external capacitors \( C_{\text{EX}} \) are usually added in parallel to \( C_{\text{OSS}} \) to achieve desired ZVS switching waveforms, in which case, \( I_{\text{DISP}} \) is shared between the parasitic device capacitance \( C_{\text{OSS}} \) and \( C_{\text{EX}} \), resulting in \( P_{\text{DISP}} = \left( \frac{C_{\text{OSS}}}{C_{\text{OSS}} + C_{\text{EX}}} \right)^2 R_{\text{OSS}} I_{\text{DISP,RMS}}^2 \).

There are two different gating options at VHF operations, hard gating and resonant gating. For a hard-gated converter, its gating loss is proportional to frequency, \( V_{\text{GATE}} = V_C^2 f_{\text{SW}} C_{\text{ISS}} \); whereas for a converter with resonant gating, its gating loss is given by
3.2 Device Design

\( V_{GATE} = 2(\pi V_{G,AC} f_{SW})^2 C_{ISS}^2 R_{GATE} \). Different device parameters should be optimized depending on the desired gate-driver design. For a hard-gated converter, its \( C_{ISS} \) should be minimized; and the critical device parameters for minimizing gating loss in a resonant gate drive design depends on the product of \( C_{ISS} R_{GATE} \).

Due to the complexity of tuning a resonant drive and the number and the size of components required (especially in the CMOS case, where the driver components may be on the same order size as the power stage components), an integrated driver is more desirable at low voltages, considering its size, simplicity, loss and accurate timing control. The total semiconductor loss in a soft-switched converter with hard gating is given by

\[
P_{TOT} = P_{COND} + P_{DISP} + P_{GATE, HARD} = R_{DS,ON} I_{cond, RMS}^2 + \left( \frac{Coss}{Coss + Cex} \right)^2 R_{oss} I_{DISP, RMS}^2 + V_{G}^2 f_{SW} C_{ISS}.
\]

With these loss mechanisms in mind, we now can understand how the losses in a soft-switched, resonant gated converter may scale as we vary the size of a device on a given IC process. As the total device width \( W \) increases, \( R_{DS,ON} \) and \( P_{COND} \) decreases (ideally proportionally to \( 1/W \)). \( C_{ISS} \) ideally increases proportionally to \( W \) which causes \( P_{GATE, SOFT} \) increase proportionally to \( W^2 \) (whereas \( P_{GATE, HARD} \) in the hard-switched case increases linearly with \( W \)). \( P_{DISP} \) also grows proportional to \( W^2 \) as \( C_{oss} \) grows proportionally to \( W \). Therefore, the tradeoffs between device loss mechanisms with relation to the total device width can then be summarized as \( P_{TOT} = a_1 \frac{1}{W} + a_2 W + k_3 W^2 \), where \( a_1, a_2 \) and \( a_3 \) are process-dependent constants [66], which suggests that there is an optimal device size for a given converter design and a given IC process.

3.2.1 Device Layout Optimization

CMOS which has traditionally been confined to the digital and analog designs has proven its merits as a competitive technology in the RF power space. Its switching speed and relative low-cost has deemed itself as an attractive alternative to the state-of-the-art RF processes in certain applications. Likewise, it is being widely applied in low-voltage hard-switched converters, especially buck converters [Add refs.]

This work follows the general device optimization approach described in [59], but is focused on optimization of low-voltage CMOS. In particular, device design is optimized for a TSMC 0.35um CMOS mixed signal process. A set of easily-measured device parasitics is chosen.
and used to parametrize a model that predicts device loss for a given particular resonant converter design. These parameters are then associated with layout geometries which permit a layout optimization. For a given set of circuit dependent constants, by assuming the shapes of the drain and gate waveforms are maintained as frequency is scaled, we calculate how these three loss mechanisms are related to five key device parameters ($R_{DS-on}$, $ROSS$, $RG$, $Coss$ and $C_{ISS}$), based on the results from the previous section. As frequency is scaled, conduction loss will remain constant because $R_{DS-on}$ is not a function of frequency and the RMS of the conduction current does not vary. However, displacement current (current associated with off-state conduction) and gate current rises linearly as the capacitances increases, which leads to a square-law rise in displacement and gating loss with capacitance for a given frequency.

We take as an input the TSMC35HV design rules. By relating the device geometry to the device parasitic parameters for particular values of the design parameters, such as aspect ratio, gate finger length, total device area and other configuration variables, the five key device parameters, $R_{DS-on}$, $ROSS$, $RG$, $Coss$ and $C_{ISS}$ and their associated loss can be calculated. We can then search across the design space (the space of our design variables), we can identify the design with lowest loss.

Figure 3.2a shows the basic cell structure that makes up a single transistor in the TSMC035HV process. Large transistors are formed by scaling the width of the basic single cell's finger via connecting multiple instances of the cells in parallel. While many parameters of a particular cell (such as the length of the drain, source and bulk diffusions and the number of contacts) are fixed by the design rules for a given process, the two scalable dimensions are the width of the cell and the width of the field termination for a single cell, which are two variables to be used in the optimization.

The individual cells are then connected both vertically and horizontally in an array (with their drain, gate, source/bulk terminals in parallel). In this particular process, the 0.35μm TSMC process TSMC035HV, there are four metal layers that can be used. The drain and source/bulk contacts of each cell are adjoined to each other via vertical segment of the metal-1 layer, whereas, the gate contacts of each row of cells are connected by horizontal metal-1 strips, Figure 3.2b. These horizontal metal-strips are then connected to an array of gate pads to be attached to bondwires. The vertical metal-1 strips are then connected in parallel through via to horizontal metal-2 strips alternately forming drain and source
3.2 Device Design

buses, Figure 3.2c. Finally, metal-3 and metal-4 straps are running vertically to connect the metal-2 drain/source buses in parallel and out to their respective bondpads, Figure 3.2d.

With the layout picture discussed above, there are eight major layout parameters that directly affect the characteristics of a device. These are:

1. the total effective device width
2. the cell width
3. the width of metal-1 gate fingers
4. the overall device aspect ratio
5. the width of metal-2 drain/source stringers
6. the number of metal-3/metal-4 strips
7. the tapering-angle of the metal-3 strips
8. the number of gate bondpad arrays

The effects of each layout parameter on the device characteristics is explained as follows: The total effective device width sets the intrinsic $R_{DS-on}$, and the minimum terminal capacitances. The conduction loss decreases as the total device effective width increases. On the other hand, the frequency dependent off-state conduction and gating losses exhibit the opposite behaviors due to the effects of parasitic capacitance; effective device width is thus critical to device optimization. The individual cell width plays an equally important role. For a given intrinsic $R_{DS-on}$, the device can be designed either via a single cell or multiple cells with the same total cell width. While $C_{iss}$ and $C_{oss}$ grows as the number of cells increases as a larger termination regions are needed, and $R_{DS-on}$ also rises due to the extra metallization needed to connect multiple cells. Conversely, more cells allows for a larger number of gate fingers, which in turn lowers the metal-1 contribution to the gate resistance. Therefore, there exists an optimum individual cell width by trading off rising gate resistance with lower capacitance and lower extrinsic $R_{DS-on}$ per intrinsic $R_{DS-on}$.

The number of metal-3/metal-4 strips and the tapering angle of the metal-3/metal-4 strips affects the total $R_{DS-on}$. The tapering design of metal-3/metal-4 buses are utilized to
Figure 3.2: Single transistor cell and inter-metal layout connections that affect the device parasitics
counteract the fact that the current density grows from the end of a metal strip towards the bondpad bus, and thus lowers the loss. However, as the tapering angle increases, the resistance due to metal-2 also rises since the number of vias connecting metal-2 to metal-3 layers is also changed, and the longer sections of metal-2 strips are now needed to carry current back to metal-3 strips. There is a similar tradeoff between the number of metal-3/metal-4 strips used. A higher number of metal strips keeps the metal-2 current density small, however, it limits the total amount of metal-3 available due to the metal-3 layer spacing rules. These observations suggest that an optimal design exists via simultaneously scaling the tapering angle and varying the number of metal-3/metal-4 strips.

The overall device aspect ratio has significant impact on the metallization resistance between the drain and the source nodes. Stacking cells in a few rows with many columns results in long and few gate fingers (higher gate resistance), but short and numerous drain and source strips (lower drain-to-source resistance). Stacking cells in the opposite manners (many rows with few columns) will result in a device with relative low gate resistance, but higher drain-to-source metal resistance.

For a given individual cell width and width of metal-1 gate fingers, the total available metallization area for metal-2 drain and source buses is fixed. However, by varying the distribution of metal-2 to each, the total number of drain and source vias can be changed and can help to minimize the overall loss in the metal.

The number of gate bondpad arrays has a significant impact on the overall structure of the device layout. A larger number of gate bondpad arrays requires more die area, however, it can significantly lowers the gate resistance (without affecting the resistance associated with the drain-to-source network). However, this observation doesn’t suggest that we will be able to continuously reduce the gate resistance by arbitrarily increasing the number of gate bondpad arrays. Beyond a certain point, there is a diminishing return by adding additional arrays of gate bondpads (at the cost of wasting a large area of die area).

By considering the tradeoffs between these design parameters outlined in the previous section, an optimum device can be found using a search algorithm coded in MATLAB (scripts are available in Appendix D). The search algorithm looks at the many possible combinations in the eight major layout handles within the process rules and calculates the device parameters $R_{DS, on}$, $R_G$, $C_{ISS}$, $C_{OSS}$ and $C_{RSS}$ and the three major semiconductor loss
Table 3.1: Integrated Device Parameters, Predicted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>3.3V MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR}$</td>
<td>3.3 V</td>
</tr>
<tr>
<td>$R_{DS-ON}$</td>
<td>42 mΩ</td>
</tr>
<tr>
<td>$C_{OSS}$</td>
<td>41 pF</td>
</tr>
<tr>
<td>$C_{RSS}$</td>
<td>20 pF</td>
</tr>
<tr>
<td>$C_{ISS}$</td>
<td>65 pF</td>
</tr>
<tr>
<td>$R_{G}$</td>
<td>500 mΩ</td>
</tr>
</tbody>
</table>

Table 3.2: Integrated Device Parameters, Measured

<table>
<thead>
<tr>
<th>Parameter</th>
<th>3.3V MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR}$</td>
<td>3.3 V</td>
</tr>
<tr>
<td>$R_{DS-ON}$</td>
<td>61 mΩ</td>
</tr>
<tr>
<td>$C_{OSS}$</td>
<td>47 pF</td>
</tr>
<tr>
<td>$C_{RSS}$</td>
<td>17 pF</td>
</tr>
<tr>
<td>$C_{ISS}$</td>
<td>82 pF</td>
</tr>
<tr>
<td>$R_{G}$</td>
<td>633 mΩ</td>
</tr>
</tbody>
</table>

components $P_{COND}$, $P_{DISP}$ and $P_{GATE}$, and finally returns an optimized device with the predicted characteristics in Table 3.1.

From a comparison of Table 3.1 to the experimentally-measured device parameters shown in Table 3.2, we see that the measured device characteristics are not far off from the algorithm-predicted values, suggesting that this algorithm is equally viable in device optimization in low-voltage CMOS process as well as other high-voltage processes.

### 3.2.2 Cascoded Structure

From the device optimization procedure described above, we are able to obtain a custom-designed switch that achieves a good balance between conduction, gating and displacement loss and minimizes the overall semiconductor loss for a given converter design on a given CMOS process. The challenge of very limited operating voltage range associated with
3.2 Device Design

Figure 3.3: Device stacking configuration, top device $M_1$ in a common-gate configuration with its gate connected to a dc bias voltage, and the bottom device $M_2$ in a common-source configuration gated on and off at the switching frequency.

the low breakdown voltage of a low-voltage CMOS process remains to be addressed. For the particular CMOS TSMC 0.35$\mu$m process, the breakdown limit voltage for the drain is 3.3V. For inverter designs with class-E waveforms, this limits the maximum input voltage to be below 1V, and significantly hinders the design and application space such a topology may be useful for. Although relatively high breakdown voltage may be achieved in a similar 0.8$\mu$m process, the best achievable switch characteristics is noticeably worse than its 0.35$\mu$m counterpart, makes it desirable to seek alternative route to address the voltage-range issue.

Device stacking (cascoding), Figure 3.3 is a viable technique to reduce the voltage stress across a single active device [67-70]. An additional device $M_1$ is placed in series with the switching device $M_2$, in such a way that the peak $V_{DS}$ voltage is divided between the two devices. In the cascode structure, the top device $M_1$ is used in a common-gate configuration (with its gate connected to a DC bias voltage) to extend the breakdown voltage range and the bottom device $M_2$ is used as a common-source device (gated on and off) at the switching speed) for its switching speed. In this manner, the bottom device "source switches" the top device. This switching scheme can ideally increase the maximum allowable input voltage by a factor of two (ideally) without introducing any additional complexity to the inverter topology. The device-stacking technique is especially attractive in an integrated approach because it simply involves in placing two switches (in this case, the optimized single device
Figure 3.4: Unequal voltage sharing in a cascode pair. A 100MHz class-E inverter is designed with a cascoded pair with two identical devices, figure 4.4. Without additional capacitance across \( M_1 \), the bottom device absorbs most voltage stress on the cascode structure, resulting in the total breakdown voltage significantly less than twice of a single device. The component values are: \( C_F = 150pF \), \( L_R = 17nH \), \( C_R = 200pF \) and \( R_L = 2.15\Omega \). Simulation files are included in Appendix D.

However, utilizing the cascoded device structure to extend its operating voltage is not without challenges. By simply stacking two identical devices in series, one does not fully extend the cascode pair's breakdown voltage to twice the breakdown voltage of an individual device, as illustrated in figure 3.4. Without careful consideration of relative capacitance sizing between \( M_1 \) and \( M_2 \), the majority of the voltage stress appears across the drain-to-source of the common-gate device \( M_1 \), which reduces the effective breakdown voltage to significantly less than twice the breakdown voltage of a single device. Furthermore, ideally, in this configuration, it would be desirable if the two devices turned on and off
simultaneously to minimize the power loss due to the overlapping of the voltage and the current. The reality is that $M_1$ and $M_2$ in the cascoded device do not turn on and off simultaneously, due to the finite amount of time it takes for the source voltage of $M_1$ to reach above $V_{GB} - V_{TH}$ after $M_2$ turns off. This transient time between having $M_1$ and $M_2$ on to turning both devices off cannot be ignored and significant loss may occur during this transition period that it defeats some of the benefits a cascode structure may bring.

Fortunately, both of these challenges associated with device-stacking with may be addressed with a single component, $C_{EX}$, figure 3.5. Incorporating a capacitive element between the drain-to-source node of the common-gate device $M_1$ not only addresses the uneven voltage sharing issue with the cascoded pair, but also accelerates the charging speed for turning off a common-gate device ($M_1$) after a common-source device ($M_2$) is turned off.

Because of the Miller effect, adding a capacitor $C_{EX}$ across $M_1$ is equivalent to adding additional capacitance $C'_{EX}$ across $M_2$, where $C'_{EX} = (1 - G_V)C_{EX}$ and $G_V$ is the voltage gain of the capacitors' nodes, figure 3.7. Due to the positive voltage gain of the common-
Figure 3.6: Adding additional capacitance across $M_1$ allows the drain voltage to be shared more equally between the two devices. A $100MHz$ class-E inverter is designed with a cascoded pair with two identical devices, figure 4.4. With additional capacitance across $M_1$, the drain voltage is shared equally between the top and the bottom device. The component values are: $C_F = 150pF$, $C_{EX1} = 50pF$, $C_{EX2} = 120pF$, $L_R = 17nH$, $C_R = 200pF$ and $R_L = 2.15\Omega$. The calculated $C_{EX1}$ value from Equation 3.5 is $51pF$. Simulation files are included in Appendix D.

The gate stage, $C'_{EX}$ appears to be a negative capacitor across $M_2$ [67]. This effective negative capacitance redistribute the voltage stresses across the two transistors, and alleviates the large voltage stress on $M_2$ with $M_1$. Based on the the peak voltage across the cascode pair, the gate bias voltage $V_{GB}$ and the threshold voltage of a single transistor $V_{TH}$, we may calculate the additional capacitance needed across the common-gate device to ensure equal voltage sharing.

Assuming two identical transistors are stacked in series, the common-gate device $M_1$ is still on until the source of $M_1$ reaches $V_{GB} - V_{TH}$, after which point, both $M_1$ and $M_2$ are off, and the ratio between the subsequent changes in drain-to-source of the two devices are

$$\frac{\Delta V_{DS2}}{\Delta(V_{DS2} + V_{DS1})} = \frac{C_{TOP}}{C_T + C_{TOP}}$$ (3.1)
3.2 Device Design

![Circuit Diagram](image)

Figure 3.7: Due to Miller effect, $C_{EX}$ across $M_1$ effectively appears as a negative capacitance across $M_2$.

where $C_{TOP} = C_{DS1} + C_{EX}$ and $C_T = C_{DS2} + C_{GD2} + C_{GS1}$. The moment before $M_1$ turns off, its drain-to-source voltage is 0 and the drain voltage of $M_2$ is $V_{GB} - V_{TH}$. In order to evenly divide the peak voltage between $M_1$ and $M_2$, we would like

\[
V_{DS2} = V_G - V_{TH} + \Delta V_{DS2} = \frac{1}{2} V_{PK} \\
V_{DS1} + V_{DS2} = V_G - V_{TH} + \Delta(V_{DS1} + V_{DS2}) = V_{PK}
\]

(3.2)

From which, we can derive that

\[
\Delta V_{DS2} = \frac{1}{2} V_{PK} - V_G + V_{TH} \\
\Delta(V_{DS1} + V_{DS2}) = V_{PK} - V_G + V_{TH}
\]

(3.3)

Based on Equation 3.1 assuming two devices are identical (i.e. $C_{DS1} = C_{DS2}$)
\[
\frac{\Delta V_{DS2}}{\Delta (V_{DS2} + V_{DS1})} = \frac{C_{TOP}}{C_T + C_{TOP}} = \frac{C_{DS} + C_{EX}}{2C_{DS} + C_{GD} + C_{GS} + C_{EX}} = \frac{\frac{1}{2}V_{PK} - V_G + V_{TH}}{V_{PK} - V_G + V_{TH}}
\]

(3.4)

Solving for \(C_{EX}\), we arrive at that in order for two identical transistors to share the voltage stress equally, additional capacitance needed is given by:

\[
C_{EX} = \frac{1}{2} \left( C_{GD} + C_{GS} \right) \left( \frac{1}{2}V_{PK} - V_G + V_{TH} \right) + C_{DS} \left( V_{TH} - V_G \right)
\]

(3.5)

The additional \(C_{EX}\) also minimizes the lossy transition state when \(M_2\) is off and \(M_1\) is on [68]. In a cascode structure, \(M_1\) and \(M_2\) do not turn off simultaneously because for a period of time after \(M_2\) is turned off, \(M_1\) is still on until the source of \(M_1\) reaches \(V_{GB} - V_{TH}\). As illustrated in Fig. 1.8, this may create a substantial amount of loss. Right after \(M_2\) is turned off, \(R_{DS1}\) of \(M_1\) starts out small, however, it increases sharply with increasing source voltage of \(M_1\), which results in only a small amount of current following in the \(R_{DS1}\) and \(C_{DS2}\) branch, causing the voltage across \(C_{DS2}\) and hence the drain-to-source voltage of \(M_2\) to rise slowly. On the other hand, a much larger portion of the current is flowing in the parasitic capacitance between the drain node of \(M_1\) and the ground, causing the drain voltage of \(M_1\) to rise quickly. The drain voltage of \(M_1\) and the source voltage are rising at two very different rates, causing a large voltage difference between them, which may lead to a substantial amount of power loss during this transition. Placing additional capacitance \(C_{EX}\) across \(M_1\) and \(C_3\) accelerates the rate at which its source voltage is being charged, and significantly reduces the amount of time it takes for the source voltage to reach up to \(V_G - V_{TH}\), at which point \(M_1\) turns off as well.

The additional \(C_{EX}\) may be implemented on-die (e.g., as either added capacitance or by re-optimizing device size) or as an additional discrete component off the chip. While placing the capacitance on-die capacitance minimizes any loop inductance that may affect the switching waveforms, it is much easier to achieve a high quality factor with a discrete capacitor, which can be important for minimizing loss. In this design, no additional \(C_{EX}\) is placed across the common-gate device on-die and an off-the-chip high-\(Q\) capacitor is employed; its effects are discussed in details in the context of an inverter in Chapter 4.
Figure 3.8: Possible cascode device states: $M_1$ and $M_2$ are both on; $M_1$ is still on while $M_2$ is off ($V_{S1}$ has yet to reach $V_{GB} - V_{TH}$; $M_1$ and $M_2$ are both off. In the middle state, the loss due to overlapping voltage and current can be significant.
In summary, device stacking (or "cascoding") is a viable technique to extend the breakdown voltage range achievable for a given IC process and it provides a simple integrated solution to further extend the operating voltage range. However, careful consideration must be given to the device capacitance sizing when utilizing the cascoded structure; additional capacitance across the drain-source port of the common-gate device may further reduce the loss incurred and fully extend the usable voltage range to twice of an individual device.

### 3.2.3 Safe Operating Area Considerations

Further benefits regarding extended operating voltage range may also arise through an expanded safe operating area (SOA) specified for devices under hard-switched operation [59]. In some cases, under ZVS soft-switched operation, where there is little voltage stress on the device at turn on or turn off, devices can be operated at higher peak off-state voltage than as suggested by their specifications for hard-switching. This occurs because the lack of high voltage at the transition reduces generation of "hot carriers" traveling through the device at the transitions. Such hot carrier effects (in conventional hard switched transitions) reduce the voltage at which devices may be used below that for device breakdown [59,71]. Therefore, for a given process, use under ZVS switching can provide higher peak operating voltage. For devices built on the $0.35\mu m$ TSMC035HV process, the avalanche breakdown voltage that we can operate an individual device at is about $5.5V$ in these soft-switched applications. With the cascoded structure with equal-voltage sharing, we can now use stacked device up to $11V$. A $3\times$ increase in breakdown voltage (compared to $3.3V$ nominal process breakdown voltage) is achieved in the same process via device-stacking and SOA utilization in ZVS soft-switched applications.

### 3.3 Integrated Gate Drive Design

Even with an optimized device geometry, driving the input capacitance of such a device tens to hundreds of MHz is not a trivial issue. For a off-the-chip gate drive design, even a few nano-henries of packaging and layout inductance may significantly distort the gate drive signal waveshape and negatively impact its efficiency and performance, such as accurate control of gate drive timing, which is critical in applications to be discussed in Chapter 5.
3.3 Integrated Gate Drive Design

Figure 3.9: A tapered buffer gate driver with N-stages and a tapering factor of F.

![Tapered Buffer Gate Driver Diagram]

Figure 3.10: The normalized delay time $t_{\text{norm}} = N(C_x + \left(\frac{C_x}{C_y} + C_y\right)/F)$ through the inverter chain given the device $C_{\text{ISS}} = 82pF$, the output capacitance, and the input capacitance of a single inverter on TSMC035HV process. The optimum number of stages in this case is 7.

The issues associated with off-the-chip gate drivers can be addressed with an integrated gate drive design on-die.

Although there have been other resonant on-chip gate-drivers implemented on-die [72], in this design, we opt for a simple tapered driver on-chip because the incremental power loss between a fully resonant design and hard-switched design is not substantial to justify the additional complexity. In order to drive this input capacitance at high speeds, tapered drivers are often required which must quickly source and sink relatively large currents while not degrading the performance of previous stages. The two criteria in designing a tapered drive considered here are propagation delay and power dissipation.
A tapered buffer structure, Figure 3.9 consists of a series of inverters where each transistor channel width is a fixed multiple, $F$, larger than that of the previous stage. Assuming the output current drive to the output capacitance (in this case, the $C_{iss}$ of the optimized device) ratio is fixed for each stage within the buffer, the inverter stage then share equal rise, fall and delay time. Since the delay through each stage is equal, the total delay with a $N$ stage inverter chain can be calculated by multiplying the single stage delay by the number of stages, $N$. As described in [1], the propagation delay through a tapered buffer is $t_{buffer} = t_{onset \text{norm}} \left( \frac{K_{UL} + K_{LU}}{2} \right)$ where the normalized delay time $t_{\text{norm}}$ (delay expressed as a function of only variables which may be controlled during the design process) of an inverter chain is $t_{\text{norm}} = N \left( C_x + \frac{C_L}{N} C_y \right)$, where $C_x$ is the output diffusion capacitance of a single inverter, $C_y$ is the input gate capacitance of an inverter and $C_L$ is the $C_{iss}$ of the optimized main device (i.e., the load capacitance to be driven), Figure 3.11. Based on this relationship, shown in figure 3.10, for a given $C_L/C_y$, there exists an optimum number of stages that minimizes the delay time. In addition, we see that when the propagation delay dramatically increases when using a value of $N$ that’s much smaller than the optimum $N$. However, the delay time only increases slowly when the actual number of stages is larger than the optimum number of stage.

The second optimization criteria used in the gate drive design is its power dissipation, for obvious reasons, as the amount of power dissipated in the gate driver directly affects the overall efficiency of the converter. The two primary mechanisms of how power is dissipated in the switching of a CMOS tapered buffer are dynamic power dissipation (often the dominant component) and short circuit power [1]. Dynamic power dissipation arises from the charging and discharging of capacitance, and it is dissipated in the channel on-resistance of the transistors. The short circuit power dissipation arises during the time in which the NMOS and PMOS devices in an inverter are both on. It’s found in [1] that using fewer buffer stages reduces both short-circuit and dynamic power dissipation within the buffer from
3.3 Integrated Gate Drive Design

Figure 3.12: Simulated Tapered Inverter Chain Gate Drive Waveforms. The waveforms shown are the simulated Cadence waveforms for a 7-stage tapered driver with a tapering factor of 4 after stage 1, 3, 5, and 7. The input capacitance of the device is 82pF.

\[ P_{total} = (K_1 + 1)V_{DD}^2f(C_x + FC_y)(\frac{-1 + CL}{F-1}) \]

where \( K \) is a constant (usually much smaller than 1) dependent on the transistor threshold voltage, velocity saturation of the drain-to-source voltage and the supply voltage.

Therefore, when both power dissipation and propagation delay are considered, the number of inverter stage should then be set as the optimum number of stages in the propagation delay calculation or the next smaller number of stages that do not significantly increase the propagation delay time.

Based on these observations and design equations, starting with a minimum-sized transistor for a given process (in this case, TSMC35HV), by varying the tapering factor and the number of stages, the propagation delay and power dissipation (both dynamic and static) to drive the input capacitance of the optimized design can be calculated based on [1]. Based on the design equations given in [1], 7 inverter stages driving the optimized cascoded device discussed in Section 3.2.2 with a tapering factor of 4 will allow VHF operation while maintaining low gating loss, 40mW at 100MHz switching speed, Figure 3.12.
Chapter 4

Parallel-Series Reconfigurable Inverter Design

This chapter proposes a new resonant inverter topology. The topology leverages the custom-designed cascoded device structure mentioned in the previous chapter to reduce switching and gating loss at VHF operation. With the cascoded structure as a building block, this design enables dramatic increases in switching frequency and bandwidth while maintaining good efficiency across a wide range of operating conditions at low voltages. The tuning procedure of such a topology is described and experimental evaluation of a prototype operating at 100MHz is presented illustrating the merits of such a design.

4.1 Background

Frequency dependent losses are one of the major factors that limit the switching frequency of conventional switch-mode power converters. Techniques such as resonant switching have been used to address these losses to in order to realize converters operating in the VHF regime. These design techniques rely on a reactive network to shape the voltage and current waveforms across the switches and reduce switching loss. The Class-E inverter, Figure 4.4 is an example of such resonant inverter designs. It shapes the switch voltage for ZVS (and ideally zero dv/dt) turn on to overcome capacitive discharge loss at turn on and overlap loss at turn on and turn off [6, 7]. In the conventional implementation of this topology, $L_F$ is a large choke inductor that only delivers DC current. Energy from the source is first stored on the capacitor $C_F$, then transferred to the load. The resonant network comprised of $C_R$, $L_R$ and $R_{Load}$ may be tuned in such a way that the voltage across the switch will ring up and then back to zero at a given later time [6, 7], allowing the inverter to turn the switch back on without any switching loss. However, there are several drawbacks of this


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class-E inverter design tuned in the traditional manner (e.g., as in [6,7]). First, the class-E inverter is unable to operate over a wide load range because $R_{\text{load}}$ is an integral part of the resonant network that shapes the switch voltage. As the load resistance changes, the inverter loses its soft-switching characteristics and incurs significant switching losses, Figure 4.1b. Furthermore, the inverter design requires a large choke inductor, limits its dynamic response (e.g., for on-off control).

![Class E inverter diagram](image)

(a) Class E inverter

![Class E drain voltage waveforms](image)

(b) Class E drain voltage waveforms

Figure 4.1: Single-switch resonant design often suffer from limited load range in power conversion applications. The classical implementation of the Class E inverter drain voltage waveforms are shown as the load is varied between $\frac{1}{2}R$ to $2R$ where (where R is the nominal load value). Component values are: $L_F = 20\mu H$, $C_P = 75.5pF$, $C_R = 97pF$, $L_R = 35nH$ and R is varied between 4.4$\Omega$ to 8.8$\Omega$. The loss of ZVS and negative impact on efficiency are evident.
4.2 Inverter Design

Here we introduce a new reconfigurable resonant inverter topology, Figure 4.2a, suitable for efficient VHF resonant power conversion across a wide operating range, and to achieving fast response speed to changes in operating conditions.

Figure 4.2: Series/Parallel Reconfigurable Resonant Inverter Topology. The inverter topology introduced here utilizes two individual inverters which can be connected in series or in parallel.
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This inverter utilizes a pair of custom-designed cascoded switches (introduced in Chapter 3) optimized for VHF operation. These devices CAS₁ and CAS₂ are tuned to operating at the VHF switching frequency. A separate set of switches SW₁, SW₂ and SW₃ reconfigures the system for different operating modes, with the reconfiguration happening at a much lower frequency. This reconfigurable structure allows the inverter to modulate power at the low "reconfiguration" frequency and/or to maintain closer to a constant output as the input voltage is varies. The inverter topology and its tuning procedure is described, along with the design of the cascoded structure and its integrated gate drive for minimizing loss. The design and experimental evaluation of prototype inverter operating at 100MHz is also described.

The design introduced here utilizes two resonant inverters, Figure 4.2b, sharing an output network and load, which can be operated with its inputs in parallel or in series, depending on the configurations of SW₁, SW₂ and SW₃. Each individual resonant inverter topology may appear similar to that of a conventional a class-E inverter. However, instead of a bulk input choke inductor, each inverter utilizes a small-valued inductor \(L_F\), resonating with any parasitic switch capacitance plus any external capacitors. The seemingly small change from a bulky inductor to a resonant inductor is in fact significant. It leads to a smaller magnetic value (hence, a smaller inductor footprint and a higher power density), and allows the inverter to achieve excellent transient response, addressing one of the key limitations of a conventional class-E inverter design.

This topology works as follows: when SW₂ and SW₃ are on (SW₁ is off), each inverter sees the full input voltage, \(V_{IN}\), and the two inverters operate with their inputs in parallel. When SW₁ is on (SW₂ and SW₃) are off, each inverter seeing half of the input voltage, \(V_{IN}/2\), and the two inverters operate with their inputs in series. With the total output power is proportional to the input voltage squared, each inverter in the series mode is delivering approximately 1/4 of its power in the parallel configuration. In steady state, for a given input voltage, when the inverter is switching back and forth between the parallel/series configurations, the inverters are operating between full power and 1/4 of the full power, achieving a much wide operating range, with merely four additional components. With its reconfigurable feature, the inverter’s output power can be easily controlled via on-off modulation control scheme []. Alternatively, if a given output power level is desired, this topology allows for a much wider input voltage range.
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The simulated waveforms in Figure 4.3 illustrate the operation of the inverter. The top device of both cascoded device, $M1$ and $M3$ are gated via a dc bias, whereas the bottom devices, $M2$ and $M4$ are gated on and off simultaneously with a square wave. Upon turning off both switches $M2$ and $M4$, the voltages at the drain of the devices $V_{DS1}$ and $V_{DS2}$ rises, the current in both resonant inductor $L_{F1}$ and $L_{F2}$ increases while capacitor in parallel to the switches $M1$, $M2$, $M3$ and $M4$ are being charged. The voltage across the drain of both cascoded structures continue to rise until the total current in $C_{EX1}$ and $C_{EX2}$ rings down to zero, at which point, the devices turns on, establishing ZVS characteristics across both devices.

4.2.1 Inverter Tuning Procedure

In order to minimize switching loss, the inverter is tuned to operate under zero-voltage switching. Since the essence of this inverter topology is comprised of two identical resonant class-E inverters, the overall inverter tuning can start by separating the two inverters and tuning each individually, Figure 4.2b. For each individual inverter, the output "tank" is comprised of $L_R$, $C_R$ and $R_L$. In conventional RF designs, the loaded Q ($Q_L$) of the class-E inverter is usually chosen to be quite large. However, the requirements on $Q_L$ for power conversion is different, since the goal is to maximize power transfer with minimum loss. In this case, a lower $Q_L$ value is preferred because it results in less energy resonated in the tank, consequently reduces the conduction loss in the parasitic elements of the inverter.

Following the design equations for class-E RF inverters with low $Q$ in [73], the component values for $L_R$, $C_R$ and $R_L$ can then be determined for a given operating frequency, input voltage, power level and $Q_L$.

The input resonant network, comprising $L_F$, $C_{EX1}$, $C_{EX2}$ and any additional parasitics shunt capacitance of the cascoded device, largely shapes the frequency at which the drain waveform rings up and down. For an inverter operating at a 50% duty ratio, one possible starting point for $L_F$ is to tune the input resonant network such that its resonance frequency is at twice the switching frequency, as in (4.1). This tuning selection is similar to that of the "second harmonic" class E inverter in [11,13].
Figure 4.3: Series/Parallel Drain and Gate Drive Voltage Waveforms. $V_{GB}$ is the gate bias voltage applied on the common-gate device in the cascode structure $M_1$, $V_B$ is the gate voltage on the common-source device $M_2$ and is switching at the operating frequency 100 MHz. The inverter drain voltage $V_DS$ across each cascode device and the voltage across the bottom device of the cascode structure are also shown. Relevant simulation files can be found in Appendix B.

Figure 4.4: Class E Inverter
4.2 Inverter Design

\[ L_F = \frac{1}{16\pi^2 f_{SW}^2 C_F} \]  

(4.1)

Note that the capacitor \( C_F \) is the total shunt capacitance in parallel with the semiconductor switching including the parasitic capacitance of the semiconductor switch and possibly external capacitors \( C_{EX1} \) and \( C_{EX2} \). In some applications where the packaging inductance of the semiconductor switch is significant, selecting \( C_F \) to be solely provided by the device capacitance may be a good choice, because it prevents waveform distortion caused by additional ringing between the external capacitance and the package inductance. In other cases where the circulating current is significant, it is a better choice to add additional high-Q ceramic capacitance in parallel with the lossy device parasitic capacitance to reduce the circulating current loss. One starting point for \( C_F \) is to assume it is comprised solely of parasitic capacitance of the semiconductor switch, allowing an initial value of \( L_F \) to be calculated. Since \( L_F \) significantly impacts the transient response speed, a small \( L_F \) is generally preferred. If the starting point of \( C_F \) leads to too large a value of \( L_F \), additional parallel capacitance \( C_{EX1} \) and \( C_{EX2} \) may be added until the value of \( L_F \) is in the desired range.

Once the initial values of \( L_F \), total \( C_{EX} \), \( L_S \) and \( C_S \) are determined from the procedure above, additional tuning can be made via minor adjustments of the component values along with the duty ratio until the resulting drain-to-source switching waveform \( V_{DS} \) achieves ZVS and zero \( dv/dt \) turn on, the so-called class E switching waveform.

Once an individual resonant inverter design has been determined, the purposed parallel-series topology may be accomplished via merely four additional component \( SW1, SW2, SW3 \) and \( C_3 \). When the two inverters are connected, \( C_3 \) is selected to be as small as possible provided that it’s still an AC short at the switching frequency, because \( C_3 \) directly influences the transient response speed of such a inverter. The larger the \( C_3 \) is, the more time it takes to extract the energy out of the capacitor when the inverter switches between parallel and series operation, Figure 4.5. When combining two inverter to achieve the proposed design via \( C_3 \), the drain-to-source impedance seen by each cascoded device pair \( CAS_1 \) and \( CAS_2 \) may slightly change, resulting in slightly different circuit waveforms and power levels. Minor additional tuning may thus be required to achieve ZVS and the required power level.
4.2.1.1 Design Considerations about $C_{EX1}$ and $C_{EX2}$

For a given design, the total $C_F$, which includes the parasitic capacitance of the semiconductor switch and external capacitors, can be determined from the tuning procedure just described. For a given semiconductor switch, once the overall $C_F$ has been determined, there are many ways to divide the required external capacitance between the two devices in the cascoded pair, Figure 4.6. There are two factors that determine how the capacitance

![Figure 4.5: Effect of $C_3$ on transient response speed. $C_3$ is selected to be as small as possible provided that it's still an AC short at the switching frequency. Component values are $C_1 = C_2 = 0.01\mu F$, $L_{F1} = L_{F2} = 18.5nH$, $C_{EX1} = C_{EX3} = 47pF$, $C_{EX2} = C_{EX4} = 80pF$, $L_R = 17.5nH$, $C_R = 230pF$ and $R_L = 2.11\Omega$. At 100MHz of switching frequency, $C_3 = 0.01\mu F$ and $C_3 = 0.1\mu F$ are both an AC short. A smaller value of $C_3$ is preferred in this case for its faster transient response speed. Simulation script is included in Appendix B.](image)
Figure 4.6: Different ways to divide the required external capacitance among the cascoded structure to achieve ZVS characteristics.

may be shared between the two external capacitors, voltage-stress on each individual device and additional ringing introduced by the parasitic inductance.

From the device sizing discussion in Chapter 3, we see that the relative amount of capacitance across the individual device determines the voltage sharing between the two devices in a cascoded pair. In designs where external off-the-chip high-Q ceramic capacitors are desired, the same voltage-sharing relationship holds as well. From Figure 4.7, it is apparent that if the total required capacitance is provided by one external capacitor $C_{EX}$ only, the voltage is shared unequally among the two devices, $M_1$ and $M_2$, leading to $M_1$ breaking down earlier than $M_2$ and the full available extended voltage range being under-utilized. In order to share the voltage equally between $M_1$ and $M_2$, both Figure 4.6(a) and Figure 4.6(b) are valid ways to distribute the total required external capacitance. The exact calculation to arrive at a value of $C_{EX}$ for equal voltage sharing is discussed in Chapter 3.

A second consideration of how the external capacitance should be shared between the devices comes from the significant effects of parasitic inductance at hundreds of MHz operating frequency. From the previous discussion, we see that both Figure 4.6(a) and (b) are feasible ways to distribute capacitance among the two cascoded switches to fully extend its operating voltage range to twice of an individual device. However, at an operating frequency of 100MHz, a few nano-henries of packaging and layout inductance parasitics can significantly impact the waveform shape and efficiency. In this design particularly, the parasitics at the drain node of the cascoded device not only impact the overall inverter negatively, but also tremendously decrease the practical voltage range the inverter is able to operate at, Figure
Figure 4.7: Voltage sharing between two devices in a cascoded pair based on external capacitance distribution. Figure 4.7a illustrates the drain-to-source voltage waveforms for a cascoded device under configuration Figure 4.6(a). The drain voltage is unevenly distributed among the two devices although the switches achieve ZVS waveforms. Figure 4.7b and 4.7b illustrate the same drain-to-source voltage waveforms under configuration Figure 4.6(b) and (c). In both cases, equal voltage sharing is achieved within the cascoded device. Simulation script and component values are included in Appendix B.
4.2 Inverter Design

4.2.2 Gate Width Switching

One aspect of the purposed inverter design that may be further improved is its gating loss in "series" mode, when the system is operating at reduced power. In the series configuration, the output power is scaled back to a quarter of its power in parallel configuration, while its gating loss remains constant (assuming continuous switching of the high-frequency switches), consuming a larger portion of the overall efficiency. This can be achieved through a control concept that has similar advantages to "gate width switching", a technique sometimes used in CMOS converters.

Gate width switching is a method that helps circumvent the issue of increasing gating loss at light-load [74,75]. The principle of width switching involves that the optimum width of a MOSFET changes with the load of an inverter. If the width of a given transistor can be altered to their respective optimum value for each load, then the maximum efficiency over a wide output power range can be achieved. Under gate width switching, two parallel power MOSFETs operate in tandem during high load currents and switched so that only a smaller device continues to operate under light load conditions. The concept is based on the assumption that the majority of dynamic losses in low-voltage, CMOS converters results from driving the MOSFET's input capacitance. When light-load condition is detected, the gate of one of the two parallel power MOSFETs is grounded so that only one MOSFET continues to actively switch and carry any load current. Since only a portion of the total gate width is being driven under light load, the input current of one of the devices is zero and overall inverter efficiency is improved.

In the purposed inverter design, the cascoded device pair CAS1 and CAS2 are being switched on and off simultaneously under both parallel and series configurations, with M1 and M3 biased by a dc voltage and M2 and M4 gated on and off by the same 100MHz square waveform, figure 4.9a. However, in the series case, where the power level is scaled
Figure 4.8: Drain-to-source on the cascoded pair due to external capacitance placement including the effects of layout and packaging parasitics for configurations shown in figure 4.6(b) and (c). Both configurations achieve equal voltage sharing among the cascoded device, as shown in figure 4.7b and 4.7c. However, the peak voltages on the stacked devices are different when the parasitic inductance is taken into account. In this case, figure 4.6 results in a lower peak voltage and is therefore preferred. Simulation script and component values are included in Appendix B.
back to a quarter of its full power, the cascoded device pair are oversized, resulting in deteriorated inverter efficiency. While we do not have a device comprising paralleled sections that would admit traditional gate-width switching, we can take advantage of the proposed circuit structure to achieve similar results in gating loss. In this case, since both inverter blocks are linked via a dc-blocking capacitor $C_3$, this topology offers an inherent gating loss reduction capability. By alternating and pulse-skipping gate switching waveforms between $M2$ and $M4$ (while maintaining the dc bias at $M1$ and $M3$), Figure 4.9b, only half of the cascaded device pair is being utilized in a given switching cycle, achieving the loss advantages of gate-width switching without any additional components in the inverter stage. The amount of gating loss saved in this alternative gating scheme far offsets the incremental additional conduction loss, and improves the overall inverter performance in the series configuration. One could undertake this same "alternating pulse" operation in the parallel configuration; it would only be beneficial at low input voltages, however, when the reduction in gating loss outweighs the increase in conduction loss. Consequently, the pulse skipping operation is most advantageous in the series mode, where power is naturally low.

4.3 Inverter Implementation and Experimental Results

Following the tuning procedure previously described, a practical implementation for a 100MHz inverter is designed. The basic characteristics and component values are included in Table Table 4.1. At a switching frequency of 100MHz, the inverter was designed for an input voltage of 2.5V and a full output power level of 1.5W. The custom-designed cascoded device structure utilized here is described in Chapter 3.

The basic inverter waveforms as simulated are presented in Figure 4.3, with the simulation files available in Appendix B. The inverter implementation is tuned according to the procedure outlined in Section 4.2.1. For a given operating frequency, input voltage and output power level, the values of the load tank network, $L_s$, $C_s$ and $R_L$ can first be determined using the design equations in [7]. For a load network with a $Q$ of 5, an input voltage of 2.5V, an output power of 1.5W at 100MHz switching frequency, the following set of equation from [7] may be used to determine the load network ($L_s$, $C_s$ and $R_L$) and the total capacitance needed in parallel with the switch $C_F$ (including external capacitance and device parasitic capacitance) to achieve ZVS.
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\[
\frac{P_{QRL}}{V_{IN}^2} = 0.5166 \\
\omega R_L C_S = 0.26924 \\
\frac{\omega L_S}{R_L} = 5 \\
\omega R_L C_F = 0.20907
\]

Figure 4.9: Non-Skipping vs. Pulse-Skipping Gate Drive Scheme. In both case, the inverter output is operating at 100MHz with nearly identical drain-to-source waveforms. However, the gating loss is cut by in the pulse-skipping case due to the inherent switching control capabilities of the topology.
4.3 Inverter Implementation and Experimental Results

Table 4.1: Component Values and Specifications for Parallel-Series Inverter

<table>
<thead>
<tr>
<th>Component/Spec</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{F1}, L_{F2}$</td>
<td>18.5 nH</td>
</tr>
<tr>
<td>$C_{EX1}, C_{EX3}$</td>
<td>80 pF</td>
</tr>
<tr>
<td>$C_{EX2}, C_{EX4}$</td>
<td>47 pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>0.01 $\mu$H</td>
</tr>
<tr>
<td>$L_R$</td>
<td>17.5 nH</td>
</tr>
<tr>
<td>$C_R$</td>
<td>200 pF</td>
</tr>
<tr>
<td>$R_L$</td>
<td>2.11 $\Omega$</td>
</tr>
<tr>
<td>$CAS_1, CAS_2$</td>
<td>Custom-Designed Cascoded Pair</td>
</tr>
<tr>
<td>$M_1, M_2, M_3, M_4$</td>
<td>Device Characteristics shown in Table 3.2</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>2.5 V</td>
</tr>
<tr>
<td>$P_{OUT}$</td>
<td>1.5 W</td>
</tr>
<tr>
<td>$f_{SW}$</td>
<td>100 MHz</td>
</tr>
</tbody>
</table>

Then based on the operating frequency, component values of input resonant network $L_F$ and $C_{EX1}$ and $C_{EX2}$ can be realized from Equation 4.1. When the device parasitic lead inductances are modeled in the simulation, which introduces the extra ringing visible in the drain waveforms.

The inverter prototype was constructed using standard PCB techniques, with its full schematics and PCB layout files available in Appendix B. Figure 4.10 shows a picture of the inverter prototype along with a plot of measured $V_{DS}$ for the top and bottom cascoded structures. Whereas the first-order design procedure provides a starting tuning point for the inverter, the final tuning point was chosen by iterating design values and measured values in the impedance domain. This characterization allows the PCB and individual components to attain the best possible match between simulation and experiment. The inverter achieves an efficiency of 76% in the parallel case with an output power of 1.48W and an efficiency of 62% in the series case (with continuous switch gating) with an output power of 0.36W. As described in Section 4.2.2, gate drive loss becomes a larger portion of the total loss budget in the series configuration, owing to the drive loss remaining constant while output power reduces; this causes a loss in efficiency of nearly 14%. Figure 4.11 illustrates the experimental waveforms for the inverter under pulse-skipping gate drive scheme. Under this gating scheme, the gating loss is reduced by nearly a half and the inverter efficiency performance is improved to 68% under the pulse-skipping gating scheme. There is a slight asymmetry in the drain-to-source waveforms depending on which cascoded device is being
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Figure 4.10: Inverter prototype picture and experimental inverter drain waveforms. The operating conditions are: $V_{IN} = 2.5V$, $P_{OUT} = 1.5W$, $f_{SW} = 100MHz$. $V_{DS}$ is the voltage across the entire cascoded structure, and $V_{DSMID}$ is the drain-to-source voltage on the bottom device of the cascoded device.

gated on. This waveform asymmetry is due to the small differences in current paths on the prototype board for the two inverters.

As described in Section 3.2, the small sizes of the energy storage elements used in the design of the inverter allows for faster transient response speed than in traditional class E inverters having an input choke inductor. This benefits the ability to control the output under on-off control (or "parallel-series-off" control, as may be realized here). Figure 4.12 shows the command signal and the drain to source voltage of the cascoded structure $CAS_2$ when the inverter switches between the series and parallel configuration. At 100MHz operating frequency, the inverter is able to settle at about 10 cycles when its power is scaled up and down by modulating between series and parallel forms. The superior response characteristic
4.3 Inverter Implementation and Experimental Results

Figure 4.11: Experimental waveforms illustrating the gate drive and drain waveforms of non-pulse skipping and pulse-skipping gating scheme in the series configuration. The operating conditions are: $V_{IN} = 2.5V$, $P_{OUT} = 1.5W$, $f_{SW} = 100MHz$. The drain voltage shown here is the voltage across $V_{DS2}$ the cascoded device as shown in Figure 4.2a.
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of the resonant converter can be ascribed to the far lower values of inductance and energy storage of the resonant converter power stage, owing to its high switching frequency, which clearly indicates the merits of VHF resonant designs across a wide operating conditions for a low-power application.

Figure 4.12: Waveforms illustrating inverter transient performance switching between full power and 1/4 of full power, by switching between series and parallel modes.
VHF POWER conversion is especially challenging at low output voltages. One of the difficulties is resolving poor efficiency due to rectification loss. Even the best Schottky diodes of today have about 0.3V forward voltage drop. This forward voltage of the rectifying Schottky diode alone sets a theoretical maximum of efficiency at 90 % for an output voltage of 3V. At low output voltages, replacing a rectifying Schottky diode with a synchronous switching device (an active rectifier switch) offers a significant opportunity to improve efficiency. Given its high switching speed and low driving loss advantages, a MOSFET is deemed as suitable substitution for diode in low voltage rectification. This is so-called synchronous rectification.

However, implementing synchronous rectification in the VHF frequency regime is not without its challenges. While some synchronous rectification implementations have been demonstrated in [13, 76–81], the approaches e.g. gate drive techniques demonstrated in previous designs do not produce satisfactory performance at the VHF frequencies. Accurate control of the gate-drive timing is critical to achieve optimum performance for a synchronous rectifier. Unfortunately, at hundreds of MHz, even a few nano-henries of parasitic inductance can tremendously impact the gate drive waveshape and timing. Parasitic inductance associated with off-the-chip designs can tremendously impact the timing of the gate drive signal, which is critical to synchronous rectification. Moreover, at hundreds of megahertz, switching and gating losses associated with most commercial low-voltage transistors are so substantial (even when soft-switching and resonant gating techniques are employed) that it defeats the whole purpose of replacing the diode with another switch. Together, these design challenges make a VHF synchronous rectifier design extremely difficult.
In this section, we introduce a resonant synchronous rectifier topology, which leverages the custom-designed cascoded device structure described in Chapter 3 to reduce switching and gating loss associated with an active rectifier device. Furthermore, with its on-die gate driver, the cascoded structure also provides excellent timing control of gate drive signal. Even at output voltage at 1V, this rectifier design achieves reasonably good efficiency while maintaining excellent transient performance and bandwidth. Together with the inverter introduced in Chapter 4, this rectifier design enables dramatic increases in switching frequency and bandwidth while maintaining good efficiency across a wide range of operating conditions at low voltages. The tuning procedure of such a resonant synchronous rectifier is described and experimental evaluation of a converter prototype incorporating this rectifier topology operating at 100MHz is presented.

5.1 Background

Various design techniques suitable for VHF operating frequencies (30 - 300 MHz) have been discussed in [3, 6, 8, 10, 16-18, 27, 32, 60-62, 82-85]. As illustrated in Figure 5.1, these circuits have several blocks. This typically includes a soft-switched resonant inverter having ground-referenced switches to produce an intermediate ac waveform. The inverter output is then coupled to a resonant rectifier stage through a transformation stage (a matching network or transformer) to achieve dc-dc conversion. Much of the study thus far has been targeted at medium-to-high voltage (>5V) and medium power (>5W) applications. While certain design considerations are similar, tradeoffs for low-voltage, low-power applications can be quite different.

Most previous VHF converter designs such as those discussed in [3, 6, 8, 10, 16-18, 27, 32, 33, 60-62, 80, 82-85] have relied on diode rectifiers. Resonant dc-dc converter designs utilizing
such rectifier designs have been able to realize efficient power conversion in the VHF regime at medium-to-high voltages (>5V). However, the exacerbated conduction loss associated with the diode forward drop, $V_F$ in such designs have made these topologies unsuitable for the low output voltage applications.

The class-E zero-voltage-switching (ZVS) rectifier is an example of such resonant rectifier design that realize high-efficiency ac/dc power conversion at high frequencies, Figure 5.2a, [14,86,87]. Utilizing time reversal duality, a class-E rectifier topology can be derived from the class-E inverter structure. The switching condition found in class-E ZVS rectifiers is very similar to that of class-E inverters. The current and voltage waveforms of these rectifier designs are time-reversed images of the corresponding waveforms in class-e inverters, Figure 5.2b. When the diode is off, the capacitor current $i_C$ is equal to the inductor current, which can be modeled as a DC current sink. Consequently, the capacitor voltage rises linearly. When the diode voltage reaches its threshold voltage, the diode turns on, with the derivative of its voltage after turn-off being zero. Then the diode voltage slowly decreases, reaches its peak voltage, and then gradually returns to zero. Under this soft-switching operation, where the diode turns on at low $dv/dt$ and turns off at zero $dv/dt$, switching losses in both switching transitions are minimized.

5.2 Rectifier Design

In the conventional class-E rectifier described above, $L_F$ is a large choke inductor that keeps the near-zero ripple in the output filter current. Similar to the case of a conventional class-E inverter, this significantly limits dynamic response and achievable wide bandwidth of the rectifier design.

Similar to the case of a class-E inverter, we may replace the choke inductor $L_F$ in a conventional class-E rectifier with a resonant inductor $L_{REC}$ to arrive at a fully resonant rectifier design to improve its transient response speed while maintaining its soft-switching ZVS characteristics, as shown in figure 5.4.
**Class E Rectifier**

**Figure 5.2:** Conventional class-E rectifier topology and its voltage and current waveforms. In the conventional implementation, $L_F$ is a choke inductor.

**Figure 5.3:** Fully-resonant Class E rectifier
5.3 Class-E Synchronous Rectification

A fully resonant class-E synchronous rectifier may be derived from a class-E fully resonant rectifier by replacing the diode by a controllable switch, Figure 5.5. As a transistor has a smaller saturation resistance than a diode, the circuit has an advantage of potentially reducing power dissipations caused by the switch current (provided that gating loss and other constraints, such as accurate timing control, are dealt with). The ground-referenced switch of such a synchronous rectifier topology may also reduce the complexity of the gate.

![Rectifier Voltage and Current Waveforms](image)

(a) Fully-resonant class E rectifier voltage and current waveforms

![Startup Transient Comparison](image)

(b) Class E drain voltage waveforms

Figure 5.4: Class-E rectifier topology, its voltage and current waveforms and its transient performance. The small-valued $L_{REC}$ in a fully resonant class-e rectifier leads to much improved transient performance. Simulation files are included in Appendix C.
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![Diagram of a resonant class-E synchronous rectifier](image)

Figure 5.5: Resonant class-E synchronous rectifier
driver circuitry and makes it an attractive implementation especially because gating is not a trivial issue at hundreds of MHz operating regime.

The particular resonant rectifier topology of interest here utilizes a resonant tank comprising a resonant inductor $L_{REC}$ and a capacitance comprising the external capacitor $C_{REC}$ along with additional parasitic capacitance from the switch $M_1$ and $M_2$. Similar to the case of the inverter discussed in Chapter 4, the top device of the cascoded switch for the synchronous rectifier is biased at a dc voltage and the bottom device is switched on and off at 100 MHz with a square wave. To evaluate rectifier operation, the rectifier is driven by sinusoidal current source at the switching frequency, providing an approximate representation of the inverter behavior. The output is modeled as a voltage source of value $V_{OUT}$, which represents the behavior of the rectifier load when the output voltage is controlled under closed-loop operation. Figure 5.6 illustrates the rectifier operation via time domain simulation results.

The current flowing through the resonant shunt capacitor $C_{REC}$ along the gate drive signal $V_G$ shapes the voltage across the switch so that it turns on and off at low $di/dt$, reducing the current passing through at both transitions. The switch voltage $V_{REC}$ gradually increases when the capacitor current $I_{CREC}$ is negative, and the voltage reaches its peak value when $I_{CREC}$ is zero. Thereafter, $V_{REC}$ gradually decreases and returns to zero when $I_{CREC}$ is positive, after which point the switch may be turned on and the inductor current $I_{LREC}$ increases until the switch is turned off and the cycle repeats itself. The resonant frequency of $C_{REC}$, which includes any additional parallel parasitic capacitance of $M_1$ and $M_2$, and $L_{REC}$ shapes the frequency at which $V_{REC}$ rings up and down. An active switch introduces an additional degree of freedom, duty ratio $D$. For a given design, we may adjust $D$ in
5.3 Class-E Synchronous Rectification

Figure 5.6: A class-E synchronous rectifier and its voltage and current waveforms. At an output voltage of 1V, the component values are: $C_{REC} = 100pF$, $L_{REC} = 23nH$, $L_{IN} = 5nH$, $C_{OUT} = 0.001\mu F$. Simulation files are included in Appendix C.


5.3.1 Rectifier Tuning Procedure

Consider the circuit for rectifier tuning shown in Figure 5.5, the amplitude of the current source driving the rectifier is selected such that the output power requirement can be met (Note that a whole range of values may be successfully used). There are four design handles in this synchronous rectifier, $L_{REC}$, $C_{REC}$, the duty ratio $D$ of the gate drive signal and the time at which the device is turn on $T_D$. A straightforward way to tune this rectifier topology given a specified amplitude of the current source is to adjust $C_{REC}$ and $L_{REC}$ until a desired...
characteristic impedance \( Z_0 = \sqrt{L_{REC}/C_{REC}} \) and center frequency \( f_C = \frac{1}{2\pi\sqrt{L_{REC}C_{REC}}} \) is achieved, while adjusting the duty ratio \( D \) and \( T_D \) of the gate drive signal such that desired ZVS characteristics is achieved. The analysis for a conventional class-e rectifier may serve as a starting tuning point for such a rectifier [86]. Based on this initial tuning point, the choke inductor is then replaced by a resonant inductor \( L_{REC} \) such that \( L_{REC} \) and \( C_{REC} \) including the device parasitic capacitance and any additional external capacitor is tuned to resonate at about twice the switching frequency if a duty cycle of 50% is to be obtained. The rectifier input impedance can be tuned to look resistive, slightly capacitive or slightly inductive, \( Z_{REC} = V_F/I_F \), Figure 5.7. The characteristic impedance of the rectifier determines the output power, while the center frequency determines whether the rectifier input impedance is made to look resistive at the fundamental or to include a reactive component. The input impedance of the rectifier in the describing sense is then the impedance found by looking at the fundamental voltage and current components, which can then be used in the inverter design. For a given rectifier output voltage and output power requirement, there are many tuning points that achieve both ZVS operation and the desired output power. The overall rectifier efficiency and its operating range are considered also to reach an optimum design.

In addition, by adjusting the resonant capacitor along with the resonant inductor, the peak reverse voltage and the length of the conduction interval of the switch can be traded off [18]. For certain design where low-voltage CMOS devices are employed, the break-down voltage of the switch (in this case, the combined breakdown voltage of \( M_1 \) and \( M_2 \)) itself needs to be taken into consideration while determine the appropriate values for \( L_{REC} \) and \( C_{REC} \), Figure 5.8.

### 5.3.2 Converter Tuning

An entire dc-dc converter design maybe accomplished by connecting the tuned inverter, introduced in Chapter 3, with the synchronous rectifier design, Figure 5.9.

The input impedance of the rectifier now becomes the load network for the inverter. In some cases, a transformation stage, such as a matching network may be needed when the impedance achieved by the rectifier at a given output power level (following the tuning procedure from the previous section) is too high for the inverter to achieve ZVS, provide minimum output power, or operate at acceptable efficiencies. However, introducing this
additional sub-system between the inverter and the rectifier does not necessarily introduce additional components or circuit complexity, Figure 5.10. It is possible to absorb the matching network component $L_M$ and $C_M$ into the inverter component $L_R$ and $C_{REC}$.

When the inverter and rectifier are connected, the drain waveforms and the output power level may be slightly different from what the inverter provides due to the non-linear interaction between the inverter/matching network with the rectifier; minor additional tuning may be required to achieve ZVS and the required power level. If the converter is no longer displaying ZVS operation, minor adjustments to component values, by changing the center frequency of $C_F$ and $L_F$ or $L_R$ and $C_R$ following the same procedure outlined for achieving ZVS in tuning an inverter in Section 3.2, will lead to soft-switching drain voltage waveforms. If the power level of the converter is lower than required, the impedance of all components may be lowered until the output power is as desired. On the other hand, the impedance of all components may be increased by the same factor to maintain the overall switching
Figure 5.8: Synchronous rectifier’s peak voltage vs. duty ratio. By adjusting $C_{REC}$ and $L_{REC}$, the peak voltage and the length of the conduction interval of the switch can be traded off. Simulation files for this example may be found in the Appendix C.

Figure 5.9: Dc-dc converter with synchronous rectifier. The converter may be achieved by connecting the inverter introduced in Chapter 3 with the rectifier topology.
5.3 Class-E Synchronous Rectification

Figure 5.10: Dc-dc converter with synchronous rectifier and a transformation network. The transformation network components $L_M$ and $C_M$ may be absorbed into $L_R$ and $C_{REC}$.

behaviors if the output power is higher than desired [88]. While the minor additional tuning may take a few iterations to achieve the desired output power level and switching characteristics, it can be done very quickly based on a knowledge of the effect each component has on the inverter and rectifier behavior. Figure 5.11 shows the final converter simulation waveforms. As Figure 5.11 indicates, the drain and rectifier waveforms are not identical for those of a converter as that of an inverter or a rectifier due to the non-linear interaction between the two subsystems.

In addition to overcoming the gating and conduction loss of the rectifier device, maintaining accurate timing of the gate drive signal for the synchronous rectifier device is another challenge associated with most synchronous rectification topologies. In this topology however, with the on-chip gate driver, and topology's inherent insensitivity to the gate drive signal timing, Figure 5.12, the converter is able to operate with ZVS characteristics efficiently to tolerate a wide range of gate drive signal timings.

Another critical component of a synchronous rectifier implementation at 100MHz is its gate-driver timing adjustment circuitry. A programmable ECL delay chip MC100EP195 is employed to generate the desired delay time between the gate drive voltage $V_G$ and $V_{GSR}$. The delay chip is able to generate a time delay between 2.2ns to 12.2nS, with approximately 10ps increments. As shown in Figure 5.12, the converter is able to operate with ZVS characteristics across a wide range ($\pm 1ns$) of gate drive signal timings, and the level of accuracy that the programmable delay chip provides is more than enough for the synchronous rectifier and the converter to achieve the desired switching waveforms and performance. The circuit to achieve this operation is illustrated in Figure 5.14. The
Figure 5.11: 100MHz dc-dc converter with synchronous rectifier simulation waveforms. The operating conditions are $V_{IN} = 2.3V$, $P_{OUT} = 1.5W$, $V_{OUT} = 1V$, and $f_{SW} = 100MHz$. Component values are $C_1 = C_2 = 0.01\mu F$, $L_{F1} = L_{F2} = 18.5nH$, $C_{EX1} = C_{EX3} = 47pF$, $C_{EX2} = C_{EX4} = 80pF$, $C_3 = 0.01\mu F$, $L_R = 10nH$, $C_R = 390pF$, $C_{REC} = 200pF$, and $L_{REC} = 12.5nH$. Simulation files are included in Appendix C.

The synchronous rectifier is operating at a constant duty ratio 50%. The inputs to the circuit are P/S, CLK, EN and RESET while the outputs are GATE1, GATE2 and GATE_{SR}. The circuit generates pulse-skipping or non-pulse-skipping gate drive waveforms based on the input pin P/S, which also determines whether the circuit is operating in series or in parallel. The EN pin is set as high and the RESET input pin is set low. CLK is an input clock signal that establishes the switching frequency of the gate drive signal for the power stage. The programmable delay chip $MC100EP195$ is shown as a time delay block $T_D$, and there are eleven additional input pins ($t_0$ to $t_{10}$) for this chip determining its exact output signal time delay based on its configuration pin P/S, which can be either controlled via an FPGA board or an external terminal strip. GATE1 drives the tapered driver for the inverter device $M_2$. 

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5.4 Converter Implementation and Experimental Results

Following the tuning procedure just described, a practical implementation of a 100MHz converter is designed. The basic characteristics and component values are included in Table 5.1. At a switching frequency of 100MHz, the converter was designed for input
Parallel/ Series Reconfigurable Converter Design

voltage of 2.3V, output voltage of 1V and a full output power level of 1.5W. The custom-designed cascoded device structures, which include an on-chip gate driver described in Chapter 3, are utilized as switches for the inverter and the synchronous rectifier.

The converter prototype was constructed using standard PCB techniques, with its detailed schematics and board layout included in Appendix C. Figure 5.15 shows a picture of the converter prototype along with a plot of measured $V_{DS}$ along with the $V_{REC}$. Whereas the first-order design procedure outlined in Section 5.2 provides a starting tuning point for the converter, the final tuning point was chosen by iterating design values and measured values.

Figure 5.13: Synchronous rectifier experimental gate drive waveforms with no pulse-skipping (a) and pulse-skipping gating scheme (b). The component values and the gate-drive schematics are included in Appendix C.
5.4 Converter Implementation and Experimental Results

Figure 5.14: Timing adjustment circuitry for the 100MHz dc-dc converter with synchronous rectification. A 3.3V ECL programmable delay chip MC100EP195 is used to generate the time delay block $T_D$, which can achieve a time delay between 2.2ns to 12.2nS, with approximately 10ps increments. The detailed schematics and board layout are included in Appendix C.

Table 5.1: Component Values and Specifications for Parallel-Series Converter with Synchronous Rectifier.

<table>
<thead>
<tr>
<th>Component/Spec</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{F1}, L_{F2}$</td>
<td>17.5 nH</td>
</tr>
<tr>
<td>$C_{EX1}, C_{EX3}$</td>
<td>120 pF</td>
</tr>
<tr>
<td>$C_{EX2}, C_{EX4}$</td>
<td>47 pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>0.01 μH</td>
</tr>
<tr>
<td>$L_R$</td>
<td>8 nH</td>
</tr>
<tr>
<td>$C_R$</td>
<td>390 pF</td>
</tr>
<tr>
<td>$L_{REC}$</td>
<td>12.5 nH</td>
</tr>
<tr>
<td>$C_{REC}$</td>
<td>200 pF</td>
</tr>
<tr>
<td>$M_1$ to $M_6$</td>
<td>Custom-Designed Cascoded Pair</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>2.3 V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>1 V</td>
</tr>
<tr>
<td>$P_{OUT}$</td>
<td>1.5 W</td>
</tr>
<tr>
<td>$f_{SW}$</td>
<td>100 MHz</td>
</tr>
</tbody>
</table>
Parallel/Series Reconfigurable Converter Design

Figure 5.15: Converter prototype pictures.

Figure 5.16: Converter model including all critical layout and packaging parasitic inductances. This model is attained via measurements of the PCB board in the impedance domain. With all other component values the same as those in figure 5.11, the additional parasitic component values are: $L_{PAR1} = 0.6nH$, $L_{PAR2} = 0.5nH$, $L_{PAR3} = 1nH$, $L_{PAR4} = 1.3nH$, and $L_{PAR5} = 0.5nH$. The simulation files capturing this model are included in Appendix C.
in the impedance domain. This characterization allows the PCB and individual components to attain the best possible match between simulation and experiment, as seen in Figure 5.17a and Figure 5.17b. Additional packaging parasitic inductances at the drain of each cascoded structures are included and the layout parasitic inductances in the high-frequency resonant loops are also added to capture the behaviors of the overall converter system, Figure 5.16. The experimental converter waveforms are very similar to the simulated ones after the effects of the parasitic inductance (both layout and packaging) are taken into consideration,
Parallel/Series Reconfigurable Converter Design

suggesting that the overall converter system is accurately captured in the converter model. The converter achieves an efficiency of 64% in the parallel case with an output power of 1.37W and an efficiency of 58% in the series case with an output power of 0.47W. Compared to the theoretical maximum efficiency of a similar class-e diode rectifier version of 30% at similar operating voltages and power levels, the synchronous rectifier is indeed an attractive alternative at lower output voltages. It should be noted that while this is achieved with a low-input-voltage dc-dc converter, one could also realize a design with a high-input voltage and a transformation stage with a large transformation ratio.

In both the inverter and rectifier design, we are cognizant of detrimental effects that large-valued inductors have on the overall converter performance, and the resonant networks in the inverter and rectifier are tuned in a way to keep the value of $L_F$, $L_R$ and $L_{REC}$ small provided that they are not on the same order of magnitude with the lossy parasitic packaging and layout inductance. The small sizes of the energy storage elements used in the design of the inverter allows for faster transient response and much higher achievable bandwidth. Figure 5.18 shows the command signal and the drain to source voltage of the cascoded structure $CAS_2$ when the converter switches between the series and parallel configuration. At 100MHz operating frequency, the converter is able to settle at about 15 cycles when its power is scaled up and down. The superior response characteristic of the resonant converter can be ascribed to the far lower values of inductance and energy storage of the resonant converter power stage, owing to its very high switching frequency, which clearly indicates the merits of VHF resonant designs across a wide operating conditions for a low-power application.
Figure 5.18: Waveforms illustrating converter transient performance switching between full power and 1/4 of full power, by switching between series and parallel modes.
Chapter 6

Summary and Conclusions

This thesis explores the design techniques of very high frequency (VHF) dc-dc converters with high bandwidth and wide operating range at low voltages. Through developments in design techniques encompassing passives, devices and circuit topologies, a 100MHz dc-dc converter with synchronous rectifier is developed and demonstrated. By operating at hundreds of MHz switching frequencies, air-core magnetics becomes a viable alternative to its cored counterparts, and the size and volume of passive components is considerably reduced. IC design approaches, such as device optimization, on-chip gate driver design and cascoded switch structure, not only reduce the semiconductor device loss, but also address the limitations of narrow voltage range and the difficulties in attaining precise gate drive timing control that are often associated with conventional low-voltage devices. Altogether, these integrated components have served as critical building blocks to enable low-voltage, wide-operating-range, high-bandwidth inverter and synchronous rectifier designs, which have not been previously achievable for converters switching in the VHF regime. It is anticipated that the approaches developed in this thesis will allow further development of low-voltage switching power converters to improve their achievable size, bandwidth and efficiency.

6.1 Thesis summary and key take-aways

Chapter 1 introduces the benefits of increasing switching frequency for dc-dc power converters, and discusses the major limitations that have constrained the operating frequencies of many conventional designs. Major loss mechanisms such as switching loss, gating loss and magnetics loss have set the upper bound on switching speeds to a few megahertz. Various design techniques suitable for VHF operating frequency have been developed in the past decade, however, much of the study thus far has been targeted at medium-to-high volt-
Summary and Conclusions

age (>5V) and medium power (>5W) applications. While certain design considerations are similar, tradeoffs for low-voltage, low-power applications can be quite different. This work addresses the challenges of achieving a high-bandwidth, wide-operating-range VHF converter at low-voltages.

Chapter 2 explores magnetics design tradeoffs and scaling in VHF dc-dc converters, and examines how the physical sizes of magnetic components change by increasing the switching frequency for different design options. Quantitative examples of magnetics scaling are provided and opportunities in further size reduction and performance improvement in VHF magnetics designs are discussed. It is found that while core-loss of inductors constructed with conventional MnZn and NiZn ferrite materials and low-permeability materials imposes a fundamental frequency limit, volume and loss of coreless (air-core) inductors may continuously improve with increased switching frequency. The magnetics analysis suggests that air-core inductors provide a much better tradeoff in terms of size and loss in the VHF regime provided that other semiconductor, topology and architecture limitations are dealt with.

Chapter 3 examines methods to improve upon achievable performance via commercial off-the-shelf semiconductors for use in VHF applications. There are a limited number of commercial MOSFETs with breakdown voltages lower than 20 V, and even the available ones are generally optimized for applications other than resonant power conversion. For example, RF power MOSFETs intended for use in linear power amplifiers are optimized for their linearity, which doesn't correlate to optimal performance in power conversion; And devices designed for hard-switched converters are optimized for reducing switching loss, which is not significant in ZVS resonant converters to begin with. Besides device characteristics, most commercial low-voltage devices are over-packaged resulting in many nano-henries of packaging inductance. This parasitic inductance makes many otherwise viable topologies impractical to implement or significantly deteriorates converter performance when operated at hundreds of MHz. Chapter 3 also explores opportunities in device geometry optimization on a CMOS low-voltage process, gate drive integration, and employment of a cascoded structure while carefully considering packaging issues for high-impact semiconductor advancement for better VHF converters for low-voltage applications.

Chapter 4 explores circuit topologies as a means to leverage the optimized device/gate drive design in the tens to hundreds of MHz operating regime. An inverter topology operating at hundreds of MHz that can dynamically adjust the output power from full power to 1/4
of the full power level is introduced. The inverter topology addresses the narrow-load-range limitations of the conventional class-E inverter designs via the use of four additional components. The fully resonant designs employ small-valued, air-core inductors which translate to small-size, reduced magnetics loss and vastly improved transient response speed. Furthermore, this topology has an inherent gate-width switching capability that further reduces gating loss by half for substantial performance improvements at light load.

VHF power conversion is especially challenging at low voltages due to poor efficiency resulting from rectification loss. For example, only considering the forward voltage drop of the best commercial silicon Schottky diodes alone can set a theoretical maximum rectifier efficiency of 70% for an output voltage of 1V. Chapter 5 treats in detail the design and performance of a dc-dc converter utilizing a synchronous rectifier operating in the VHF regime, which is a major contribution of this thesis, to overcome the substantial losses produced by diode rectifiers at low voltages. In particular, it is a $100\,MHz$ class-E resonant rectifier, which results in a $2.5 \times$ overall converter efficiency improvement compared to its diode counterpart. The culmination of the developed design techniques in passives, semiconductor devices, and circuit topologies throughout this thesis is an experimental prototype of a miniaturized $100\,MHz$, $1.5W$ power converter with synchronous rectification.

### 6.2 Thesis Conclusions

Resonant power conversion has enabled substantial improvements in terms of converter size, efficiency and bandwidth, and provides a viable means to achieve miniaturization and integration, mostly in medium-to-high voltage and power ranges. This thesis work has extended the capabilities of VHF circuits into the low-end of the output voltage spectrum. For example, devices optimized in a CMOS process with reasonably low on-state resistance and small parasitic capacitance have successfully been utilized for VHF power conversion resulting in minimized switching, conduction and gating loss. In addition, cascading two low-voltage devices and utilizing the device's SOA range in soft-switched topologies it has been shown that it is possible to further extend the semiconductor operating voltage range.

Discrete resonant gate drive designs often suffer from poor performance due to the parasitic inductance around the gate loop, making synchronous rectification at hundreds of MHz
Summary and Conclusions

difficult to implement. A two-prong approach including an on-die gate driver design and an exploration of synchronous rectifier topologies that are less sensitive to gate signal timing has led to the development of a practical synchronous rectifier implementation which can operate at hundreds of MHz switching speeds. The rectifier design together with a fully resonant inverter design, which has inherent gate-width switching capabilities, has led to a 100MHz converter that attains high bandwidth and wide operating range while maintaining good efficiencies.

6.3 Future Work

The design approaches and topologies introduced in this thesis open opportunities for further development and research.

A potential area for substantial improvement is adapting the device geometry optimization techniques based upon the findings related to cascoded device in Chapters 4 and 5 resulting in a more optimized cascoded structure. Optimizing the on-die capacitance in a cascoded structure for equal voltage sharing can eliminate additional external capacitors (and hence additional layout and packaging inductance in the semiconductor drain-to-source loop), further reducing the amount of ringing in the converter waveforms and improving the inverter and converter’s overall performance.

In addition, adapting the integrated gate-drive design with additional on-die pulse-skipping capabilities is another area to further increase the converter’s power density. Currently, this pulse-skipping gate drive and control circuitry occupies a significant area in the inverter and converter prototype shown in Chapters 4 and 5 (more so than the power stage itself). This suggests that the converter power density can be vastly increased through a more integrated approach.

The 100MHz synchronous rectifier prototype has also paved the way for topologies that permit bidirectional power flow. Its excellent transient speed suggests that it may be the ideal candidate for applications where the output voltage needs to be slewed with high bandwidth, such as envelope tracking systems. The performance of the demonstrated synchronous rectifier may further be improved via on-die control circuitry designs, ensuring
6.3 Future Work

even more accurate time control and opening the possibilities to other synchronous rectifier topology implementations.

With the advancement in device packaging technologies, the device packaging inductance may further be reduced via flip chip packaging to push the designs for even higher switching frequencies, higher bandwidth and smaller size. Lastly, there is also a significant amount of work that could be done with passives. The small-valued off-the-shelf resonant inductor employed in the prototypes may also be replaced with integrated passive components on the die or within the device package, which will lead to even higher power density and size reduction.
Appendix A

A.1 Magnetics Scaling Code

clear all;

L=100000; %H %16000; %100kHz
pcu=1.7e-6; %copper resistivity: unit ohm*cm
Uc=2000; %permeability 3f3 Material
Uo=4*pi*1e-7;

scaling=4;
Cm=[2.53e-4, 2e-5, 3.6e-9]
alpha=[1.63,1.8,2.4]
beta=[2.45,2.5,2.25]

Iac=10.7 %A
Idc=0

P_max=300; %mw
T_max=40; %75000; %50;
factor=1.5;
B_max=0.3;

AL_norm=100; %nh/turn_squard
n_norm=sqrt(L/AL_norm);
gap_norm=800e-6; %m
Vol_norm=1325*1e-9; %m^3

%for RM7 core
core_length_norm=20.3; %mm
core_h_norm=13.4; %mm
window_h_norm=8.4; %mm
Appendix A

window \( w_{\text{norm}} = \frac{(14.75 - 7.25)}{2} \); \( \text{mm} \)
winding length norm = 14.75; \( \text{mm} \)
mid window \( w_{\text{norm}} = 7.25 \); \( \text{mm} \)

\[
\begin{align*}
\text{AL max gap norm} &= 1000e^{-9}; \\
\text{lg max gap norm} &= 8000e^{-6}; \\
\text{AL no gap norm} &= 25000e^{-9}; \\
\end{align*}
\]

\[
\begin{align*}
\text{eff A norm} &= 44.1 \% \left( \text{AL max gap norm} \times \text{lg max gap norm} / U_0 \right) \times 1e6 \times \text{mm}^{-2} \times 44.1 \\
\text{eff l norm} &= 30 \% \left( U_c \times U_0 \times \text{eff A norm} \times 1e-6 / \text{AL no gap norm} \right) \times 1e3 \times \text{mm}^{-3} \\
\text{eff v norm} &= 1325; \text{mm}^{-3} \\
\end{align*}
\]

\[
\begin{align*}
\text{freq start} &= 100e3; \\
\text{count} &= 1; \\
\text{f min} &= 0.01; \\
\text{f max} &= 1000; \\
\text{num decade} &= \log_{10}(\text{f max}) - \log_{10}(\text{f min}); \\
\text{for i}=1:1: \text{num decade} \\
\text{for j}=1:0.1:9 \\
\text{scaling factor (count)} &= \left( \text{f min} \times 10^{(i-1)} \right) \times j^{(-1/2)}; \\
\text{count} &= \text{count} + 1; \\
\text{end} \\
\text{end} \\
\text{count} &= 1; \\
\text{f min} &= 0.1; \\
\text{f max} &= 100; \\
\text{num decade} &= \log_{10}(\text{f max}) - \log_{10}(\text{f min}); \\
\text{for i}=1:1: \text{num decade} \\
\text{for j}=1:0.1:9 \\
\text{f (count)} &= \text{f min} \times 10^{(i-1)} \times \text{freq start} \times j; \\
\text{count} &= \text{count} + 1; \\
\text{end} \\
\text{end} \\
\text{freq scaling} &= \text{size(f)}; \\
\text{size scaling} &= \text{size(scaling factor)}; \\
\text{for i}=1:1: \text{freq scaling}(2) \\
\text{L scaled (i)} &= \text{freq start} \times \text{L / f(i)}; \text{scale inductance with frequency keep } wL \text{ product constant} \\
\text{end}
\]
A.1 Magnetics Scaling Code

core_length_scaled=scaling_factor.*core_length_norm; %mm
core_h_scaled=scaling_factor.*core_h_norm; %mm
window_h_scaled=scaling_factor.*window_h_norm; %mm
window_w_scaled=scaling_factor.*window_w_norm; %mm
winding_length_scaled=scaling_factor.*winding_length_norm; %mm
mid_window_w_scaled=scaling_factor.*mid_window_w_norm;
vol_scaled=(core_length_scaled.*core_h_scaled).*winding_length_scaled; %mm^3
surface_area_scaled=((winding_length_scaled.*core_h_scaled)*pi)+pi*2*((winding_length_scaled./2).^2); %mm^2
eff_A_scaled=(scaling_factor.^2)*eff_A_norm; %mm^2
eff_l_scaled=scaling_factor.*eff_l_norm; %mm
eff_v_scaled=(scaling_factor.^3)*eff_v_norm; %mm^3
gap_ratio=0:0.001:0.08;
gap_scaling=size(gap_ratio);

for i=1:1:freq_scaling(2)
    for j=1:1:size_scaling(2)
        for z=1:1:gap_scaling(2)
          gaplength(j,z)=efflscaled(j)*gapratio(z); %mm
          Rc(j,z)=gap_length(j,z)*le-3/(Uo*eff_A_scaled(j)*le-6);
          Rg(j,z)=(eff_l_scaled(j)-gap_length(j,z))*le-3/(Uc*Uo*eff_A_scaled(j)*le-6);
          AL_scaled(j,z)=1e9/(Rc(j,z)+Rg(j,z)); %nH/turn^-2
          n(j,i,z)=ceil(sqrt(L-scaled(i)/ALscaled(j,z)));
          if n(j,i,z)<1
              n(j,i,z)=1;
          end
          Bac(j,i,z)=L_scaled(i)*le-9*Iac/(n(j,i,z)*eff_A_scaled(j)*le-6); %T
          % Bac(j,i,z)=(L_scaled(i)*le-9*Iac/(n(j,i,z)*eff_A_scaled(j)*le-6))/2; RMS current %T
          factor1(i)=f(i)^2.4;
          factor2(j,i,z)=Bac(j,i,z)^2.25;
          Pcore_vol(j,i,z)= Cs(3)*factor1(i)*factor2(j,i,z); %mw/cm^3
          Pcore(j,i,z)=Pcore_vol(j,i,z)*eff_v_scaled(j)*le-3; %mw
          wire_d_upper_1(j,i,z)=window_h_scaled(j)*0.5/n(j,i,z); %mm
          wire_d_upper_1(j,i,z)=window_h_scaled(j)/n(j,i,z); %mm
          wire_d_upper_2(j)=window_v_scaled(j)*0.5; %mm
          wire_d(j,i,z)=min( wire_d_upper_1(j,i,z), wire_d_upper_2(j));
          wire_r(j,i,z)=pcu/(pi*(wire_d(j,i,z)*le-3/2)^2)*10*le-3; %mOhm/m*le-3
    end
end

Appendix A

\[ lw(j,i,z) = \pi \left( \text{midwindow}_w \cdot \text{scaled}(j) + \text{wire}_d(j,i,z) \cdot 2 \right) \cdot \text{n}(j,i,z) \] \[ Rdc(j,i,z) = \text{wire}_r(j,i,z) \cdot lw(j,i,z) \cdot 10^{-3} \] \[ \text{skin}(i) = \sqrt{\frac{\text{pcu} \cdot 10^{-2}}{\pi \cdot Uo \cdot f(i)}} \] \[ Rac(j,i,z) = \text{wire}_d(j,i,z) \cdot 10^{-3} / \text{skin}(i) \cdot Rdc(j,i,z) \] \[ Pwire(j,i,z) = (Rdc(j,i,z) \cdot \text{Idc}^2 + 0.5 \cdot \text{Iac}^2 \cdot Rac(j,i,z)) \] \[ Ptotal(j,i,z) = Pcore(j,i,z) + Pwire(j,i,z) \cdot 1000 \] \[ \text{Surface}_A(j) = \text{surface}_a \cdot \text{scaled}(j) \cdot 10^{-2} \] \[ Ttotal(j,i,z) = \frac{Ptotal(j,i,z)}{\text{Surface}_A(j)} \]
p_gap_min_length(i)=gap_scaling(2);
end

for i=1:1:freq_scaling(2)
    for j=1:1:size_scaling(2)
        for z=1:1:gap_scaling(2)
            if (Ptotal(j,i,z)<=P_max && Bac(j,i,z)<=B_max)
                p_index_temp(i)=j;
                p_gap_temp(i)=z;

                if p_index_temp(i)>p_min_size(i)
                    p_min_size(i)=p_index_temp(i);
                    p_gap_min_length(i)=p_gap_temp(i);
                end
            end
        end
    end
end

index=min_size;
p_index=p_min_size;

for i=1:1:freq_scaling(2)
    t_min_size(i)=1;
    t_gap_min_length(i)=gap_scaling(2);
    t_index_temp(i)=-1;
    t_gap_temp(i)=-1;
end

for i=1:1:freq_scaling(2)
    for j=1:1:size_scaling(2)
        for z=1:1:gap_scaling(2)
            if (Ttotal(j,i,z)/factor<=T_max && Bac(j,i,z)<B_max)
                t_index_temp(i)=j;
                t_gap_temp(i)=z;

                if t_index_temp(i)>t_min_size(i)
                    t_min_size(i)=t_index_temp(i);
                    t_gap_min_length(i)=t_gap_temp(i);
                end
            end
        end
    end
end
Appendix A

```
end
end
end
end

end

end

figure (5);
a=loglog(f/1e3,vol_scaled(p_index)*1e-3,'--', f/1e3,vol_scaled(t_index)*1e-3);
axis([10^-1 3*10^3 10^-2 10^-2])
set(a(2), 'Color', [0.399, 0.399, 0.399]);
set(a(1), 'Color', [0.597, 0.199, 0.199])
set(a, 'LineWidth', 4);

ti=xlabel('Operating Frequency [kHz] ');
set(ti, 'FontSize', 14);
set(ti, 'FontWeight', 'bold');
t1=ylabel('Volume [cm^3] ')
set(t1, 'FontSize', 14);
set(t1, 'FontWeight', 'bold');
t1=title('Resonant Cored Inductor Volume vs. Operating Frequency')
set(t1, 'FontSize', 14);
set(t1, 'FontWeight', 'bold');
t2=legend('Q Limited', '\Delta T Limited', 3)
set(t2, 'FontSize', 14);
set(t2, 'FontWeight', 'bold');
grid on
hold

Q=L*1e-9*2*pi*freq_start/(P_max*1e-3/((Iac)^2))

for i=1:1:freq_scaling(2)
    Bac_plot(i)=Bac(p_index(i),i,p_gap_min_length(i));
Pcore_plot(i)=Pcore(p_index(i),i,p_gap_min_length(i)); %mw
Pwire_plot(i)=Pwire(p_index(i),i,p_gap_min_length(i))*1000; %mw
N_plot(i)=ceil(n(p_index(i),i,p_gap_min_length(i)));
gap_plot(i)=gap_length(p_index(i),p_gap_min_length(i));
gap_ratio_plot(i)=gap_plot(i)/eff_l_scaled(p_index(i));
```

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A.1 Magnetics Scaling Code

end

figure(1);
a=loglog(f/1e3,Bac_plot);
axis([10^1 3.5*10^3 10^-5 10^0])
set(a(1),'Color',[0.597,0.199,0.199])
set(a,'Linewidth',4);

t1=xlabel('Operating Frequency [kHz] ')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t1=ylabel('Bac');
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t1=title('Bac vs. Frequency')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t2=legend('Core Loss','Winding Loss',4)
set(t2,'FontSize',8);
set(t2,'FontWeight','bold');

figure(2);
a=loglog(f/1e3,Pcore_plot,'--',f/1e3,Pwire_plot);
axis([10^1 3.5*10^3 10^-2 10^3])
set(a(2),'Color',[0.399,0.399,0.399])
set(a(1),'Color',[0.597,0.199,0.199])
set(a,'Linewidth',4);

t1=xlabel('Operating Frequency [kHz] ')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t1=ylabel('Loss [mW]')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t1=title('Loss vs. Frequency')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t2=legend('Core Loss','Winding Loss',4)
set(t2,'FontSize',8);
set(t2,'FontWeight','bold');

figure(3);
Appendix A

\[ a = \log_{\log}(f/1e3, N_{\text{plot}}) \]
\[ \text{axis([10^{-1} 3.5*10^{-3} 10^{-2} (0) 10^{-2}])} \]
\[ \text{set(a(1),'Color', [0.597, 0.199, 0.199])} \]
\[ \text{set(a,'Linewidth',4);} \]
\[ \text{tl=xlabel('Operating Frequency [kHz] ')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]
\[ \text{tl=ylabel('# of Turns')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]
\[ \text{tl=title('N vs. Frequency')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]

\[ \text{figure(4);} \]
\[ a = \log_{\log}(f/1e3, g_{\text{plot}}) \]
\[ \text{axis([10^{-1} 3.5*10^{-3} 10^{-2} (0) 10^{-2}])} \]
\[ \text{set(a(1),'Color', [0.597, 0.199, 0.199])} \]
\[ \text{set(a,'Linewidth',4);} \]
\[ \text{tl=xlabel('Operating Frequency [kHz] ')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]
\[ \text{tl=ylabel('Gap Length [mm]')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]
\[ \text{tl=title('Gap Length vs. Frequency')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]

\[ \text{figure(6);} \]
\[ a = \log_{\log}(f/1e3, g_{\text{ratio}_{\text{plot}}}) \]
\[ \text{set(a(1),'Color', [0.597, 0.199, 0.199])} \]
\[ \text{set(a,'Linewidth',4);} \]
\[ \text{tl=xlabel('Operating Frequency [kHz] ')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]
\[ \text{tl=ylabel('Gap Length [mm]')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]
\[ \text{tl=title('Gap Length Ratio vs. Frequency')} \]
\[ \text{set(tl,'FontSize',12);} \]
\[ \text{set(tl,'FontWeight','bold');} \]

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A.1 Magnetics Scaling Code

figure(7);
grid on;
a=loglog(f/1e3,pcore_plot)
set(a(1),'Color',[0.597,0.199,0.199])
set(a,'Linewidth',4);
axis([10^-1 3.5*10^-3 10^-2 10^-3])

hold
[AX,H1,H2]=plotyy(f/e3,pwire_plot,f/1e3,bac_plot,@loglog);
axis(AX(1),[10^-1 3.5*10^-3 10^-(-2) 10^-3])
axis(AX(2),[10^-1 3.5*10^-3 10^-(-5) 10^-0])
t1=title('Loss and Flux Density vs. Frequency');
set(t1,'FontSize',14);
set(t1,'FontWeight','bold');

t2=xlabel('Operating Frequency [kHz] ');
set(t2,'FontSize',14);
set(t2,'FontWeight','bold');

H=[H1 H2];
set(get(AX(1),'Ylabel'),'String','Loss [mW] ');
set(get(AX(1),'Ylabel'),'FontSize',14);
set(get(AX(1),'Ylabel'),'FontWeight','bold');
set(AX(1),'YColor',[0.597,0.199,0.199]);
set(get(AX(2),'Ylabel'),'String','Bac [T] ');
set(get(AX(2),'Ylabel'),'FontSize',14);
set(get(AX(2),'Ylabel'),'FontWeight','bold');
set(AX(2),'YColor',[0.399,0.399,0.399]);
t2=legend('Core Loss','Winding Loss','Flux Density',4)
set(t2,'FontSize',8);
set(t2,'FontWeight','bold');

grid on;
Appendix A

clear all;

% P material inductor volume scale
f=[20, 30, 40, 50, 60]*1e6;
freq_scaling=size(f);
pcu=1.7e-6; % copper resistivity: unit ohm*cm
Uc=4; % permeability -17 Material
Uo=4*pi*1e-7;

k=[3.57e-2, 4.91e-2, 2.18e-1, 6.96e-1, 1.34];
beta=[2.29, 2.33, 2.18, 2.09, 2.04];

beta=(2.29+2.33+2.18+2.09+2.04)/5;

ur=40
core_nom=[2*ur*2.54*0.025*log(0.05/0.025), 1.27, 0.64, 0.64, 0.3, 0.0019, 0.0006] % P

Iac=1;
Idc=0;
Wire_size=-1;
Wire_index=1;

P_max=300; % P
T_max=40; % P

count=1;
fmin=0.0001;
fmax=10000;
num_decade=log10(fmax)-log10(fmin);
for i=1:1:num_decade
    for j=1:0.01:9
        scaling_factor(count)=(fmin*(10^((i-1))*j)^(-1/2);
        core(count,1)=core_nom(1)*scaling_factor(count);
        core(count,2)=core_nom(2)*scaling_factor(count);
        core(count,3)=core_nom(3)*scaling_factor(count);
        core(count,4)=core_nom(4)*scaling_factor(count);
        core(count,5)=core_nom(5)*(scaling_factor(count)^2);
        core(count,6)=core_nom(6)*(scaling_factor(count)^3);
        count=count+1;
    end
end
A.1 Magnetics Scaling Code

```matlab
end
end

k=[3.57e-2,4.91e-2,2.18e-1,6.96e-1,1.34];
f=[20,30,40,50,60];

order=8
[P,S]=polyfit(f,k,order)
kfit=polyval(P,f)

freq_start2=20e6;
count2=1

fmin2=1;
Fmax2=10;
num_decade2=log10(fmax2)-log10(fmin2);
for i=1:1:num_decade2
    for j=1:0.01:9
        f2(count2)=fmin2*(10^((i-1)))*freq_start2*j;
        L_scaled(count2)=10000*1e6/f2(count2);
        k2(count2)=0;
        for q=1:1:order
            k2(count2)=P(q)*((f2(count2)/le6)^(order-q+1))+k2(count2);
        end
        count2=count2+1;
    end
end

freq_scaling=size(f2);

L_nom=L_scaled(1);
f2_nom=f2(1);
k2_nom=k2(1);
n_nom=ceil(sqrt(L_nom/core-nom(1)));

wire_d=min(core_nom(3)*pi/n_nom,core_nom(3)*pi/(n_nom*pi)); %mm
wire_r=pcu/(pi*(wire_d*1e-3/2)^2)*10*1e-3; %mOmega/m*1e3

lw_nom=(2*core_nom(4)+2*(core_nom(2)-core_nom(3)))/2*n_nom*pi*core_nom(2);
Hdc_nom=wire_r*lw_nom*1e-3; %ohm
skin_nom=sqrt(pcu*1e-2/(pi*Uo*f2_nom));
```
Appendix A

\[
R_{ac, nom} = \text{wire}_d \times 1e^{-3} / \text{skin} \times R_{dc, nom}; \ \%\text{ohm}
\]

\[
\text{size}_\text{scaling} = \text{size}(\text{scaling}_\text{factor});
\]

\[
B_{ac, nom} = L_{\text{nom}} \times 1e^{-9} \times I_{ac} / (n_{\text{nom}} \times \text{core}(4) \times 1e^{-3} \times \text{core}(2) \times 1e^{-3} - \text{core}(3) \times 1e^{-3} / 2) \times 10000;
\]

\[
P_{\text{core}_\text{vol}, nom} = k_2_{\text{nom}} \times (B_{ac, nom} / \beta);
\]

\[
P_{wire, nom} = (R_{dc, nom} \times \text{Idc}^2 + 0.5 \times I_{ac}^2 \times R_{ac, nom}); \ \%\text{100kHz}
\]

\[
\text{Vol}_\text{scaled, nom} = \text{core}(4) \times \pi / 4 \times ((\text{core}(2) - ((\text{core}(3) / 2))) \times 1e^{-3}; \ \%\text{cm}^3
\]

\[
\text{Surface}_\text{A, nom} = (\pi \times (\text{core}(2) \times \text{core}(4) + \text{core}(3) \times \text{core}(4)) + 2 \pi / 4 \times (\text{core}(2) \times \text{core}(2) - \text{core}(3) \times \pi / 2) \times 1e^{-3}; \ \%\text{cm}^3
\]

\[
P_{\text{core, nom}} = \text{Vol}_\text{scaled, nom} \times P_{\text{core}_\text{vol, nom}}; \ %\text{mw}
\]

\[
P_{total, nom} = P_{\text{core, nom}} + P_{\text{wire, nom}};
\]

\[
T_{total, nom} = (P_{\text{total, nom}} / \text{Surface}_\text{A, nom})^{(0.833)};
\]

\[
\text{for } i = 1:1:\text{freq}_\text{scaling}(2)
\]

\[
\text{for } j = 1:1:\text{size}_\text{scaling}(2)
\]

\[
\text{n}(j, i) = \sqrt{L_{\text{scaled}}(i) / \text{core}(j, 1)};
\]

\[
\text{if } (\text{n}(j, i) < 1)
\]

\[
\text{n}(j, i) = 1;
\]

\[
\text{end}
\]

\[
\text{wire}_d(j, i) = \min(\text{core}(j, 3) \times \pi / \text{n}(j, i), \text{core}(j, 3) \times \pi / (\text{n}(j, i) + \pi)); \ \%\text{mm}
\]

\[
\text{wire}_r(j, i) = \text{pcu} / (\pi \times (\text{wire}_d(j, i) \times 1e^{-3} / 2)^2) \times 10 \times 1e^{-3}; \ \%\text{mOhm/mm} \times 1e^{-3}
\]

\[
\text{lw}(j, i) = (2 \times \text{core}(j, 4) + 2 \times (\text{core}(j, 2) - \text{core}(j, 3) / 2)) \times \text{n}(j, i) + \pi \times \text{core}(j, 2);
\]

\[
R_{dc}(j, i) = \text{wire}_r(j, i) \times \text{lw}(j, i) \times 1e^{-3}; \ \%\text{ohm}
\]

\[
\text{skin}(i) = \sqrt{\text{pcu} \times 1e^{-2} / (\pi \times U_{o} \times f_2(i))};
\]

\[
R_{ac}(j, i) = \text{wire}_d(j, i) \times 1e^{-3} / \text{skin}(i) \times R_{dc}(j, i); \ \%\text{ohm}
\]

\[
B_{ac}(j, i) = L_{\text{scaled}}(i) \times 1e^{-9} \times I_{ac} / (n(j, i) \times \text{core}(j, 4) \times 1e^{-3} \times (\text{core}(j, 2) \times 1e^{-3} - \text{core}(j, 3) \times 1e^{-3}) / 2) \times 10000; \ \%\text{gauss}
\]

\[
P_{\text{core}_\text{vol}(j, i)} = k_2(i) \times (B_{ac}(j, i) / \beta); \ %\text{mw/cm}^3
\]

\[
P_{\text{wire}(j, i)} = (R_{dc}(j) \times \text{Idc}^2 + 2 \times I_{ac}^2 \times R_{ac}(j, i)); \ %\text{w}
\]

\[
\text{Vol}_\text{scaled}(j) = \text{core}(j, 2) \times 1e^{-3} \times \text{core}(j, 4); \ %\text{cm}^3 \text{ box volume}
\]

\[
\%\text{total core vol core}(j, 4) \times \pi / 4 \times ((\text{core}(j, 2) - ((\text{core}(j, 3) / 2))) \times 1e^{-3}; \ %\text{cm}^3
\]

\[
\%\text{Surface}_\text{A}(j) = \text{core}(j, 5);
\]

\[
P_{\text{core}(j, i)} = \text{Vol}_\text{scaled}(j) \times P_{\text{core}_\text{vol}(j, i)}; \ %\text{mw}
\]
A.1 Magnetics Scaling Code

\[ P_{\text{total}}(j,i) = P_{\text{core}}(j,i) + P_{\text{wire}}(j,i) \times 1000; \text{mW} \]

\[ \text{Surface}_A(j) = \pi \times (\text{core}(j,2) \times \text{core}(j,3) + \text{core}(j,4))^2 + 2 \times \pi / 4 \times (\text{core}(j,2) \times \text{core}(j,3) \times \text{core}(j,3))^2 \times 10^{-2}; \text{not cou} \]

\[ T_{\text{total}}(j,i) = (P_{\text{total}}(j,i)/(\text{factor} \times \text{Surface}_A(j))) \; \text{; see program Rth.m} \]

\[ \text{max\_scaling\_factor}(i) = L_{\text{scaled}}(i) / (2 \times \text{ur} \times 2.54 \times 0.025 \times \log(0.05/0.025)); \]

\[ \text{max\_Vol\_scaled}(i) = \text{core\_nom}(4) \times L_{\text{scaled}}(i) / (\pi / 4 \times (\text{core\_nom}(2) \times \text{max\_scaling\_factor}(i))^2 - ((\text{core}_3)^2)); \]

for \( i = 1:1:\text{freq\_scaling}(2) \)

\[ P_{\text{constant}}(i) = -1; \]

\[ P_{\text{index}}(i) = 1; \]

end

for \( i = 1:1:\text{freq\_scaling}(2) \)

for \( j = 1:1:\text{size\_scaling}(2) \)

if \( P_{\text{total}}(j,i) \leq P_{\text{max}} \)

\[ P_{\text{temp}}(i) = P_{\text{total}}(j,i); \]

\[ P_{\text{index\_temp}}(i) = j; \]

if \( P_{\text{temp}}(i) > P_{\text{constant}}(i) \)

\[ P_{\text{constant}}(i) = P_{\text{temp}}(i); \]

\[ P_{\text{index}}(i) = P_{\text{index\_temp}}(i); \]

end

end

end

for \( i = 1:1:\text{freq\_scaling}(2) \)

\[ T_{\text{constant}}(i) = -1; \]

\[ T_{\text{index}}(i) = 1; \]

end

for \( i = 1:1:\text{freq\_scaling}(2) \)

for \( j = 1:1:\text{size\_scaling}(2) \)
Appendix A

if \( T_{\text{total}}(j,i) \leq T_{\text{max}} \)
    \( T_{\text{temp}}(i) = P_{\text{total}}(j,i) \);
    \( T_{\text{index temp}}(i) = j \);
    if \( T_{\text{temp}}(i) > T_{\text{constant}}(i) \)
        \( T_{\text{constant}}(i) = T_{\text{temp}}(i) \);
        \( T_{\text{index}}(i) = T_{\text{index temp}}(i) \);
    end
end
end

for \( i = 1:1:freq\_scaling(2) \)
    \( \text{index}(i) = \min(P_{\text{index}}(i), T_{\text{index}}(i)) \);
end

\[
a = \loglog(f2/1e3, \text{Vol\_scaled}(P_{\text{index}}), '-' , f2/1e3, \text{Vol\_scaled}(T_{\text{index}}), '-' )
\]
axis([10^1 4*10^-1 10^-2])
set(a(1), 'Color', [0.597, 0.199, 0.199]);
set(a(2), 'Color', [0.399, 0.399, 0.399]);
set(a(3), 'Color', [0.597, 0.199, 0.199]);
set(a, 'Linewidth', 4);

\( t1 = \text{xlabel('Operating Frequency [MHz] ')} \)
set(t1, 'FontSize', 20);
set(t1, 'FontWeight', 'bold');
\( t1 = \text{ylabel('Volume [cm^3]')} \)
set(t1, 'FontSize', 20);
set(t1, 'FontWeight', 'bold');
\( t1 = \text{title('Resonant Cored Inductor Volume vs. Operating Frequency')} \)
set(t1, 'FontSize', 20);
set(t1, 'FontWeight', 'bold');
\( t2 = \text{legend('Q Limited','\Delta T Limited',2)} \)
set(t2, 'FontSize', 16);
set(t2, 'FontWeight', 'bold');
grid on
hold

\[
Q = L_{\text{scaled}}(i) * 1e-9 * 2 * \pi * f2(i) / (P_{\text{max}} * 1e-3 / ((I_{\text{ac}})^2))
\]
clear all;

L_nom=10e-6; %10000nh at 1MHz
D_nom=1e-2; %m
Iac=1;
P_max=0.3;
T_max=40; %75;

freq_start=1e6;
count=1;

fmin=0.001;
fmax=100;
num_decade=log10(fmax)-log10(fmin);
%frequency scaling matrix
for i=1:1:num_decade
    for j=1:0.1:9
        f(count)=fmin*(10^-(i-1))*freq_start*j;
        count=count+1;
    end
end

fmin=0.000001;
fmax=10000;
num_decade=log10(fmax)-log10(fmin);
%scaling factor
for i=1:1:num_decade
    for j=1:0.1:9
        scaling_factor(count)=(fmin*(10^-(i-1))*j)^(-1/6);
        count=count+1;
    end
end

freq_scaling=size(f);
scale_scaling=size(scaling_factor);

D=scaling_factor.*D_nom;
L=5*D;

Si=0.88; %0.96*tanh(0.86*sqrt(5))

for i=1:1:freq_scaling(2)
for j=1:size_scaling(2)
Q(j,i)=7.5*D(j)*Si*sqrt(f(i));
Rac(j,i)=freq_start*2*pi*L_nom/Q(j,i);
Ptotal(j,i)=Rac(j,i)*(Iac^2)/2;
Surface_area(j)=10/2*pi*(D(j)^2)*1e4; %cm^2
Ttotal(j,i)=Ptotal(j,i)*1000/(1.5*Surface_area(j));
Vol(j)=D(j)*D(j)*5*D(j)*1e6; %5/4*pi*(D(j)^3)*1e6; %cm^3
end
end
for i=1:freq_scaling(2)
P_constant(i)=-1;
P_index(i)=1;
end
for i=1:freq_scaling(2)
   for j=1:size_scaling(2)
      if Ptotal(j,i)<=P_max
         P_temp(i)=Ptotal(j,i);
P_index_temp(i)=j;
      end
      if P_temp(i)>P_constant(i)
         P_constant(i)=P_temp(i);
P_index(i)=P_index_temp(i);
      end
   end
end
for i=1:freq_scaling(2)
   T_constant(i)=-1;
   T_index(i)=1;
end
for i=1:freq_scaling(2)
   for j=1:size_scaling(2)
      if Ttotal(j,i)<=T_max
         T_temp(i)=Ptotal(j,i);
         T_index_temp(i)=j;
      end
      if T_temp(i)>T_constant(i)
         T_constant(i)=T_temp(i);
         T_index(i)=T_index_temp(i);
      end
   end
end
if T_temp(i)>T_constant(i)
    T_constant(i)=T_temp(i);
    T_index(i)=T_index_temp(i);
end
end
end

for i=1:1:freq_scaling(2)
    index(i)=min(P_index(i), T_index(i));
end

figure(5);
a=loglog(f/1e3,Vol(index))
axis([10^-1 10^5 10^-2 10^5])
set(a(1),'Color',[0.597,0.199,0.199]);
set(a,'Linewidth',4);
t1=xlabel('Operating Frequency [kHz] ')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t1=ylabel('Volume [cm^3] ')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t1=title('Resonant Air-Core Inductor Volume vs. Operating Frequency')
set(t1,'FontSize',12);
set(t1,'FontWeight','bold');
t2=legend('Air Core',2)
set(t2,'FontSize',12);
set(t2,'FontWeight','bold');
grid on
Appendix B

B.1 Inverter Boards and Schematics

Figure B.1: Parallel/Series reconfigurable inverter board - top copper layer
Appendix B

Figure B.2: Parallel/Series reconfigurable inverter board - layer-2 copper

Figure B.3: Parallel/Series reconfigurable inverter board - layer-3 copper
Figure B.4: Parallel/series reconfigurable inverter board - bottom copper layer
Figure B.5: Parallel/Series reconfigurable inverter board - schematic
B.1 Inverter Boards and Schematics

Figure B.6: 100MHz Parallel/Series reconfigurable inverter

Figure B.7: 100MHz Parallel/Series reconfigurable inverter, effect of $C_3$
Figure B.8: 100MHz Parallel/Series reconfigurable inverter, effect of $C_{EX}$ on equal voltage sharing

Figure B.9: 100MHz Parallel/Series reconfigurable inverter, no additional capacitance across top device in the cascoded structure
Figure B.10: 100MHz Parallel/Series reconfigurable inverter, effect of parasitics
Figure B.11: 100MHz Parallel/Series reconfigurable inverter, effect of parasitics part 2
C.1 Converter Boards and Schematics

Figure C.1: Parallel/Series reconfigurable converter with synchronous rectifier board - top copper layer
Figure C.2: Parallel/Series reconfigurable converter with synchronous rectifier board - layer-2 copper
Figure C.3: Parallel/Series reconfigurable converter with synchronous rectifier board - layer-3 copper
Figure C.4: Parallel/series reconfigurable converter with synchronous rectifier board - bottom copper layer
Figure C.5: Parallel/Series reconfigurable inverter board - schematic
Figure C.6: Conventional class-E rectifier.

Figure C.7: A fully resonant class-E rectifier.
Appendix B

Figure C.8: A fully resonant class-E synchronous rectifier.

Figure C.9: In fully resonant class-E synchronous rectifier, there is a tradeoff between duty ratio and peak device voltage.
Figure C.10: 100MHz Parallel/Series reconfigurable converter with synchronous rectifier.
Figure C.11: 100MHz Parallel/Series reconfigurable converter with synchronous rectifier. The rectifier is somewhat insensitive to the time delay of its gate drive voltage.
Figure C.12: 100MHz Parallel/Series reconfigurable converter with synchronous rectifier with packaging and layout parasitics.
Appendix D

Appendix B

D.1 Converter Boards and Schematics

Figure D.1: Parallel/Series reconfigurable converter with synchronous rectifier board - top copper layer
Figure D.2: Parallel/Series reconfigurable converter with synchronous rectifier board - layer-2 copper
Figure D.3: Parallel/Series reconfigurable converter with synchronous rectifier board - layer-3 copper
Figure D.4: Parallel/Series reconfigurable converter with synchronous rectifier board - bottom copper layer
Figure D.5: Parallel/Series reconfigurable inverter board - schematic
Figure D.6: Conventional class-E rectifier.

Figure D.7: A fully resonant class-E rectifier.
Figure D.8: A fully resonant class-E synchronous rectifier.

Figure D.9: In fully resonant class-E synchronous rectifier, there is a tradeoff between duty ratio and peak device voltage.
Figure D.10: 100MHz Parallel/Series reconfigurable converter with synchronous rectifier.
Figure D.1: 100MHz Parallel/Series reconfigurable converter with synchronous rectifier. The rectifier is somewhat insensitive to the time delay of its gate drive voltage.
Figure D.12: 100MHz Parallel/Series reconfigurable converter with synchronous rectifier with packaging and layout parasitics.


BIBLIOGRAPHY


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