A Merged Two-Stage Power Conversion Architecture with Switched Capacitor Circuit for an LED Driver Module

by

Seungbum Lim

B.S., Electrical Engineering
Seoul National University (2010)

Submitted to the Department of Electrical Engineering
in partial fulfillment of the requirements for the degree of

Master of Science in Computer Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2012

Author .....
Department of Electrical Engineering
May 23, 2012

Certified by .....
David J. Perreault
Professor
Thesis Supervisor

Accepted by .....
Leslie A. Kolodziejski
Chair, Department Committee on Graduate Students

A Merged Two-Stage Power Conversion Architecture with Switched Capacitor Circuit for an LED Driver Module

by

Seungbum Lim

Submitted to the Department of Electrical Engineering
on May 23, 2012, in partial fulfillment of the
requirements for the degree of
Master of Science in Computer Science and Engineering

Abstract

In a power converter specified to convert from wide-range and high-level DC voltage or AC line voltage to low-level DC voltage, satisfying high efficiency, high power density, and high power factor is challenging because of the higher device stress and difficulty of maintaining ZVS/ZCS conditions. Our purpose of the proposed two-stage power conversion architecture is to manage this high peak voltage stress and widely-varying operating conditions and to reduce dissipation by placing a switched capacitor pre-regulator stage in front of a very high frequency DC-DC converter stage. Our proposed two-stage architecture has been designed, built, and tested.

Thesis Supervisor: David J. Perreault
Title: Professor

Acknowledgments

I would like to deeply thank my advisors, Professor David J. Perreault. His technological knowledge and constant encouragement have allowed me to complete my research successfully. Not only in technical point of view but also in many other aspects, studying under him is very fortunate and makes me happy. His tremendous passion makes me focus on research and I am very appreciate to work with him.

And I also want to thank my lab mates who are always willing to answer and help my questions about PCB layout, circuit design, measurement setup and just about anything else. I truly appreciate to John, Wei, Jackie, Alex, Minjie, Wardah, Samantha, Tony, Dave G., Robert, Brandon, Justin, Nate, and Kesavan. Thanks a lot. You guys gave me a lot of energy to move forward.

I also appreciate my friends who made my days rich and fun: Jinhyuck, Chaiwoo, Doyeon, Sunghyuk, Jinhong, Taesoo, Donghun, Youngwoo, Sangtae and others.

Lastly, I would also like to thank my parents who have always been behind me throughout my entire life. I dedicate my thesis to them.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Many modern electrical applications demand high efficiency and fast transient response along with small size and low cost. To achieve high power density, high switching frequency converters are desirable to reduce the numerical values of passive components, including transformers, inductors, and capacitors. Furthermore, greatly increased frequency enables reduction in energy storage and volume of the passive components that limit achievable transient response and account for the majority of converter size and cost. To keep high efficiency at high switching frequency, a number of approaches based on resonant topologies operating under zero-voltage switching (ZVS) and zero-current switching (ZCS) have been proposed and used. Many ZVS and ZCS high efficiency topologies, however, demand higher device voltage stress and higher device count. There is thus a need for better conversion topologies suited for higher frequency and higher efficiency with smaller number of components operating under reduced stress.

In converters specified to convert from wide-range and high-level DC voltage or AC line voltage to low-level DC voltage, satisfying all the constraints is even more challenging because of the higher device stress and the difficulty of maintaining ZVS/ZCS conditions. In addition, if we use AC line voltage, high power factor over 90% is mandatory to make full use of the AC line voltage (e.g., for meeting EnergyStar requirements). A design converting AC wide-range input line voltage to DC low-level output voltage with only one stage typically results in highly-sensitive control, large

size, poor power density, and poor average efficiency. This thesis proposes a two-stage architecture to manage a high peak voltage stress and widely-varying operating conditions coming from the large, wide-ranging input, and to enable reduced dissipation. This is achieved by placing a variable-conversion-ratio switched capacitor pre-regulator stage in front of a very high frequency DC-DC regulation stage.

To build superior power converters, developments in power switch devices are valuable. The requirements of a better power switch include high blocking voltage, low output capacitance, low on-state resistance, low gate AC resistance, low gate-source input capacitance, ease of turn-on and turn-off control, and small volume. The emerging GaN power switch device, expected to meet the requirements above, will enable many improved circuit topologies and open the way to higher-frequency power converters. High quality-factor inductors are also essential in that efficiency is closely related to the loss dissipated in the inductor. Moreover, obtaining a high quality-factor inductor at small size is difficult; thus, micro-fabricated custom inductors developed for high performance at high frequencies will be used. Our two stage architecture will fully utilize the capability of GaN transistors and micro-fabricated inductors and high performance at small size is expected.

The importance of high efficiency lighting has come into the spotlight recently with continuous development of efficient LED(Light Emitting Diode) lighting devices. The LED driver circuit to drive LED lights is the main application of the proposed two stage architecture explored in this thesis, though it has a very wide application range. In this LED driver circuit, AC input line voltage or wide-range DC input voltage is transformed to power a 30-40V DC LED string at 25-30W average power. In this work, the proposed two stage architecture will be simulated, built, and measured for the LED driver circuit. This architecture can be easily applied to not only this LED driver circuit but also a variety of other electrical applications which have wide-swinging high-value input voltage and require high performance at high frequency.

1.1 Figures of Merit for Power Converter

To evaluate various power converters, figures of merit to compare many circuits needs to be defined. In a power conversion circuit, key parameters are efficiency, operating frequency, and power factor at a certain power range.

First of all, efficiency is defined as average output power divided by average input power, and high efficiency is beneficial not only for delivering power effectively but also keeping the temperature acceptable because the dissipation heats the whole circuit, and heat removal incurs size and cost penalties. Therefore, poor efficiency circuit usually require large volume of heat sink to cool down this dissipation.

Second, the frequency is an easy way to estimate the volume of a power converter. As the switching frequency goes up, the discrete components only have to filter out higher frequency and can be designed with smaller value. Low-value discrete component in turn provide lower volume, higher power density and fast transient characteristic.

Lastly, power factor is another important factor we should consider when a converter works as an AC to DC converter. High power factor is necessary to transfer power effectively without sloshing current back and forth. In an LED driver circuit, especially, high power factor above 0.9 is mandatory to meet EnergyStar requirements.

1.2 Commercial LED Driver Module

Recently, many companies have made LED driver modules for LED lamps connected to the AC line voltage. To evaluate the state of the art, we tested some commercial LED driver circuits ranging from 6-24W and measured the input and output voltage/current waveforms as shown in several examples in figure 1-1, figure 1-2, and figure 1-3. Then, three of these LED driver modules are categorized as shown in in table 1.1. Up to the present, commercial driver circuits operate at or below 100kHz and result in one or more of low power density, poor power factor, or poor efficiency. Therefore, we are proposing our new two-stage architecture to meet high efficiency, high power factor, and high power density at the same time.

Commercial LED Light Evaluation			
Paramater	6 W, 3 LEDs	9 W, 3 LEDs	12.5 W, 18 LEDs
Input Current [mA]	45.79	54.45	137.1
Input Power [W]	5.139	3.733	12.468
Output Voltage [V]	8.911	9.157	50.403
Output Current [mA]	437.07	322.28	205.30
Output Power [W]	3.499	2.915	10.35
Power Factor	0.9596	0.5875	0.776
Efficiency [%]	68.08	78.08	82.99
Switch Frequency [kHz]	92.08	42.3	103.6

Table 1.1: commercial LED light evaluation.

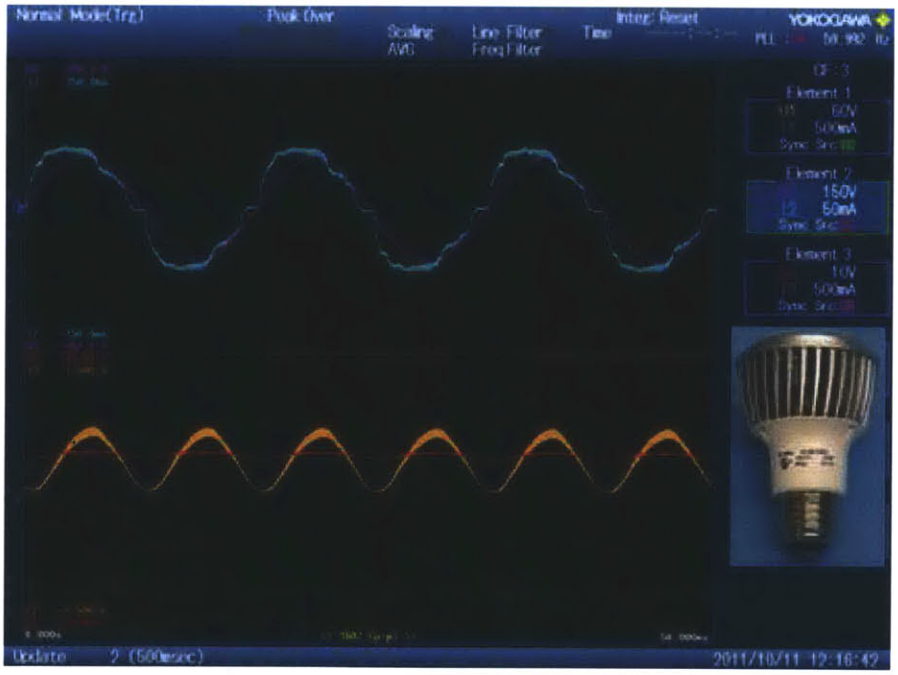


Figure 1-1: 6W, 3 LED input output voltage/current waveform.

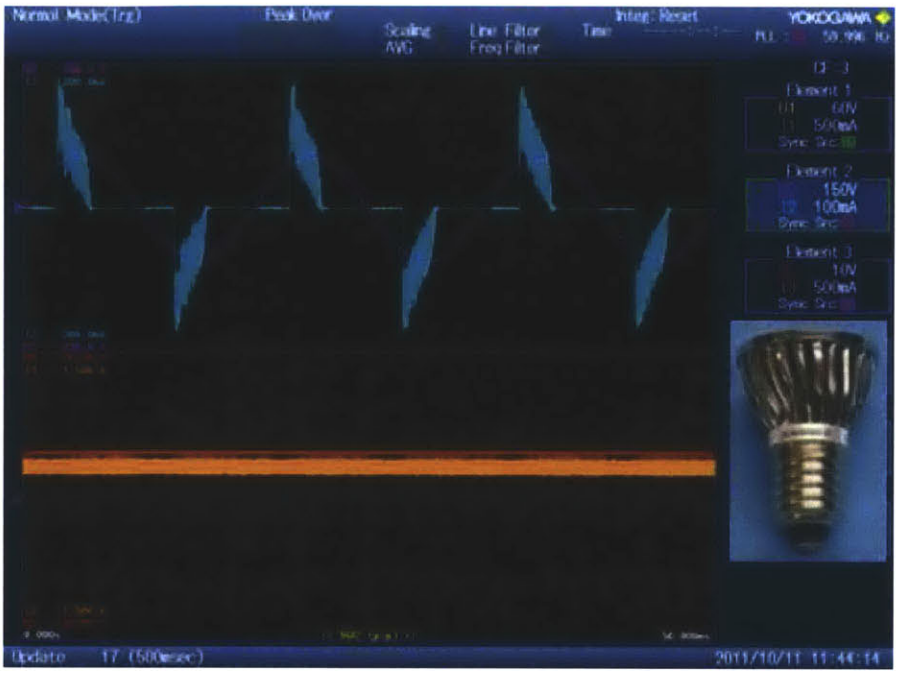


Figure 1-2: 9W, 3 LED input output voltage/current waveform.

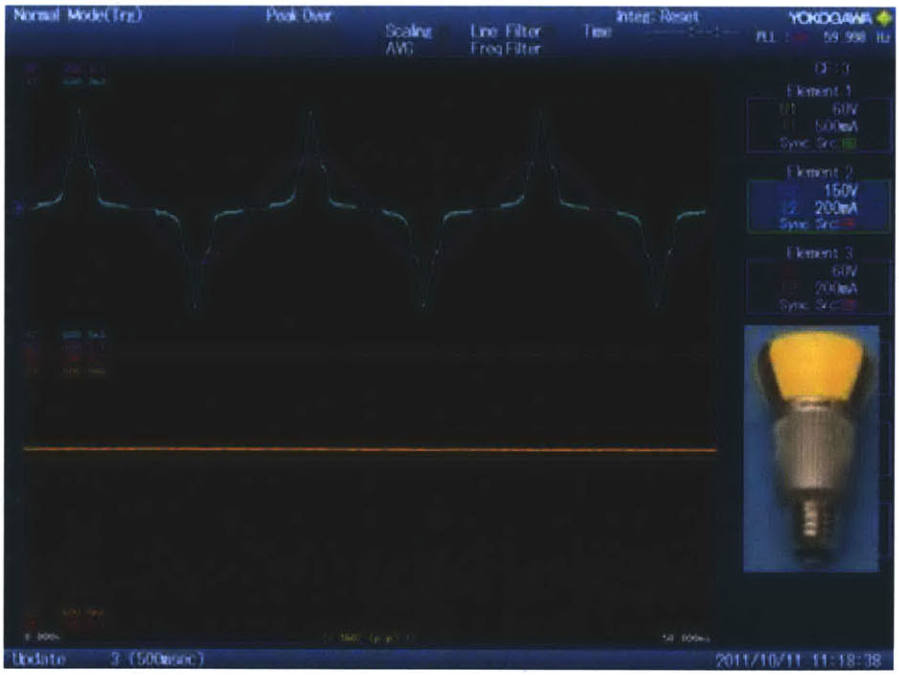


Figure 1-3: 12.5W, 18 LED input output voltage/current waveform.

Chapter 2

Two-Stage Architecture

To achieve high performance in a miniaturized design, a two stage architecture, placing a pre-regulator stage in front of a regulation stage, has been proposed as shown in figure 2-1. This kind of architecture has been used in low-voltage CMOS power converters[1][2], but we employ it here in new ways for grid-scale voltage. In our AC line interfaced LED driver circuit application, the line input AC voltage (e.g. 0-170V, 60Hz) has to be converted to a DC voltage(e.g. between 30-40V), the LED driving voltage. Also in wide-range DC application, a wide range input voltage (e.g., 25-200V) should likewise be regulated to the same LED DC string voltage. When a usual ZVS/ZCS converter is connected directly to rectified AC line voltage from full-bridge rectifier, it typically needs large number of high voltage/current rating passive components and high voltage/current rating active devices and shows low efficiency. This difficulty comes from 120Hz rectified sinusoidal voltage swinging over wide range (e.g. 0-170V). Similar problem happens too when we make DC-DC converter converting from high voltage to small voltage and delivering medium power because the large input voltage makes a converter require a large value and size of inductor. (The size of capacitors tend to be much smaller, and in fact at high voltage, low power one sometimes ends up with numerically small capacitor values that are difficult to work with in the face of parasitics.) the two-stage architecture mitigate these challenges.

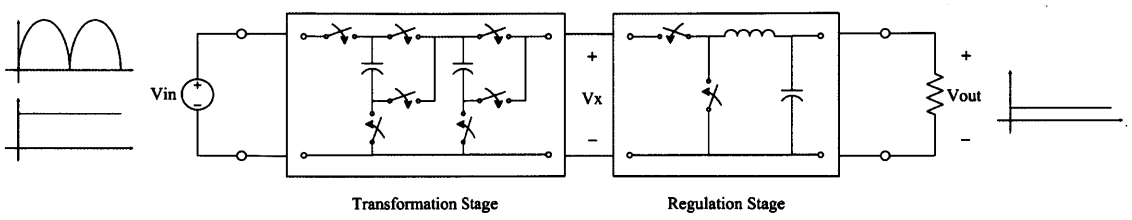


Figure 2-1: illustrative drawing of two stage architecture.

2.1 Two-Stage Architecture Behavior

To address this challenge, an additional stage, a switched capacitor DC-DC circuit, is placed before a VHF regulation stage. The purpose of this architecture is separating the transformation function and regulation function of a converter to relieve the burden on the VHF circuit, which must otherwise achieve both high-ratio stepping down from the large input voltage to low output voltage and regulating this output voltage at the same time.

The switched capacitor stage, only focusing on voltage transformation, can be designed with capacitors and switches. This first stage, thus, can be designed with high power density because it does not require inductors. Because this switched capacitor circuit only uses capacitors and switches and the required capacitors provide high energy power density, the size of switched capacitor circuit can be made small even at relatively low operating frequencies. Moreover "merged" or "soft-charged" operation of the first stage through interactions with the high frequency second stage enables further size and loss reduction(e.g described in section 3.3). In addition, since the efficiency of this first stage degrades without many benefits at high frequency, we turn modulate this first stage at switching frequencies in the 30-100kHz range. The only benefit of increasing the switching frequency of switched capacitor circuit is decreasing the voltage ripple at the output of the switched capacitor circuit which will be consequently regulated by VHF regulation second stage; thus, as long as the VHF stage can stand the voltage ripple of the switched capacitor circuit output node, the frequency of the switched capacitor circuit can be scaled down.

Switched capacitor circuits are excellent for transforming voltages, but have several issues. First, the input current to output current ratios should be related as rational number determined by topology and/or operating mode. This then constrains the output voltage to input voltage conversion ratio to be the same ratio if high efficiency is to be maintained. Second, regulation of the output voltage is difficult with switched capacitor circuit and is lossy insofar as the voltage conversion ratio is forced to deviate from the ideal[3][4]. This is because all switch capacitor circuit topologies operate by transferring and redistributing charge (and current) in fixed ways using the switches and capacitors, so non-ideal voltage conversion ratios necessarily provide loss.

To address the need to regulate the output voltage at low loss, and inductor-based very high frequency regulation stage is placed after the first stage. This very high frequency stage now can be optimized to provide the regulation function with high efficiency, high power density, and fast transient response. With a use of inductor, the output current and power can be regulated more naturally and continuously and since this inductor volume can be reduced by operating the converter at higher frequency, this regulation stage should be operated at high switching frequency. In our prototype converter, we designed and built inverted resonant buck converter as the regulation second stage.

Specifically, in our proposed two-stage architecture the switched capacitor first stage serves multiple functions. First, it takes a wide-input range voltage (e.g. rectified sinusoidal voltage or wide-range DC voltage) and provides an intermediate voltage having a lower voltage and a greatly reduced voltage range: with the approach introduced here a 25-200V input voltage magnitude can be reduced to a 50-100V intermediate voltage range over which the second stage, high frequency regulator converter, operates; that is, 8:1 input voltage swing range is narrowed to 2:1 voltage range. Second, it reduces the peak input voltage for which the high frequency stage must operate by a factor of two, mitigating device voltage stress and improving the impedance levels for which the circuit must operate, i.e., increasing the capacitance and reducing the inductance that high frequency stage needs. Improved impedance

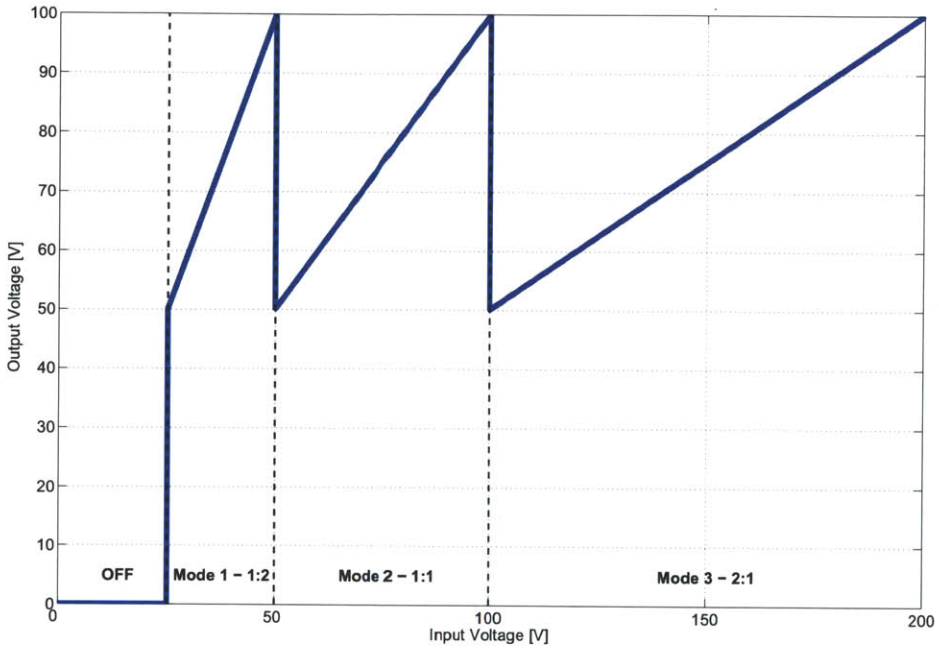


Figure 2-2: DC version: input voltage output voltage relation.

levels help to offset the total size of converter by decreasing the large volume of inductor and making the capacitors in the high frequency stage have more desirable values of capacitance. This switched capacitor circuit works slightly differently in a DC input application or an AC input application, with the details described below.

2.2 Switched Capacitor Circuit Operation for a DC Input Application with Wide Input Voltage Range

In a DC input voltage applications, the system may need to run across a wide input voltage range. Here we consider the case where the input voltage to the switched capacitor circuit is in the range of 25-200V DC voltage. To make a suitable intermediate voltage that is connected to the input node of the second stage, we divide the input voltage into 3 ranges according to the input voltage level and convert them to

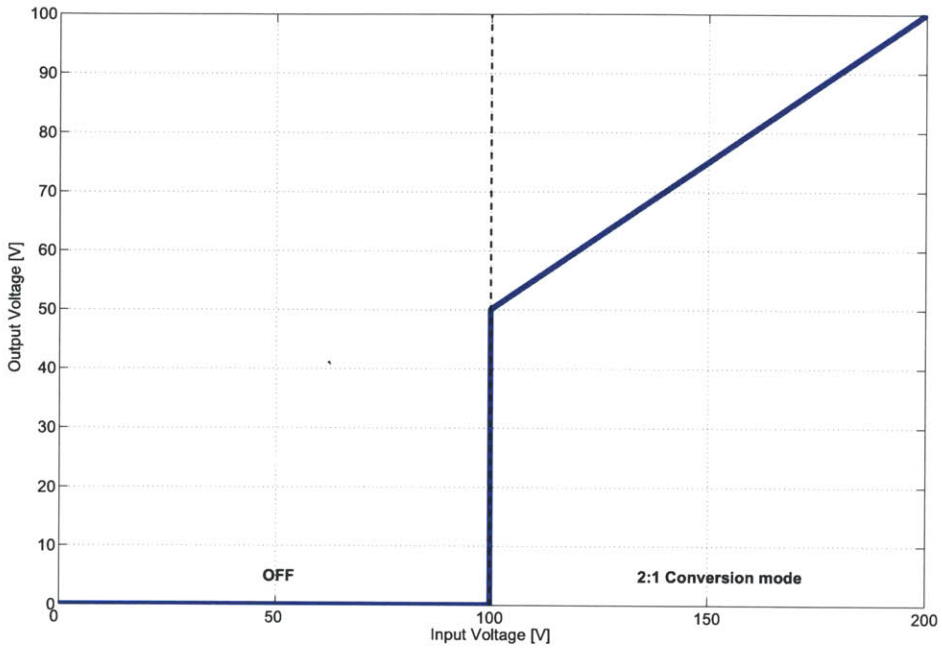


Figure 2-3: AC version: input voltage output voltage relation.

an intermediate voltage as shown in figure 2-2. In the first range(e.g. 25-50V), the input voltage is low and this circuit supplies twice the input voltage to the second stage. In the second range (e.g. 50-100V), we directly deliver the input voltage to the second stage. In the third range (e.g. 100-200V), we halve the input voltage and deliver this half of the input voltage to the second stage. Consequently, the first stage, a switched capacitor DC-DC converter, needs three operation modes, i.e. 1:2, 1:1, and 2:1 input to output voltage ratio, according to the input voltage. It is recognized that switched capacitor converters more precisely provide specific current conversion ratios, here 2:1, 1:1, and 1:2, with the voltage conversion ratios being approximate. As will be seen, in the first range, 1:2 voltage conversion ratio, we hard charge and soft discharge the capacitor. In the second range, 1:1 voltage conversion ratio, we bypass the capacitor and need not modulate the SC stage and in the third range, 2:1 voltage conversion ratio, we are able to soft-charge (or adiabatically charge) the switched capacitor stage. Our approach takes advantage of merged operation of the two stages with soft charging [1][2].Only a single energy transfer capacitor required

in the simplest version of the switched capacitor circuit, and two capacitors are used for an interleaved version with low input and output current ripple. The Details of soft-charging or adiabatic-charge is described in section 3.3.

2.3 Switched Capacitor Circuit Operation for an AC Input Application

In an AC input application, the switched capacitor circuit is connected to the output of a full-bridge rectifier. Over part of the range, power is drawn from the line in a manner that the rectifier output follows a rectified version of the line voltage. Below some input voltage threshold, however, the converter stops switching so that the rectifier output is constant and the line current is zero, as shown in figure 2-5. To minimize total volume including input filter and to get high power factor above 0.9, our circuit operates so as to deliver power only above 100V input voltage; as shown in figure 2-3, the switched capacitor circuit operates to halve the rectified line voltage above 100V and turns off below 100V. Figure 2-4 shows a waveform of the ideal voltage of before and after the switched capacitor circuit connected to full-bridge rectifier. Because we turn off the switched capacitor circuit below 100V, and also transfer no power to the load(i.e. no modulating of the VHF stage and the LED voltage provided by a line-frequency holdup capacitor), the output voltage of the switched capacitor circuit stays at a constant voltage held by the small bypass capacitor. As shown in the figure 2-4, the switched capacitor circuit not only reduces the wide-range input voltage range to the shaded narrow-range voltage range but also reduces the peak voltage provided to the regulation stage down to 85V(for a 170V peak line voltage). Supposing we draw power proportional to the square of the input voltage above 100V by modulating the current waveform as shown in figure 2-5, the calculation of power factor is as follows:

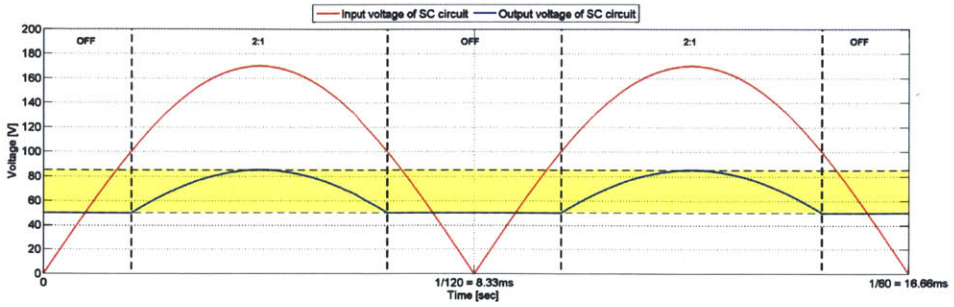


Figure 2-4: AC Version: input/output voltage waveform of SC circuit vs time.

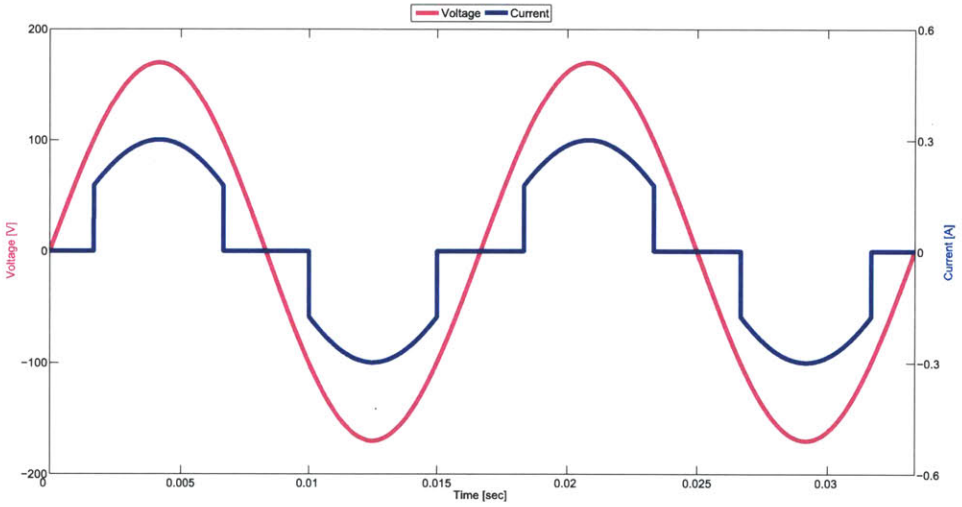


Figure 2-5: AC Version: input voltage and current waveform vs time.

$$
\begin{aligned}
PowerFactor &= \frac{< P >}{V_{rms} I_{rms}} \\
&= \frac{\int_{sin^{-1}(\frac{100}{120\sqrt{2}})}^{\pi - sin^{-1}(\frac{100}{120\sqrt{2}})} V sin(wt) I sin(wt) d(wt)}{\sqrt{\frac{1}{\pi}\int_0^{\pi} V^2 sin^2(wt) d(wt)} \sqrt{\frac{1}{\pi}\int_{sin^{-1}(\frac{100}{120\sqrt{2}})}^{\pi - sin^{-1}(\frac{100}{120\sqrt{2}})} I^2 sin^2(wt) d(wt)}} \\
&\simeq 0.95 \qquad (2.1)
\end{aligned}
$$

As shown in above equation (2.1), transferring power only above 100V input voltage and shaping the current waveform makes our proposed two-stage architecture

ideally provide 0.95 power factor, which is well above the minimum desired 0.9 power factor requirement for a LED driver circuit.

2.4 VHF Regulation Circuit

In general, any kind of DC-DC converter with high efficiency and high power density operating at high frequency can be utilized as a second stage of two-stage architecture. In our prototype system, a high ripple inverted resonant buck converter is employed as a regulation second stage as shown in figure 2-6. This circuit, whose design has been developed in conjunction with MIT graduate student John Ranson, operates step by step as depicted in figure 2-7 and figure 2-8.

Interval (a): the switch(SW1) turns on and the inductor(L1) current rises as voltage $V_{in} - V_{LED}$ is applied to the inductor.

Interval (b): the switch(SW1) turns off, inductor current flows through the output capacitance of the switch, and the output capacitance of switch(C_{oss}) is charged up to V_{in}.

Interval (c): As the output capacitance of switch(C_{oss}) is charged up to V_{in}, the diode(D1) turns on and the inductor(L1) current falls as a voltage $-V_{LED}$ is applied across the inductor.

Interval (d): When the inductor(L1) current goes to zero, the diode(D1) turns off and the inductor(L1) and the switch output capacitance(C_{oss}) start to resonate. From this resonance, the drain-to-source voltage(V_{ds}) of the switch(SW1) rings down from V_{in} to $V_{in} - 2V_{LED}$; thus, if $V_{in} < 2V_{LED}$ the V_{ds} can reach zero voltage and if $V_{in} > 2V_{LED}$ the switch voltage V_{ds} can reach the minimum voltage $V_{in} - 2V_{LED}$. For zero-voltage-switching(ZVS) or minimum-voltage switching, the switch turns on again at this minimum V_{ds} voltage.

Interval (e): If $V_{in} < 2V_{LED}$, the voltage V_{ds} can ring down below zero voltage and the diode embedded in the device turns on and clips voltage V_{ds} zero voltage. The switch should be turned on during the time when this built-in-device diode conducts.

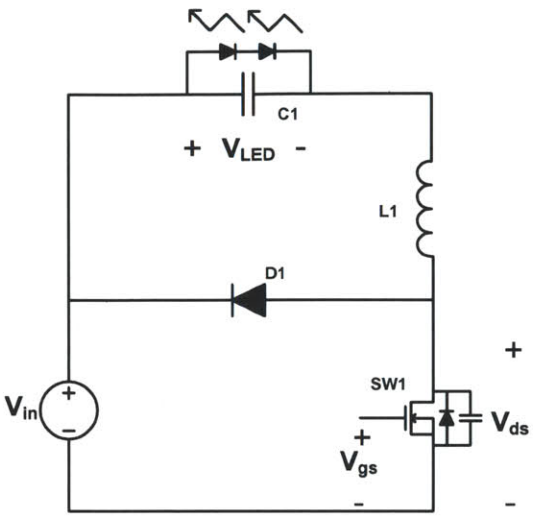


Figure 2-6: VHF regulation stage inverted resonant buck circuit schematic.

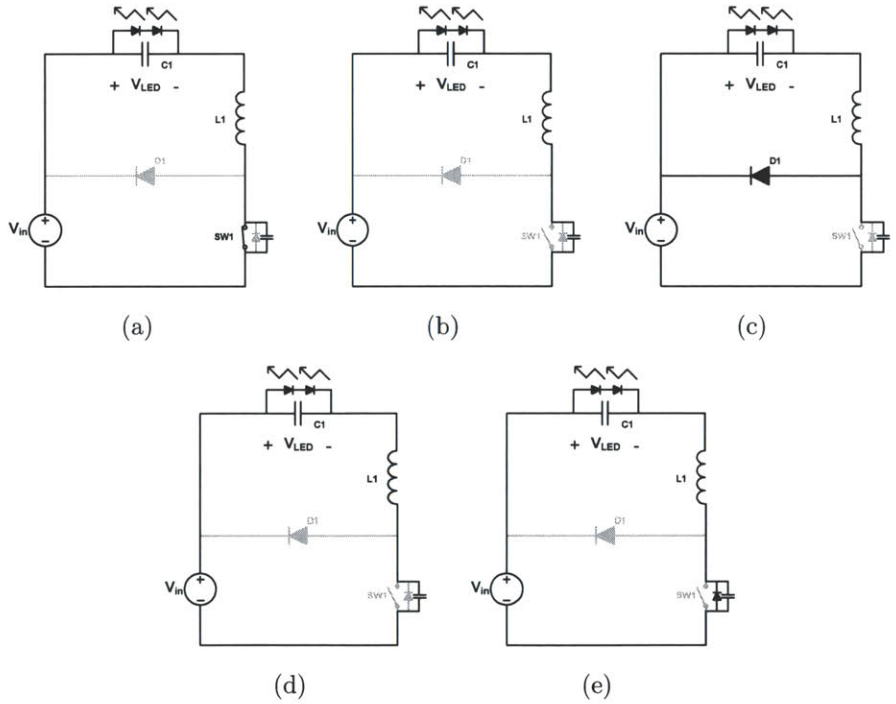


Figure 2-7: VHF regulation stage inverted resonant buck circuit behavior.

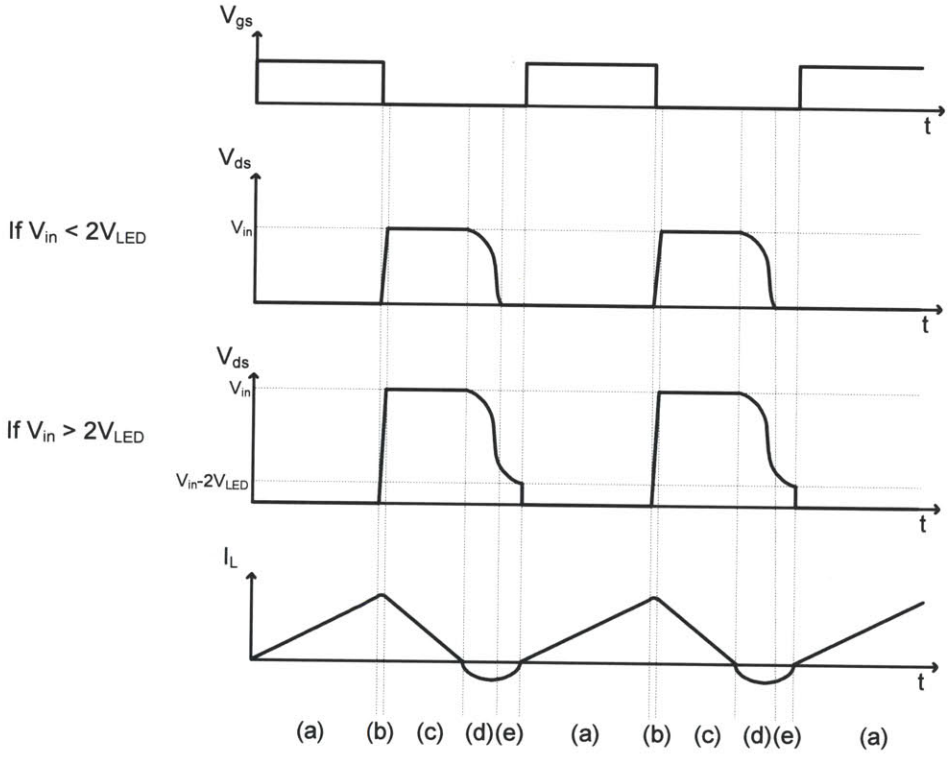


Figure 2-8: VHF regulation stage inverted resonant buck circuit ideal waveform.

Chapter 3

Switched Capacitor Pre-Regulator Stage

To build an efficient two-stage power converter with high power density and high efficiency, reducing the size and total number of switches and passive components are essential. Also as shown in chapter 2, our switched capacitor circuit can be operated to double (i.e. 1:2 conversion mode), bypass (i.e. 1:1 conversion mode), and halve (i.e. 2:1 conversion mode) the input voltage and transfer to drive the VHF regulation stage. The switched capacitor circuit can be designed with one energy transfer capacitor in a non-interleaved version or two energy transfer capacitors in interleaved version. The switched capacitor stage operates at 30-100kHz switching frequency and the behavior is described as follows.

3.1 Switched Capacitor Circuit Behavior

Figure 3-1 shows the topology of the simplest (non-interleaved) version of the switched capacitor conversion stage along with its connection to the second stage. In this non-interleaved switched capacitor circuit, only one 100V rating energy transfer capacitor C1, four 200V rating switches and one 100V rating diode are used. Owing to the fact that the first stage operates at a much lower frequency than the second stage (e.g. one tenth the frequency), we can model the second VHF stage as a ideal current

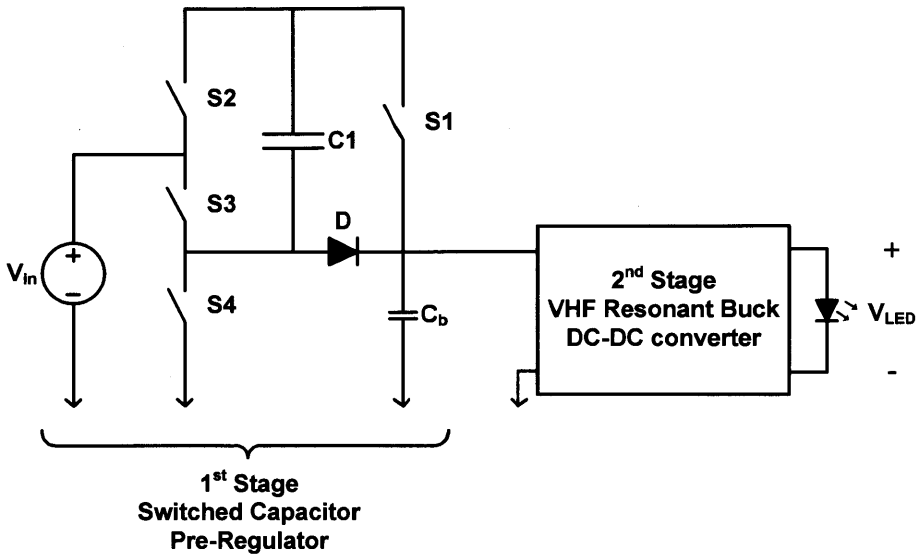


Figure 3-1: switched capacitor circuit with VHF stage.

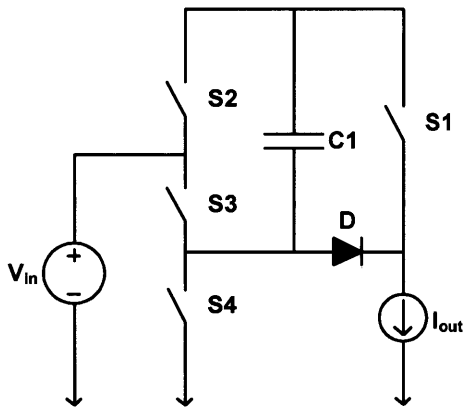


Figure 3-2: SC circuit schematic.

Case	1:2	1:1	2:1
S1	q	on	$\overline{q}$
S2	$\overline{q}$	on	q
S3	q	off	off
S4	$\overline{q}$	off	$\overline{q}$
D	off	off	q

Table 3.1: control of SC circuit.

source loading the first stage as shown in figure 3-2. In addition, to obtain high efficiency with soft-charging (described in section 3.3) of C1 in the 2:1 mode, we design the capacitor C_b value which is much smaller than capacitor C1; C_b is a tiny capacitor(e.g. several nF) only suited as a high frequency input bypass capacitor for

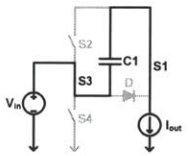
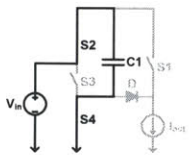
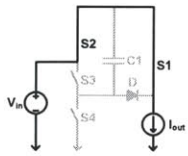
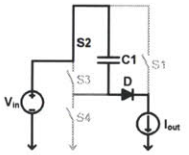
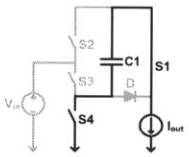
mode	state 1	state 2
1:2		
1:1		
2:1		

Table 3.2: behavior model of the switched capacitor stage.

the second stage. If we suppose 100% efficiency of the second stage, the current value of the current source is the LED output power over the output voltage of the switched capacitor circuit.

To realize the desired voltage range for second stage when operating from a DC input of 25-200V, the switched capacitor DC-DC stage has to be operated with three different conversion modes and at each mode the switched capacitor circuit switches are turned on and off as shown in Table 3.1. Table 3.2 describes each state at three different conversion modes including the current flow path and the following subsection describes the detailed behavior of each operating mode.

3.1.1 1:2 conversion mode

As described above, at a low input voltage (e.g. below 50V), the switched capacitor DC-DC converter stage operates to supply twice input voltage to the second stage. As shown in the table 3.2, capacitor C1 is charged toward the input voltage in state 2 and the sum of this charged voltage and the input voltage supply twice the input voltage to the second stage in state 1. It should be noted that in this mode, power is only

provided to the second stage during state 1 and the second stage should be turned off in state 2. Moreover, the input current drawn from the line pulsates (as a quasi-square wave) at the switched capacitor stage switching frequency. If desired, these limitations can be addressed by interleaving two switched capacitor stages and operating them out of phase as illustrated in section 3.2. This interleaving switched capacitor cells also reduces input EMI filtering requirements at the expense of component count and complexity. The final design demonstrated in this thesis will be an interleaved design owing to these advantages.

3.1.2 1:1 conversion mode

In the mid-range input voltage(e.g. 50-100V), the first stage operates in as a bypass mode, passing the input voltage directly to the second stage. As shown in the table 3.1 and table 3.2, switches S1 and S2 are held on to provide a current path from the input voltage to the second stage. In this state, there is no switching, and constant power is drawn from the input and delivered to the second stage.

3.1.3 2:1 conversion mode

At high input voltages (e.g. above 100V), the switched capacitor DC-DC converter acts to halve the input voltage. Table 3.1 and table 3.2 specify the control of each switch and show two states of the 2:1 conversion case. In state 1, capacitor C1 is charged by the power draw of the second converter stage. In state 2, this capacitor is discharged by the power draw of the second converter stage. The switching between states is designed to regulate the voltage of the output node and the voltage of the capacitor C1 near half of the input voltage. The switched capacitor circuit can supply the current in both state 1 and state 2. Because the second stage absorbs the difference between the input voltage and the voltage on C1, soft charging (e.g. quasi-adiabatic charging and discharging) of C1 is realized[1][2]. However, note that the current drawn from the input pulsates as a quasi-square wave at the switched capacitor converter switching frequency, which can drive up input filtering requirements. Again, this

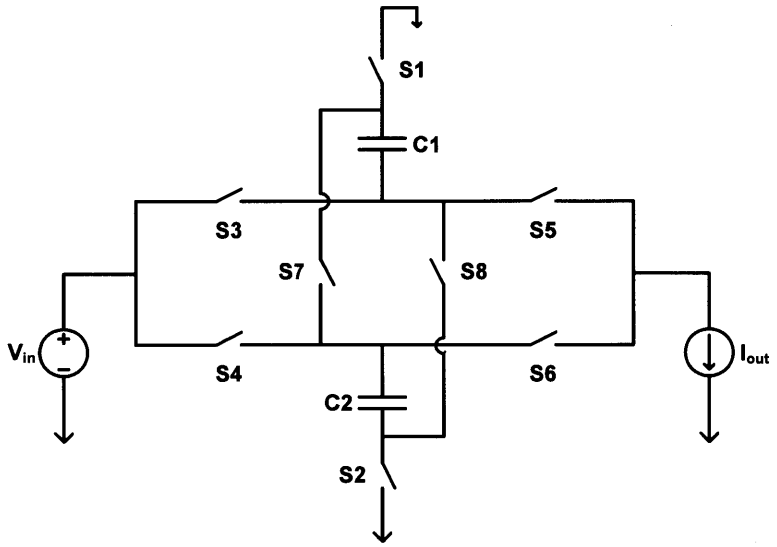


Figure 3-3: interleaved switched capacitor circuit schematic with ideal current model of source second stage.

Case	S1	S2	S3	S4	S5	S6	S7	S8
1:2	q	$\overline{q}$	q	$\overline{q}$	$\overline{q}$	q	$\overline{q}$	q
1:1	q	off	on	on	on	on	off	off
2:1	q	$\overline{q}$	$\overline{q}$	q	q	$\overline{q}$	$\overline{q}$	q

Table 3.3: control of interleaved switched capacitor circuit.

drawback can be mitigated with an interleaved design.

3.2 Interleaved switched capacitor Converter

The switched capacitor circuit topology described in section 3.1 works well for all three different conversion modes. However, there are some restrictions. First, at 1:2 conversion mode, the second stage must be modulated on and off at the switched capacitor converter switching frequency, as it can only draw power only in state 1 as shown in table 3.2. Second, the input current drawn by the switched capacitor stage is pulsating for both 1:2 and 2:1 modes. If we connect this two-stage architecture

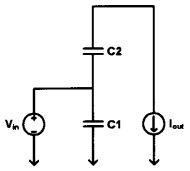
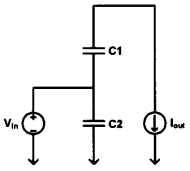
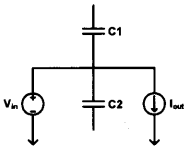
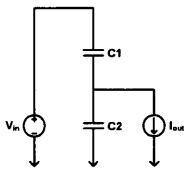
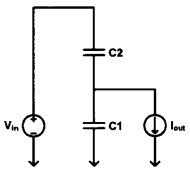
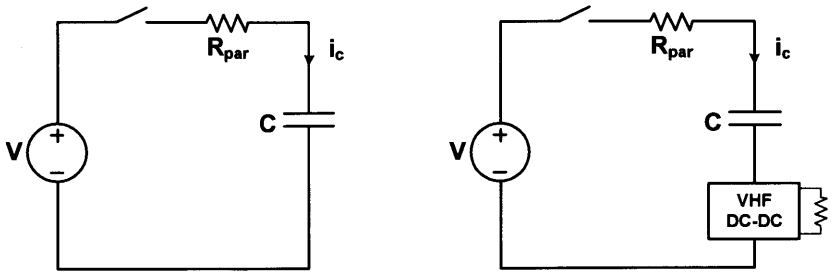
mode	state 1	state 2
1:2		
1:1		
2:1		

Table 3.4: behavior model of the interleaved switched capacitor stage.

to the AC line voltage or in many DC applications, electric magnetic interference (EMI) specifications should be met; thus the large pulsating currents at the switched capacitor circuit switching frequency and its harmonics should be filtered out. In addition, to minimize the dissipation coming from driver circuit and hard-switching of switched capacitor circuit switches, the operating frequency of the switched capacitor circuit is kept low(e.g., around 30-100kHz) such that the switched capacitor circuit harmonic frequency components need to be filtered out to meet EMI specifications. Therefore, since our proposed switched capacitor circuit only has two states operating at near 50% duty ratio, we connect two switched capacitor circuit cells in parallel and operate them 180 degree out of phase. This interleaved switched capacitor circuit allows nearly continuous current flow at its input and output instead of the pulsating currents as described in figure 3-3 and table 3.4.

3.3 Soft Charging(Adiabatic Charging)

One additional benefit of two-stage architecture is soft charging/discharging(or adiabatic charging/discharging) of the switched capacitor circuit. In general, for a



(a) hard charging (b) soft charging

Figure 3-4: comparison between hard charging and soft charging.

switched capacitor circuit, the capacitors are charged by voltage sources by the switches connecting a capacitor "stack" to voltage sources as shown in figure 3-4(a). Consequently high peak current flows through the parasitic resistance, i.e., hard charging/discharging, causing loss. The power sourced by voltage sources, charged to the capacitor, and dissipated in the parasitic resistor are as follows.

Power sourced by voltage source:

$$= \int_0^t V_f i_c dt = V_f \int_0^t C\frac{dv_c}{dt}dt = V_f \int_{V_i}^{V_f} C dv_c = CV_f(V_f - V_i) \tag{3.1}$$

Power charged to capacitor:

$$= \int_0^t v_c i_c dt = \int_0^t v_c C\frac{dv_c}{dt}dt = \int_{V_i}^{V_f} C v_c dv_c = \frac{1}{2}C(V_f^2 - V_i^2) \tag{3.2}$$

Power dissipated at parasitic resistor:

$$= \int_0^t i_c^2 R_{par} dt = \int_0^t (V_f - v_c)C\frac{dv_c}{dt}dt = C(\frac{1}{2}V_f^2 - V_i V_f + \frac{1}{2}V_i^2) \tag{3.3}$$

As shown above, in hard-charging/discharging case every time the switch turns on to charge up the discharged capacitor, $C(\frac{1}{2}V_f^2 - V_i V_f + \frac{1}{2}V_i^2)$ amount energy is dissipated in the parasitic resistance which comes from equivalent series resistance(ESR) of capacitor, resistance of PCB trace, or turn-on transistor resistance. To reduce this

consumption, the difference between the voltage before charging(V_i) and the voltage after charging(V_f) should be minimized. Consequently, conventional hard-switching switched capacitor circuits require either large capacitors or high switching frequencies to attain small voltage ripple on a capacitor; but, both solution degrade the converter performance in terms of large volume, low power density, and high driving circuit power dissipation, causing low efficiency.

This close relation of efficiency with capacitance and switching frequency in the conventional switched capacitor circuit can be relieved with soft-charging(adiabatic charging), obtained by merging switched capacitor circuit with high frequency DC-DC converter in our two-stage architecture as shown in figure 3-4(b). Compared to hard-charging case, soft-charging case does not allow applying voltage directly to capacitor and charge/discharge the capacitor only through the current flowing to the VHF regulation second stage. Since the frequency of the switched capacitor circuit (e.g. 30-100kHz) is much lower than the frequency of the VHF regulation circuit(e.g. 5-10MHz), the VHF regulation circuit charge and discharge the capacitors at the switched capacitor circuit like an ideal current source; getting away from pulsed charging current, the charging/discharging with smooth sourcing current to VHF stage diminish the loss dissipating at parasitic resistance. Described in other way, the voltage difference of the capacitor voltage and input voltage is applied directly to the VHF stage, therefore, the capacitor does not have to be charged instantaneously by pulsing current though the capacitor. This allows conduction losses commensurate with the "fast switching limit" of the switched capacitor converter [3][4] while operating at low frequencies commensurate with the slow switching limit. As noted before in table 3.4, the 2:1 conversion mode shows fully usage of this soft-charging technique and the 1:2 conversion mode shows soft-charging only half of the cycle.

Chapter 4

Prototype Converter

A prototype two-stage dc-dc converter of the proposed power converter architecture was simulated, built, and demonstrated. In this chapter, the simulation results and estimated loss of the switched capacitor circuit are illustrated. In a following section, the detailed implementation and measurement results of the merged two-stage converter are described.

4.1 Simulation Results

The switched capacitor stage was designed and simulated in the Spice circuit simulator. All the operation modes are tested with ideal current source load modeling the VHF regulation circuit. The efficiency estimated from the circuit simulation was around 95%, varying with operating point(i.e., changing switching frequency, operation modes, or input voltage). The losses come mainly from the switch on-state conduction loss and switch output capacitor discharge loss. The detail of dissipation estimation is described below.

4.1.1 Estimated Dissipation

The main dissipation of the switched capacitor circuit comes from two portions, resistive loss from switch conduction loss and hard-charging/discharging loss from each

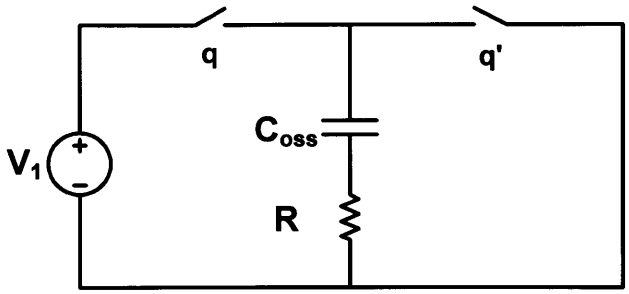


Figure 4-1: model of hard switching transistor.

switch output capacitor.

First, the resistive loss comes from dissipation at the turn-on switch resistance as current flows through the switches. When we suppose continuous current flowing through the switched capacitor circuit, the power losses from turn-on resistor in each conversion mode are as follows:

Dissipated Power during switch on-state:

$$P_{diss:conduction} = I_{in}^2 R_{total} = \begin{cases} (\frac{I_{in}}{2})^2 \times 5\ R_{sw} & 1:2\ conversion\ mode \\ I_{in}^2 \times 2\ R_{sw} & 1:1\ conversion\ mode \\ (2I_{in})^2 \times 2\ R_{sw} + I_{in}^2 \times 4\ R_{sw} & 2:1\ conversion\ mode \end{cases}$$

As shown above, $1.25R_{sw}I_{in}^2$, $2R_{sw}I_{in}^2$, and $12R_{sw}I_{in}^2$ power is dissipated in the switches connecting the input voltage to the VHF regulation second stage. Supposing that R_{sw} of our prototype GaN switch is about 0.1 Ω, $I_{in} = \frac{P_{out}}{V_{in}}$, and maximum power(e.g., 30W) at the minimum voltage in each mode(i.e., largest loss case at each mode), the power losses are 0.18W in 1:2 conversion mode, 0.072W in 1:1 conversion mode, and 0.108W in 2:1 conversion mode. The switched capacitor circuit conduction losses are up to 0.6% of the output power in a wide-range DC-DC converter implementation and up to 0.2% of the power in a AC-DC converter implementation.

Second portion of the loss comes from discharging/charging the output capacitance

	SW1/SW2	SW3/SW4	SW5/SW6	SW7/SW8
1:2 Conversion Mode	$2V_{in}$	V_{in}	V_{in}	$2V_{in}$
2:1 Conversion Mode	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	V_{in}

Table 4.1: blocking boltage of each switch at each conversion mode.

of the switches during turn on and after turn off. As described briefly in section 3.3 and figure 3-4(a), hard-switching causes loss of the stored energy in the switch output capacitor when a switch turns on, and the process of charging the output capacitor likewise incurs loss after switch turn off. blocks the voltage or not. The figure 4-1 shows the model of charging and discharging a switch with a parasitic resistor and the dissipated energy and dissipated power is as follows:

Dissipated Energy at charging:

$$E_{diss:ch} = \int_0^t i_c^2 R dt = \int_0^t (V_1 - v_c)c(v)\frac{dv_c}{dt}dt = \int_0^{V_1} (V_1 - v_c)c(v)dv_c$$

Dissipated Energy at discharging:

$$E_{diss:dch} = \int_0^t i_c^2 R dt = \int_0^t -v_c c(v)\frac{dv_c}{dt}dt = \int_{V_1}^0 -v_c c(v)dv_c$$

Dissipated Power:

$$P_{diss:capacitor} = \frac{E_{diss:ch} + E_{diss:dch}}{T} = (E_{diss:ch} + E_{diss:dch})f_{sw} = f_{sw}V_1 \int_0^{V_1} c(v)dt$$

If we suppose constant output capacitance of the switch and charging/discharging between 0 and V, the dissipated energy at charging and discharging is $E_{diss:ch} = E_{diss:dch} = \frac{1}{2} cV^2$. Thus, total cV^2 energy is dissipated over a cycle during which the switch turns on and off. At the interleaved switched capacitor circuit, table 4.1 shows the

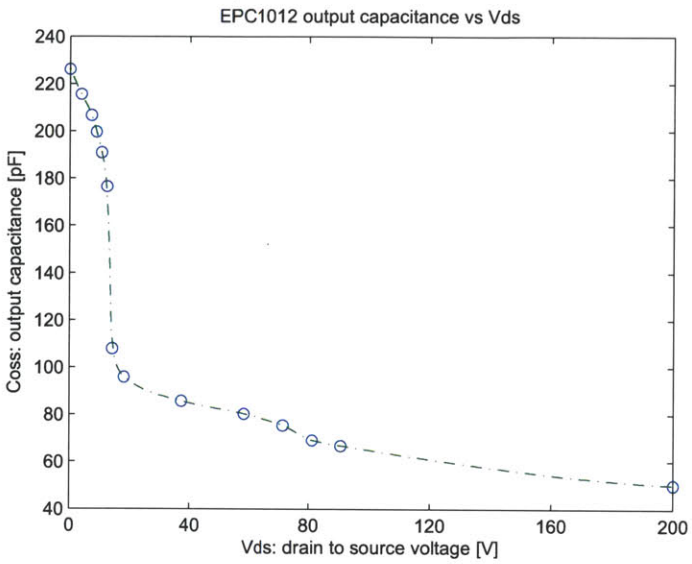


Figure 4-2: output capacitance of GaN transistor vs V_{DS} voltage.

blocking voltage of each switch at 1:2 conversion mode and 2:1 conversion mode. In 1:1 conversion mode, we turn on SW3, SW4, SW5, and SW6 all the time and there is no loss coming from hard-switching C_{oss} charging/discharging loss. The total power loss in each conversion mode is as shown below:

1:2 Conversion Mode - hard switching Dissipated Power:

$$P_{diss:Coss} = \{C_{oss}(2V_{in})^2 + C_{oss}V_{in}^2 + C_{oss}V_{in}^2 + C_{oss}(2V_{in})^2\} \times 2 \times f_{sw} = 20C_{oss}f_{sw}V_{in}^2$$

1:1 Conversion Mode - hard switching Dissipated Power:

$P_{diss:Coss} = 0$

1:2 Conversion Mode - hard switching Dissipated Power:

$$P_{diss:Coss} = \left\{C_{oss}(\frac{V_{in}}{2})^2 + C_{oss}(\frac{V_{in}}{2})^2 + C_{oss}V_{in}^2 + C_{oss}(\frac{V_{in}}{2})^2\right\} \times 2 \times f_{sw} = \frac{7}{2}C_{oss}f_{sw}V_{in}^2$$

Using a nominal 80pF output capacitance from the datasheet of the EPC1012 and

operating at 100kHz switching frequency, the worst case losses are 0.4W (i.e., 1.67% of 30W load) in 1:2 conversion mode and 1.12W (i.e., 4.67% of 30W load) in 2:1 conversion mode.

Even worse, when we actually measured the commercial GaN device output capacitance (C_{oss}), the output capacitance is larger than the 80pF datasheet value as shown in figure 4-2. From this figure, the large output capacitance especially at low drain to source voltage increases the hard-switching loss; from the fitted data the estimated maximum losses are $4.83 f_{sw}$ μW in 1:2 conversion mode and $12 f_{sw}$ μW in 2:1 conversion mode(with f_{sw} in Hz).

From the above estimation, it was shown that the major portion of the dissipation of the switched capacitor circuit comes from hard-switching of the switches. To gain high efficiency by reducing this dissipation, we can compromise by decreasing the frequency of the switched capacitor circuit, because the dissipated power is ideally proportional to output capacitance of switch, switching frequency, and the square of blocking voltage.

In our proposed interleaved version of the switched capacitor circuit topology, the lower limit of the switching frequency was restricted by three factors: audible frequency content, EMI specifications, and voltage ripple restrictions. Since people can hear frequencies up to about 20kHz, the proposed circuit needs to be operated above 20kHz. Also, EMI conducted specifications limit the current frequency components ranging from 150kHz to 30MHz; to reduce the EMI filter size the switched capacitor circuit should be operated below 150kHz. The other factor of deciding switching frequency is the allowed voltage ripple to the VHF regulation stage. Using our soft-charging technique, the capacitor is charged and discharged by the VHF regulation stage which can be modeled as a current source. The charged/discharged capacitor voltage ripple should be in the desirable voltage range for operation of the second stage. Equations 4.1 and 4.2 show the relations between capacitor value, switching frequency, and allowed voltage ripple to the VHF regulation stage. For example, if we design with 1μF energy transfer capacitor and allow 5V ripple input voltage to the VHF second stage, the switching frequency should be above 30kHz.

$$q_c = I_c t = \frac{I_c}{2f_{sw}} = C\Delta V < C\Delta V_{ripple} \tag{4.1}$$

$$f_{sw} > \frac{I_c}{2C\Delta V_{ripple}} = \begin{cases} \frac{P_{out}}{4C\Delta V_{ripple}V_{in}} & 1:2\ conversion mode \\ \frac{P_{out}}{2C\Delta V_{ripple}V_{in}} & 2:1\ conversion mode \end{cases} \tag{4.2}$$

4.2 Implementation

Both non-interleaved and interleaved versions of the switched capacitor circuit were implemented and measured. In addition, a complete merged two-stage power conversion system was designed, including an on-board micro-controller which controls the switching signal. In this section, the operation of a merged two-stage prototype circuit for wide-range dc input is illustrated.

Brief schematics of the switched capacitor circuit and gate driver circuit are shown in figure 4-3 and figure 4-4. Figure 4-4 shows switch 3 driver circuit and the other switch driver circuits are configured similarly. The components used in this circuit are categorized in Table 4.2(the detailed schematics and board layouts are provided in Appendix A). As shown in figure 4-3, switches S3, S4, S5, and S6 are realized by connecting two GaN HEMTs back-to-back to block bidirectional voltage. These switches can also be implemented with one switch and one diode because the power flows only one direction, from input voltage to the VHF regulation circuit. But, because of the diode forward drop loss, configuring switch with two back-to-back HEMTs is more attractive, providing around 5% higher efficiency.

Another point to be noted is the means for driving the switches. Since the source nodes of several switches (i.e., S3, S4, S5, S6, S7, and S8) are not ground referenced (flying control port), a floating driver is needed. In some of the prototype converters developed in this thesis, the floating drivers are each realized with an isolated power supply/gate driver followed by a low-side gate driver, as shown in figure 4-4. The main merit of this technique is flexibility of operation, since the selected driver can

provide both isolation (level shifting) and power for the driver (e.g., in figure 4-4, isolating power supply/gate driver provides power to charge capacitors CD6 and CS5, which charged voltage is then used for low-side gate driver). Another way to provide power to drive the floating switches (also validated in this thesis) is using a boot-strap technique incorporating diodes and capacitors, as shown briefly in figure 4-5. The advantage of this technique is that it has relatively low cost and power dissipation as compared to using the isolated power supply/gate driver to feed the floating gate drivers. (We nevertheless continue to use isolators to provide gate drive command level shifting, and use the same low-side gate drivers to drive the transistors. Given the availability of the bootstrap power supply, simpler level shifting circuits are available, but were not used.)

Here we describe the operation of the bootstrap driver system of figure 4-5. To drive floating switches with low-side gate driver, the bootstrap capacitors (Cb3, Cb4, Cb5, Cb6, Cb7, and Cb8), each referenced to source node of a switch, need to be charged to the desired logic/driver voltage. The bootstrap technique works with proper switch and diode operation as shown in Table 4.3, which includes which devices are on during at each state in each conversion mode. One thing should be noted is that, originally in 1:1 conversion mode, the switched capacitor circuit does not change the state and always turns on switches S3, S4, S5, and S6 providing two current paths from input voltage to second stage (i.e., S3,S5 path and S4,S6 path). But to charge the bootstrap capacitors, periodic turning on/off of the switches is required in 1:1 conversion mode and we make the switched capacitor circuit change state, selecting one path (S3,S5 path or S4,S6 path) and toggling between these states when using bootstrap based driver circuit. With bootstrap technique, CD6 and CS3 capacitors in figure 4-4 was charged through bootstrap diode and logic supply instead of isolated supply/gate driver component ADuM5240. The isolated supply/gate driver (ADuM5240) only operates to level shift gate drive signal. The prototype merged two-stage dc-dc converter was designed to be selectively use with either the isolated supply/gate driver and the bootstrap. The detailed schematics and components are shown in Appendix A figure A-1 and figure A-2.

The VHF regulation stage inverted buck converter was also implemented, along with its control circuit. The main circuit block schematic and components for this stage are briefly shown in figure 4-6 and table 4.4. The VHF regulation circuit is closed-loop controlled based on peak current flowing through the inductor; it will be described thoroughly in MIT graduate student John Ranson's M.Eng. thesis.

The PCB board was designed and the components are properly placed and soldered on PCB board as shown in the figure 4-7. The detailed layout of the PCB is attached in Appendix A.

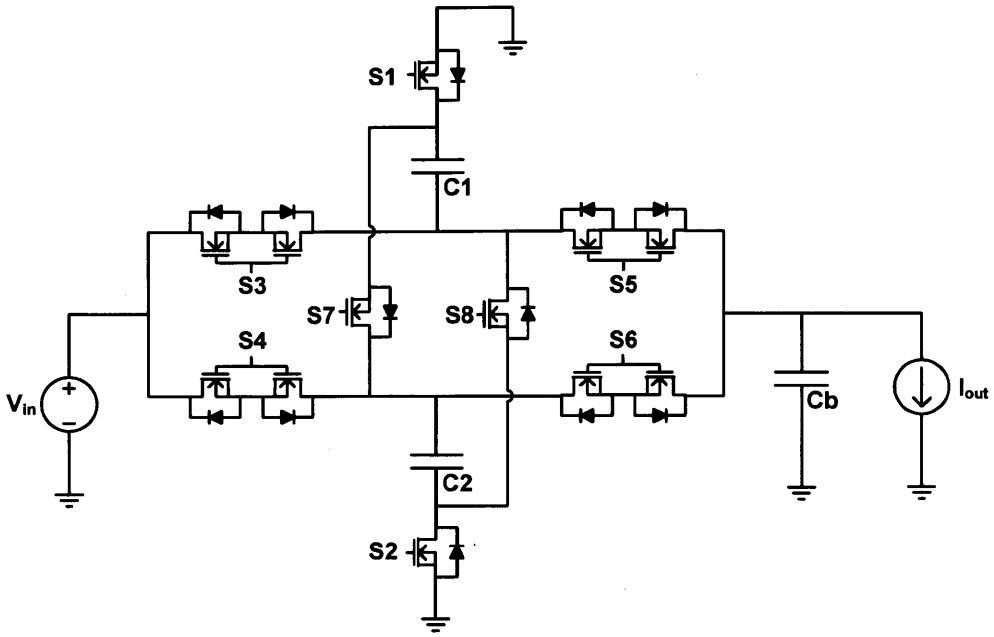


Figure 4-3: switch realization of switched capacitor circuit.

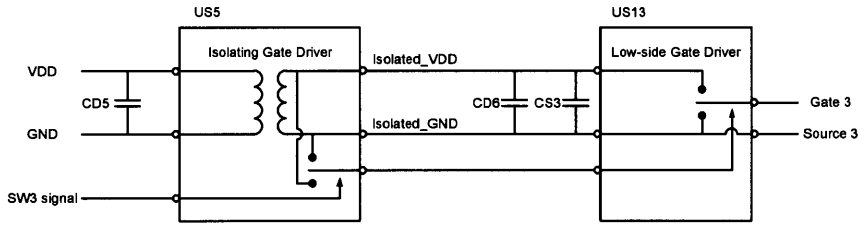


Figure 4-4: switch 3 driver circuit of switched capacitor circuit.

Designator	Description	Manufacturer	Part Number
S1, S2, S3, S4, S5, S6, S7, S8	HEMT - GaN - 200V - 3A	EPC	EPC2012
C1, C2	Capacitor - 1uF - 100V - X7R - 1210	Taiyo Yuden	HMK325B7105KN-T
Cd5	Capacitor - 1uF 16V - X7R - 1206	Taiyo Yuden	EMK316B7105KF-T
Cd6	Capacitor - 1uF 10V - X5R - 0306	Taiyo Yuden	LWK107B7105KA-T
CS5	Capacitor - 1uF 16V - X7R - 1206	Taiyo Yuden	EMK316B7105KF-T
US5	Isolated Power Supply Gate Driver	Analog Devices	ADuM5240ARZ
US13	Low side Gate Driver 1A SOT23-5	Fairchild	FAN3111CSX

Table 4.2: components of switched capacitor and driver circuit.

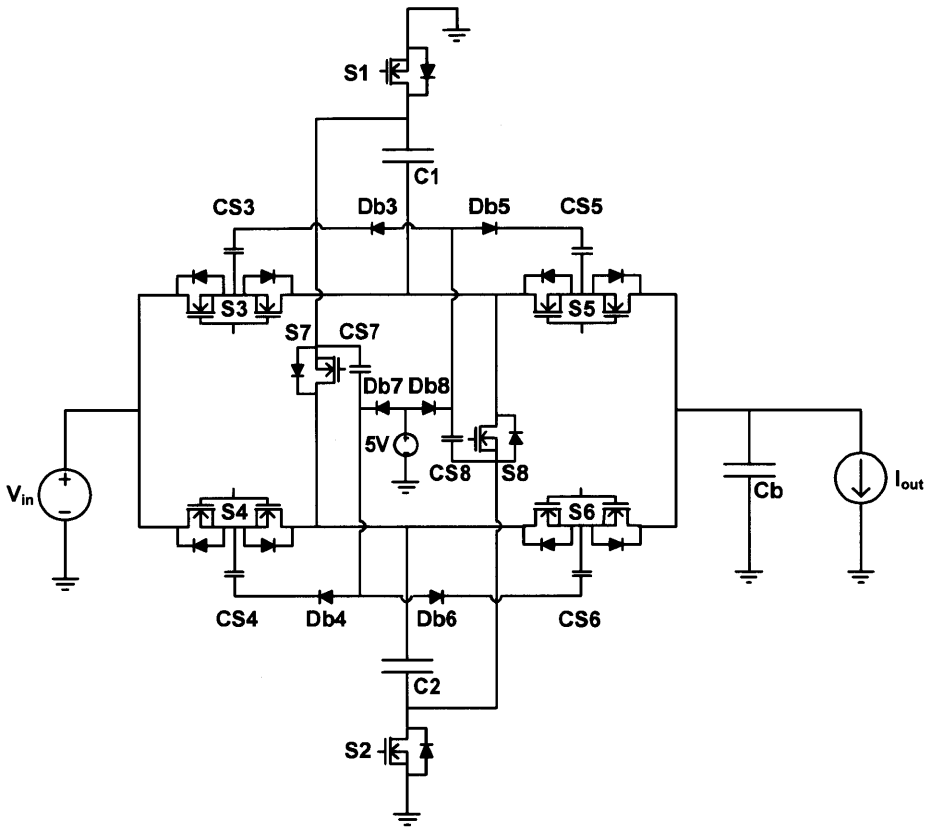


Figure 4-5: switched capacitor circuit driver bootstrap circuit schematic.

	state 1	state 2
1:2 conversion mode	S1, S3, S6, S8, Db3, Db5, Db7	S2, S4, S5, S7, Db4, Db6, Db8
1:1 conversion mode	S1, S3, S5, S8, Db3, Db5, Db7	S2, S4, S6, S7, Db4, Db6, Db8
2:1 conversion mode	S1, S4, S5, S8, Db3, Db5, Db7	S2, S3, S6, S7, Db4, Db6, Db8

Table 4.3: switched capacitor circuit bootstrap state. In each case the devices that are on/conducting are indicated.

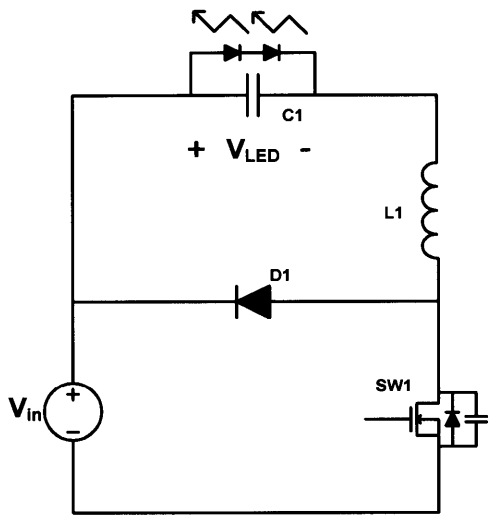


Figure 4-6: VHF regulation circuit schematic.

Designator	Description	Manufacturer	Part Number
C1, C2	Capacitor - 10uF 50V - X5R - 1210	Taiyo Yuden	UMK325BJ106KM-T
D1	Diode - Schottky 170V - 2x5A - DPAK	ST Microelectronics	STPS10170CB-TR
J1	Terminal Block Two Piece - 150mil - 1x2	Tyco Electronics	284517-2
L1, L2	Coilcraft Maxispring Inductor 422nH	Coilcraft	132-18SMGLB
QH2	HEMT - GaN - 200V - 3A	EPC	EPC1012
TP1, TP2	Test Point - TH	Keystone Electronics	1249

Table 4.4: components of VHF regulation circuit.

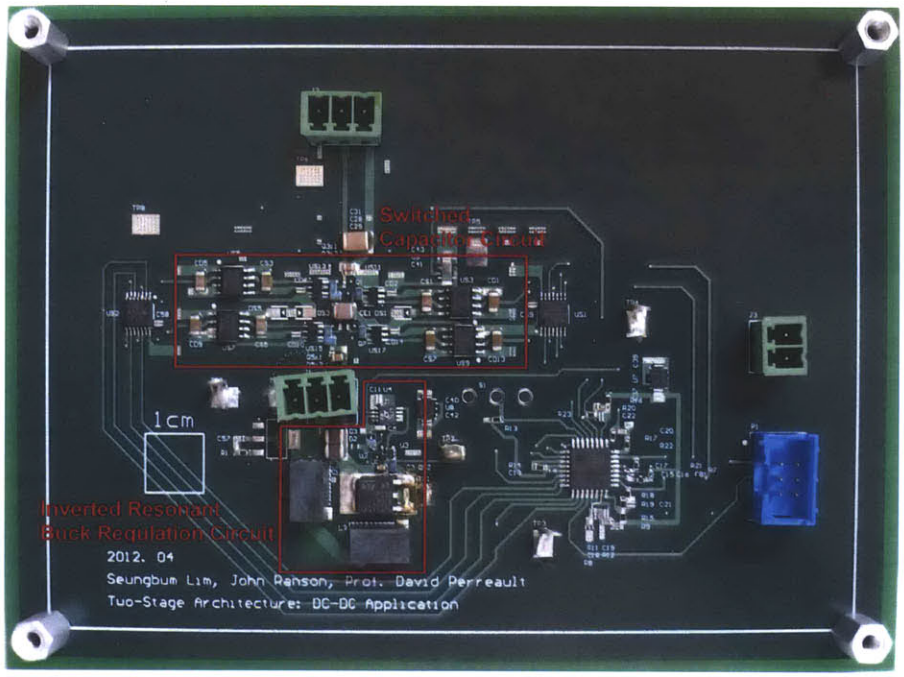


Figure 4-7: implemented PCB.

4.3 Measurement Results

The prototype circuit was implemented and measured with a constant 35V voltage load, provided by strings of LED or zener-diodes (experiments were run with both kinds of load, which act similarly). The two-stage dc-dc converter was powered by a Kepco KLO600-4 power supply, and the efficiency was calculated across input voltage range (25-200V) and the output power range (10-25W) by measuring dc input voltage/current and output voltage/current with four Agilent 34401A digital multimeters.

Figure 4-8, Figure 4-9 and Figure 4-10 illustrate the measured input voltage, intermediate voltage(i.e., the voltage between SC stage and VHF second stage), and switch control signal operating in each conversion mode of the switched capacitor circuit in the prototype two-stage dc-dc converter. The switched capacitor circuit works to double, bypass, and halve the voltage. Because the energy transfer capacitor is discharged by sourcing current to the second stage in 1:2 conversion mode and in 2:1 conversion mode, the intermediate voltage applied to the second stage declines as long as the switched capacitor circuit keeps in one state as shown in figure 4-8 and figure 4-10. The sudden decrease on the intermediate voltage comes from the SC circuit switch dead time between the two states. For this test measurement, we assigned about $0.5\sim1\mu$s dead time which can be decreased so long as shoot-through current is blocked safely.

Figure 4-11 shows a measured example waveform of switch gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) in the VHF regulation circuit at 60V input voltage (i.e., the switched capacitor circuit operates in 1:1 conversion mode and the intermediate voltage is around 60V). As seen in this figure, the switch operates at near zero-voltage switching as the V_{DS} rings down to close to zero voltage when the switch turns on. The proposed peak-current based control scheme modulates only the turn-on-duration to control power, so the switching frequency of the VHF regulation circuit is variable, typically operating around 7-11MHz (e.g., sample waveform figure 4-11 was operated at 11.05MHz switching frequency with 60V input voltage and 35V,

1.09W output load. Another sample waveform figure 4-12 was operated at 9.242MHz switching frequency with 60V input voltage and 35V, 6.29W output load; and figure 4-13 was operated at 7.847MHz switching frequency with 60V input voltage and 35V, 12.15W output load. The above three measurements in figure 4-11, figure 4-12, and figure 4-13 were modulated by the same peak-current based control scheme).

Figure 4-14 shows another sample waveform measuring gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) when the switched capacitor circuit operates in 1:1 conversion mode at 85V input voltage and 35V, 6.29W output load. Compared to the figure 4-12 (60V input voltage and 35V, 6.29W output load), the switch turns on higher V_{DS} voltage because the implemented inverted resonant buck converter allows zero-voltage-switching condition only if the intermediate voltage is below twice the output LED voltage. In addition, to keep the same peak current in the inductor, the switch on-time should be shortened at higher input voltage(i.e., increasing switching frequency). The efficiency of the VHF regulation stage thus degrades when the intermediate input voltage to the VHF second stage increases above two times the output voltage due to lose of ZVS and higher operating frequency.

In the two-stage dc-dc converter, the driver circuits, linear regulators, and the microcontroller are powered by separate 6V power supply. The dissipated power of these circuit was 0.6W with bootstrap driving method (figure 4-5 and table 4.3) or 4.32W with isolated power supply gate driver (figure 4-4). Thus, the commercial isolated power supply gate driver ADuM5240 dissipates a lot of power and using boot-strap technique can decrease driving circuit dissipation a lot.

Figure 4-15 shows the measured power stage efficiency (except logic and driver circuit power) and total efficiency (including logic and driver circuit power) of the complete system across input voltage at 12W output power operating into a 35V output voltage. The power stage efficiency is always above 85%, and goes as high as 95% when the SC circuit just operates to bypass the input voltage. As described above, the switched capacitor circuit operates in 1:2 conversion mode at 25-50V input voltage, in 1:1 conversion mode at 50-100V input voltage, and in 2:1 conversion mode at 100-200V input voltage to sustain the desired 50-100V intermediate voltage range

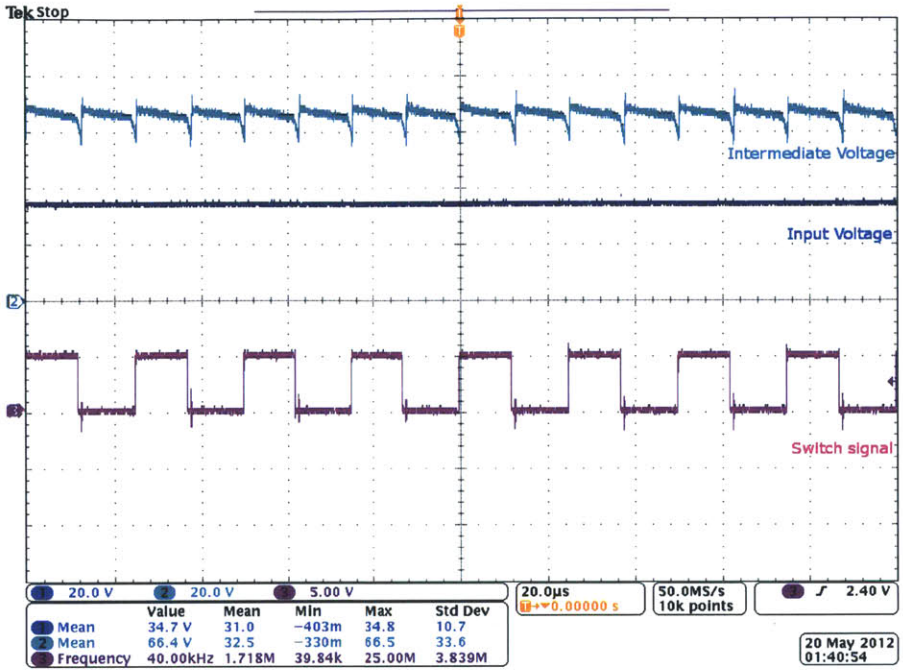


Figure 4-8: input voltage, intermediate voltage, and control signal in 1:2 conversion mode with 35V input voltage and 35V zener-diode 15.52W output load.

for the VHF stage. The VHF regulation circuit efficiency degrades as the VHF stage input voltage is above twice the output voltage. As found in the measured efficiency of figure 4-15, the efficiency drops as the input voltage goes up in each SC conversion mode because the VHF regulation stage loses zero-voltage-switching and operates at higher frequencies as the intermediate voltage goes up. However, as the switched capacitor circuit changes the conversion modes (i.e., crossing 50V point and crossing 100V point), the intermediate voltage falls to a more desirable lower voltage and the system efficiency rises up again. Figure 4-16 shows the efficiency across input voltage at 20W output power. Comparing figure 4-15 and figure 4-16, the efficiency with 35V 20W output load is similar to the efficiency with 35V 12W output load.

It may be concluded from the results in figure 4-15 and figure 4-16 that the proposed two-stage power conversion architecture has a great advantage in enabling high performance across a wide-range input voltage.

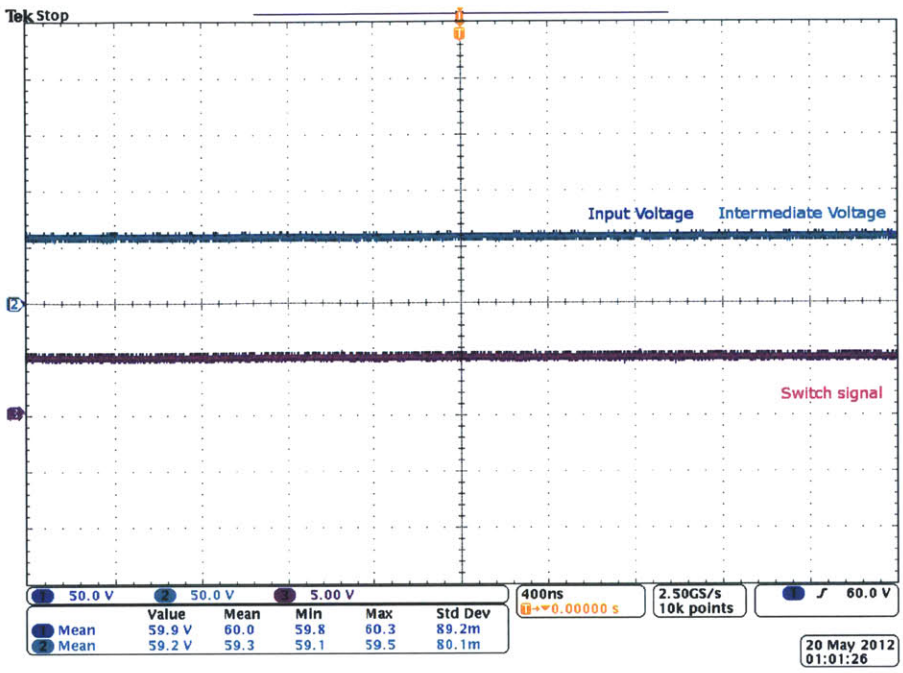


Figure 4-9: input voltage, intermediate voltage, and control signal in 1:1 conversion mode with 60V input voltage and 35V zener-diode 15.44W load.

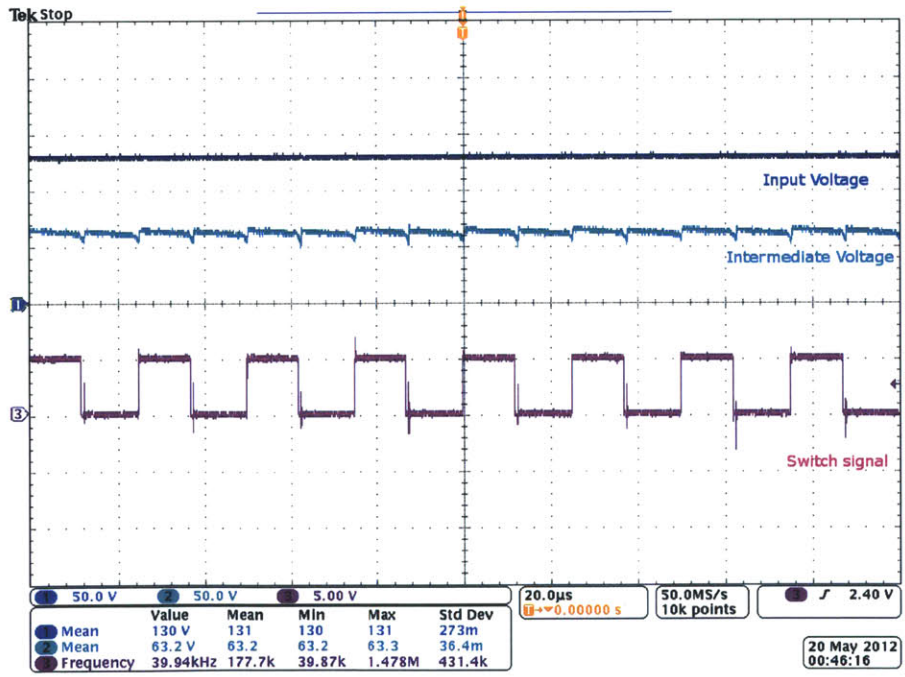


Figure 4-10: input voltage, intermediate voltage, and control signal in 2:1 conversion mode with 130V input voltage and 35V zener-diode 15.65W load.

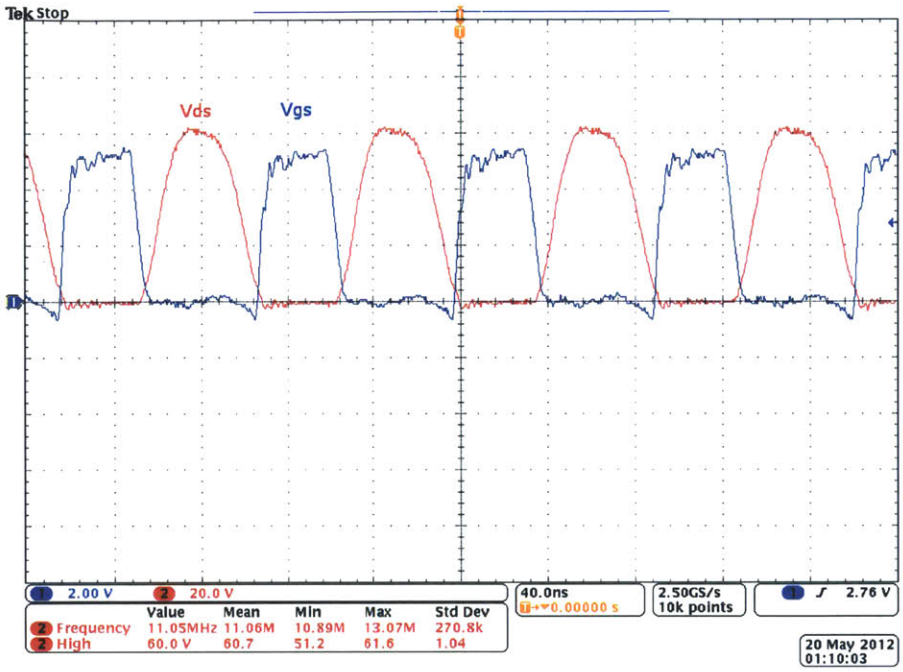


Figure 4-11: measured V_{GS} and V_{DS} at 60V input voltage with 35V zener-diode load and 1.09W output power.

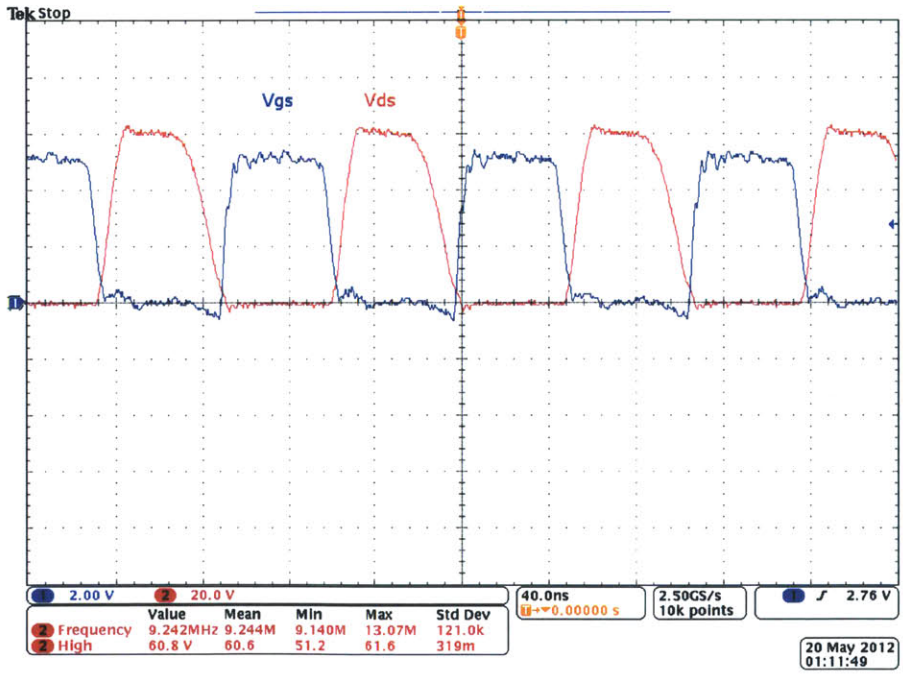


Figure 4-12: measured V_{GS} and V_{DS} at 60V input voltage with 35V zener-diode load and 6.29W output power.

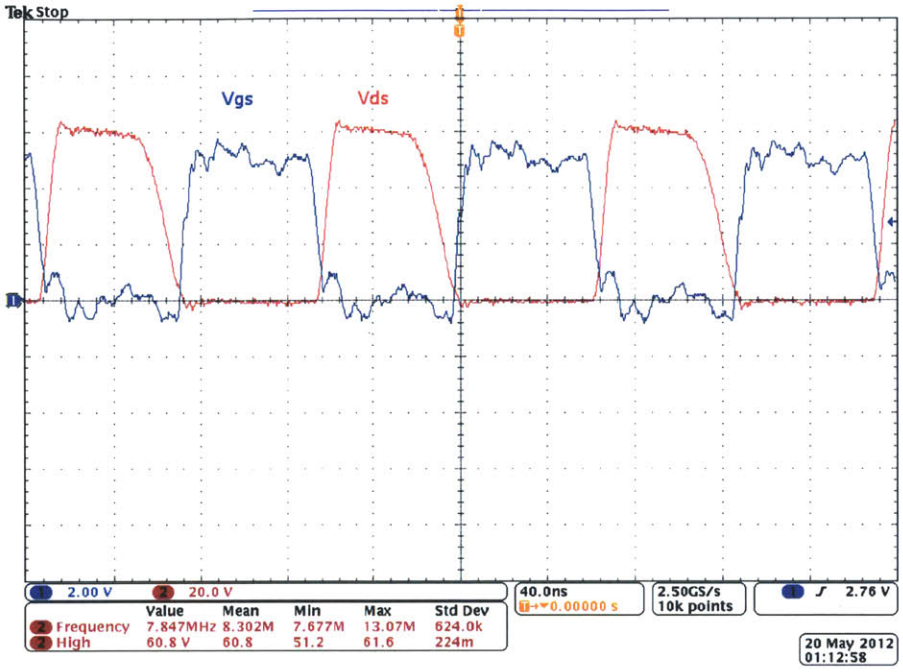


Figure 4-13: measured V_{GS} and V_{DS} at 60V input voltage with 35V zener-diode load and 12.15W output power.

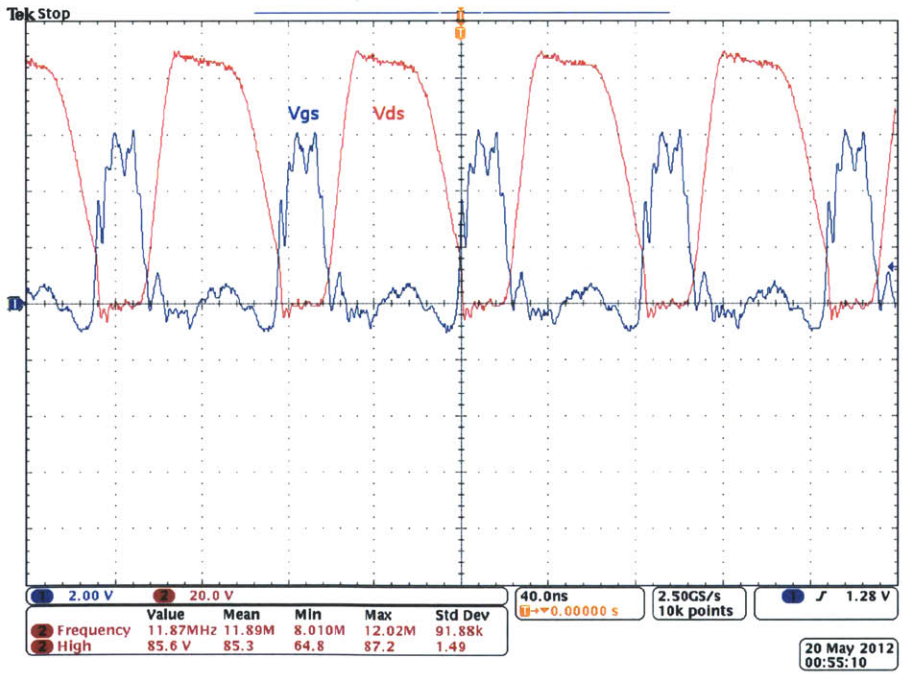


Figure 4-14: measured V_{GS} and V_{DS} at 85V input voltage with 35V zener-diode load and 6.29W output power.

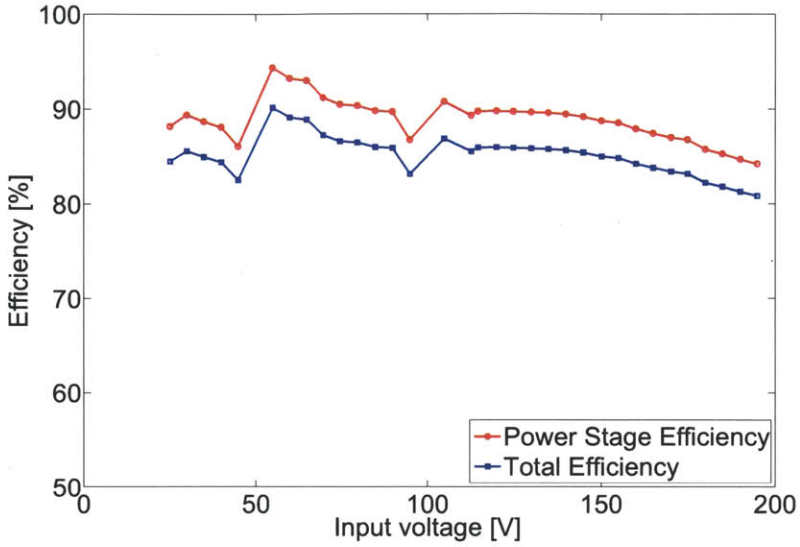


Figure 4-15: experimental efficiency of the merged two stage converter for 12W output power and a 35V zener-diode load across the input voltage range of 25-200V.

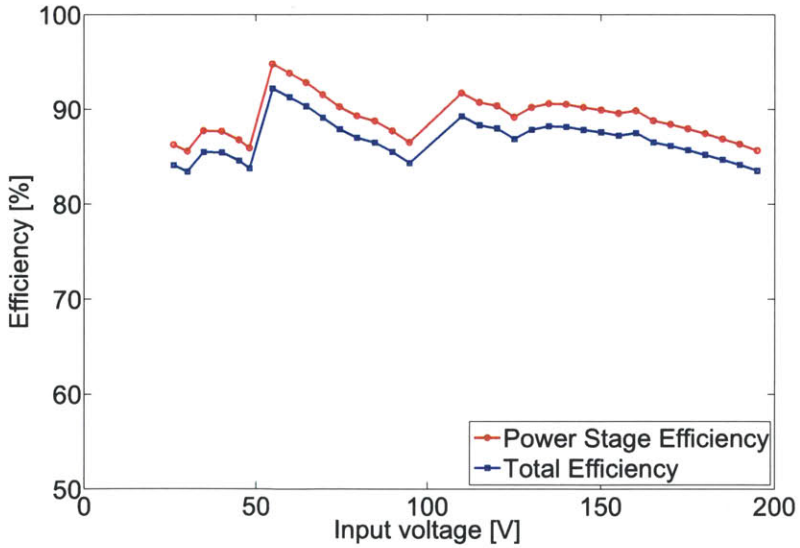


Figure 4-16: experimental efficiency of the merged two stage converter for 20W output power and a 35V zener-diode load across the input voltage range of 25-200V.

Chapter 5

Conclusion

5.1 Thesis Summary

In this thesis a two-stage power conversion architecture is described, implemented, and measured. The main contribution of this thesis is introducing and demonstrating a new power conversion architecture. This two-stage architecture includes a variable-topology switched capacitor converter that enables an 8:1 input voltage range to be compressed down to a 2:1 output voltage range, while using few passive components and having low input and output current ripple. This Sc circuit can be used with any current high performance ZVS DC-DC converter. This two-stage power conversion architecture helps to shrink the wide-voltage-range to the narrow-voltage-range and reduce the high voltage stress of the VHF regulation stage. In addition, proposed architecture can be used not only as DC-DC converter but also as a high power factor AC-DC converter by including a rectifier and modulating the power drawn over a line cycle. With a two-stage converter prototype, high performance and high power density was attained.

5.2 Future Work

The proposed architecture was implemented and tested for a wide-range DC voltage up to present. An AC input version of two stage architecture was also designed, built

and the measurements are in progress. Two-stage power conversion circuit was built based on discrete devices and there is tremendous room for saving power dissipation and volume by integrating a control circuit and a driver circuit in fabricated integrated chip(i.e., IC). In addition, our discrete inductor can be replaced by high performance and small volume nano-fabricated inductors and better GaN device fabrication is also in progress. In the future, we will test our current architecture with IC flip-chip, nano-fabricated inductor and GaN devices and high-density packaging based on a thin PCB interposer board. This highly integrated power converter will be expected to gain in power density and efficiency.

Appendix A

PCB Schematic and Layout

The prototype two-stage architecture circuit described in chapter 5 is demonstrated here. The detailed sub-block schematics and component parts of prototype PCB are illustrated in this section. The prototype PCB layout figures are attached (layer by layer).

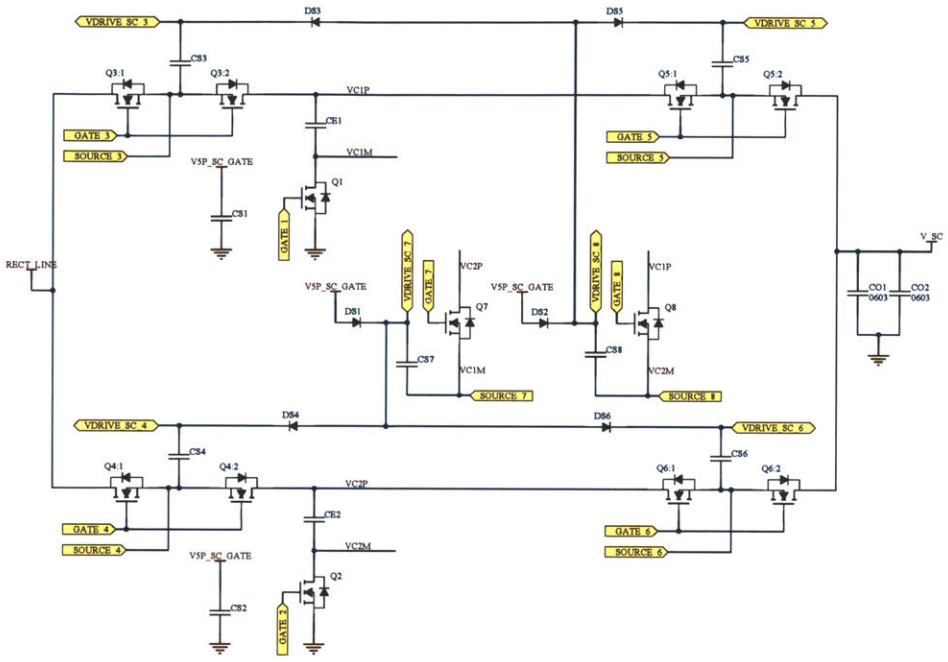


Figure A-1: schematic of two-stage architecture: switched capacitor circuit.

Designator	Description	Manufacturer	Part Number
CE1, CE2	Capacitor - 1uF - 100V - X7R - 1210	Taiyo Yuden	HMK325B7105KN-T
CO1, CO2	Capacitor - 10nF - 200V - X7R - 0603	Kemet	C0603C103K2RACTU
CS1, CS2, CS3, CS4, CS5, CS6, CS7, CS8	Capacitor - 1uF - 16V - X7R - 1206	Taiyo Yuden	EMK316B7105KF-T
DS1, DS2, DS3, DS4, DS5, DS6	Diode - Schottky 150V - 1A - PowerDI 123	Diodes Inc.	DFLS1150
Q1, Q2, Q3:1, Q3:2, Q4:1, Q4:2, Q5:1, Q5:2, Q6:1, Q6:2, Q7, Q8	HEMT - GaN - 200V - 3A	EPC	EPC2012

Table A.1: components of two-stage architecture: switched capacitor circuit.

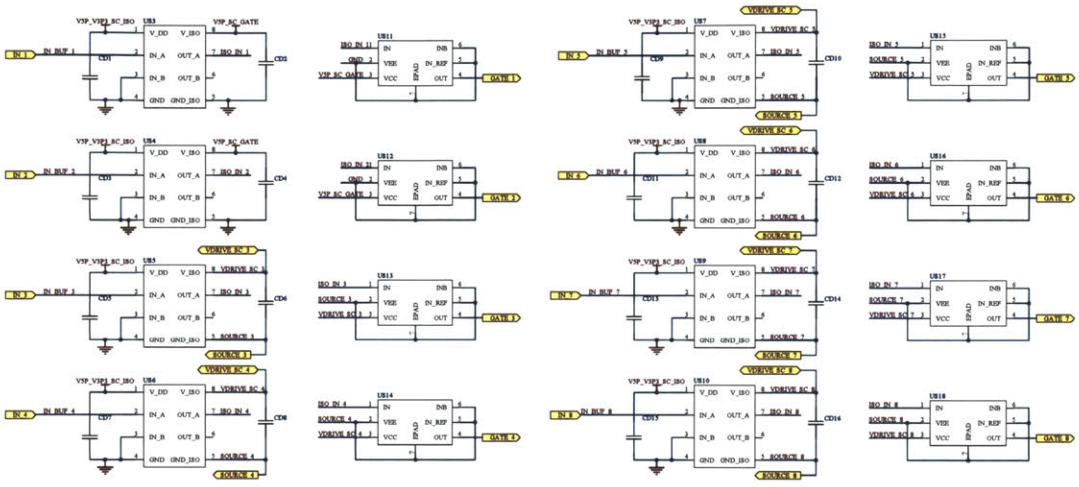


Figure A-2: schematic of two-stage architecture: switched capacitor driving circuit.

Designator	Description	Manufacturer	Part Number
CD1, CD3, CD5, CD7, CD9, CD11, CD13, CD15	Capacitor - 1uF 16V - X7R - 1206	Taiyo Yuden	EMK316B7105KF-T
CD2, CD4, CD6, CD8, CD10, CD12, CD14, CD16	Capacitor - 1uF 10V - X5R - 0306	Taiyo Yuden	LWK107B7105KA-T
US3, US4, US5, US6, US7, US8, US9, US10	Isolated Power Supply Gate Driver	Analog Devices	ADuM5240ARZ
US11, US12, US13, US14, US15, US16, US17, US18	Low side Gate Driver 1A SOT23-5	Fairchild	FAN3111CSX

Table A.2: components of two-stage architecture: switched capacitor driving circuit.

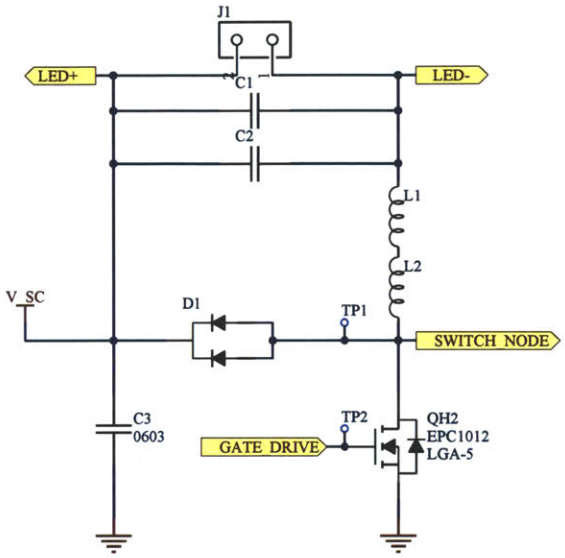


Figure A-3: schematic of two-stage architecture: VHF regulation inverted buck circuit.

Designator	Description	Manufacturer	Part Number
C1, C2	Capacitor - 10uF 50V - X5R - 1210	Taiyo Yuden	UMK325BJ106KM-T
D1	Diode - Schottky - 170V - 2x5A - DPAK	ST Microelectronics	STPS10170CB-TR
J1	Terminal Block Two Piece - 150mil - 1x2	Tyco Electronics	284517-2
L1, L2	Coilcraft Maxispring Inductor 422nH	Coilcraft	132-18SMGLB
QH2	HEMT - GaN - 200V - 3A	EPC	EPC1012
TP1, TP2	Test Point - TH	Keystone Electronics	1249

Table A.3: components of two-stage architecture: VHF regulation inverted buck circuit.

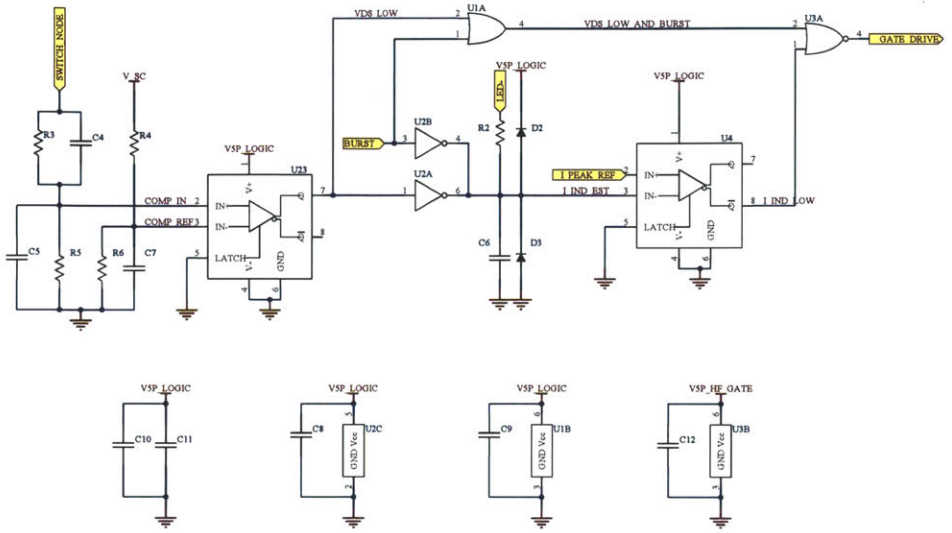


Figure A-4: schematic of two-stage architecture: VHF regulation inverted buck control and driving circuit.

Designator	Description	Manufacturer	Part Number
C4	Capacitor - 1.6pF - 250V - C0G - 0805	Murata	GQM2195C2E1R6BB12D
C5	Capacitor - 30pF - 100V - C0G - 0603	Murata	GRM1885C2A300JA01D
C6	Capacitor - 10pF - 100V - NP0 - 0603	TDK	C1608C0G1H100C
C7	Capacitor - 330pF - 100V - X7R - 0603	Murata	GRM188R72A331KA01D
C8, C9, C10, C11, C12	Capacitor - 4.7uF - 6.3V - X5R - 0306	Taiyo Yuden	JWK107BJ475MV-T
D2, D3	Diode - RF Schottky 40V - 20mA -TSSLP-2	Infineon	BAT62-02LS
R2	Resistor - 100k Ohm - 1% - 0805	Panasonic	ERJ6ENF1003V
R3	Resistor - 200k Ohm - 1% - 0805	Panasonic	ERJ6ENF2003V
R4	Resistor - 287k Ohm - 1% - 0805	Panasonic	ERJ6ENF2873V
R5, R6	Resistor - 10.5k Ohm - 1% - 0603	Panasonic	ERJ3EKF1052V
U1	OR Gate - 2.4ns - 1.65V - 5.5V	NXP	74LVC1G32GF
U2	Inverter - Dual - Open Drain 2.4ns, 1.65-5.5V	Texas Instruments	SN74LVC2G06YZPR
U3	NOR Gate - 2.4ns - 1.65V - 5.5V	Fairchild	NC7SZ02L6X
U4, U23	Comparator - 4.5ns - +/-5V	Linear	LT1711CMS8

Table A.4: components of two-stage architecture: VHF regulation inverted buck control and driving circuit.

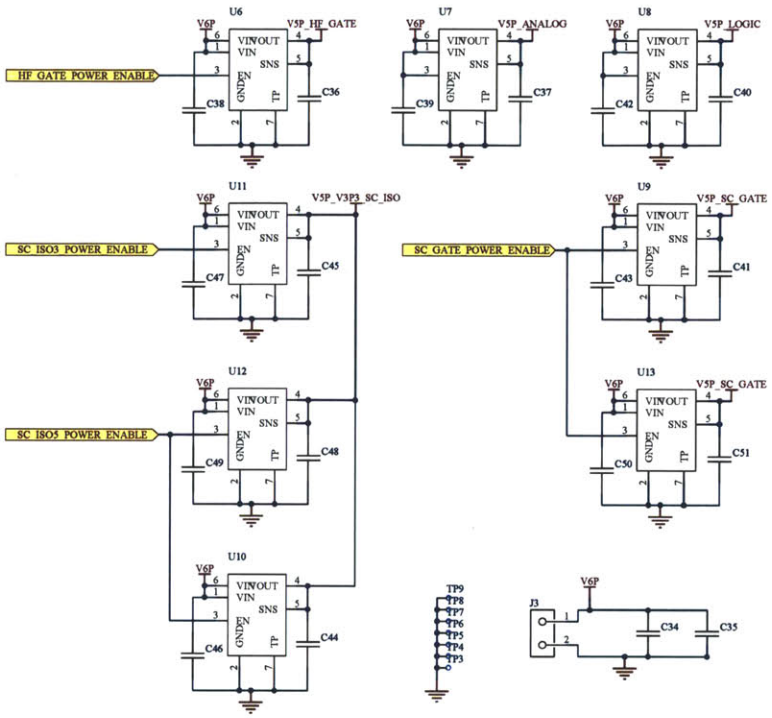


Figure A-5: schematic of two-stage architecture: power supplies.

Designator	Description	Manufacturer	Part Number
C34, C35	Capacitor - 10uF 16V - X5R - 0805	Taiyo Yuden	EMK212ABJ106KD-T
C36, C37, C38, C39, C40, C41, C42, C43,C44, C45, C46, C47, C48, C49, C50, C51	Capacitor - 4.7uF 6.3V - X5R - 0306	Taiyo Yuden	JWK107BJ475MV-T
J3	Terminal Block Two Piece - 150mil - 1x2	Tyco Electronics	284517-2
TP3, TP4, TP5, TP6, TP7, TP8, TP9	Test Point - SMT	Keystone Electronics	5016
U6, U7, U8, U9, U10, U12, U13	LDO Regulator - 5V - 1A	Texas Instruments	LP38692SD-5.0
U11	LDO Regulator - 3.3V - 1A	Texas Instruments	LP38692SD-3.3

Table A.5: components of two-stage architecture: power supplies.

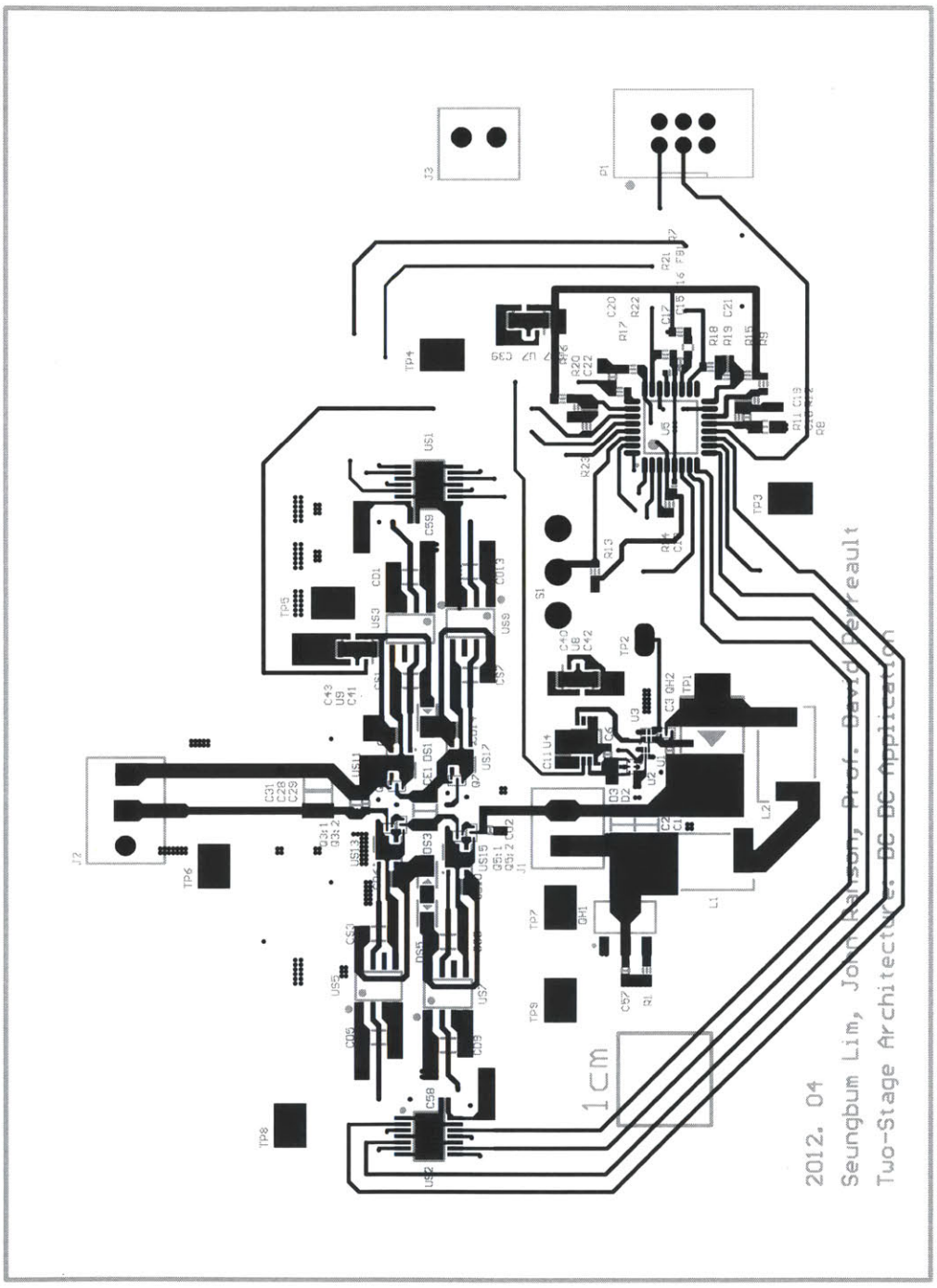


Figure A-6: two-stage architecture PCB layout layer 1.

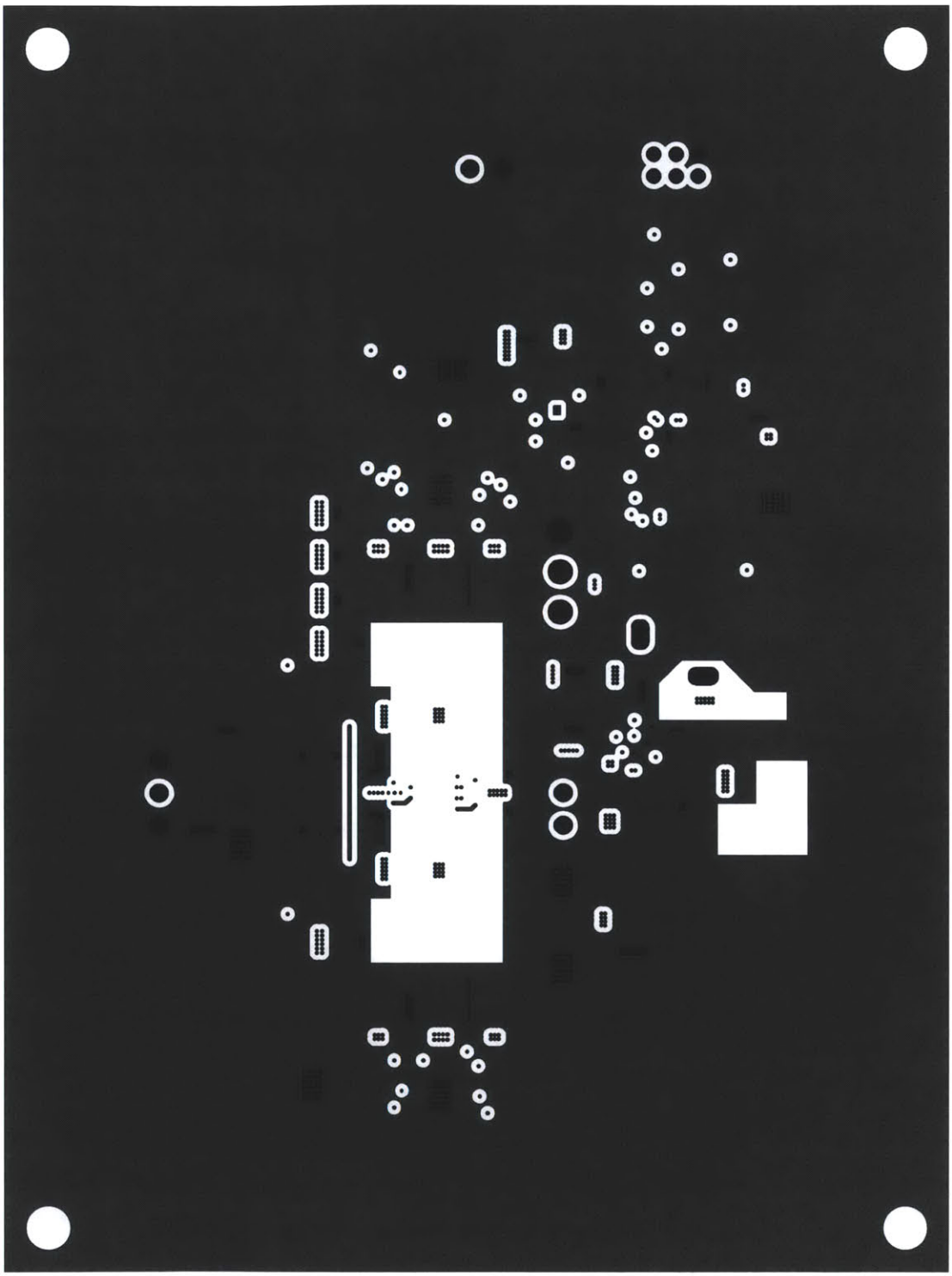


Figure A-7: two-stage architecture PCB layout layer 2.

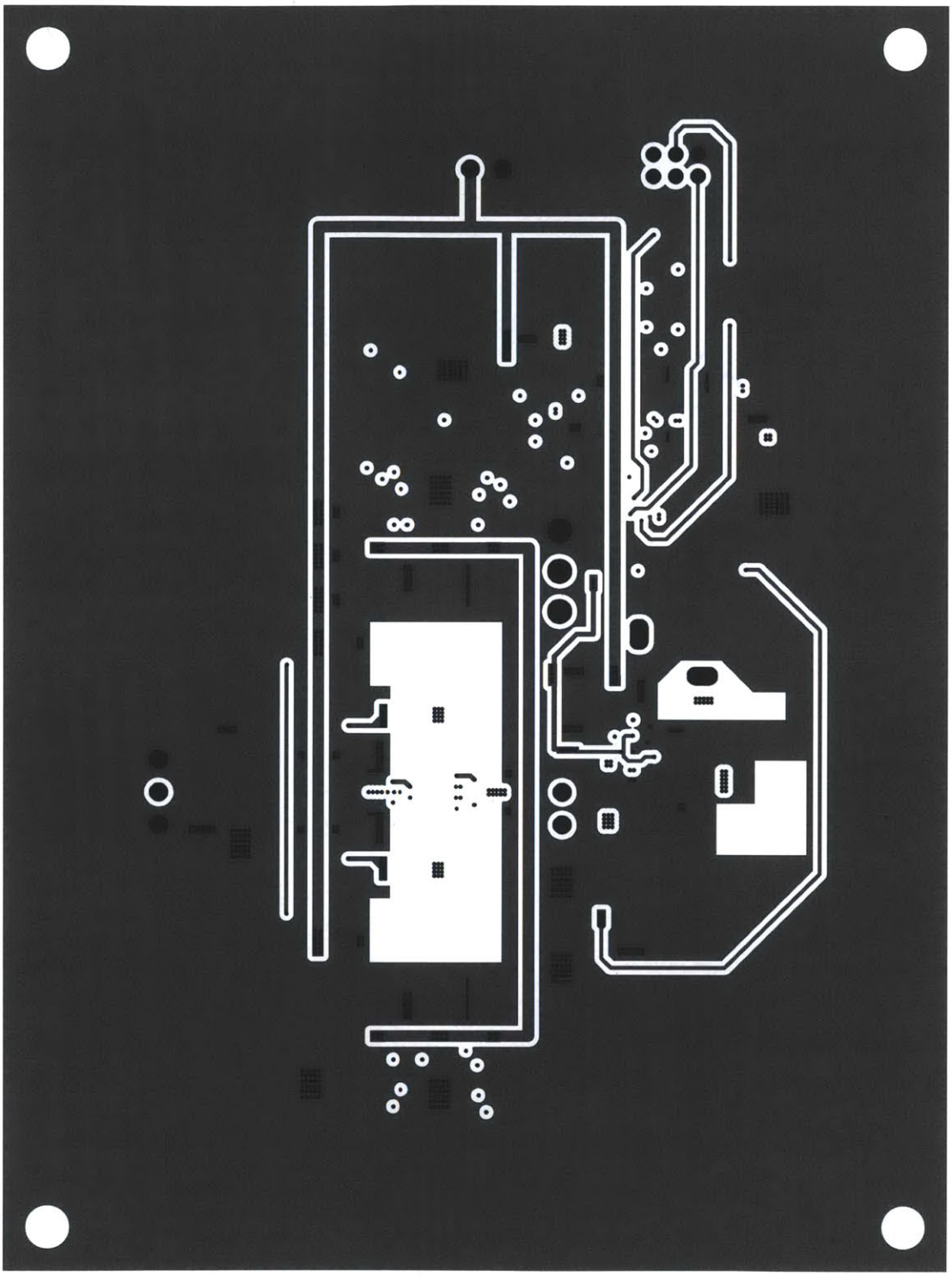


Figure A-8: two-stage architecture PCB layout layer 3.

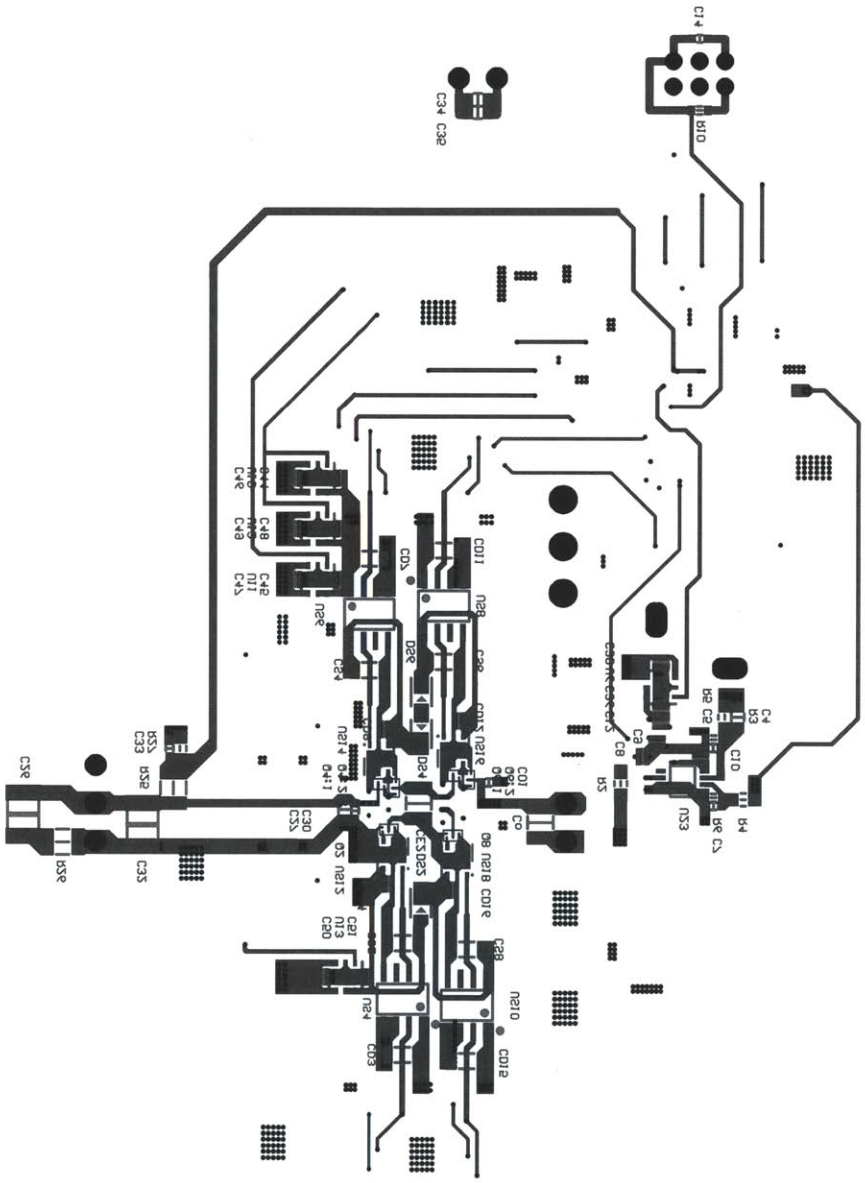


Figure A-9: two-stage architecture PCB layout layer 4.

Bibliography

[1] R. C. N. Pilawa-Podgurski, W. Li, I.L. Celanovic, and D. J. Perreault. Integrated CMOS dc-dc converter with maximum power point tracking for a portable thermophotovoltaic power generator. In *Submitted to the third annual IEEE Energy Conversion Congress and Exposition*, 2011.

[2] R. Pilawa-Podgurski, D Giuliano, and D Perreault. Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer. In *39th IEEE Power Electronics Specialists Conference*, 2008.

[3] M.D. Seeman and S.R. Sanders. Analysis and optimization of switched-capacitor dc-dc converters. In *IEEE Computers in Power Electronics Workshop*, pages 216–224, 16-19 July 2006.

[4] M.D. Seeman and S.R. Sanders. Analysis and optimization of switched-capacitor dc-dc converters. *Power Electronics, IEEE Transactions on*, 23(2):841 –851, march 2008.