

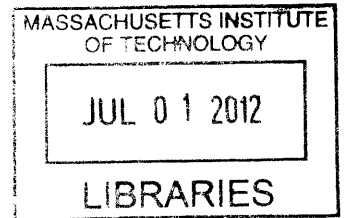
**A Continuous-Time Multi-Stage Noise-Shaping
Delta-Sigma Modulator with Analog Delay** **ARCHIVES**

by

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B.S., Electrical Engineering

Korea Advanced Institute of Science and Technology (2010)



Submitted to the Department of Electrical Engineering
in partial fulfillment of the requirements for the degree of
Master of Science in Computer Science and Engineering

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Abstract

A new continuous-time multi-stage noise-shaping delta-sigma modulator has been designed. This modulator provides high resolution and robust stability characteristics which are the primary advantages of the conventional multi-stage noise-shaping architecture. At the same time, previous critical challenges that degraded the overall performance of multi-stage noise-shaping delta-sigma modulators are eliminated through several unique techniques. Additionally, these techniques relax the requirements of each component of the proposed delta-sigma modulator. As a result, this new delta-sigma modulator architecture can provide several advantages that are not obtainable in other modulator architectures.

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Title: Professor

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Chapter 1

Introduction

Most electronic systems receive analog signals from the real world and then convert them to digital signals for processing in the digital domain. Therefore, analog-to-digital converters (ADCs) are essential in many electronic systems. In particular, modern wireless communication applications require accurate and high-speed ADCs. Such ADCs must consume low power due to the significant constraints in battery-powered wireless systems (e.g., mobile phones). For wireless applications, delta-sigma ($\Delta\Sigma$) ADCs have been used for fifty years, since the first idea of $\Delta\Sigma$ operation was presented [1], and this idea was adapted to the real ADC [2]. Among other types of ADCs, $\Delta\Sigma$ ADCs are suitable for modern wireless applications, due to their oversampling, high dynamic range (DR), and low-power consumption characteristics. Over the last decade, significant efforts have been made to increase the speed of the $\Delta\Sigma$ ADCs with high resolution and low-power consumption. As a result, many architectures for $\Delta\Sigma$ ADCs have been investigated, but they have been unable to achieve performance metrics required for next generation wireless applications. For this reason, this thesis presents a new $\Delta\Sigma$ ADC architecture that can achieve the higher resolution and signal bandwidth required by modern wireless applications.

1.1 Motivation

Wireless communication is a rapidly advancing field and new wireless applications are continuously being developed.

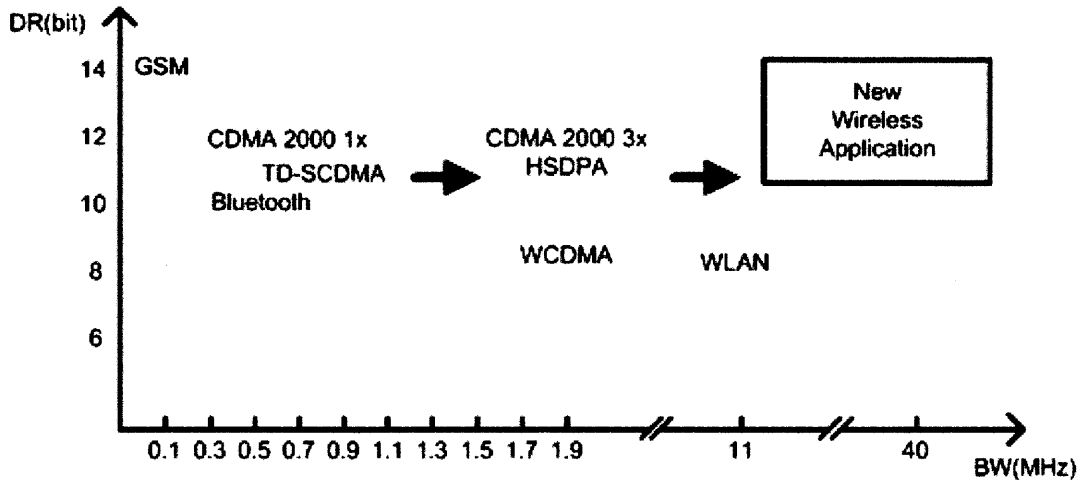


Figure 1-1: DR and signal bandwidth requirements of ADCs for different wireless applications

Figure 1-1 shows each application space and the required DR [3]. As shown in Figure 1-1, new wireless applications, such as Long Term Evolution technology, demand signal bandwidth and resolution over 50-MHz and 14 bits, respectively. At the same time, the systems for new wireless applications must consume low power due to the limited battery-power. In order to meet all these requirements, a proper type of ADCs has to be carefully chosen.

Figure 1-2 shows the DR and signal bandwidth of ADCs presented at the International Solid-State Circuits Conference and Symposium on VLSI circuits from 1997 to 2012 [4]. As shown in the figure, to achieve a DR over 70-dB, $\Delta\Sigma$ and pipelined ADC architectures are typically used. Especially, the achieved DR values of $\Delta\Sigma$ ADCs are higher in this region. When considering power consumption by using the Figure-of-Merit (FOM) as shown in Figure 1-3 [4], it is shown that $\Delta\Sigma$ ADCs have better advantages. Equation 1.1 shows how FOM can be calculated.

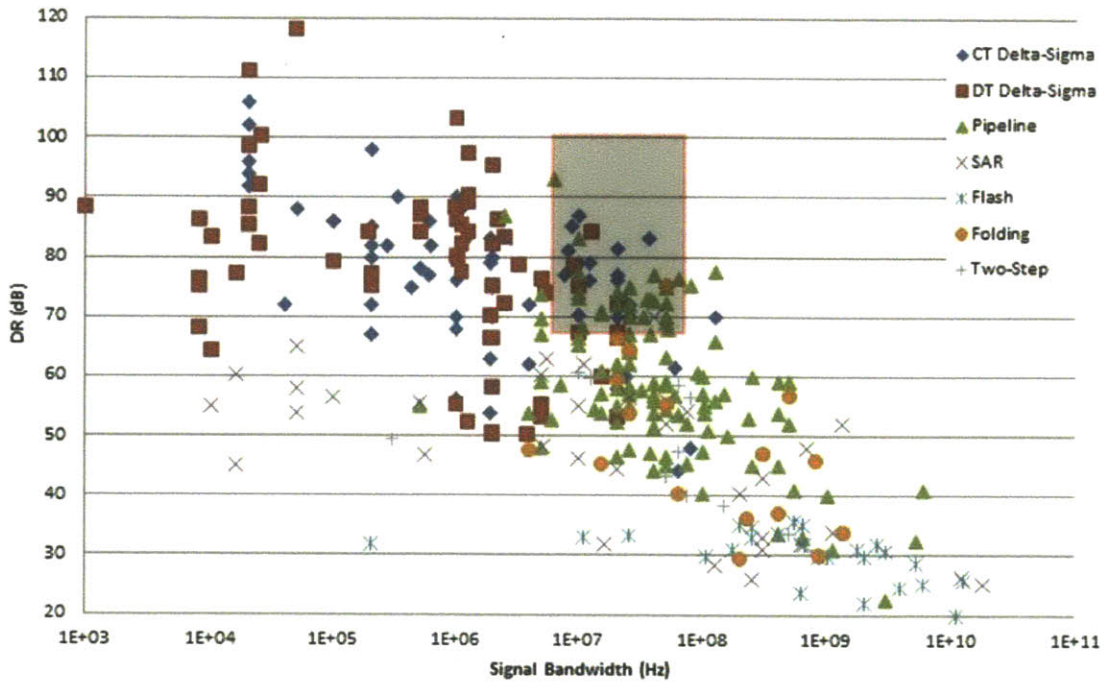


Figure 1-2: DR and signal bandwidth of different types of ADCs

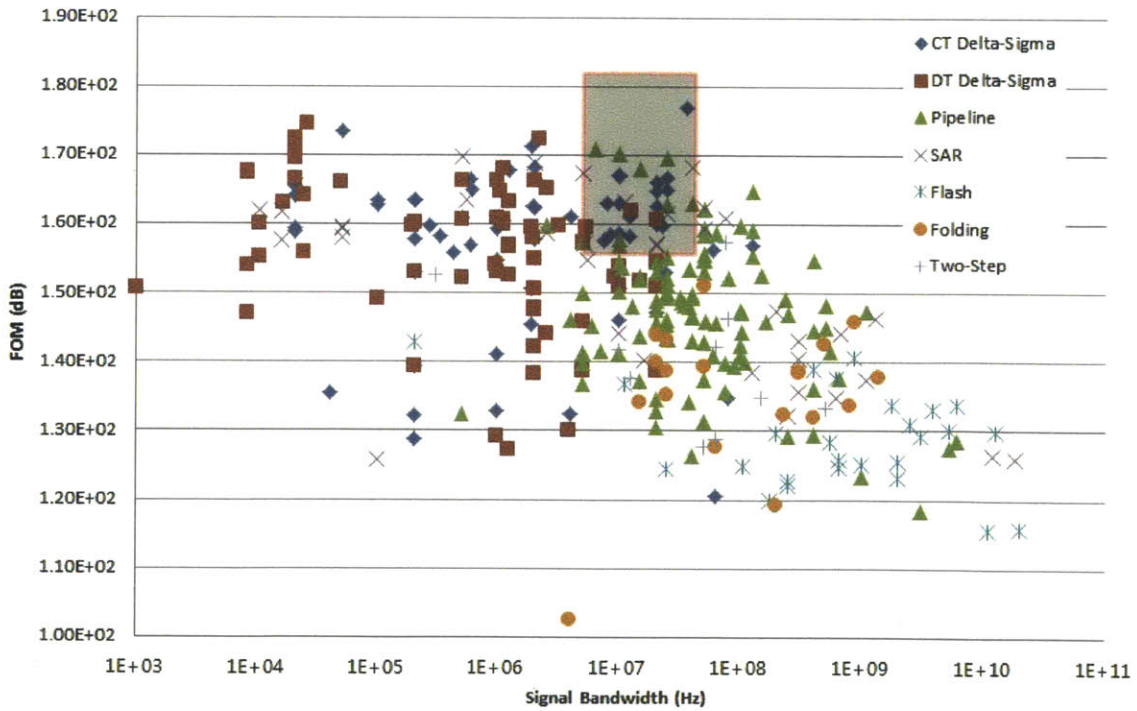


Figure 1-3: FOM and signal bandwidth of different types of ADCs

$$FOM = DR_{dB} + 10 \log\left(\frac{BW}{P}\right) \quad (1.1)$$

where P is power and BW is signal bandwidth. The higher FOM, the more power-efficient ADCs. For signal bandwidth near 20-MHz, the FOM of $\Delta\Sigma$ ADCs is generally high, while achieving the high DR. Therefore, $\Delta\Sigma$ ADCs are a suitable architecture for use in upcoming wireless applications.

ADCs can be implemented in either a discrete-time (DT) or continuous-time (CT) structure. Until recently, the majority of $\Delta\Sigma$ ADCs have been implemented in DT by using switched-capacitor(SC) techniques. Since the implementation methodologies of DT $\Delta\Sigma$ ADCs have been thoroughly examined, it is much easier to build $\Delta\Sigma$ ADCs in DT. Moreover, due to the robustness of the capacitor matching in a modern CMOS process, DT $\Delta\Sigma$ ADCs can easily provide high resolution. However, since next generation wireless applications require high speeds of operation, a renewed interest in CT $\Delta\Sigma$ ADCs is observed, as they are able to work at much higher sampling frequencies than comparable DT $\Delta\Sigma$ ADCs. The detailed advantages of CT $\Delta\Sigma$ ADCs will be described in the following chapter.

For these reasons, this thesis presents a new CT $\Delta\Sigma$ modulator architecture, which is the primary component of a CT $\Delta\Sigma$ ADC, to achieve high resolution and signal bandwidth, while consuming low power. This new architecture is designed specifically for the application of multiple-input multiple-output wireless receivers. The main goal is to achieve a 50-MHz signal bandwidth and DR 84-dB or greater, while keeping power consumption below 100-mW. Achieving this goal will solve many of the problems found in current CT $\Delta\Sigma$ modulator designs. The fundamental idea is to implement a CT multi-stage noise-shaping (MASH) $\Delta\Sigma$ modulator consisting of two stages. This structure will give additional noise suppression without introducing stability and complexity issues and will mitigate accuracy requirements of the analog loop filter at high sampling frequencies.

1.2 Thesis Organization

A new CT MASH $\Delta\Sigma$ modulator is proposed in this thesis. First, several common issues of CT $\Delta\Sigma$ modulators are presented. These issues extend to challenges in the design of an original CT MASH $\Delta\Sigma$ modulator. Finally, these issues are resolved by use of a new CT MASH $\Delta\Sigma$ modulator. Several unique advantages of the new CT MASH $\Delta\Sigma$ modulator are also presented. The thesis is organized as follows:

Chapter 2 describes the fundamentals of $\Delta\Sigma$ ADCs. CT $\Delta\Sigma$ ADCs are studied primarily to help motivate the rest of the thesis. The several issues that arise when a DT $\Delta\Sigma$ modulator is converted to a CT $\Delta\Sigma$ modulator are described as well.

Chapter 3 provides an explanation of MASH $\Delta\Sigma$ modulators, and, in particular, describes the bottlenecks of a CT MASH $\Delta\Sigma$ modulator.

Chapter 4 proposes a new CT MASH $\Delta\Sigma$ modulator based on the DT sturdy-MASH $\Delta\Sigma$ modulator. In this chapter, solutions to several challenges in the design of conventional CT MASH $\Delta\Sigma$ modulators are presented. The practical implementation of this architecture is also proposed.

Chapter 5 presents the simulation results from the proposed CT MASH $\Delta\Sigma$ modulator. Compared to other CT $\Delta\Sigma$ modulators, distinct advantages of the new architecture are proven based on the simulation results.

Chapter 6 concludes the thesis and discusses future work.

Chapter 2

Overview of a $\Delta\Sigma$ ADC

This chapter provides fundamental information about $\Delta\Sigma$ ADCs. First, oversampling and noise shaping characteristics are described. Based on these characteristics, the overall structure of $\Delta\Sigma$ ADCs is illustrated with operational descriptions. Moreover, differences between DT and CT $\Delta\Sigma$ ADCs are described, and the main advantages and issues of CT $\Delta\Sigma$ ADCs are presented to aid in understanding the rest of the thesis.

2.1 Oversampling and Noise Shaping

$\Delta\Sigma$ ADCs exploit two primary characteristics: oversampling and noise shaping. These two characteristics can be explained by fundamental analog-to-digital conversion.

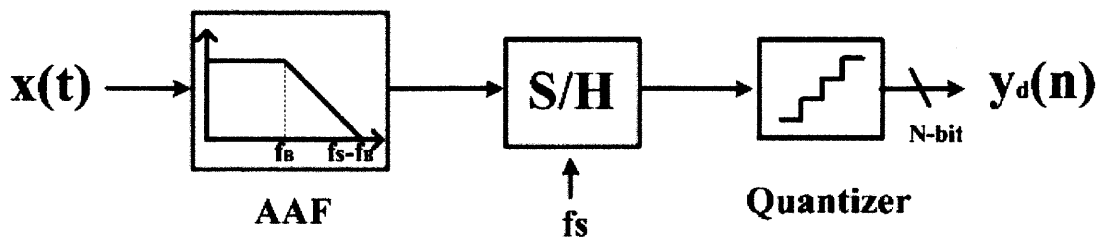


Figure 2-1: Analog-to-digital conversion

Figure 2-1 shows the blocks for analog-to-digital conversion. The process of this

conversion is to sample a CT signal, by using a sample-and-hold(SH) block, and then to assign the sampled value to one of discrete reference values, which is commonly referred to as quantization. Prior to sampling, an anti-aliasing filter(AAF) is needed to avoid high frequency components from folding into the signal bandwidth.

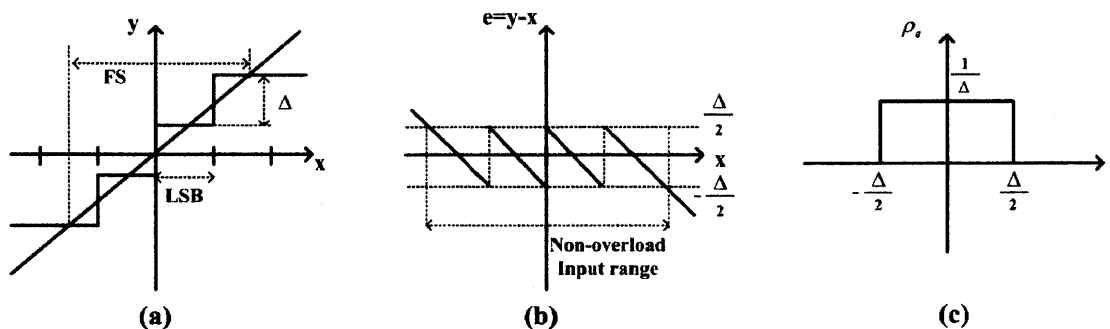


Figure 2-2: 4-level quantizer characteristics: (a) transfer curve, (b) error function, (c) probability density function

The transfer curve of an example 4-level quantizer conversion is shown in Figure 2-2(a). The least-significant bit (LSB) represents the difference between input thresholds and the quantizer step size is shown as Δ . These two values are equivalent in the sample system and are given by $\Delta \equiv \text{LSB} \equiv \text{FS}/3$, where full-scale(FS) is the maximum input range. In general, for an n -bit quantizer, the step size becomes $\Delta \equiv \text{FS}/(2^n-1)$. Compared to the ideal case $y = x$, the quantization error, e , can be found and is illustrated in Figure 2-2(b). Within the non-overload input range, given by $[-\text{FS}/2-\text{LSB}/2, \text{FS}/2+\text{LSB}/2]$, the quantization noise, e , is distributed within the range $[-\Delta, \Delta]$. As shown in Figure 2-2(b), the quantization error is directly determined by the input, but under certain circumstances [5][6][7][8], it can be modeled as white noise that is uniformly distributed in the range $[-\Delta/2, \Delta/2]$, as shown in Figure 2-2(c). Based on this probability density function, the total quantization noise power, σ_e^2 , can be calculated. Since quantization noise power is also uniformly distributed in the range $[-fs/2, fs/2]$, the power spectral density of the quantization noise is given by:

$$S_E(f) \equiv \frac{\sigma_e^2}{f_s} = \frac{1}{f_s} \left[\frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de \right] = \frac{\Delta^2}{12f_s} \quad (2.1)$$

Within the in-band frequency range, the quantization noise power is given by

$$P_E \equiv \int_{-f_B}^{f_B} S_E(f) df = \frac{2f_B \Delta^2}{12f_s} \quad (2.2)$$

where f_B represents the signal bandwidth.

2.1.1 Oversampling

According to the Nyquist Theorem, the sampling frequency, f_s , should be greater than twice f_B . Therefore, the minimum sampling frequency is $2f_B$, commonly referred as the Nyquist rate. The Nyquist rate is the sampling frequency used by Nyquist ADCs. Unlike Nyquist ADCs, oversampling ADCs such as $\Delta\Sigma$ ADCs use a sampling frequency that is much higher than $2f_B$. In this case, the oversampling ratio (OSR) is defined as $OSR = f_s/2f_B$. The main advantage of oversampling ADCs is illustrated in Figure 2-3.

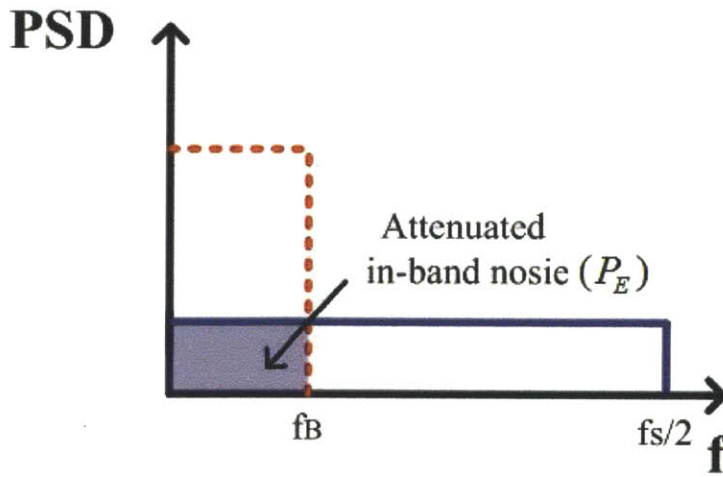


Figure 2-3: Attenuated in-band noise

Equation 2.2 shows how the in-band quantization noise relates to the oversampling characteristic directly. This equation is inversely proportional to the OSR, which means that in-band quantization noise is attenuated, for increased OSR. This is because fixed quantization noise power, σ_e^2 , is uniformly distributed in the range $[-f_S/2, f_S/2]$, as shown in Figure 2-3. Therefore, if $f_S/2$ is much greater than f_B , the eventual in-band quantization noise is reduced. Based on Equation 2.2, the in-band quantization noise power can be decreased by the OSR at a rate of 3 dB/octave. This illustrates a simple trade-off between speed and resolution. Another advantage of oversampling ADCs is that the high sampling relaxes the requirements of the AAF, since if $f_S/2$ is much greater than f_B , a sharp AAF at the input of a SH circuit is not required.

2.1.2 Noise Shaping

As described previously, high sampling frequency can reduce in-band noise, due to the oversampling characteristic. In addition, $\Delta\Sigma$ ADCs have another characteristic, noise shaping, that can further suppress in-band noise. The main idea is that a loop filter in the modulator pushes in-band noise to out-of-band frequencies.

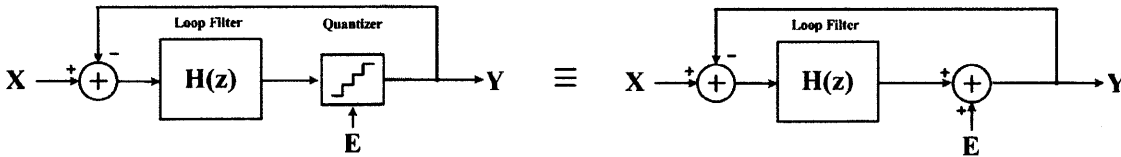


Figure 2-4: Linear model of $\Delta\Sigma$ ADCs

Figure 2-4 shows a basic block diagram of DT $\Delta\Sigma$ ADCs. It consists of a feedback system with a loop filter, $H(z)$, and a quantizer. The quantization noise, E , is directly injected at the quantizer to create a linear system model. In this case, the output is given by:

$$Y = X \cdot \frac{H(z)}{1 + H(z)} + E \cdot \frac{1}{1 + H(z)} \quad (2.3)$$

From Equation 2.3, signal transfer function (STF) and noise transfer function (NTF) can be defined:

$$STF = \frac{H(z)}{1 + H(z)} \text{ and } NTF = \frac{1}{1 + H(z)} \quad (2.4)$$

If the loop filter has extremely large gain within the in-band frequency range, STF becomes 1 and NTF becomes 0. Therefore, the input signal, X , passes through the modulator unaffected, while the quantization noise, E , is suppressed. That is, E within in-band can be shaped by the NTF. Using this characteristic to make a low-pass $\Delta\Sigma$ ADC, an integrator can be used as the loop filter. On the other hand, to create a band-pass $\Delta\Sigma$ ADC, a resonator, which has a large gain at the given center frequency, can be used.

To implement a low-pass $\Delta\Sigma$ ADC, the NTF is generally given by:

$$NTF = (1 - z^{-1})^L \quad (2.5)$$

where L denotes the order of a loop filter, $H(z)$. To calculate the in-band quantization noise power shaped by the NTF, it is necessary to find the squared magnitude of the NTF:

$$|NTF(e^{j\Omega})|^2 = |1 - e^{-j\Omega}|^{2L} = |1 - \cos(\Omega) + j \sin(\Omega)|^{2L} \quad (2.6)$$

$$= [2 - 2 \cos(\Omega)]^L = \left[2 \sin\left(\frac{\Omega}{2}\right)\right]^{2L} \quad (2.7)$$

where Ω is defined as $\Omega=2\pi f/f_s$. To calculate the real quantization noise power at

the output, the squared magnitude of the NTF is multiplied to the quantization noise power. The in-band noise power is given by:

$$P_Q \equiv \frac{1}{2\pi} \int_{-\Omega_B}^{\Omega_B} \sigma_e^2 |NTF(e^{j\Omega})|^2 d\Omega = \frac{\Delta^2}{12\pi} \int_0^{\pi/OSR} \left[2 \sin\left(\frac{\Omega}{2}\right) \right]^{2L} d\Omega \quad (2.8)$$

where Ω_B is defined as $\Omega_B = \pi/OSR$. Due to the high sampling frequency, π/OSR is, in general, very small. Within the range $[0, \pi/OSR]$, the sine term can be simplified as:

$$2 \cdot \sin\left(\frac{\Omega}{2}\right) \simeq 2 \cdot \frac{\Omega}{2} = \Omega \quad (2.9)$$

Combining Equations 2.8 and 2.9, the final in-band noise power shaped by the NTF is given by:

$$P_Q \equiv \frac{\Delta^2}{12\pi} \int_0^{\pi/OSR} (\Omega)^{2L} d\Omega = \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \quad (2.10)$$

Here, compared to using the oversampling characteristic only, the in-band noise power is attenuated more efficiently. This result is illustrated clearly in Figure 2-5. Due to the oversampling characteristic, quantization noise is uniformly distributed over the range $[-fs/2, fs/2]$, so that the in-band noise can be attenuated. The in-band noise is further suppressed by the NTF as shown in Figure 2-5.

The operation of $\Delta\Sigma$ ADCs is primarily based on these two characteristics. With a specific OSR, loop filter order, and number of bits of the quantizer, the maximum signal-to-quantization noise ratio (SQNR) can be calculated based on Equation 2.10 as follows:

$$SQNR_{\max} = 6.02N + (20L + 10)\log_{10}OSR + 1.76 - 10\log_{10}\frac{\pi^{2L}}{2L+1} [dB] \quad (2.11)$$

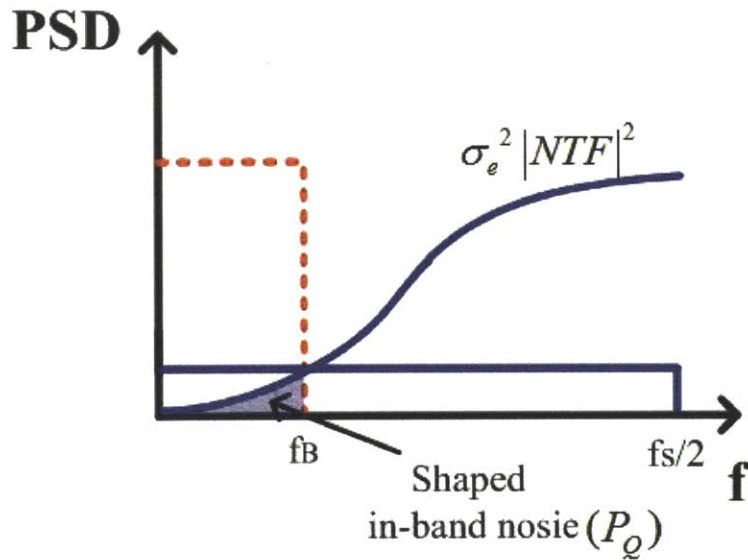


Figure 2-5: Shaped in-band noise

There are three ways to increase the resolution of $\Delta\Sigma$ ADCs: increasing the order of the loop filter, the OSR, and the number of bits of the quantizer. Each method, however, has its own associated costs. First, increasing the order of the loop filter brings about stability issues. Since a $\Delta\Sigma$ ADC is a feedback system, if the order of a loop filter is increased ($L > 2$), this system becomes conditionally stable with a limited input range [9]. Second, increasing the OSR gives rise to speed and power problems. Since the actual sampling frequency is limited, simply increasing OSR is an unacceptable solution. Moreover, if higher OSR is chosen, and a high signal bandwidth is required, each block in the $\Delta\Sigma$ ADC must consume more power to handle the faster operation speed. Finally, it is not an effective solution to significantly increase the number of bits of the quantizer, since the accuracy of a quantizer is fairly limited. Furthermore, if a multi-bit quantizer is used, non-linearities from the multi-bit digital-to-analog converters (DACs) degrade the linearity of $\Delta\Sigma$ ADCs. DAC non-linearities add directly to the input signal and therefore is not suppressed by the NTF. In this situation, increasing the order of a loop filter and then solving the stability issues is a more effective solution. Since increasing the order of the loop filter causes stability problems, alternative methods have been investigated. These

methods attempt to increase the effective order of the NTF, while maintaining a stable lower order loop filter. These methods are presented in following chapters.

2.2 Overall Structure of a DT $\Delta\Sigma$ ADC

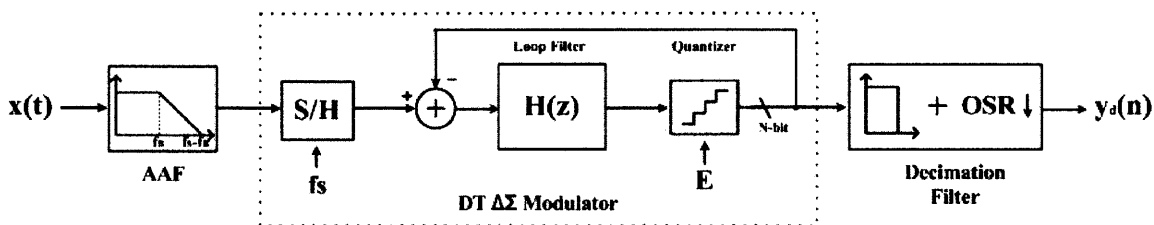


Figure 2-6: Block diagram of a DT $\Delta\Sigma$ ADC

Figure 2-6 shows the overall block diagram of a DT $\Delta\Sigma$ ADC. The overall structure of the DT $\Delta\Sigma$ ADC consists of an AAF, a DT $\Delta\Sigma$ modulator, and a decimation filter. The main characteristic of DT $\Delta\Sigma$ ADCs is that the CT signal is sampled at the input of a $\Delta\Sigma$ modulator, and the DT signal is processed in the $\Delta\Sigma$ modulator. To avoid aliasing when the signal is sampled, an AAF is required before the input of the $\Delta\Sigma$ modulator. To implement the desired NTF, a proper loop filter, consisting of switched-capacitor (SC) circuits, is needed. Since the output of a $\Delta\Sigma$ modulator is generated at the high sampling frequency, the output data frequency of the $\Delta\Sigma$ modulator should be reduced to the Nyquist rate for use in subsequent signal processing blocks. Therefore, a decimation filter is required at the output of the DT $\Delta\Sigma$ modulator, in order to realize a complete DT $\Delta\Sigma$ ADC.

2.3 CT $\Delta\Sigma$ ADC

Figure 2-7 shows the overall block diagram of a CT $\Delta\Sigma$ ADC. The main characteristic of CT $\Delta\Sigma$ ADCs is that the input of the CT $\Delta\Sigma$ modulator remains a CT signal, until it is sampled at the quantizer. Therefore, the loop filter in a CT $\Delta\Sigma$ modulator utilizes CT components such as RC and Gm-C integrators. Unlike a DT $\Delta\Sigma$ ADC, the CT

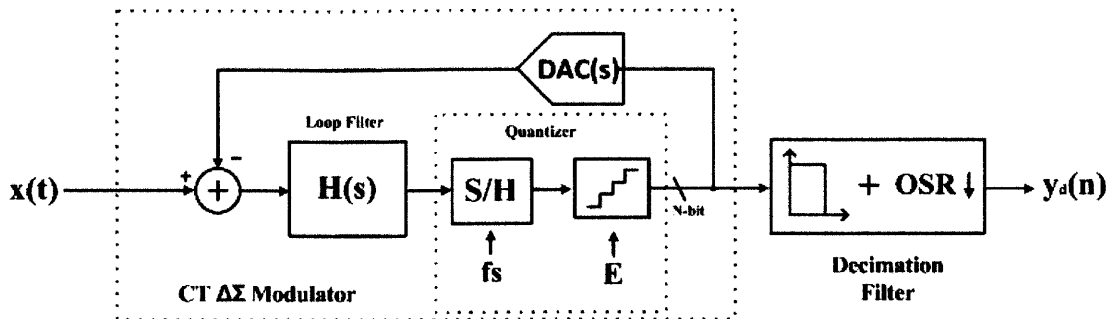


Figure 2-7: Block diagram of a CT $\Delta\Sigma$ ADC

input signal of a CT $\Delta\Sigma$ ADC can be directly fed into the CT $\Delta\Sigma$ modulator without an AAF. This is because the sampling process at a quantizer in a loop filter provides an inherent AAF [10]. However, following the CT $\Delta\Sigma$ modulator, a decimation filter is still needed. Therefore, CT $\Delta\Sigma$ ADCs consist of a CT $\Delta\Sigma$ modulator and a decimation filter only. Since an equivalent decimation filter is needed for both DT and CT $\Delta\Sigma$ ADCs, only the modulators in $\Delta\Sigma$ ADCs will be investigated.

2.3.1 Difference between DT and CT $\Delta\Sigma$ Modulators

As mentioned before, the modulators in $\Delta\Sigma$ ADCs can be implemented in either a DT or CT structure. The DT $\Delta\Sigma$ modulator, based on SC circuits, generally offers higher accuracy compared to that of the CT $\Delta\Sigma$ modulator, because this accuracy depends on precise capacitor matching, which is easily achievable by using calibration circuits or dynamic element matching. Moreover, the DT $\Delta\Sigma$ modulator is robust under process variation. However, since the DT $\Delta\Sigma$ modulator requires op-amp settling within each half-clock period, the gain-bandwidth requirement for the op-amp is rather high, such that the DT $\Delta\Sigma$ modulator consumes more power than an equivalent CT $\Delta\Sigma$ modulator. Another crucial disadvantage of DT $\Delta\Sigma$ modulators is the need for an AAF at its input.

CT $\Delta\Sigma$ modulators, however, do not use SCs, so the op-amps require much lower gain-bandwidth, therefore easing the design requirements of the op-amp. Since no

sampling is performed within the filters, the restriction of maximum sampling frequency is dependent only on the regeneration time of the quantizer and the update rate of the DAC [11]. Thus, it is possible for CT $\Delta\Sigma$ modulators to function at a higher sampling frequency and achieve wide bandwidth compared to DT $\Delta\Sigma$ modulators.

Recent wireless applications demand high bandwidth, which decreases the OSR for a fixed sampling frequency, thereby reducing resolution. Thus, to achieve wide bandwidth and maintain high resolution, it is necessary for the $\Delta\Sigma$ modulator to work at high sampling frequencies over 1-GHz. To achieve op-amp settling, the unity gain bandwidth (UGBW) of the op-amp in a DT $\Delta\Sigma$ modulator must be greater than or equal to about five times the sampling frequency [12]. Therefore, it is extremely difficult for DT $\Delta\Sigma$ ADCs to operate at sampling frequencies over 1-GHz. On the other hand, the UGBW of active-RC integrators that CT $\Delta\Sigma$ modulators use is the same as the sampling frequencies, or even below, depending on the chosen scaling coefficient [13]. Thus, CT $\Delta\Sigma$ modulators are suitable to use for high sampling frequencies to achieve wide signal bandwidth. Moreover, CT $\Delta\Sigma$ modulators consume less power while working at high sampling frequencies [14] [15] [16]. In addition, CT $\Delta\Sigma$ modulators can save additional power and circuit complexity due to their inherent anti-aliasing property. In this regard, CT $\Delta\Sigma$ modulators are more suitable to meet the demands of new wireless applications.

2.3.2 CT $\Delta\Sigma$ Modulator Implementation

The design methodology of DT $\Delta\Sigma$ modulator has been well studied. Additionally, implementation of a DT loop filter is quite straightforward, similar to implementing an active filter by using SC circuits in the z-domain. There are many convenient and useful design tools such as the $\Delta\Sigma$ toolbox based on MATLAB [17]. On the other hand, implementing a CT loop filter for a CT $\Delta\Sigma$ modulator is more complicated. This is mainly because the CT loop filter can only deal with CT signal input and output, while the target NTF in the design tool is represented by a z-transform in which only a DT signal can be represented. Therefore, the transform conversion

of a loop filter is needed in order for a CT $\Delta\Sigma$ modulator to have a same noise shaping characteristic as that of a DT $\Delta\Sigma$ modulator. Furthermore, since the output of feedback DACs is a CT signal, DACs are also represented by Laplace-transform, similar to a loop filter, as shown in Figure 2-7.

The fundamental idea in implementing a CT loop filter is to make the CT path, consisting of DACs and a CT loop filter, provide the same result as the output of a DT loop filter at the input of the quantizer at every sampling step. This process can be represented as follows:

$$H(z) = Z\{L^{-1}[DAC(s)H(s)]\left[\sum_{n=0}^{\infty} \delta(t - nT_s)\right]\} \quad (2.12)$$

Therefore, with the same digital input, if there is no difference between the output of the DT loop filter and the sampled output of the CT path, which consists of a CT loop filter and DACs. This equivalent CT path can then replace the DT loop filter.

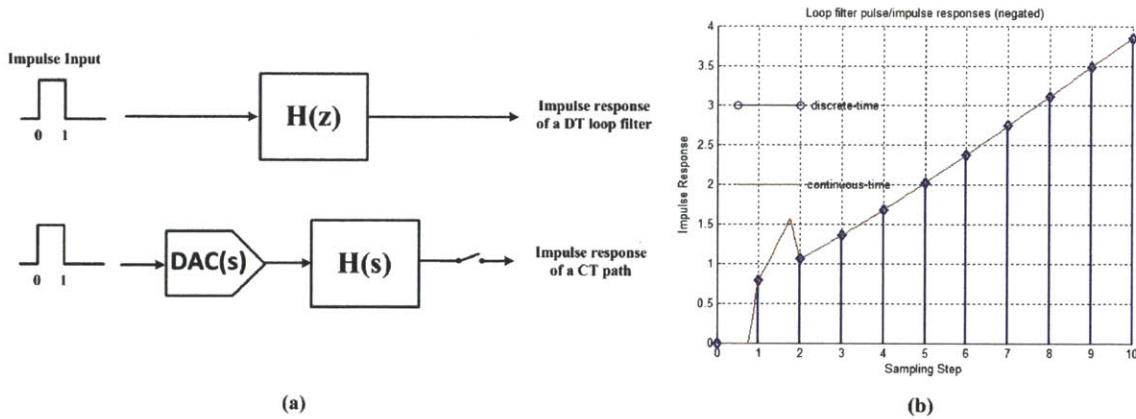


Figure 2-8: Impulse response comparison: (a) DT loop filter and CT path, (b) matched impulse response

A practical way to implement a CT loop filter is shown in Figure 2-8(a). By tuning the CT loop filter, with the given transfer function of DACs, the impulse response from a DT loop filter and a CT path can be matched. If impulse responses are well matched as shown in Figure 2-8(b) at every sampling step, this CT path shapes the

quantization noise in exactly the same manner as the DT loop filter.

2.3.3 CT $\Delta\Sigma$ Modulator Issues

In spite of the several advantages of CT $\Delta\Sigma$ modulators, such as fast speed and low power consumption, there are four main issues, especially when high sampling frequencies are exploited: (1) quantizer metastability, (2) excess loop delay (ELD), (3) multi-bit DAC non-linearity, and (4) clock jitter. The quantizer metastability issue is due to the variation in comparison time with the input signal [18]. Since the quantizer cannot generate the output instantly, to guarantee the correct outputs from the quantizer, additional delay blocks are needed at the output of quantizer. These delay blocks are simply implemented by latches, which sample the quantizer output delayed by half a clock cycle to allow the quantizer adequate settling time. The second problem is ELD, which is due to the finite transient response of the quantizer and the DAC circuits in the modulator loop filter response [19]. Moreover, the delay that occurs from each integrator due to the finite DC gain and UGBW is also considered as ELD, especially when using high sampling frequencies. ELD introduces additional parasitic poles that increase the order of both the STF and NTF, which make the modulator less stable. To compensate for ELD, several methods have been studied [20]. Among these methods, the best-known technique is to add an additional feedback path from the output of a quantizer to the input of quantizer directly in order to reduce the effect of the parasitic poles [21]. The third issue is DAC non-linearity. In general, a multi-bit DAC consists of several unit-element DACs, based on the number of bits. Ideally, each unit-element DAC is exactly the same, so the output from each unit-element DAC is also precisely matched. The real output value is the sum of all output values from all the unit-element DACs. If there is nonlinearity due to mismatch of unit-element DACs, the output of a multi-bit DAC has a nonlinear error. However, unlike a quantization error, this error cannot be suppressed by the NTF and will be directly reflected at the output of the modulator. Therefore, non-linearity of the unit-element DACs is an important issue. Many techniques have been presented to make accurate multi-bit DACs such as analog calibration [21], digital correction

[22], and dynamic element matching (DEM) [15] [23]. Among them, DEM is one of the most popular techniques. The main idea of DEM is that the thermometer output code from the quantizer is assigned to a different unit-element every time by the DEM circuitry. As a result, the fixed error from the unmatched unit-element DACs can be changed to time-varying error. By switching the assigned unit-element DACs based on the thermometer output code, this error can be modulated out of band. This is a common problem of all $\Delta\Sigma$ modulators, but it is much more serious in CT $\Delta\Sigma$ modulators, since the matching issue of current-steering DACs is worse than that of SC DT DACs. Lastly, clock jitter caused by uncertainties in the clock-signal edge can degrade the resolution of CT $\Delta\Sigma$ modulators [16]. In DT $\Delta\Sigma$ modulators, DACs move stored charge on the capacitors into the main loop within a sampling period, and this amount of charge is barely affected by the sampling period. Therefore, uncertainties in the clock-signal edge are not significant problems in the DT case. In CT $\Delta\Sigma$ modulators, however, since the output of the DACs is current, which is directly synchronized to the sampling period, if the sampling period varies, due to the uncertainties in the clock-signal edge, the amount of charge transferred also varies. Since this error occurs at the output of the DACs, it will be directly observed at the output of the CT $\Delta\Sigma$ modulator without suppression by the loop filter. Clock jitter error occurs at the quantizer as well, but is reduced by the loop filter. The clock jitter problem can be attenuated by using a multi-bit quantizer and DAC, since the amount of charge injected between each level is reduced.

Chapter 3

Multi-Stage Noise-Shaping $\Delta\Sigma$ Modulator

The order of a loop filter is one of the critical factors used to improve the resolution of $\Delta\Sigma$ modulators. However, there is less freedom to increase the order of a loop filter, because stability compromises signal-to-noise ratio (SNR). Therefore, a large number of architectures have been explored to improve the effective order of the NTF, instead of simply increasing the order of the loop filter. One of best-known architecture is multi-stage noise-shaping (MASH), which can help circumvent this stability issue, while achieving high-order noise shaping [24] [25].

3.1 Block Diagram

Figure 3-1 conceptually shows a MASH $\Delta\Sigma$ modulator. A MASH $\Delta\Sigma$ modulator consists of several stages. Each stage consists of a stable, relatively low-order $\Delta\Sigma$ modulator. The input signal is fed into the 1st-stage, and the quantization noise of the 1st-stage, E_1 , is extracted. This extracted quantization noise is injected into the 2nd-stage. The input of each following stage is the quantization noise of the previous stage. Finally, outputs from N stages are digitally filtered, and the real output is generated. This digital filter manipulates outputs from N stages so that all the quantization noise, except for the quantization noise of the last stage, can

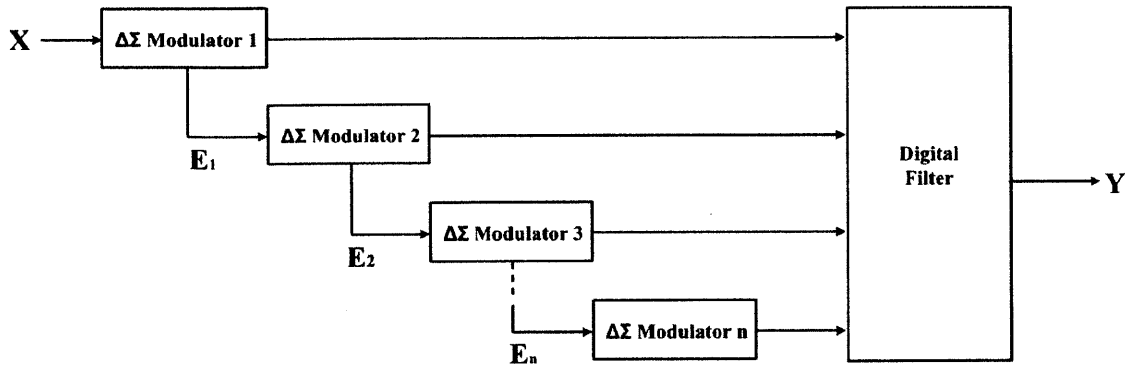


Figure 3-1: n-stage MASH $\Delta\Sigma$ modulator

be canceled. The quantization noise of the last stage is therefore suppressed by the order of all the stages in the cascade. Since the $\Delta\Sigma$ modulator within each stage has its own feedback and consists of a low-order loop filter, the requirement for the stability of the entire MASH $\Delta\Sigma$ modulator is significantly relaxed, even though the final quantization noise is shaped by the high-order NTF.

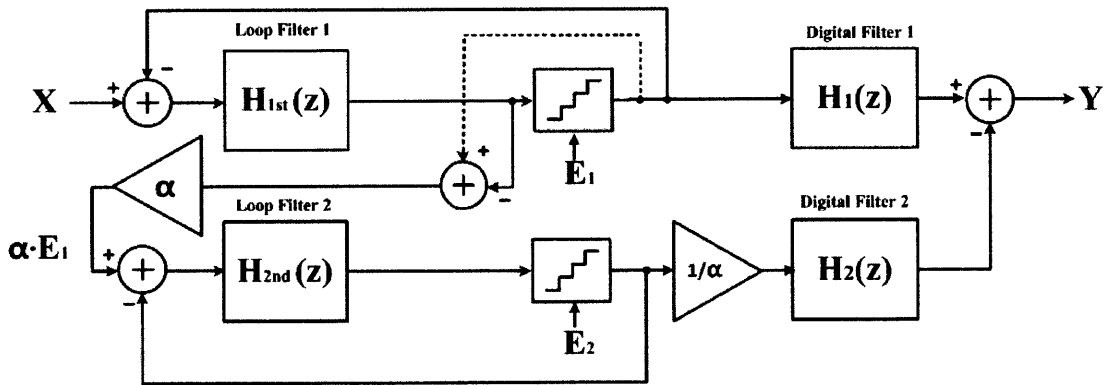


Figure 3-2: 2-stage DT MASH $\Delta\Sigma$ modulator

To examine the MASH $\Delta\Sigma$ modulator in more depth, a 2-stage DT MASH architecture is depicted in Figure 3-2. The input is fed into the 1st-stage, and the quantization noise from the 1st-stage, E_1 , is injected into the 2nd-stage. Digital filters at the quantizer outputs act to cancel E_1 and suppress the quantization noise from the 2nd-stage, E_2 , by the high-order NTF. The overall output is described by:

$$Y = (STF_1 \cdot X + NTF_1 \cdot E_1) \cdot H_1 - (STF_2 \cdot E_1 + NTF_2 \cdot E_2) \cdot H_2 \quad (3.1)$$

where $STF_1 = \frac{H_{1st}(z)}{1+H_{1st}(z)}$, $NTF_1 = \frac{1}{1+H_{1st}(z)}$, $STF_2 = \frac{H_{2nd}(z)}{1+H_{2nd}(z)}$, and $NTF_2 = \frac{1}{1+H_{2nd}(z)}$. In this modulator, if the digital filters are designed as $H_1=STF_2$ and $H_2=NTF_1$, E_1 is canceled and E_2 is shaped by $NTF_1 \cdot NTF_2$. Finally, the output of the example MASH architecture is represented by:

$$Y = STF_1 \cdot STF_2 \cdot X - NTF_1 \cdot NTF_2 \cdot E_2 \quad (3.2)$$

For an n^{th} -order 1^{st} -stage loop filter and m^{th} -order 2^{nd} -stage loop filter, the quantization noise, E_2 , is effectively suppressed by the $n + m^{th}$ -order NTF. However, since the stability of each stage is determined by the order of its loop filter, the stability of the MASH $\Delta\Sigma$ modulator is limited by its highest order loop filter. Since the highest order of the loop filter is still lower than the overall order of the NTF, the MASH $\Delta\Sigma$ modulator thus circumvents the stability issue. Therefore, compared to the original $\Delta\Sigma$ modulator with a $n + m^{th}$ -order loop filter, the MASH $\Delta\Sigma$ modulator can be much more stable. Increased stability with high-order noise shaping is the primary advantage of a MASH $\Delta\Sigma$ modulator.

In addition to the noise shaping advantage, E_2 can be further suppressed by using the gain blocks shown in Figure 3-2. Since the input of the 2^{nd} -stage is the quantization noise, whose magnitude is much smaller than the FS of the normal input, this quantization noise can be scaled up using gain blocks, which have a gain-of-alpha factor. These blocks are located at the input of the 2^{nd} -stage. With the fixed FS of the quantizer in the 2^{nd} -stage, the scaled E_1 is quantized and then becomes restored to its original magnitude by using another gain block. Through this process, the effective quantization noise from the 2^{nd} -stage is reduced.

3.2 NTF of a MASH $\Delta\Sigma$ Modulator

The stability advantage is directly reflected by the overall NTF of a MASH $\Delta\Sigma$ modulator.

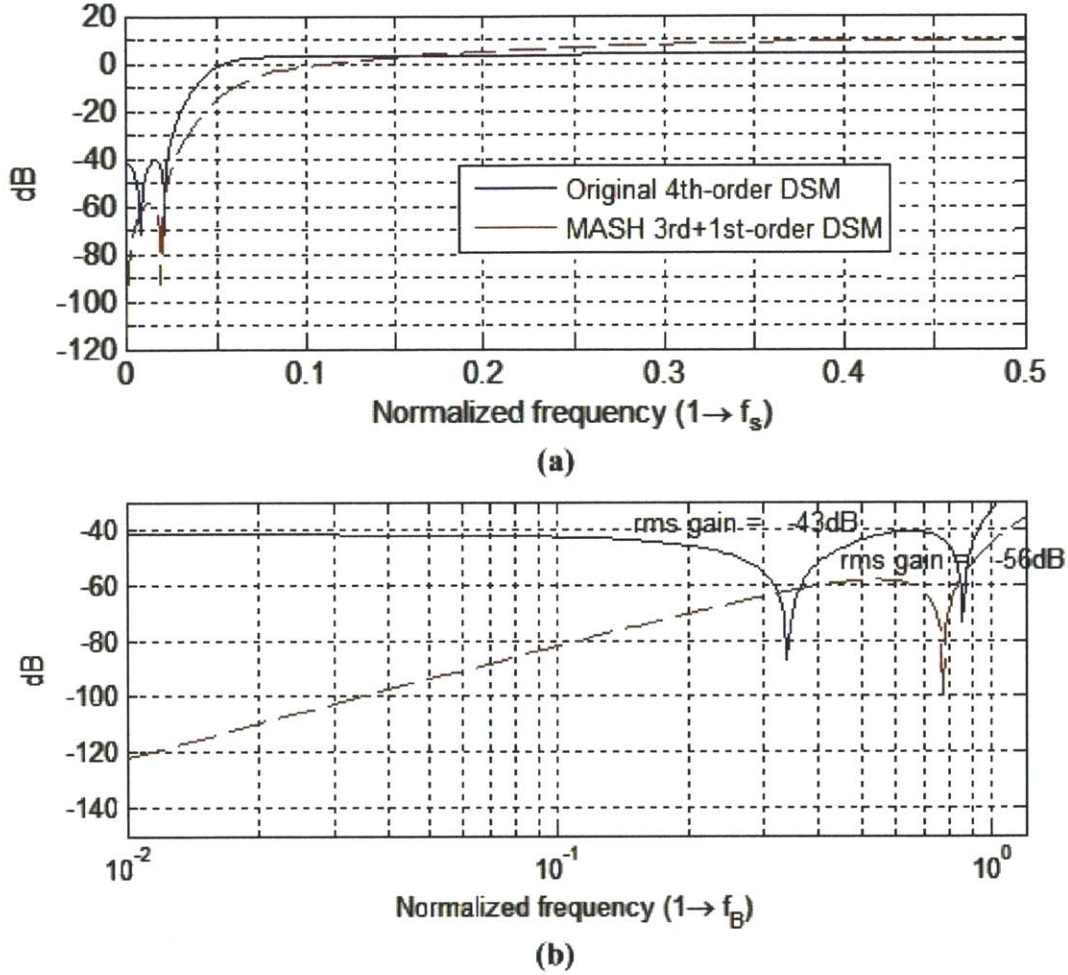


Figure 3-3: NTF graphs of an original 4th-order $\Delta\Sigma$ modulator and a MASH 3rd+1st-order $\Delta\Sigma$ modulator: (a) overall NTF, (b) NTF within the in-band frequency

Figure 3-3(a) shows the overall NTF magnitude of the original $\Delta\Sigma$ modulator and the MASH $\Delta\Sigma$ modulator. The blue graph represents the original 4th-order $\Delta\Sigma$ modulator, and the red graph represents the MASH $\Delta\Sigma$ modulator consisting of a 3rd-order 1st-stage and a 1st-order 2nd-stage.

As shown in Figure 3-3(b), the NTF of the MASH $\Delta\Sigma$ modulator can be much

lower within the in-band frequency range. The in-band rms gain is calculated, and the NTF of the MASH $\Delta\Sigma$ modulator suppresses in-band noise by additional 13-dB. This is because the primary stability of the MASH $\Delta\Sigma$ modulator is related to the 1st-stage with a 3rd-order loop filter, which is more stable than a 4th-order loop filter. On the other hand, the stability of the original $\Delta\Sigma$ modulator is related to the higher-order 4th-order loop filter. As a result, it is possible for a MASH $\Delta\Sigma$ modulator to use a more aggressive NTF.

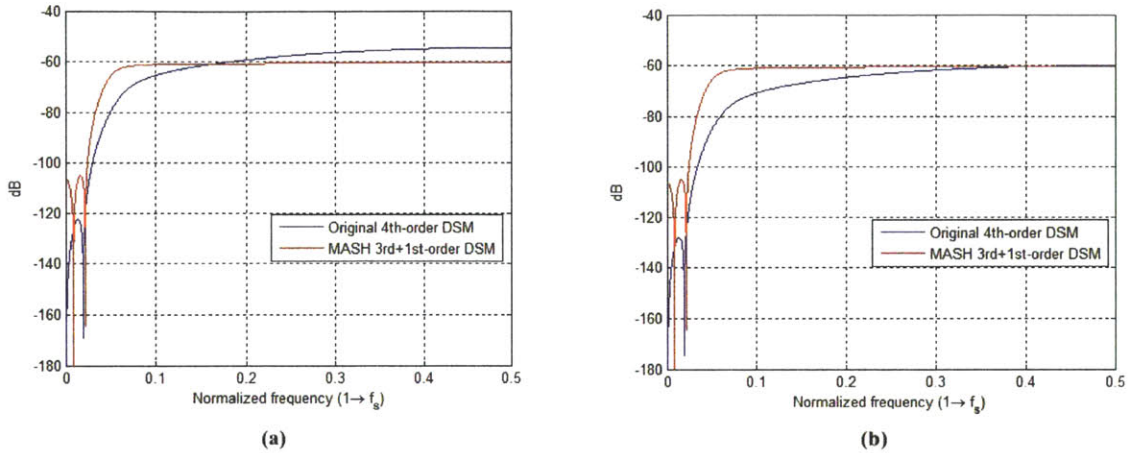


Figure 3-4: NTF graphs of an original 4th-order $\Delta\Sigma$ modulator and a MASH 3rd+1st-order $\Delta\Sigma$ modulator: (a) NTF with a 4-bit quantizer, (b) NTF with a 4-bit quantizer and gain blocks

The NTF of the MASH $\Delta\Sigma$ modulator can be further improved if gain blocks are used, as shown in Figure 3-4. First, the overall NTFs are redrawn by considering a 4-bit quantizer. Since E_1 is canceled and E_2 is reduced with gain blocks, the overall magnitude is further reduced. When a gain-of-4 factor is used, the overall NTF of a MASH $\Delta\Sigma$ modulator is lower than the NTF of an original $\Delta\Sigma$ modulator, not only within the in-band frequency range, but also at the out-of-band frequency range.

In summary, a MASH $\Delta\Sigma$ modulator has three main advantages compared to the original $\Delta\Sigma$ modulator with the same effective NTF order. First, the NTF of a MASH $\Delta\Sigma$ modulator can suppress in-band noise more aggressively. Second, the quantization noise itself can be reduced by gain blocks. Finally, the stability issue of the 2nd-stage is truly dependent on a low-order $\Delta\Sigma$ modulator, which has better

stability. However, these advantages can be obtained, only if digital filters are well matched to analog filters. This matching requirement causes several practical issues that degrade the performance significantly. This problem is presented in the following section.

3.3 CT MASH $\Delta\Sigma$ Modulator

So far, only the DT MASH $\Delta\Sigma$ modulator has been discussed. However, as mentioned in the previous chapter, to achieve high resolution at high sampling frequencies, the MASH architecture can be implemented in CT. However, it is not straightforward to convert DT loop filters to CT loop filters as mentioned in the previous chapter.

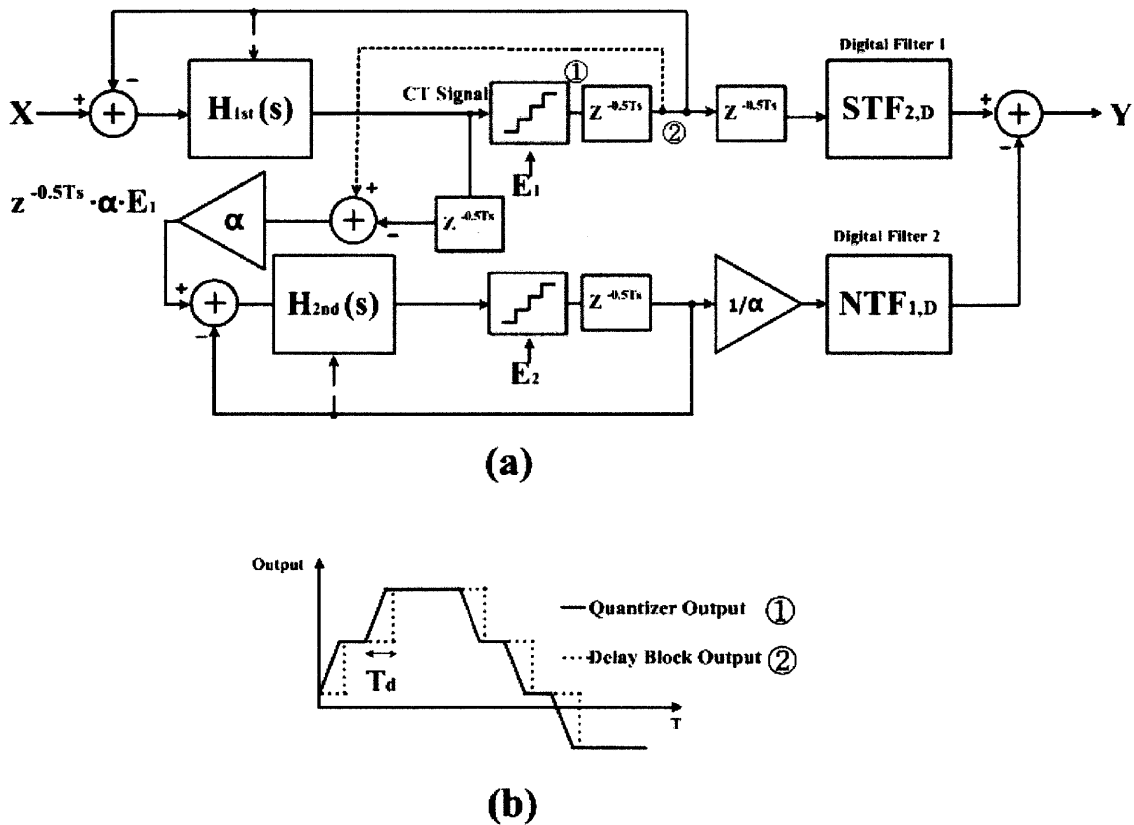


Figure 3-5: Block diagram of a CT 2-stage MASH $\Delta\Sigma$ modulator: (a) block diagram, (b) output of a quantizer and a delay block

Figure 3-5(a) shows the overall block diagram of a CT 2-stage MASH $\Delta\Sigma$ modula-

tor, which is comparable to the previous DT 2-stage MASH $\Delta\Sigma$ modulator shown in Figure 3-2. This block diagram not only highlights the difference from a DT MASH $\Delta\Sigma$ modulator, but also the main issues of a CT MASH $\Delta\Sigma$ modulator.

First, the loop filters are replaced by CT elements, based on the impulse response matching technique, mentioned in the previous chapter. Additionally, delay blocks are required at the output of the quantizers. Since the quantizer cannot generate its output instantly as shown in Figure 3-5(b), a delay block such as a latch provides enough time for the quantization output to settle. The delay time is usually less than one sampling clock period and in this block diagram, half a clock period is used. Use of the delay block brings about two issues. First, this intentional delay, which can be considered ELD, should be compensated to make the $\Delta\Sigma$ modulator stable. Therefore, another feedback path, represented by a dashed line toward each loop filter, is added. The second issue is that since the manipulable output of a quantizer is obtained with a delay, the extractable quantization noise should be delayed as well. To generate a correct delayed quantization noise, the input of quantizer needs to be also delayed. For this reason, another delay block is added at the input of the quantizer. However, since the input of the quantizer is a CT signal, in order to delay this signal, a SH circuit or an analog delay line is required. The sampled signal from a SH circuit can then be delayed by a half or a full clock period. The issue here is that it is difficult to implement an accurate SH circuit for sampling frequencies over 1-GHz. Also, since the SH circuit is added directly to the output of the loop filter, the loading effects from the SH circuit could cause negative effects on the original loop filter. Analog delay line with a precise delay is also difficult to implement.

The most serious problem of CT MASH $\Delta\Sigma$ modulators occurs at the digital filters. In Figure 3-5(a), digital filters are designed as STF_2 and NTF_1 , respectively. In order to cancel E_1 , digital filters should be well matched with the analog filters. If the digital filters are not well matched, the output of the CT MASH $\Delta\Sigma$ modulator is given by:

$$\begin{aligned}
Y = & \quad STF_{1,A} \cdot STF_{2,D} \cdot X + (NTF_{1,A} \cdot STF_{2,D} - STF_{2,A} \cdot NTF_{1,D}) \cdot E_1 \\
& \quad - NTF_{1,D} \cdot NTF_{2,A} \cdot E_2
\end{aligned} \tag{3.3}$$

Subscript A and D represent the analog and digital filters, respectively. As shown in Equation 3.3, to completely cancel E_1 , $NTF_{1,D}$ and $STF_{2,D}$ must be the same as $NTF_{1,A}$ and $STF_{2,A}$, respectively. Therefore, if analog and digital filters are not well matched, the second term in this equation, cannot be fully suppressed. The uncanceled portion of E_1 then leaks to the output, degrading the SNR of the CT MASH $\Delta\Sigma$ modulator, since it is not suppressed by the high-order NTF, $NTF_1 \cdot NTF_2$. Although both analog and digital filters target matched STF and NTF to fully cancel E_1 , the analog filter transfer characteristic is modified by fabrication mismatches and other non-idealities. These non-idealities include significant RC variation and additional errors due to finite op-amp DC gain and UGBW. Therefore, $NTF_{1,A}$ and $STF_{2,A}$ resulting from the analog loop filters cannot be naturally matched to digital filters without additional calibration. Also, since the CT loop filter is used in the 2^{nd} -stage, it is difficult to implement $STF_{2,A}$ in the z -domain perfectly with a digital filter. Therefore, only an approximate $STF_{2,D}$ can be used as the digital filter, causing further mismatches between analog and digital filters.

3.4 Previous Work

Due to several issue with CT MASH $\Delta\Sigma$ modulators, there are only a few published papers with results from experimentally tested circuits [26][27][28][29]. These previous works focus mainly on matching analog and digital filters, in order to fully cancel quantization noise. Several methodologies have been explored, but since loop filters and digital filters were implemented based on the specific cascaded architectures [25] [30], there was the limitation to choose NTF. Moreover, the effect of the delay block at the output of a quantizer was ignored. Table 3.1 summarizes the

Table 3.1: Performance table of prior CT $\Delta\Sigma$ modulators

	[26]	[27]	[28]	[29]	[31]	[32]	[33]	Target
Fs(GHz)	0.36	0.208	0.16	0.34	0.64	4	3.6	2
BW(MHz)	18	10/15	10	20	20	125	36	50
DR(dB)	68	70/61	67	77	80	70	83	84
Peak SNDR(dB)	62.5	61/55	56	69	74	65	70.9	80
Power(mW)	183	10.5	68	56	20	256	15	100
Technology	0.18um	65nm	0.18um	90nm	130nm	45nm	90nm	28nm
FOM(pJ/step) ¹	4.66	0.57/0.76	6.59	0.61	0.12	0.70	0.073	0.122
FOM(pJ/step) ²	2.47	0.14/0.38	1.86	0.24	0.06	0.40	0.018	0.077
FOM(dB) ³	147.9	159.8/152.5	148.7	162.5	170	156.9	176.8	171

performance of four previous papers and recent state-of-the-art publications [31] [32] [33] with target specifications of the proposed $\Delta\Sigma$ modulator. The proposed target specifications are relevant for future wireless communication applications. There are three different types of FOMs: $FOM^1 = \frac{P}{2 \cdot BW \cdot 2^{\frac{SNDR-1.76}{6.02}}}$, $FOM^2 = \frac{P}{2 \cdot BW \cdot 2^{\frac{DR-1.76}{6.02}}}$, and $FOM^3 = DR_{dB} + 10 \log(\frac{BW}{P})$, when SNDR represents the signal-to-noise and distortion ratio. As shown in this table, due to several limitations of the previous publications, adequate DR and FOM for the target specification were not achieved.

Therefore, to meet all design requirements, a new CT $\Delta\Sigma$ modulator architecture needs to be developed. In the following chapter, a new CT $\Delta\Sigma$ modulator is presented based on a modified MASH architecture.

Chapter 4

A New CT MASH $\Delta\Sigma$ Modulator

The ideal MASH $\Delta\Sigma$ modulator provides several significant advantages. Specifically, it allows for a high-order noise shaping characteristic with improved stability. In spite of its advantages, the MASH $\Delta\Sigma$ modulator has seen limited use, since physical MASH $\Delta\Sigma$ modulator implementations often encounter many practical problems. In particular, CT MASH $\Delta\Sigma$ modulators have several problems mentioned in the previous chapter, such as delaying CT signal and matching filter requirements. In this chapter, a new CT MASH $\Delta\Sigma$ modulator, which circumvents the critical problems of conventional CT MASH $\Delta\Sigma$ modulators is proposed. The goal of the proposed $\Delta\Sigma$ modulator is to suppress quantization noise such that it does not limit the target resolution and bandwidth, 84-dB and 50-MHz respectively, for the intended application. At the same time, this $\Delta\Sigma$ modulator eases the requirements of its component matching. To demonstrate the concept, a CT 2-stage MASH architecture with a 4th-order overall NTF is designed for the proposed CT MASH $\Delta\Sigma$ modulator. In the 1st-stage, a 3rd-order loop filter is used, and a 1st-order loop filter is used in the 2nd-stage.

4.1 DT Sturdy-MASH $\Delta\Sigma$ Modulator

The most serious problem of MASH $\Delta\Sigma$ modulators is the matching issue between analog and digital filters. If these two filters are not well matched, the quantization noise from the 1st-stage cannot be completely eliminated. Since the actual analog filter

transfer function is sensitive to fabrication tolerances, special methods are needed for MASH $\Delta\Sigma$ modulators to achieve matched analog and digital filters. Under such methods, either the analog or digital filters must be calibrated. To do this, additional circuitry is needed to implement calibration algorithms, causing design complexity. To avoid this problem, a new MASH architecture, referred to as sturdy-MASH [34], was proposed. The block diagram of a sturdy-MASH $\Delta\Sigma$ modulator is shown in Figure 4-1.

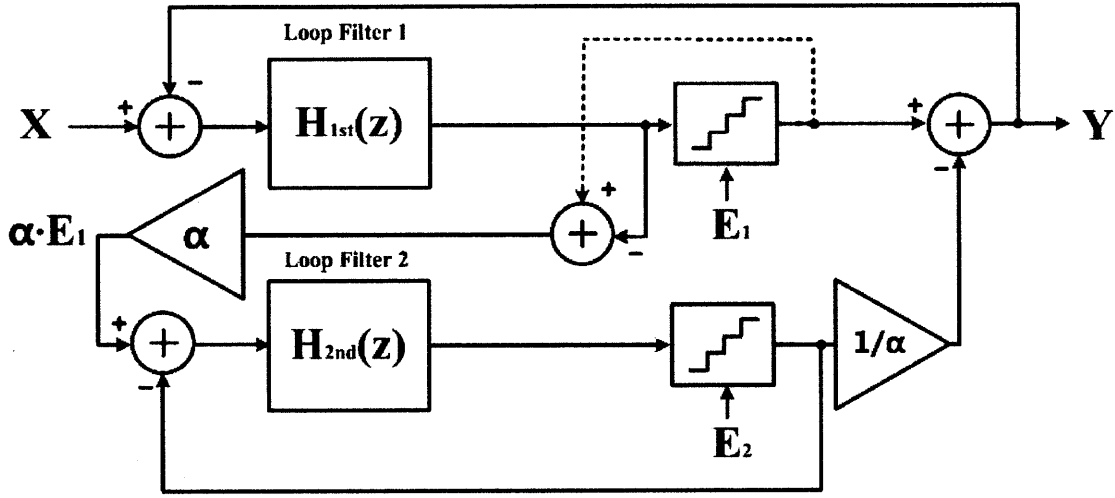


Figure 4-1: Block diagram of a sturdy-MASH $\Delta\Sigma$ modulator

Based on Figure 4-1, the output transfer function is represented by:

$$Y = STF_1 \cdot X + NTF_1 \cdot [E_1 - (STF_2 \cdot E_1 + NTF_2 \cdot E_2)] \quad (4.1)$$

$$= STF_1 \cdot X + NTF_1 \cdot (1 - STF_2) \cdot E_1 - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.2)$$

In this equation, the quantization noise from the 1st-stage, E_1 is not eliminated, unlike E_1 of a conventional MASH $\Delta\Sigma$ modulator. However, if the 2nd-stage is designed such that $(1-STF_2)$ is equal to NTF_2 , the output transfer function is given by:

$$Y = STF_1 \cdot X + NTF_1 \cdot NTF_2 \cdot E_1 - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.3)$$

Thus, E_1 and E_2 can be simultaneously shaped by $NTF_1 \cdot NTF_2$, which is of the same order NTF as a conventional MASH $\Delta\Sigma$ modulator.

For example, NTF_1 , NTF_2 , and STF_2 in [34] are given by:

$$NTF_1 = \frac{(1 - z^{-1})^2}{1 - z^{-1} + 0.5z^{-2}}, \quad NTF_2 = (1 - z^{-1})^2, \quad \text{and} \quad STF_2 = (1 - z^{-1})^2 \quad (4.4)$$

Therefore, the overall NTF, which suppresses E_1 and E_2 , is given by:

$$NTF_{overall} = \frac{(1 - z^{-1})^4}{1 - z^{-1} + 0.5z^{-2}} \quad (4.5)$$

[34] uses a 2-stage structure with a 2^{nd} -order loop filter used in each stage. As a result, the overall NTF becomes 4^{th} -order. Quantization errors, E_1 and E_2 , are suppressed by the 4^{th} -order NTF, but stability of the entire modulator is dictated by the 2^{nd} -order loop filter, which is inherently more stable.

Equation 4.3 shows that a sturdy-MASH $\Delta\Sigma$ modulator can provide the same advantage that an original MASH $\Delta\Sigma$ modulator. Theoretically, the only disadvantage is that since E_1 cannot be perfectly eliminated, there is a 3-dB degradation in SQNR, assuming E_1 and E_2 are uncorrelated. By paying this cost, quantization noises, E_1 and E_2 , are suppressed by the high-order NTF, $NTF_1 \cdot NTF_2$ without requiring digital filters matched to analog transfer functions. Although the $\Delta\Sigma$ modulator shown is implemented in DT, the advantages of a sturdy-MASH architecture can also be exploited in CT. A CT MASH $\Delta\Sigma$ modulator based on the DT sturdy-MASH $\Delta\Sigma$ modulator is thus developed further in the next section.

4.2 Main Challenges and Solutions of a CT MASH $\Delta\Sigma$ Modulator

Although a DT sturdy-MASH $\Delta\Sigma$ modulator can suppress quantization noise with a relatively high-order NTF, because it is implemented in DT, the use of high sampling frequencies to achieve increased signal bandwidth is significantly restricted. Since the achievable signal bandwidth of a DT sturdy-MASH $\Delta\Sigma$ modulator is below the requirements of modern wireless applications, a CT implementation is explored. The development of a CT implementation leads to several key issues, which must be resolved.

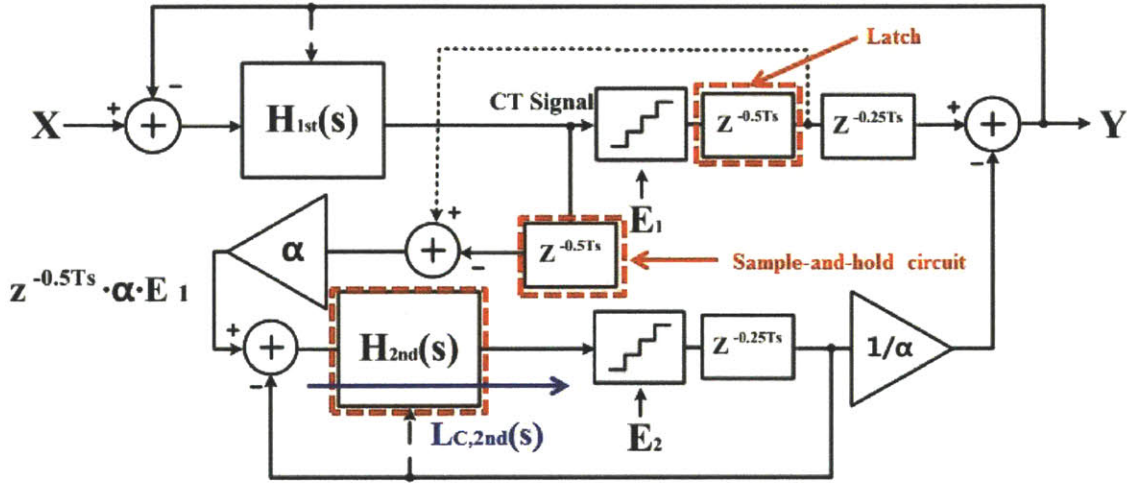


Figure 4-2: Block diagram of an early version of the new CT-MASH $\Delta\Sigma$ modulator

Figure 4-2 shows a block diagram of an early version of the new CT MASH $\Delta\Sigma$ modulator. This block diagram illustrates the main challenges in the implementation of the CT MASH $\Delta\Sigma$ modulator. The output transfer function of this $\Delta\Sigma$ modulator is given by:

$$Y = STF_1 \cdot X + NTF_1 \cdot (1 - STF_2) \cdot E_1 - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.6)$$

Equation 4.6 is similar to Equation 4.2, except that the STF in Equation 4.6

cannot be represented by a z-transform. This is due to the fact that loop filters in this $\Delta\Sigma$ modulator are implemented in CT. The NTF can be still represented by a z-transform, since the CT path from the output of the quantizer to the input of the quantizer is designed to be matched with a DT loop filter. Therefore, the STF of the CT MASH $\Delta\Sigma$ modulator must be represented differently.

$$STF_2 = L_{C,2^{nd}}(s) \cdot NTF_2(z) \quad (4.7)$$

Equation 4.7 specifically shows the actual STF_2 . Unlike the STF of DT $\Delta\Sigma$ modulators, the STF of CT $\Delta\Sigma$ modulators is represented by a Laplace-transform and a z-transform at the same time. Here, $L_{C,2^{nd}}$ is the Laplace-transform of the CT impulse response from the input of the CT loop filter to the input of the 2^{nd} -stage quantizer.

In the new CT MASH $\Delta\Sigma$ modulator, there are two main issues. The first problem is the implementation of the 2^{nd} -stage CT loop filter. In the case of the DT sturdy-MASH $\Delta\Sigma$ modulator, STF_2 was designed to equal $(1-NTF_2)$ in order to suppress E_1 with $NTF_1 \cdot NTF_2$. This is a mathematically straightforward process, since both STF and NTF are in DT. However, in the case of the new CT MASH $\Delta\Sigma$ modulator, due to the Laplace-transform term in STF_2 , STF_2 cannot be made equal to $(1-NTF_2)$ directly. Therefore, a loop filter is required to properly implement $L_{C,2^{nd}}$. The second problem is the implementation of a delay block at the input of the 1^{st} -stage quantizer. As mentioned in the previous chapter, a SH circuit is used to implement a delay block in DT, as shown in Figure 4-2. However, at high sampling frequencies, it is difficult to implement an accurate SH circuit. Moreover, a SH circuit causes loading effects on the main loop filter which degrades filter performance. These two issues are the main bottlenecks that must be solved in order to implement the new CT MASH $\Delta\Sigma$ modulator based on the DT sturdy-MASH $\Delta\Sigma$ modulator. In the following sections, with the concrete architecture of the proposed $\Delta\Sigma$ modulator, solutions to these challenges will be presented.

4.2.1 First Solution: Feedforward Path in the 2nd-Stage

The first problem can be solved, with proper design of the 2nd-stage.

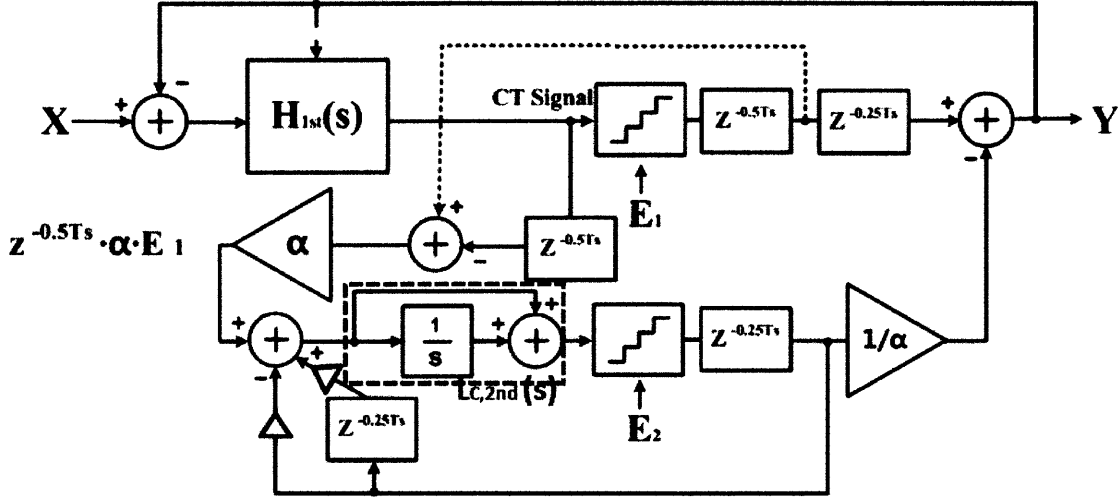


Figure 4-3: Loop filter in the 2nd-stage

Figure 4-3 shows how to correctly implement the 2nd-stage loop filter. The 2nd-stage consists of a 1st-order loop filter and target NTF of $(1-z^{-1})$. The differentiated DACs [31] are used as feedback in order to compensate for the ELD mainly due to the delay block at the output of a quantizer. A CT loop filter is implemented using one integrator with a feedforward path. This feedforward path can provide a significant advantage to help the CT loop filter issue.

$$STF_2(z) \simeq Z\{L^{-1}\{L_{C,2nd}(s)\}\} \cdot NTF_2(z) = Z\{L^{-1}\{1 + \frac{1}{s}\}\} \cdot NTF_2(z) \quad (4.8)$$

Equation 4.8 represents the STF transformed to the z -domain. Here, a Laplace-transform term from the CT loop filter is transformed to the z -domain. In this case, although exact conversion over the entire frequency range is unobtainable, the CT transfer function can be approximated to a DT transfer function over a particular range of frequencies. To do this, the DT integrator z -transform is represented in the

frequency domain as follows:

$$\frac{1}{z-1} = \frac{1}{e^{j\Omega} - 1} = \frac{1}{e^{\frac{j\Omega}{2}} \cdot (e^{\frac{j\Omega}{2}} - e^{-\frac{j\Omega}{2}})} \quad (4.9)$$

$$= \frac{1}{e^{\frac{j\Omega}{2}} \cdot \sin(\frac{\Omega}{2}) \cdot 2j} = \frac{\frac{\Omega}{2}}{e^{\frac{j\Omega}{2}} \cdot \sin(\frac{\Omega}{2}) \cdot j\Omega} \quad (4.10)$$

where Ω represents $2\pi f/f_s$. Therefore, within the frequency range which is much smaller than the sampling frequency, Ω becomes very small. In that case, the magnitude of the DT integrator is simplified by using Equation 4.10.

$$\left| \frac{1}{z-1} \right| = \left| \frac{\frac{\Omega}{2}}{e^{\frac{j\Omega}{2}} \cdot \sin(\frac{\Omega}{2}) \cdot j\Omega} \right| = \left| \frac{1}{j\Omega} \right| \cdot \left| e^{-\frac{j\Omega}{2}} \right| = \left| \frac{1}{j\Omega} \right| \quad (4.11)$$

Equation 4.11 shows that the magnitude of the DT integrator at low frequencies is equivalent to the magnitude of the CT integrator. Therefore, the z-transform of the CT integrator is approximately represented as:

$$Z\{L^{-1}\{1 + \frac{1}{s}\}\} \cdot NTF_2(z) \simeq (1 + \frac{1}{z-1}) \cdot NTF_2(z) \quad (4.12)$$

By using Equation 4.12, the STF_2 is redefined as:

$$STF_2(z) \simeq Z\{L^{-1}\{1 + \frac{1}{s}\}\} \cdot NTF_2(z) \quad (4.13)$$

$$\simeq (1 + \frac{1}{z-1}) \cdot (1 - z^{-1}) = \frac{z}{z-1} \cdot \frac{z-1}{z} = 1 \quad (4.14)$$

Equation 4.14 shows that the CT loop filter consisting of an integrator and a feedforward path can make STF_2 become 1 at low frequencies. In this situation, E_1 is removed as deserved in the ideal MASH $\Delta\Sigma$ modulator.

$$Y = STF_1 \cdot X + NTF_1 \cdot (1 - STF_2) \cdot E_1 - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.15)$$

$$= STF_1 \cdot X - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.16)$$

Since the in-band frequency of $\Delta\Sigma$ modulators is much lower than the sampling frequency, Equation 4.16 is valid over the in-band frequencies. At high frequencies, E_1 cannot be canceled, since STF_2 is no longer 1. However, quantization noise outside the signal bandwidth will be suppressed by the decimation filter following the $\Delta\Sigma$ modulator.

If there is no feedforward path in the CT loop filter, STF_2 makes a different effect. In this case, the approximated STF_2 is given by:

$$STF_2(z) \simeq Z\{L^{-1}\{\frac{1}{s}\}\} \cdot NTF_2(z) \simeq (\frac{1}{z-1}) \cdot (1 - z^{-1}) = z^{-1} = 1 - NTF_2 \quad (4.17)$$

and the overall output transfer function is represented by:

$$Y = STF_1 \cdot X + NTF_1 \cdot (1 - STF_2) \cdot E_1 - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.18)$$

$$= STF_1 \cdot X + NTF_1 \cdot NTF_2 \cdot E_1 - NTF_1 \cdot NTF_2 \cdot E_2 \quad (4.19)$$

Without the feedforward path, Equation 4.19 becomes the same as the output transfer function of a DT sturdy-MASH $\Delta\Sigma$ modulator. To verify these equations, the proposed modulator in Figure 4-3 was simulated. This modulator is implemented in CT with the proper loop filter of the 2^{nd} -stage, but with an ideal SH circuit at the input of a quantizer.

Figure 4-4 shows the signal-to-quantization-noise ratio (SQNR) from four different $\Delta\Sigma$ modulators based on H_{inf} , the maximum absolute value of the NTF. In general, a high H_{inf} value makes the NTF suppress in-band noise more aggressively. At the same time, the out-of-band noise floor increases. Added high frequency noise can lead

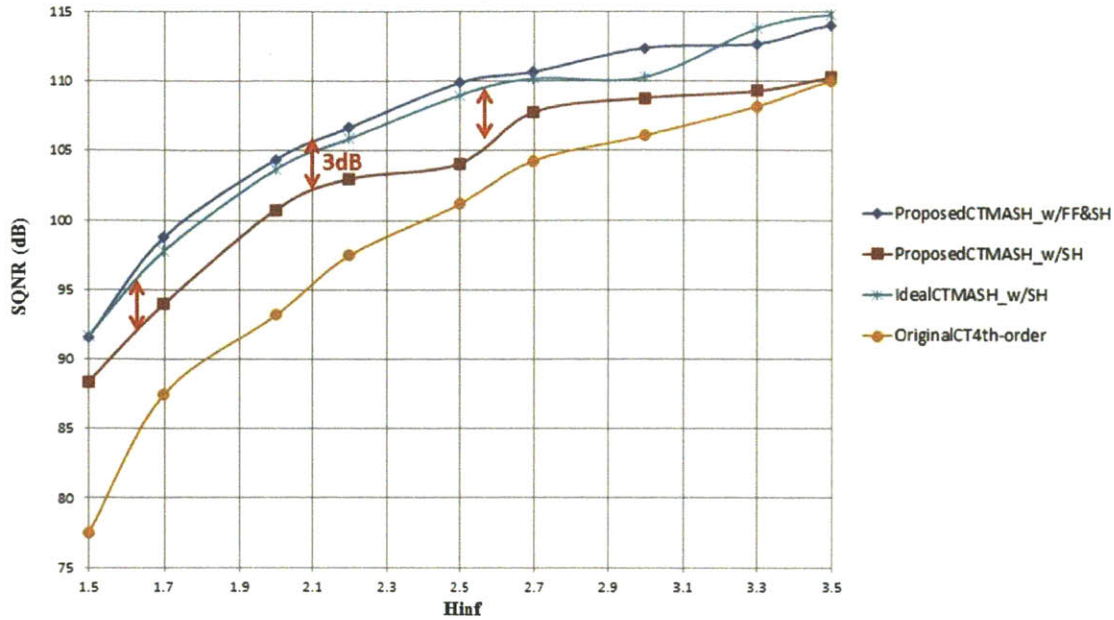


Figure 4-4: SQNR from the proposed $\Delta\Sigma$ modulator and others

to instability of the $\Delta\Sigma$ modulator. Therefore, a trade-off exists between SQNR and stability through adjustment of the H_{inf} value. The blue trace is the SQNR of the proposed new $\Delta\Sigma$ modulator described in Figure 4-3. The green trace is the SQNR of the ideal CT MASH $\Delta\Sigma$ modulator with perfectly matched analog and digital filters. The blue trace almost overlaps with the green trace, because Equation 4.16 is the same as Equation 3.2. If the feedforward path is removed, as shown in the red trace, there is 3-dB degradation compared to the blue trace. Finally, since MASH $\Delta\Sigma$ modulators achieve improved performance over the original $\Delta\Sigma$ modulator, the SQNR trace of the original non-MASH 4th-order $\Delta\Sigma$ modulator is much lower than others. In summary, using a simple 1st-order loop filter with a feedforward path allows more complete suppression of the 1st-stage quantization noise.

4.2.2 Second Solution: Analog Delay

Although the first problem can be solved by using proper loop filter design, the second problem, implementation of a delay block, still remains. Since it is difficult to design an accurate SH circuit at sampling frequencies over 1-GHz, it is necessary to create

an alternate way to delay the CT signal between the 1st and 2nd-stages.

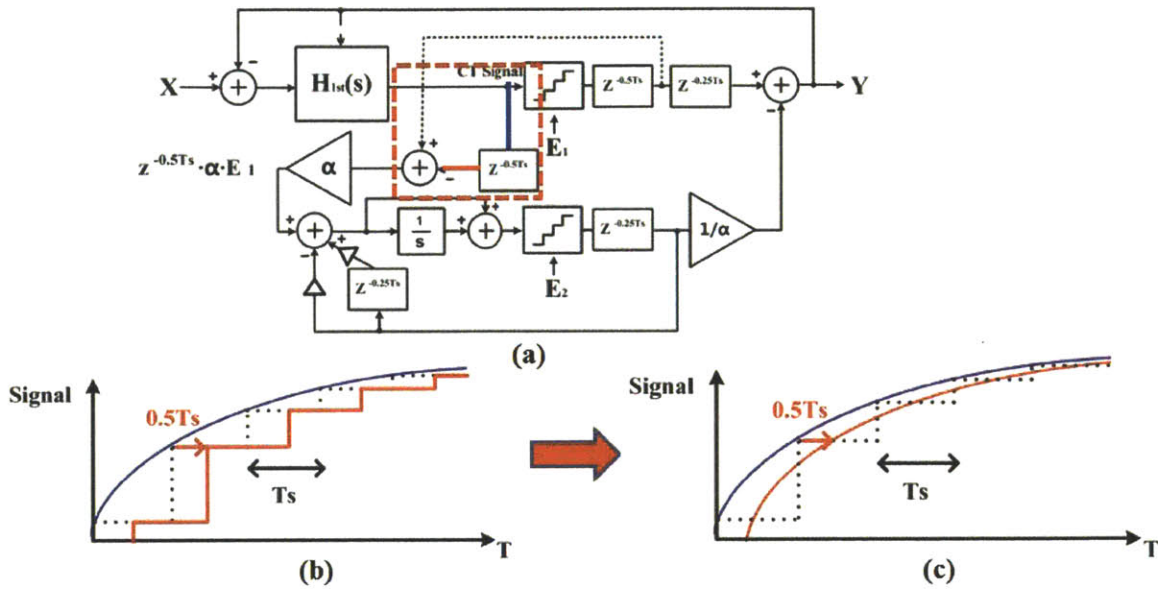


Figure 4-5: Signals at the input and output of the delay block: (a) block diagram, (b) signals from the ideal DT delay block, (c) signals from alternate block

Figure 4-5 shows the signals at the input and output of the delay block. Figure 4-5(a) illustrates the location of each signal. The blue and red lines represent the input and the output of the delay block, respectively. Figure 4-5(b) shows the ideal case, where the CT input signal is accurately sampled to create the DT signal, and then delayed by half a clock period. In this situation, instead of using a SH circuit to delay the DT signal, if the CT input signal is delayed directly as shown in Figure 4-5(c), this delayed signal can replace the red signal in Figure 4-5(b). The CT signal can be easily delayed as required in Figure 4-5(c) by using a simple low-pass filter (LPF) or an all-pass filter.

Figure 4-6 shows the CT MASH $\Delta\Sigma$ modulator with an analog delay implementation. Here, the DT delay block is replaced by a 1st-order LPF. To verify that the LPF provides constant delay to the CT signal, the characteristic of the LPF is represented by following equations. First, the output of the 1st-order LPF is represented by:

$$V_{OUT}(t) \approx A \sin(\omega_{IN}(t - RC)) = A \sin(\omega_{IN}(t - T_{delay})) \quad (4.25)$$

This indicates that the output signal is the input signal delayed by the RC, irrespective of the input signal amplitude or frequency. By matching the RC time constant with the necessary delay of one-half or one clock period, the CT signal can be accurately delayed. Referring to Figure 4-5, the input signal of the quantizer is delayed by the same amount as the quantizer delay using an LPF. With the delayed input signal, a correct delayed 1st-stage quantization error, E_1 , is fed to the 2nd-stage.

In a practical implementation, an LPF added directly to the input node of the quantizer can affect the characteristic of the loop filter, due to the loading effect. For example, since an LPF consists of a resistor and a capacitor, when attached at the input of a quantizer, it affects the loop filter transfer function and degrades the effect of the noise shaping. This problem can be avoided by integrating the LPF function into an active element such as an op-amp or a transconductor. As a result, the output signal of an active element is delayed by RC.

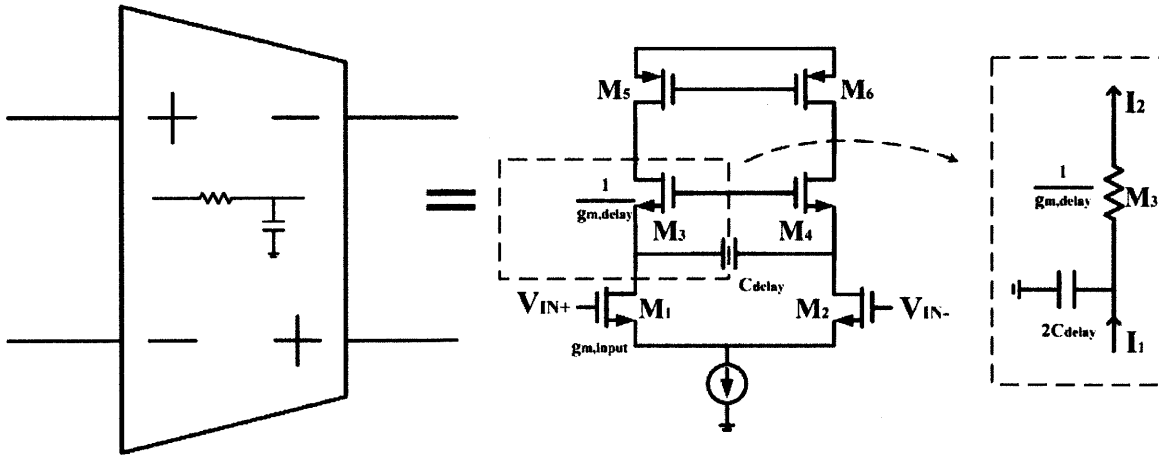


Figure 4-7: Transconductor with a built-in LPF

Figure 4-7 shows how an LPF can be absorbed into the active element. A simple operational transconductance amplifier (OTA) is used as an example. It can be shown

4.3 Overall Implementation

So far, a new CT MASH $\Delta\Sigma$ modulator has been illustrated architecturally using block diagrams. In this section, the process of implementing this $\Delta\Sigma$ modulator using real circuit components is presented. First, a schematic of the 2nd-stage is shown in Figure 4-9.

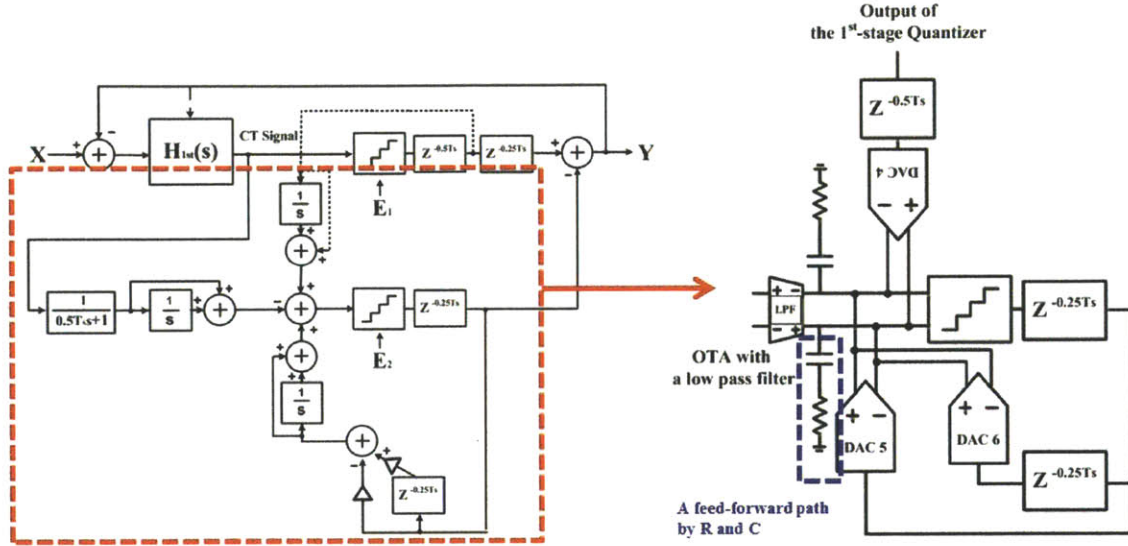


Figure 4-9: 2nd-stage implementation

This figure shows the embodiment of the new CT MASH $\Delta\Sigma$ modulator using the delay inside an OTA. By using an OTA with the delay shown above, the input signal to the 1st-stage quantizer is delayed. The outputs of the 1st and 2nd-stage quantizers are also delayed by digital latches such that the delay through the quantizer and latch matches the delay through the OTA. The feedforward path can be implemented simply by arranging a resistor and capacitor in series.

Figure 4-10 shows the overall schematic of the entire modulator. The blue and the brown dashed lines represent the 1st and the 2nd-stages, respectively. The 1st-stage has a feedforward structure consisting of two RC integrators and one Gm-C integrator [32]. The main advantage of this structure is that the input node of the quantizer becomes purely capacitive. If this node is not purely capacitively loaded, parasitic capacitance at the node creates a negative effect on the modulator in terms of speed

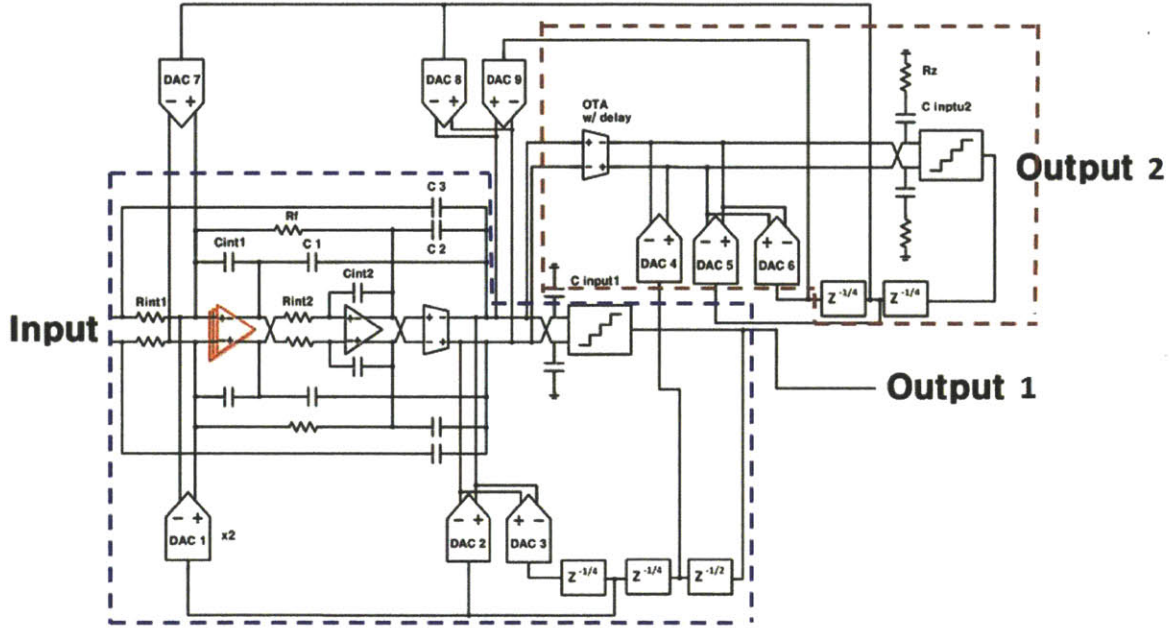


Figure 4-10: Overall schematic

and stability, especially when a high sampling frequency is used. In this structure, the parasitic capacitor can be considered as a part of the integrating capacitor, thereby eliminating the potentially negative effects of the parasitic capacitance. The 2^{nd} -stage consists of one Gm-C integrator with an internal delay as mentioned above. According to the block diagram, the actual output can be generated by a digital adder that adds output signals to both stages. However, in the real implementation, the output of the 2^{nd} -stage, *Output2*, is directly fed into the 1^{st} -stage with the original feedback path of the 1^{st} -stage. Therefore, the digital adder is no longer necessary. The total output of this modulator is generated by adding *Output1* and *Output2* digitally.

In this modulator, a special integrator is exploited as the 1^{st} -integrator in the 1^{st} -stage using a replica technique [35]. Using this technique, very high effective DC gain and reasonable UGBW can be easily achievable. This characteristic significantly improves the robustness of the $\Delta\Sigma$ modulator.

Chapter 5

Simulation Results

In this chapter, simulation results of the new CT MASH $\Delta\Sigma$ modulator are presented. Simulations mainly focus on SQNR and stability comparisons. Op-amp finite DC gain and UGBW non-idealities are considered. The simulation results prove that the proposed CT MASH $\Delta\Sigma$ modulator can provide all the advantages of CT MASH $\Delta\Sigma$ modulators, while solving several critical problems identified in CT MASH $\Delta\Sigma$ modulators. Further, simulation results show that the new CT MASH $\Delta\Sigma$ modulator provides additional unique advantages.

5.1 SQNR Comparison

Figure 5-1 shows the SQNR comparisons based on SQNR. Here, the new CT MASH $\Delta\Sigma$ modulator and an original CT MASH $\Delta\Sigma$ modulator use gain-of-4 blocks to reduce quantization noise from the 2nd-stage. The green trace shows the result of the new CT MASH $\Delta\Sigma$ modulator using an LPF to implement the required analog delay. The red trace shows the simulated SQNR of the same modulator, but utilizing an ideal SH circuit. By examining these traces, the simulated performance of the proposed CT MASH $\Delta\Sigma$ modulator is compared to the ideal result, as mentioned in the previous chapter. For values of H_{inf} up to 2.0, two traces are well matched. This means that the LPF functions well as an ideal delay circuit, within this operating regime. However, above an H_{inf} of 2.0, the proposed CT MASH $\Delta\Sigma$ modulator becomes

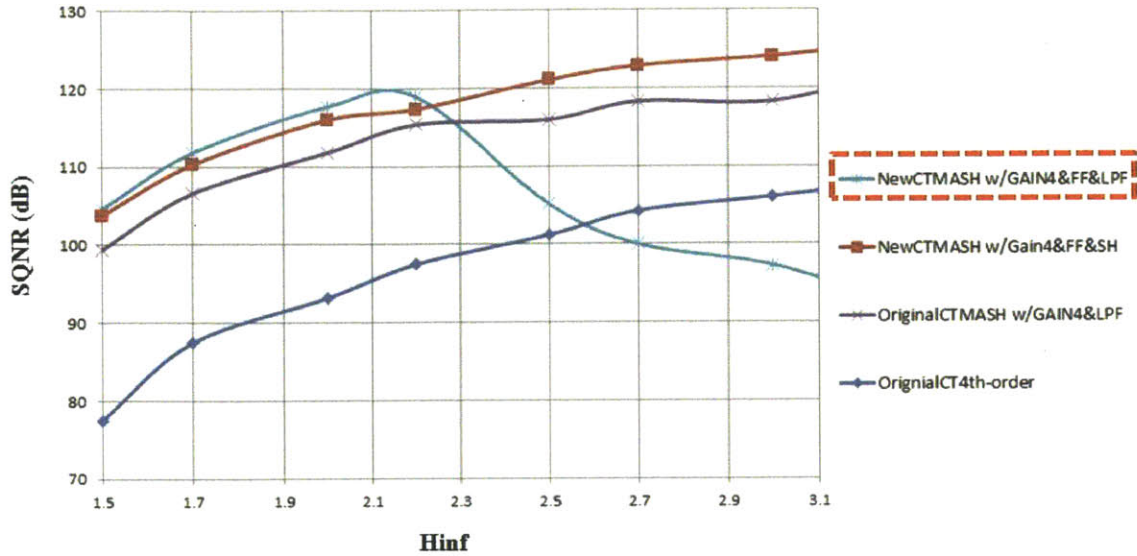


Figure 5-1: SQNR comparison

unstable, and its SQNR degrades significantly. This stability issue is explained in the following section. In addition, the purple trace, which represents the simulated SQNR of the original CT MASH $\Delta\Sigma$ modulator using the LPF, is lower than previous two traces. This is because only the ideal SH circuit can be used for the original MASH $\Delta\Sigma$ modulator to achieve complete cancellation of the quantization noise by digital filters. Although an LPF can be used in place of the ideal SH circuit, since it does not generate the same output as the ideal SH circuit, the extracted quantization noise from the 1st-stage is different from the ideal quantization noise, which results in incomplete cancellation. This brings about degradation of converter SQNR. Since the new CT MASH $\Delta\Sigma$ modulator does not require digital filters matched to analog transfer functions, the LPF does not degrade the resolution. Below Hinf value of 2.0, the MASH $\Delta\Sigma$ modulators examined here have better SQNR than the original 4th-order $\Delta\Sigma$ modulator.

5.2 Stability Issue

In Figure 5-1, the new CT MASH $\Delta\Sigma$ modulator achieve excellent SQNR for Hinf values below 2.0, but becomes unstable for Hinf values above 2.0. This result can be explained from several different view points.

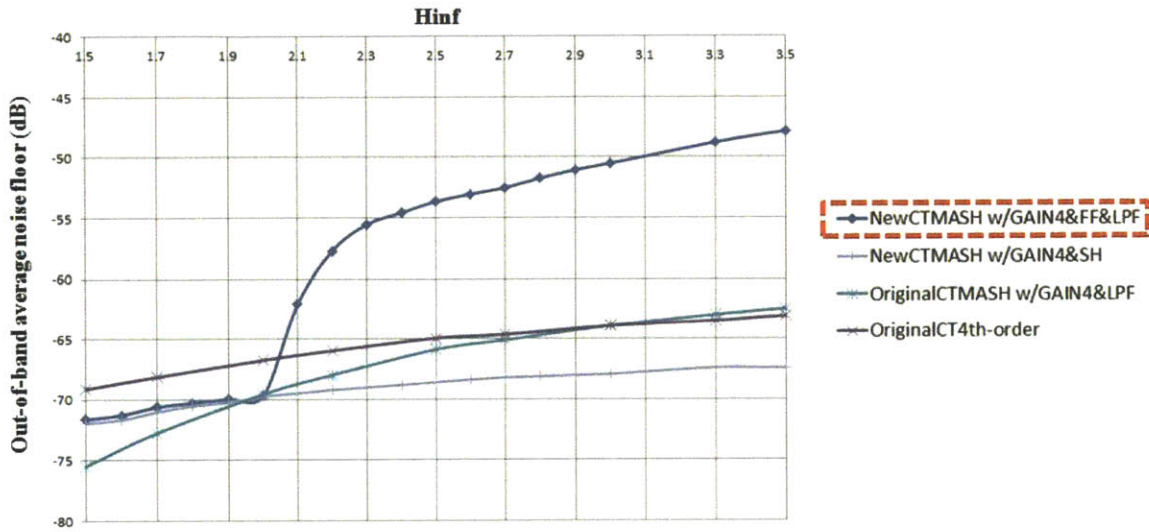


Figure 5-2: Out-of-band average noise floor comparison

Figure 5-2 shows the out-of-band average noise floor of the previous four $\Delta\Sigma$ modulators. As mentioned previously, if Hinf is increased, the out-of-band noise floor also increases. The blue trace represents the out-of-band noise floor of the new CT MASH $\Delta\Sigma$ modulator using an LPF. Again compared to the light purple trace of the same modulator using an ideal SH circuit, the noise floors of two modulators are equivalent up to an Hinf of 2.0. For Hinf below 2.0, these two traces are significantly lower than the noise floor for the original 4th-order $\Delta\Sigma$ modulator, indicating the new CT MASH $\Delta\Sigma$ modulator is more stable. However, for Hinf above 2.0, the noise floor of the new CT MASH $\Delta\Sigma$ modulator increases dramatically. This result shows that the new CT MASH $\Delta\Sigma$ modulator becomes suddenly unstable. This stability issue is due to the characteristics of the LPF.

Figure 5-3 shows input and output signals of the LPF, for different Hinf values. As Hinf increases, the input signal of the LPF, which is also the input signal of the 1st-

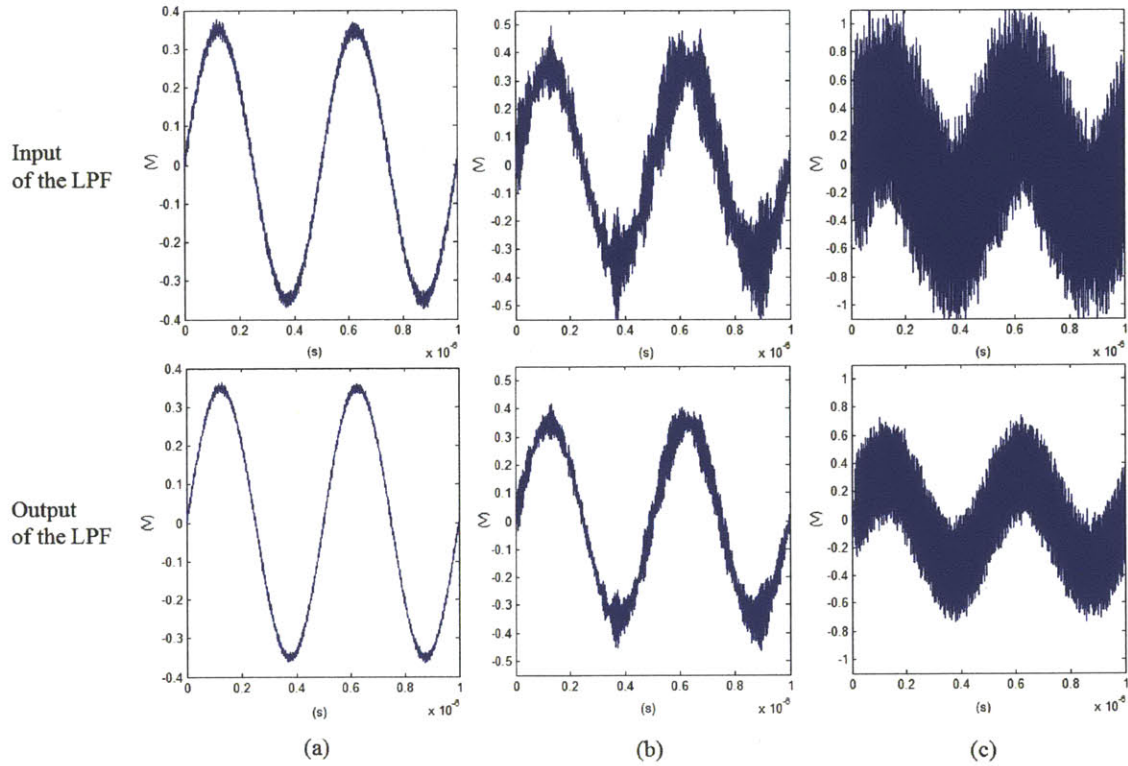


Figure 5-3: Input and output of the LPF: (a) $H_{inf}=1.5$, (b) $H_{inf}=2.0$, (c) $H_{inf}=2.5$

stage quantizer, contains more high frequency noise and deviates from the sinusoidal waveform observed for lower H_{inf} values. The purpose of the LPF is to delay the signal without affecting the signal magnitude. However, if the input signal contains large high frequency components, these are filtered by the LPF. Therefore, the signal magnitude at the output of the LPF is altered, and the LPF no longer acts as a simple analog delay element. This effect is shown in Figure 5-3(b) and (c), for higher values of H_{inf} . In this case, a significant difference between the input and output waveforms of the LPF generates an incorrect 2^{nd} -stage input signal which cannot be eliminated later. Moreover, once the modulator can no longer handle the difference, it becomes unstable. This problem may be addressed by employing an all-pass filter instead of an LPF, although its implementation is not as straightforward. However, for low H_{inf} values, the LPF sufficiently works as an ideal SH circuit, and the modulator remains stable. Even at low H_{inf} values, the new CT MASH $\Delta\Sigma$ modulator can provide large

SQNR for the target application. Therefore, the stability issue associated with the new CT MASH $\Delta\Sigma$ modulator for high H_{inf} values is not a significant concern.

5.3 Finite DC Gain and UGBW

In this section, finite DC gain and UGBW are considered as non-ideality factors. If these two factors are too low, they cause additional errors and can lead to SQNR degradation or instability. However, these factors cannot be increased without bound due to the power budget and technology limitations. Therefore, it is important to find reasonable DC gain and UGBW values that only marginally degrade system performance, while consuming minimal power.

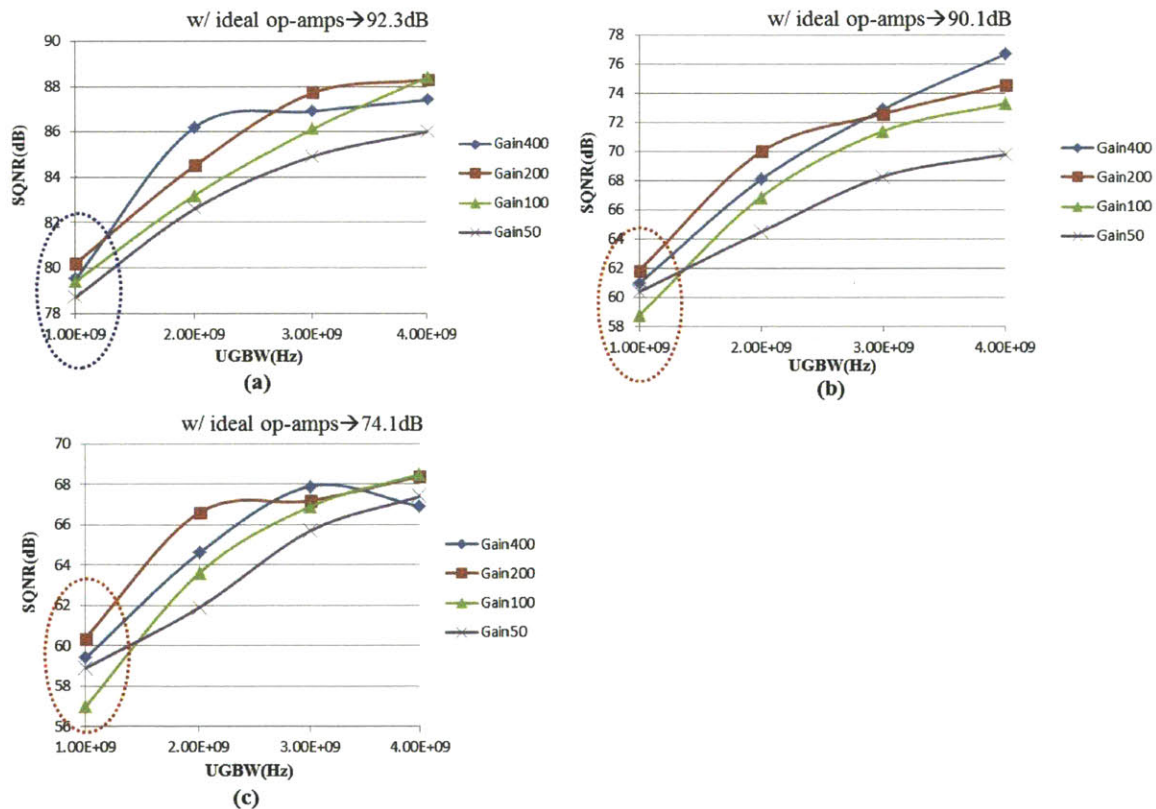


Figure 5-4: SQNR graphs based on different finite DC gains and UGBWs: (a) proposed CT MASH $\Delta\Sigma$ modulator with the gain-of-1 block, the feedforward path, and the LPF, (b) original CT MASH $\Delta\Sigma$ modulator with the gain-of-1 block, the feedforward path, and the LPF, (c) original 3rd-order $\Delta\Sigma$ modulator

Figure 5-4 shows simulated SQNR across various different DC gains and UGBWs. As these values continue to increase, they approach the SQNR obtained for the ideal case. Figure 5-4(a) represents the SQNR results for the new CT MASH $\Delta\Sigma$ modulator. As a DC gain drops below 200 and UGBW declines to less than 3-GHz, the SQNR value obtained decreases rapidly. Therefore, these are the minimum DC gain and UGBW values required to provide adequate performance. For these minimum threshold values, modulator SQNR is degraded by about 4-dB as compared to the ideal case. However, for the original CT MASH $\Delta\Sigma$ modulator, when using the minimum DC gain and UGBW values given previously, SQNR degradation is more than 17-dB. This is because the analog filter deviates from the ideal filter, due to the finite DC gain and UGBW. As a result, the digital filter can no longer fully cancel the quantization noise. Furthermore, if DC gain and UGBW are low in the original CT MASH $\Delta\Sigma$ modulator, the SQNR is comparable to an original 3rd-order $\Delta\Sigma$ modulator. This means that digital filters no longer cancel the quantization noise at all. From this simulation result, the new CT MASH $\Delta\Sigma$ modulator is much more robust in terms of DC gain and UGBW of op-amps. This is especially true when compared to the original CT MASH $\Delta\Sigma$ modulator, which needs good matching between the analog and digital filters.

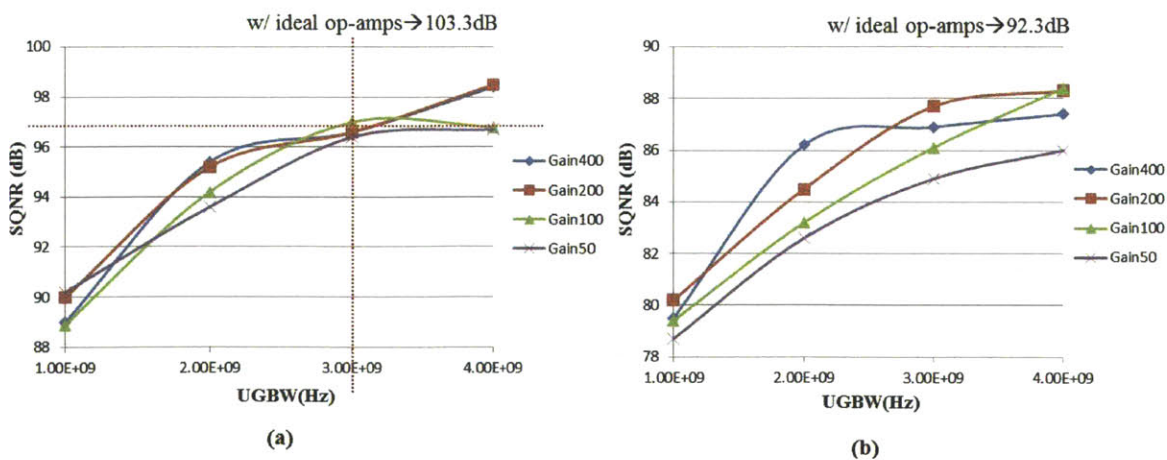


Figure 5-5: SQNR graphs based on different finite DC gains and UGBWs. (a) Gain-of-4, (b) Gain-of-1

Figure 5-5 illustrates the advantage of using gain blocks for further quantization noise suppression. Since the new CT MASH $\Delta\Sigma$ modulator eliminates quantization noise from the 1st-stage, and quantization noise from the 2nd-stage is reduced by gain blocks, these blocks can directly improve the resolution. Figure 5-5(a) shows the resolution result, when gain-of-4 blocks are used. The overall trend of the each trace is similar to the trends seen when gain-of-1 blocks are used. However, SQNR improves by approximately 10-dB in all cases when gain-of-4 blocks are used. Since implementing gain blocks does not require extra circuitry, using these blocks allows higher SQNR to be achieved at minimal cost.

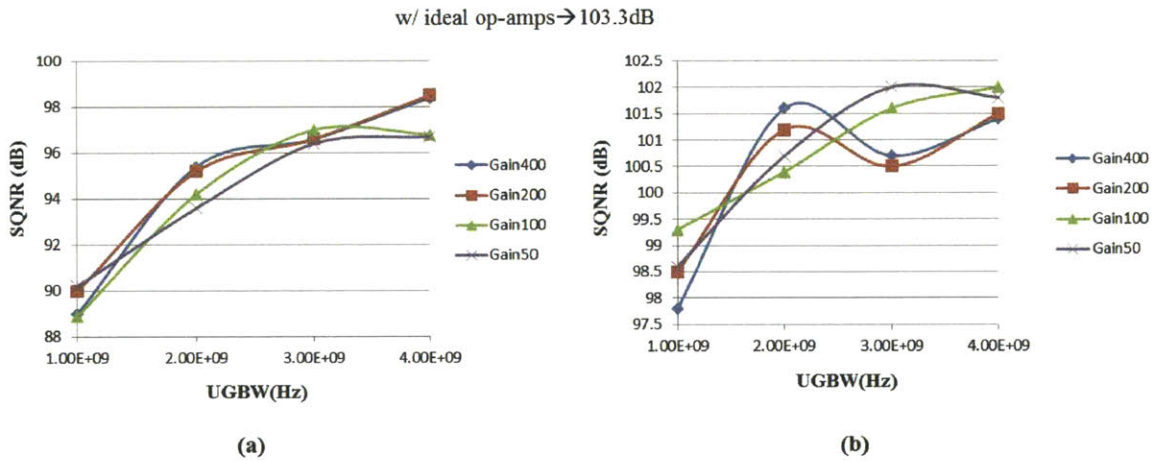


Figure 5-6: SQNR graphs based on different finite DC gains and UGBWs: (a) Gain-of-4, (b) Gain-of-4 with the gain-enhancement 1st-integrator

So far, a conventional 1st-integrator in the 1st-stage has been used for the simulation results. As mentioned in the previous chapter, if a replica gain-enhancement integrator is used, the effective DC gain and AC gain in the signal band can be increased significantly. As a result, SQNR is improved dramatically with the same DC gain and UGBW. In Figure 5-7, graph(a) shows simulation performance when an ordinary integrator is used, while graph(b) highlights the increase in resolution that can be achieved when a gain-enhancement integrator is used. As shown in the graph, overall SQNR in all cases increases by 5-dB, and is close to the resolution achieved in the ideal case. In summary, by using gain blocks and a gain-enhancement integrator,

the degraded resolution due to finite DC gain and UGBW of op-amps can be almost completely restored.

5.4 Acceptable Input Range

Another significant advantage of the proposed CT MASH $\Delta\Sigma$ modulator exists over current MASH $\Delta\Sigma$ modulator implementations.

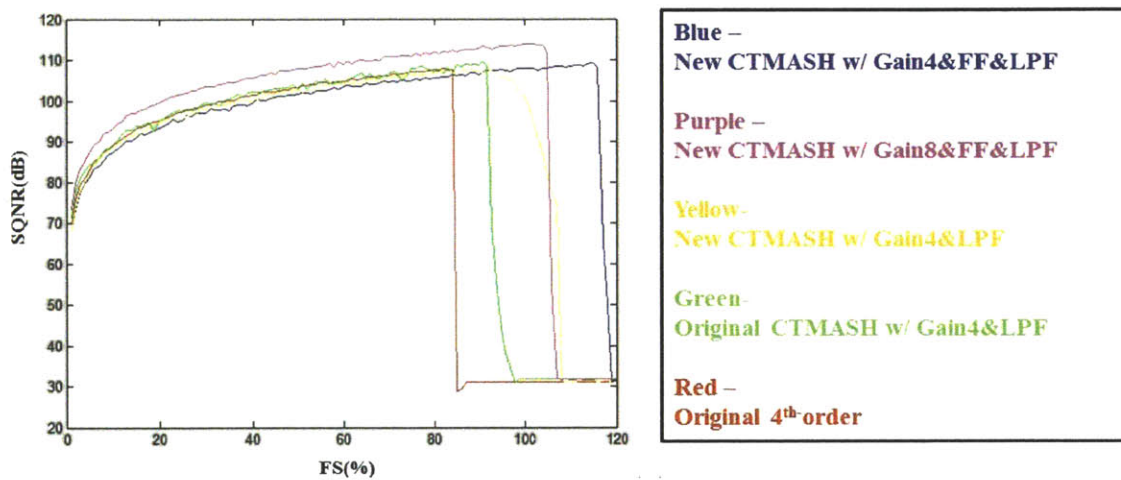


Figure 5-7: SQNR vs. input amplitude

Figure 5-7 shows SQNR values over a range of input amplitudes. This input amplitude is shown compared to the FS of the outer feedback DAC in the 1st-stage. In general, $\Delta\Sigma$ modulators become unstable, if input amplitude approaches 100% FS of the outer feedback DAC. This aspect is shown in Figure 5-7. The red trace represents the result from a standard 4th-order $\Delta\Sigma$ modulator. As shown in Figure 5-7, the input amplitude of this modulator can be only increased up to 84% FS. The green trace represents the results for the original CT MASH $\Delta\Sigma$ modulator, whose input can be increased up to 91% FS. Above these points, the two modulators become unstable and SQNR values suddenly drop. The remaining traces show results from the new CT MASH $\Delta\Sigma$ modulators with different features, such as gain blocks and a feedforward path. An interesting point is that the input amplitude of these modulators can exceed

100% FS of the outer feedback DAC. In particular, the blue trace, which represents the new CT MASH $\Delta\Sigma$ modulator with gain-of-4 blocks and the feedforward path, shows the input of this modulator can be increased up to 116% FS. This characteristic of the new CT MASH $\Delta\Sigma$ modulator is helpful in improving the DR, an important target specification.

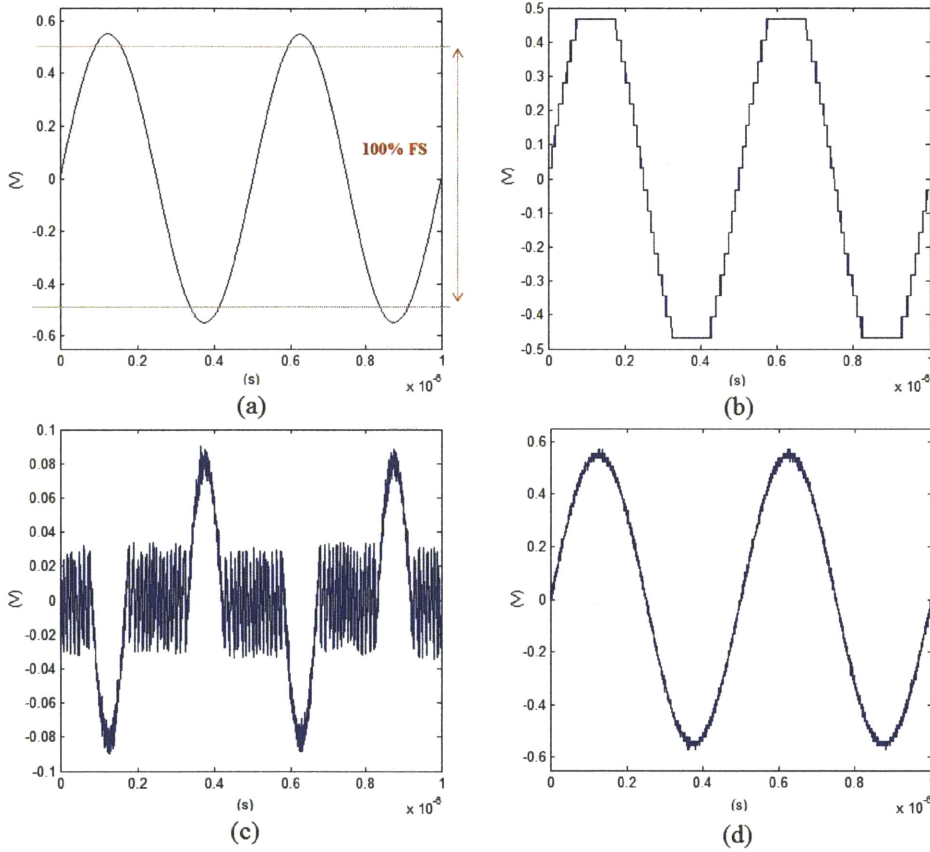


Figure 5-8: Signals when the input amplitude is 110% FS: (a) input of the entire modulator, (b) output of the quantizer in the 1st-stage, (c) input of the 2nd-stage, (d) output of the entire modulator

Figure 5-8 illustrates the reason why the input of the new CT MASH $\Delta\Sigma$ modulator can exceed 100% FS. Figure 5-8(a) shows the input of the entire modulator for an input amplitude of 110% FS. Since the input exceeds FS of the 1st-stage quantizer, the quantizer output is saturated, as shown in Figure 5-8(b). However, the difference between the input of the entire modulator and the output of the quantizer is injected into the 2nd-stage, as shown in Figure 5-8(c). Therefore, the 2nd-stage provides extra

headroom to handle the difference. Finally, the real output becomes the saturated output from the 1st-stage quantizer plus the output from the 2nd-stage, as shown in Figure 5-8(d). Although the outer feedback DAC of the 1st-stage cannot follow the input, for input amplitudes exceeding 100% FS, the feedback DAC of the 2nd-stage provides the extra range to aid in following the input. As a result, a high SQNR is maintained for much larger inputs when using the new CT MASH $\Delta\Sigma$ modulator, as compared to other $\Delta\Sigma$ modulator types.

Chapter 6

Conclusions

6.1 Thesis Summary

In this thesis, a new CT MASH $\Delta\Sigma$ modulator incorporating analog delay is described. The main contribution of this thesis is the practically implementable methodology for a CT MASH $\Delta\Sigma$ modulator. This new CT MASH $\Delta\Sigma$ modulator can provide all the SQNR and stability advantages of an ideal MASH $\Delta\Sigma$ modulator over ordinary CT $\Delta\Sigma$ modulators. The new CT MASH $\Delta\Sigma$ modulator also solves several of key challenges associated with previous CT MASH $\Delta\Sigma$ modulators, as described below.

First, using a feedforward path and modified architecture without digital filters, quantization noise from the 1st-stage is canceled. Therefore, the additional circuitry needed to match analog and digital filters is no longer required. Also, analog filters in the modulator are now more robust to process variation and other non-ideal factors. Specifically, low DC gain and UGBW op-amps can be used without significant resolution degradation, making the modulator design easier and less power intensive.

Second, by absorbing the LPF into active circuitry, the SH circuit is eliminated. Because implementation of an accurate SH circuit is difficult for sampling frequencies above 1-GHz, the use of an LPF can significantly ease design complexity.

Finally, unlike conventional $\Delta\Sigma$ modulators, the input amplitude can exceed 100% FS of the outer feedback DAC in the 1st-stage. This improves the DR of the modu-

lator.

By using the proposed architecture, all previous challenges can be resolved, and the quantization noise of the modulator is no longer a limiting factor in achievable resolution. Therefore, a CT $\Delta\Sigma$ modulator with high SQNR and signal bandwidth can be implementable.

6.2 Future Work

So far, ideal DACs have been used in the modulator. However, the noise and linearity errors from DACs cannot be suppressed by the loop filter, so non-ideal DACs degrade resolution dramatically. Therefore, further research into accurate DAC implementation is needed.

Following this research, this proposed architecture will be designed at the transistor level. Although overall circuit schematics have already been completed, the careful transistor-level design and layout of each component in the modulator is required to achieve target specifications.

Finally, the proposed CT MASH $\Delta\Sigma$ modulator will be fabricated and characterized using a 28-nm CMOS technology.

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