Characterization and Modeling of

Silicon-On-Insulator Field Effect Transistors

by

Thomas P. Allen

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

May 20, 1999

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Author_____

Department of Electrical Engineering and Computer Science

May 20, 1999

Certified by_____

Professor Clifton G. Fonstad

Thesis Supervisor

Accepted by_____

Arthur C. Smith

Chairman, Department Committee on Graduate Theses

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ABSTRACT

A model is developed for the simulation of Silicon-On-Insulator (SOI) Field Effect Transistors (FETs). The general disadvantages and advantages of SOI FETs are looked at, and several existing models are examined to determine their usefulness. Issues such as noise and thermal conductivity are taken into account. The application in which the FETs are to be used offers simplifications to the model which are taken into account. Equations and schematics suitable for implementation in PSPICE are synthesized and presented. An error of approximately 6% is obtained, improving upon the SOI FET model provided by the vendor of the devices.

Thesis Supervisor: Clifton G. Fonstad
Title: Professor, Department of Electrical Engineering

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I. Introduction

Currently the Acoustical Imaging Department at Lockheed Martin Infrared Imaging Systems (LMIRIS) is developing an underwater ultrasonic camera capable of operating in conditions such as turbidity and darkness which render light based cameras useless. A key part of this system is its proposed ability to combine both a transmitting transducer and a receiving transducer into one array. This requires a special transmit/receive integrated circuit (TRIC). The TRIC must have both high-voltage switching DFETs to handle the high voltage transmitting pulses, which are on the order of 150 volts, and high sensitivity Field Effect Transistors (FETs) to amplify and process the pulse returns, which are on the order of millivolts. These two different kinds of transistor must be all processed on the same silicon wafer, which will then be bonded to the actual transducer array.

The problem with using a conventional transistor process to manufacture this TRIC is that the application of a transmit pulse to one of the DFETs will most likely burn out the sensitive amplification FETs with the high voltage. The solution to this problem chosen at Lockheed-Martin is to use a technology known as Silicon-On-Insulator (SOI). With this process, an insulating oxide is placed over the entire surface of the silicon substrate, and then each individual transistor is created as a "mesa" on this insulating layer. The result is that the individual FETs are electrically isolated from one another, and will never "see" the high voltage transmit pulses being applied to the switching DFETs. A general cross section diagram of an SOI FET appears below in Figure 1.

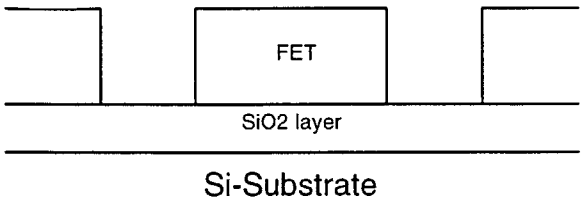

Figure 1: Cross-section diagram of SOI process FET.

There are many advantages and disadvantages to using SOI. SOI is often faster than conventional bulk processes, and has better DC gain and gain-bandwidth product (1). In this application, however, SOI was not chosen for any of these properties. It was, instead, chosen solely for its ability to electrically isolate FETs on the same chip. It is

therefore necessary to consider the problems associated with SOI, and deal with them in order to get what is wanted out of the technology while minimizing the parasitic effects of the insulating, or buried, oxide.

The final goal of this thesis is to develop a simulation model for both N and P type SOI FETs that can be used to accurately design the TRIC for this application. Such a model needs to take into account all pertinent parasitic effects which pose a problem in this application.

II. General Parasitic Effects of Silicon-On-Insulator Technology

SOI FETs have many unique characteristics which can present a design problem if not properly understood. These problems are:

- Interface Coupling
- Floating Body Effects
- Transient Effects
- Edge Effects
- Transconductance Variations

The presence of the buried oxide in an SOI FET causes a back gate to be formed at the bulk/buried oxide interface. This leads to **interface coupling**, wherein slight changes in the back gate voltage can greatly affect the electrical characteristics of the front channel. Effects include a lowering of the threshold voltage as the back gate moves from accumulation to inversion, a sharpening of the sub-threshold slope when the back gate is depleted; transconductance curve distortion when the back gate is inverted; and interference with characterization testing at the front channel [1].

The buried oxide also causes **floating body effects**. The most prevalent is the kink effect, which manifests as an increase in the slope of $I_D(V_D)$ curves [1]. Even though all of the FETs in the circuit in question have a body contact which is tied to a fixed potential (body tied), it has been demonstrated that local floating body effects still exist. Among these are dependencies of kink voltage and output resistance on width, and dependency of the low frequency noise corner frequency on drain-to-source voltage [2]. In fully depleted FETs, the kink effect also causes a reduction in the Early voltage [3].

Other common floating body effects are latching (a loss of gate control for high V_D) and increased impact ionization due to the bipolar transistor at the source-to-body junction [1].

The complete isolation of the SOI FET body also causes two types of undesirable **transient effects**. First, a longer period of time is needed to reach equilibrium after the body is charged, leading to long transients [1]. The second and more serious transient arises from the poor thermal conductivity of the buried oxide. SOI FETs have no place to dissipate heat as do bulk FETs. In addition, the thermal conductivity of the silicon film itself is greatly reduced from that of bulk silicon at low temperatures by phonon-boundary scattering [4]. This causes significant problems with temperature dependent parameters such as carrier mobility, and needs to be well characterized.

Processing of SOI FETs in "islands" on the insulating oxide (mesa-etching) causes **edge effects** in which the lateral edges become a parasitic conduction path between the source and the drain. A sidewall transistor is created, working parallel to the main transistor [1]. These effects are not noticeable in the strong inversion region, but cause a hump in the subthreshold $I_D(V_G)$ curves. Parasitics cause a lower doping in the edge regions, which tends to lower the threshold voltage; also at lower gate voltages, the current in the sidewall portions of the channel tends to dominate the current in the channel center [5]. In addition, edge effects can contribute to excessive current leakage when the transistor is off [1].

Transconductance variations are a direct result of a back gate bias affecting front channel parameters. This subsequently affects device parameters such as threshold voltage, and sub-threshold slope, and carrier mobility. As the back gate moves through the depletion region from accumulation to inversion, the front threshold voltage drops, although it holds constant while the back gate remains accumulated or inverted. This change in back gate bias also causes a sharpening in the subthreshold $I_D(V_{GS}, V_{DS})$ plot and has a direct effect on effective carrier mobility in the front channel [1]. An extra series resistance added by the back gate appears in addition to the series resistance of the front gate. This increased resistance causes shifting and reduction of the

transconductance peak, as well as a sharper decrease of front channel transconductance in strong inversion [1].

There are already several models which take into account one or more of the parasitic effects of SOI. Robilliart and Dubois offer a model which is non-quasi-static and valid for long and short channel fully depleted devices, based upon an SOI adaptation of the charge sheet model for bulk MOSFETs [6]. Adan, et. al. present a 2D model which takes into account a non-uniform channel doping profile, short channel effects, and floating body effects [7]. The Cheng and Fjeldly I-V Model features a single expression description of all regimes, smooth current transition from the linear to the saturation region, parasitic series resistances, short channel effects, and mobility dependence on gate bias [8].

Several models also exist to predict thermal response. Arora, et. al. present a model which includes self heating by allowing temperature to be recalculated in a linear fit with power at each different bias point [9]. Tenbroek, et. al. introduce into the model a subcircuit driven by a power source (I_{DS}*V_{DS}) and consisting of three parallel resistance/capacitance pairs in series [10]. These models can be augmented by the use of the lossy heat conduction equation using body resistance, capacitance, and conductivity which are estimated from 1D - theory [11]. The subcircuit offered by Tenbroek and the techniques offered by Arora provide a good basis to which to add the lossy heat equation. The result will be a subcircuit which can be added to the electrical model to accurately predict self heating.

III. Fabrication Process

Allied Signal is actually fabricating the final TRIC, using their SOI process. They have supplied ten test FETs, five N-type and five P-type, for use in this characterization effort. These FETs are processed on a silicon substrate having a doping of approximately 6E14 cm^{-3} P-type. The buried oxide (BOX) has a thickness, t_{box}, of 4E-5 cm. The front oxide thickness, t_{ox}, is 2.25E-6 cm. The body film, which extends from the front oxide to the buried oxide, has thickness, t_{Si}, of 3.1E-5 cm. The doping of the body will be discussed later. The gate material used is a polysilicon with an N-type doping of

approximately 5E20 cm^{-3} N-type. The drain and source regions, which also extend all the way through the transistor from the front oxide to the buried oxide, are identically doped to about 1E20 cm^{-3} N-type. A very general cross section diagram of Allied Signal's SOI FETs appears in Figure 2.

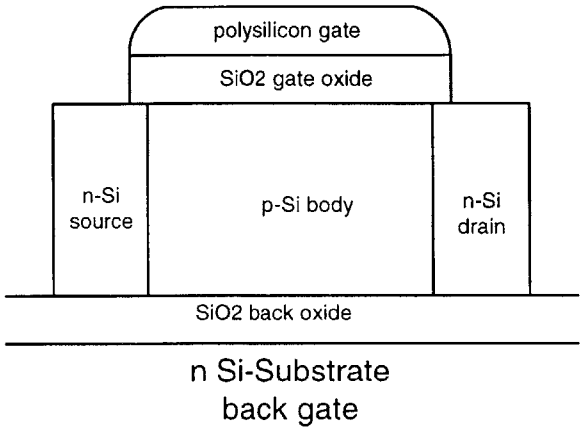

Figure 2: Cross Section of an Allied Signal SOI FET

The ten test FETs provided were all 40 μm wide, with gate lengths of 1.2, 1.5, 2, 5, and 40 μm.

The body doping in these FETs is of interest because it is non-uniform. Figure 3 shows the doping profiles for N-type body films as provided by Allied Signal.

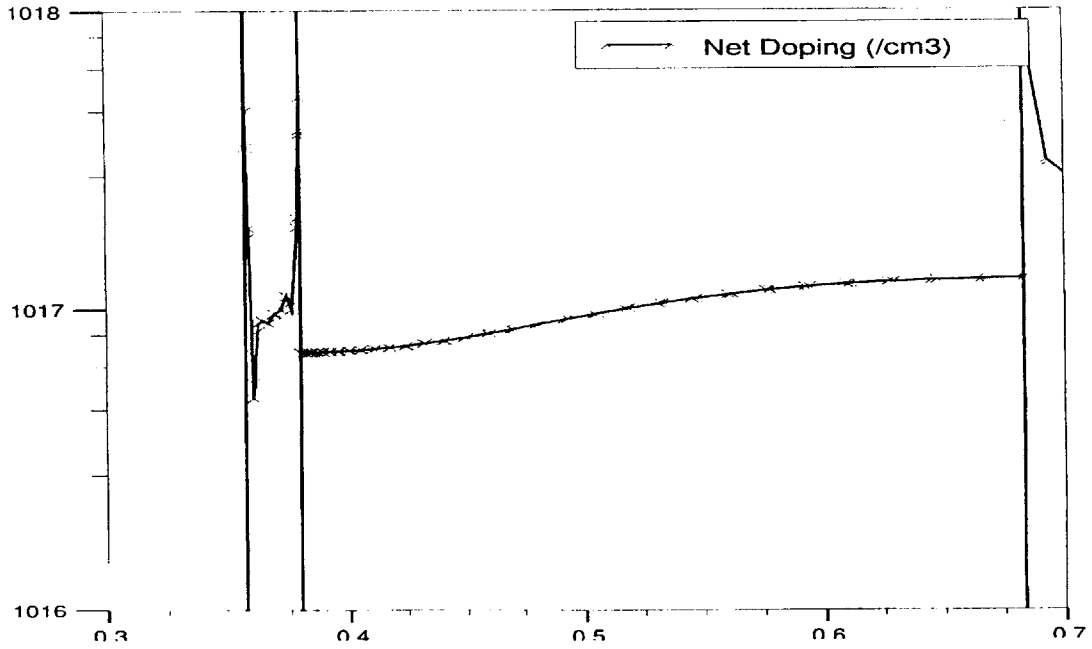

Figure 3: N-type body film doping profile

The doping of the N-type FETs is relatively straightforward. Doping was achieved using a boron ion implantation, and the film is doped P-type all the way through the thickness of the film. The P-type device doping, however, is more complicated. It will be discussed later, but is shown in Figure 4 for comparison.

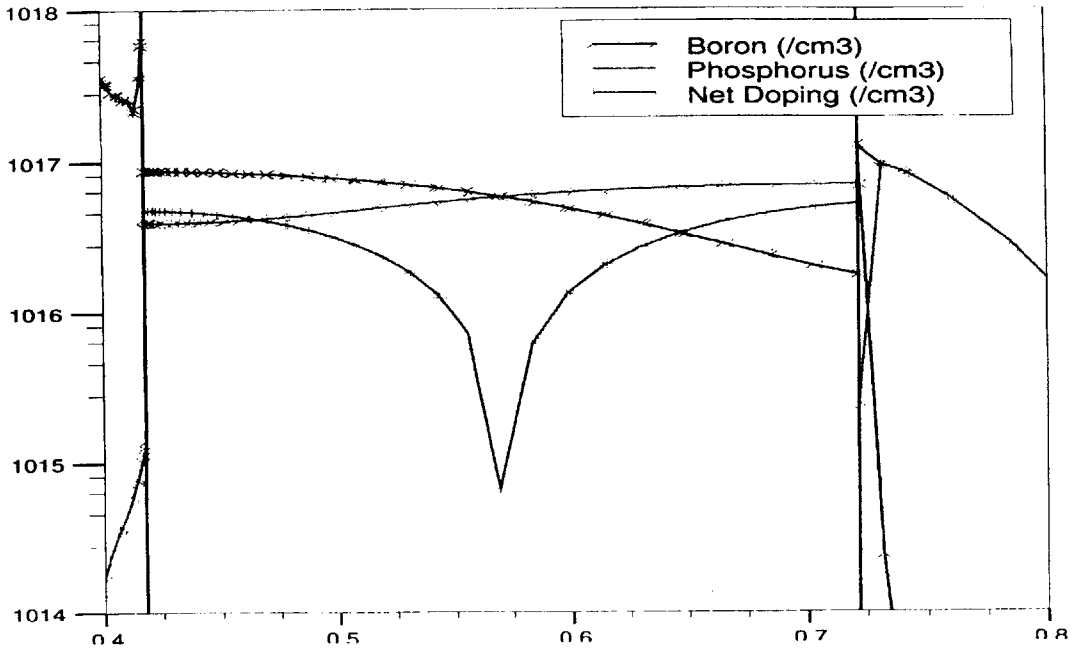

Figure 4: P-type body film doping profile

Several simplifications to the task at hand are presented by the process that Allied Signal uses. First of all, as can be seen from the doping profiles above, these transistors are partially depleted. This immediately removes several of the parasitic effects found in general in SOI. Now, parameter extraction and modeling techniques used on bulk FETs apply much more readily to the SOI process being used [3]. The kink effect is no longer a concern, and interface coupling is greatly reduced. Interface coupling goes away entirely due to the fact that these transistors are thick film, that is the body film is wider than the sum of the maximum depletion depths of the front and back interfaces. This assumption can be checked for the N-type FETs:

The maximum depletion depth at either interface, x_d, is given by the following equation [12]:

$$x_D = \sqrt{\frac{2\varepsilon_{Si}|2\phi_p|}{qN_A}} \tag{1}$$

where Φ_p is given by :

$$\phi_p = -\left(\frac{kT}{q}\right)\ln\frac{N_A}{n_i} \tag{2}$$

Plugging in the process parameters above and assuming a temperature of 300K, this yields a maximum front interface depletion depth of 0.126 μm and a maximum back interface depletion depth of 0.091 μm. The sum of these is 0.217 μm which is approximately 70% of the total film thickness. This result proves the assumption to be acceptable. The back and front depletion regions never interfere with each other, leading to no interface coupling.

This process also offers a way to deal with floating body effects, by providing a direct contact to the back gate, or substrate. By directly controlling the potential of the back gate, parasitic effects due to electrical "flotation" of the body can be minimized. In the ideal case, the body and the back gate would be shorted together, thereby completing eliminating these effects.

Edge effects are also minimized in this process by the use of a special technique which is the proprietary information of Allied Signal and therefore cannot be disclosed. This leaves thermal transient effects and increased noise as the parasitic effects which must be dealt with during the characterization and modeling of FETs fabricated with Allied Signal's FET process.

IV. Model Hierarchy

In order to derive a model for an SOI FET that will be useful, such a model needs to be applicable over a number of different bias conditions. However, the large and small signal characteristics of the FETs are different depending on which region the device is biased in. Therefore, a number of steps must be followed in order to determine the appropriate large and small signal models. First, the terminal voltages must be examined. They are abbreviated V_X, for back gate voltage, V_G for front gate voltage, V_D for drain voltage, V_S for source voltage, and V_B for body voltage; however when referring to one terminal with respect to another the notation will use both terminal letters, i.e. V_{GS} for gate to source voltage. These voltages and their relationships to one another determine the correct model. To this end, one of the terminals must be chosen as a reference point, and for convenience the source has been chosen for this purpose. Most of the terminal voltages are examined with respect to the source, which can be taken, for simplicity's sake, to be grounded. This section deals with establishing model architectures for every different bias region. In the following discussion, large signal parameters are denoted with a upper case letter and an upper case subscript. In addition, all front (upper) interface properties are denoted with a subscript 1, and all back (bottom) interface properties are indicated with a subscript 2.

Architectural Hierarchy

As mentioned before, the device bias region and therefore the model to be used in simulation depends on the five terminal voltages. Of these, two voltages are of paramount importance. These are the back-gate to source voltage, V_{XS}, and the gate to

source voltage, V_{GS}. These voltages control inversion channel formation at the back and front interfaces, respectively.

The back gate voltage, V_{XS}, controls inversion channel formation at the back oxide in the FET. This is because the source and drain extend all the way through the body film to the back oxide. Hence, the back interface looks much like a simple MOS transistor, controlled by the gate to source voltage. At the back gate flatband voltage, V_{FB2}, no potential change exists over the back interface. When V_{XS} drops below this voltage, accumulation occurs at the back interface. Under either of these conditions, no conduction occurs from the drain to source due to FET action at the back interface. This region is abbreviated BC, for Back Cutoff. When V_{XS} rises above V_{FB2}, however, a channel is formed at the back interface and current flows due to the back interface FET action. This region is abbreviated BI, for Back Inverted. This situation is depicted in Figure 5. Note that the BC region contains the line $V_{XB} = V_{FB2}$.

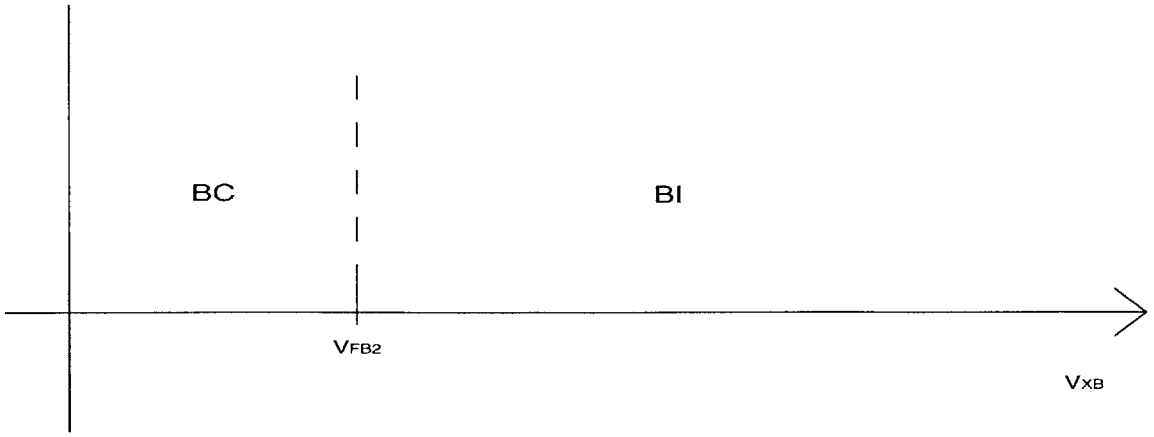

Figure 5: Back Interface Regions

This is exactly analogous to what occurs at the front interface, with the exception that the front interface is controlled by V_{GS}, as has been mentioned before. The subscript numeral has been changed to a 1 in order to denote front interface properties. Thus, the

front gate flatband voltage is denoted V_{FB1}. For V_{GS} greater than V_{FB1}, the transistor is in the FI, or Front Inverted, region. For V_{GS} less than or equal to V_{FB1}, the transistor is in the FC, or Front Cutoff, region. This is depicted in Figure 6. Note again that the FC region includes the line $V_{GS} = V_{FB1}$.

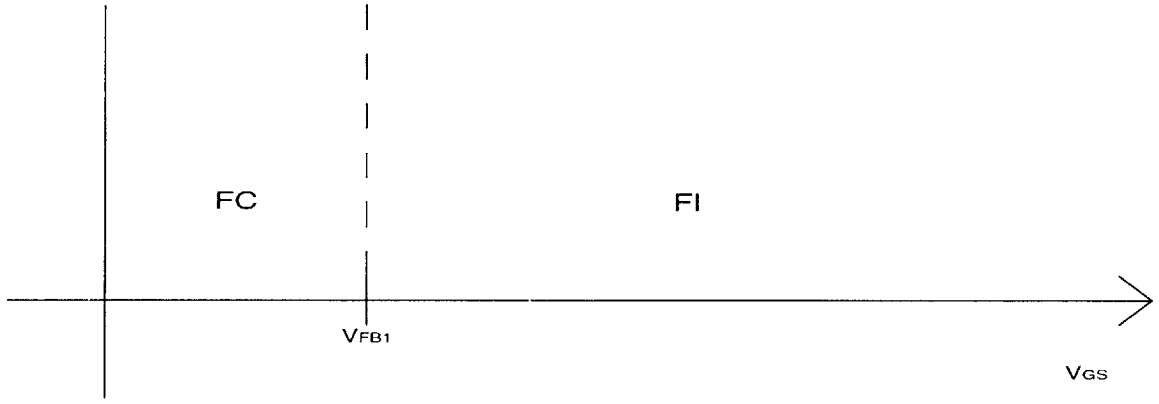

Figure 6: Front interface regions

The fact that the FETs being modeled are partially depleted thick film transistors greatly simplifies the establishment of bias regions. As has been mentioned above, the film is partially depleted and therefore thicker than the sum of the front and back interface depletion depths in strong inversion, which means that the front and back channels do not interfere with each other, i.e. no interface coupling occurs. If V_{GS} and V_{XS} do not interfere with the properties of the opposite interface, then their corresponding axes can be placed orthogonal to each other, creating a modeling region chart as in Figure 7.

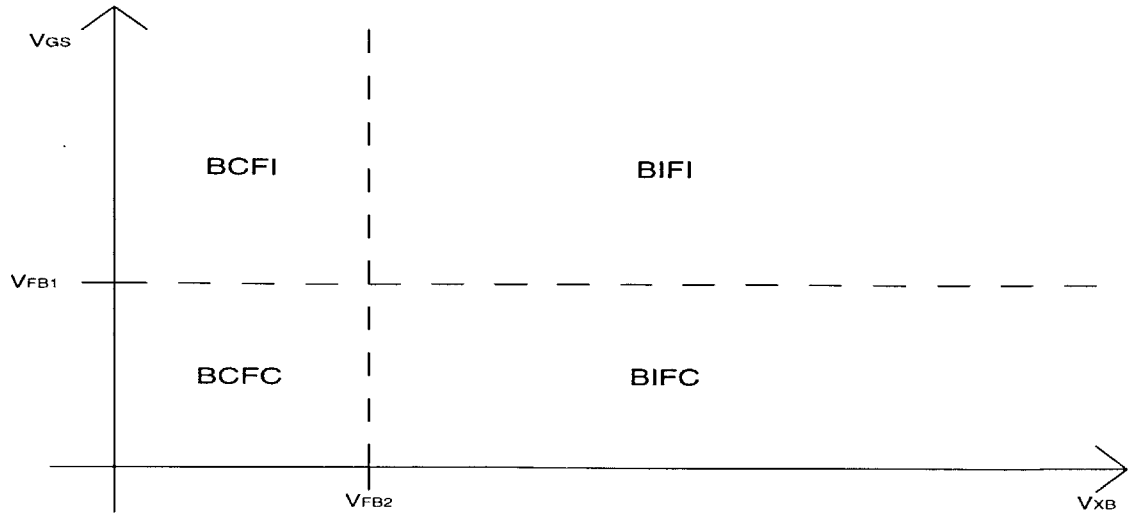

Figure 7: 2-D Model Region Chart

The regions are denoted in Figure 7 by a four letter code. The first two letters denote the state of the back interface, and the last two letters denote the state of the front interface. Hence, region BCFC is the region in which both interfaces are cut off, etc. Now the other voltages of interest (V_{BS}, V_{DB}, and V_{DS}) must be considered, to determine their impact on the possible addition of a third dimension to the chart of Figure 7. First, consider V_{BS} and V_{DB}. These voltages control the diodes at the source-body and drain-body junctions. When these diodes are back biased, they contribute only a tiny bit of leakage current to the model. However, if either diode is forward biased, the current out of the source or into the drain is dominated by the diode characteristics of the junction. This does not allow any current to flow from FET action. Hence, if either junction diode is forward biased, the transistor looks cut off at both interfaces.

V_{DS} has a different effect on the modeling regions. For fixed front gate and back gate voltages, V_{DS} determines whether the transistor is in the saturation or linear region. This, however, does not add a third dimension to the graph. This is because the progression from the linear to the saturated region with increasing V_{DS} does not have

effects orthogonal to those of the progression from weak to strong inversion with increasing V_{GS}. Rather, the bias value of V_{DS} defines a point along the V_{GS} axis where the transistor enters saturation. The definition of the point of transition between the linear and saturation region is made easier by the creation of a voltage V_{DSsat}. This is a function of V_{GS} (or V_{XS}, depending on which interface is being modeled) and the threshold voltage at the interface of interest. When V_{DSsat} is less than the bias value of V_{DS}, then the device is saturated. If V_{DSsat} is greater than V_{DS}, then the device is in the linear region. The boundary between the two regions is when $V_{DS} = V_{DSsat}$. This is roughly analogous to the definition point between weak and strong inversion. The amended model region chart appears in Figure 8.

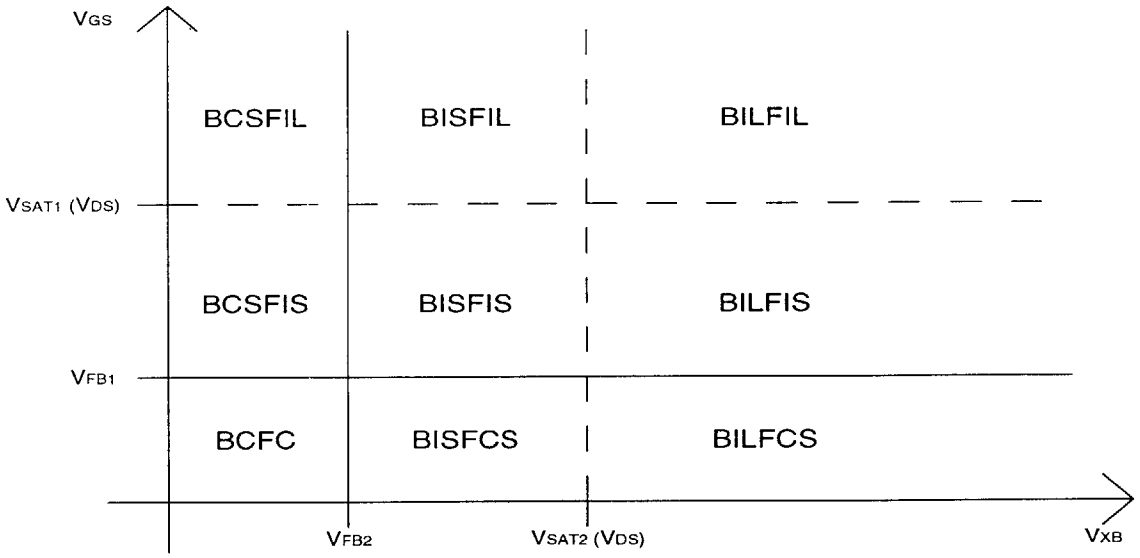

Figure 8: Revised Model Region Chart

Now two new letters have been added to the region code. These letters denote the state of each interface with an S for saturated and an L for linear. Hence BISFIL means that the Back is Inverted, in the Saturation region, and the Front is Inverted in the Linear region. However, the distinction between saturation and linear region does not have any

effect on the architecture of the models. This distinction only comes into play when deriving equations for drain current and capacitances. Because of this, the chart from Figure 7 will be used in the development of the four different model architectures required. Figure 8 will be used later to determine equations for these models.

Region BCFC:

This is the most trivial of all the regions. Since no current flows in the film due to FET action, there is no current source in the model. Instead, the model simply consists of the diodes formed by the source-body and drain-body junctions, the terminal resistances (each denoted with a subscript referring to the terminal), and the capacitances formed by the oxides and the junctions within the transistor. Because there are differences in the models for NMOS and PMOS devices, these will be dealt with separately. The models will also have an "N" for NMOS and a "P" for PMOS appended to the beginning of the letter code. The model for NBCFC appears in Figure 9 below.

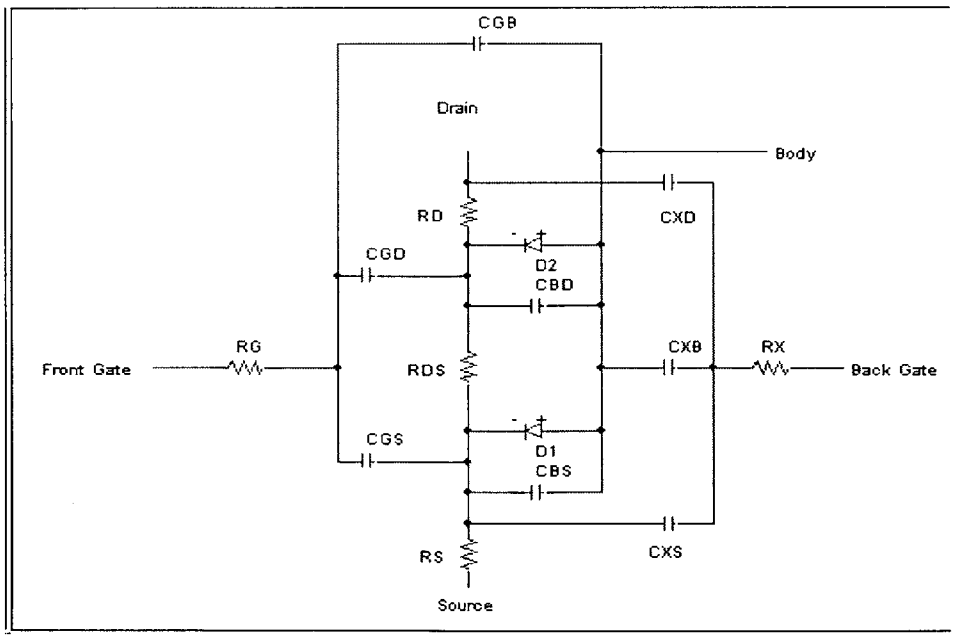

Figure 9: NBCFC Model

The only differences between the NMOS and PMOS models for this region are the polarities of voltages and the direction of currents. The PMOS model is shown in Figure 10.

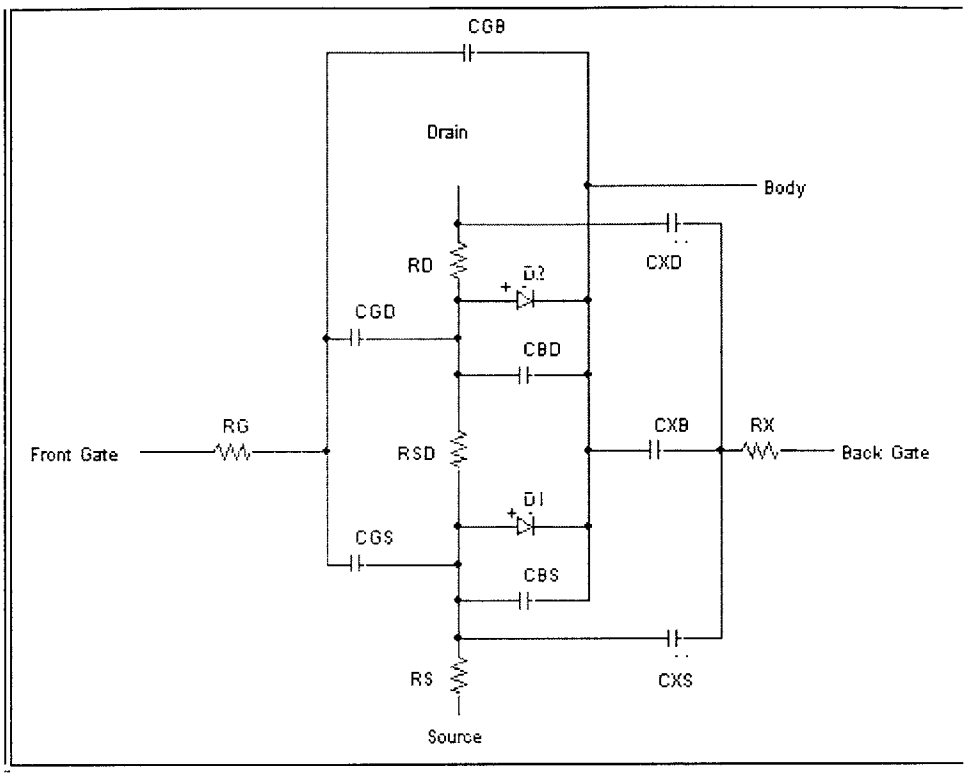

Figure 10: PBCFC Model

The only action of interest in this model is the diode currents and the minimal AC feedthrough provided by the resistor-capacitor network. The contact resistances are all process dependent and must be experimentally determined or calculated. The diode leakage currents must also be measured. All of the capacitors have values dependent upon the terminal voltages, and the equations used to determine their values will be covered later in Section V. It is important to note that this is the model that is defaulted to when the FET is off at both the front and the back interfaces, regardless of the state of the junction diodes in the model.

Region BIFC:

This region is interesting, and the models for the NMOS and PMOS FETs in this region are very similar. The NMOS model is shown in Figure 11.

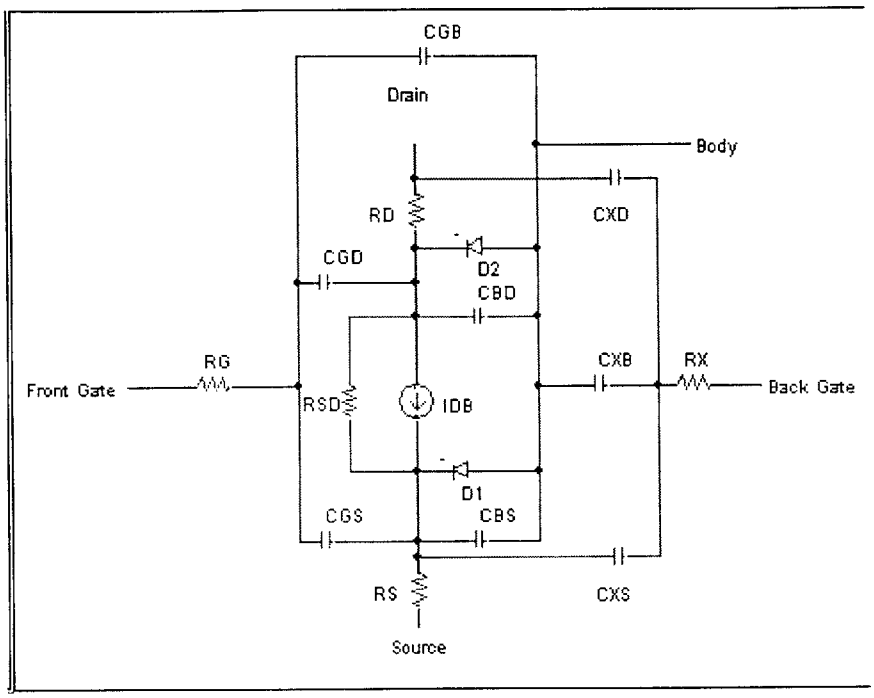

Figure 11: NBIFC Model

This model consists of all the capacitances and diodes from the BCFC model, as well as a current source denoted as I_{D2}, for drain current induced by FET action at the back interface.

The PMOS model is very similar to the NMOS model in this region. Refer to the doping profile of the PMOS channel region in Figure 4 above. Figure 4 is a computer simulation (supplied by Allied Signal) of the doping profile along the body film in the P-type FETs. The left hand side of the plot is the front oxide, and the right hand side is the back oxide. Note that the entire body is not doped uniformly N-type, as one might assume in a PMOS process. Rather, the back of the channel is doped N-type, and the front of the channel is doped P-type. Allied Signal believes that, due to their doping

process, the junction between the N- and P-type regions occurs closer to the front of the body than it is shown in Figure 4. The reason for this P-type counter doping at the front of the channel lies with the material used to make the gate. This material is N+ doped. This implies that the NMOS devices must have a heavily P doped body in order to achieve a threshold voltage of approximately 1 Volt. However, heavy N type doping in the PMOS devices yields a threshold voltage of approximately one volt lower than the desired approximately -1 Volt. The counter doping adjusts the threshold voltage to the desired level. The fact that the back interface is N-doped in a P-type transistor must be taken into account when modeling the back interface. For instance, the equations which use film doping assume that, for a P-type transistor, the doping is N-type. For this reason, the concentration of P-type dopant cannot just be "plugged in" to the equation as it could if it were N-type dopant.

The FET action at the back interface is included in the model in Figure 12.

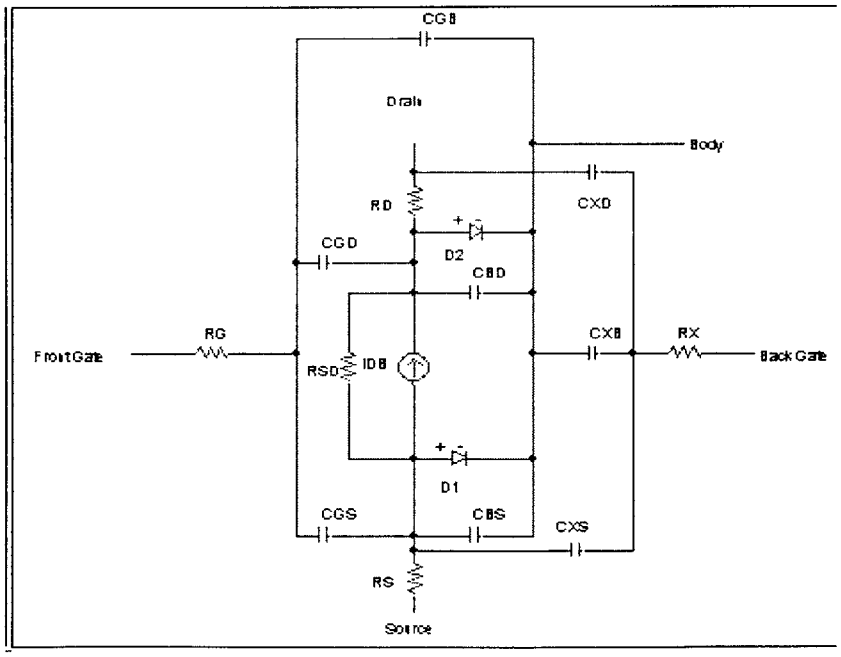

Figure 12: PBIFC Model

Region BCFI:

This is the most traditional and widely used model of all the ones being examined here. Once again, the basis for the model is the collection of components in the BCFC model. In this region, with the back interface cutoff, the only contribution of the back gate is the contact resistance and the capacitance of the back oxide. The only addition to the BCFC model is a current source, denoted I_{D1}, for drain current caused by FET action at the front interface. The value of this current source will be discussed later. The model for NMOS FETs in this region is given in Figure 13.

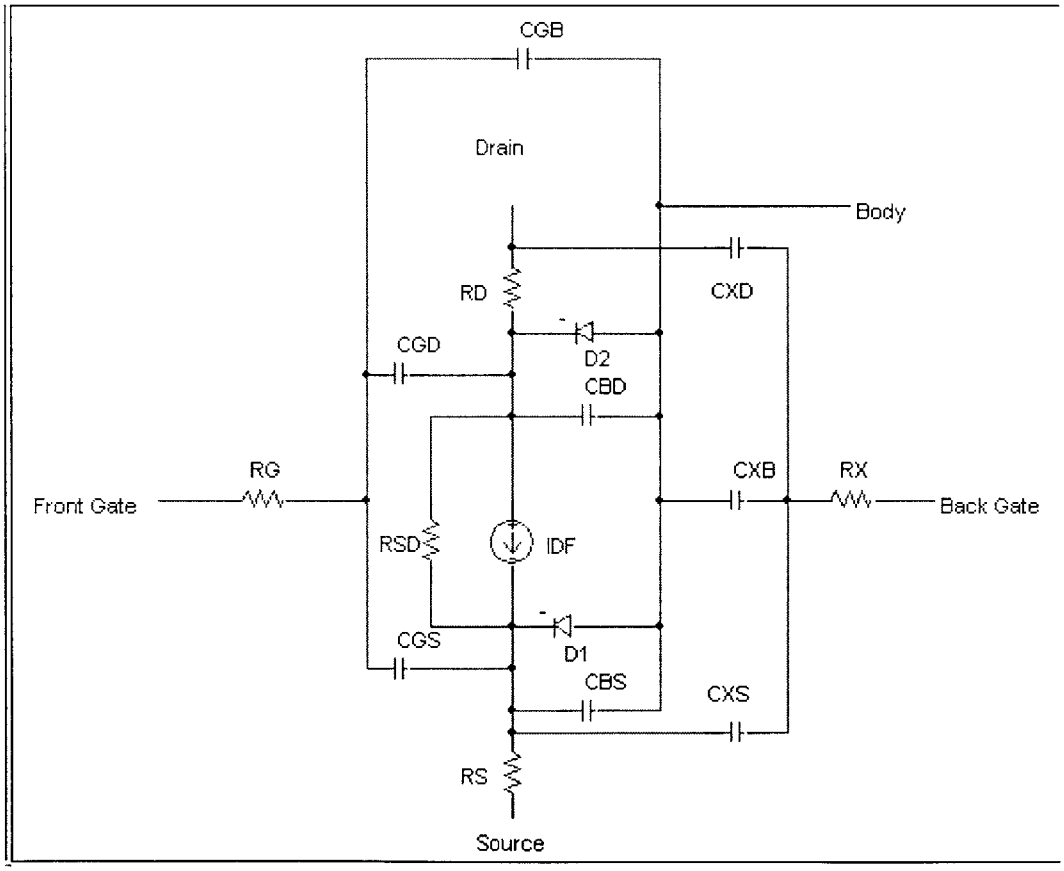

Figure 13: NBCFI Model

The P-type model again only differs in voltage polarities and current directions. It is shown in Figure 14 below.

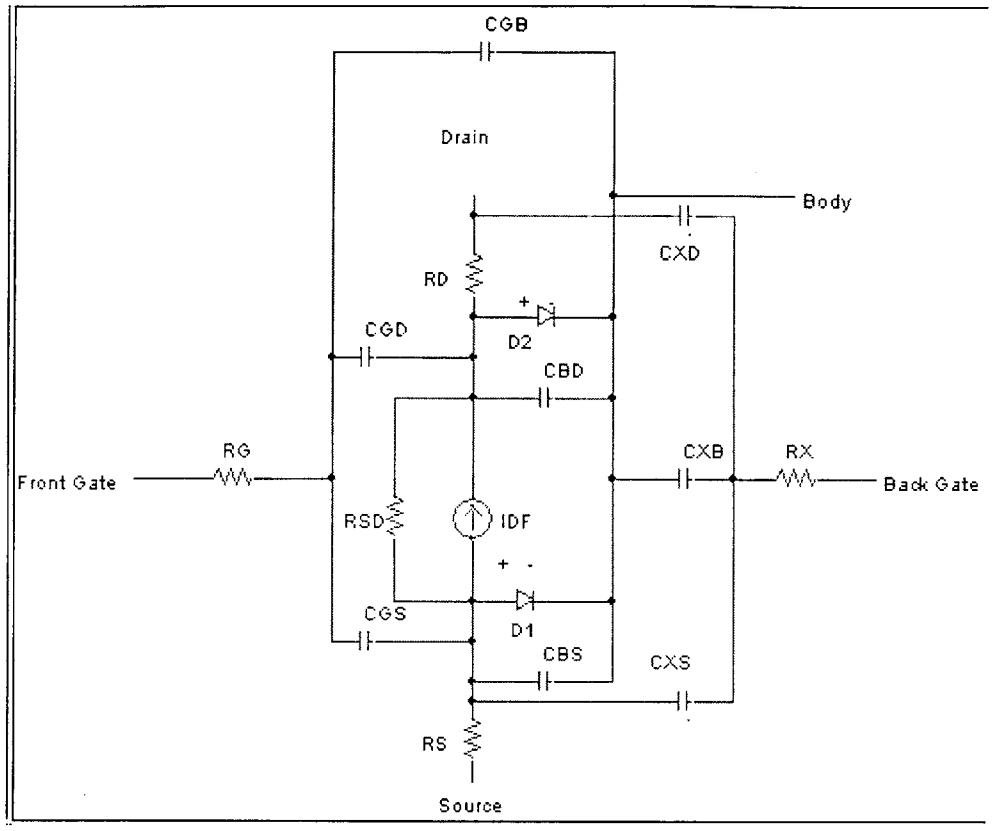

Figure 14: PBCFI Model

The equations that govern the capacitances and currents in the P-type model will also be discussed later.

Region BIFI:

This is perhaps the most interesting of all the model regions. Again, the NMOS and PMOS models in this region are very similar architecturally. The NMOS model appears in Figure 15.

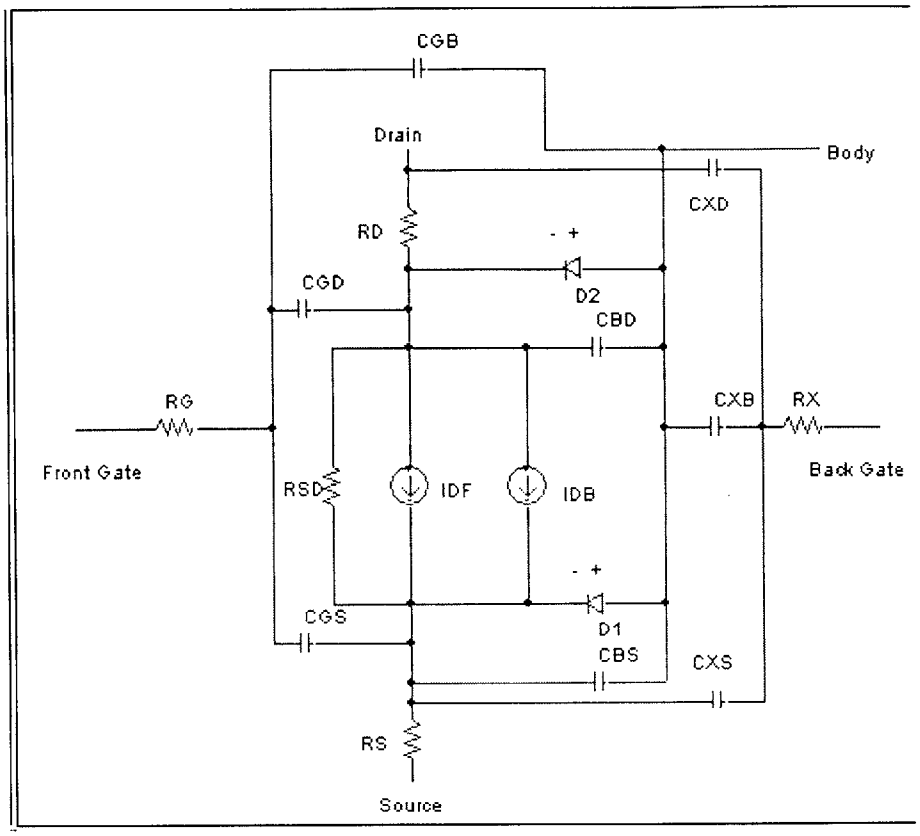

Figure 15: NBIFI Model

Once again, this model is built upon the BCFC model presented above. Now, the current source I_{D1} appears in it's "proper" place, in parallel with the source to drain resistance R_{SD}. In parallel with I_{D1} appears the back channel current source, I_{D2}. Now it must be proven that this model is indeed accurate for the condition in which both the front and back channels are inverted.

The way to do this is to use a type of superposition. The models for the BCFI and BIFC regions can be used. In each model, one of the interfaces is cutoff, and the other interface is inverted. First, these two models are to be connected together. This is done by shorting all five of the contact terminals together with the corresponding terminal on the other model. This results in a model with a number of redundant components (two C_{GB}s, for instance). This model is shown in Figure 16.

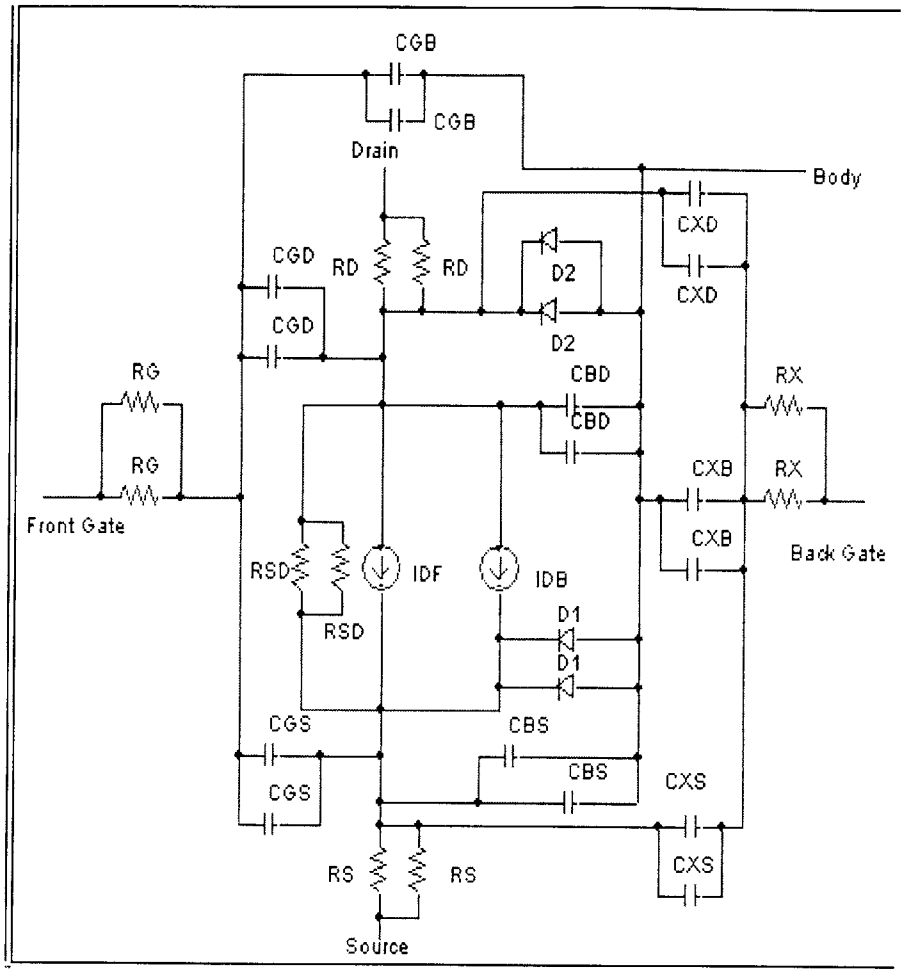

Figure 16: Parallel combination of BCFI and BIFC models

If the redundant components in the model of Figure 16 are eliminated, what is left is the model for the case in which both interfaces are inverted. Proceeding with this exercise indeed does yield the model in Figure 15.

The PMOS model in this region is simply the logical extension of the NMOS model, making the necessary changes in currents and polarities. It appears in Figure 17.

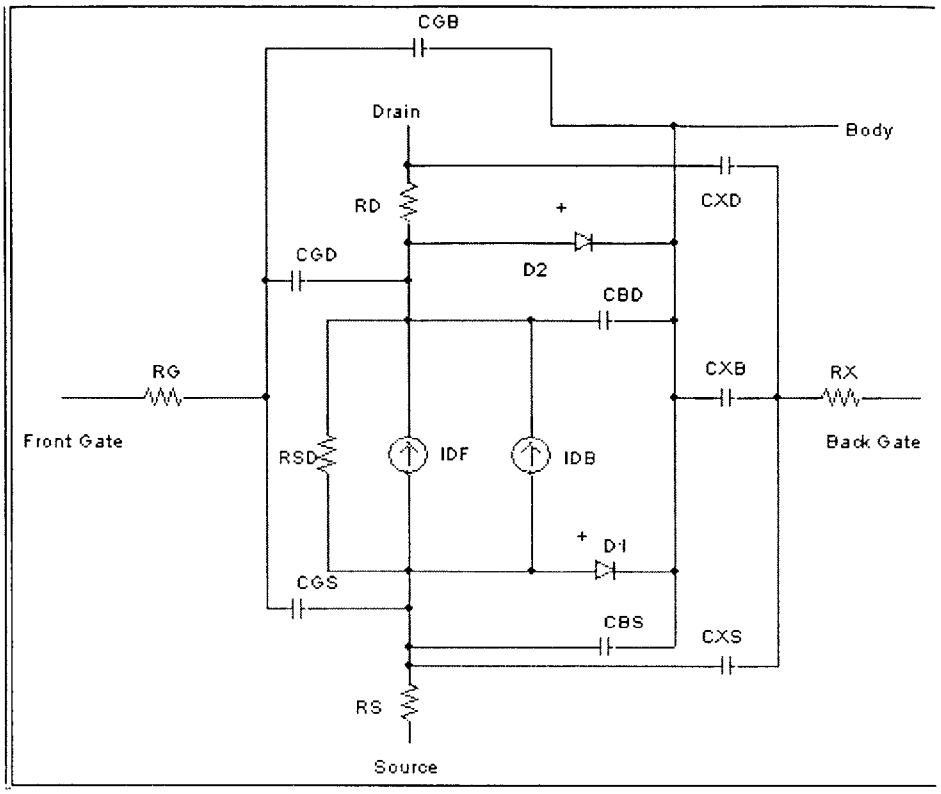

Figure 17: PBIFI Model

These regions are a starting point for establishing large signal models. It may become apparent later that additional regions must be added to the basic region chart presented above, but those regions defined here are an acceptable base from which to start modeling.

V. Component Equations

This section contains the equations for all the standard circuit components of the large signal models presented above. The equations that determine the value of the current sources, I_{D1} and I_{D2}, will be discussed later. From this point onward, derivations are performed for the N-type devices only. The derivation of the P-type device equations is straightforward and follows directly from the N-type derivation.

Capacitors:

The equations regarding capacitors are all primarily based on physical dimensions and doping concentrations. These quantities are very well understood, and Allied Signal has provided reliable process values for the test FETs being used in this study.

C_{BD} and C_{BS}:

The simplest capacitors to deal with are the capacitors C_{BD} and C_{BS}. These are created by the p-n junctions at the interface between the bulk and the source or drain. As such, they are dependent upon the area of the source-bulk and drain-bulk junctions, as well as the voltage across the junction. There are several process dependent parameters which also play into the equations. The value of the junction capacitors is given by the following equation from Allen and Holberg [13], split into two parts to allow for high injection effects.

$$C_{BZ} = CBZ0 \bullet A_{BZ} \bullet \left[1 - \left(\frac{V_{BZ}}{\phi_0}\right)\right]^{-MJ} ; \qquad V_{GS} \leq (\phi_0/2) \qquad (3a)$$

$$C_{BZ} = \left[\frac{CBZ0 \bullet A_{BZ}}{0.5^{(1+MJ)}}\right] \bullet \left[1 - \left(\frac{1+MJ}{2}\right) + \left(\frac{MJ \bullet V_{BZ}}{\phi_0}\right)\right] ; \quad V_{GS} > (\phi_0/2) \qquad (3b)$$

In the equation, Z is either D for drain or S for source. A_{BZ} is the junction area, MJ is the bulk-junction grading coefficient, and CBZ0 and ϕ_0 are given by the following equations.

$$CBZ0 = \sqrt{\left[\frac{(q \bullet \varepsilon_{Si} \bullet N_{SUB})}{\phi_0}\right]} \tag{4}$$

$$\phi_0 = \left(\frac{kT}{q}\right)\ln\left(\frac{N_{SUB} \bullet N_Z}{n_i^2}\right) \tag{5}$$

Here N_{SUB} denotes the doping of the silicon film, and N_Z is the doping concentration in either the drain or the source (depending on what Z is). It is important to note that N_S is equal to N_D, therefore ϕ_0 will be equal for both the drain-bulk and source-bulk junctions. Because the junction areas are also the same, it is also true that when the voltages applied to the junctions are identical, the junction capacitances will also be identical. Plugging the process constants from above into Equation (5), and assuming a temperature T of 300K (room temperature) yields a ϕ_0 of 0.981 V. Again plugging this value into Equation (4) yields a CBZ0 of 0.102 $\mu F/cm^2$. The area, A_{BZ}, of the two junctions is easily determined. Since the drain and source regions extend all the way through the film to the back interface, A_{BZ} is simply the thickness of the film, t_{Si}, multiplied by the width of the device. In the case of the Allied Signal test FETs, this yields an A_{BZ} of 0.124 cm^2. The only other unknown in the above equations is MJ, the bulk-junction grading coefficient. According to Allied Signal, the bulk-drain and bulk-source junctions are step junctions, therefore MJ = 0.5. This yields a final value for C_{BD} and C_{BS} of:

$$C_{BZ} = \left(\frac{1.2648E-14}{\sqrt{1-\left(\frac{V_{BZ}}{0.981}\right)}} \right) F \qquad V_{BZ} \leq (0.4505) \qquad (6a)$$

$$C_{BZ} = \left[3.577E-14 \bullet \left(0.25 + \frac{V_{BZ}}{1.962} \right) \right] F \qquad V_{BZ} > (0.4505) \qquad (6b)$$

A quick check reveals that plugging V_{BZ} = 0.4905V into both Equations (6a) and (6b) yields 1.789E-14 F, which means that Equation (6) is continuous. Note that the first derivative of Equation (6) is not continuous. This, however, does not pose a problem to a simulation model, because there are no small signal quantities which depend on the derivative of capacitance. The small signal value of this and the other capacitors will be dealt with later.

$\underline{C_{GB}}$:

This is the most straightforward of the gate associated capacitors. It is easier and, as shall be shown later, of no disadvantage to assume when calculating C_{GB} that the source and body are tied together. In this case, the determinant voltage for C_{GB} is not V_{GB} but V_{GS}. It is also easier, when determining the equation for C_{GB}, to break it into three pieces. These pieces correspond to the regions where V_{GS} is below the front interface flatband voltage V_{FB1}, where V_{GS} is between V_{FB1} and V_{T1}, and where V_{GS} is greater than V_{T1}. In the first region, the front interface is cutoff, and there is no depletion region formation. Therefore, the capacitance looking from the gate to the body film of the transistor is simply the capacitance of the front oxide, given by Equation (7a) [13].

$$C_{GB} = \left(C_{ox} L_{eff} W \right) \qquad (7a)$$

Here, C_{ox} is capacitance per unit area, L_{eff} is the effective channel length, and W is the channel width. C_{ox} is simply equal to ε_{ox}/t_{ox}, or 0.153 $\mu F/cm^2$. W, in all of the test devices, is 40 μm, and L_{eff} is equal to the length of the device less 2*LD, the lateral diffusion of the drain and source regions underneath the edges of the gate. LD will be experimentally determined later.

When V_{GS} first exceeds V_{FB1}, a depletion region begins to form underneath the front oxide. This depletion region creates another source of capacitance. Now, the capacitance seen looking from the gate to the body film is the series combination of the front oxide capacitance and the depletion region capacitance. Using the equation for depletion capacitance from Fonstad [12], this series combination boils down to:

$$C_{GB} = \left(\frac{C_{ox} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{ox}^2 (V_{GS} - V_{FB1})}{\varepsilon_{Si} q N_{SUB1}} \right]}} \right) \tag{7b}$$

Another quick check reveals that plugging in $V_{GS}=V_{FB1}$ yields the same value for C_{GB} that Equation (7a) yields, showing that the characteristic is continuous across the boundary between these equations. Again, the first derivative is not continuous, but, as shown before, that is of no importance.

In the third and final region of the C_{GB} equation, V_{GS} is greater than V_{T1}, the front interface threshold voltage. At this point, the equation is greatly simplified by the assumption that the depletion region does not increase in depth with increasing V_{GS}. Therefore, the capacitor value C_{GB} is once again constant. It's actual value is determined by plugging $V_{GS} = V_{T1}$ into Equation (7b). This also shows the characteristic to be

continuous across the border between the second and third region. The result is an equation for C_{GB} valid and continuous across all values of V_{GS}.

C_{XB}:

The back gate to body capacitor is exactly analogous to it's front interface equivalent. The body doping is different, as per the doping profile in Figure 3, and the oxide capacitance C_{box} is smaller. The flat band voltage V_{FB2} and the back interface threshold voltage, V_{T2}, are also different. They will be calculated, along with their front interface counterparts and the lateral diffusion, at the end of this section. For reference, the equation for C_{XB} is:

$$C_{XB} = C_{box} L_{eff} W; \qquad V_{XS} \leq V_{FB2} \qquad (8a)$$

$$C_{XB} = \left(\frac{C_{box} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{box}^2 (V_{XS} - V_{FB2})}{\varepsilon_{Si} q N_{SUB2}} \right]}} \right); \qquad V_{FB2} \leq V_{XS} \leq V_{T2} \qquad (8b)$$

$$C_{XB} = \left(\frac{C_{box} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{box}^2 (V_{T2} - V_{FB2})}{\varepsilon_{Si} q N_{SUB2}} \right]}} \right); \qquad V_{T2} \leq V_{XS} \qquad (8c)$$

C_{GD}:

The value of the gate to drain capacitor is dependent upon the formation of the depletion region at the front interface, and, as such, is dependent upon the gate to source voltage, as argued before. Therefore, it is once again useful to find different equations for

C_{GD} in the different regions of operation along the V_{GS} axis, as determined above, and then to put these equations together, checking to make sure that the characteristic is continuous in V_{GS}.

The first region to consider is the area where V_{GS} is less than V_{FB1}. In this region, with the front interface cutoff, there is no capacitance seen in the channel between the gate and the drain. The only capacitance present, therefore, is that brought about by the lateral diffusion of the drain region underneath the gate polysilicon. This capacitance is given by the equation [13]:

$$C_{GD} = C_{ox} W \bullet LD \tag{9a}$$

As the gate to source voltage begins to climb above the flatband voltage, the inversion layer begins to form. This causes the front oxide capacitance to appear between the gate and source and between the gate and drain. While V_{DSsat1} is less than V_{DS}, the device is saturated. In this region, the inversion layer has a familiar gradient, from full depth at the source end of the channel to non-existent at the drain end of the channel. The common assumption in this region for the way in which the oxide capacitance is split between the gate-source and gate-drain capacitors is that the gate-source capacitor sees two thirds of C_{ox} while the gate-drain capacitor sees none of it. Hence, the value for C_{GD} is still given by Equation (9a).

As V_{DSsat1} becomes greater than V_{DS}, the device enters the linear region. In this region, the thickness of the inversion layer from one end of the channel to the other is considered constant. At this point, the capacitance of the front oxide is split evenly between the gate-drain capacitor and the gate-source capacitor (not to say it is not still a component in the gate to body capacitance). The equation for C_{GD} in this region is given

by the sum of Equation (9a) and half of the front oxide capacitance, since these two components appear in parallel and can therefore be summed. This equation is [13]:

$$C_{GD} = \left(C_{ox}W \bullet LD\right) + \left(0.5C_{ox}L_{eff}W\right) \tag{9b}$$

These equations yield the endpoints of the C_{GD}-V_{GS} curve, but they are not continuous. However, this does not pose a problem, as long as the endpoints of the region are well defined. What is desired is to prevent the simulation from using two different values for the same capacitor. Therefore, the equations above work as long as the regions are well defined within the program.

C_{GS}:

For the gate to source capacitor, the derivation follows directly from that of C_{GD}. When the front interface is cutoff, C_{GS} is identical to C_{GD}, assuming that the lateral diffusion is identical on both ends of the channel (which is a reasonable assumption). When V_{GS} exceeds the front interface threshold voltage and the device enters the saturated region, then according to the assumption used above, 2/3 of the front oxide capacitance is added to the gate to source capacitor. As V_{DSsatI} exceeds V_{DS}, putting the device in the linear region, C_{GS} again equals C_{GD}, because the inversion layer, as mentioned before, evenly splits the oxide capacitance between the ends of the channel.

The region dependent values for C_{GS} are therefore [13]:

$$C_{GS} = C_{ox}W \bullet LD; \qquad V_{GS} \leq V_{FBI} \tag{10a}$$

$$C_{GS} = \left(C_{ox}W \bullet LD\right) + \left(\frac{2C_{ox}WL_{eff}}{3}\right); \; V_{FBI} < V_{GS}; \; V_{DSsatI} \leq V_{DS} \tag{10b}$$

$$C_{GS} = \left(C_{ox}W \bullet LD\right) + \left(0.5C_{ox}L_{eff}W\right); \; V_{FBI} < V_{GS}; \; V_{DS} < V_{DSsatI} \tag{10c}$$

Again, this equation is not continuous, but as has been argued above, this is not necessary. Note that in the above equations, the boundaries are defined by a "less than or equals" sign on one side of the region, and simply a "less than" sign on the other side. This prevents the simulation from trying to use both values at the endpoints of the regions.

C_{XD}:

The back gate to drain capacitance is simple to determine. Since the "back gate" is actually the substrate, it extends along the bottom of the entire device, including underneath the gate and drain. Therefore, the capacitance looking from the back gate to the drain is simply the capacitance of the piece of the buried oxide which is underneath the drain. Of course, when an inversion layer is formed at the back interface, it adds some capacitance between the back gate and the drain. However, this capacitance appears in parallel with that contributed by the buried oxide, and it is much smaller; therefore it can be ignored. If the length of the drain is denoted as L_{drain}, then the capacitor C_{XD} is given by the equation:

$$C_{XD} = C_{box} W L_{drain} \tag{11}$$

This equation holds true for all regions of operation. The length of the drain is approximately 1.2 μm, and C_{box} is 8.63 nF/cm^2.

C_{XS}:

The equation for C_{XS} exactly follows from that for C_{XD}. The same reasoning holds. If the source length is now defined as L_{source}, then the value of capacitor C_{XS} is given by:

$$C_{XS} = C_{box} W L_{source} \tag{12}$$

As with C_{XD}, this value is also constant over all regions of operation, and L_{source} is approximately equal to the length of the drain.

Diodes:

The two junction diodes in the model are there basically for the purpose of modeling leakage current. Their current is given by [12]:

$$I_{BZ} = I_S \left[e^{\left(\frac{qV_{BZ}}{kT}\right)} - 1 \right] \tag{13}$$

where I_S is the reverse bias current of the junction. Once again, Z in Equation 13 is either S for source or D for drain. It is important to note that this same equation is used to yield junction diode current in all regions; this equation never changes. The leakage current, I_S, is given by the equation [12]:

$$I_S = A_{junc} q n_i^2 \left[\left(\frac{D_e}{N_{SUB}\left(L - x_p\right)} \right) + \left(\frac{D_h}{N_Z\left(L_Z - x_n\right)} \right) \right] \tag{14}$$

This equation follows the assumption of a short-base limit. This assumption is valid considering that the minority carrier diffusion length is on the order of tens of microns and the intended length of channel that this application intends to use is on the order of one or two microns. This expression for I_S contains many constants which would need to be extracted by easily corruptible methods. For the purposes of this model, the forward biased characteristics of the source-bulk and drain-bulk p-n junctions is not a priority, and the reverse leakage current of those junctions is minuscule compared to currents of interest. Therefore it is acceptable in the scope of this project to estimate values for I_S. Plugging in reasonable estimates for diffusion constants yields an I_S on the order of 5 fA,

which is a credible answer. Using this value and assuming a temperature of 300K yields the following graph of I_{BZ} vs. V_{BZ}:

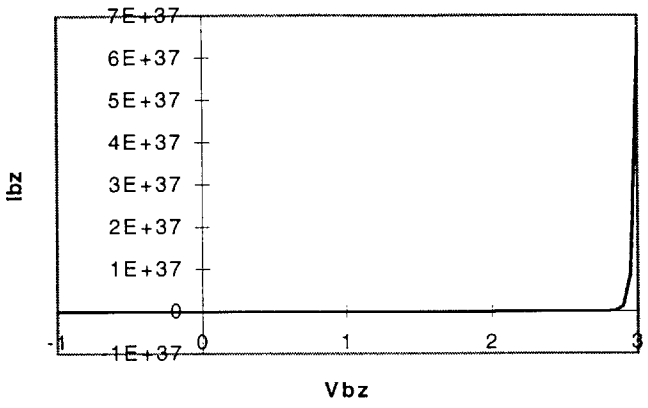

Figure 18: Junction diode current vs. junction voltage

Resistors:

R_D, R_G, R_S, and R_X are all contact resistances resulting from the metal used to contact the different terminals of the device. There appears no R_B because Allied Signal has assumed this resistance to be small enough to treat as a short circuit. For values of the other contact resistances, Allied Signal supplied numbers of approximately 50 ohms to n-type silicon, and approximately 10 ohms to the polysilicon gate material. Therefore, $R_D = R_S = R_X = 50\ \Omega$, and $R_G = 10\Omega$.

The resistor R_{SD} represents the very large resistance seen in an off-state looking from the drain to the source. It determines the amount of leakage current that flows through the channel when the transistor is cutoff. The larger this resistor, the smaller the off-state leakage. R_{SD} is determined using an experiment from Cristoloveanu [1]. In this experiment, all five test FETs are used. For each one, the test setup is as in Figure 19:

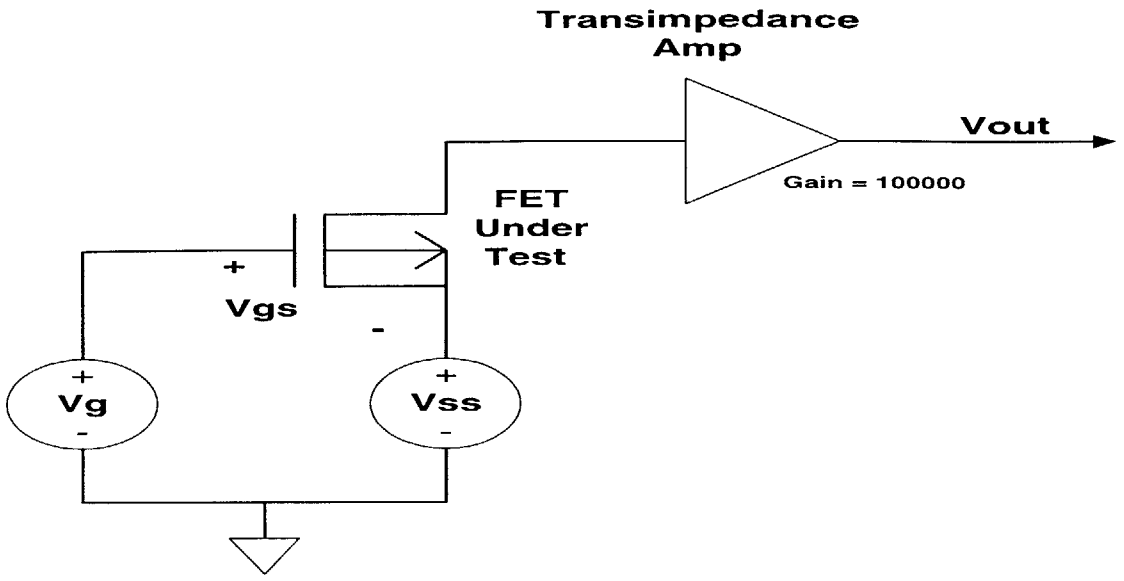

Figure 19: Test setup for R_{SD} extraction

V_{DS} is set to 0.1 V to ensure operation of the device in the linear region. V_{GS} is made up of an AC signal of 100 mV p-p on top of a DC bias that is swept. For each step, g_m and I_D are calculated. Then, for each step, a quantity θ is calculated with the following equation [1]:

$$\theta = \frac{\left(I_D \Big/ \left(g_m - 1 - V_{GS} + V_{T1} \right) \right)}{10\left(V_{GS} - V_{T1} \right)} \tag{15}$$

It is clear that, for large values of V_{GS}, θ approaches a constant value. This value changes with the length of the device being tested. If, now, the inverse of the length of the device is plotted against the calculated θ for that device, the characteristic is linear with a slope equal to R_{SD}.

The result summary appears below, and, as is shown, R_{SD} is calculated to be 11 MΩ. This is an extremely credible result, and as such is the value that will be used in this model.

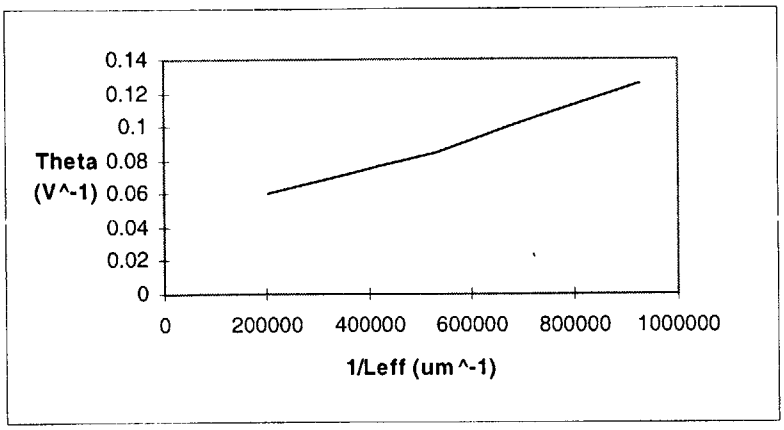

Figure 20: Graph of 1/Leff vs. Theta

FET	Drawn Length (m)	Actual Length (m)	1/L	Theta
MN05	0.0000012	1.081E-06	925069.4	0.12552
MN06	0.0000016	1.481E-06	675219.4	0.09967
MN07	0.000002	1.881E-06	531632.1	0.08492
MN08	0.000005	4.881E-06	204876	0.0602
MN09	0.00004	3.9881E-05	25074.6	-0.0195

Theta nought: 0.03966 V^-1
Rsource-to-drain: 10.9518 Megohms

Figure 21: Data Summary for RSD extraction.

Derivation of Constants for Component Equations:

Most of the constants in the component equations discussed thus far are dimensions and doping concentrations of the device which were supplied by Allied Signal. The only real parameter that must be extracted is the lateral diffusion, LD. The front and back interface flatband and threshold voltages must also be calculated or extracted. The exercise to extract LD is from Allen and Holberg [13].

The experiment is based upon the fact that the transconductance, g_m of a FET, in the linear region, is given by some lumped constant that will be denoted as K, multiplied by V_{DS} and divided by L_{eff}, which equals L-2LD:

$$g_m = \frac{KV_{DS}}{L - 2LD} \tag{16}$$

What is needed are two different transistors with different lengths. The process involves measuring g_m for these two transistors at the same value of V_{DS}, small enough to insure operation of the device in the linear region. The test setup used is identical to that used to measure R_{DS}. Gm is determined by applying an AC signal to the gate of the device, and then measuring the amplitude of the AC voltage at the output of the transimpedance amplifier. With two devices with drawn lengths denoted L_1 and L_2, the measured transconductances are denoted g_{m1} and g_{m2}. By manipulation of Equation 16, the result becomes apparent that

$$\frac{g_{m1}}{g_{m1} - g_{m2}} = \frac{L_2 + 2LD}{L_2 - L_1} \tag{17}$$

Plugging in the measured g_{m1} and g_{m2} as well as the drawn lengths L_1 and L_2 yields LD. Since this is a measurement requiring two different length transistors, and there are five different lengths of transistor supplied by Allied Signal, the experiment was performed on ten distinct pairs of transistors, using V_{DS} equal to 0.1V. The summarized results appear in Figure 22 below.

FET	Length	Vt	Slope	1/Slope^2
MN05	1.2E-06	1.028282	0.024948	1606.629
MN06	1.6E-06	1.031851	0.020987	2270.302
MN07	0.000002	1.021942	0.018983	2775.007
MN08	0.000005	1.006528	0.011741	7254.425
MN09	0.00004	0.999878	0.0041	59483.42

Mobility (cm^2/V*s): 1093.194
Delta L (um): 0.119
Vthreshold (V): 1.017696

Average: 1.017696 Delta L: 1.19E-07
Std. Dev.: 0.013898 Slope: 1.49E+09
% Error: 1.365681

Figure 22: Results of LD extraction

Taking LD to be the average of the results of the ten trials yields an LD of 6E-8 m, or 0.06 μm. This is a reasonable answer, and there are no individual results which strongly disagree with it, so this value will be used for LD.

The flatband voltage can be determined a number of ways, either by parameter extraction or by numerical calculation. The equations in the literature for flatband voltage yield reasonable results, and are also agreed upon widely throughout the literature, so that is what will be used. In particular, the equation from Allen and Holberg [13] will be used. For the front interface, V_{FB1} is defined by the following equation:

$$V_{FB1} = \left[\left(\frac{kT}{q}\right)\ln\left(\frac{n_i^2}{N_G N_{SUB}}\right)\right] - \left(\frac{qN_{SS1}}{C_{ox}}\right) \tag{18}$$

where N_G is the gate doping, N_{SUB1} is the doping at the front of the channel, and N_{SS1} is the front interface surface state density. It was supplied by Allied Signal to be 1E11 cm^{-2}. Plugging this into the equation above along with the constants from before, and, as always, assuming room temperature of 300K, yields a flatband voltage V_{FB1} = -1.131V. The equation for V_{FB2} directly follows that of V_{FB1}, except the back gate doping is used, C_{ox} is replaced by C_{box}, and N_{SS2}, the back interface surface state density, is approximately 3E11 cm^{-2}. Using these values and Equation 18 yields a back interface flatband voltage, V_{FB2}, of -2.42V. These results are reasonable, so they will be used in these equations.

Threshold voltage is one of the most important quantities to accurately model. The first step is to determine the threshold voltage with a source to bulk voltage of 0V. Once this quantity has been obtained, determining V_{SB} dependency is relatively straightforward. There are several ways to determine this. This study uses one experimental method and one equation as a check for the information supplied by Allied Signal to arrive at a single value which can be used for all of these equations.

First, the front interface threshold voltage will be determined. The easiest step to examine is the equation for V_T. It comes from Fonstad [12]. This equation is:

$$V_{T1}(0) = V_{FB1} + \left|2\phi_{f1}\right| + \left(\frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{Si}qN_{SUB1}\left|2\phi_{f1}\right|}\right) \tag{19}$$

where ϕ_f is the strong inversion surface potential, and is equal to:

$$\phi_{f1} = \left(\frac{kT}{q}\right)\ln\left(\frac{N_{SUB1}}{n_i}\right) \tag{20}$$

Assuming a temperature of 300K and plugging in the values given for constants previously yields ϕ_{f1} = 0.395V. Putting this result back into Equation 19, along with the value previously calculated for V_{FB1} yields $V_{T1}(0)$ equal to approximately 0.5V.

Next, an extraction experiment is performed that comes from Cristoloveanu et.al. [1]. In this experiment, each different length of device was biased with the back gate, body, and source all tied together and grounded. The drain was set at 0.1V, to ensure

operation in the linear region. Then, a signal was applied to the gate of the device consisting of a DC bias and an AC voltage of 40 mV p-p. The DC bias was stepped from 0.6 to 1.7 Volts. At each step, the value of the drain current and the value of the transconductance were measured. The drain current measurement was straightforward, using the DC component of the voltage at the output of the transimpedance amplifier. The transconductance was measured by measuring the peak to peak amplitude of the AC component of the output voltage and dividing by the amplitude of the input. The test setup, again, was identical to that in Figure 19.

Once the data had been taken, the ratio of the drain current to the square root of transconductance, $I_D/\sqrt{g_m}$, was calculated at every step of V_{GS}. Plotting this quantity vs. V_{GS} yields a linear characteristic for V_{GS} greater than V_{T1}. By running a linear regression for the linear portion of the curve, the x-axis intercept was calculated, and this is equal to V_{T1}. The summary of the data appears below.

FET	Length	Vt	Slope	1/Slope^2
MN05	1.2E-06	1.028282	0.024948	1606.629
MN06	1.6E-06	1.031851	0.020987	2270.302
MN07	0.000002	1.021942	0.018983	2775.007
MN08	0.000005	1.006528	0.011741	7254.425
MN09	0.00004	0.999878	0.0041	59483.42

Mobility (cm^2/V*s): 1093.194
Delta L (um): 0.119
Vthreshold (V): 1.017696

Average: 1.017696
Std. Dev.: 0.013898
% Error: 1.365681

Delta L: 1.19E-07
Slope: 1.49E+09

Figure 23: Data Summary for V_{T1} extraction

Using the average of V_{T1} as calculated for each FET yields a value with only 1% error, meaning that no individual result varies from the average by more than 1%. This value, as is shown, is $V_{T1} = 1.0V$. This varies significantly from the value given by the equation previously. Allied Signal, using a C-V measurement technique, provided a value for the front interface threshold voltage in the N-type FETs of 0.895V. Due to the accuracy of the C-V technique, this is the value that will be used, but the previous exercise illustrates that the equations in the literature do not very accurately describe the devices being characterized. Ad hoc experiments, like the one in Cristoloveanu, tend to give more reasonable result. This issue will be discussed in more detail shortly.

For the back interface threshold voltage, V_{T2}, Allied Signal supplied a value of approximately 10 V. This number is approximate, but, as shown shortly, this does not cause problems.

Now, having calculated or found V_{T1}, V_{T2}, V_{FB1}, V_{FB2}, and LD, it is possible to calculate the actual equations for the capacitors discussed so far, and to plot their characteristics. These are determined and plotted below for the test FET with a length of 2 μm.

$$C_{BZ} = \left(\frac{1.2648E-14}{\sqrt{1-\left(\frac{V_{BZ}}{0.981}\right)}} \right) F \qquad V_{BZ} \leq (0.49) \qquad (6a)$$

$$C_{BZ} = \left[3.577E-14 \bullet \left(0.25 + \frac{V_{BZ}}{1.962} \right) \right] F \qquad V_{BZ} > (0.49) \qquad (6b)$$

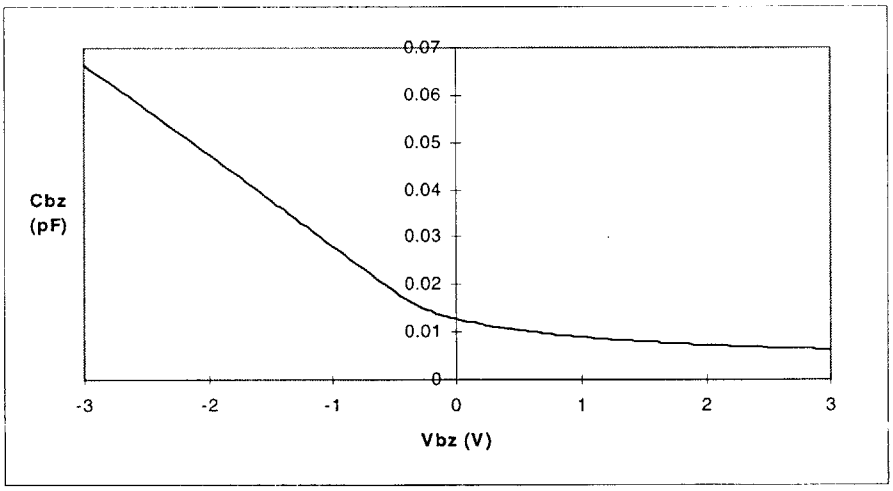

Figure 24: Junction Capacitance vs. V_{BZ}

$$C_{GB} = (1.165E-13)F \; ; \qquad V_{GS} \leq -1.1 \qquad (21a)$$

$$C_{GB} = \left[\frac{(1.164E-13)}{\sqrt{1+4.585(V_{GS}+1.1)}} \right] F \; ; \qquad 1.1 \leq V_{GS} \leq 0.895 \qquad (21b)$$

$$C_{GB} = (3.6688E-14)F \; ; \qquad 0.895 \leq V_{GS} \qquad (21c)$$

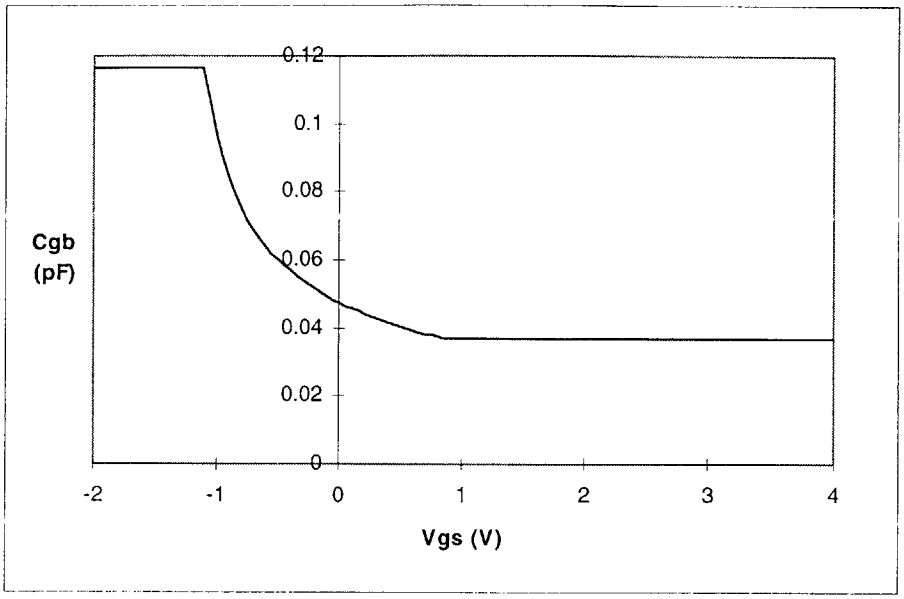

Figure 25: C_{GB} vs. V_{GS} (L=2μm)

$$C_{XB} = (6.9E-15)F; \qquad V_{XS} \leq -5.6 \qquad (22a)$$

$$C_{XB} = \left[\frac{(6.9E-15)}{\sqrt{1+(7.898E-3)(V_{XB}+5.6)}}\right]F; \qquad 5.6 \leq V_{XS} \leq 30 \qquad (22b)$$

$$C_{XB} = (6.096E-15)F; \qquad 30 \leq V_{XS} \qquad (22c)$$

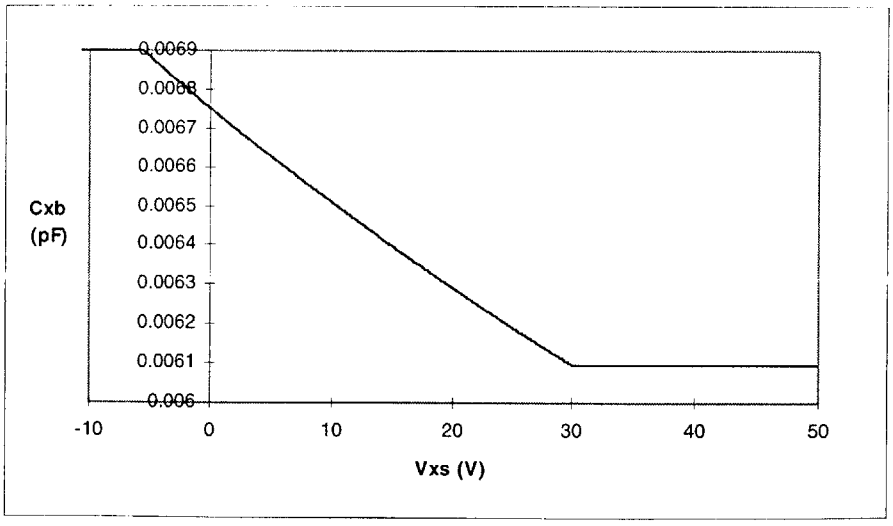

Figure 26: C_{XB} vs. V_{XS} (L=2μ)

$$C_{GD} = (3.672E-15)F \qquad V_{GS} \leq -1.1;\ V_{DSsat1} \leq V_{DS} \qquad (23a)$$

$$C_{GD} = (6.12E-14)F \qquad 1.1 < V_{GS};\ V_{DS} < V_{DSsat1} \qquad (23b)$$

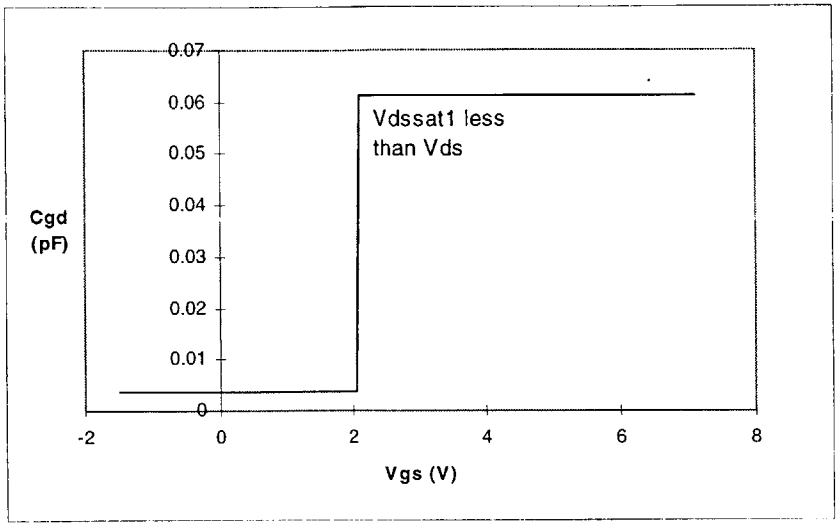

Figure 27: C_{GD} vs. V_{GS} (L=2μm)

$$C_{GS} = (3.672E-15)F \qquad V_{GS} \leq -1.1 \qquad (24a)$$

$$C_{GS} = (8.038E-14)F \qquad -1.1 < V_{GS};\ V_{DSsat1} \leq V_{DS} \qquad (24b)$$

$$C_{GS} = (6.12E-14)F \qquad -1.1 < V_{GS};\ V_{DS} < V_{DSsat1} \qquad (24c)$$

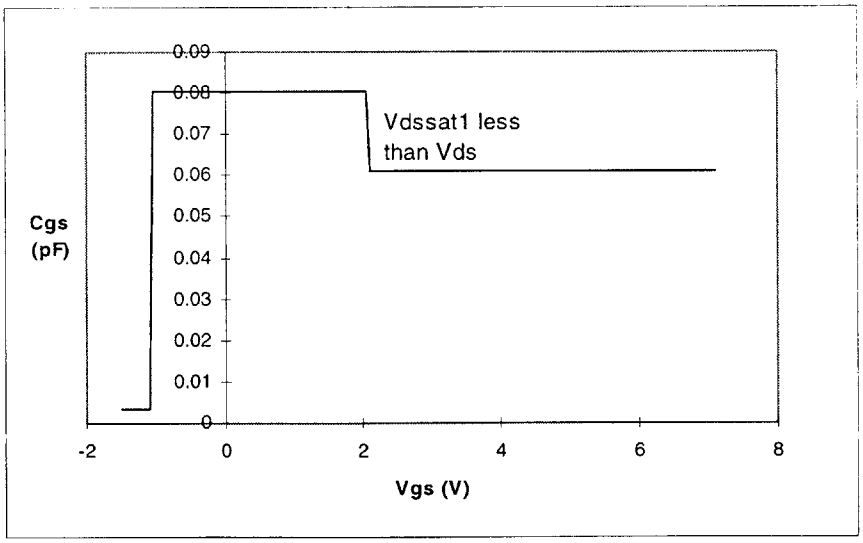

Figure 28: C_{GS} vs. V_{GS} (L=2μm)

The final two capacitors can be treated as constants, so do not need to be plotted:

$$C_{XD} = (6.486E-15)F \qquad (25)$$

$$C_{XS} = (6.486E-15)F \qquad (26)$$

VI. Simplifications Due to Application

Since the model being created here is to be used in a specific application, several simplifications can be made. These simplifications will be used when determining values for the current sources in the model, because, as will be seen, this is a much more complicated part of the modeling process. In order to determine what these simplifications are, the schematic must be examined. It appears in Figure 29. Please note that the aspect ratios given in this schematic are not the actual ratios used in the final design. The right and left parts of the schematic have been removed, as they contain information that is proprietary to Lockheed-Martin.

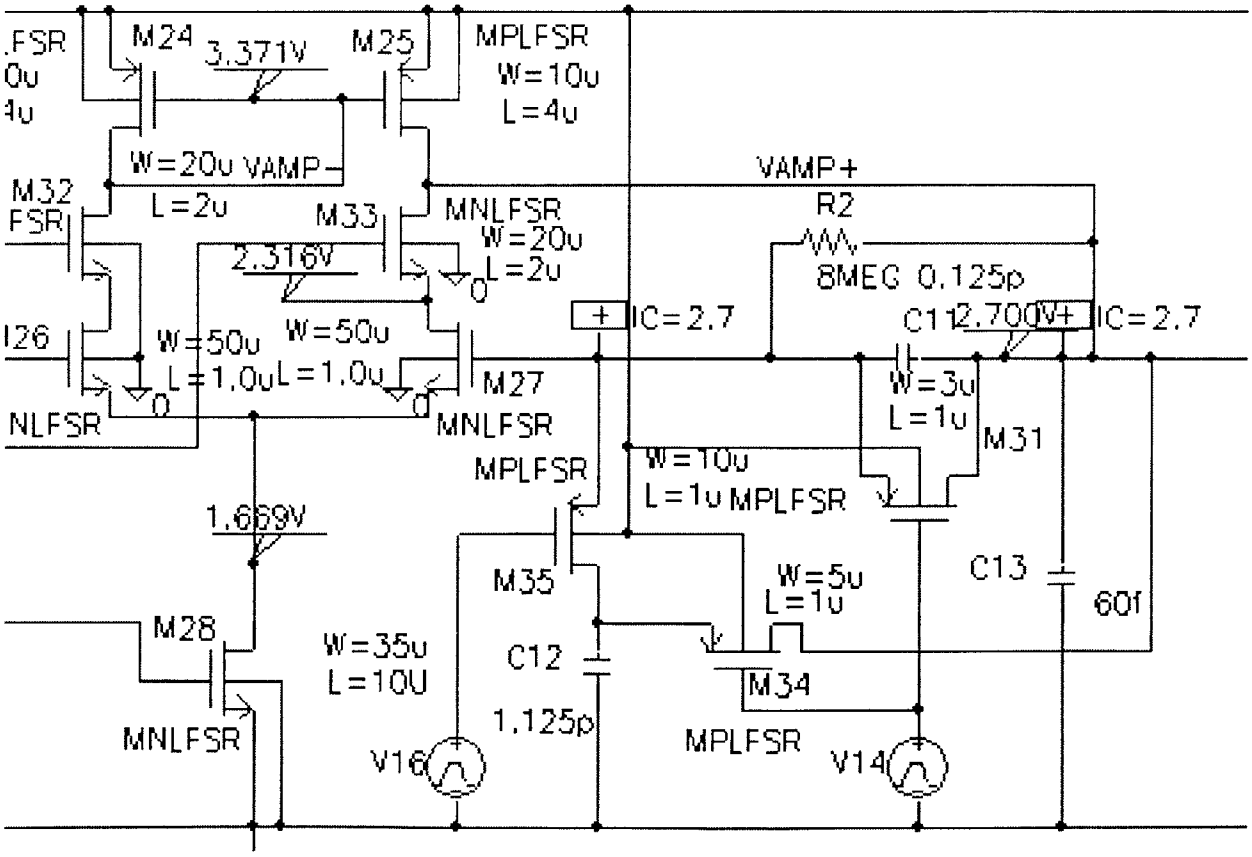

Figure 29: Schematic of TRIC Amplifier with SOI FETs

First, note that everywhere a FET (except the switching FETs) appears in this schematic, it is configured the same. That is, the back gate, body, and source are all tied together. Because of this, the model can be essentially turned into a two terminal device. Allen Hairston, the designer of the circuit, has also provided bounds on the actually occurring ranges of V_{GS} and V_{DS}. In this application, V_{DS} is constrained to always fall between 0.5 and 2.5 Volts. V_G is defined at the output of the amplifier as having a bias value of 2.5 Volts and a $\pm$ 2 Volt swing about that operating point. However, there is an amplifier with a gain of 2 between the output and the actual FETs being modeled. This means that the effective range of V_G that will actually be seen by the FETs being modeled here is from 1.5 to 3.5 Volts. The potential at the node where the source, bulk, and back gate are all tied will vary to keep VGS within approximately 1 to 2 V (the exact range will be discussed later). In the determination of values for I_{D1}, these ranges will be focused on in an effort to minimize error within them.

VII. Drain Current Equations

As was mentioned earlier, the fact that the devices being modeled are partially depleted thick film FETs offers a number of simplifications. However, it also renders useless all of the current models from the literature mentioned previously, as they focus on modeling fully depleted devices. The common feeling in SOI technology is that partially depleted devices can be best modeled using equations and methods for standard bulk FETs. However, as was shown earlier in the threshold voltage calculations, the equations for bulk FETs do not do a satisfactory job of modeling the test FETs from Allied Signal. This point will again be illustrated in the context of drain current.

Equations from the literature

The standard equation for drain current in a FET is very similar throughout the literature. The actual equations from Allen and Holberg have been chosen for this illustration. As with most texts, the equations here assume that, for V_{GS} below V_{T1}, there is absolutely no flow of current in the drain. For V_{GS} greater than V_{T1}, the equation is broken up into two pieces for the linear and saturation region. As previously mentioned, a variable V_{DSsat1} is created. When V_{DS} is greater than V_{DSsat1}, the device is in the

saturation region, and otherwise the device is in the linear region. This voltage V_{DSsat1} is given by the equation [13]:

$$V_{DS_{sat1}} = \left(\frac{V_{GS} - V_{T1}}{1-\alpha_1}\right) - \left[\frac{\lambda_1 (V_{GS} - V_{T1})}{2(1-\alpha_1)^2}\right] \tag{27}$$

where the parameter λ_1 is the inverse of the Early voltage, and α_1 is a parameter defined by the equation:

$$\alpha_1 = \frac{1}{C_{ox}} \sqrt{\frac{\varepsilon_{Si} q N_{SUB1}}{2(|2\phi_{f1}| - V_{BS})}} \tag{28}$$

The equations then are:

$$I_{Drift1} = \frac{\mu_0 C_{ox} W}{L_{eff}} \left[V_{GS} - V_{T1} - \left(\frac{V_{DS}(1-\alpha_1)}{2}\right)\right] V_{DS} \tag{29a}$$

$$I_{Drift1} = \frac{\mu_S C_{ox} W (V_{GS} - V_{T1})^2}{2 L_{mod1} (1-\alpha_1)} \left[1 + \lambda_1 (V_{DS} - V_{DS_{sat1}}) - \frac{\lambda_1^2 (V_{GS} - V_{T1})^2}{4(1-\alpha_1)^2}\right] \tag{29b}$$

Note that μ, the carrier mobility, is different in these two equations. This is to account for the fact that, once the device becomes saturated, the carrier mobility effectively decreases. These equations also involve another parameter, L_{mod}, which is included to account for channel length modulation effects. The equation for L_{mod} is

$$L_{mod} = L_{eff}(1 - \lambda_1 V_{DS}) \tag{30}$$

Allen and Holberg discuss methods for extracting the parameters that are used in these equations. As mentioned before, the SOI school of thought says that, because the devices being characterized are partially depleted and thick film, these techniques should apply well to the test devices. The extraction experiments were carried out, and the result is plotted in Figure 30, for a device of width 40 µm, length 5 µm, and a V_{DS} of 3 V.

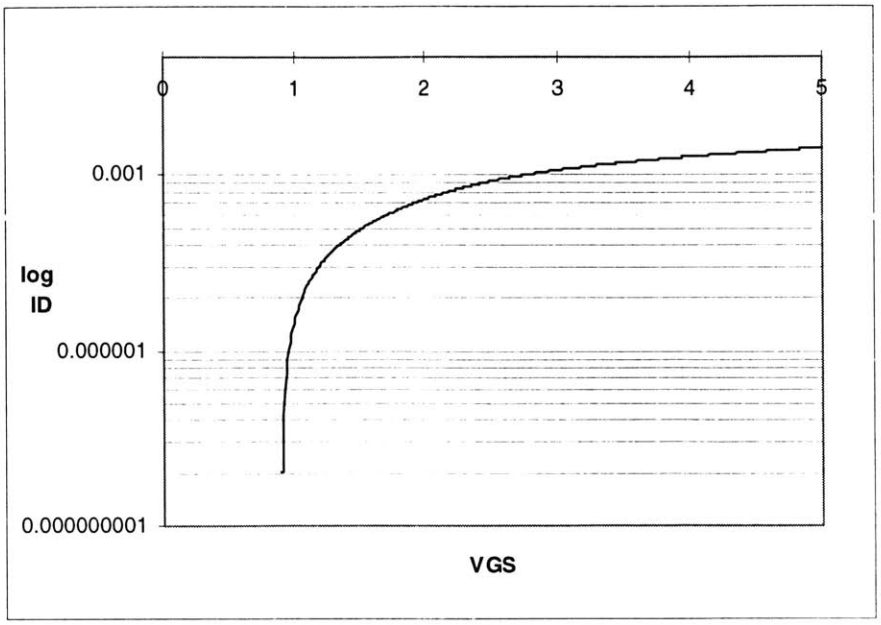

Figure 30: Allen & Holberg's drain current equation plotted

Of course, the assumption that there is no drain current for V_{GS} less than threshold is totally wrong. While several solutions to this problem have been suggested, a particularly attractive one is offered by Antognetti, et. al. Their method involves treating the drain current as the sum of a diffusion current component and a drift current component. The equations mentioned just previously are actually determinant of drift current; in Allen & Holberg's assumption, there is no diffusion current. In reality, however, for V_{GS} below threshold, the drain current is actually dominated by the diffusion current. The idea is to represent both components with their own equations, and then represent drain current as the sum of the two components.

The equations from Antognetti [14] appear below.

$$I_{diff1} = \frac{qD_n \eta_1 \overline{x_{d1} W}}{L_n \tanh \frac{L_{A1}}{L_n}} \left[1 - e^{\left(\frac{-qV_{DS}}{kT} \right)} \right] \frac{n_{s1} n_{x1}}{n_{s1} + n_{x1}} \tag{31}$$

where

$$L_{A1} = L - \sqrt{\frac{2\varepsilon_{Si} V_{DS}}{qN_{SUB1}}} \tag{32}$$

$$n_{x1} = X_{NA1} N_{SUB1} \tag{33}$$

$$n_{S1} = N_{SUB1} e^{\left[\frac{z_{a1} q (V_{GS} - V_{T1})}{kT\left(1+\frac{C_{S1}}{C_{ox}}\right)}\right]} \tag{34}$$

$$z_{a1} = 1 + z_1 \sqrt{V_{SB}} \tag{35}$$

$$\overline{x_{d1}} = \sqrt{\frac{\varepsilon_{Si} kT}{2q^2 N_{SUB1}\left[1+\frac{q(V_{SB}+0.5)}{kT}\right]}} \tag{36}$$

These equations work by treating the concentration of carriers in the channel as the parallel combination of two terms, one an exponential that dominates below threshold, and one a constant which dominates above threshold. Using a parallel combination picks the larger one of the two. The rest of the equation is simply there to model the constant dependencies upon V_{DS}, V_{SB}, and temperature.

In their article, Antognetti et. al. discuss other methods of extracting the necessary parameters in this equation. These experiments were performed, and the results plugged back into Equation 31. Assuming a V_{SB} of 0V, a V_{DS} of 3V, a width of 40 μm, a length of 5 μm, and a temperature of 300K, the equation for diffusion current is plotted below, along with the two pieces of the term describing channel carrier concentration.

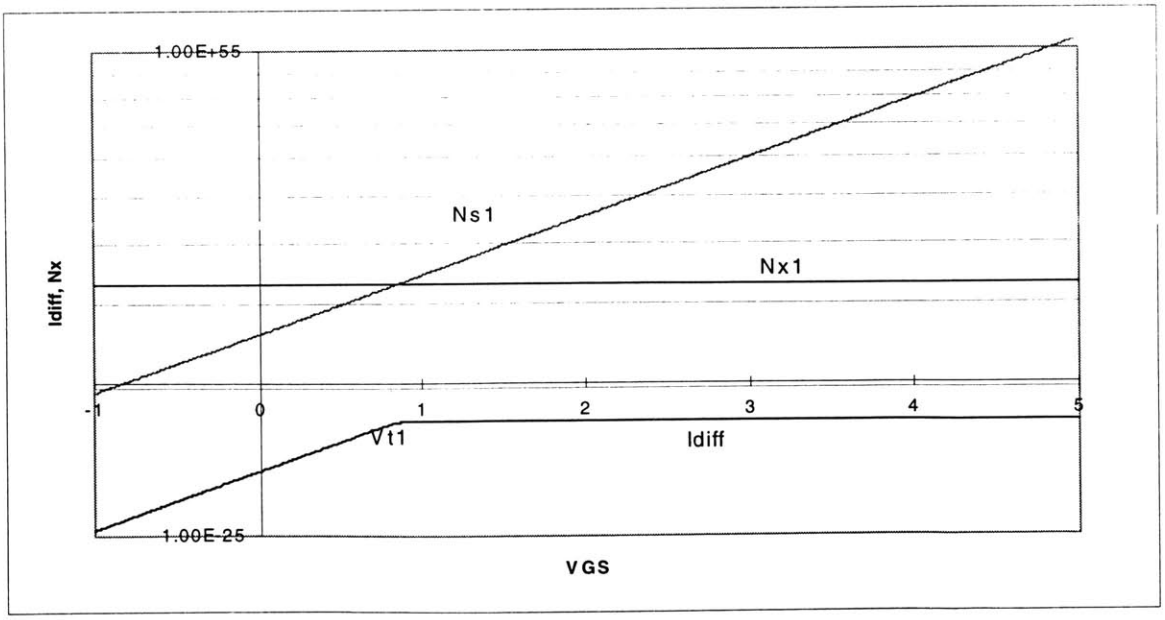

Figure 31: Plot of Diffusion current with carrier concentration terms

The drain current is now just the sum of the drift and diffusion current equations. Since I_{drift} is assumed to be zero at V_{GS} less than threshold, the final equation is actually in three pieces. When V_{GS} is less than V_{T1}, the drain current is solely I_{diff}. When V_{GS} exceeds V_{T1}, the drain current is I_{diff} added to the saturation region equation for I_{drift}. This saturation region equation is replaced by the linear region equation for I_{drift} when V_{DSsat} exceeds V_{DS}.

Again assuming a V_{DS} of 3V, a width of 40 μm, a length of 5 μm, and a temperature of 300K, this characteristic is depicted in Figure 32:

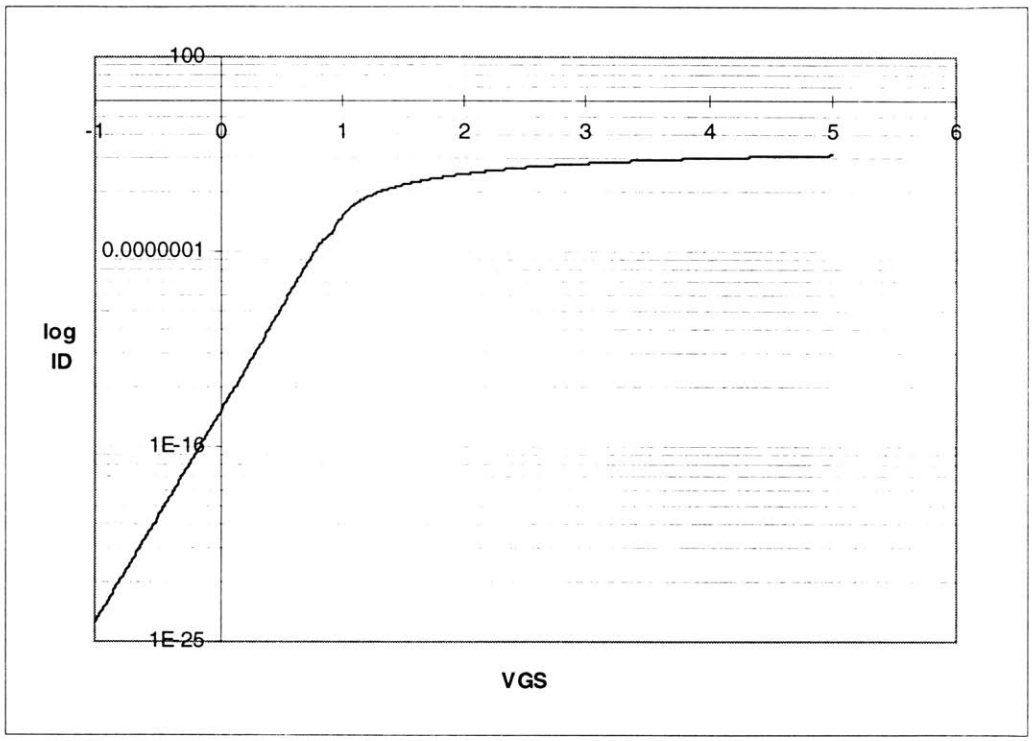

Figure 32: Total Drain Current Characteristic

Right away it can be seen that this equation will not work. Although the data itself is continuous, there is a huge discontinuity in the first derivative at $V_{GS} = V_{T1}$. This problem is so bad that it is visible to the naked eye, and can be sure to cause conversion problems with any computer simulation. Instead, a commonly used technique is to "RSS" these two equations together. Using this method, the drain current is computed to be the square root of the sum of the squares of the drift and diffusion components at any given V_{GS}. This is a valid method in this case, because the maximum value of diffusion current is orders of magnitude less than the drift current, hence the drain current above

threshold will still be nearly identical to Equation 29. Below threshold, where there is 0 drift current, the characteristic will obviously be identical. The only place that RSS should change the characteristic is about the point $V_{GS} = V_{T1}$, when the drift and diffusion components are on the order of each other. It hopefully should have the effect of smoothing out the discontinuity. The RSS version of the drain current equation is plotted in Figure 33:

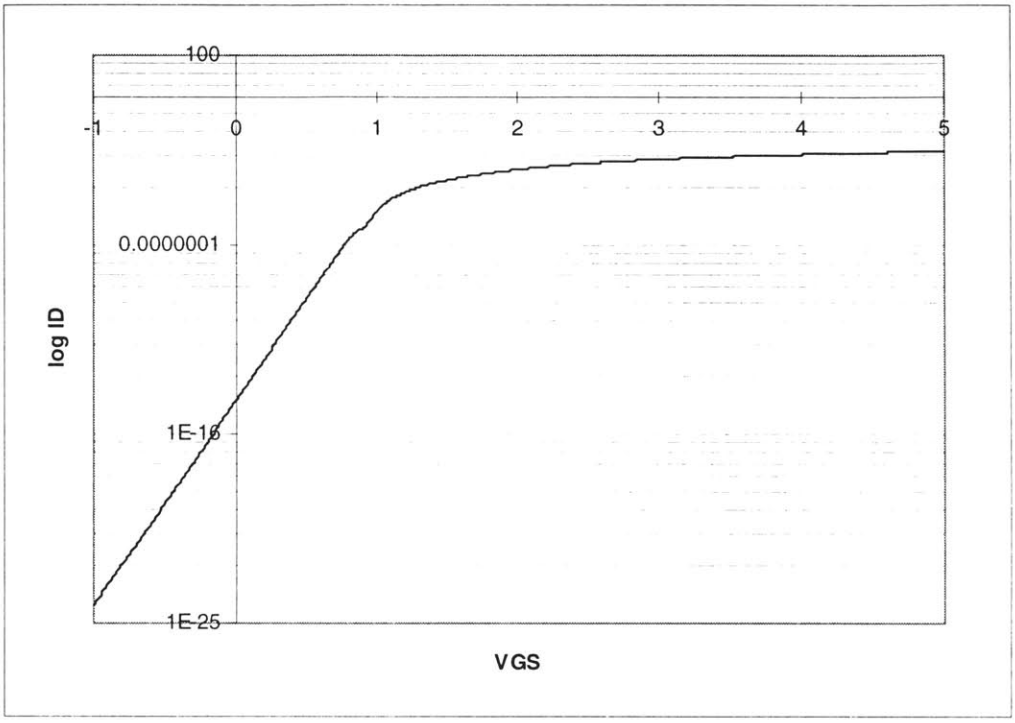

Figure 33: RSS Version of Drain Current Equation

As is shown, although this makes the problem better, it does not solve it. To see if there is anything useful in this equation, it is compared to actual data. For the same set of device and temperature assumptions used in the plotting of Figures 32 and 33, actual data was taken from a device with length of 5 μm. The test setup used a Hewlett-Packard 4145B Semiconductor Parameter Analyzer, and this setup is depicted in Figure 34.

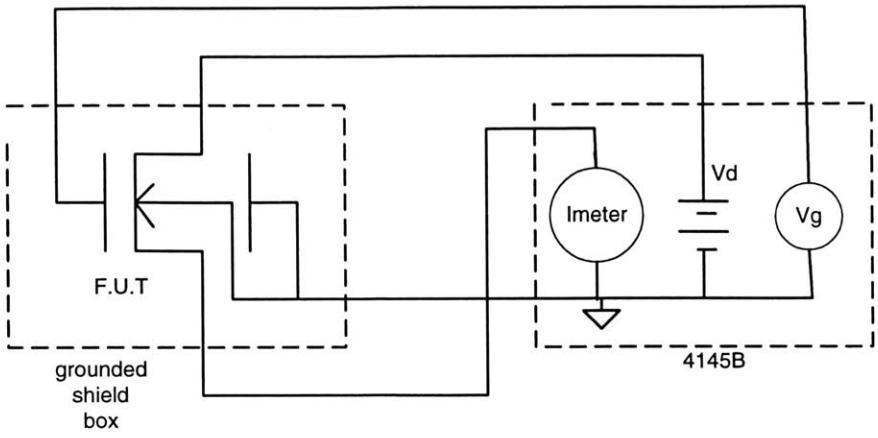

Figure 34: Test Setup for Drain Current Measurements

The taken data is plotted on the same set of axes as the RSS version of the drain current equation in Figure 33:

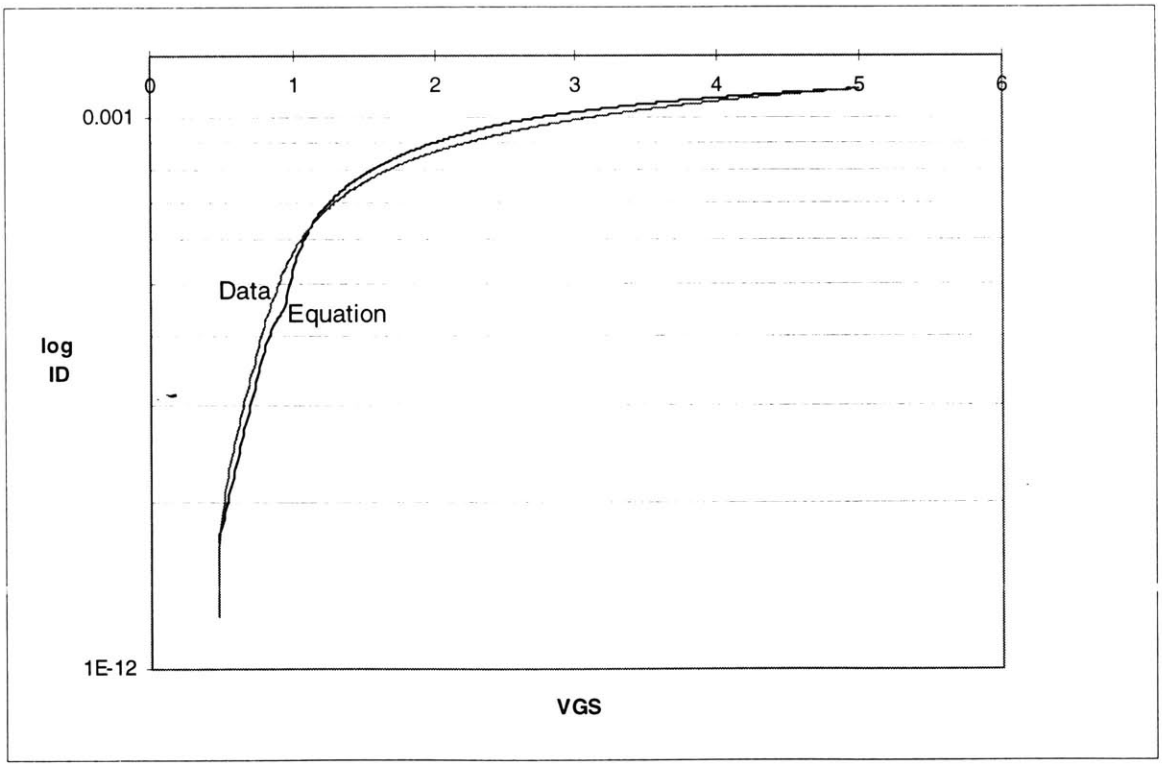

Figure 35: Drain Current Equation vs. Actual Data

The result is completely unsatisfactory. It is shown that even the general shape of the equation is not sufficient. Time was spent attempting to adjust the constants to get a closer match between the equation and the data, but all such attempts failed.

The point of this exercise is that the equations from the literature are simply inadequate to accurately model drain current in the device to be characterized. For this

reason, it is necessary to develop other methods for arriving at an equation that will be useful and accurate.

Process Specific Empirical Equations

The goal here is to synthesize an equation in the two terminal voltages of interest, V_{DS} and V_{GS}, for drain current, with the constraint that both the characteristic and it's first derivative will be continuous and it will vary from actual measured data by no more than ±3% throughout the ranges of $0.5<V_{DS}<2.5$ and $1<V_{GS}<2$. The range of V_{GS} through which the error must be minimized is not necessarily fixed at 1 to 2 volts. The lower edge of the range is fixed at 1 volt, as V_{GS} will never drop below this, but the upper edge of the range is determined more by the value of the drain current at which the devices will be normally biased. The bias current will never exceed 200 μA, so the upper edge of the V_{GS} range is defined as the value of V_{GS} at which the drain current is 200 μA.

Using this empirical approach to synthesize the drain current equation obviously requires data from one of the test FETs provided by Allied Signal. In determining which transistor to use, it is important to once again consider the actual devices to be used in the circuit. The amplification FETs being modeled here are going to be 52 μm wide and 1.8 μm long. This yields an aspect ratio of 28.889. Of the test FETs available, the FET with a length of 1.6 μm has an aspect ratio of 25, and the FET with a length of 1.2 μm has an aspect ratio of 33.33. Therefore, the equation will be synthesized with data taken from the 1.6 μm long transistor, and then this equation will be checked on the 1.2 μm long device to make sure that it scales appropriately with device aspect ratio.

The drain current was measured on the test device while the gate to source voltage was swept from 1 V to 2 V. The measurement was repeated while V_{DS} was stepped every half of a volt from 0.5V to 2.5V. The measurements were made once again with the Hewlett-Packard 4145B Semiconductor Parameter Analyzer; the test setup was identical to that in Figure 34.

Once the data had been taken, the first step was to determine what analytical shape the data would take. The strategy for determining this shape was to guess a term and then plot the error between the measured data and this term. Then, a new term which matched this error would be subtracted from the original term. Once again, the error

would be plotted, and a term found to match this new error. This term would in turn be subtracted from the first two, and so on until acceptable error percentages had been achieved. In determining the shape of the equation, the data for V_{DS} = 1.5V was used.

When V_{DSsat} is greater than V_{DS}, a linear term dominates the drain current equation. Using this linear term in the appropriate region generates an error between the data and this linear term that is very small for large V_{GS} and then tails downward exponentially when V_{DSsat} drops below V_{DS}. This was undesirable due to the fact that a continuous equation was desired and compensating for this error term would involve two separate regions in the drain current equation. However, it was found that in effect "sliding" the linear term down the characteristic so that it exactly equaled the data at either end of the V_{GS} range of interest provided an error which was very close to parabolic. Such an error term was easy to compensate for with another continuous term, not requiring the addition of a separate region, and thereby avoiding the possibility of a discontinuous characteristic or derivative.

Therefore, the first term tried was a linear term of the form $A(V_{GS}-V_{T1})$. The number A was chosen to make the term match the data exactly at V_{GS} = 1.5V. This term has been plotted with the measured data in Figure 36:

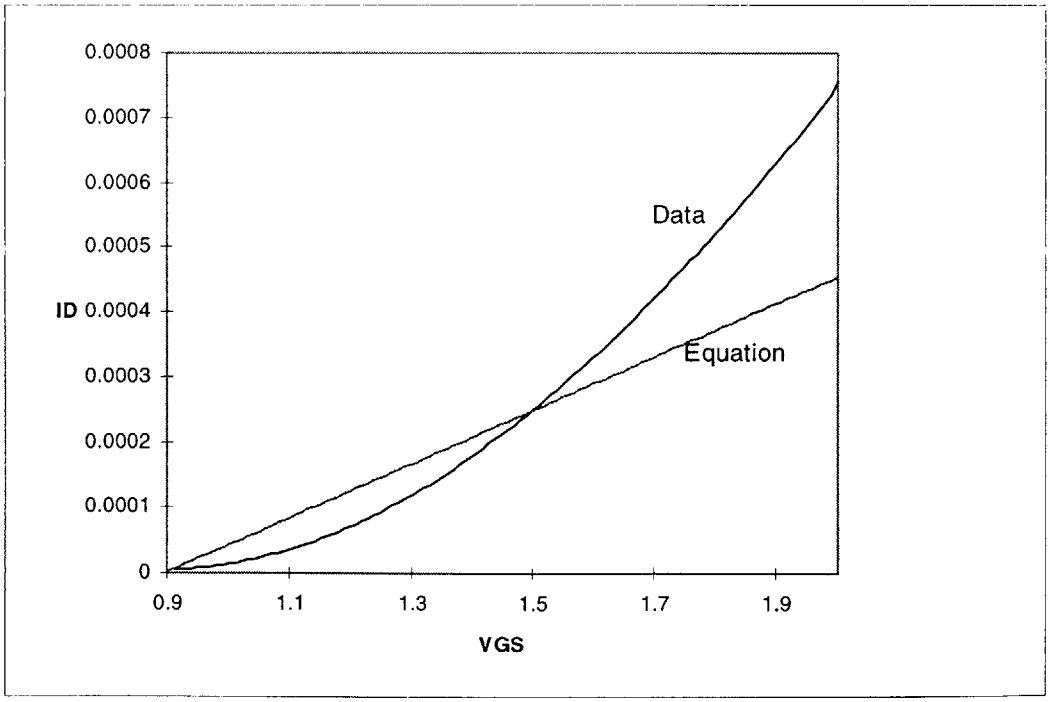

Figure 36: First Equation Term and Measured Data (V_{DS}=1.5V)

The error between the linear term and the data has an easily definable parabolic form. This error is plotted vs. V_{GS} in Figure 37:

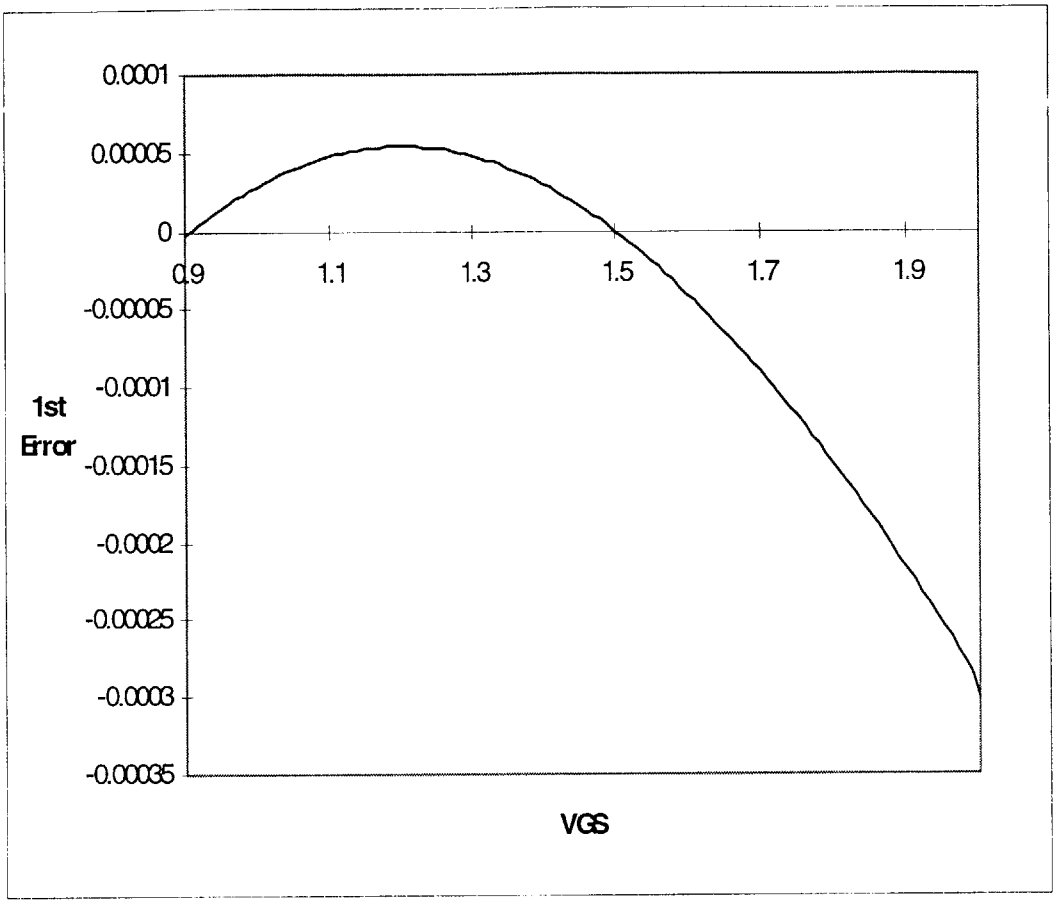

Figure 37: First Term Error vs. V_{GS} (V_{DS}=1.5V)

Next, it was necessary to determine a second term which matched this error as closely as possible. A parabolic term was obviously the first guess. This term is of the form $-B(V_{GS}-C)^2 + D$. C is chosen to be the value of V_{GS} at which the first error term is at a maximum. This way, the parabolic term will line up correctly with this error. D was chosen to be equal to the maximum value of the first error term, and provides the offset necessary to the parabolic term. B was chosen last in order to make the parabolic term match as closely as possible with the first error term. For V_{DS} equal to 1.5 V, this parabolic term appears below, plotted with the first error term for this value of V_{DS}:

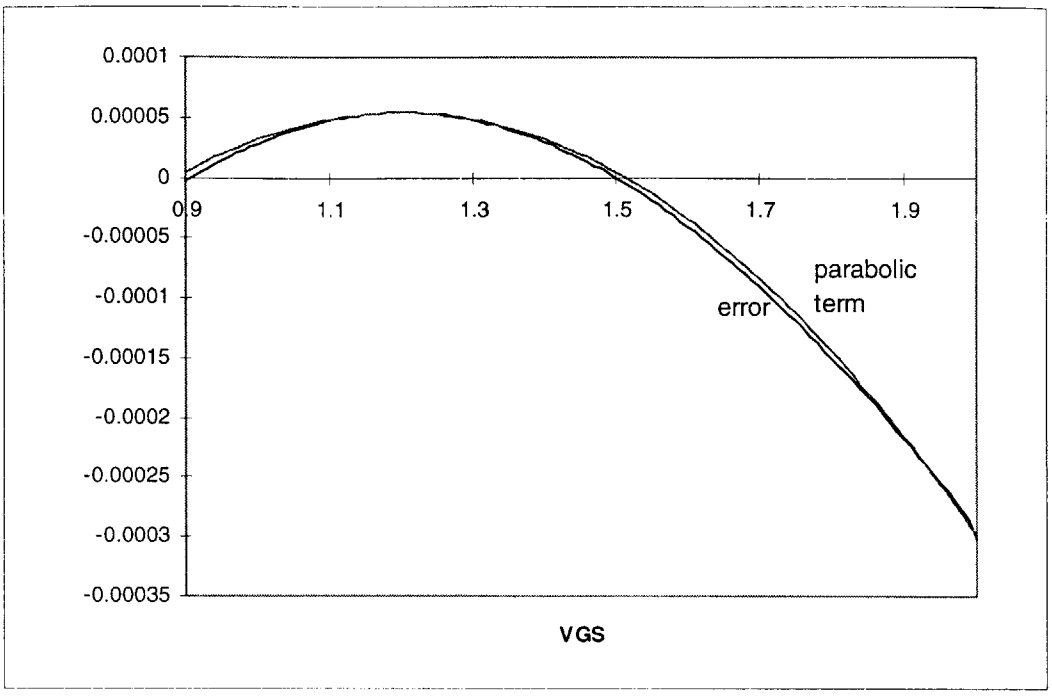

Figure 38: Parabolic Term and First Term Error vs. V_{GS} (V_{DS}=1.5V)

It is important to note that the left hand side of the parabolic term does not match closely with the error. This is important, as this mismatch generates the second error term, which is plotted below.

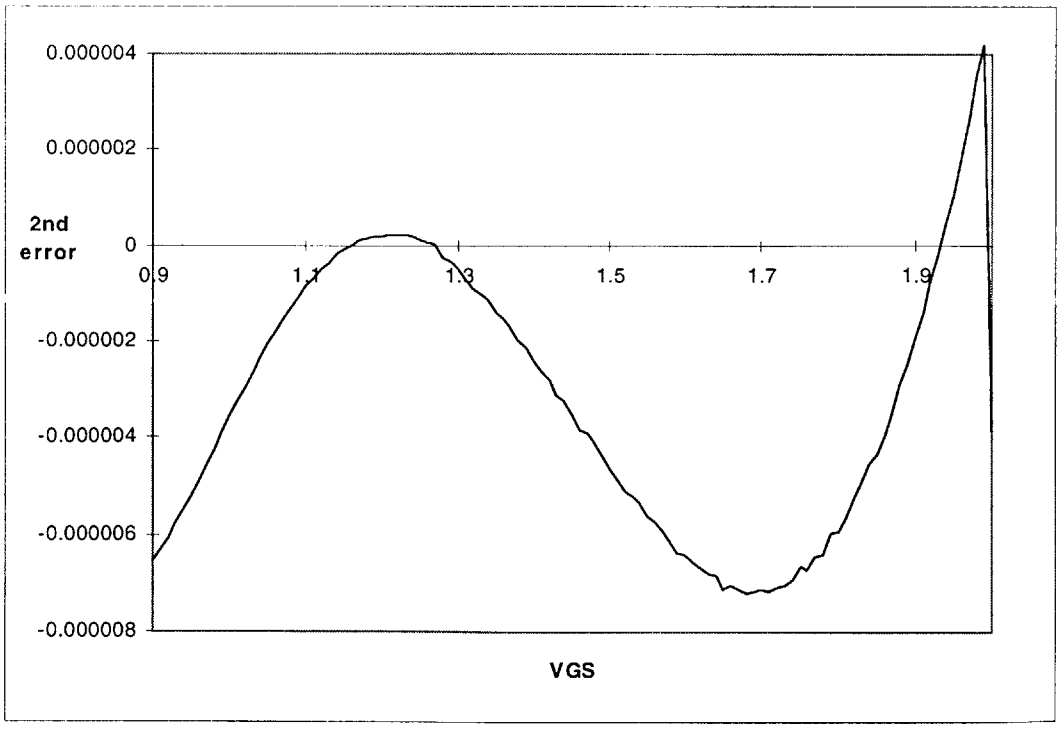

Figure 39: Second Term Error vs. V_{GS} (V_{DS}=1.5V)

This error term is not quite so easily definable as the first error term. For V_{GS} less than C (as it was determined in the parabolic term), the error appears parabolic again. However, for V_{GS} greater than C, the error is very ill defined in terms of standard equation shapes. This, though, turns out to be inconsequential. That is because the value of the drain current for these values of V_{GS} is high enough that this error fits within the ±3% boundary chosen before. When V_{GS} is lower than C, the drain current is smaller and the error is bigger, therefore the error percentage is unacceptable. The result of this is that the only part of this second error term that needs to be compensated for is the portion that occurs for V_{GS} less than C. The problem that this causes is that the third term only has to be added for $V_{GS} < C$. This means that, despite efforts otherwise, a second region will need to be established. $V_{GS}=C$ will be defined as the boundary between the two separate drain current equations. It is necessary to make sure that the transition from one equation to the other is not only continuous, but that it's first derivative is also continuous.

This error again appears to be parabolic. However, the exponent is not a two, as was the case with the previous parabolic term. Therefore, the new term in the equation takes the form $-E(C-V_{GS})^F$. E and F are chosen by trial and error iteration in the following manner; first a value of F is chosen, and then E is chosen to make this term equal to the second error term at V_{GS} equal to 1 V. Then the term is checked to make sure that it tracks the error well between 1V and C. If not, a new value of F is tried and a new value of E determined, until the match between this term and the error is acceptable. The finished term is plotted with the second error term in Figure 40 below:

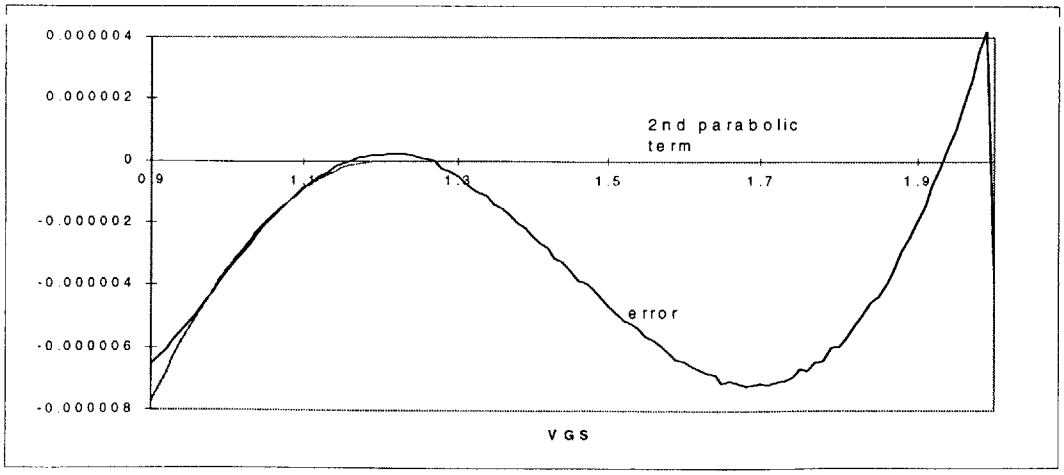

Figure 40: Second Parabolic Term and Second Error Term vs. V_{GS} (V_{DS}=1.5V)

One important thing to note is that, at V_{GS}=C, this second parabolic term is zero, as is it's derivative. This means that the transition from one equation to the next will meet the requirements mentioned above. This third term is subtracted from the first two, and once again this sum is compared to the measured data. The new error is plotted below:

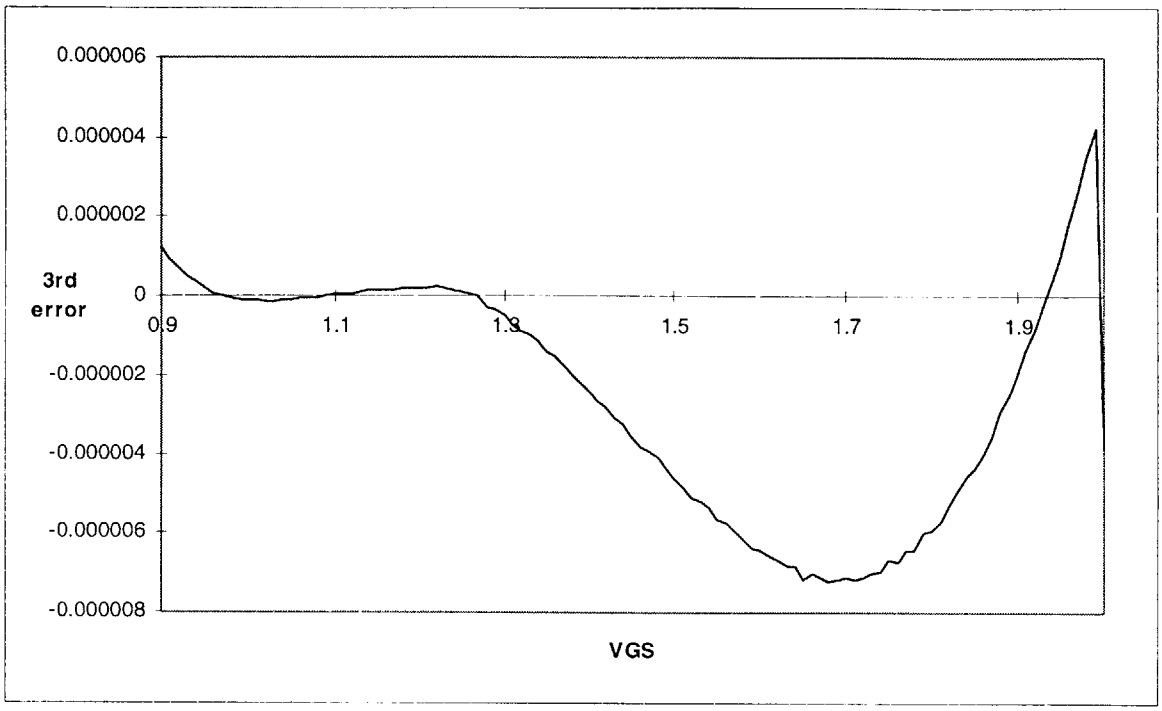

Figure 41: Third Error Term vs. V_{GS} (V_{DS}=1.5V)

This error, when converted to percentage, falls within the ±3% window. Therefore, the final shape of the equation is:

$$I_D = A(V_{GS} - V_T) + B(V_{GS} - C)^2 + E(C - V_{GS})^F - D; \qquad V_{GS} \leq C \qquad (37a)$$

$$I_D = A(V_{GS} - V_T) + B(V_{GS} - C)^2 - D; \qquad C \leq V_{GS} \qquad (37b)$$

V_{DSsat} turns out to not be an important factor in this equation at all, so it can be forgotten for the purposes of this model. Instead, C is the voltage which determines which equation will be used for drain current.

Now that the shape of the equation has been determined, it is necessary to determine the values of the parameters A, B, C, D, E, and F. These parameters will depend on V_{DS}. To determine this dependence, the parameters were determined for each value of V_{DS} that data was taken at, and then these determined values were plotted vs. V_{DS} in an attempt to come up with an equation in V_{DS} which matched these determined

values. The first parameter to be determined is A. The values for A vs. V_{DS} are plotted below.

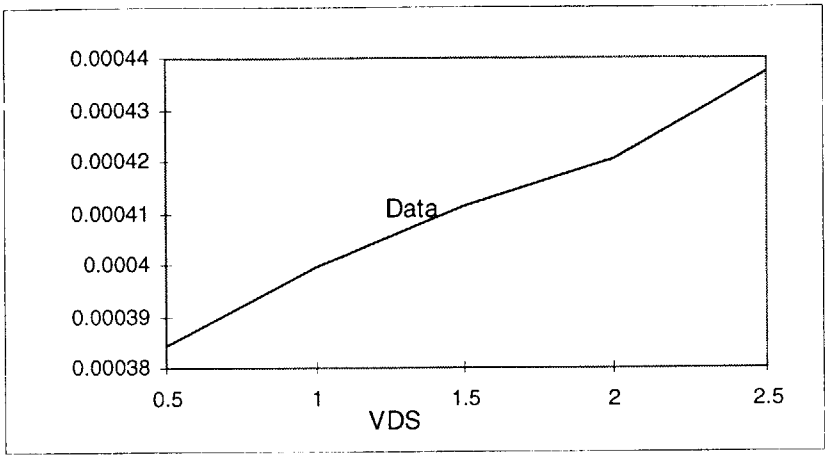

Figure 42: Parameter A vs. V_{DS}

A was found to be almost linear in V_{DS}, so a linear solution was tried. The equation that was found was:

$$A = (2.39794E-5)V_{DS} + (3.73942E-4) \tag{38}$$

This equation is plotted with the determined values of A below:

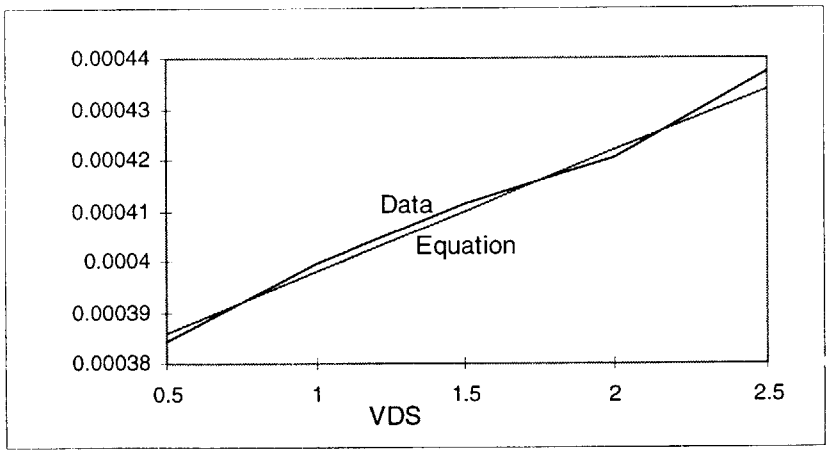

Figure 43: A and Equation vs. V_{DS}

The values of A from the Equation 38 were inserted into each data series and the error was plotted, in effect using the calculated values of A to determine the next constants, B and C. Interestingly, both B and C were found to be constant and independent of V_{DS}. Their values are B = $(5.5*10^{-4})$ and C = 1.2V. These values were also placed into the equation, and this new equation was used to calculate the next parameter, D.

The determined values for D are plotted below vs. V_{DS}:

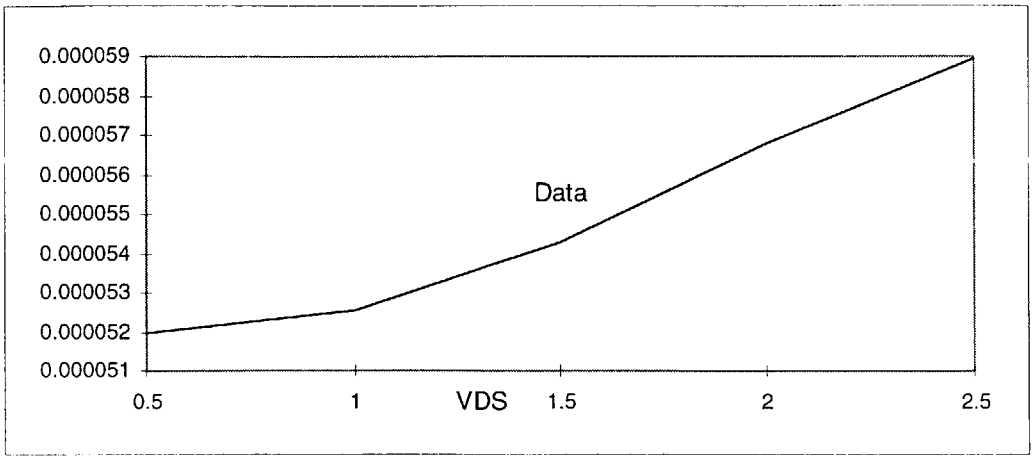

Figure 44: Parameter D vs. V_{DS}

The characteristic for D appeared to be parabolic in V_{DS}, with an offset. The following equation for D was determined:

$$D = \left[(2.1E-6)(V_{DS}-0.5)^{1.75}\right] + (5.19999E-5) \tag{39}$$

This equation is plotted with the measured values in Figure 45 below:

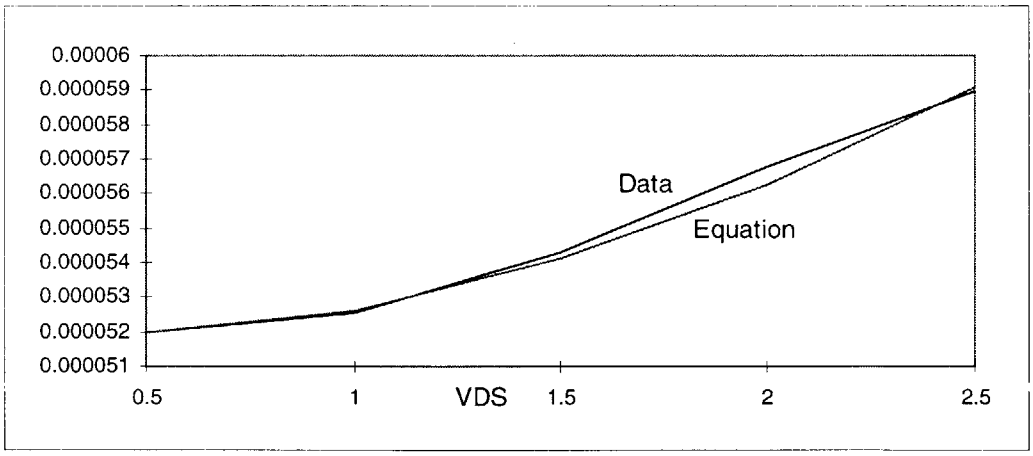

Figure 45: D and Equation vs. V_{DS}

Once again, the values yielded by Equation 39 were inserted into the different equations, and these were once again used to determine the remaining two parameters, E and F. The measured values of E and F appear in Figures 46 and 47 below:

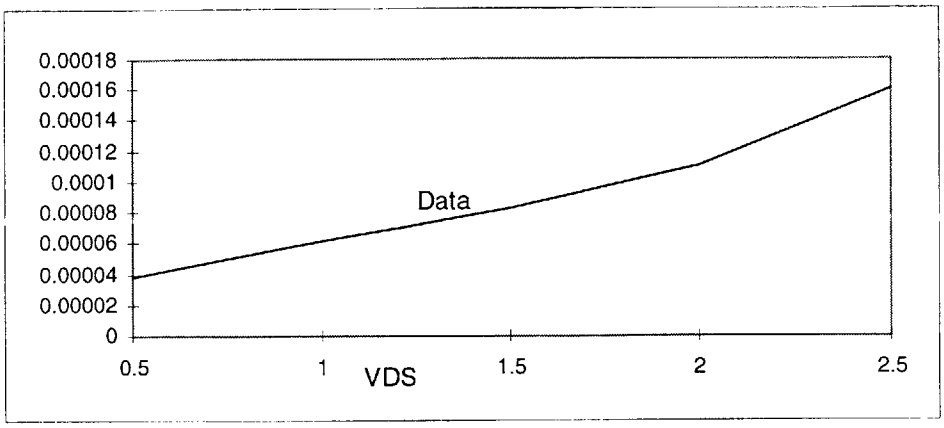

Figure 46: Parameter E vs. V_{DS}

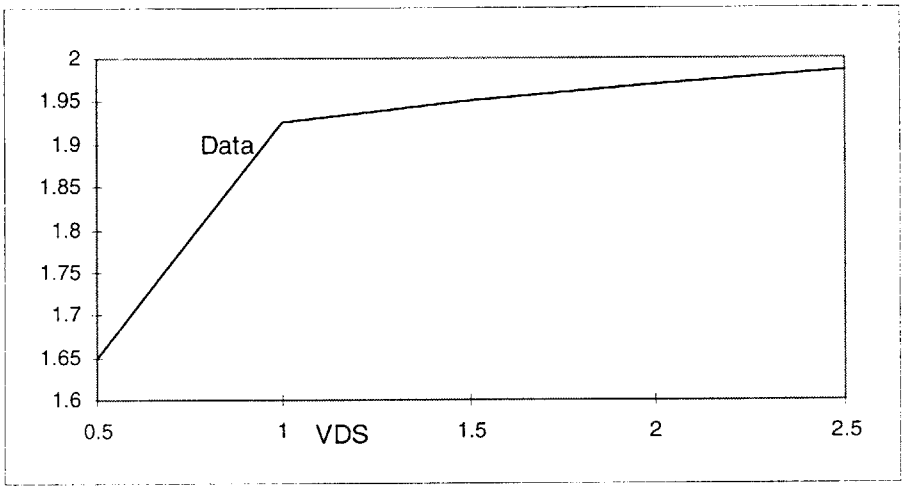

Figure 47: Parameter F vs. V_{DS}

Both of these parameters also appear to be parabolic. The equations which were determined are:

$$E = \left[(4.5E-5)(V_{DS}-0.5)^{1.4}\right] + (3.83872E-5) \tag{40}$$

$$F = -\left[(1.045E-2)(2.5-V_{DS})^{5}\right] + 1.985 \tag{41}$$

These equations are plotted with their measured values vs. V_{DS} below:

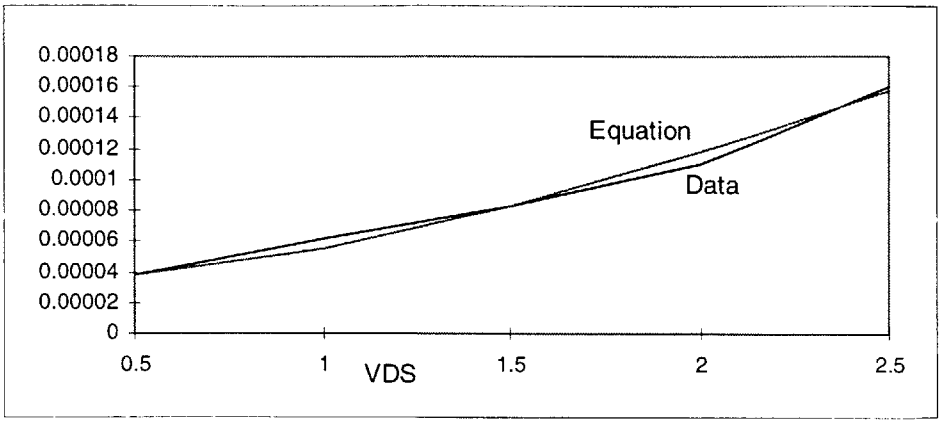

Figure 48: E and Equation vs. V_{DS}

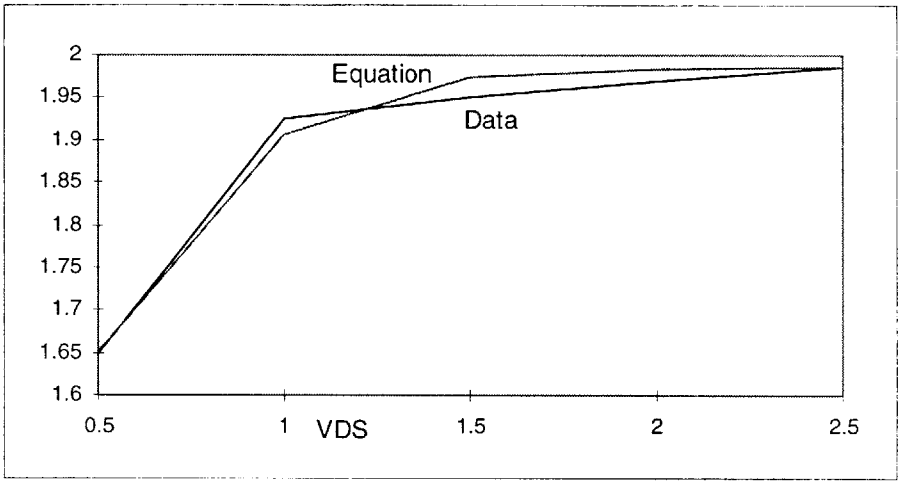

Figure 49: F and Equation vs. V_{DS}

It is reasonable to assume that, by using V_{DS} stepped at every half of a volt, there are no local maxima or minima in the above characteristics that would render them inaccurate. In other words, the equation determined above holds over the entire range of interest of V_{DS}. The error percentages between the equation and the data at each value of V_{DS} all fall within ±3% for the range of interest of V_{GS}. Therefore, the final equation for drain current is given by Equation 37, using the equations for the parameters determined above.

The only remaining factor to take into account is the aspect ratio. This should appear as a strictly multiplicative factor in front of Equation 37. To test this, the drain current vs. V_{GS} characteristic was taken from the device with a length of 1.2 μm. This device has an aspect ratio of 33.333, which is 1.3333 times the aspect ratio of the 1.6 μm long device used to extract the equation. Therefore, the whole drain current equation was

multiplied by 1.3333, and compared with the data taken from the 1.2 μm long device. The error percentage is plotted below vs. V_{GS}:

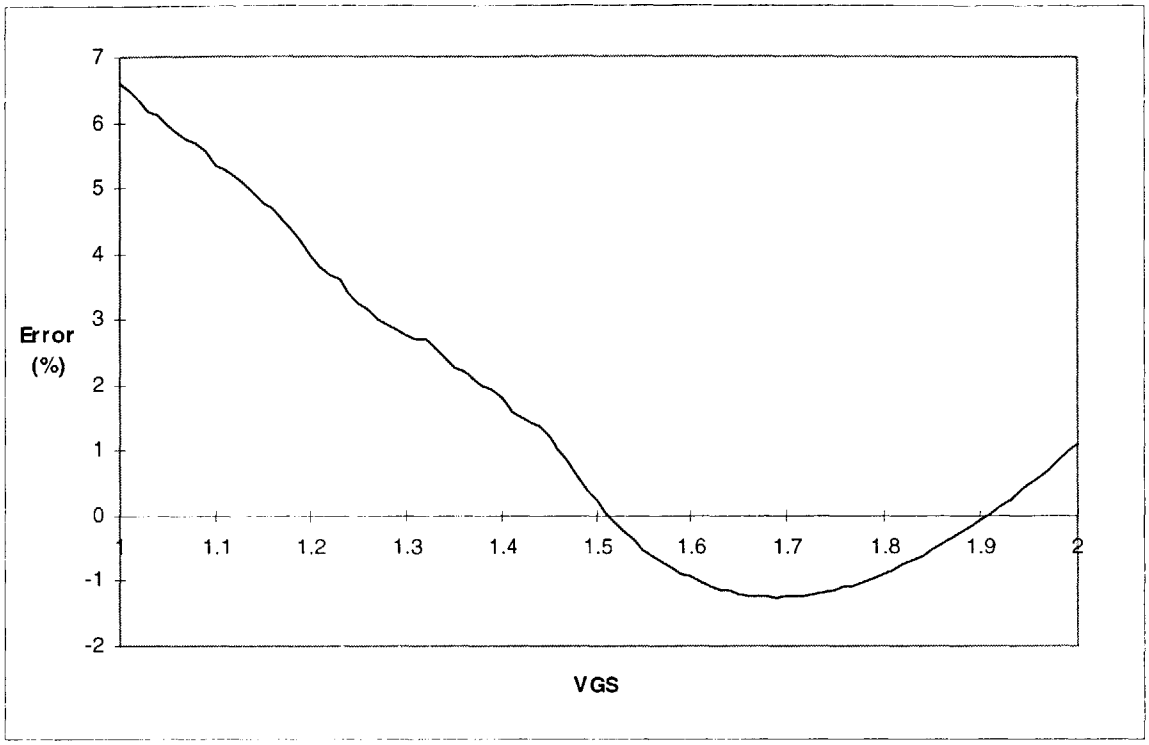

Figure 50: Equation Error vs. V_{GS} (V_{DS} = 1.5V, L = 1.2 μm)

For high V_{GS}, the error percentage is minimal. However, as V_{GS} approaches 1V, the error rises to approximately 6%. This is most likely due to the onset of some sort of weak inversion exponential term that was not captured in the equation. Still, this result is acceptable, since the entire window of error percentage is not much greater than the 6% originally specified. Since the target aspect ratio of the devices to actually be used falls between that of the 1.2 μm and 1.6 μm devices, it can be assumed that the error percentage will be better than this for the target aspect ratio. Therefore, the equation is deemed a successful one.

The last thing to do is to normalize this equation to include aspect ratio. This is accomplished simply by dividing Equation 37 by the aspect ratio of the 1.6 μm long device. In summary, the drain current is given by the following set of equations:

$$I_D = \left(\frac{R}{25}\right)\left[A\left(V_{GS} - 0.895\right) + (5.5E-4)\left(V_{GS} - 1.2\right)^2 + E\left(1.2 - V_{GS}\right)^F - D\right] \text{ ;} V_{GS} \leq 1.2 \quad (42a)$$

$$I_D = \left(\frac{R}{25}\right)\left[A(V_{GS} - 0.895) + (5.5E-4)(V_{GS} - 1.2)^2 - D\right]; \quad 1.2 \leq V_{GS} \quad (42b)$$

$$A = (2.39794E-5)V_{DS} + (3.73942E-4) \quad (43)$$

$$D = \left[(2.1E-6)(V_{DS} - 0.5)^{1.75}\right] + (5.19999E-5) \quad (44)$$

$$E = \left[(4.5E-5)(V_{DS} - 0.5)^{1.4}\right] + (3.83872E-5) \quad (45)$$

$$F = -\left[(1.045E-2)(2.5 - V_{DS})^5\right] + 1.985 \quad (46)$$

where R is the aspect ratio (W/L) of the device and V_T, the threshold voltage, is equal to 0.895V.

Although this equation is empirical, it does make physical sense. The presence of the linear term has been argued above. The term involving $(V_{GS}-C)^2$ makes sense also, because of the fact that the region being modeled is somewhat between the saturation and linear region (depending on the value of V_{DS}), and a square term dominates the equations in the literature while in the saturation region. Lastly, the final term makes perfect sense. The half-parabola looks almost like an exponential, and this exponential behavior is expected as V_{GS} approaches threshold. Even the value of C, 1.2 V, fits perfectly. Referring to the plot above of the equation from the literature, it can be noted that V_{GS}=1.2V is approximately where the analytical shape of the equation begins to deviate from the data. This proves that, at this point, the moderate inversion exponentials which are disregarded in the literature equations begin to come into play. Therefore, the addition of the third term (which is reminiscent of an exponential) at this point makes perfect physical and empirical sense. The result is an equation which, though it may look purely empirical, is backed up by the physical evidence on hand.

VIII. Noise Properties

It is necessary, especially in terms of the small signal model, to determine the voltage noise referred to the gate of the FET. Once this has been determined, an equivalent voltage source can be added to the gate of the small signal model to accurately and easily include noise in the model for the transistor.

In a typical FET, referred-to-input, or RTI, noise usually consists of two pieces. In the low frequency range, this noise is dominated by 1/f noise, so called because it follows a 1/f rolloff all the way across the frequency spectrum. The other chief component, that dominates the noise at higher frequencies, is thermal, or Johnson noise. The value of this noise depends on the transconductance of the device, and therefore on the bias current. The equation for Johnson noise in a FET is

$$V_n = (F-1)\sqrt{\frac{8kT}{3g_m}} \tag{47}$$

where F is defined as the "noise factor" and can vary anywhere from about 2 to about 5, and which must be experimentally determined.

Measurement

The test setup for determining input referred noise in a FET is shown in Figure 51 below:

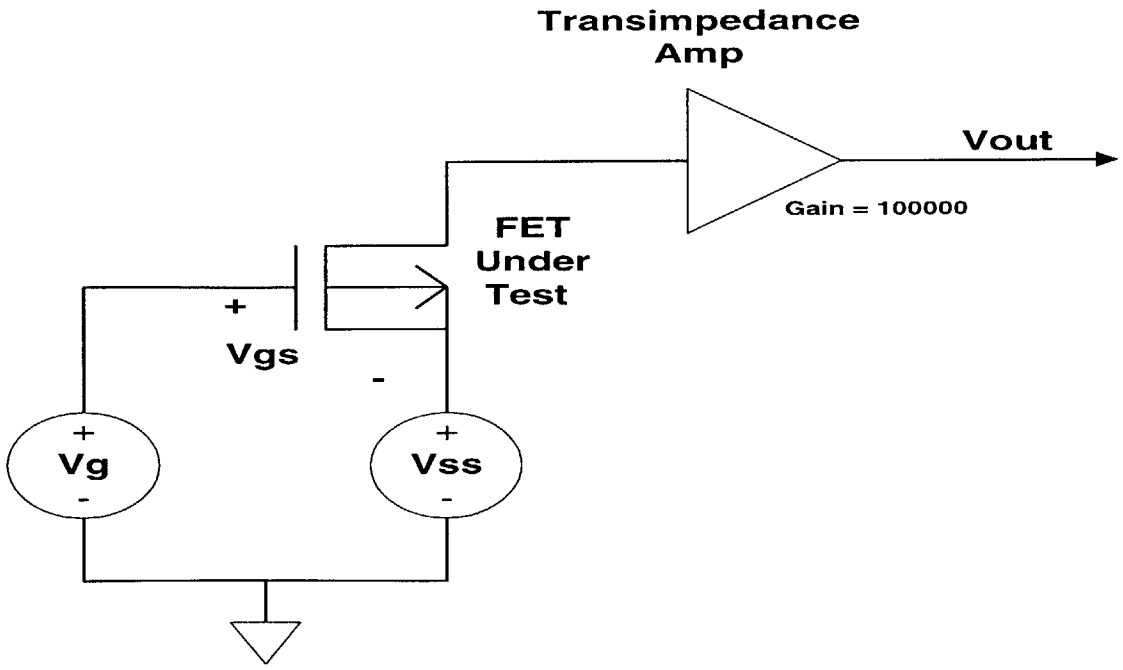

Figure 51: Schematic for Measurement of FET Noise

The method devised for the noise test involved placing the FET into the simple source follower configuration pictured in Figure 51. The bias drain current is adjusted by changing Vgs, and can be determined by dividing the output voltage of the transimpedance amp by the amplifier gain. The procedure involves, for each current:

1. Set a bias current for the transistor.
2. Measure the voltage noise at the output of the transimpedance amplifier.
3. Refer that data to the input of the FET.

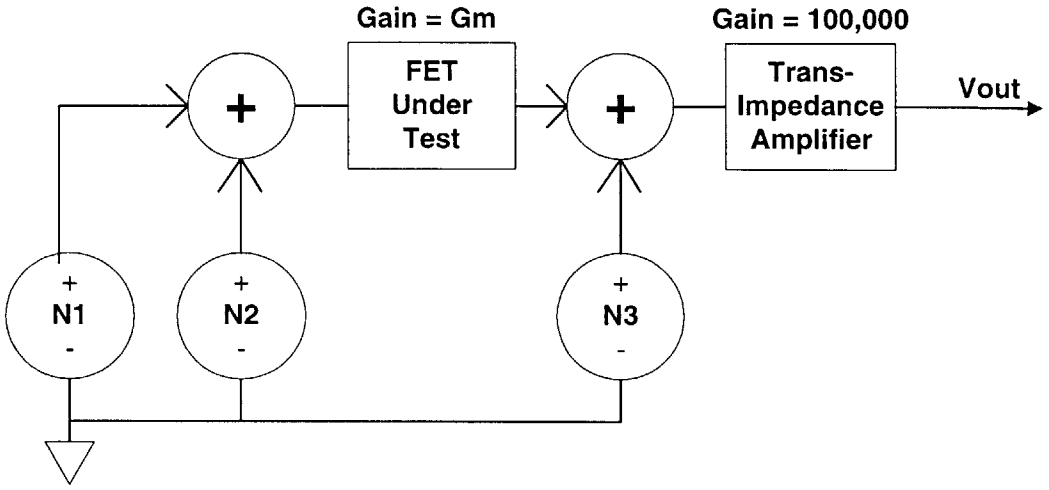

Figure 52: Test Setup Noise Model

While taking the output referred noise data was relatively straightforward, referring that figure to the FET input required the measurement of the noise of the transimpedance amp, the power suppy, and the spectrum analyzer as well as the forward transconductance (g_m) of the FET under test.

The FET used for this study was one with a width of 40 μm and a length of 2 μm. Four bias drain currents were chosen for testing to represent a span of likely operating conditions. These currents were 4.5, 10.5, 16.5, and 25.5 μA. The g_m measurement procedure is:

1. Inject a 20 mV peak-to-peak sine wave into the gate of the FET.
2. Measure the amplitude of the sine wave at the output of the amplifier.
3. Divide by the input voltage and the gain the amplifier to yield FET gain at that frequency.

To measure the additive noise from the different test setup components, they were disconnected from the FET and connected to the spectrum analyzer. First, the noise at the output of transimpedance amplifier was measured. This measurement was taken to include both amplifier and analyzer noise. Dividing this figure by the gain of the amplifier, 100,000 V/A, yields the referred to input (RTI) noise of the amp/analyzer combination, in nA/rtHz. This is represented in Figure 52 as N3. The measurement of power supply noise was also relatively straightforward. By testing, it was found that changing V_{SS} had no effect on the drain current when V_{GS} was held constant, so the V_{SS} supply was not considered in the analysis. The noise from V_{GS} was measured by connecting the leads of the spectrum analyzer to the battery/resistor divider power supply (a battery was chosen as a power supply because of it's extremely low noise relative to line-driven hardware). This noise is represented in Figure 52 as N2. The desired quantity, RTI FET noise, is designated as N1.

Once these measurements had been obtained, calculating the RTI FET noise was done in the following manner (please refer to Figure 52):

1. Measure the rms noise at Vout.
2. Divide this figure by 100,000 V/A, the transimpedance amplifier gain.
3. Subtract N3 using the square root of the difference of the squares.
4. Divide by the FET transconductance at the bias current and frequency of interest.
5. Subtract N2 using the square root of the difference of the squares. These steps can be summarized by the following equation:

$$N1 = \sqrt{\left[\frac{\left(\frac{N_{Vout}}{100000}\right)^2 - N3^2}{g_m^2}\right] - N2^2} \qquad (48)$$

This measurement and calculation was performed for each of the four drain currents of interest. Figure 53 below depicts the noise characteristics from the testing versus frequency, for each of the four drain current values. Also included in the graph are the theoretical Johnson noise levels for the four test currents, assuming a noise factor F of 2.

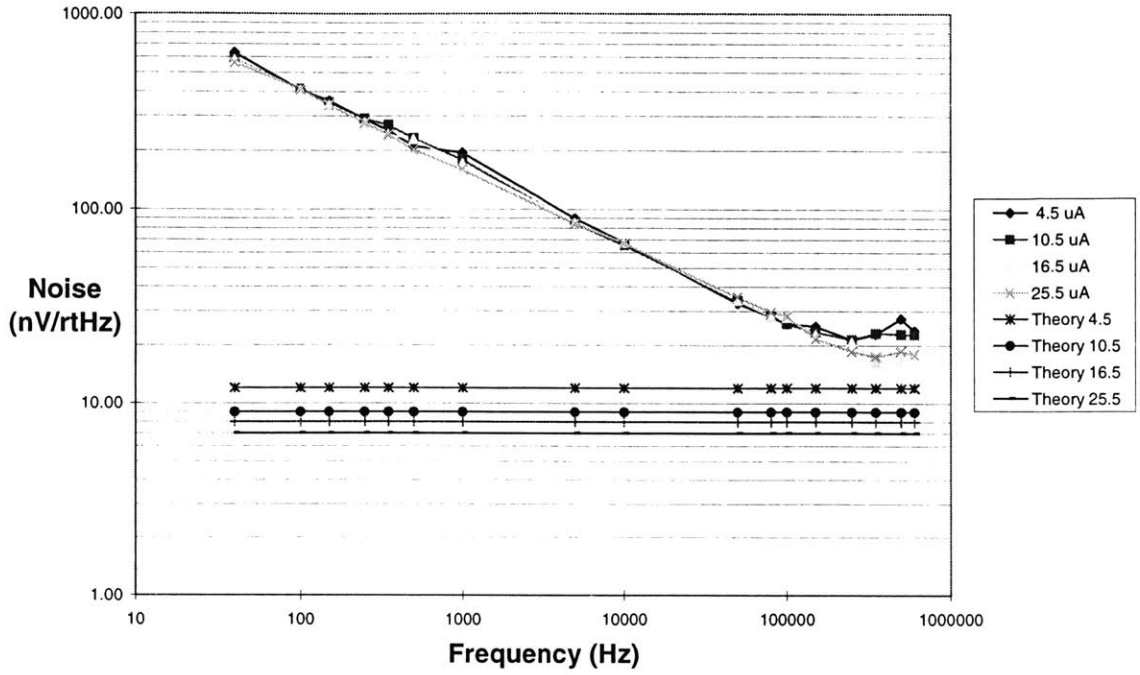

Figure 53: FET RTI Noise vs. Frequency (L=2μm)

This graph immediately appears as expected. At low frequency, all four characteristics have identical values and show a 40 dB/decade rolloff. This rolloff is consistent with that of 1/f noise, and the fact that the four data sets are identical is also good, as the value of 1/f noise does not depend on g_m, or therefore on I_D. The noise rolls off at a corner frequency of approximately 200 kHz. This does not pose a problem, since the target system frequency of 3 MHz is much greater than this number.

After the rolloff, the noise levels do appear to be I_D dependent, as is expected of Johnson noise. The values of the measured flatband noise are about 2.5 times the theoretical Johnson noise terms that were plotted here, which leads to a noise factor, F, of 3.5. This is all that is required for a complete characterization of the frequency dependent noise. The corner frequency of the 1/f rolloff is 200kHz, and the noise factor, F, for the Johnson noise is 3.5.

Faccio, et. al. [15], discuss a third component of noise which consists of an extra "hump" in the noise vs. frequency characteristic, as shown below in Figure 54.

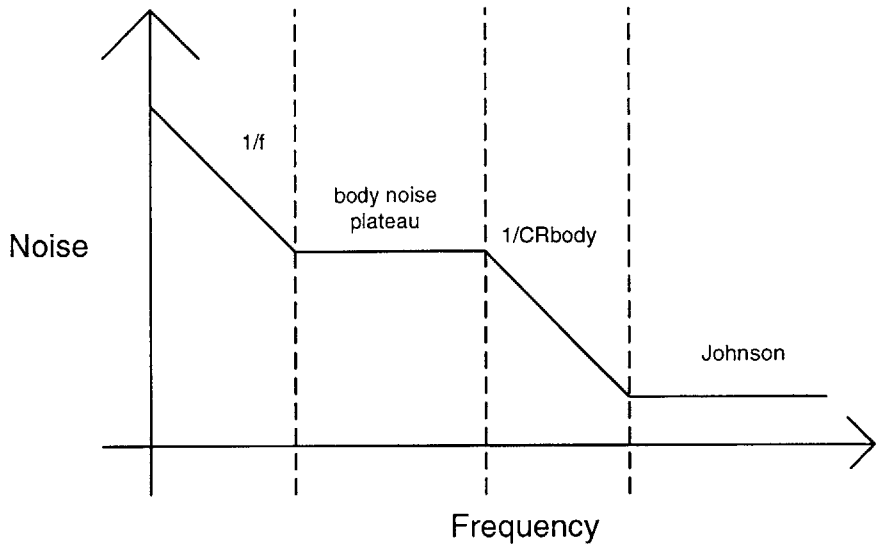

Figure 54: Body noise "hump" in RTI FET noise

This hump is a result of body noise generated by the on resistance of the FET. The corner results from low pass filtering of this noise by the parallel combination of the front and back oxide capacitances. A quick check, however, reveals that with an on FET resistance on the order of a kilo-ohm and a capacitance on the order of femto-farads, the corner frequency (given by the familiar 1/RC) will be much higher than the target system frequency of 3MHz. What this means is that the "Johnson noise" that is observed may actually be the sum of Johnson noise and this body noise. However, for the purposes of this application, the body noise can be treated as being accounted for in the noise factor, F. In this case, the noise model derived above will be consistent and correct.

IX. Thermal Properties

The thermal properties of SOI FETs are notoriously bad, given that the insulating back oxide also acts as a thermal insulator, making the problem of self-heating within the device much worse. It was necessary to perform experiments to determine if thermal issues were indeed going to be dominant in this application.

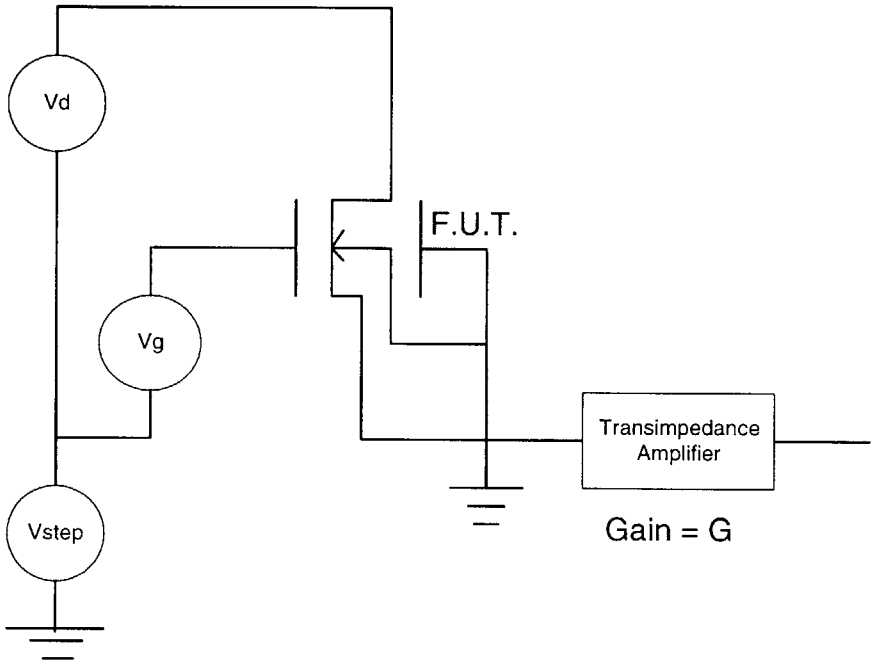

Figure 55: Thermal Measurement Test Setup

The setup used for this test is pictured in Figure 67. The test was conducted as follows: First, V_{DS} and V_{GS} were biased so as to cause the device to have a drain current of approximately 20 μA. A sinusoidal voltage was applied to the gate on top of the V_{GS} bias. At the output of the transimpedance amplifier, the DC portion of the signal yielded drain current while a measurement of the peak-to-peak amplitude of the AC portion of the signal which, when divided by the amplifier gain and the amplitude of the input signal, yielded transconductance. The target of this experiment was to determine if a step in power applied to the FET would cause noticeable device heating. Transconductance was chosen as the meter for temperature for two reasons. For one, the transconductance is relatively sensitive to temperature. The second reason is that the effect of temperature on transconductance is the most critical thermal effect to evaluate. In other words, if the

transconductance does not seem to be affected by stepping the power into the device, then thermal effects can be disregarded for the purposes of this application.

A power step was achieved by stepping the value of V_{DS}. The value of the step was calculated by multiplying the new value of V_{DS} by the new value of I_D (as extracted from the output of the transimpedance amplifier), and subtracting the initial device power. The value of the steps made in this experiment were on the order of 20-30 μW, which is somewhat greater than the typical power swing of a device in this application. The transconductance was measured as a function of time after the power step. It initially jumps to the new value dictated by the new drain current flowing through the device. If the FET were to then begin to heat, the transconductance would begin to decrease. However, no decrease was noted, and the final value of the transconductance strongly agreed with the theoretical value assuming room temperature.

This experiment was repeated several times with each of the different test FETs, both N and P-type, but no thermal transients were observed. For this reason, it was deemed unnecessary in this design to consider and model thermal behavior of the devices.

X. Small Signal Model

Now that the large signal model has been established, the small signal model is relatively simple to derive. The schematic appears below in Figure 56:

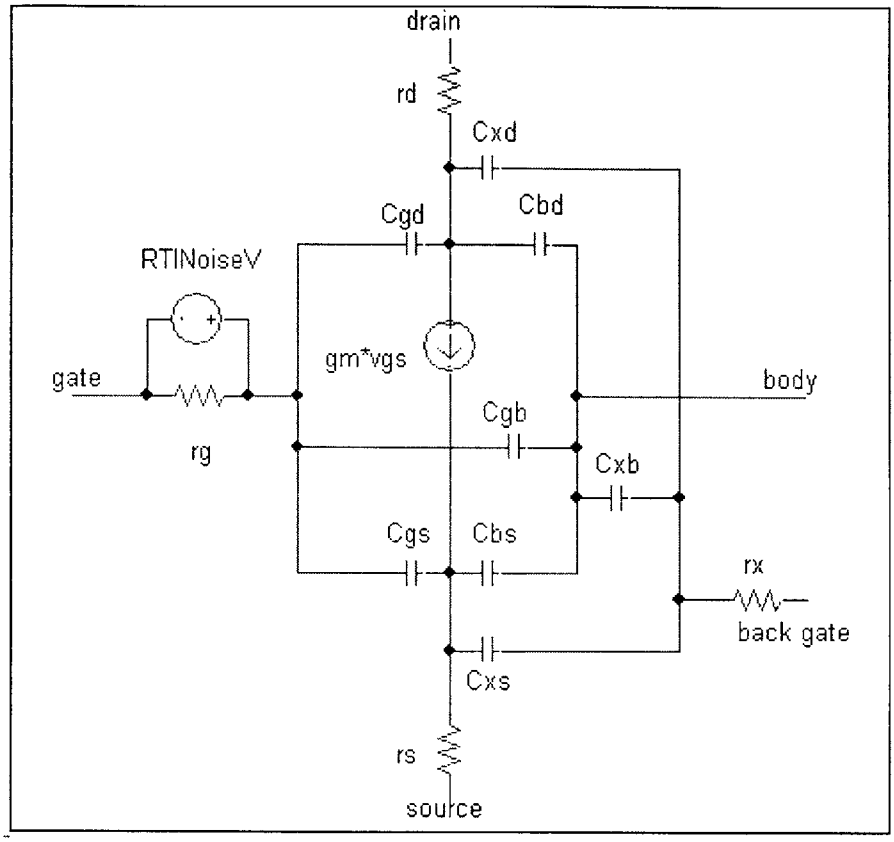

Figure 56: Small Signal Model Schematic

Determining values for the components in the schematic of Figure 56 is simple. The capacitors simply take on the values yielded by their constituent equations (given above) evaluated at the bias conditions. The only transconductance term that needs to be modeled is the forward transconductance, g_m, which is obtained by simply taking the derivative of Equation 42 with respect to V_{GS} at the bias point. This yields the following:

$$g_m = A + (1.1E-3)(V_{GS} - 1.2) - EF(1.2 - V_{GS})^{(F-1)}; \qquad V_{GS} \leq 1.2 \quad (49a)$$

$$g_m = A + (1.1E-3)(V_{GS} - 1.2); \qquad 1.2 \leq V_{GS} \quad (49b)$$

where A, E, and F are given by their equations above. The small signal resistances at the terminals of the device have the same value as their large signal counterparts. The only other component is the noise source at the gate. The characteristics of this noise source were established in Section VIII above. That completes the small signal model, which is

valid for the same range of bias conditions as the large signal model, namely $0.5<V_{DS}<2.5V$, and $1V<V_{GS}<\sim 2V$. As was mentioned before, no thermal effects need to be considered in this model.

XI. Final Model Summary

The model that is presented is applicable over two different areas. First, the large signal model holds for analysis of an N-type SOI FET when it is off. The schematic of this model is repeated here for ease:

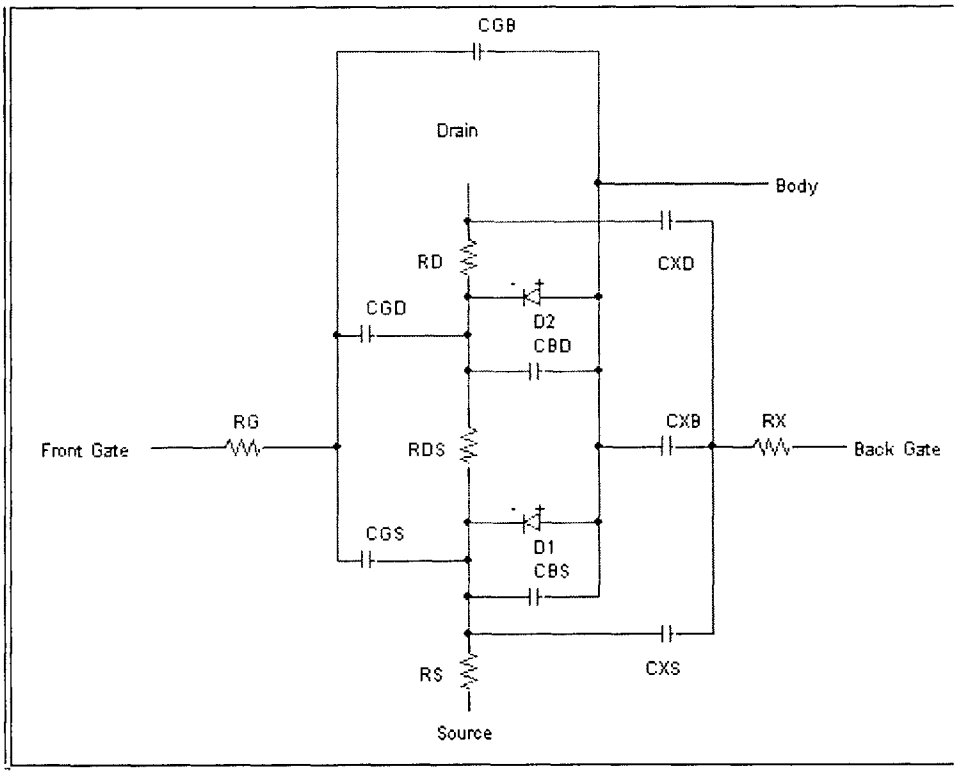

Figure 57: Large Signal Model for Off-State Analysis

The model is also viable in the on state for the specified ranges of $1V<V_{GS}<2V$ and $0.5V<V_{DS}<2.5V$, assuming the back gate, source, and substrate are all tied together. The schematic for this operating range is again repeated here:

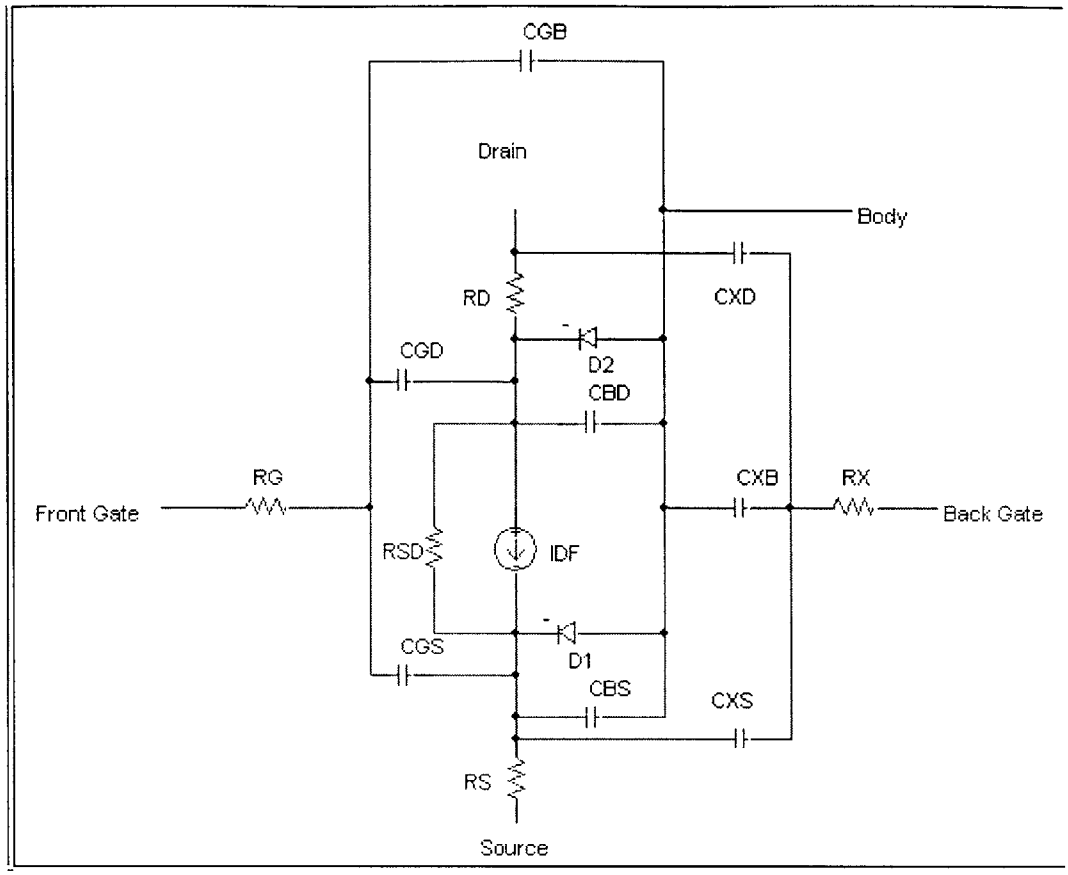

Figure 58: Large Signal Model for On-State Analysis

The equations that yield the values of the circuit components in these two regions are summarized below:

$$C_{BZ} = CBZ0 \bullet A_{BZ} \bullet \left[1 - \left(\frac{V_{BZ}}{\phi_0}\right)\right]^{-MJ} ; \qquad V_{GS} \leq (\phi_0/2) \qquad (3a)$$

$$C_{BZ} = \left[\frac{CBZ0 \bullet A_{BZ}}{0.5^{(1+MJ)}}\right] \bullet \left[1 - \left(\frac{1+MJ}{2}\right) + \left(\frac{MJ \bullet V_{BZ}}{\phi_0}\right)\right] ; \quad V_{GS} > (\phi_0/2) \qquad (3b)$$

$$C_{GB} = \left(C_{ox} L_{eff} W\right) \qquad V_{GS} \leq V_{FB1} \qquad (7a)$$

$$C_{GB} = \left(\frac{C_{ox} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{ox}^2 (V_{GS} - V_{FB1})}{\varepsilon_{Si} q N_{SUB1}} \right]}} \right) \qquad V_{FB1} < V_{GS} \qquad (7b)$$

$$C_{GB} = \left(\frac{C_{ox} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{ox}^2 (V_{T1} - V_{FB1})}{\varepsilon_{Si} q N_{SUB1}} \right]}} \right); \qquad V_{T1} \leq V_{GS} \qquad (7c)$$

$$C_{XB} = C_{box} L_{eff} W; \qquad V_{XS} \leq V_{FB2} \qquad (8a)$$

$$C_{XB} = \left(\frac{C_{box} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{box}^2 (V_{XS} - V_{FB2})}{\varepsilon_{Si} q N_{SUB2}} \right]}} \right); \qquad V_{FB2} \leq V_{XS} \leq V_{T2} \qquad (8b)$$

$$C_{XB} = \left(\frac{C_{box} L_{eff} W}{\sqrt{1 + \left[\frac{2C_{box}^2 (V_{T2} - V_{FB2})}{\varepsilon_{Si} q N_{SUB2}} \right]}} \right); \qquad V_{T2} \leq V_{XS} \qquad (8c)$$

$$C_{GD} = C_{ox} W \bullet LD; \qquad V_{GS} \leq V_{FB1} \qquad (9a)$$

$$C_{GD} = (C_{ox} W \bullet LD) + (0.5 C_{ox} L_{eff} W); \; V_{FB1} < V_{GS}; \; V_{DS} < V_{DSsat1} \qquad (9b)$$

$$C_{GS} = C_{ox} W \bullet LD; \qquad V_{GS} \leq V_{FB1} \qquad (10a)$$

$$C_{GS} = (C_{ox} W \bullet LD) + \left(\frac{2 C_{ox} W L_{eff}}{3} \right); \; V_{FB1} < V_{GS}; \; V_{DSsat1} \leq V_{DS} \qquad (10b)$$

$$C_{GS} = \left(C_{ox}W \bullet LD\right) + \left(0.5C_{ox}L_{eff}W\right);\ V_{FB1}<V_{GS};\ V_{DS}<V_{DSsat1} \quad (10c)$$

$$C_{XD} = C_{box}WL_{drain} \quad (11)$$

$$C_{XS} = C_{box}WL_{source} \quad (12)$$

$$I_D = \left(\frac{R}{25}\right)\left[A\left(V_{GS} - 0.895\right) + (5.5E-4)\left(V_{GS} - 1.2\right)^2 + E\left(1.2 - V_{GS}\right)^F - D\right];\ V_{GS}\leq 1.2 \quad (42a)$$

$$I_D = \left(\frac{R}{25}\right)\left[A\left(V_{GS} - 0.895\right) + (5.5E-4)\left(V_{GS} - 1.2\right)^2 - D\right];\quad 1.2\leq V_{GS} \quad (42b)$$

$$A = (2.39794E-5)V_{DS} + (3.73942E-4) \quad (43)$$

$$D = \left[(2.1E-6)\left(V_{DS} - 0.5\right)^{1.75}\right] + (5.19999E-5) \quad (44)$$

$$E = \left[(4.5E-5)\left(V_{DS} - 0.5\right)^{1.4}\right] + (3.83872E-5) \quad (45)$$

$$F = -\left[(1.045E-2)\left(2.5 - V_{DS}\right)^5\right] + 1.985 \quad (46)$$

The small signal model for the device has a schematic repeated here:

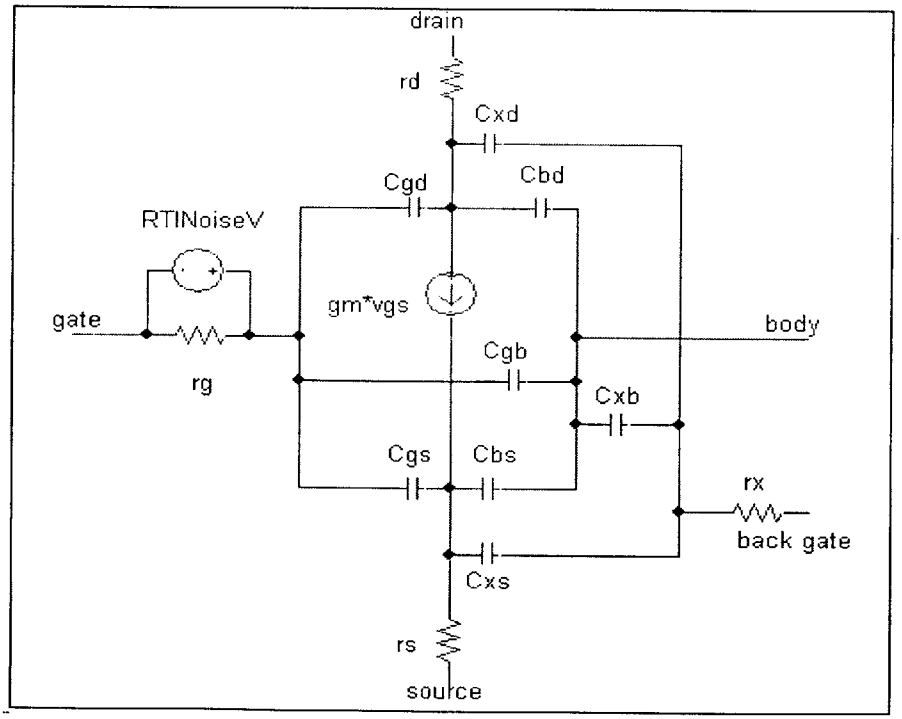

Figure 59: Small Signal Model Schematic

The values of the capacitors and resistors in this schematic are given by evaluating their large signal equations at the bias point of the device. The value of gm is given by the following equations:

$$g_m = A + (1.1E-3)(V_{GS} - 1.2) - EF(1.2 - V_{GS})^{(F-1)}; \qquad V_{GS} \leq 1.2 \quad (49a)$$

$$g_m = A + (1.1E-3)(V_{GS} - 1.2); \qquad 1.2 \leq V_{GS} \quad (49b)$$

and the noise characteristics are as given above. This completes the small and large signal model of the N-type SOI FET specified for the amplification application discussed above.

XII. Comparison of Performance

Although the actual implementation of this model in PSPICE or another suitable circuit simulation program was beyond the time scope of this project, some comments about the performance of the model can be made. The value of the capacitors in the model are well defined equations based upon process dependent physical parameters, and hence are considered accurate. The resistances in the model were either provided by Allied Signal or measured by trusted techniques, therefore they too can be considered accurate enough for this modeling application. The drain current equation is accurate to within a 6% window over the previously mentioned bias voltage ranges, and furthermore it is completely continuous, yielding no convergence problems should it be implemented in a circuit simulation program. By comparison, the PSPICE model provided by Allied Signal was accurate only to within a 10% window. Thus, the model generated in this paper is more accurate than that provided by the makers of the device themselves. For this reason, it can be considered to be a success.

XIII. Conclusion

This paper has presented and developed several techniques for devising empirical models of SOI devices. While it is true that the accuracy of the particular model here is within specifications for only a relatively small range of bias values, it is also true that the techniques above could be used to widen this range, should the need arise. The effect of a back gate could be added by simply extracting a back gate induced drain current equation

in a manner identical to that in which the front gate drain current equation was obtained. Furthermore, the error for bias conditions outside the range specified in this paper could be reduced by the addition of more error terms to the drain current equation, exactly as done here. The result is that, through the use of the techniques and equations discussed here, a model suitable for any application and any range of bias conditions could be derived.

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