An Evaluation of Three Dimensional Integration Technology

by

Andy Fan

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1999
[June 1999]

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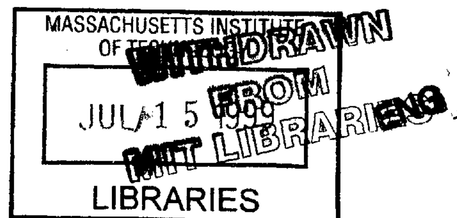

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Abstract

The first part of the research is an overview of existing three-dimensional (3-D) integration technologies such as wafer bonding, selective epitaxy, multi-chip modules, and micromaching (MEMS) methods. Each technological option was evaluated based on several variables, which include both processing constraints, applications, and viability. Indirect wafer bonding, specifically using copper metal as the bonding adhesive, was chosen because it offers advantageous schemes such as heat dissipation conduits, inter-wafer vias, and interconnect ground planes.

The technology development consists of copper wafer bonding at 400°C, satisfying the processing temperature requirements for aluminum back-end technology. Silicon wafers, coated with 300 nm of evaporated copper, were successfully bonded at 450°C for 30 min with a post-bonding anneal in N_2 for 30 min. Post-bonding anneal was required for successful bonding, but annealing temperature did not influence the bond strength from 400 °C to 620°C. The inclusion of tantalum diffusion barrier layer for Cu did not affect the bonding strength nor the boning temperature.

Thesis Supervisor: Rafael Reif
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Acknowledgments

I would like to acknowledge Arifur Rahman for inputs regarding materials in the analysis of 3-D wiring distributions. Also, inputs from students in Dmitri Antoniadis's group were extremely helpful in CAD layouts, design of experiments, and in actual processing. Talking with prof. Martin Schmidt and his students helped me understand the intricacies of wafer bonding. Furthermore, I would like to thank the MTL staff for providing training and processing tips, not to mention putting up with my reckless machine usage. Thanks also to Libby Shaw in the CMSE Analytical Lab, who spent countless hours in front of the AES machine trying to make sense of what's on my wafers. Finally, I would like to acknowledge everyone in the Reif group for their knowledge, care, and encouragements. And of course prof. Rafael Reif, who was always very patient with my graduate research progress from day 1. Without the people above, this thesis would definitely not be happening.

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Chapter 1

Introduction

Copper metallization, with low electrical resistivity and high electromigration resistance [1], is rapidly developing to be the mainstream interconnect technology. Along with advances in low k-dielectrics, these are two practical approaches in reducing interconnect RC delay in integrated circuits. However, new schemes, such as direct three-dimensional integration, have shown promises in significant reduction of interconnect delay and an increase system performance [2, 3]. In exploring the implementation of 3-D integrated circuits, wafer bonding is an attractive technology option. However, there are also other 3-D schemes such as epitaxial Si growth [4], multi-chip modules (MCM) [5], and MEMS techniques such as through-holes and micro-spring contacts [6]. Each technique has its own advantages and trade-offs. In this study, it was found that wafer bonding was the most robust way of implementing 3-D structures.

1.1 Interconnect Technology

Back-end processing is the art of electrically connecting pre-existing devices on a substrate. Electrical interconnections between devices can be made either with doped polysilicon, silicide, or metal lines, depending on the distance and spatial distributions among the devices. Often, a large portion of a silicon chip area are occupied by devices, thus leaving little room to include metal interconnections on the same level. In turn, metal lines are constructed layer by layer in the vertical direction. If the number of devices on a chip stays constant, then building the interconnects on a different level will add another degree of freedom in wire layout. Therefore, by appropriate design, the chip area can be made smaller by reducing the real estate required interconnects. This translate into a decrease in average interconnect length in a given chip. Often, these interconnect lines are parallel among themselves in-plane and orthogonal when out-of-plane, as in Figure 1-1. Chemical vapor deposited (CVD) W vias are made at the wire crossing points whenever a connection from one interconnect layer to another is desired.

To examine in detail how interconnects are fabricated, one can start out with device wafers which have

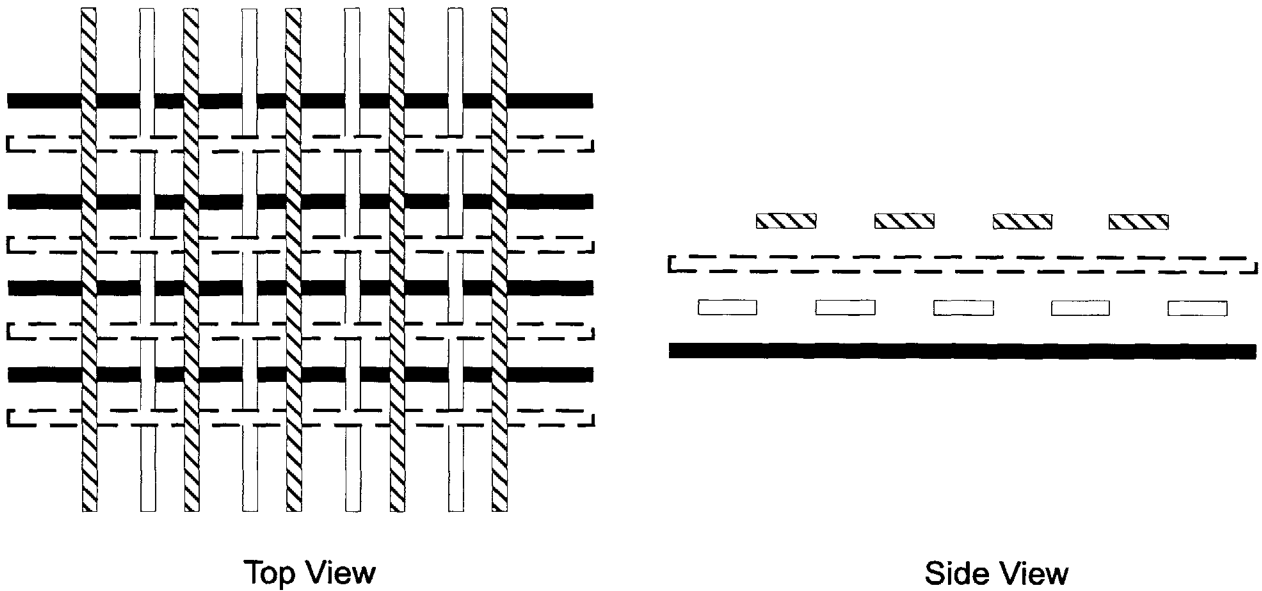


Figure 1-1: Multi-level interconnect layout.

completed all front-end processing. The most common way of connecting devices located with the vicinity of each other is to use doped polysilicon lines. First, silicon dioxide masks is grown where electrical isolation is needed. Then, a blanket doped polysilicon is deposited on top and subsequently patterned. This type of local interconnection is called multi-poly technology [7], and is used extensively for memory circuit. The polysilicon lines can be used as both interconnects and resistive loads.

Another technique to form local interconnects is to use silicided lines such as $TiSi_2$. Titanium is first sputtered onto the device, which is directly contacted with the doped Si source, drain, and polysilicon gate. The process is depicted in Figure 1-2.

The silicidation process is then activated at 600°C - 700°C in N_2 ambient. $TiSi_2$ will be formed only at the Si-Ti (or polysilicon-Ti) interface, whereas in the field-oxide or Si_3N_4 spacer regions, TiN is formed. After silicide/TiN formation is completed, TiN local interconnects can be patterned using a combination of dry and wet etches, at the same time the unreacted Ti can be removed. The main advantage for using silicided contacts is the low contact resistivity of $TiSi_2$ to other metals. This method is also relatively low-cost and saves a window mask step for patterning interconnects.

For longer interconnects, the metal of choice is aluminum because it exhibits excellent electrical conductivity and is one of the cornerstone materials for semiconductor metal technology. The current technology in creating Al interconnect structures is the damascene process, which is shown in Figure 1-3.

The first Al metal layer can be denoted by M1, followed by M2, etc. To begin with, inter-level dielectrics (ILD) such as plasma-enhanced CVD (PECVD) oxide is deposited uniformly on top. The ILD is then planarized using chemo-mechanical polishing (CMP). Then, vias are etched in the ILD, which is followed by filling of via using CVD W at around 450°C. Excess W is removed by means of metal CMP, and another ILD

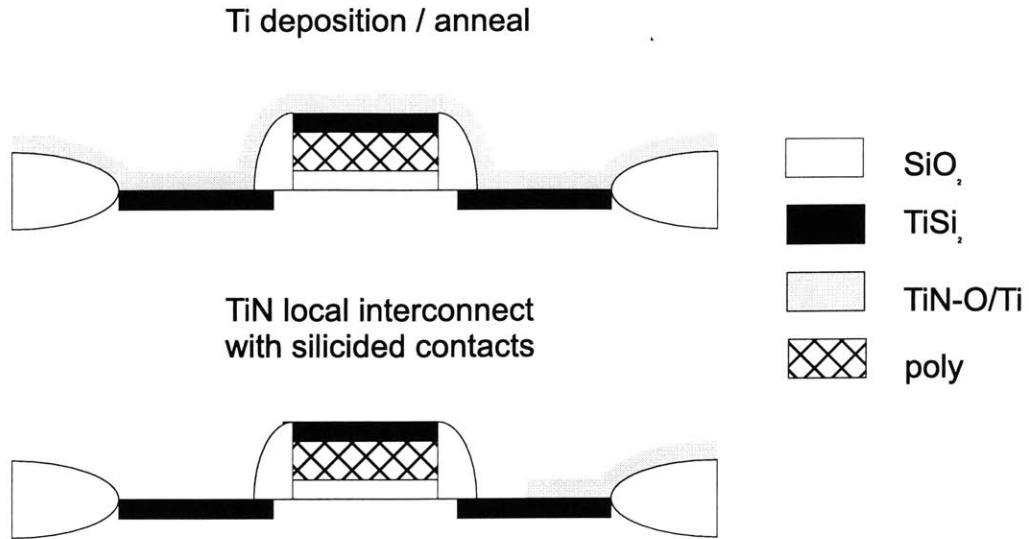


Figure 1-2: Silicided source-drain process with $TiSi_2$.

layer is deposited. Next, the second ILD is patterned and aluminum is blanket sputtered over the second ILD. Metal CMP on the Al layer completes the definition of the M1 interconnect lines. Finally, subsequent layers are processed by depositing another ILD deposition. Between the ILD and W, a barrier metal (TiN) and an adhesion layer (Ti) is usually needed. The barrier metal is needed because during W deposition the WF_6 will attack silicon surfaces, forming wormholes. The adhesion layer is also needed because TiN barrier layer has high contact resistance with Si surface. In all, Al back-end processing temperatures should not exceed 450°C to prevent Al bulk diffusion, electromigration, and stress migration failures.

Before making interconnections from one metal layer to another, it is desirable to globally planarize the surface after ILD deposition. Without planarization, subsequent metal features suffers from step coverage height mismatches. Referring to Figure 1-4, suppose there are regions of dense and sparse wires in M1.

Without planarization on ILD 2, regions in M2 that overlaps with dense M1 wires will be higher than regions overlapping with sparse M1 wires. This step height is detrimental to the lithographic depth of focus for higher metal layers. On the other hand, the use of CMP can backfire when one or more lower ILDs undergo a local planarization. In this scenario, the distance from the top ILD to a lower ILD will change, even though the top ILD surface is globally planarized. Filling vias of different height in one step becomes a challenge.

In general, the wire widths and pitch increases for higher metal layers (see Figure 1-5. This is because upper metal layers usually contain global (or long) interconnects or power lines, and these wires require high driving currents for signal integrity. A thin global line would degrade over time, suffering from electromigration, stress migration, and thermal stress. However, having thicker interconnects introduces new dilemma in processing, system layout, and circuit performance. As metal lines grow wider in successive layers, the contact plugs between layers also grows in proportion in order to support the required current

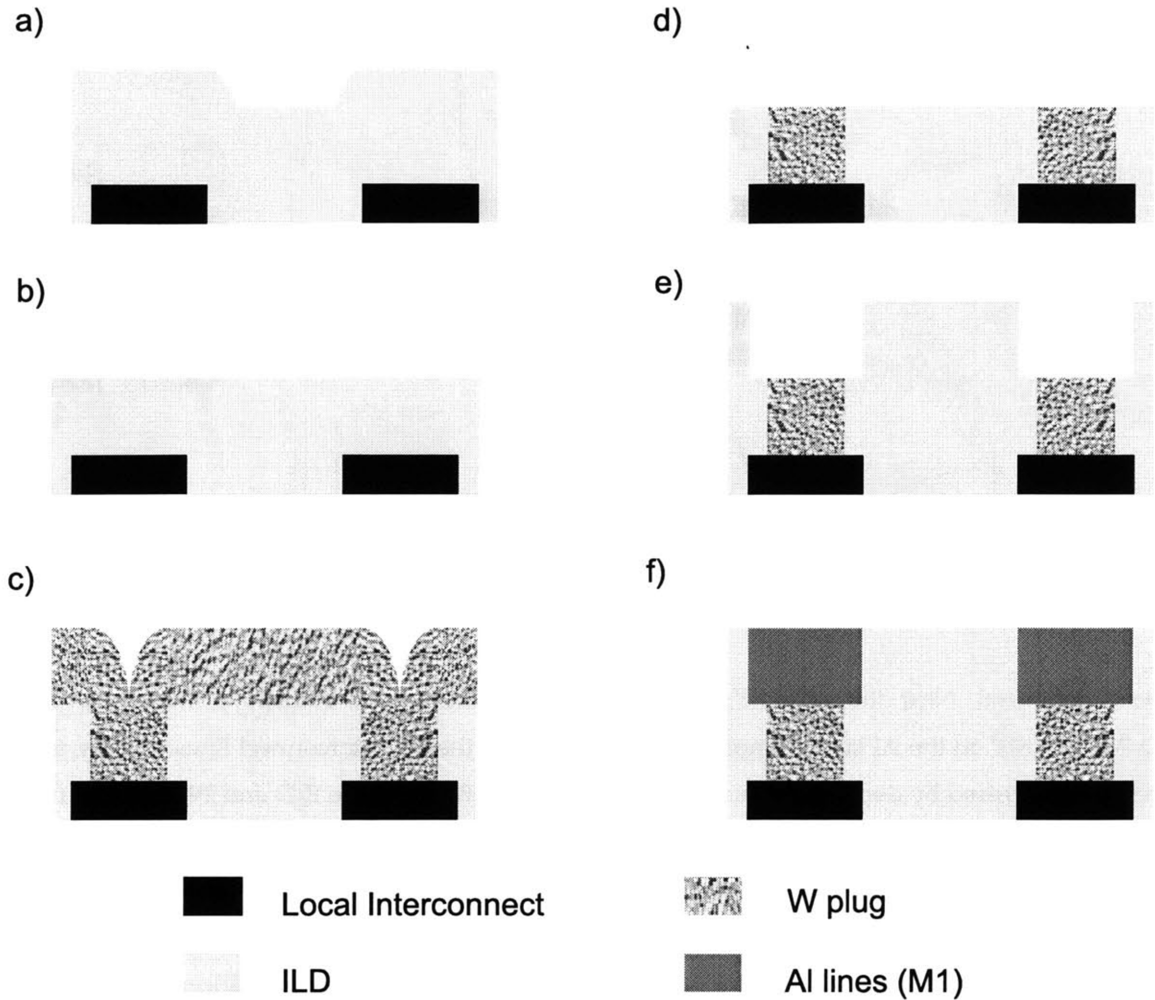


Figure 1-3: Damascene process: [a] ILD deposition; [b] ILD CMP; [c] ILD patterning, CVD W deposition [d] Metal CMP; [e] Second ILD deposition, patterning; [f] Al deposition, metal CMP.

density. Soon, real estate for both wires and vias will rapidly diminish, thus prompting more metal layers to be built . Commercial processors today contain up to five or six interconnect layers, and this trend will continue in the near future.

1.2 Interconnect Resistance and Capacitance

From a system performance viewpoint, increasing metal layers will increase RC delays along the critical path. To illustrate, in Figure 1-5, interconnect layers can be modeled as a lumped element circuit consisting of capacitors and resistors.

The resistors represents the electrical resistivity in the critical path. The horizontal capacitors represent the parallel-plate capacitance between two given in-plane wires. Similarly, the vertical capacitors represent the capacitance between either two inter-plane wires or between a wire and a substrate plane. In general, it

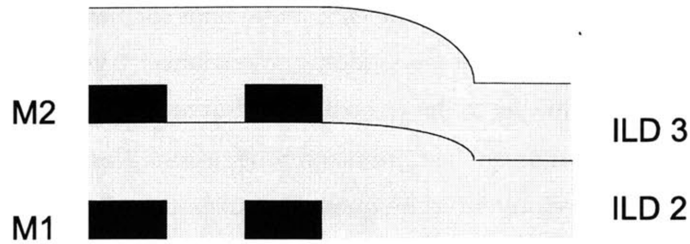


Figure 1-4: Height-difference effects without ILD planarization

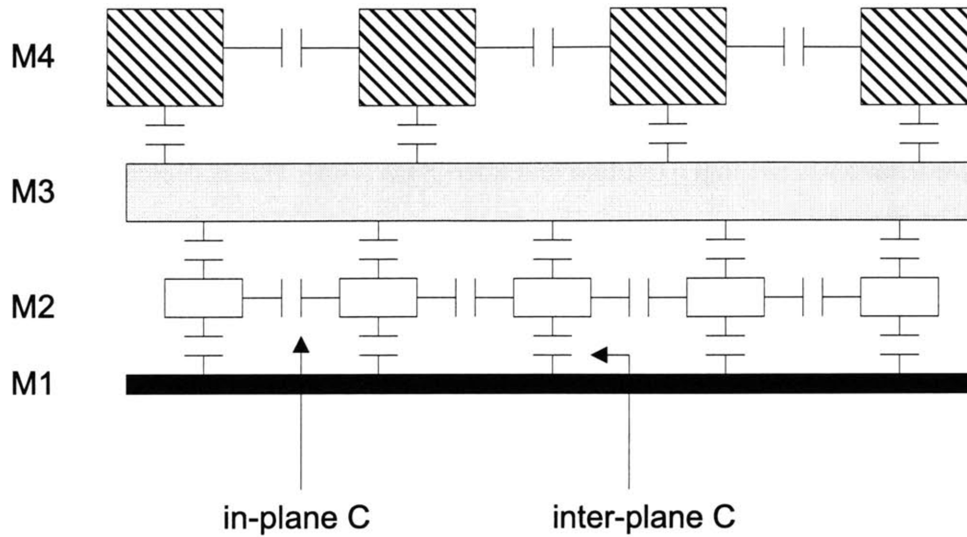


Figure 1-5: Interconnect capacitance model. Note: The effective resistors were not drawn but can be placed wherever metal lines exist.

is desirable to simultaneously reduce both R and C, but in reality it is a challenge. To begin, the resistivity of a metal wire can be expressed as:

$$R = \frac{\rho \cdot l}{A} \tag{1.1}$$

where

- R = wire resistance
- ρ = resistivity of the metal
- l = length of the wire
- A = cross-sectional area of the wire

From Equation 1.1, the resistance R is proportional to l, ρ, and inversely proportional to the cross-sectional area. Since local interconnects are relatively short, acceptable wire resistance in the critical path can be obtained with doped polysilicon lines, which has higher resistivity($\rho = 10^4\Omega$-cm) than metals. To

reduce the critical path resistance in global interconnects, metal lines such as Al ($2.7\mu\Omega$-cm) must be used. Given a constant number of logic gates on a chip, adding interconnect layers may actually decrease the average and total interconnect length due to the reduction of chip area. Therefore, in a multi-layer interconnect scheme, the critical wire length can be minimized to an extent (though still quite long compared to local interconnects) by using clever layout techniques. However, the wire resistance is still sensitive to the cross-sectional area and metal resistivity. Recent advances in metal etching and plating has allowed Cu metallization ($\rho = 1.7\mu\Omega$-cm) to replace Al in the immediate future. With the possible exception of using superconductor wires, new innovations in materials research is necessary for metallization technologies beyond Cu.

As mentioned above, the wire resistance is also influenced by the wire cross-sectional area. The area is dependent on the wiring pitch, which is the distance between centers of the two nearest in-plane wires. The pitch, in fact, is not arbitrary but directly relates to the interconnect capacitance. There are equivalent parallel-plate capacitances between the in-plane and inter-plane wires. This is depicted in Figure 1-5. The capacitance can be given by:

$$C = \frac{\epsilon_r \cdot A}{d} \tag{1.2}$$

where

- C = capacitance
- ϵ_r = dielectric constant of inter-level dielectric
- A = cross-sectional area of dielectric
- d = distance between two given wires

Therefore, if the in-plane interconnect pitch is small, there will be a dramatic increase in the wiring capacitance due to the decrease in d. Also, the wire capacitance will increase if the aspect ratio of in-plane wires is large. The aspect ratio is defined as the height to width ratio of a rectangular cross-section. An increase in aspect ratio will elongate the rectangular cross-section in the vertical direction, hence increasing the surface area shared between adjacent in-plane wires.

On the other hand, the wiring topology has less effect on the inter-plane capacitances. This is because the thickness of each interconnect layer can be kept relatively constant (invariant d in Equation 1.2), giving a flexible wire aspect ratio design range (keep A small whenever possible). The above statement is true provided a reliable ILD CMP process is available. Usually in multi-level interconnects, the first few metal layers (M1-M3) contain high- aspect ratio lines with small pitches; in this region the in-plane capacitances will have more effect on the critical path than the inter-plane variety. However, in higher metal layers (M4-M6), current density requirements force the wire cross-sections to be large and the aspect ratio to approach 1. To maximize the real estate of each layer, the wire pitch will be made to be small as possible, though the pitch will still be large. So in the global interconnect regime, both in-plane and inter-plane capacitances play a major role in the critical path.

From Equation 1.2, one can also decrease the equivalent capacitances by choosing a low-dielectric constant (low-k) material as the ILD. Silicon dioxide (SiO_2), the conventional ILD, has a dielectric constant of $\epsilon_r = 3.9$. Although it is the cornerstone dielectric material in semiconductor manufacturing, the high ϵ_r of SiO_2 is unsatisfactory for the next generation of high-speed VLSI circuits. Earlier developments has been exploring polymeric systems as a replacement for SiO_2 ILDs. Some popular compounds include parylene (N or F), bis-benzocyclobutene (BCB), poly(arylethers) (N or F), polyimide, silsesquioxanes (alkyl or hydrido) [8]. Most of these polymers have ϵ_r around 2.7 - 2.4 or so, and nearly all contain certain qualities that make them ideal for ILD implementation: Thermally stable up to 350°C or more, relatively good gap-filling and planarization properties, high acid-base-solvent resistance, and exhibits good adhesion to metals or other ILD materials. [9]. On the other hand, some properties that has plagued polymer ILDs are in moisture intake, low glass-transition temperatures, thermal expansion coefficients, material anisotropy, and deposition methods. Polyimide, for example, is a popular spin- on polymer dielectric in VLSI fabrication, but such films displays high anisotropy (in-plane or out-of-plane) in index of refraction, ϵ_r, and other mechanical properties. Also, in general spin-on polymer films will have problems in global planarity upon outgassing of solvents and conformal coverage in small topographies (0.25 μm or below). Recent developments have been towards CVD films such as Teflon AF, fluorinated parylene, and advanced materials such as xerogels and nanoporous silica. Of course, the ultimate ILD would be an air gap, for $\epsilon_r = 1$ is the lowest of all materials other than plasma.

In all, the two apparent approaches to alleviate interconnect RC delay is to:

1. Reduce the wire resistance using lower-resistivity materials
2. Reduce the interconnect capacitance using low dielectric constant (low-k) materials for the ILD.

Reducing interconnect resistance and capacitance not only benefits the circuit from speed but also from issues such as signal integrity, clock management, and power consumption. To begin with, the switching speed of an transistor defines the ceiling in circuit speed, and it depends on factors such as intrinsic capacitances. Referring to Figure 1-6, these are mostly parasitic characteristics of the device itself, and are related to junction / gate capacitances, MOSFET transconductance, contact resistances, etc. To be specific, for a MOSFET, the parasitic junction capacitance is dependent on the source-drain depletion width, which is dependent on doping and operating voltage. The non-parasitic gate capacitance C_g, which is one order of magnitude larger than C_j, is dependent on the gate oxide length and thickness. The intrinsic switching speed of a MOSFET can be approximated as (without parasitic elements) [7]:

$$\tau = \frac{C_g V}{I_{Dsat}} \tag{1.3}$$

where

- τ = approximate intrinsic switching speed
- C_g = gate capacitance
- V = power supply voltage

- I_{Dsat} = device saturation current

or τ is mainly dependent on C_g. Junction capacitances can be reduced by designing a desirable front-end process, but the gate capacitance cannot be easily reduced because the MOSFET drain current is proportional to C_g. In fact, gate dielectrics are purposely made very thin because one desires high gate capacitance, thereby creating high output current to drive the number of interconnects that exist on the critical path. Currently, research is being conducted to create new materials with high dielectric constants ($\epsilon_r > 10$) that would satisfy future generation CMOS devices that requires high drive currents, low power consumption, and high switching speed.

Conversely, the power consumption of a MOSFET without parasitics has the form:

$$P = CV^2 f \tag{1.4}$$

where

- P = power consumption
- C = total capacitance (largest contribution by C_g)
- V = power supply voltage
- f = frequency of operation

Therefore, there is an opposite effect between power consumption - switching speed and drive current when gate capacitance is increased. From Equation 1.4, one would try to minimize the power consumption by lowering the operating voltage. In the same equation, f of course should be set as high as possible for high-speed circuits. Also from Equation 1.3, lowering the voltage would also decrease the intrinsic switching time.

Aside from intrinsic capacitances, there are also intrinsic resistances in a MOSFET structure, such as sheet R_{sh}, accumulation R_{ac}, spreading R_{sp}, channel R_{ch}, and contact resistances R_c [7].

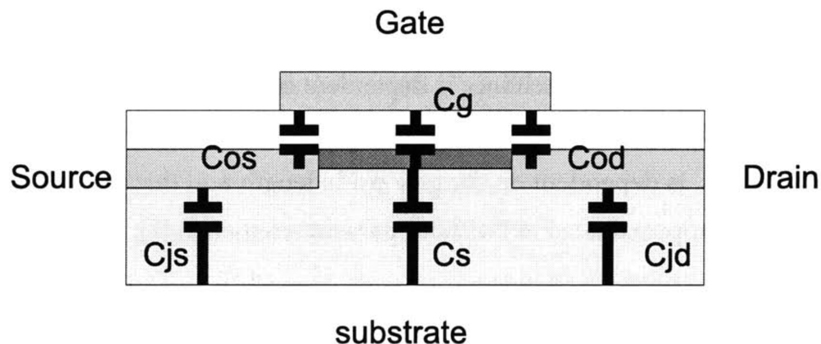


Figure 1-6: Intrinsic capacitances in a MOSFET.

From Figure 1-7, the channel resistance has the largest magnitude and is associated with the channel carrier mobility, thus also related to the device current density. Therefore, like C_g, R_{ch} is a design parameter

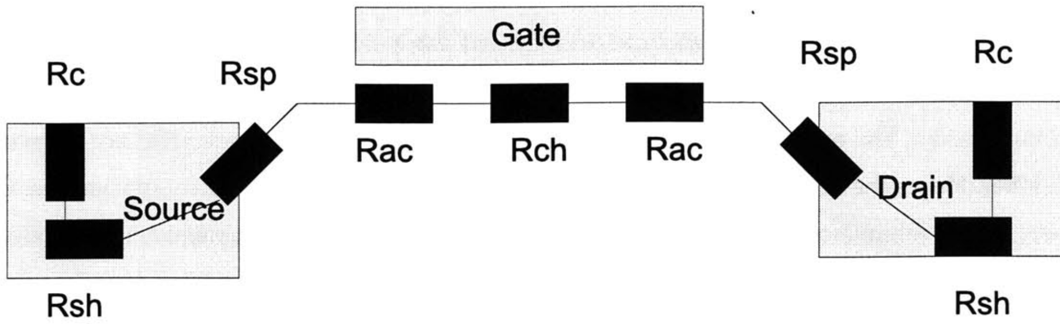


Figure 1-7: Parasitic resistance in a MOSFET.

in transistor performance, not an ideal source of reducing the transistor switching time. However, parasitic elements such as R_{ac}, R_{sh}, and R_c can be minimized with materials and process design. Out of these parameters, R_{sh} and R_c are affected by the device contact metallization, thus prompting the use of materials such as $TiSi_2$ for low resistance contacts. For a metal-semiconductor (Si) contact, the resistance at the contact can be defined as:

$$R_c = \frac{\rho_{sc}}{A} \tag{1.5}$$

Also, the resistivity of a metal film at the contact can be expressed in terms of the sheet resistivity:

$$\rho_{silicide} = R_{sh} \cdot t_{silicide} \tag{1.6}$$

where

- R_c = contact resistance (Ω)
- ρ_{sc} = metal-semiconductor specific contact resistance (Ω-cm^2)
- A = contact area (cm^2)
- $\rho_{silicide}$ = resistivity of silicide film (Ω-cm)
- R_{sh} = sheet resistance (Ω/square)
- $t_{silicide}$ = thickness of metal silicide at the contact (cm)

From Equations 1.5, and 1.9, R_c and $\rho_{silicide}$ can both be reduced in silicided contacts. Focusing on Equation 1.5, during metal-silicide formation, lateral silicide growth beyond the contact window will give an increase in the effective contact area A. At the same time, metal lines (ie. Al) deposited on silicided source-drain regions, has ρ_{sc} of around $1 \cdot 10^8 \Omega$-cm^2 [7], an order of magnitude lower than a metal-Si contact. Also from Equation 1.9, since resistivity $\rho_{silicide}$ is low for silicide films, a silicide gate (ie. ρ_{TiSi_2} = 15 $\mu\Omega$-cm, t_{TiSi_2} = 50 nm, ρ_{sh} = 3 Ω /square) can improve the gate sheet resistance by a factor of 4 or more over an un-silicided polysilicon gate (ρ_{sh}¿40 Ω/square) [7]. Current research has been aiming at developing CMOS compatible metal silicides that has both low $\rho_{silicide}$ and R_c. Such film candidates include $CoSi_2$ [10] and NiSi [10, 11, 12, 13].

In summary, several methods are available in lowering the intrinsic transistor switching time. It includes reduce the operating voltage, parasitic capacitances C_j, and intrinsic parasitic resistances such as R_{ac}, R_{sh}, and R_c. From the above discussion, minimizing the transistor switching speed sets an upper limit on the overall circuit speed. The overall circuit speed, though, is dependent on how devices are interconnected with each other. Hence the limiting factor on circuit speed is the load resistances and capacitances. Consider the case where several inverters are connected in series. There is an intrinsic capacitance associated within each inverter, denoted by C_{inv}. The wire connecting any two inverters also contains a capacitance denoted by C_w. For a given inverter-wire pair (see Figure 1-8), the total capacitance is:

$$C_{total} = C_{inv} + C_w \tag{1.7}$$

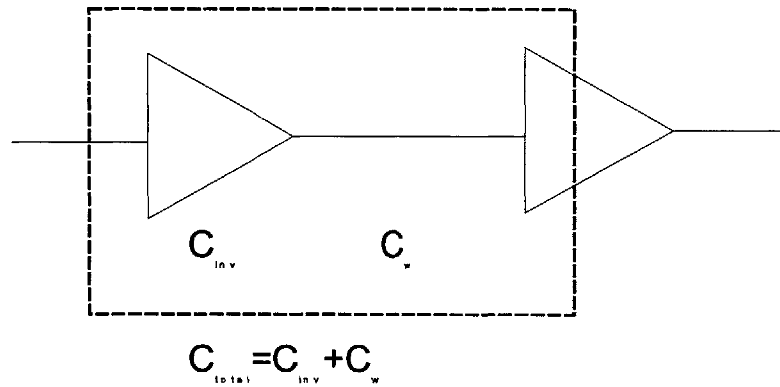


Figure 1-8: Total capacitance consisting of inverter and wire capacitances.

If the output current of the inverter to be i at voltage V, then the switching delay of the inverter-wire pair can be obtained from Equation 1.3:

$$t_{delay} = \frac{C_{total} \cdot V}{i} = \frac{C_{inv} \cdot V}{i} + \frac{C_w \cdot V}{i} \tag{1.8}$$

In Equation 1.8, the first term on the right hand side is the switching delay from the inverter itself, while the second term is the delay contribution from the wire. The wire capacitance C_w can be derived from Equation 1.2, and it depends on the ϵ_r of the ILD, wire length, and wire separation from the ground plane. Therefore, longer interconnects will increase the wire capacitance, which causes a longer delay in switching delay of an inverter-wire pair. Depending on the wire length, the delay contribution from the wire can far exceed the delay from the inverter itself - a situation of interconnect-dominated delay. Again focusing on Equation 1.8, one would attempt to reduce t_{delay} by increasing the current drive and lowering the operation voltage (which has a connection to Equation 1.4). However, increasing i will also increase the IR drop across the wire. Therefore, the voltage across downstream inverters would be dependent on length. Including the l

dependence in V in Equation 1.8, t_{delay} would be quadratic with respect to interconnect length l, a more dramatic effect than the previous linear relationship. Also, if the wire is very long (on the order of 1 mm), too much IR drop on the wires could force subsequent transistors to operate in the linear region, in which the CMOS pair cease to operate as an inverter.

To sum up the points, interconnect resistance and capacitances can affect circuit performance such as speed, signal/clock integrity, and power consumption. The transistor switching speed defines the top circuit speed, but to increase the overall circuit speed it is necessary to reduce the device RC load. Long interconnections between devices will increase the wiring capacitance, thus directly adding to the device-wire switching delay. Furthermore, long interconnects causes large IR drops between devices, which affects the voltage level for devices further down in the critical path. Using multi-level interconnection layers will give flexibility in routing, thus possibly reducing the required chip area needed for both devices and wire. This area reduction will also lead to a general decrease in average interconnect length. However, drawbacks in utilizing multi-level interconnects are the increase in wire-to-wire capacitances (both in-plane and inter-plane), the need for reliable interconnect fabrication technology (metal CMP, trench etching-filling), and the need for advances in materials science (silicide, Cu interconnects, low-k dielectrics, etc).

1.3 Exploring 3-D Technology

From the SIA roadmap, using copper and low-k dielectrics can only contribute a maximum performance gain of about 6x [14]. Instead of improving the materials and processing aspects of interconnect technology, one can change the system architecture to reduce the interconnect delay. The main objective is to keep the interconnects short, while not only improving device and wiring density on a chip, but also receive gain in performance metrics such as high speed, low power, and low cost. In a microprocessor, normally there exists a large number of short (not necessarily local) interconnects and a small number of global interconnects. The local to intermediate-length interconnects usually contain signal lines, while the global interconnects are usually clock and power routes, with some global signal lines present. If the interconnect distribution function (which is proportional to the number of interconnects of a given length in a circuit) is plotted vs the interconnect length, the log-log plot should have a negative slope, with the distribution tailing off at the longest interconnect length [15]. The area under the curve is equal to the total interconnect length in the circuit.

The interconnect distribution in Figure 1-9 was obtained by using Rent's rule, which is an empirical relation between the number of logic gates and the number of input-outputs in a given family of chips in two-dimensions [15, 16]. This relation is given by:

$$T = kN^p \tag{1.9}$$

where

- T = number of I/O terminals in the area considered

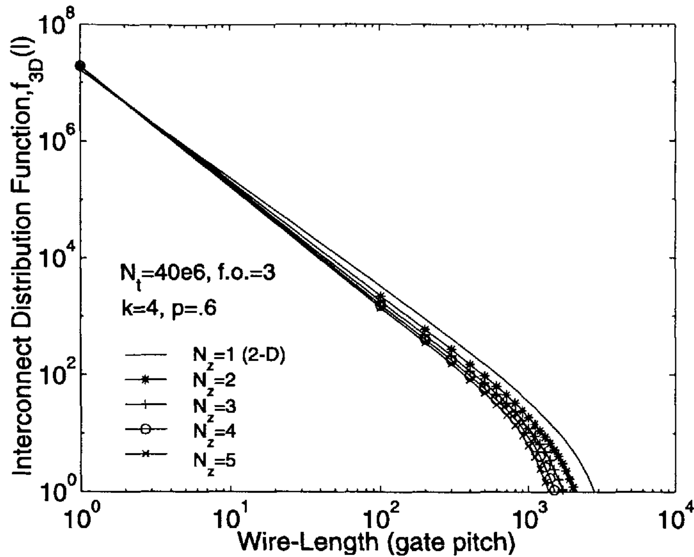


Figure 1-9: Simulated interconnect distribution function. Taken from [18].

- k, p = empirical constants for a given chip
- N = number of gates in the area considered

Ideally, one would like the interconnect distribution function to be as narrow as possible, ie. the x-intercept of the graph should occur at a lower wire length, or the number of long global wires should be as small as possible. To obtain a tight interconnect distribution, research has been focusing on taking the advantage of the third dimension in placing electronic devices. As stated before, the goal is to reduce the global interconnect length, which constitutes about 40-45$about$15[17]. In this particular reference, the interconnect distribution was computed using a 3-D extension of Rent's rule. Assuming the total interconnect length is kept constant as in a 2-D circuit and using pre-determined Rent's constants, placing devices in 3-D narrows the interconnect distribution function. Additional references showed that the average wire length decreases from 2-D to 3-D implementation [18].

There are many approaches to 3-D integration of active layers. To start with, commercial 2-D chips today usually consist of one layer of active / passive devices on Si substrate, followed by multi-layer interconnect structure in the vertical direction. In this discussion, such device-interconnect construction will be referred to as a strata. The simplest way of implementing a 3-D circuit is to use a stacked 2-D array. Stacked 2-D array is an analog to multi-chip modules (MCM), where packaged or bare dies are vertically stacked to form a 3-D array.

Vertical connectivity between adjacent devices is limited because non-adjacent chip connections, ie. connections between the bottom-most chip to the very top chip, is very difficult without peripheral metal interconnects around the stacked array package. This is especially true for packaged chips, where inter-chip vias is difficult to fabricate once ceramic packaging has been applied to each device layer. Intra-plane inter-

connections, however, can be dense because each layer is a working chip by itself. From the above reasons, inter-plane interactions is negligible compared to inter-plane ones, and this method cannot fully utilize the third dimension in device connectivity. Devices on adjacent chips can easily be interconnected by utilizing low-temperature solder joints such as Pb/Sn (roughly about 100 μm), though the interconnect density cannot be large.

Next, fully 3-D connectivity can be obtained if direct vertical integration (DVI) is implemented. In DVI, different device/multi-level interconnect wafers can be bonded together, forming a multi-strata structure. Deep, high-aspect ratio inter-strata vias can exist anywhere inside a given stratum, giving full utilization of the third dimension in device placement and routing. Therefore, DVI has the potential to achieve wafer-scale integration, whereas in stacked 2-D the 3-D structure are built from individual Si segments. Furthermore, one property that sets DVI apart from 2-D stacked array is the density of inter-strata vias. Using wafer bonding techniques, it is conceivable for DVI to improve the vertical via density by a factor of 400 using DVI over the stacked 2-D architecture. This is assuming that the via pitch equals the via width, and $w_{stacked2-D}$ = 100 μm and w_{DVI} = 5 μm, as in Figure 1-10. If current wafer-to-wafer alignment technology improves (align tolerance of about 1 μm), a 2μm via width would increase the via density by a factor of 2600. The 2 or 5 μm vias can be achieved using a combination of wafer-thinning and deep-via etching technologies. Since the via density is large, there is great flexibility in positioning the inter-strata vias while maintaining high device density within a given strata. One limitation to the via size is the accuracy of wafer-to-wafer alignment during bonding. The details of these processes will be discussed in Chapter 3.

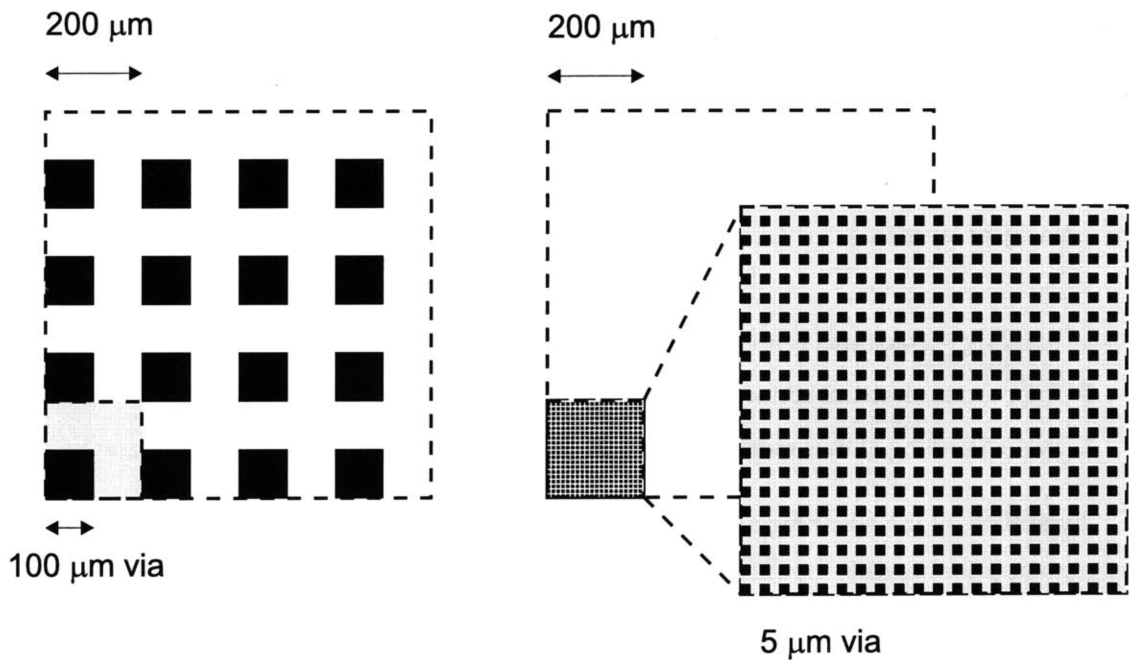


Figure 1-10: Increase of via density by factor of 400 from 100 μm via to 5 μm via.

There are many advantages to putting devices in the vertical dimension. To begin with, device density per volume can be increased. Another way of interpreting this is that in n number of bonded strata, the device density can be increased n-fold for a given planar real estate. In reality, the density improvement is less than n-fold because of physical placement of devices, via blockages, process variations, etc. Next, through clever circuit placements, one can significantly decrease the critical path from one device to another. An example of this is putting memory directly on top of logic circuits in order to decrease access time between the two units. In other words, the maximum benefit from DVI comes from using the third dimension as a circuit design parameter, not when one implements DVI with a previously designed circuit optimized for 2-D operation. Furthermore, DVI architectures can easily be turned into a system-on-a-chip technology when heterogeneous strata are bonded together. This means device layers with different technologies, for example Si and GaAs, can be integrated monolithically to produce an optoelectronic system on top of logic/memory circuits. Schemes such as vision-sensing arrays [19] and 3-D image sensors [20] have possibilities to be a driving force for future technological developments in DVI.

Aside from the benefits of 3-D integration, there are also caveats to this scheme. To begin with, a reliable stratum transfer technology has to be developed. Currently, the most robust method of bonding a stratum to another is to use wafer bonding or solder bump joints. Refer to Figures 1-11 and 1-12 for visual aid. In wafer bonding, a pre-fabricated stratum is transferred to another substrate by four basic steps: bonding of stratum to an auxiliary wafer, original substrate etchback, bonding of stratum-auxiliary pair to the desired substrate, and releasing the auxiliary wafer.

A similar bonding process exists for bonding with solder bumps, usually known as flip- chip bonding. The three basic steps are: solder ball formation on the chip and chip carrier, aligned chip-attachment to the carrier using resins (intra-chip connection), formation of large solder balls for inter-chip connections, and repeatable stacking of chip carriers.

Although the flip-chip bonding method appears to be more simple, wafer bonding is actually the more robust way of layer transfer. This is because:

1. Bonding surface area is less in the flip-chip method
2. Inter-strata electrical connections can be made dense in wafer bonding
3. Wafer bonding allows more reliable post-bonding processing of stacked structure

Even with all the advantages, these two layer transfer methods have common setbacks: layer-to-layer alignment prior bonding, bonding surface treatments, bonding material compatibility, processing temperatures, etc. Next, methods in etching and filling of high-aspect ratio vias (on the order of 20 μm deep, AR = 8:1), with CVD W plug and CVD TiN conformal adhesion layer, needs to be developed. Also, since there are multiple device layers, power dissipation per unit volume increases. Techniques in intra-strata and inter-strata heat removal has to be found. There are other concerns such as via blockage, electrical isolation

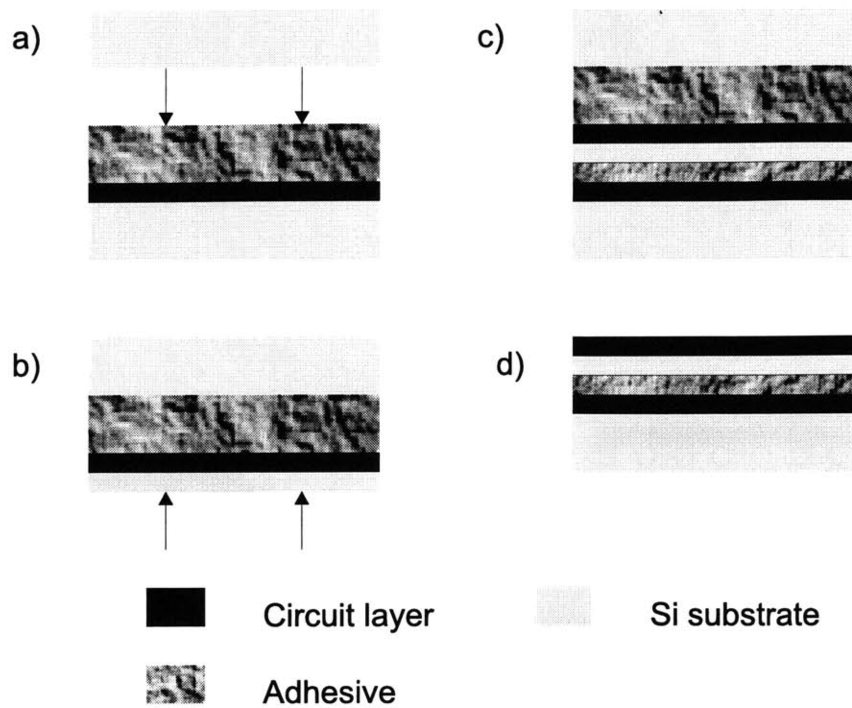


Figure 1-11: Layer transfer using wafer bonding. [a]Bonding of stratum to handle wafer; [b]Etchback; [c]Bonding of stratum to another device wafer; [d]Release of handle wafer.

between different strata, and most importantly the cost of operation. Therefore 3-D integration is not a trivial proposition, nor it is the only solution to keep interconnects short.

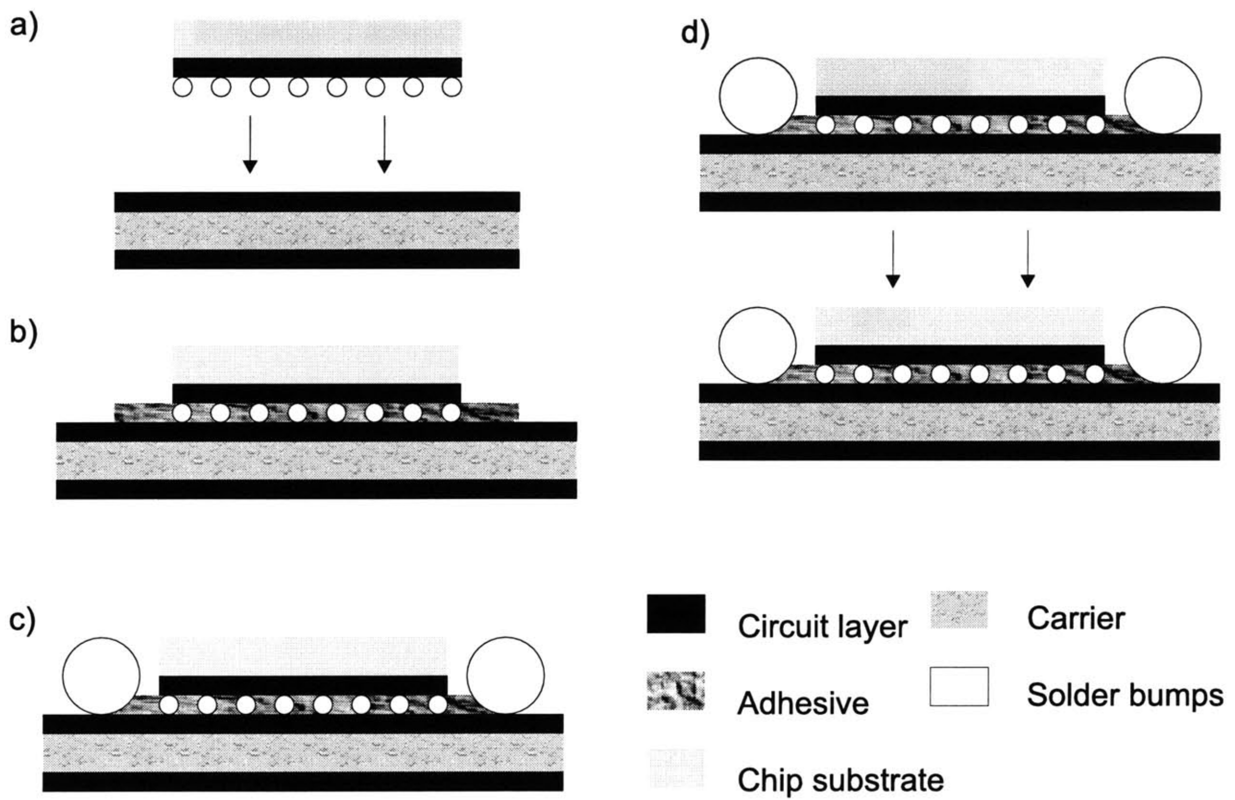


Figure 1-12: Layer transfer using flip-chip bonding. [a]Solder ball electrical interconnection between chip and carrier; [b]Chip-to-carrier bonding using polymers; [c]Solder ball formation for carrier-to-carrier interconnection; [d]Carrier-to-carrier bonding

Chapter 2

Overview of 3-D Integration Technology

As mentioned in previous chapters, there are many ways of implementing 3-D integration, whether it is DVI or a stacked 2-D array. The most prominent ways of vertically stacking active layers is to use wafer bonding, multi-chip module (MCM) approaches, and micro-machining (MEMS) approaches. Among the approaches, there are certain characteristics that can be compared:

- Bonding strength
- Thermal budget required for layer transfer
- Possibility for Al metallized strata prior to stacking
- Processing pressure
- Surface preparation prior to stacking
- Process repeatability
- Layer-to-layer alignment during bonding
- CMOS materials compatibility

Through the analysis in the next few sections, metal-to-metal wafer bonding was chosen to be the desired 3-D integration technology to pursue.

2.1 Wafer Bonding

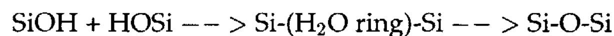
In this method, active device wafers are bonded together, and devices in different strata are electrical interconnected by high aspect ratio vias. Ideally, each strata is assumed to contain one active layer and a multi-layer Al interconnect structure. This requires a processing temperature ceiling of 450°C to avoid Al degradation [7]. When different metallization technology is used, ie. Cu, then this temperature constraint

can be relaxed somewhat. Further temperature requirements depends on the ILD stability, the thermal characteristics of the bonding adhesive (if it exists), and the thermal budget for strata of different technologies (ie. Heterogeneous strata of Si and GaAs circuits).

There exists three main types of wafer bonding: Indirect, direct Si-Si (or SiO_2- SiO_2), and anodic bonding. A direct Si-Si wafer bond refers to bonding of two Si wafers without any barriers in between. This usually requires an extensive pre-bonding surface preparation, not only to remove particles but also to chemically passivate the surface to induce bonding. Indirect wafer bonding refers to bonding of two wafers with an aid of a medium, such as polymers, glass, or metal. In this method, the bonding medium will greatly determine all the characteristics listed in the beginning of Chapter 2. Finally, an anodic bond is where a sodium (Na)-filled glass is inserted between a metal contact and a Si wafer, and bonding is performed by applying a voltage across [21]. The Na^+ ions in the glass will drift towards the cathode of the Si-glass-Si structure (or the anode terminal of the power supply), and the negative charges accumulate near the glass-Si interface. This forms a large potential difference across glass-Si interface, which forces a irreversible chemical bond between the glass and Si. Anodic bonding will not be discussed here because Na^+ contamination is detrimental to CMOS devices.

2.1.1 Silicon Direct Bonding

Silicon direct bonding refers to bonding of two Si wafers face to face without any intermediates in-between. The most common Si-Si wafer bonding consists of treating the wafers with RCA-SC1 clean (NH_4OH:H_2O_2:H_2O) followed by a HF dip. This creates hydrophilic (not hydrogen -H, but hydroxyl -OH terminated) Si surfaces on which the wafers can be bonded spontaneously upon contact at room temperature via weak hydrogen bonding [22]. In [22], a model suggests that the hydrogen bonding occurs when two hydrophilic SiOH surfaces forms a ring of water molecules at temperatures above 200°C. Further annealing of the bonded pair in excess of 700°C will cause the ring of water molecules to decay, forming a local Si-O-Si bond. Finally, anneals at 900-1100°C will form additional Si-O-Si bond around that local position, and the Si-O-Si structure propagates throughout the bonded interface. This process creates a non-separable bond between the two Si wafers.



$$\text{SiOH + HOSi} --> \text{Si-(H}_2\text{O ring)-Si} --> \text{Si-O-Si}$$

Hydrophilic surfaces is not limited only to SC1-cleaned Si wafers. In fact, normally SiO_2 surfaces are inherently hydrophilic. Essentially, the purpose of SC1-clean on clean Si (non-oxidized) wafers is to produce a thin native oxide layer that aids in bonding. Therefore, reports of SiO_2-SiO_2 wafer bonding is also available [22, 23], and the bonding process is similar: Initiate contact at room temperature, with post- anneals up to 1100°C.

On the other hand, Si wafers with hydrophobic (hydrogen terminated) surfaces can also be bonded at room temperature followed by annealing. This is done by treating Si wafers in RCA clean plus HF dip,

water rinse, and spin dry steps. HF dip, of course, will remove any native oxide on the Si surface, and H_2O cannot adhere to the wafer. However, a hydrophobic surface is prone to hydrocarbon contamination. Therefore, hydrophobic wafers do not spontaneously bond upon contact like in the hydrophilic case. Rather, bonding has to be initiated with a little compressive force. The end result is the same - the hydrophobic wafers are inseparable after high-temperature annealing. Models suggests that hydrophobic bonding mechanisms should be the same as in the hydrophilic case, but with different degrees of water adsorption at the bonding interface.

Silicon direct wafer bonding has been a foundation in the microelectromechanical systems (MEMS) industry. It creates a very reliable bond when performed carefully, and its high bonding strength allows various post-bonding processing to be performed. Despite its versatility, there are some disadvantages in the direct Si bonding method described above. To start, the wafer surfaces has to be very clean to obtain an acceptable bond. Particulates create voids (bubbles), which decreases the bonding area and perhaps discourages bond propagation upon annealing. In turn, direct Si wafer bonding is usually done in vacuum. Second, if bubbles do exist after the wafers are in contact, getting rid of it requires an anneal of around 1100°C for many hours (sometimes in excess of 20 hrs). Unless the circuit could withstand such thermal budget, the only other way to remove voids is to repeat the bonding procedure. Finally, since the direct Si wafer bonding is a high-temperature process, is not suitable for bonding Al-metallized strata, thus eliminating itself as a potential DVI technology.

Direct Si wafer bonding is not limited to only high temperatures; there exists several low-temperature Si direct bonding processes. To begin with, one source reports that bonding of Si-Si, Si-SiO_2, and SiO_2-SiO_2 wafers can be achieved first by creating hydrophilic surfaces (in Si-Si only) with RCA SC1 and SC2 [23]. The wafers are then contacted in room temperature with Teflon-tipped tongs and annealed in atmospheric furnace, ranging from room temperature to 150°C for 10 to 400 hrs. In this particular study, the optimal bonding temperature for Si-Si was 150°C, and for Si-SiO_2 and SiO_2-SiO_2 was determined to be 300°C. Although this is a low-temperature process, an anneal of 200 hrs (best result) bares a large quantity of thermal budget. Furthermore, from the study, a minimum of 100 hrs storage is necessary for the interface energy to reach stabilization (data points at room temp, 43°C, and 110°C).

In another literature, two hydrophilic Si wafers were bonded using a surface clean by Ar beam etching in vacuum [24]. Using Ar sputter clean in vacuum, the wafers can be cleaned and bonded before any residual gas atoms redeposits on the wafer surfaces. For Si-Si bonding, the bonding mechanism here is not with hydrophilicity (hydroxyl-terminated bonds) but with covalent bonds between two metal surfaces. The result Si-Si bond exhibited bond strengths comparable to conventional Si-Si bonding with 1100°C anneal upon tensile test. Oxide-to-oxide wafers can also be bonded using Ar-sputtering, but the bond strength was only half as strong as the Si-Si bond. The major advantage lies in that no post-bonding anneal was required, thus a true room temperature bonding process. However, this bonding method uses sophisticated vacuum chambers, where the surface sputtering and wafer contact were performed in-situ. Surface

activation methods can indeed be a viable DVI technology if proper equipment and setup is available.

2.1.2 Indirect Bonding - Polymer Adhesives

To recapitulate, indirect wafer bonding is the adhesion of two wafers through an intermediate layer of materials. One example of such material is the family of polymer adhesives. Referring to Figure 2-1, polymer adhesives, such as polyimide, photoresist, and epoxy, can be used to bond wafers at low curing temperatures ranging from 150°C to 400°C [25, 26, 27, 19].

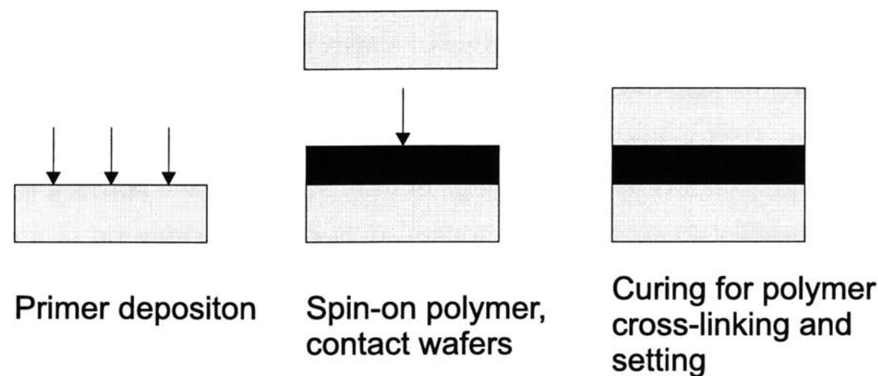


Figure 2-1: Polymer wafer bonding

Before depositing the polymer adhesive layer, primer deposition are necessary to ensure good polymer-substrate adhesion. In the case of photoresist, the conventional primer is to use hexamethyldisilazane (HMDS) - the same primer for photolithography. Silazanes create a hydrophobic (hydrogen-terminated) surface to which organic compound adheres to (see discussion in Section 2.1.1). For polyimide or epoxy, primer such as APS (γ-aminopropylsilane) is often used [25]. After primer deposition, the polymer is then spun-on and wafers are put into contact face-to-face. Bonding sequence is complete upon curing of the polymer, and the curing temperature depends on how much thermal stress a specific polymer can receive. For good bonding strength, the general thickness for polyimide films is around 2 to 5 μm upon a curing temperature of around 400°C for 30 to 90 min. [26, 27, 19]. In another study, Si wafers were bonded with 1.4 μm of negative photoresist, prebaked at 150°C (140 min) before contacting the wafers and cured at 150°C (90 min) afterwards [28].

In addition to good bonding strength, polymer wafer bonding is simple, fast, and is a lower temperature process (below 400°C), which satisfies the thermal constraint imposed by bonding Al-metallized wafers. Also, polymers (especially polyimide and photoresist) are widely-used CMOS compatible materials in industry. Most importantly, the bond quality of polymers is independent of surface topography. Polymer films can be reflowed at low temperatures, resulting a smooth surface profile even when overlaid onto rough surfaces.

On the other hand, several disadvantages exist in using polymers as the bonding adhesive. First of all, there is a volumetric change in the polymer upon curing due to solvent evaporation after curing. This can drastically change the planarity of the bonding interface and create unwanted voids, which decreases the bonding area and strength. Second, the polymer layer can only be patterned after curing. Therefore, inter-strata vias can only be etched and filled after bonding, which creates a hassle when the wafer gets too thick to fit into the load lock of an etcher. Also, etching high-aspect ratio via in a thick stack of bonded strata (Si substrate of top strata, polymer layer, and ILD of lower strata) can be a challenge. Finally, polymer layers exhibit low thermal and electrical conductivity. This can be a problem in a multi-strata structure, where channeling the heat dissipation from the devices is important. As described further in later sections, using metals as the bonding medium could alleviate this problem.

Nevertheless, polymer wafer bonding is definitely a major component in DVI technology. To map out the process sequence, the frontside of a given stratum is bonded to an auxiliary (handle) wafer. The substrate to this stratum is then mechanically thinned down and bonded to another stratum, again using polyimide. Upon curing, the handle wafer is released and inter-strata vias are then etched. Finally, via filling with oxide spacers (CVD TEOS), CVD TiN for liner/barrier, and CVD W plug formation completes the layer transfer process. After deposition of additional interconnect structures on the top stratum, another layer transfer sequence can be repeated [27, 19].

2.1.3 Indirect Bonding - Glass adhesives

Instead of polymers, one can also use BPSG (borophosphosilicate glass) as the bonding adhesive [29], with a film thickness of usually from 1.8 μm to 4.2 μm. However, when using glasses (450°C to 950°C) for wafer bonding, global planarity of the glass film is needed for good wafer-to-wafer contact. Most BPSG films need to be densified and reflowed at around 950°C to planarize and prevent the films from absorbing water [29]. Before densification, a nitride barrier layer should be deposited to prevent P, B dopants from diffusing into the Si wafers. Once planarized and densified, the bonding strength of BPSG is very high. In fact, if air pockets are trapped at the bonding interface, the bonded wafer would crack upon annealing from the expanding pockets. Furthermore, if the films were deposited on rough surface features, then it may be necessary to planarize the BPSG using CMP prior to bonding. In all, the high processing temperatures and the film planarity issues makes BPSG un-attractive for DVI.

2.1.4 Indirect Bonding - Eutectic Systems

Instead of polymeric or glass films, one can also take advantage of metal eutectic systems to create a bond between two substrates. By definition, the eutectic point is where a mixture of two metals becomes a liquid at a specific concentration proportion and a specific temperature [30]. For example, from a phase diagram, the gold (Au) and Si mixture contains an eutectic point at 363°C at 19 atomic [31]. The industry has been

using this property to bond Si dies to packaging substrates for at least 20 years. The Si die is usually attached to a ground plane on the ceramic substrate to prevent the Si substrate from having a floating voltage [32]. Therefore, in die backside metallization it is necessary to obtain a good ohmic contact and strong mechanical bonding between the Si chip and solder. A lack of ohmic contact would result in a potential drop across the chip-solder interface, creating joule heating and substrate voltage instability. [32]. A lack of mechanical stability in the chip-solder interface, would cause die cracking and chip separation from the ceramic package. [31].

The die attachment process starts by polishing the bottom of the Si chip in order to have good wettability of Au solder. The ceramic substrate is also polished and coated with Au solder. Wettability of a liquid on solid surfaces can be observed by the contact angle that the liquid makes with the substrate. This contact angle is proportional to the surface energies between phase boundaries [31]:

$$\gamma_{sv} - \gamma_{sl} = \gamma_{lv} \cdot cos\theta \tag{2.1}$$

where

- γ_{sv} = surface energy of solid-vapor interface
- γ_{sl} = surface energy of solid-liquid interface
- γ_{lv} = surface energy of liquid-vapor interface

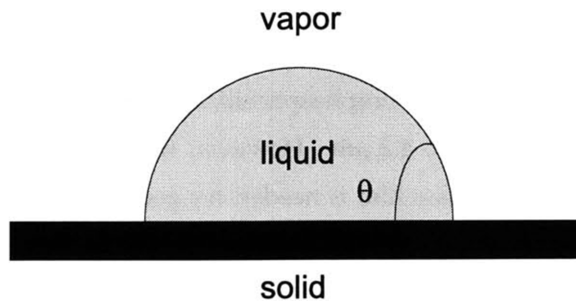


Figure 2-2: Wetting angle between liquid solder and solid substrate.

Therefore, when θ = 0, then the liquid is completely wettable and spreads on the substrate spontaneously. When $0^o < \theta < 90^o$, then the liquid is partially wetttable. When $90^o < \theta < 180^o$, then the liquid is not wettable on the substrate [31]. A clean substrate and a pure solder are both said to have high surface energies. Since a high surface energy substrate tends to attract random molecules, the natural tendency is for the substrate to lower its surface energy by growing an oxide. The protective oxide, having a lower surface energy, tends to lower the tendency for adsorption of molecules, thus causing poor wetting to pure solders. Therefore, the backside polish removes the native SiO_2 on the chip, which creates a high energy Si surface that allows good wetting for the Au solder. Solder wetting minimizes the formation of voids and oxides between the Au solder and the ceramic package. Referring to Figure 2-3, this oxidation happens because in the presence of moisture, Si atoms will diffuse through the Au film, producing oxide on Au (often

called "green gold"). This will decrease the wettability between the Au_{Sichip}-$Au_{preform}$ interface [33].

To continue, once the Au is in contact with the Si chip and on the ceramic substrate, both the metallized ceramic and metallized Si are bonded to a Au preform, a thick solder layer of approximately 50 μm.

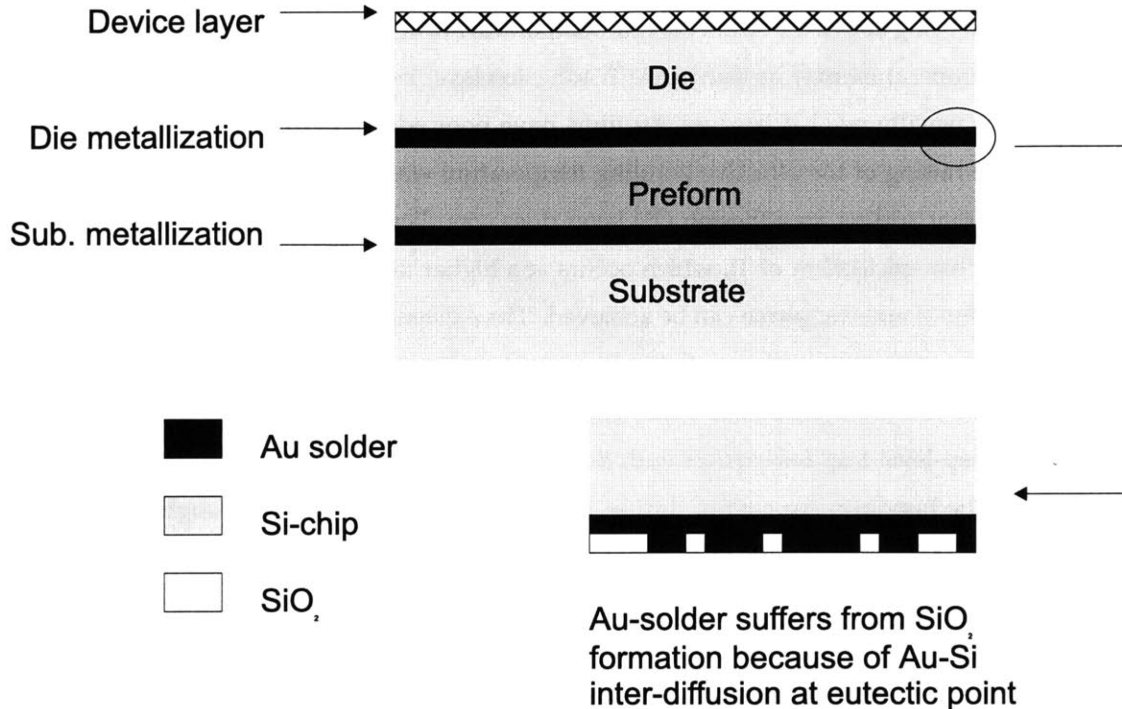


Figure 2-3: Chip bonding metallization.

The bonding mechanism consists of melting the Au-Si interface above the eutectic temperature. The Au preform consumes Si from the chip until the saturation composition is reached. The Au-Si melt will then condense into metastable Au silicides (such as AuSi, Au_3Si, Au_5Si [33] and regions of interlocking Au and Si islands upon cooling of the bonding interface, creating both a physical and chemical bond [31, 34].

When Au solder wetting becomes difficult on the Si surface despite surface grinding, a thin metal adhesion layer can be deposited to aid Au adherence. In addition, the adhesion layer can prevent SiO_2 formation on the Au solder surface, leading to a more reliable bond when Au solder is ready to be attached onto the Au preform. The adhesion layers are sometimes called barrier layers because they prevent atomic mixing of the backside Si and Au solder to a certain degree [32]. Some typical adhesion metals are Ti, Cr, and W. When atomic intermixing is needed for die attachment, care must be taken because Si has limited solubility in Cr, nitrogen- incorporated Ti, and W films at elevated temperatures [32, 35]. A limited amount of Si would then reach the adhesion layer - solder interface, thus discouraging Au-Si eutectic reactions from lack of Si source.

The main idea is to extend the die-bonding method to a wafer bonding scale. In theory, two Si wafers coated with Au films can be bonded by pressing the wafers together and heating the system to above the

eutectic temperature. Wafer bonding using Au films has been demonstrated to be feasible but at higher temperature than expected [35]. In the particular study, Si wafers with 20 nm Ti and 100 nm Au were bonded face-to-face in air (contacting wafer) and the pair was annealed at various temperatures in N_2. Reliable wafer bond was obtained at 600°C anneal for 30 min, while partial bonding was obtained at 500°C anneal for 30 min, both being above the Au-Si eutectic temperature of 363°C. According to the literature, this increase in bonding temperature may be due to the Ti adhesion layer between the Au film and Si substrate. The adhesion layer is usually needed because Au films have poor adhesion to SiO_2, again revisiting the wettability issue. The raising of the effective bonding temperature was not resolved in that study, but the experiments showed that adding an adhesion (Ti) layer does complicate the Au-Si bonding process. The author has proposed that silicidation of Ti, which occurs at a higher temperature than e-point of Au-Si, is necessary before the Au-Si eutectic phase can be achieved. The existence of $TiSi_2$ was not confirmed in the study.

Diffusion of Au into Si is always an issue when CMOS devices exist on the wafer. Gold is a fast diffuser in Si, and acts as a deep-level trap for carriers with donor and acceptor levels in Si about E_v+0.35 eV and E_v+0.63 eV [36]. In die bonding, Au cannot diffuse far enough through the chip (roughly 500 μm of Si backside) to contaminate the CMOS devices on the frontside. However, when bonding wafers with CMOS devices, Au contamination cannot be overlooked, and diffusion barrier layers become a necessity. Films such as sputtered TiW (3:97 by weight) [37] and CVD TiN [38] have demonstrated to be adequate diffusion barriers up to 700°C and 550°C for 30 to 40 min, respectively. There are also quality trade-offs between diffusion barriers such as film resistivity, effective thickness for barrier action, conformal step coverage, and film adherence [37]. With diffusion barriers in mind, Au-Si wafer bonding is also considered to be a viable 3-D integration technology because it is a low-temperature, reliable, and has certain characterics that DVI can take advantage of. For example, metal adhesion layers in a multi-strata structure can be used as heat conduits, electrical ground plane, electrical contact pad, etc. Further details of these schemes will be described in Section 3.1. Part of the work for the thesis will be to verify the effectiveness of the TiW barrier and evaluate the effectiveness of Au-Si bonding.

2.1.5 Indirect Bonding - Silicide Systems

An alternative metal system suitable for wafer bonding is metal silicides. Early work on silicide fusion bonding was done on platinum silicide (PtSi) [39]. PtSi is a stable, low resistivity silicide of approximately 30 μm-cm, and is formed by electron-beam evaporation of Pt film onto a Si wafer heated at 350°C in situ. Silicide formation was immediate upon Pt deposition, and 6 nm of PtSi was formed on the Si substrates. After removing the unreacted Pt in aqua regia (3:1 HCl:HNO_3), two wafers containing the silicide were put in face-to-face contact at room temperature. This room temperature adherence was a result of the hydrophilic (non-hydrogen terminated) surface between the two wafers upon acid etching and cleaning. The bonded pair underwent a 700°C anneal in N_2 for 2 hrs to fuse the two wafers together. The bonding strength of

PtSi was not reported, but studies showed that an ohmic contact exists between the p-type Si substrate and the PtSi bonding interface. PtSi bonding, in general, would not be an attractive Al- interconnect DVI technology simply because of the high annealing temperature. Similar systems, such as cobalt silicide ($CoSi_2$), has also been applied to wafer bonding [40]. Unfortunately, the annealing temperature was in the range of 700°C to 900°C, again too high for bonding Al-metallized wafers (below 450°C).

On the other hand, nickel silicide (NiSi) wafer bonding seems to be a promising DVI technology because of its low resistivity (14 to 50 μm-cm) and low formation temperature (350 to 550°C). [10]. From the literature, two Si wafers coated with 300 nm sputtered Ni were bonded by face-to-face contact at room temperature. The wafer pair was then heated at 440°C for 2 hrs in N_2 to induce NiSi formation at the bonding interface [40]. Using Auger electron spectroscopy, it was shown that all 600 nm Ni at the bonding interface converted to NiSi after annealing. The bonding strength of NiSi, however, only compared favorably to anodic Pyrex-glass bonding, far from the bonding strength of direct Si-Si. In addition, unless the Si substrate is heavily doped, NiSi creates a Schottky junction with respect to both electron and hole carriers. Ohmic contacts can be obtained when the doping levels exceed 10^{19} cm^{-3} for both n and p dopants.

Regarding film morphology, NiSi contain several unstable phases at temperatures ranging from 250°C to 900°C. To begin with, Ni deposited on single-crystal Si will react to form Ni_2Si around 250°C [10]. At temperatures above 350°C, the more prominent phase is NiSi because of increasing Si composition in reaction, but NiSi film is unstable until the temperature reaches around 500°C. At this stage the film sheet resistance is at its lowest [11].

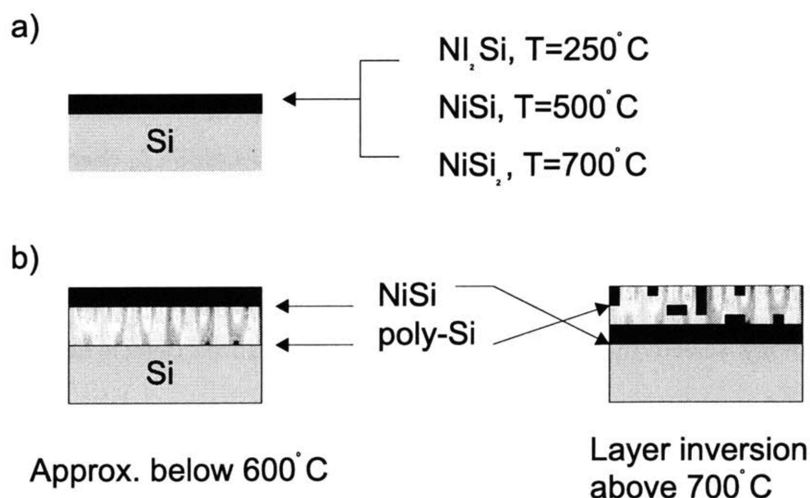


Figure 2-4: Nisi phase transformation and inversion.

Further increase in temperature (> 700°C) will transform NiSi into $NiSi_2$, the most stable phase of nickel silicide and also the most resistive. Also, NiSi agglomeration on Si starts to appear near the grains of NiSi. Changes in sheet resistance and film morphology is even more aggressive in the case of Ni films

on polysilicon or amorphous Si. In amorphous Si, the sheet resistivity maintains the same trend as in the single-crystal Si but three times as large. In the polysilicon system, NiSi films on Si suffers from silicide inversion at temperatures above 650°C cite article:Colgan. That is, NiSi will diffuse through the polysilicon grains at high temperatures, effectively putting NiSi below the polysilicon layer. At the same time, NiSi will undergo phase transition into $NiSi_2$.

Despite processing issues such as phase transformations, silicide inversions, and only an acceptable bonding strength, since NiSi wafer bonding is a low-temperature process and the bonding interface has low resistivity, it appears to be a promising technique for implemention of DVI. Part of the work for this thesis will be to reproduce NiSi bonding at 450°C and test the integrity of the bond.

2.2 Silicon Epitaxy

2.2.1 Selective Epitaxial Growth

Another way of implementation of 3-D integrated circuits is to use Si selective epitaxial growth (SEG) to construct multiple active layers. In SEG, thin Si films can be grown at pre-defined regions on the wafer without spurious Si deposition elsewhere. The process starts by the deposition of SiO_2 on a Si substrate and opening seed windows in the oxide film [41, 42, 43]. Then, gas mixtures such as SiH_2Cl_2 and HCl mixes to grow silicon islands at the exposed Si sites. Increasing the chlorine content (HCl) further inhibits Si growth on SiO_2, thus turning the oxide into a good growth mask. In early results, the Si growth temperature was in excess of 1000°C using $SiCl_4$ at atmospheric pressure. The growth was of low quality because oxide masks tend to degrade at such high temperatures. The remedy to this problem was to use silicon nitride (Si_3N_4) hard masks, which can withstand higher processing temperatures than oxide. However, Si growth selectivity decreased because Si_3N_4 provides good nucleation sites for $SiCl_4$ chemistry [43].

In later studies, it was shown that Si can be selectively grown at 600°C or below, either with SiH_2Cl_2 or silane chemistry using low pressure systems. The lack of chlorine in the gas mixture was compromised by adding excess HCl or Cl_2. The emergence of low temperature-pressure silicon epitaxy has improved the Si film morphology, selectivity, thickness uniformity, and reduced defects near the seed-seed window interface [41].

Referring to Figure 2-5, there are basically two types of SEG. Type I SEG is the standard epitaxy process described above, where epi-Si is grown on exposed Si seed windows within an oxide hard mask. In Type II SEG, the growth chemistry (SiH_4) allows single-crystalline Si to be grown inside the seed windows, while polysilicon is deposited on top of the dielectric mask [43]. The lack of chlorine removes the Si growth selectivity, thereby allowing Si nucleation on the oxide film. Type II growth is often called epitaxial lateral overgrowth (ELO).

The advent of selective epitaxial growth has expanded the variety of novel Si structure design, some of which could not have ever been fabricated before. Type I SEG has already developed into a major tech-

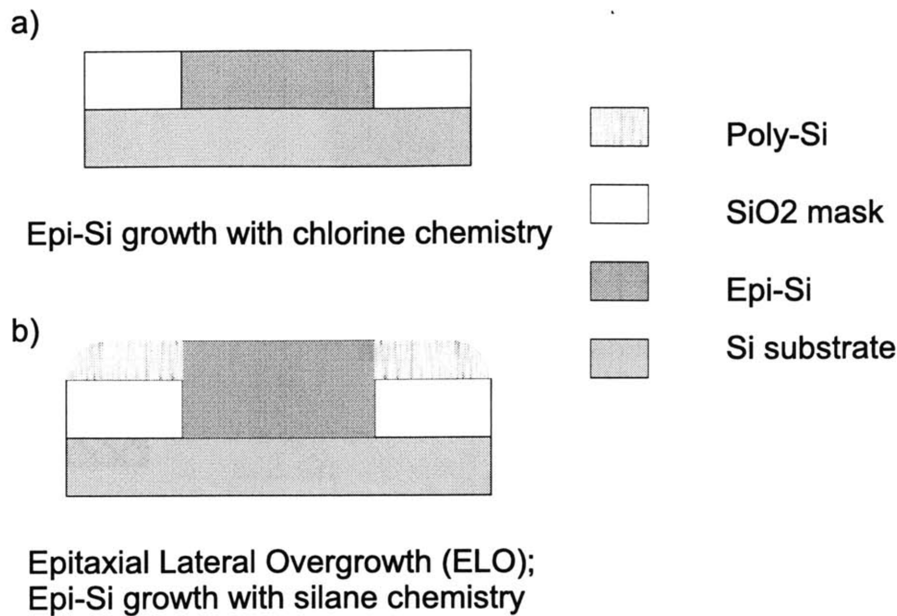


Figure 2-5: Epitaxial silicon growth. [a] Type I; [b] Type II.

nology in the fabrication of 3-D stacked MOS transistors [4], silicon-on-insulator (SOI) dual-gate MOSFETs [44], and 3-D SOI memory cells [41]. In these structures, the main thrust was create SOI active layers with narrow isolation between adjacent devices. The reasons why SOI technology is a main technological thrust entails the following: First, reliable isolation between individual devices can reduce inter-device parasitic capacitances, which would improve the overall circuit speed and removes common latch- up problems [45]. Along the same idea, narrow device isolation would increase device density, thus possibly reducing the chip area. Also, SOI devices are also projected to be low-power, to operate at higher temperatures, and to reduce short-channel effects that plague devices with small critical dimensions. Furthermore, SOI increases freedom of device design because structures can now be built on both sides of a CMOS (topside and bottom-side of the Si island). One example of this is the development in double-gate devices, which can add a degree of freedom in threshold voltage (V_t) control. It also offers top-bottom electrical connections, which is similar to 3-D integration.

With regards to DVI, there are several concerns in using SEG as a technology for 3-D integration. To begin with, the processing temperature is usually greater than 600*o*C, which prohibits Al metallization in a mult-strata structure. Interestingly, DVI can be implemented using SEG if polysilicon metallization (local interconnections) is used within each stratum. For example, in a stacked transistor scheme, an NMOS can be grown on top of an existing PMOS, thus giving a 3-D CMOS structure. Since individual transistors are practically right next to each other, a polysilicon network can interconnect the devices by taking advantage of double-gate designs.

The stacked transistor scheme would greatly increase the device density pending clever circuit design,

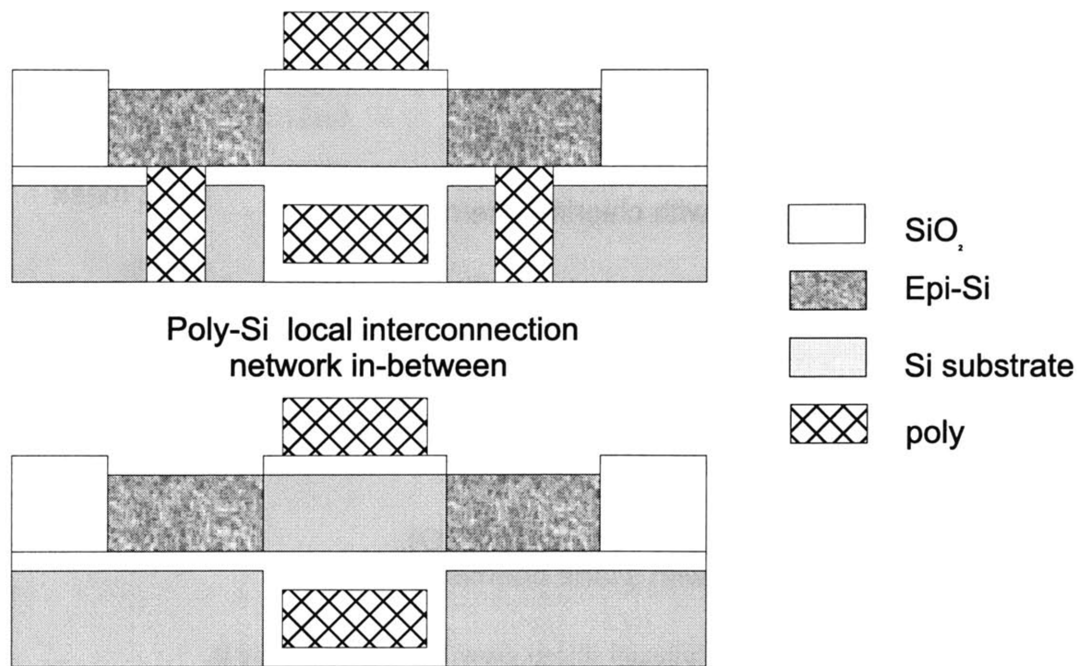


Figure 2-6: Possible double-gate stacked devices using epitaxial silicon growth.

device placement, and the overall system function. The drawback to the scheme is that devices would have to be placed in clusters, or close in close proximity, to reduce the effects of high-resistance polysilicon interconnects. Aluminum metallization is only possible after all strata have been constructed using SEG.

2.2.2 SIMOX Technology

Instead of epitaxially growing Si, another technique in creating thin Si layers for SOI and 3-D structures applications is using SIMOX (separation by implantation of oxygen) wafers [46]. To create a SIMOX wafer, regular Si wafers are implanted with a thin layer of O_2 at high energy and concentration. Then, the SIMOX wafers are thermal oxidized at 1100°C for 16 hours, and in the process a buried oxide layer (BOX) of approximately 100 to 300 nm is formed, depending on the O_2 implant conditions.

At this moment, the top Si-BOX interface is very rough and the BOX is not of device-quality. Next, a layer of low-temperature oxide is deposited on top of the epi-Si, and the SIMOX wafer is bonded to an oxidized device (auxiliary) wafer at temperatures around 700 to 1000°C. The SIMOX Si-substrate is then chemically etched back, stopping on the thin BOX layer. Upon removal of BOX and CMP of the epi-Si, SOI devices are then ready to be built. The resultant epi-Si thickness is usually around 200 nm.

In spite of the complicated bond-etchback process, SIMOX wafers can be an important starting material in DVI technology. SIMOX wafers have the ability to create very thin Si layers with relatively simple and controllable chemical etchbacks, an element that is important when one desires a thin multi-strata structure.

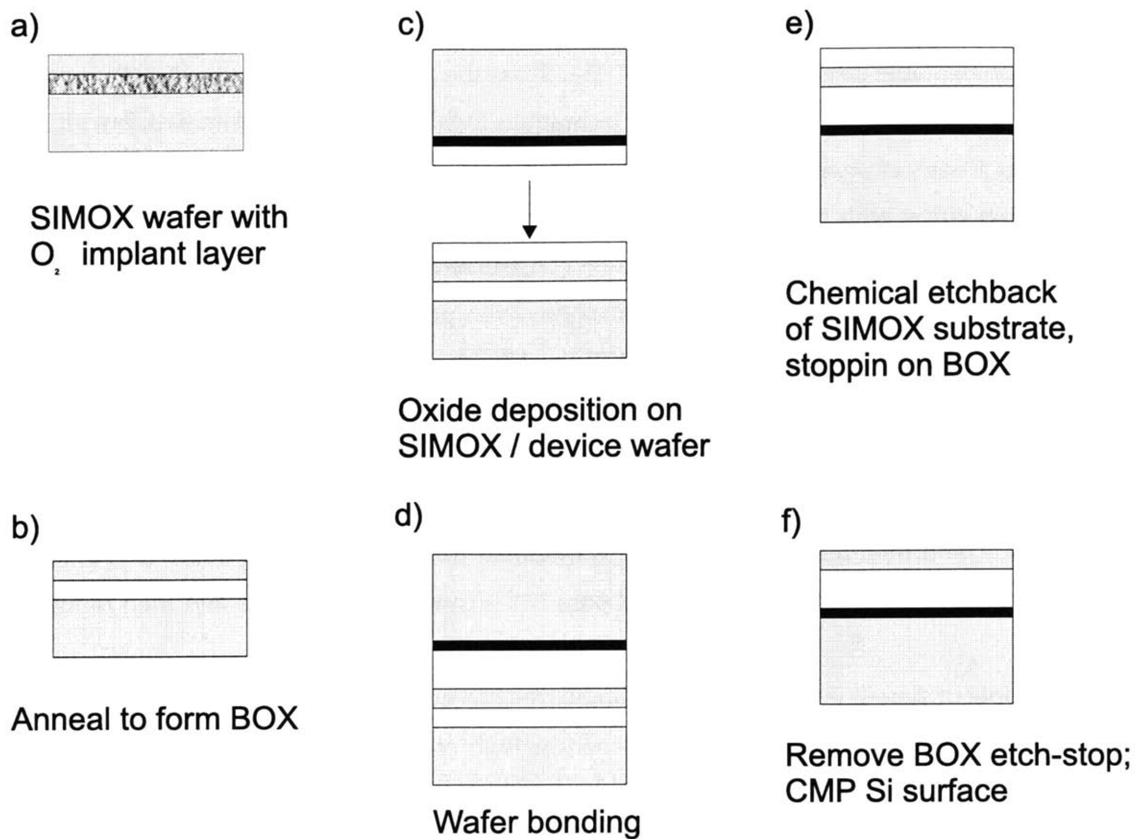


Figure 2-7: Wafer bonding with SIMOX.

The thinned epi-Si layer can also reduce the aspect ratio in inter-strata vias, alleviating the deep trench etching-filling dilemma. To continue, the high temperature oxide-oxide wafer bonding step can be replaced with any bonding methods described in Section 2.1. Given all the options that SIMOX wafers can offer, a rough DVI process can be prescribed as:

1. Completion of front-end and back-end processing of device wafers on SIMOX substrate
2. Bond device wafer to handle wafer; perform etch-back of Si substrate on device wafer
3. Etch stop removal; formation of inter-strata via
4. Aligned wafer bonding of device wafer to another completely-processed device wafer
5. Handle wafer release; bonding cycle repeated

2.3 Multi-Chip Modules

Instead of direct 3-D integration in a monolithic (wafer-scale) fashion, one can construct 3-D structures using hybrid wafer scale integration. The definition of hybrid wafer scale integration can be taken from [5],

which states that H-WSI is an electronic system built from a collection of discrete, unpackaged ICs. These discrete circuits are electrically connected using thin-film interconnect structures with "at least ten times the complexity of available device technologies." [5]. From the above definition, multi-chip modules (MCM) fits the description perfectly. There are many techniques in fabricating a MCM system, but all of them have the following things in common: The system is built from discrete components, and the components are interconnected either with thin-film interconnects, solder joints, or metal tapes (tape automated bonding or TAB). In general, MCM does not have to be constructed from unpackaged entities; in fact, there are many MCM schemes in which packages memory or even processors are wired together [47]. Depending on the application, MCMs integrated on a PCB-level (with packaged chips), a co-fired ceramic substrate level (packaged or bare chips), or on a Si substrate with thin-film interconnections (bare chips). From classifications of packaging-level integration, the packaging of MCM onto printed wiring boards follows two types. In type-2 integration, bare chips are first packaged as a single chip, then mounted onto a second-level substrate, and then the whole structure is mounted to a printed wiring board (PWB) [47]. In type-3 integration, bare chips are directly packaged onto the second-level substrate and then mounted onto the PWB.

An example of type-2 integration is stacking bare-chip memory modules to increase the memory density per unit chip area [48]. In the particular study, each of four 4M packaged DRAMs were electrically connected to chip carriers, which contain metal interconnects and bond pads, using Au solder balls at 350-400°C. Glass epoxy films of 50μm were used to physically attach the memory chips onto the carriers. Then, large Pb/Sn solder balls were formed at the edges of the chip carriers. Each chip carriers were stacked together by aligning and melting the solder balls at 230-250°C. In other examples, instead of memory modules, 3-D structures can also be assembled with fully packaged integrated circuits [49]. Some different schemes include stacked tape carriers, solder edge conductors, thin film conductors on face-of-a-cube, interconnection substrate soldered to a cube face, and folded flex circuits.

An example of type-3 integration is related to a class of MCM process approach called thin film deposited MCM (MCM-D) [5]. In this approach, interconnect structures are built from alternating metal layers, usually sputtered Al or Cu, and thin dielectric films such as polyimide. The interconnect layers is either grown on a ceramic substrate (chip-last) or on the chip itself (chip-first). In chip- last technology, the chip sits on top of the interconnect structure. There are two ways of electrically contacting the chip to the interconnects. If the chip is facing up, then wire bond or TAB is required to connect the top of the chip to top of the interconnect structure. On the other hand, the chip can be bonded to the interconnects face-down with solder ball connections. This is commonly known as "flip-chip" bonding, and it is often the preferred way of constructing MCM-D structures.

Next, in chip-first technology, the interconnect sits on top of the chip. This configuration is usually referred to as "embedded chip" [5]. There are two main advantages of using embedded chip schemes. First, the thermal path from the chip to the heat sink is minimized, since the chip itself sits on high-thermal

conductivity substrates such as alumina or aluminum nitride (AlN). Second, since the thin- film interconnect structure is created on top of the chip, wire bonds, TAB, and solder bump connections are eliminated. Overall, flip-chip has an advantage over embedded chip in one aspect: Testing and repair. If an embedded chip was found to be faulty during tests, replacing the chip would require stripping the interconnect layers above it. Meanwhile, replacing a faulty flip-chip would be a quick fix - just melt the solder joints and replace the chip with another. Therefore, flip-chip bonding alleviates the "known-good-die" dilemma. If embedded chips are desired, then bare-die burn-in tests are required to increase die yield.

2.4 Other Approaches

In addition to wafer bonding, silicon epitaxy, and MCM, there are other ways of 3-D integration, both on a wafer scale and on a chip-scale. For example, device wafers can be stacked together using tabs, pinholes, and wafer-to-wafer alignment fixtures at the wafer edges [6]. To electrically connect wafers on different levels, Al dots are first formed on n-type Si wafers. From the Al-Si phase diagram, 1.5 atm migrate into Al upon annealing, and p-channels will form in the n-Si wafer, serving as inter-wafer vias. Then, micro-spring bridges are formed on the wafer backside using MEMS techniques, with contact pads aligned with the inter-wafer vias. By placing successive springs in a crossing pattern, wafers on different levels can then be electrically connected to one another. Other ways of making active layer-to-active layer connections include laser drilling / solder fill 34, using lasers to write metal lines on faces of MCM cubes [49], using conductive materials in castellation, etc.

Chapter 3

Experimental

3.1 Proposed Research

After evaluating possible DVI technology options, metal-to-metal wafer bonding was chosen to be pursued. Thin metal films from both wafers will fuse together upon applying compressive force and heat, which provide enough adhesion to bond the wafers together. Such metal-to-metal bonding has been demonstrated using Cu-Cu bumps in chip bonding applications [50]. In the particular study, Cu bumps with size and height varying from 10 μm to 30 μm were electroplated on a substrate, while on another wafer thin-film Cu lines of unspecified thickness (approximately 2 μm from sem) were electroplated on a Si chip. Afterwards, solder balls are created on the substrate for chip alignment purposes. Then, both the Cu bumps and the thin Cu lines were sputter cleaned using Ar beam radiation in a vacuum chamber, thereby activating the metals. Chip-substrate contact was performed by first aligning the chip to the substrate using solder ball attachments. At the same time, if both chip and substrate contain a uniform surface topography, the substrate Cu-bump would be in contact with the chip Cu-film (separated by 10 to 30 μm), and the activated metal surfaces would mutually create a chemical bond. In the case of uneven surface topographies, air gaps between the Cu-bump and Cu-film would be filled by injecting Cu plating solution into the separation. Note that all steps following Ar activation was performed in a clean, vacuum environment (in- situ).

This thesis will focus on an extension of the Cu-Cu chip attach technology. Namely, one could extend the metal-to-metal bonding technique to the wafer-level. Surface-activated bonding, however, was not pursued in the thesis study because the Ar-sputtering chamber and the in-situ Cu plating apparatus from [50] was quite specialized. In all, the bulk of the thesis will focus on metal-to-metal bonding using three systems: Au-Si eutectic, NiSi, and Cu-Cu films. Optimization of bonding temperatures below 450°C, in compliance with Al metallized devices, will be attempted. The proposed 3-D structure is shown in Figure 3-1.

From Figure 3-1, metal (Au, NiSi, or Cu) bumps on both wafers can serve as electrical contacts between the inter-strata via on the top wafer and Al interconnects on the bottom wafer. These metal bumps also

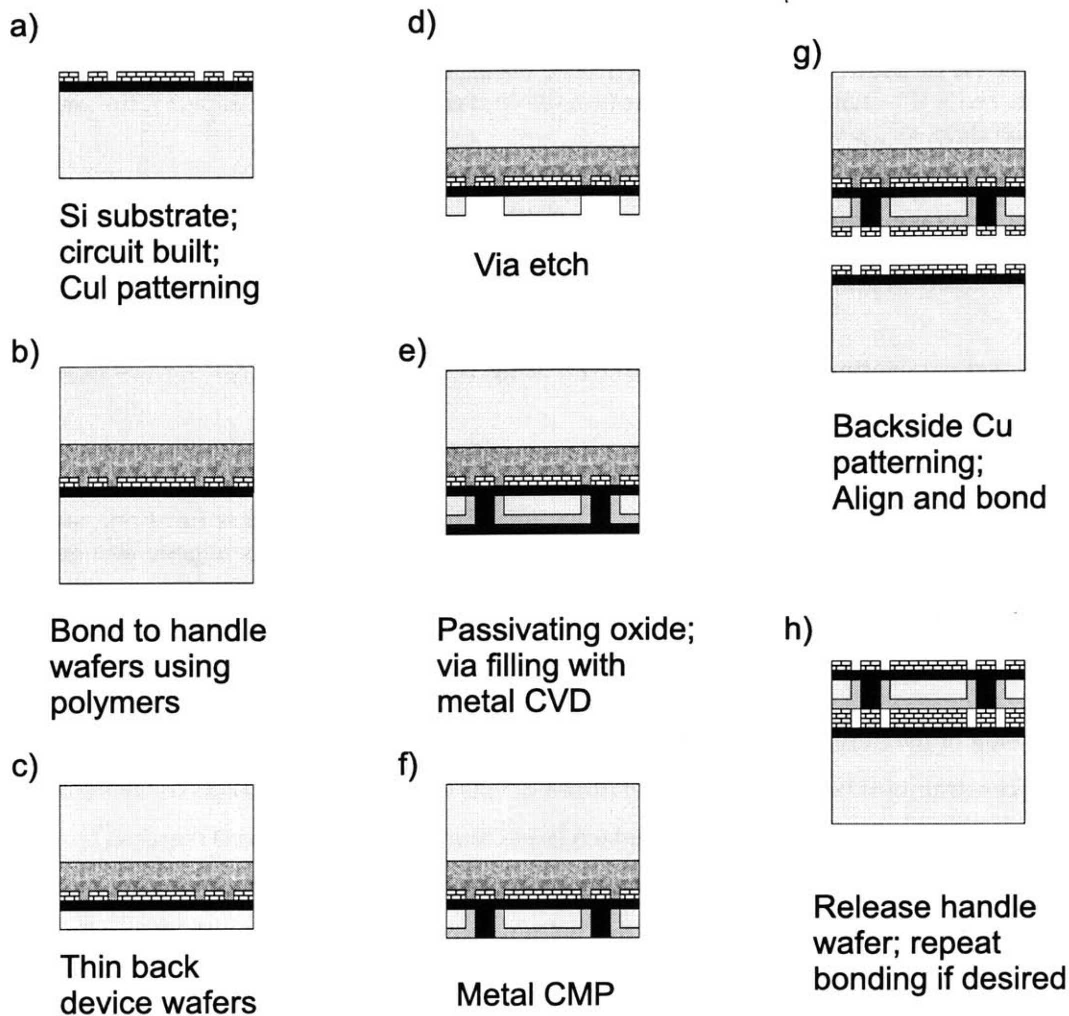


Figure 3-1: Process flow of proposed structure.

function as small bond pads for wafer bonding. The thesis work would not involve measuring the contact resistance of the wafers, but merely testing the bondability of the bumps. The process flow can be summarized as follows. The DVI example presented below refers to Cu-Cu bonding with Ta diffusion barriers [51]. Generalization to Au-Si and NiSi bonding is immediate, with Au metal / TiW diffusion barrier and Ni metal / Si film replacing the Cu bumps:

1. The starting point is a front-to-back-end completed device wafer, preferably built on SIMOX wafers for easy substrate etchback. Copper-diffusion barrier (Ta) bumps are patterned onto the interconnect layer.
2. The device wafer is then bonded to a handle wafer using polymers, for example photoresist. This bonding steps does not require special wafer-to-wafer alignment.
3. The Si substrate of the stratum is thinned back to prepare inter-wafer via etch-fill. If the stratum was built on a SIMOX wafer, the etchback stops at the buried oxide layer (BOX), which is removed

afterwards. Resultant Si substrate thickness should be around 200 nm. Otherwise, Si is etched back using mechanical grinding, which would make the Si substrate thickness be about 20 μm (if lucky).

4. Inter-wafer via of width 2 to 5 μm is etched. The via aspect ratio would be small if SIMOX wafer is used. Otherwise the etching step could prove to be challenging, for the via aspect ratio can approach 10:1 (20 μm deep vs 2 μ wide).
5. Electrical isolation between the via and the substrate is a must. The passivating oxide needs to have conformal coverage, which makes CVD oxide (TEOS) very attractive. Via filling can be performed using standard CVD W deposition. Again, if the via aspect ratio approaches 8:1 or 10:1, then via filling without void formation also becomes a technological challenge. Cu plating might be an option here.
6. Excess W and passivating oxide can be removed using W CMP. The post-CMP surface should exhibit global planarity.
7. Cu-Ta bumps are formed at the backside of the device wafer, which is aligned with the inter-wafer vias. Notice not all Cu bumps are electrically connected to the via or the substrate. These are auxiliary Cu films that increase the wafer bonding surface area. They could offer other functions, such as heat conduits, electrical ground or power planes, etc. Then, the device wafer is aligned and bonded to a pre-existing device wafer, having gone through step "a'.".
8. After wafer bonding, the handle wafer is released. The resultant multi-strata stack can be bonded to another device wafer through repeat of step "g".

The main result of the thesis work is that Cu-Cu wafer bonding was successful at 400°C, which satisfies the processing constraints of both Al and Cu metallized device wafers. This was achieved using two Cu/Ta bilayers, with a combined thickness of 700 nm, which is less than the usual thickness required for polyimide wafer bonding (1-2 μm) [27]. Finally, the Cu film does not require special planarization steps such as metal CMP or etchback prior to bonding. In addition to Cu-Cu wafer bonding, Au-Si and NiSi bonding was also explored.

3.2 Gold Wafer Bonding

Since Au is a deep-level trap for carriers, the first task to the Au-Si eutectic bonding experiment was to test the effectiveness of the reported 3:97 Ti:W (by weight) diffusion barrier [37]. In the reference, 100 nm of sputtered TiW was an effective Au diffusion barrier up to 700° C at low DC bias and nitrogen incorporation during sputtering. However, such films suffer from high resistivity (ρ=180 μm-cm) when film thickness is greater than 70 nm. Pure TiW films without nitrogen incorporation has inferior diffusion barrier qualities compared to TiW(N). If the diffusion barrier analysis is reproducible, then the next task is to bond blanket SiO_2-TiW-Au wafers with plane SiO_2-TiW-Si wafers face-to-face. One of the wafer contains evaporated Si because the solubility of Si in the TiW alloy was not known at the time. Recall from Section 2.1.4 that a lack of Si solubility in an adhesion / diffusion barrier could prevent the Au-Si eutectic reaction from ever happening. At the same time, ways of patterning Au will be explored, in particular finding a suitable Au sputter-etching chemistry.

3.2.1 Au Deposition and Bonding

The starting materials for the Au-Si wafer bonding experiment was 4 in n-type Si test-grade wafers. To begin with, Si wafers underwent RCA cleaning (SC1 for 10 min, HF for 30 sec, SC2 for 10 min):

- SC1: Removal of organic contaminants with 5:1:1 H_2O:H_2O_2:NH_4OH
- HF : Removal of thin native SiO_2 using a dilute 50:1 H_2O:HF solution
- SC2: Removal of metal contaminants using 6:1:1 H_2O:H_2O_2:HCl

Then, 600 nm wet thermal oxide was grown on the blanket Si. Ten oxide wafers were sent to Lincoln Lab for sputtering of 100 nm of 3:97 Ti:W. Unfortunately, a 3:97 TiW target and N_2 incorporation during sputtering was not available. Therefore, the oxidized wafers were sputtered with 100 nm of 10:90 TiW film without nitrogen stuffing, but substituted with 5 min ambient air exposure for TiW grain stuffing [52]. Afterwards, 1 μ of Au was electron-beam evaporated onto the TiW barrier. Upon Au deposition, it was apparent that Au films do not adhere well to TiW. Gold would be scratched off in the vicinity of wafer handling using tweezers. Despite of the non-adherence, most of the Au film was intact, and one proceeded to bond oxide-TiW-Au wafers to oxide-TiW-Si wafers. The overall experimental matrix is outlined in Figure 3-2.

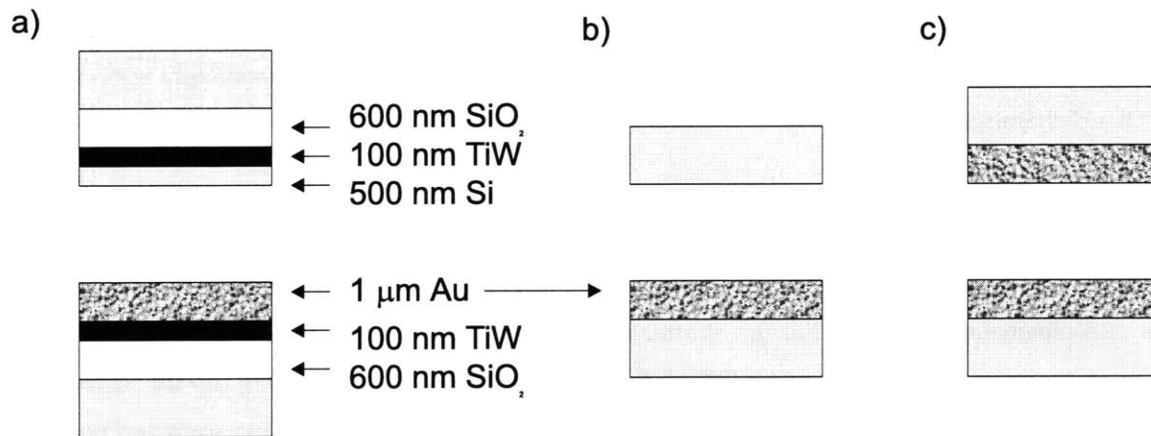


Figure 3-2: Gold bonding experimental matrix.

Immediately prior to wafer bonding, all wafers were subjected to 10 to 60 min ultraviolet radiation in order to remove organics from the wafer surface. Through further testing it was found that UV exposures may not have a bearing on the bondability of TiW-Au system. To continue, wafer bonding was initially done using by pressing the wafers together with an approximately 10 kg weight, and at the same time annealing was done in a ceramic oven at various temperatures centered around the Au-Si eutectic point (363°C). Wafer bonding was unsuccessful at all temperatures and durations in this schemes. Then, wafer

bonding was attempted in the Electronic Vision EV 450 Aligner and AB1-PV Bonder. The bonder contains four control parameters: Bonding temperature, chamber gas pressures, contact force, and contact duration. Two variables were fixed: The contact force was set to 4000 mbar, and the chamber gas pressure was set on N_2 purge. The bonding procedure begins by using the EV aligner to clamp together two wafers, separated by 30 μm flaps, on the bond chuck. The bond chuck was then transferred to the bond chamber. The basic script for EV-bonder (inside the bond chamber) runs can be written as:

1. N_2 purge on for 30 sec
2. Evacuate chamber to 10^{-3} torr
3. N_2 purge on for 30 sec
4. 300 mbar contact force - at center of wafer
5. Remove the three 30 μm wafer separation flaps
6. 4000 mbar contact force
7. Heating both top and bottom wafer to desired temperature (40°C/min).
8. System idle for variable duration upon reaching desired temperature
9. Contact force removed
10. Cooling to room temperature

The desired temperatures ranges from 360°C to 400°C, while the idling duration was set from 10 min to 30 min. Again, wafer bonding failed in all test matrices - the wafers separated immediately upon removal from the bond chamber.

3.2.2 Au Sputter-Etching

While waiting for the completion of TiW sputtering, Au sputter etching was performed in Oxford pecvd-rie chamber and plasmaquest in TRL. For the sputter-etching runs, test-grade n-type wafers were deposited with 1 μm of Au upon pre-metal cleaning (3:1 H_2SO_4:H_2O_2 for 10 min; 50:1 H_2O:HF dip for 30 sec). Note that no adhesion layers (such as Ti) was deposited. Then, 6 μm of AZ P4620 resist was spun and patterned. The contact mask for contained vertical grating patterns with linewidths from 200 μm down to 60 μm.

In sputter-etching of Au, CF_4 was chosen as the gas etchant, and the variables were RF power, etch time, gas flow rate, and chamber pressure. The maximum RF power in the Oxford was 350 W, the maximum CF4 flow rate was 42 sccm, and the minimum obtainable chamber pressure was around 50 mtorr. All etch matrices were unsuccessful in the Oxford. Generally the plasma failed to stabilize at low chamber pressures, which is essential for anisotropic sputter-etching. Surface profiling showed that the plasma only removed resist and perhaps an undetectable amount of Au.

On the other hand, successful etches occurred in the Plasmaquest, where much lower pressure can be obtained. Successful etch conditions were:

- Power = 50 W
- Flow rate = 42 sccm of CF_4
- Chamber pressure = 5 mtorr
- Ech rate = 3.3 A/sec

However, this result was only reproduced twice. Because of the high bias power, burning of the resist in subsequent etch runs was encountered. In addition, Teflon formation, or polymerizations of CF_4 into -$(CF_2)_n$- on the Au surface, may have prevented further etching of Au. At that particular point, incorporation of O_2 in the etch chemistry did not alleviate the problem. Lowering the bias power results in a decrease in Au etch rate. At 20 W of bias power, the Au etch rate decreased to 1.28 A/sec, indeed a very low etch rate for 1 μm Au etches.

3.2.3 TiW Diffusion Barrier Analysis

For TiW diffusion analysis, a wafer with 100 nm of Au was evaporated onto the TiW barrier, again with no adhesion layer for Au. One wafer was cleaved into four pieces and each piece underwent three cycles of rapid-thermal annealing (RTA) at various temperatures to simulate the thermal budget needed for Au-Si bonding (10-15 min).

Sample	A	B	C	D
Temp(°C)	350	370	400	450
Total time (min)	15	10	10	10

Table 3.1: RTA table for TiW diffusion. Note: RTA ramp-up speed is 50°C/sec.

After annealing, the four samples underwent Rutherford back-scattering spectroscopy (RBS) analysis to examine the TiW diffusion barriers' effectiveness. The beam conditions are: 2 mm diameter, 3 MeV He^{++} incident ions. The RBS system can detect elements down to about 0.5 atomic percent of the host crystal (Si). Therefore, one can only detect Au concentrations around 10^{20} atoms/cm^3. The general results were:

- There was no evidence of gold diffusion in ALL samples.
- Using the pre-annealed sample and simulated RBS plots as references, it appears tha the Au films were a little thicker than 100 nm.
- Comparing the simulated plots from the experimental, the TiW layer was about 90 nm and the SiO_2 layer was close to 900 nm, an unexpected result.
- The TiW composition was approximately 15:85 of Ti:W, not 10:90 by weight.

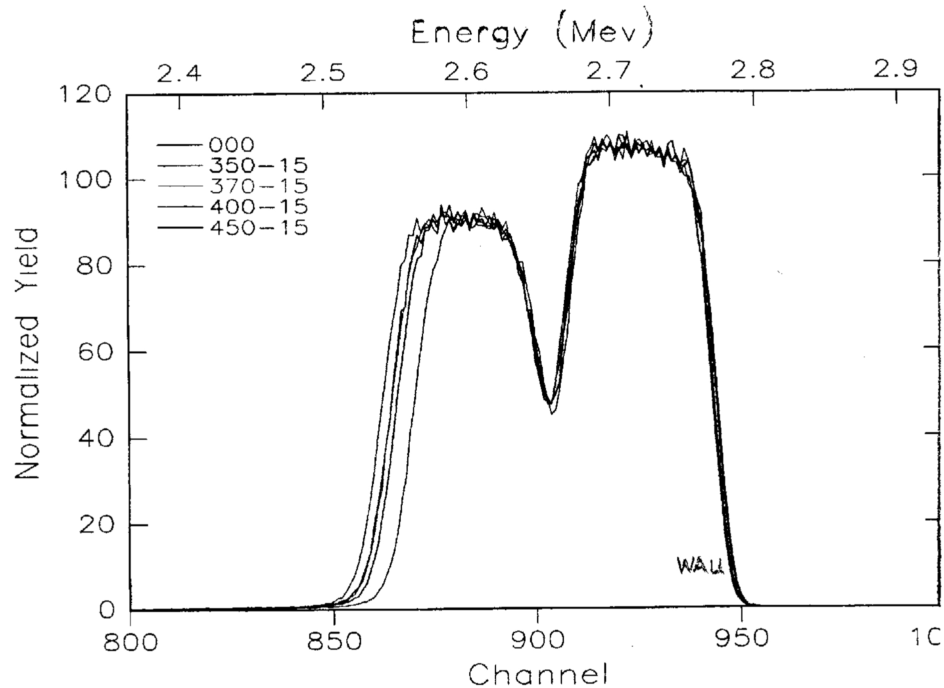


Figure 3-3: Au-TiW RBS Analysis.

3.2.4 Results and Discussions

In all, the Au-Si wafer bonding experiment was unsuccessful. Some speculations on why the wafers failed to bond may include the following. To begin with, in wafer bonding experiments, it is usually more reliable to use prime-grade wafers because of improved planarity and reduced wafer bow. In fact, wafer bowing could be a deciding factor in whether two wafers can indeed have face-to-face contact. Next, the lack of adhesion of Au on TiW may also be detrimental to wafer bondability. Titanium adhesion layer deposited on top of TiW should alleviate this problem. Third, native oxide formation on the e-beam Si layer can also affect the Au-Si bonding interface (refer to Section 2.1.4 for details). Finally, the Si solubility in TiW may be very low, thus causing insufficient Si concentration for Au-Si eutectic reaction to proceed. Along the same line, TiW was shown to prevent Au diffusion into Si within the wafer bonding temperature range.

Furthermore, the sputter-etching of Au with CF_4 was a success. However, the Teflon formation on Au dilemma still needs future attention. A remedy to this problem is to include more O_2 concentration in the CF_4 plasma to induce ashing of fluorocarbons. On the issue of burnt resist, an answer can be found if one experiment with metal hard-masks instead of resist masks for Au patterning.

3.3 Nickel Silicide Wafer Bonding

According to [40], two wafers with 300 nm of Ni deposited on Si can be bonded face-to-face provided annealing the contacted pair at 440°C, apparently without any surface preparation. At this temperature, the main diffusion component are the Ni atoms, and all 600 nm of Ni should react with single-crystalline Si

to produce NiSi, a low resistivity film. The thesis work will focus on reproducing the reported result and qualitatively compare the bonding strength between different annealing temperatures. Also, the chemical species at the bonding interface will also be examined using Auger electron spectroscopy, as well as the effect of annealing on the Ni-Si interface by itself.

3.3.1 Nickel Deposition and Bonding

Since the Ni experiment was done at the same time as the Au-Si bonding experiment, the test- grade wafer bowing variable was not thought of. Therefore, the following films were deposited on test-grade n-Si wafers (see Figure 3-4):

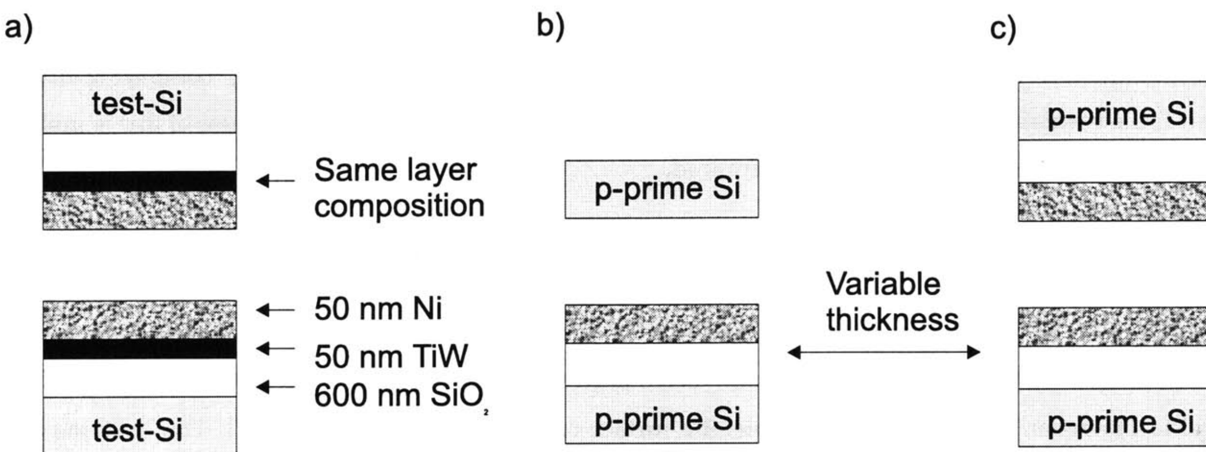


Figure 3-4: Nickel Silicide experiment matrix, in lieu with Table 3.2.

The Ti adhesion layer was added because Ni films exhibits high stress when deposited on bare Si. This fact was ignored afterwards when 300 nm of Ni seemed to adhere well. To continue, after the films were deposited, wafer bonding began with face-to-face contact of Ti-Ni to another Ti-Ni wafer. Wafer contact was made by placing a quartz boat on top of the wafer pair, and the whole system was annealed in a furnace at 440°C, N_2 purge for 2 hrs. The end result was obvious - the wafers were not in contact because much of the Ni on the wafer surface (metallic silver) turned to light blue, a sign of Ni oxidation or silicidation. The answer to this question was found by comparing the Auger depth profile between an unannealed Ni-Ti-Si sample and an annealed sample see Section 3.3.2.

Once Auger analysis determined that no NiSi films were present, the Ti-Ni test-grade wafers were abandoned, and Ni wafer bonding was attempted with a new set of p-prime Si-Ni(300 nm) wafers in the EV-bonder. The following table shows the test matrix:

From Table 3.2, Ni wafers were successfully bonded at conditions shown in entries C, where both wafers contained 300 nm Ni and were annealed at 600°C. This condition can be compared to entry E, where all the variables were the same, except the annealing temperature was reduced to 450° C. From these two entries,

Entry	Wafer 1	Wafer 2	Bond temp	Bond time	Anneal temp	Anneal time	Bonded ?
A	Ni=300 nm	Si	450°C	10	n/a	n/a	no
B	Ni=300 nm	Si	450°C	10 min	600°	120 min	no
C	Ni=300 nm	Ni=300 nm	450°C	60 min	600°	30 min	yes
D	Ni=300 nm	Si	450°C	60 min	600°	30 min	no
E	Ni=300 nm	Ni=300 nm	450°C	60 min	450°	30 min	no
F	Ni=50 nm	Ni=50 nm	450°C	60 min	450°	30 min	no

Table 3.2: NiSi bonding experimental matrix.

it can be generalized that a post-bonding anneal of greater than 450°C is necessary to ensure good bonding between Ni-Ni wafers. From entries A, B, and D, it seems that the Ni-bare Si system does not bond very well to each other. It is highly speculative that a thin Si native oxide on the blank Si wafer is impeding Ni diffusion, which inhibits NiSi reaction from lack of Ni atomic concentration. Finally, comparing entries C and F, the bondability of Ni-Ni wafers seems to be a function of Ni thickness. The cause of this is unknown at the moment and further studies are required.

3.3.2 Ni-Si Auger Analysis

From Section 3.3.1, the chemical composition of an unannealed Ni-Ti-Si wafer was compared to an annealed Ni-Ti-Si film. From auger surface analysis, the unannealed sample surface contained the expected Ni, O, and C. However, on the annealed sample, the surface contained Ni, Ti, O, C, and Cl. The Ti atoms on the surface was a surprise. This might suggest that upon annealing Ni has diffused into the Ti adhesion layer, creating a layer inversion similar to NiSi on polysilicon at high temperatures (see Section 2.1.5 for details).

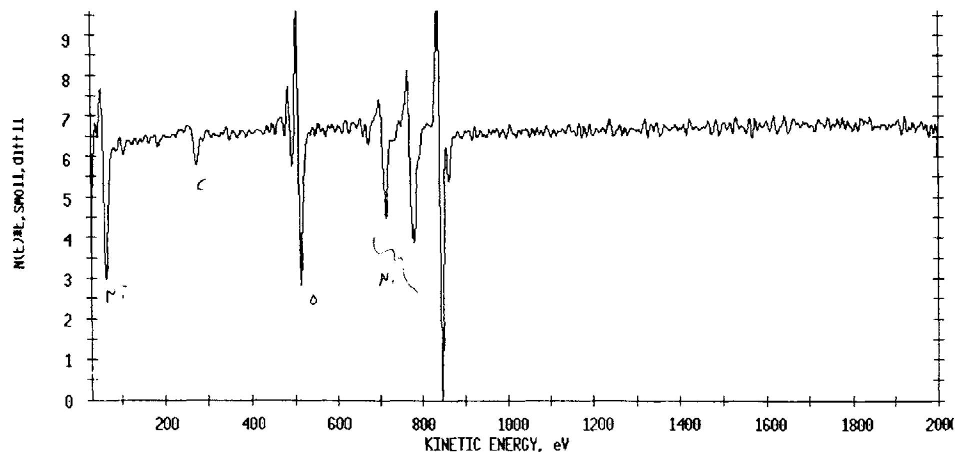


Figure 3-5: Auger surface profile of unannealed Ni-Ti-Si sample.

From Auger depth analysis, the unannealed sample (Figure 3-6) showed that there is a sharp boundary

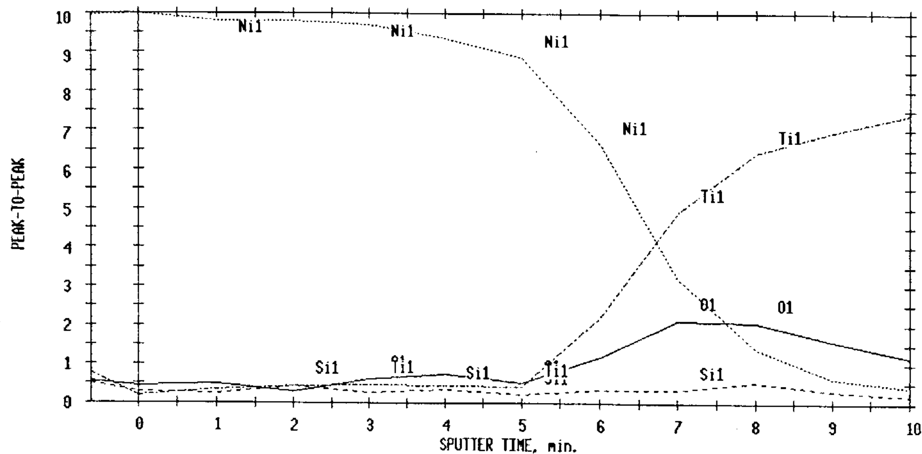


Figure 3-6: Auger depth profile of unannealed Ni-Ti-Si sample.

between the Ni-Ti interface. The oxygen content at the wafer surface was nominal, thereby suggesting only a native nickel oxide is present. From Figure 3-8, the sharp transition of Ni was not evident in the annealed sample, even though the Ti concentration was not monitored during the sputtering. Finally, from both depth analysis plots in Figures 3-6 and 3-8, the NiSi compound was definitely not present because the Si concentration was too low with respect to Ni throughout the entire sputtering sequence. The lack of NiSi may be due to the inability of Si or Ni to reach each other because of the Ti adhesion layer. Finally, one must caution in analyzing Figures 3-5 and 3-7. The Auger surface plots only reveal a survey of chemical species that exists on the wafer surface. The difference in magnitude between peaks do not correlate to a relative concentration between different atomic species.

3.3.3 Results and Discussions

In general, the following conclusions can be made from the studies in Sections 3.3.1 and 3.3.2:

1. Bond was successful at 450°C for 60 min in N2, 4000 mbar pressure (with 1000 mbar during temperature ramp-up), post-bonding anneal at 600°C for 30 min in N2. Used prime-grade wafers.

2. Ni thickness was found to be important. In the bonded pair above, Ni = 300 nm each. When Ni = 150 nm, the bond was unsuccessful, as well as in Ni = 50 nm.

3. The annealing temperature could not be pushed down to < 600°C. Therefore, it may not be a suitable bonding technology for Al-metallized wafers. In addition, the results from the Ni-bonding literature [40] (440°C bond for 2 hrs in N2) could not be reproduced.

4. In the beginning, the Ni film was though to have high stress when deposited on Si. Therefore, a Ti adhesion layer was added. Bonding with Ni/Ti did not succeed; Auger analysis upon annealing a Ni/Ti wafer showed massive oxide growth on the Ni surface and no Ni diffusion into Si or vice versa. Therefore,

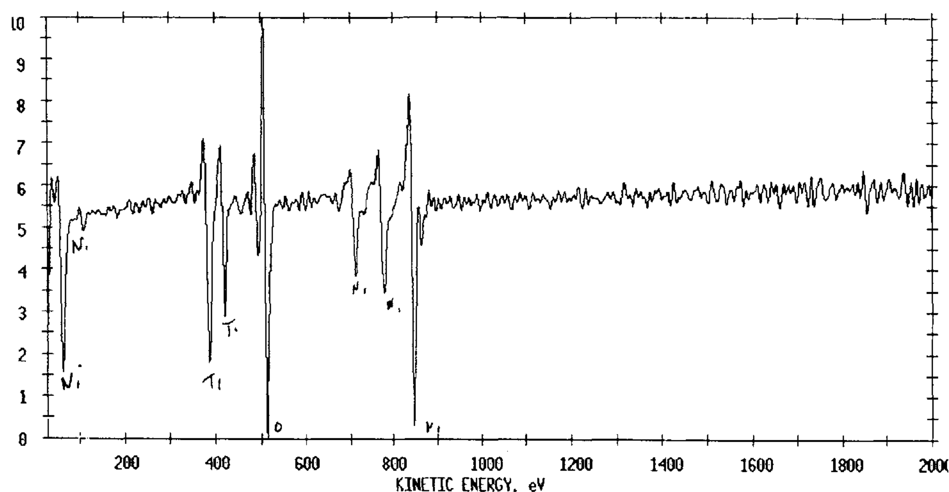


Figure 3-7: Auger surface profile of annealed (450°C) Ni-Ti-Si sample.

no NiSi was detected. Also, Auger surface spectroscopy showed evidence of Ni-Ti inter-diffusion upon annealing at 440°C.

3.4 Copper Wafer Bonding

3.4.1 Copper Deposition and Surface Preparation

The starting materials were four groups of prime-grade p-type Si wafers. Prior to metal deposition, all wafers were cleaned in H_2SO_4:H_2O_2 (3:1 by volume) for 10 min, followed by DI water rinse. Then, the wafers were dipped in H_2O:HF (50:1) for 20 sec to remove native oxide on the silicon surface. Next, four different metal compositions were deposited on the four wafer groups by e-beam evaporation: 300 nm Cu, 300/50 nm Cu/Ta, 150 nm Cu, and 150/50 nm Cu/Ta. The Ta layer acts as a Cu diffusion barrier up to 550°C. Furthermore, on some wafers, Cu lines were formed by wet etching in H_2O_2:HCl:H_2O (1:1:125), a solution with an etch rate of 37 A/sec. The line widths range from 60 μm to 200 μm. Prior to bonding, some wafers from each of the four groups were dipped in 1:1 (by volume) H_2O:HCl for 30 sec followed by DI water rinse / spin dry. The purpose was to remove any native oxide that exists on the Cu surface. The HCl treated wafers were then bonded separately from the untreated samples.

After metal deposition and HCl treatment on selected wafers, all samples were ready to be bonded in the EV-bonder. Two variables were fixed: the chamber gas pressure was set to 1000 torr N_2 purge throughout bonding, and the contact force was set to 1000 mbar during wafer heating and 4000 mbar during bonding. Afterwards, it required 2 hrs to cool the wafers to room temperature inside the chamber. The bonded wafers were then subjected to post-bonding anneals at various temperatures in N_2. Finally, the razor test was performed to assess the bonding qualitatively. Bonded interface properties were examined using a

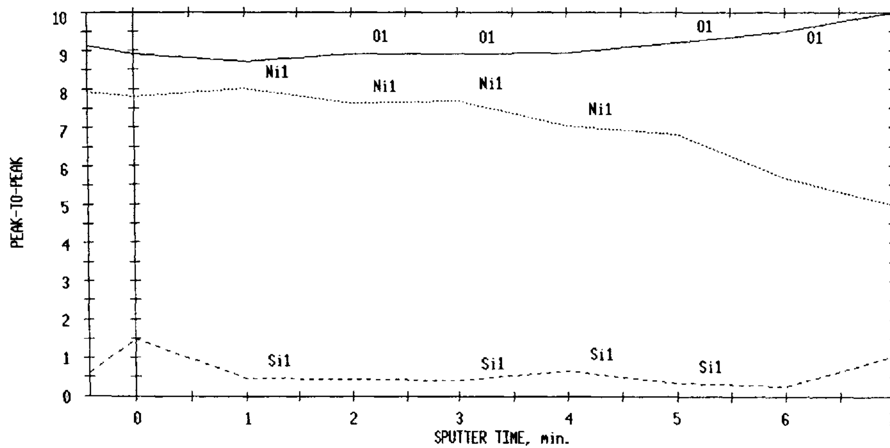


Figure 3-8: Auger depth profile of annealed (450°C) Ni-Ti-Si sample.

cross-sectional SEM and Auger electron spectroscopy.

3.4.2 Results and Discussions

Various bonding and annealing conditions are listed in Tables 3.3 thru 3.5. The bond strength was qualitatively determined with the razor test. An indication of a strong bond is when the razor cannot penetrate the bonding interface [35].

Entry	Cu film	HCl treated	Anneal	Anneal duration	Bond quality
A	300 nm	No	620°C	30 min	Good
B	300 nm	No	n/a	n/a	Partial
C	300 nm	No	620°C	30 min	Poor

Table 3.3: Bonding of wafers with variable Cu thickness without Ta barrier layers. Cu thickness are the same for both top and bottom wafers. Bonding temperature was set at 450°C, and the bonding duration was 60 min.

In Table 3.3, the bond strengths can be delineated as follows: A "good" bond is where a razor cannot penetrate the bonding interface and the wafers were inseparable. Also, in these cases, the bonded wafers fracture not at the interface, but chip off small bonded fragments. Next, a "partial" bond is where the wafers would separate from the bonding interface when considerable force is applied to the razor. Finally, a "poor' bond is where the razor separates the two wafers with relative ease or the wafers did not bond at all. Note that in all bonded wafers, a razor can be inserted at the wafer edges because those points lack Cu coverage.

From Table 3.3, wafers bonded at 450°C with only 300 nm untreated Cu films (untreated with HCl) passed the razor test regardless of post-bonding anneals. The wafers were inseparable with a 620°C anneal, while "partial" bonding was achieved without anneal. Post-bonding anneals do improve the bond-

ing strength qualitatively with respect to the razor test. However, inside given temperature range (400 to 620°C), the temperature at which the anneals occurred did not seem to have an affect on the bonding strength. The physical mechanism of the post-bonding anneal effect is still being investigated. By comparing entries in Tables I-III, all 300 nm untreated Cu wafers had "good" bonding strength when post-bonding anneal was applied (620°, 450°C, and 400°C), regardless of the presence of the Ta barrier layer.

Next, in the "partial" bonded entry of Table 3.3, the razor pried off small Si pieces from a single wafer, and the Cu layer is ripped off from one of the two interfaces. This shows that the fusion of Cu-Cu films from both wafers create a very strong bond. However, in the thin untreated Cu film (150 nm) entry in 3.3, the razor easily separated the two wafers in whole. Therefore, the bond strength of Cu-Cu not only depends on anneals but also on the film thickness. A lower limit on film thickness also limits the size of Cu patterns created using wet etch techniques. Smaller Cu features will increase the inter-wafer via density, thereby increasing the effectiveness of 3D-integration to some extent.

Since Cu diffuses very fast in bulk Si and it is a deep-level trap for carriers, a diffusion barrier is necessary to protect the active areas from the Cu bonding interface. From Table 3.4, successful bonding can also be achieved when a tantalum diffusion barrier layer is underneath the Cu layer.

Entry	Cu film	HCl treated	Bonding time	Anneal	Anneal time	Bond quality
A	300 nm	No	60 min	n/a	n/a	Partial
B	300 nm	No	60 min	450°C	30 min	Good
C	300 nm	No	30 min	450°C	30 min	Good
D	150 nm	No	30 min	n/a	n/a	Poor

Table 3.4: Bonding of wafers with Cu/Ta (Ta = 50 nm). Cu film thickness are the same for both top and bottom wafers. Bonding temperature was set at 450°C with varying bond time.

Again, comparing Table 3.4 to Table 3.3, the annealing temperature can be reduced to 4500°C without significant change to the bonding strength. Also from Table 3.4, bonding time in the chamber has been reduced from 60 min to 30 min. Furthermore, as in the 150 nm Cu case, wafers containing untreated Cu/Ta (150/50 nm) films had poor bonding strength.

Next, referring to the first three entries in Table 3.5, the top 300/50 nm Cu/Ta wafer was patterned, with line widths ranging from 60 mm to 200 mm, and bonded to a blanket Cu bottom wafer.

All bonded pairs were inseparable at points where Cu lines exist, regardless of HCl treatment (comparing entries A-D). Therefore, for Cu films with thickness of at least 300 nm, HCl surface cleans do not appear to have a significant effect on wafer bonding strength. Also from Table 3.5, both the bonding and annealing temperatures has been reduced to 400°C, which is an ideal temperature for back-end processing. Then, with the bonding temperature set to 400°C, the Cu thickness was reduced to 150 nm to further investigate the poor bonding achieved in Tables 3.3 and 3.4.

From the Tables 3.3 and 3.4, it appears that the wafer bonding quality deteriorates as Cu thickness decreases to 150 nm for samples not treated with HCl. However, from entry F of Table 3.5, 150/50 nm

Entry	Cu film	Treated/Patterned	Bond temp.	Anneal	Anneal time	Bond quality
A	300 nm	N / Y	450°C	450°C	30 min	Good
B	300 nm	N / Y	400°C	400°C	30 min	Good
C	300 nm	Y / Y	400°C	400°C	30 min	Good
D	300 nm	Y / N	400°C	400°C	30 min	Good
E	300 nm	N / N	400°C	n/a	n/a	Poor
F	150 nm	Y / Y	400°C	n/a	n/a	Good

Table 3.5: Bonding of wafers with Cu/Ta (Ta = 50 nm); Cu patterned on top of wafer wherever indicated, otherwise blanket films. Cu film thickness are the same for both top and bottom wafers. Bonding temperature varies while bonding duration was set to 30 min.

treated Cu/Ta wafers exhibited good bonding strength when bonded at 400°C for 30 min without post-bonding anneals. Also, from entry E of Table 3.5, the untreated 150/50 nm Cu/Ta wafer exhibited a poor bond at 400°C for 30 min without N_2 anneals. These results indicate that HCl surface treatments under certain conditions (ie. thin Cu films) does play a role in enhancing bonding strength of wafers. The HCl treatments, however, does not guarantee a Cu-Cu interface after the bonding process has been completed.

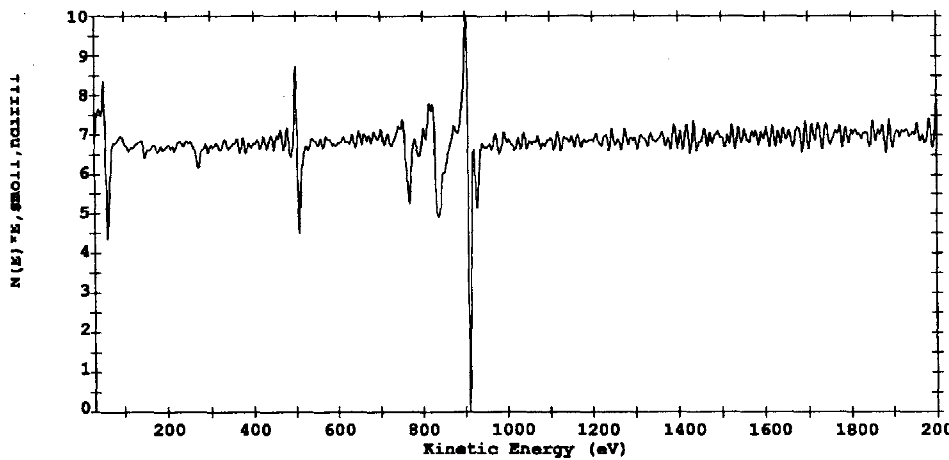


Figure 3-9: Auger surface profile of unannealed Cu-Ta sample.

Figure 3-9 is an Auger species survey of an unbonded, unannealed, and untreated 150/50 nm Cu/Ta surface. From this plot, the untreated surface contains significant amounts of Cu and O, followed by traces of sulfur (S) and carbon (C). The source of S and C may be originated from the e-beam deposition system or from general handling of the wafers. Figure 3-10 is an Auger depth profile for the same wafer. The oxygen (O) curve diminishes rapidly after 6 sec of sputtering, which suggests that a native copper oxide layer of 0.1-0.2 nm exists on the wafer surface. Results from Figures 3-9 and 3-10 was then compared to the Auger analysis (Figures 3-11 and 3-12) of a bonded, treated 150/50 nm Cu/Ta sample, more specifically the wafers

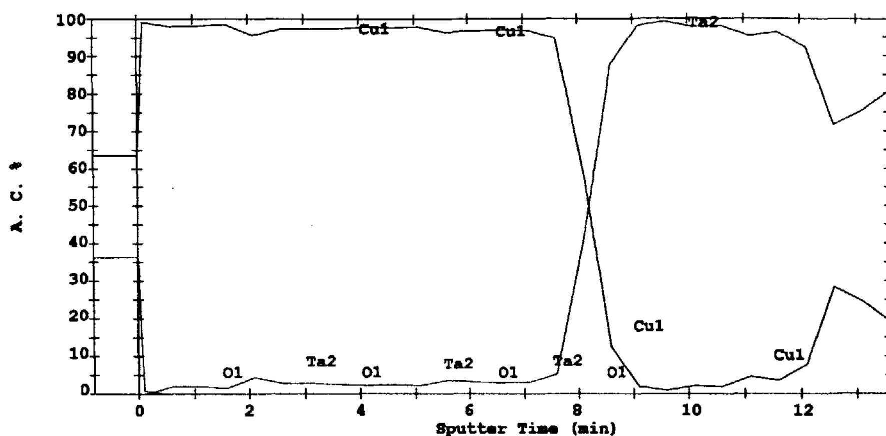


Figure 3-10: Auger depth profile of unannealed Cu-Ta sample.

in entry F of Table 3.5. Figure 4 3-11 shows that after HCl treatment, the C and S are either eliminated or below the detection level of the machine. Despite HCl treatment, there is still a significant amount of O between the Cu-Cu interface after bonding (no post-bonding anneals). This is confirmed in Figure 3-12, where a layer of approximately 35-70 A layer of copper oxide is on top of the Cu, assuming the sputter-rate of the oxide is the same as in Figure 3-10. In summary, the HCl surface treatment prior to bonding removes native copper oxide and impurities such as S and C on the wafer surface. But, it does not prevent oxide formation between the Cu-Cu interface during bonding. Also, for thick (300 nm or more) Cu, good bond However, the inclusion of HCl treatment does enhance the bonding of thin (approximately 150 nm) of Cu wafers

3.4.3 SEM Examination of Bonding Interface

To examine the bonding interface, several SEM images were taken to see if indeed there is a Cu-Cu interface contact. Ideally, Cu-Cu interface should not be visible even at high resolutions (except in TEM) when there is a true Cu-Cu metallic bond. Sample preparation for SEM proved to be difficult because bonded Si wafers have different cleave planes when not atomically aligned to each other. Die-sawing the samples does not improve the image quality; in fact, die-sawing destroys the bonding interface, and the Cu film was smeared throughout the cleaved plane. To begin with, a rectangular sample of length 2.5 cm was cleaved, starting from the edge of the bonded wafers. This is depicted in Figure 3-15

Figure 3-16 shows the Cu-Cu bonding interface at approximately 2 cm from the wafer edge. From this micrograph, the Cu-Cu interface (Cu is the bright region) was not very well-defined, nor is the Cu-Ta interface. The interface topography seems rough - the Cu in the picture almost looks like it is recessed-in on the left-hand side. This may be due the fact that a piece of Si on one side of the interface was removed

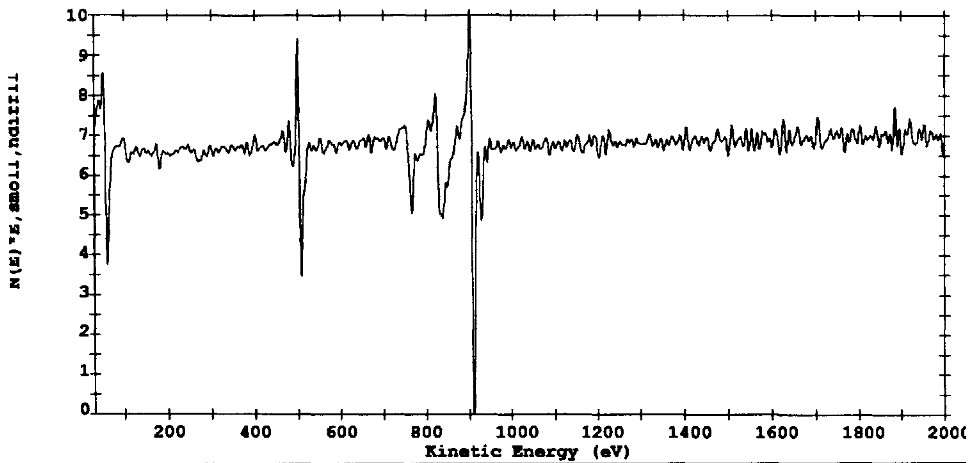


Figure 3-11: Auger surface profile of annealed (bonded) Cu-Ta sample.

while cleaving.

Figure 3-17 shows the Cu-Cu bonding interface at the wafer edge. The wafers were not bonded at this point because it lacked Cu-Ta coverage during metal evaporation.

Figure 3-18 shows the Cu-Cu bonding interface at approximately 1 cm from the wafer edge. Here, the two wafers surfaces were still not in contact. The Cu-film was accompanied by numerous pillar-like structures. The origin of these pillars are not known, but the Cu film surface, in general, appeared to be very rough and crystalline. Speculation of these effects include copper oxide growth, film morphology changes upon annealing, wafer-cleaving damage, etc.

Figure 3-19 shows a Cu-Cu bonding interface from another cleaved sample at low resolution. In this picture, the combined Cu thickness from both wafers totals to about 200 nm, which is significantly smaller than the anticipated 600 nm. Although this micrograph demonstrates a distinguishable Cu-Ta interface and a uniform Cu film, the unexpected thickness of the films makes this SEM figure questionable.

3.4.4 Conclusions

Cu metallized wafers were successfully bonded at 450oC for 30 min with a post-bonding anneal at 450°C in N2 for 30 min. Successful bonding was only obtained when the metal thickness is greater than 150 nm. Post-bonding anneals were necessary for wafer bonding, but annealing temperatures were not a factor in determining the bond strength from 400°C to 620°C. Also, the bonding time was found to be flexible from 60 min to 30 min. The Ta diffusion barrier between the Cu and Si did not affect the bonding strength or the bonding temperature. In conclusion, Cu wafer bonding may prove to be an useful option in future implementation of 3-D technology.

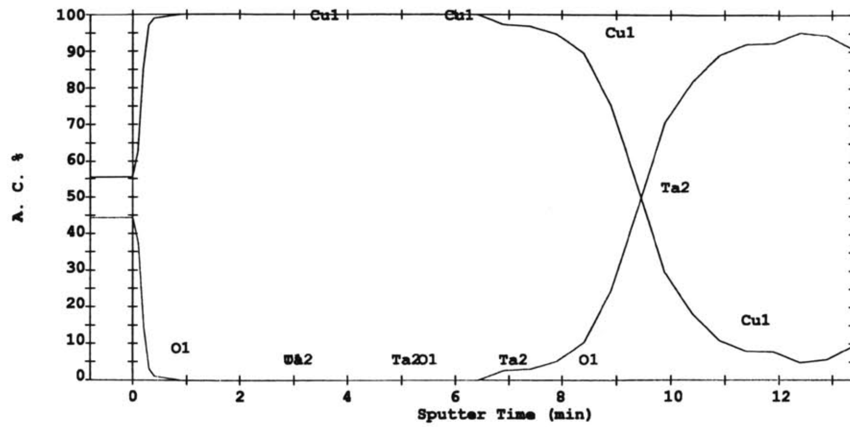


Figure 3-12: Auger depth profile of annealed (bonded) Cu-Ta sample.

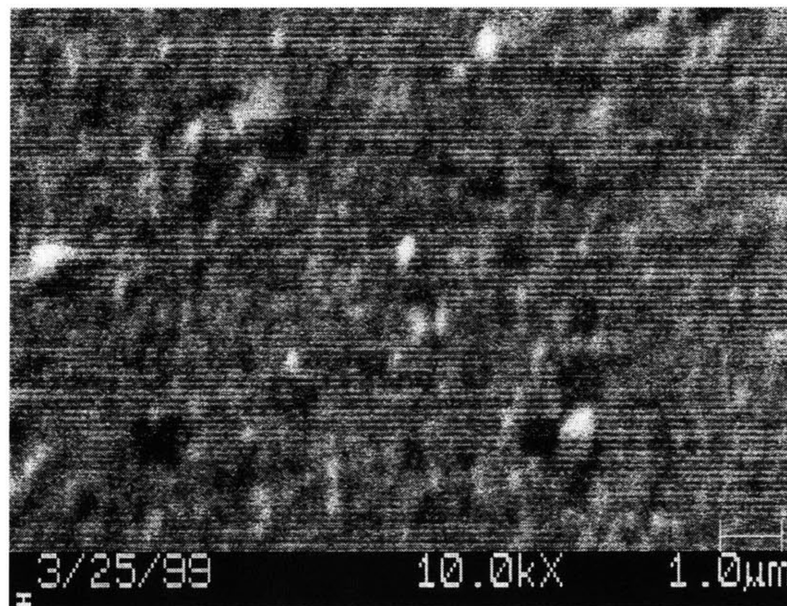


Figure 3-13: SEM of Cu-Ta interface in the unannealed sample. The surface is smooth compared to Figure 3-14.

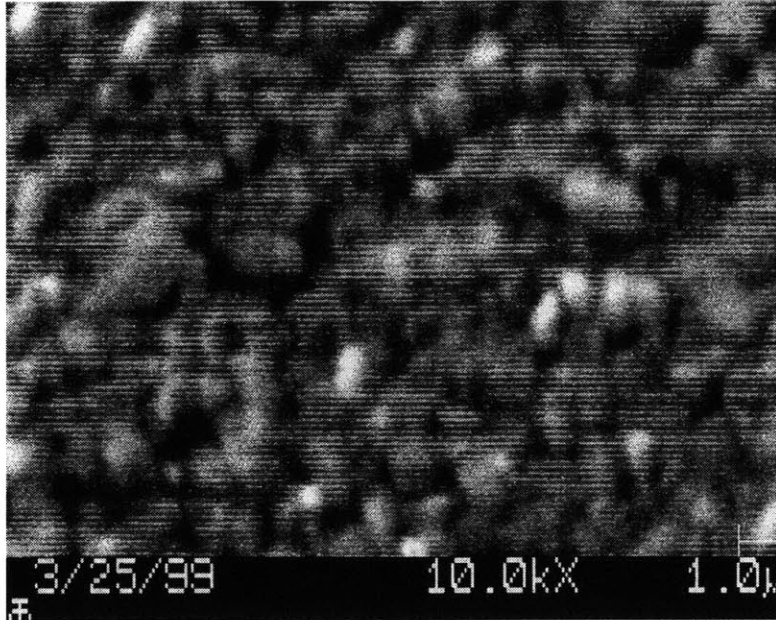


Figure 3-14: SEM of Cu-Ta interface in the annealed (bonded) sample. The surface is rough compared to Figure 3-13

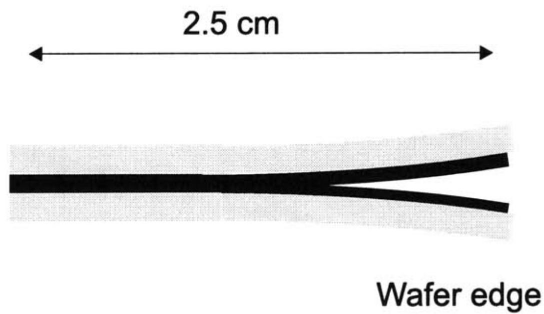


Figure 3-15: Example of a cleaved bonded-wafer sample for SEM.

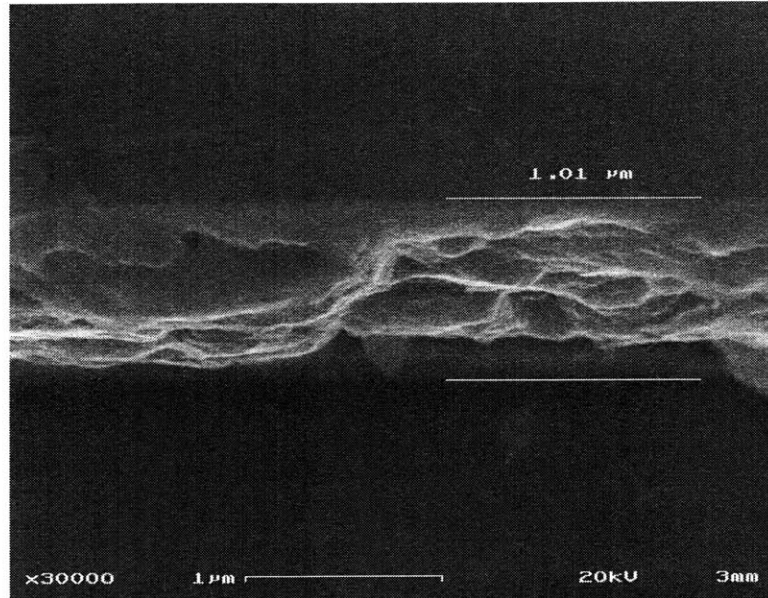


Figure 3-16: Cu-Ta Sample Bonded at 400°C for 30 min and annealed for 400°C for 30 min.

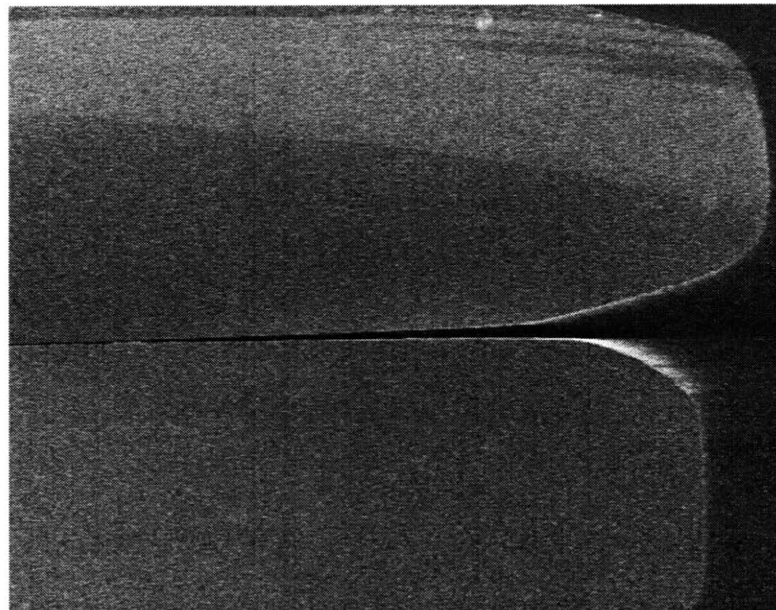


Figure 3-17: At the wafer edge; at 400°C for 30 min and annealed for 400°C for 30 min.

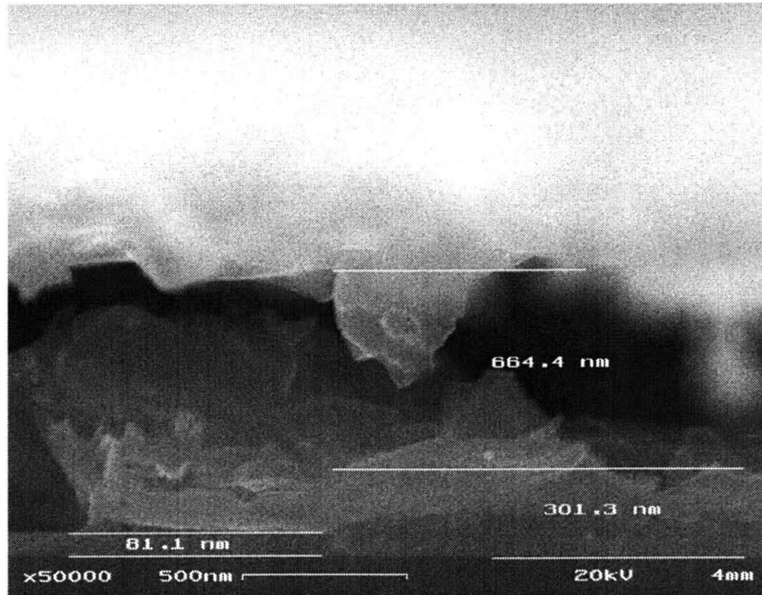


Figure 3-18: At 1 cm from the wafer edge; at 400°C for 30 min and annealed for 400°C for 30 min.

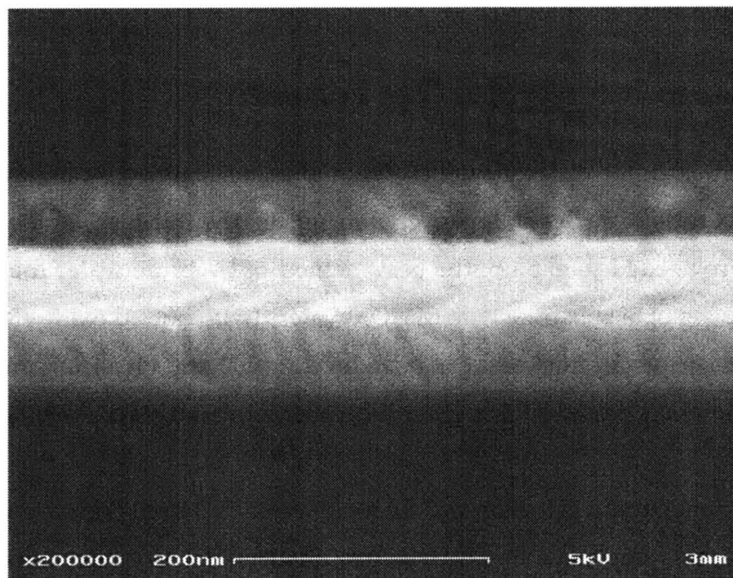


Figure 3-19: Another sample; at 400°C for 30 min and Annealed for 400°C for 30 min; low resolution

Chapter 4

Future Work

4.1 Wafer-to-Wafer Alignment

One future work that needs to be dealt with is the wafer-to-wafer alignment accuracy. As previously stated, the state-of-the-art system has an alignment tolerance of about 1 μm using an infrared system. This aligning tolerance sets a lower limits as to how small the inter-strata via pitch can be. In practice, if SIMOX wafers are used as the processing substrate, inter-strata via formation would not have a high-aspect ratio, thus making them easy to process. Therefore, the real limiting factor in vertical via density appears to be the wafer-to-wafer alignment, and it is a major topic for future work. The goal is to obtain an alignment tolerance of 2 to 3 μ with the existing EV-Aligner in TRL, which has an aligning tolerance of 5 μm specification.

4.2 Wafer Thinning; Inter-wafer Via Formation

As stated above, the maximum inter-wafer via density should be determined by the wafer-to-wafer alignment tolerance. The aspect ratio of each via, however, depends on the thickness of the Si device wafer. In turn, more experiments are needed to explore the best method of backside wafer thinning. Referring to Section 2.2.2, chemical etching of Si substrate with SIMOX wafers (with buried oxide etch stop) seems to be the preferred method, since the wafer thickness can be reduced to 200 nm. Physical grinding of Si substrate is unreliable when Si thickness is below 20 μm, since most wafers already have thickness variations of 20 μm or more.

After wafer thinning, the next task is to etch and fill inter-wafer vias from the backside. Again, depending on the wafer thickness, this step can either be trivial or challenging. Consider a substrate thickness of 20 μm and via width of 2 μm - this suggests that the inter-wafer vias have an aspect ratio of 10:1, which is difficult to achieve without a STS etcher with the Bosch process. Filling of such via with CVD TiN and W, in addition to metal CMP, will also be a challenge.

4.3 Circuit Implementation

The last challenge is to design a 3-D ring oscillator to demonstrate DVI feasibility. Before this, some simple 3-D van der Pauw structures will be built to measure various contact resistances, ie. Cu-to-Cu bump contacts. Once the ring oscillator successfully demonstrates the robustness of DVI technology, the next step would be to integrate heterogeneous structures into a 3-D system. An example of this might be to integrate a memory-logic layer with an optical interconnect network.

Appendix A

Masksets

Our masksets:

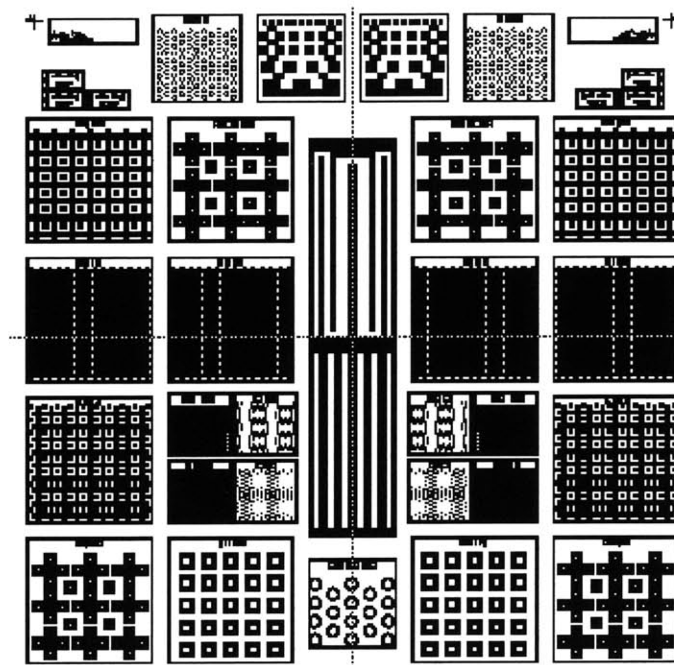


Figure A-1: CPB mask. This mask creates the Cu bumps.

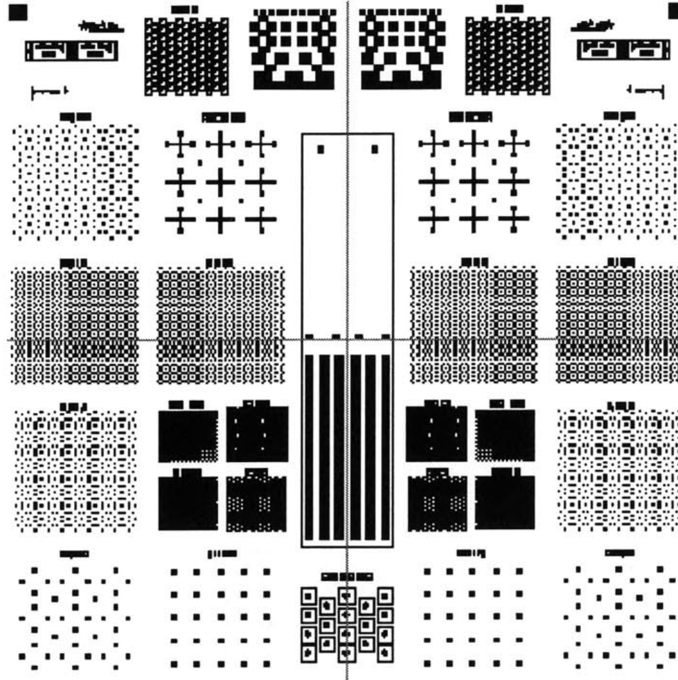


Figure A-2: CD mask. This mask creates the inter-wafer vias.

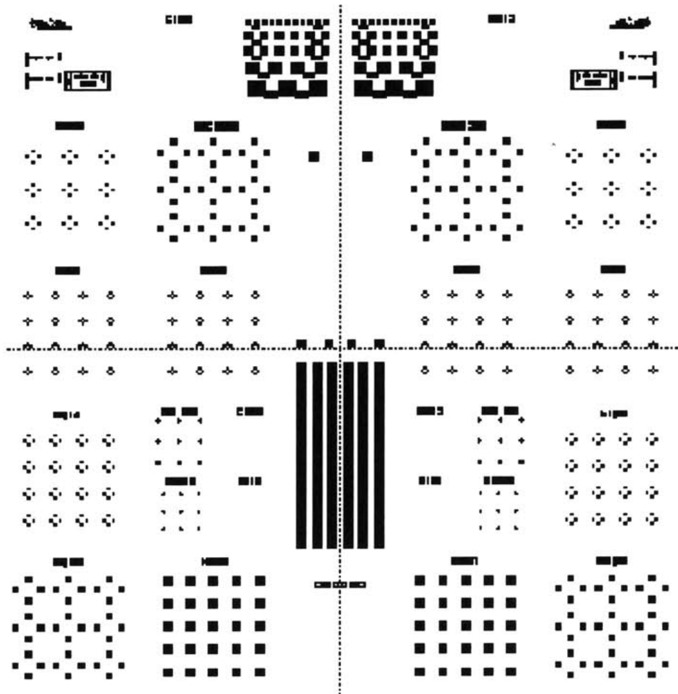


Figure A-3: CP mask. This mask creates the frontside contact holes for Al contact pads.

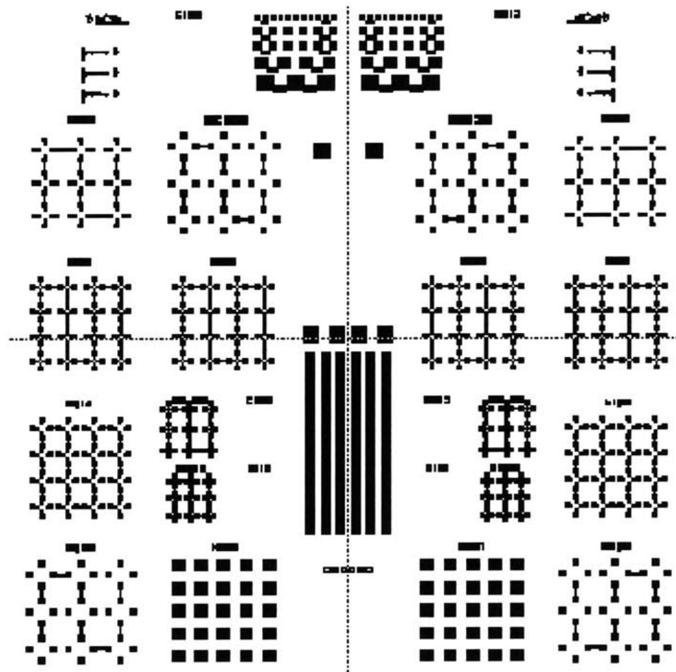


Figure A-4: CCB mask. This mask creates the Al contact pads.

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