AlGaN/GaN-based Power Semiconductor Switches

by

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ABSTRACT

AlGaN/GaN-based high-electron-mobility transistors (HEMTs) have great potential for their use as high efficiency and high speed power semiconductor switches, thanks to their high breakdown electric field, mobility and charge density. The ability to grow these devices on large-diameter Si wafers also reduces device cost and makes them easier for wide market adoption. However, the development of AlGaN/GaN-based power switches has encountered three major obstacles: the limited breakdown voltage of AlGaN/GaN transistors grown on Si substrates; the low performance of normally-off AlGaN/GaN transistors; and the degradation of device performance under high voltage pulsed conditions. This thesis studies these issues and presents new approaches to address these obstacles.

The first part of the thesis studies the breakdown mechanism in AlGaN/GaN-on-Si transistors. A new quantitative model—trap-limited space-charge impact-ionization model—is developed. Based on this model, a set of design rules is proposed to improve the breakdown voltage of AlGaN/GaN-on-Si transistors. New technologies have also been demonstrated to increase the breakdown voltage of AlGaN/GaN-on-Si transistors beyond 1500 V.

The second part of the thesis presents three technologies to improve the performance of normally-off AlGaN/GaN transistors. First, a dual-gate normally-off MISFET achieved high threshold voltage, high current and high breakdown voltage simultaneously by using an integrated cascode structure. Second, a tri-gate AlGaN/GaN MISFET demonstrated the highest current on/off ratio in normally-off GaN transistors with the enhanced electrostatic control from a tri-gate structure. Finally, a new etch-stop barrier structure is designed to address low channel mobility, high interface density and non-uniformity issues associated with the conventional gate recess technology. Using this new structure, normally-off MISFETs demonstrated high uniformity, steep sub-threshold slope and a record channel effective mobility.

The thesis concludes with a new dynamic on-resistance measurement technique. With this method, the hard- and soft-switching characteristics of GaN transistors were measured for the first time.

Thesis Supervisor: Tomás Palacios
Title: Associate Professor of Electrical Engineering

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Table of Content

Chapter 1 Introduction 23

1.1 Power Semiconductor Switches 23

1.2 Design Constrains in Power Semiconductor Switches 24

1.3 The Status of Si Power Switches 27

1.4 Wide Bandgap Semiconductors 28

1.5 Challenges in AlGaN/GaN-based Power Switches 31

1.6 Thesis Outline 33

Chapter 2 Breakdown Mechanism of AlGaN/GaN-on-Si Transistors 35

2.1 Introduction 35

2.2 Low Breakdown Voltage in AlGaN/GaN-on-Si Transistors 36

2.3 Vertical Leakage Mechanism in AlGaN/GaN-on-Si Transistors 39

2.3.1 Vertical I-V and CV Characterization 39

2.3.2 Trap-Limited Space-Charge Model (TLSC Model) 43

2.3.3 Impact Ionization Model 52

2.3.4 Trap-Limited Space-Charge Impact-Ionization Model (TLSCII Model) 56

2.3.5 Vertical Breakdown of AlGaN/GaN-on-Si Structures: Negative Bias Condition. 58

2.3.6 Vertical Breakdown of AlGaN/GaN-on-Si Structures: Positive Bias Condition .. 61

2.3.7 Guideline for the Maximum Breakdown Voltage Design of GaN-on-Si Wafers.. 67

2.4 Schottky-drain Technology 72

2.4.1 Device Fabrication 73

2.4.2 DC Characterization 74

2.5 Si Substrate Removal Technology 76

2.5.1 Device Fabrication 76

2.5.2 Device Characterization 77
2.6 Conclusion 80
Chapter 3 Normally-off GaN Transistors 83
3.1 Introduction 83
3.2 Review of Normally-off GaN Transistor Technologies 84
3.2.1 Fluorine-treatment Technology 85
3.2.2 P-type Semiconductor Gate Technology 85
3.2.3 Surface Potential Engineering Technology 86
3.2.4 Gate-recess Technology 86
3.3 Dual-gate Normally-off GaN Transistors 87
3.3.1 Device Fabrication 89
3.3.2 DC Characterization 90
3.3.3 Characterization of Recessed-gate Channel 92
3.4 Tri-gate Normally-off GaN Transistors 95
3.4.1 Device Fabrication 95
3.4.2 DC Characterization 97
3.4.3 Characterization of Tri-gate Channel Resistance 102
3.5 Impact of Sidewall-gates on Tri-gate AlGaN/GaN Transistors 103
3.5.1 Device Fabrication 103
3.5.2 DC Characterization 104
3.5.3 CV Simulation 107
3.5.4 Tri-gate Channel Mobility 119
3.5.5 Strain Relaxation in Tri-gate Structure 121
3.6 GaN Etch-Stop Barrier Structure 128
3.6.1 Device Fabrication 129

3.6.2 Surface Characterization 130
3.6.3 DC Characterization 132
3.6.4 CV Simulation 136
3.7 Conclusion 142
Chapter 4 Dynamic On-resistance Measurement 145
4.1 Introduction 145
4.2 Dynamic R_{on} Measurement Technique 147
4.3 Dynamic R_{on} Extraction in Soft-switching and Hard-switching Circuits 149
4.3.1 Gate Driver Circuit 150
4.3.2 Dynamic R_{on} in Soft-switching Condition 151
4.3.3 Dynamic R_{on} in Hard-switching Condition 153
4.4 Effect of Soft-switching and Hard-switching on Dynamic R_{on} 155
4.5 Conclusion 157
Chapter 5 Conclusions and Future Work 159
5.1 Conclusions 159
5.2 Future work 160
5.2.1 Improving device breakdown voltage 160
5.2.2 Higher threshold voltage normally-off device 160
5.2.3 Understanding Trapping and Degradation Mechanism in AlGaN/GaN HEMTs 161
Appendix A Elasticity and Piezoelectricity in III-Nitride Semiconductors 163
Appendix B Parameters of III-Nitride Semiconductors for CV Simulations 167
Appendix C Nextnano3 CV Simulation Codes for Tri-Gate and GaN-Etch-Stop Structure Devices 171
Appendix D Matlab Least-Square Fitting Codes for TLSC and TLSCII Models 199

References 209

List of Figures

Figure 1-1. On-off states of an idea power semiconductor switch. 24
Figure 1-2. Illustration of a non-punch-through depletion region in a reverse biased p^+-n-n^+ diode, which the n-layer is fully depleted creating a positively charged space-charge region. Same depletion region can be found in other power semiconductor switches as well. 25
Figure 1-3. Illustration of electric field in super-junction reverse biased p-i-n diode. Same concept applies to the drift-region of a MOSFET. 28
Figure 1-4. Specific on-resistance R_{on}×A as a function breakdown voltage V_{bk} for Si super-junction field-effect transistors (FETs), SiC MOSFETs and GaN AlGaN/GaN high-electron-mobility-transistors (HEMTs) reported in literature. 30
Figure 2-1. Illustration of off-state leakage current in an AlGaN/GaN HEMT 37
Figure 2-2. Buffer breakdown voltage as a function of contact distance measured in an AlGaN/GaN heterostructure grown on Si substrate with total epi-layer thickness of 2 μm. The inset schematic shows the testing device structure with Si substrate at floating potential. The breakdown voltage is defined as the voltage drop between the contacts at 1 mA/mm leakage current. 38
Figure 2-3. Cross-section scanning-electron-microscope (SEM) image of the wafer used in the study and schematics of two samples prepared for the electrical characterization. 39
Figure 2-4. Vertical conductance measurement of the Si(111) substrate obtained by removing the GaN epi-layer. 41
Figure 2-5. 1 kHz CV measurement of the MIS-cap structure on Si(111) substrate. 41
Figure 2-6. Vertical GaN-Si leakage measurement with (a) ohmic-contact sample 1 and (b) Al-Schottky-contact sample 2 at substrate temperature of 10°C, 50°C and 100°C. The top-contact size is 100 μm×50 μm. 42
Figure 2-7. Vertical CV measurements with (a) ohmic top contact and (b) Schottky top contact on GaN-on-Si sample at 15 kHz. The top contact has a circular shape with a diameter of 180 μm. Inset in (a) shows the corresponding vertical I-V characteristics. The schematic shows the measurement setup. 43
Figure 2-8. Schematics of the injected electrons uniformly distributed in the epi-layer at negative bias on the contact in the velocity saturation regime. The injected electrons create a linearly increasing electric field. 45

Figure 2-9. Band diagram illustrates the position of quasi-Fermi-level with respect to shallow and deep traps. 46
Figure 2-10. Schematic of electric field in the TLSC model with different trap density in two regions with $N_{t1} < N_{t2}$. 48
Figure 2-11. Calculated TLSC current in 2 μm GaN layer at 10 °C and 100 °C with three trap levels: E_c-0.55 eV, E_c-0.4 eV and E_c-0.3 eV. All have a density of $2\times10^{16}cm^{-3}$ except the E_c-0.3 eV trap having a density of $3\times10^{16}cm^{-3}$. The results are plotted in linear scale (a) and in log-log scale (b). 49
Figure 2-12. Fitting to the vertical leakage current measured on both ohmic-contact and Schottky-contact samples at negative bias: (a) ohmic-contact sample plotted in linear scale (b) and semilog scale; (c) Schottky-contact sample plotted in linear scale (d) and semilog scale. 51
Figure 2-13. Illustration of impaction ionization initiated by electron current in an impact ionization region of width W. 54
Figure 2-14. (a) Calculated impact ionization multiplication factor M as a function of peak electric field; and (b) corresponding current density as a function of voltage across a 2 μm GaN epi-layer. 55
Figure 2-15. Illustration of the trap-limited space-charge impact-ionization (TLSCII) model with negative bias on the contact with respect to the Si substrate. The impact ionization is initiated by electron injection. 57
Figure 2-16. TLSCII model fitting to the measured vertical leakage current at negative bias conditions on (a) ohmic-contact sample and (b) Schottky-contact sample. (c) Extracted hole current density from the TLSCII model at 10 °C (d) Digital camera picture of luminance from the ohmic-contact sample at bias voltage around -340 V. 60
Figure 2-17. TLSCII model calculation result fitting to the measurement data of Al-Schottky contact sample under positive bias condition. 62
Figure 2-18. Illustration of the electron injection from p-Si substrate at positive bias condition where the electron injection is limited by the generation rate G in the depletion region of the p-type Si substrate. 63

Figure 2-19. CMOS camera image showing the luminance from the edge of an Al-Schottky-contact device biased at about 400 V with respect to the Si substrate measured at room temperature. 65
Figure 2-20. (a) Band diagram of forward biased ohmic contact illustrating the SRH generation at defect states created by the ohmic contact; (b) CMOS camera image of luminance from ohmic-contact metal at 200 V bias; (c) Cross-section scan-electron-microscope (SEM) image of the ohmic contact on GaN used in the study. 66
Figure 2-21. Schematic of a buffer-breakdown test structure on a GaN-on-Si wafer with the source-drain distance L_{sd} much larger than the epi-layer thickness d. 67
Figure 2-22. (a) Calculated avalanche breakdown voltage as a function of total epi-layer thickness on Si substrate with comparison to literature reported data; (b) Average trap density as a function of avalanche breakdown voltage for zero electron injection field from Si substrate ($E_0 = 0$). Increasing E_0 results in a decreased trap density. 72
Figure 2-23. Si substrate potential measurement: (a) schematic of the measurement setup; (b) measured substrate potential as a function of V_{ds} with three leakage current components; (c) voltage distribution among the source, drain and Si substrate 73
Figure 2-24. : I-V characteristics of Schottky-drian contact with and without recess etching on AlGaN. 74
Figure 2-25. (a) Buffer lateral leakage current of the ohmic-drain and Schottky-drain devices with 14 μm contact spacing; The inset shows the leakage current in semi-log scale and the measurement configuration; (b) buffer lateral breakdown voltage as a function of source-to-drain spacing. 75
Figure 2-26. (a) Three-terminal breakdown voltages as a function of gate-to-drain distances; (b) Specific R_{on} as a function of breakdown voltages. The inset picture is the I-V curves of the ohmic-drain and Schottky-drain devices with $L_g = 2$ μm, $L_{gs} = 1.5$ μm and $L_{gd} = 10$ μm. 76
Figure 2-27. Process flow of the substrate transfer technology. (a) Standard AlGaN/GaN HEMTs are fabricated; (b) Device surface is bonded to a Si carrier wafer and Si (111) substrate is removal by SF_6 plasma etching; (c) the N-face surface of the exposed GaN/AlGaN buffer is then bonded to a glass wafer; (d) After releasing the Si carrier wafer, the device is successfully transferred to the glass wafer 77

Figure 2-28. (a) I_d-V_d characteristics of AlGaN/GaN-on-glass after the substrate transfer and of AlGaN/GaN-on-Si before substrate transfer measured in DC bias condition; (b) I_d-V_d characteristics of an AlGaN/GaN-on-glass device measured at DC and 500-μs/200-ms drain pulse conditions at 25 °C and 10 °C. All devices have same dimensions with L_g = 2 μm, L_{gs} = L_{gd} = 1.5 μm. 78
Figure 2-29. Two-terminal buffer breakdown voltage as a function of L_{sd} of devices before and after being transferred to a glass wafer. The data of the device transferred to the glass substrate can be fitted with a power law to the order of 1.5. 79
Figure 2-30. a) Three-terminal leakage current for an AlGaN/GaN HEMT on glass with L_{gd} = 18 μm at V_{gs} = - 8 V. For V_{ds} < 1220 V, the leakage current is below the sensitivity of the measurement setup (1 μA/mm). (b) Three-terminal V_{bk} as a function of L_{gd}. 80
Figure 3-1. Circuit schematic of a D-mode GaN transistor in a cascode configuration with a normally-off transistor. 83
Figure 3-2. Normally-off AlGaN/GaN transistors fabricated by: (a) fluorine-treatment technology, (b) p-type gate technology, (c) surface potential engineering technology, and (d) gate-recess technology. 84
Figure 3-3. Dual-gate normally-off AlGaN/GaN transistor designs in two different gate configurations 88
Figure 3-5. Schematic of integrated dual-gate normally-off transistor and simulation of potential profile at drain voltage of 100 V. 89
Figure 3-6. Cross-section SEM image of the gate recess in the dual-gate normally-off transistor 90
Figure 3-7. (a) I_d-V_{ds} characteristics of an integrated dual-gate E-mode device with L_{gd} = 5 μm; (b) Transfer characteristics of the E-mode device compared to a D-mode device of the same structure without gate recess. The E-mode device is biased at V_{ds} = 12 V and the D-mode device is biased at V_{ds} = 10 V 91
Figure 3-8. Three-terminal breakdown measurement of an E-mode device at V_{gs} = 0 V and a D-mode device at V_{gs} = -8 V and -6.8 V. Both devices have L_{gd} = 8 μm. The current resolution in the measurement setup is 1 μA/mm 91

Figure 3-9. R_{on} as a function of recessed-gate lengths. The extrapolation to zero recessed-gate length gives a resistance of 6.74 ohm-mm, which is the R_{on} (6.76 Ω-mm at V_{gs} = 7 V) of a standard D-mode device with the same dimensions. 93
Figure 3-10. Field-effect mobility μ_{FE} and saturation mobility μ_{sat} of the E-mode dual-gate transistor calculated from g_m-V_d characteristics at V_d = 0.1 V and 12 V. 94
Figure 3-11. Tri-gate device fabrication: (a) PECVD SiO_2 mask deposition and 660 nm tri-gate region pre-definition etching; (b) Interference lithography and subsequent dry etching; (c) 120-nm AlGaN gate-recess region lithography and recess-etching. Atomic-force-microscope (AFM) image shows the profile; (d) gate dielectric deposition and gate metallization. The cross-section scanning-electron-microscope (SEM) images show the dimensions of the tri-gate channel structure which has a period of 300 nm. The top channel width is 90 nm and the sidewall height is 250 nm. (e) Schematic of the Lloyd's mirror interference system used in the fabrication (source: Nano Structures Laboratory Lloyd's mirror interference lithography user manual). 97
Figure 3-12. Comparison of a tri-gate normally-off GaN MISFET with a standard planar-gate D-mode GaN transistor: (a) transfer characteristics at V_{ds} = 1, 3, and 5 V with bi-direction gate sweep; (b) I_d-V_{ds} characteristics. Both devices have L_{gs} = 1.5 μm, L_g = 2 μm, L_{gd} = 10 μm and W = 100 μm 98
Figure 3-13. I_{ds}-V_{gs} characteristics of the tri-gate normally-off MISFET compared with the standard planar-gate transistor and the recessed-gate MISFET with recessed-gate length of 160 nm. All the devices have the same dimensions with L_{gd} = 8 μm and are biased at V_{ds} = 1 V (solid) and 3 V (dashed). 99
Figure 3-14. Three-terminal BV measurement of the tri-gate normally-off GaN MISFET with L_{gd} = 10 μm at V_{gs} = 0 V. 101
Figure 3-15. (a) Specific on-resistance ($R_{on,sp}$) *vs.* breakdown voltage (BV) and (b) leakage current *vs.* BV of the tri-gate normally-off GaN MISFETs and other normally-off GaN devices in the literature with BV measured at V_{gs} = 0 V. 101
Figure 3-16. R_{on} as a function of source-to-drain distance L_{sd} extracted at V_{gs} = 7 V. The R_{on} of normally-off tri-gate devices is on average 1.2-1.8 Ω·mm higher than that of standard planar-gate devices 102
Figure 3-17. Cross-section schematic of the tri-gate channel of the fabricated devices 104

Figure 3-18. Transfer characteristics of a planar-gate transistor (gate length of 10 μm) and tri-gate transistors (tri-gate length of 15 μm) with side-wall height of 70 nm, 120 nm, 200 nm and 350 nm at V_{ds} = 1 V. The current is normalized by the channel width which is 150 nm for every 370 nm width for tri-gate transistors and 100 μm for planar-gate transistor. V_{gs} is stepped from negative to positive direction. 105
Figure 3-19. Quasi-static CV measurement of tri-gate capacitors with side-wall height of 70 nm, 120 nm, 200 nm and 350 nm and planar-gate capacitors. Bias votlage was swept from negative to positive direction. The cross-section schematic of one unit tri-gate structure shows the capacitor components of C_{top}, $C_{side\text{-}wall}$ and C_{bottom}. The capacitance is normalized by the top channel area. 107
Figure 3-20. (a) Net polarization charges and polarization dipole moments in the SiO_2/GaN/$Al_{0.26}Ga0_{.74}N$/GaN structure with AlGaN lattice matched to GaN; (b) Band diagram of the planar-gate device without SiO_2/GaN-cap interface charges and (c) with appropriate positive charge added to the SiO_2/GaN-cap interface. 110
Figure 3-21. Simulated CV characteristics of planar-gate device fitted well with the measurement result. 111
Figure 3-22. Measured and simulated CV curves of 70-nm-sidewall tri-gate device. The different CV simulations compare the impacts of the tri-gate sidewalls, strain relaxation and SiO_2/GaN-cap interface charges on the shift of pinch-off voltage. Open circle is the tri-gate simulation with full strain and the same interface positive fixed charge as in the planar-gate device; Cross and diamond are the results by reducing the piezoelectric charges due to strain relaxation; Filled-circles represent the simulation fitted to the measurement by changing the SiO_2/GaN-cap interface positive charges. Planar-gate CV curve is for comparison purpose. 113
Figure 3-23. Simulated 2D plots of the conduction band edge of the 70-nm-side-wall tri-gate device at gate bias of 0 (a) and -3 V (b) with 1D slices at X = 0 and Y = 50 nm positions. The plot in (c) compares the conduction band energy at y = 50 nm and 20 nm positions in (b). 115
Figure 3-24. Electron density of the 70-nm-side-wall tri-gate device at gate bias of 0.5 V, 0 V and -3 V 117
Figure 3-25. Simulated and measured CV curves of tri-gate devices with side-wall heights of 70 nm, 120 nm, 200 nm and 350 nm. 118

Figure 3-26. Simulated sidewall-gates (one pair) to 2DEG capacitance of each tri-gate structure unit shown in the inset schematic at $V_g = 0$ V. The capacitance is normalized to the tri-gate length direction perpendicular to the cross-section schematic inset. The simulation assumes an ideal side-wall interface without trap states. 119
Figure 3-27. (a) R_{on} as a function of tri-gate length L_{trig}; (b) simulated 2DEG density with planar-device as a reference; (c) calculated effective 2DEG mobility; of the 70-nm-side-wall tri-gate transistors. 121
Figure 3-28. Raman spectrum of the planar AlGaN/GaN-on-Si(111) sample (a) with laser focal point in the GaN channel layer; (b) with the laser focal point in the buffer layer. The dots are the measurement data; the red-solid lines are Lorentzian fitting; the green-colored line is the total fitting curve by two Lorentzians. 123
Figure 3-29. GaN E_2 (high) Raman shifts as a function of tri-gate side-wall heights. Each data point is averaged from 15-20 measurements. 124
Figure 3-30. Schematic of boundary conditions used in the finite-element piezoelectricity simulation. 126
Figure 3-31. Simulated x-axis strain component e_{xx} of the tri-gate structure with different side-wall heights. 126
Figure 3-32. (a) Simulated piezoelectric charge density as a function of tri-gate height at interfaces of GaN-cap/AlGaN and AlGaN/GaN and at the surface of GaN-cap layer; (b) inverse of sheet resistance of tri-gate channel as a function of tri-gate height before deposition of gate dielectric. The dashed line is to guide the eyes. Sheet resistance R_{sh} was measured with halogen lamp light illumination on the devices to reduce the side-wall depletion. Tri-gate height of 0 represents the planar device. 127
Figure 3-33. (a) Band structure and electron density profile of the new wafer structure. (b) Recess depth as a function of etch duration. The depth was measured by atomic force microscope (AFM). Inset shows the relevant dimensions of a recessed-gate GaN MISFET. 129
Figure 3-34. XPS measurement of the sample surface (a) after the 350s BCl3/SF6 dry etching; (b) showing the reduction in F1s signal after O_2 plasma treatment and 1 min TMAH wet etch. 131

Figure 3-35. XPS atomic ratio of Al2p / (Al2p + Ga3d) as a function of TMAH wet-etch time at 70 °C (red circles) and as a function of oxidation / TMAH etch cycles (diamonds). The zero point in x-axis is after 350 s BCl_3/SF_6 dry etching removing the n-GaN layer. A data point (square) also shows the result after 1 cyc of O_2/TMAH followed by 1 cyc of UV-ozone/HCl. 132
Figure 3-36. (a) I_d-V_{gs} characteristics at V_{ds} = 0.1 V with bi-directional gate sweep; (b) I_d-V_{ds} characteristics. The recessed-gate transistor has $L_{rec\text{-}g}$ = 3 μm and L_{gs} = L_{gd} = 4 μm. The planar-gate transistor (dashed line) has the same Lsd with L_g = 8 μm and L_{gs} = L_{gd} = 1.5 μm. 133
Figure 3-37. C-V characteristics of the recessed-gate capacitor measured at 1 kHz (solid line) and 1 MHz (dashed line) with bi-directional sweeps. Inset zooms in the dashed rectangular region. 133
Figure 3-38. (a) R_{on} as function $L_{rec\text{-}g}$ at V_{gs} = 1 to 3 V. The slope of each curve gives R_{ch}. (b) μ_e as a function of N_{sh} of the recessed-gate GaN MISFET extracted from DC/CV measurements and gated-Hall measurement..... 135
Figure 3-39. Three-terminal BV measurement of the recessed-gate normally-off GaN MISFET with $L_{rec\text{-}g}$ = 3 μm, L_{gd} = 13 μm at V_{gs} = 0 V..... 136
Figure 3-40. Simulated low-frequency (LF) and high-frequency (HF) CV characteristics match with measured 1kHz and 1MHz CV curves. Inset zooms in the dashed rectangle region, showing the dispersion caused by interface states..... 138
Figure 3-41. Al_2O_3/AlN interface trap density (D_{it}) *vs.* energy level relative to conduction band edge of AlN (E_c-E_{trap}). The inset shows the location of the traps in the band structure of the device at zero bias voltage. 139
Figure 3-42. Simulated band diagram and electron density at V_{gs} = 0, 1, 2 and 3 V..... 140
Figure 3-43. Simulated sheet electron density inside GaN and $Al_{0.15}Ga_{0.85}N$ with measured sheet electron density from 1 MHz CV and gated-Hall measurements..... 141
Figure 3-44. Band diagram at flat-band condition showing the electric field (E-field) direction in Al_2O_3..... 142
Figure 4-1. Illustration of current collapse and increase of dynamic on-resistance R_{on} when an AlGaN/GaN HEMT is switched-on from high voltage off-state to on-state. 145

Figure 4-2. Illustration of charge trapped on the surface and in buffer of an AlGaN/GaN HEMT. 146
Figure 4-3. Illustration of the current-voltage trace during the turn-on transition of a power transistor in hard-switching and soft-switching circuits. The turn-off transition is time reverse of the trace 146
Figure 4-4. (a) Voltage clamping circuit for V_{dson} measurement; (b) measured voltages from the voltage clamping circuit. 149
Figure 4-5. Gate drive circuit diagram 150
Figure 4-6. Gate drive output waveform at 5 V. 151
Figure 4-7. Soft switching circuit diagram. 152
Figure 4-8. Soft-switching waveforms of GaN transistor (a) V_g and V_{ds} (b) V_{dson} and I_1+I_2 waveforms. 152
Figure 4-9. Normalized dynamic R_{on} of the GaN transistor and Si MOSFET in soft-switching condition at 2 μs after the peak V_{ds} stress. 153
Figure 4-10. Hard-switching circuit diagram 154
Figure 4-11. GaN transistor hard switching V_{ds}, I_d waveforms in (a) turn-on transient and (b) turn-off transient at 150 V V_{ds} stress. The V_{ds} rises to 150 V in (b) with a RC time constant of 40 μs of the input filter 154
Figure 4-12. Normalized dynamic R_{on} of the hard-switched GaN transistor and Si MOSFET at 2 μs and 10 μs after the devices were switched on. 155
Figure 4-13. (a) ΔR_{on} of GaN transistors measured at 2 μs after the off-state peak V_{ds} in hard- and soft- conditions; (b) turn-on transient V_{ds}-I_d traces from off-state voltage of 180 V. 156
Figure 4-14. (a) circuit diagram of the connection of 10 nF capacitor; (b) increase of dynamic R_{on} measured at 2 μs after the peak V_{ds}; (c) I_d-V_{ds} traces of the hard-switching GaN transistor with 10 nF external capacitor during turn-on transient 157
Figure B-1. Comparison between nonlinear and linear polarization calculations. 168

List of Tables

Table 1-1. Comparison of wide-band-gap semiconductors with Si [Sze&Ng]. 29
Table 2-1. Extracted V_0 and effective Nt at different trap levels by least-square fitting to the vertical leakage measurement data of the negative biased ohmic-contact and Schottky-contact samples using the TLSC model. 52
Table 2-2. Extracted effective Nt at different trap levels by least-square fitting to the vertical leakage measurement data of the negative biased ohmic-contact and Schottky-contact samples using the TLSCII model. Dash means the corresponding E_t is not used in the fitting. 59
Table 3-1. Channel resistance R_{ch} (Ω/sq), charge density Q_{ch} ($\times 10^{12}$ cm^{-2}) and electron mobility μ_e ($cm^2V^{-1}s^{-1}$) as a function of V_{gs} (V) extracted from DC/CV measurements and gated-Hall measurement. R_{ch} is too large at V_{gs} = 1 V to give a reliable Hall measurement. 134
Table 4-1. Comparison of datasheet value of IRF620 and EPC1012. 150
Table A-1 Elastic constants (GPa) [Wright1997] 164
Table A-2 Spontanious polarization (C/m^2) and piezoelectric coeffeicients (C/m^2) 166

Chapter 1 Introduction

1.1 Power Semiconductor Switches

Power semiconductor switches are a type of semiconductor devices which control the flow of current in power electronics circuits for the conversion of electric power. Some of the applications where these switches are useful include High-Voltage-Direct-Current (HVDC) transmission systems, motor control systems, renewable energy generation systems, battery management systems, and consumer electronics, where electric power is converted between different voltages, current forms or frequencies.

Power semiconductor switches operate primarily in two states as shown in Figure 1-1. In the on-state, an ideal switch conducts current without any voltage drop. In the off-state, it holds off the voltage without any current conduction.

There are three types of power switches: diodes, thyristors and transistors. Diodes are two terminal p-n junction devices widely used in many power electronics circuits such as in the rectifier circuits for the conversion of alternating current (AC) into direct current (DC). Thyristors are three-terminal devices with multiple stacked p-n junctions. With very high voltage blocking and high current conduction capabilities, they find applications in most of the high power systems (mega-watts) such as the HVDC transmission systems. Finally, transistors are one of the most common three-terminal devices. Based on the type of carriers involved in current conduction, transistors are divided into two types. The first type is the unipolar transistor, in which only one type of carriers (electrons or holes) conducts the current. Examples are field-effect transistors (FETs), such as the metal-oxide-field-effect transistors (MOSFETs) and junction-field-effect transistors (JFETs). The second type is the bipolar transistor, in which both types of carriers are involved in current conduction. An example is the bipolar-junction transistor (BJT).[1] There is also a special type of bipolar transistor, which combines an FET with a BJT, the insulated-gate-bipolar-transistor (IGBT).

[1] Similar categorization also applies to diodes. For example, Schottky-diodes are unipolar devices while the p-n diodes are bipolar devices.

In low voltage (less than 1 kV) to medium voltage (1 kV to about 50 kV) applications, power MOSFETs and IGBTs are the predominant power switching devices due to their good turn-on/off capabilities and the high impedance of their insulating gate.

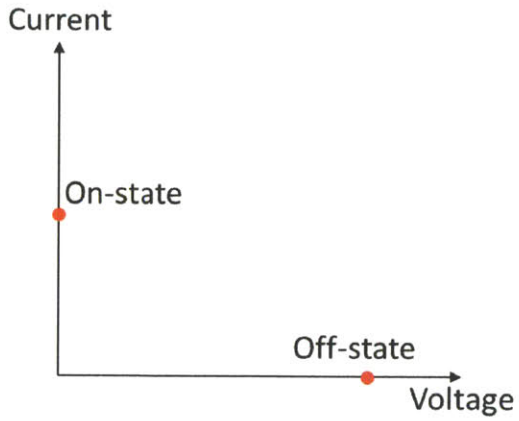

Figure 1-1. On-off states of an idea power semiconductor switch.

1.2 Design Constrains in Power Semiconductor Switches

All the power semiconductor switches mentioned above have a lightly doped region for blocking the off-state voltage. For example, in a p^+-n-n^+ diode shown in Figure 1-2, depletion occurs in the lightly doped n-layer in the off-state reverse-bias condition. For an abrupt junction, the electric field in the depletion region increases linearly. The reverse bias blocking voltage V_B and the maximum electric field E_{max} satisfy:

$$V_B = \frac{E_{max}W}{2} = \frac{qN_dW_D^2}{2\epsilon_s} \tag{1-1}$$

$$E_{max} = \frac{qN_dW_D}{\epsilon_s} \tag{1-2}$$

where N_d is the doping density in the n-region, W_D is the depletion width (less than the n-layer thickness) and ϵ_s is the dielectric constant of the semiconductor material.

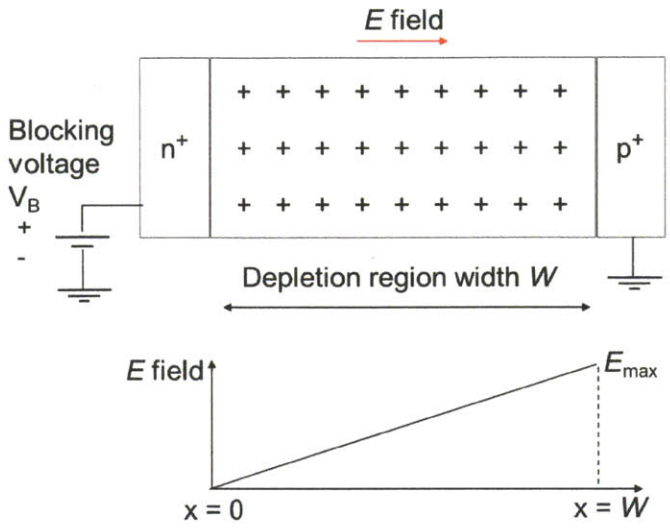

Figure 1-2. Illustration of a non-punch-through depletion region in a reverse biased p^+-n-n^+ diode, which the n-layer is fully depleted creating a positively charged space-charge region. Same depletion region can be found in other power semiconductor switches as well.

When the E_{max} reaches the critical electric field E_{cr} (also called breakdown electric field) of the semiconductor material, significant carrier generation occurs in the depletion region due to impact ionization and the semiconductor switch undergoes avalanche breakdown (see Chapter 2). The blocking voltage V_B defined at the avalance breakdown condition is the breakdown voltage of the device.

When the depletion region extends into the n^+-layer (the punch-through condition), breakdown voltage of the device will be smaller than the non-punch-through condition as shown in Figure 1-2, where the depletion region is confined in the lightly doped n-layer[2]. Here we consider the optimal condition when the n-layer thickness W is equal to the maximum depletion width at avalanche breakdown. Replacing E_{max} with E_{cr} in equation (1-1) and (1-2), we have

[2] The detailed analysis of the punch-through condition can be found in reference [Sze&Ng].

$$V_{bk} = \frac{E_{cr}\mathrm{W}}{2} \tag{1-3}$$

$$E_{cr} = \frac{qN_d\mathrm{W}}{\epsilon_s} \tag{1-4}$$

Where V_{bk} is the breakdown voltage[3], N_d is the doping concentration in the lightly doped n-region and W is the n-region thickness.

Rearranging equation (1-3) and (1-4) gives

$$W = \frac{2V_{bk}}{E_{cr}} \tag{1-5}$$

$$N_d = \frac{\epsilon_s E_{cr}^2}{2qV_{bk}} \tag{1-6}$$

For a certain voltage application, W and N_d can be determined from the above equations. The resistance per unit area of the lightly doped n-layer can be calculated by

$$R = \frac{W}{q\mu N_d} = \frac{4V_{bk}^2}{\epsilon_s \mu E_{cr}^3} \tag{1-7}$$

where μ is the carrier (electron in this example) mobility.

In unipolar power switches such as power MOSFETs and Schottky diodes, the resistance in this region contributes a significant portion of the total resistance, which limits their applications to mainly low voltage systems.

In bipolar power switches such as p^+-n-n^+ diodes, thyristors and IGBTs, the resistance in the voltage blocking region is reduced by minority carrier injection so that they can carry a large current [Sze&Ng]. As a result, these devices are suitable for high voltage and high current applications. However, due to the injected minority carriers, these devices cannot return back to the high-impedance off-state immediately until the minority carriers disappear

[3] This is the upper limit of breakdown voltage in a power semiconductor switch. Depending on device geometry, premature breakdown due to electric field crowding (edge effect [Sze&Ng]) before the maximum breakdown voltage is reached.

in the voltage blocking region. This delay time is called reverse recovery time which limits the switching speed of these devices.

As a result, for a given semiconductor material, low voltage switches have faster switching speed than high voltage switches. It should be mentioned that this trend is also observed within the same category of power switches. For example, in power MOSFETs, the resistance in the voltage blocking region increases with the square of its breakdown voltage according to equation (1-7). In order to compensate the increase of resistance, larger device area is used, which results in a larger device capacitance. The larger capacitance in turn reduces the switching speed[4]. As we will see later, a good figure-of-merit to characterize the device performance is the product of its on-resistance R_{on} with its area A: $R_{on} \times A$. It is called specific on-resistance.

1.3 The Status of Si Power Switches

The semiconductor industry is dominantly built upon the single crystalline Si, which solely consists of the second most abundant element in the Earth's crust, Si (in the natural form of SiO_2). With the Si fabrication technology being the most advanced semiconductor technology, most of the electronic devices produced today are fabricated on Si wafers, so are the power semiconductor switches.

As shown in section 1.1, the switching speed of power semiconductor switches decreases as their breakdown voltage increases. This trend has a great significance in power electronics circuits. For example, the size of the energy storage components (e.g. inductors and capacitors) in a power electronics circuit scales inversely proportional with its operating frequency. The slow switching speed of power semiconductor switches results in bulky power electronics circuits especially in high voltage applications. Furthermore, higher switching frequencies also improve the transient response and stability of DC-DC power converters [Lehman1996]. These limitations of Si power switches, determined by its intrinsic properties such as E_{cr} and μ, constitute an important bottleneck for power electronics circuits.

---

[4] With larger device capacitance, the switching loss of the device is increased if the switching frequency is kept the same. To maintain efficiency, the switching frequency is lowered to reduce the switching loss.

One way to improve the performance of Si power switches is to extend the use of the unipolar devices—power MOSFETs—to higher power applications, as their unipolar behavior allows for higher switching speeds. For this purpose, a super-junction (SJ) technology has been proposed [Deboy1998]. The basic concept of the super-junction technology is to change the electric profile in the device voltage blocking region by introducing narrow stripes of p-type regions to precisely match the stripes of n-type doping density. As shown in Figure 1-3, when the voltage blocking region is depleted, the space-charges in these stripes cancel each other and the electric field becomes uniform. The limitation on the doping density in equation (1-6) no longer applies. As a result, much higher doping density can be used to reduce the resistance of the voltage blocking region. However, the fabrication of these long stripes with very precise doping concentration is very challenging, especially for high voltage devices. As a result, the currently reported Si SJ-MOSFETs are expensive and their applications are limited to voltages below 1000 V [Deboy1998, Onishi2002, Rub2004, Sakakibara2008]. An alternative approach is to use new materials with intrinsically better characteristics than Si.

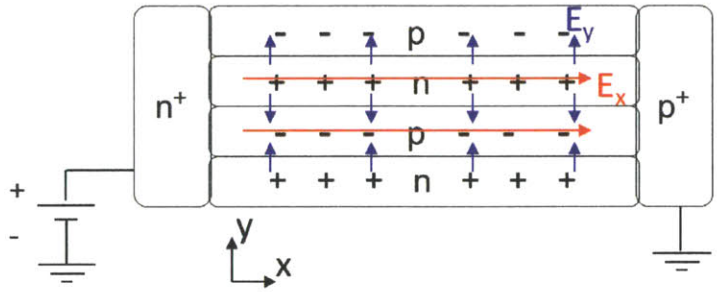

Figure 1-3. Illustration of electric field in super-junction reverse biased p-i-n diode. Same concept applies to the drift-region of a MOSFET.

1.4 Wide Bandgap Semiconductors

Wide bandgap semiconductors with higher critical electric field than Si can fundamentally improve the performance of power semiconductor switches. As shown in

Table 1-1, SiC and GaN have about 10× higher critical electric field than Si. They are great candidates for higher performance power switches.[5]

Table 1-1. Comparison of wide-band-gap semiconductors with Si [Sze&Ng].

Property	Si	4H-SiC	Wurtzite GaN
Bandgap (eV)	1.12	3.2	3.4
Dielectric constant	11.9	10	10.4
Critical electric field (MV/cm)[ǂ]	~0.3	~4	~4
Electron mobility ($cm^2V^{-1}s^{-1}$)	1350[a]	800[b]	850[c], ~1100[d]
Thermal conductivity ($Wcm^{-1}{}^oC^{-1}$)	1.5	4.9	1.7

ǂ Actual value depends on electric field profile.

a. Room temperature low field mobility of bulk n-type Si with doping concentration of about 10^{14} cm^{-3}. It varies between about 200 and 1350 $cm^2V^{-1}s^{-1}$ for doping concentration between 10^{14} and 10^{18} cm^{-3}[Sze&Ng].

b. Room temperature low field mobility of bulk n-type 4H-SiC at doping concentration of 10^{16} cm^{-3}. It varies between 200 and 950 $cm^2V^{-1}s^{-1}$ for doping concentration between 10^{15} and 10^{18} cm^{-3} [Roschke2001].

c. Room temperature low field mobility of bulk wurtzite n-type GaN at impurity concentration of 10^{17} cm^{-3}. It varies between 500 and 1150 $cm^2V^{-1}s^{-1}$ for impurity concentration between 10^{16} and 10^{18} cm^{-3} [Albrecht1998].

d. Room temperature peak effective mobility of two-dimensional-electron-gas (2DEG) in AlGaN/GaN heterostructure [Dang1999, Lu2013]. It varies between 800 and 1100 $cm^2V^{-1}s^{-1}$ for 2DEG density between 3×10^{12} and 10^{13} cm^{-2}. It also varies with Al percentage in AlGaN due to alloy scattering.

The advantage of these wide bandgap semiconductors in power electronics can be highlighted by plotting the specific on-resistance, R_{on}×A as a function of breakdown voltage of the power switches, where R_{on} is the device on-state resistance and A is its area (Figure 1-4). As discussed in Section 1.1, for high voltage unipolar devices such MOSFETs and JFETs, R_{on} is dominated by its voltage blocking region (the drift-region) resistance. Therefore, we can use equation (1-7) to calculate the specific on-resistance:[6]

$$R_{on} \times A = \frac{4V_{bk}^2}{\epsilon_s \mu E_{cr}^3}$$

[5] GaN-based devices also benefit from the high electron mobility in AlGaN/GaN heterostructure.

[6] This equation assumes ideal electric field distribution in the depletion region as shown in Figure 1-2. It does not apply to lateral device geometry where electric field concentrates at junction edges (edge effect [Sze&Ng]). However, R_{on}×A can still be used to bench mark device performance.

As shown in Figure 1-4, the wide-band-gap semiconductor devices have three orders of magnitude lower specific on-resistance than the Si unipolar devices. As a result, low loss and high speed power devices can be made from these materials.

Another advantage of wide-band-gap semiconductors is their ability to operation at high temperatures due to very small intrinsic carrier concentration. For example, at 500 °C, both GaN and SiC have an intrinsic carrier density below 10^{10} cm^{-3}.

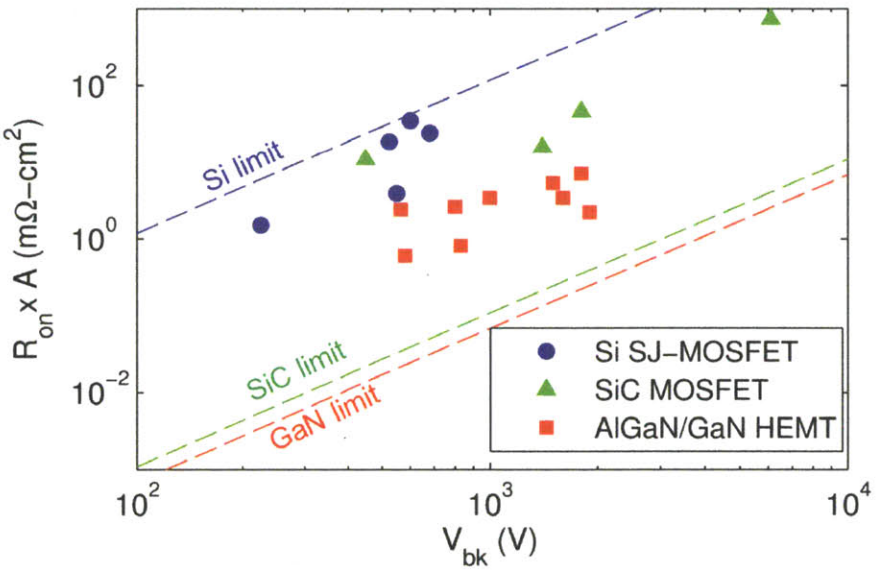

Figure 1-4. Specific on-resistance R_{on}×A as a function breakdown voltage V_{bk} for Si super-junction field-effect transistors (FETs), SiC MOSFETs and GaN AlGaN/GaN high-electron-mobility-transistors (HEMTs) reported in literature.

The development of SiC power MOSFETs started in the 1980s [Palmour1987]. Since then, kilovolts-class SiC MOSFETs were demonstrated with lower specific R_{on} than the Si MOSFET limit line as shown in Figure 1-4 [Cooper2002]. However, the device performance is severely limited by the poor channel effective mobility (10~150 $cm^2V^{-1}s^{-1}$), high density of trap states at the MOS interface, and gate oxide reliability issues [Cooper2002, Treu2007, Olafsson2004]. The high wafer cost, limited wafer size and incompatibility with Si fabrication technology due to the extremely high process temperature (>1600 °C for implantation activation) also hinders their wide applications.

On the other hand, III-Nitride semiconductors are unique in their strong polarization properties and the ability to form heterostructures. For example, due to the large spontaneous and piezoelectric charges and the conduction band offset in the AlGaN/GaN heterostructure, a polarization-induced high density ($n_e \sim 10^{13} cm^{-2}$) two-dimensional-electron-gas (2DEG) is confined at the AlGaN/GaN interface with electron Hall mobility in excess of 1200 $cm^2V^{-1}s^{-1}$ [Ambacher2000]. Thanks to the combination of large critical electric field, high charge density and high channel mobility, the high-electron-mobility transistors (HEMTs) fabricated on the AlGaN/GaN heterostructure have a great potential for high performance power switches.

Great advancement in AlGaN/GaN high voltage HEMTs has been achieved in the last decade. In 2001, the first 1 kV AlGaN/GaN HEMT grown on SiC substrate was reported [Zhang2001] with $R_{on} \times A$ of only 3.4 $m\Omega \cdot cm^2$. In 2006, 1.6 kV breakdown voltage was reported in an AlGaN/GaN HEMT grown on sapphire substrate [Tipirneni2006]. In the same year, the breakdown voltage of the AlGaN/GaN HEMT grown on SiC has reached up to 1.9 kV with $R_{on} \times A$ as low as 2.2 $m\Omega \cdot cm^2$ [Dora2006]. As shown in Figure 1-4, these early results have already demonstrated 10-100 times lower specific R_{on} than the Si limit.

Another advantage of the III-Nitride semiconductors is the ability to grow them on large area Si wafers, which enables the cost reduction in the Nitride-based devices. Since the demonstration of AlGaN/GaN HEMTs on Si(111) wafers with 100 mm diameter in 2002 [Brown2002], substantial progress has been achieved in this area. 6-inch GaN on Si wafers are now commercially available from a number of vendors. Recently the growth of AlGaN/GaN HEMT structure on a 200 mm diameter Si(111) substrate was also demonstrated [Cheng2012].

1.5 Challenges in AlGaN/GaN-based Power Switches

Despite the encouraging initial results, the development of AlGaN/GaN high voltage power switches has been hindered by three major obstacles.

First, the AlGaN/GaN-based power switches fabricated on Si substrates have lower breakdown voltages than their counterpart grown on SiC and sapphire substrates. Although the origin of this lower breakdown voltage is not clear, the traditional method to increase it is

to grow thick epitaxial layers of III-Nitride semiconductors [Ikeda2008, Selvaraj2009, Vasalli2009]. However, this technique increases the wafer cost and typically introduces large wafer bow in the wafers due to the significant thermal mismatch between GaN and the Si substrate. To overcome this technology barrier, it is necessary to understand the breakdown mechanism of the AlGaN/GaN HEMTs on Si substrates which can inspire innovations in wafer design.

Second, enhancement-mode (E-mode) or normally-off transistors are needed to be compatible with existing power electronics circuits. However, the standard AlGaN/GaN HEMTs are depletion-mode (D-mode) devices due to the existence of the polarization induced 2DEG. The current solution to make E-mode GaN transistors is cascoding an E-mode Si MOSFET with a D-mode AlGaN/GaN HEMT. However, this not only increases the device cost but also limits the device switching speed due to the Miller effect and the maximum operation temperature. A number of technologies have been proposed for fabricating normally-off GaN transistors, including n-channel GaN MOSFET [Irokawa2004, Huang2006], plasma treatment on the AlGaN layer of a AlGaN/GaN HEMT [Cai2005], p-type semiconductor gate on AlGaN/GaN structure [Uemoto2007], changing the surface potential of a AlGaN/GaN HEMT with dielectrics [Ohmaki06, Higashiwaki07, Medjdoub10], and recess-etching of the AlGaN layer of a AlGaN/GaN HEMT [Oka2008, Kanamura2010]. However, these methods either severely degrade the electron mobility in the AlGaN/GaN heterostructure or produce very limited threshold voltage (less than 1 V while $V_t > 2$ V is usually required for safety concerns of power electronics circuits) and gate bias range. Furthermore, these E-mode AlGaN/GaN-based transistors also surfer from high off-state leakage current [Lu2012]. Technology innovations are needed to overcome the limitations of these methods.

Last but not the least, it is observed that the performance of AlGaN/GaN HEMTs degrades under different switching conditions: when they are switched from high voltage off-state to on-state, the maximum current desnity becomes lower and on-resistance becomes higher than that measured under low voltage DC conditions [Binari2001]. The cause of the instability in device performance is generally believed to be the electron trapping in AlGaN/GaN HEMTs at locations below the channel region and on the surface of the AlGaN barrier [Klein2001, Rudzinski2006, Binari2001, Vetury2001, Koley2003]. The device

characteristics also degrade overtime under high voltage situations [Verzellesi2005], for which hot-electron effect [Meneghesso2008], inverse-piezoelectric effect [Joh2006] and electrochemical reactions at the surface [Gao2011, Gao2012] have been proposed as the mechanisms. Unless these problems are fully understood and resolved, the potential of AlGaN/GaN HEMTs cannot be fully exploited.

1.6 Thesis Outline

This thesis aims to understand and overcome the challenges outlined above by developing novel theoretical models, transistor structure designs and measurement techniques. The remainder of this thesis is organized as follows:

Chapter 2 elucidates the breakdown mechanism in GaN-on-Si devices. A new theory is developed and technologies for improving GaN-on-Si device breakdown voltage are presented.

Chapter 3 describes the device design, fabrication and measurement results of three novel transistor structures to achieve normally-off operation. Device physics of each structure is also quantitatively analyzed with numerical simulation.

Chapter 4 presents a new measurement technique for extracting the dynamic on-resistance of transistors and the measurement results of commercial GaN power transistors under soft- and hard-switching conditions.

Chapter 5 concludes the thesis and presents some future work.

Chapter 2 Breakdown Mechanism of AlGaN/GaN-on-Si Transistors

This chapter elucidates the breakdown mechanism in AlGaN/GaN-on-Si transistors. A new model—trap-limited space-charge impact-ionization model—is developed. Theoretical calculations of vertical leakage current and breakdown voltage using this new model show good agreement with measurement data. Technologies for improving the breakdown voltage of AlGaN/GaN-on-Si transistors are also presented.

2.1 Introduction

Silicon is the most attractive substrate for the growth of III-Nitride semiconductors due to its low cost, large wafer size and relatively high thermal conductivity. However, the growth of large area Nitride-semiconductors on Si substrate using metal-organic chemical vapor deposition (MOCVD) is very challenging because of the large lattice and thermal mismatches between GaN and Si, which cause a high density of dislocations, high stress and even cracks in the GaN epitaxial film. To overcome these challenges, a number of growth techniques have been developed over the last decade, such as the use of super-lattice buffer, graded AlGaN buffer and patterned Si substrate to control the stress of the epitaxial film [Feltin2001, Raghavan2005, Strittmatter2001]. Since the early demonstration of AlGaN/GaN high-electron-mobility transistors (HEMTs) on 100-mm-diameter Si(111) substrate in 2002 [Brown2002], substantial progress has been made. 6-inch AlGaN/GaN-on-Si wafers are now commercially available. AlGaN/GaN heterostructure was also recently demonstrated on 200-mm-diameter Si wafers [Cheng2012].

As the MOCVD growth technology becomes mature, the electrical performance of theses AlGaN/GaN-on-Si wafers needs to be investigated, especially for high voltage switching devices. Si substrates, in contrast to the sapphire and semi-insulating SiC substrates commonly used for GaN growth before large-area AlGaN/GaN-on-Si wafers became available, has lower band gap and higher conductivity. As a result, the breakdown voltage of AlGaN/GaN transistors grown on Si is lower [Lu2010Sep2]. The limited breakdown voltage has been one of the most important problems in AlGaN/GaN-on-Si power switches. The

focus of this chapter is to understand the breakdown mechanism in AlGaN/GaN-on-Si transistors and develop methods to increase their breakdown voltages. Section 2.2 introduces the breakdown voltage problem in AlGaN/GaN-on-Si devices. Section 2.3 describes the experimental results and the theoretical modeling of the breakdown voltage measured under various bias conditions. Section 2.4 and 2.5 describe two technologies that improve the breakdown voltage in AlGaN/GaN transistors grown on Si substrates. Finally, Section 2.6 concludes the chapter.

2.2 Low Breakdown Voltage in AlGaN/GaN-on-Si Transistors

Early development of high voltage GaN transistors focused on AlGaN/GaN high-electron-mobility transistors (HEMTs) grown on semi-insulating SiC and insulating sapphire substrates and very high voltage transistors were demonstrated. In 2001, the first 1 kV AlGaN/GaN HEMT grown on semi-insulating SiC substrate was reported [Zhang2001] with $R_{on} \times A$ [7] of only 3.4 $m\Omega \cdot cm^2$. In 2006, 1.6 kV breakdown voltage with $R_{on} \times A$ of 3.4 $m\Omega \cdot cm^2$ was reported in an AlGaN/GaN HEMT grown on sapphire substrate [Tipirneni2006]. In the same year, the breakdown voltage of the AlGaN/GaN HEMT grown on SiC reached up to 1.9 kV with $R_{on} \times A$ as low as 2.2 $m\Omega \cdot cm^2$ [Dora2006].

In contrast, the development of high voltage AlGaN/GaN HEMTs on Si substrate has been hindered by the relatively low breakdown voltage in these devices. For example, AlGaN/GaN HEMTs grown on Si with 2-μm-thick epi-layer typically have breakdown voltages less than 700 V [Lu2010Apr, Selvaraj2009, Ikeda2008], which is much lower than the 1.9kV breakdown voltage in the AlGaN/GaN HEMTs on semi-insulating SiC with the same epi-layer thickness [Dora2006].

The off-state leakage paths in an AlGaN/GaN-on-Si HEMT are illustrated in Figure 2-1. The drain-to-gate leakage can cause premature breakdown in these devices due to high concentration of electric field at the gate edge. With the help of field-plate structures, the electric field strength at the gate edge is reduced and the premature breakdown voltage

[7] The product of on-resistance and device area, $R_{on} \times A$, is a measure of power switch performance. The lower the product, the better is the performance. For details, see Section 1.2.

caused by the gate leakage is improved [Zhang2000, Saito2003, Xing2004]. The field-plate technology was widely used in AlGaN/GaN HEMTs on insulating substrate (e.g. SiC and Sapphire) and can be readily applied to AlGaN/GaN HEMTs on Si substrate.

While the gate leakage is device structure dependent, the vertical and lateral leakages in the AlGaN/GaN HEMTs on Si substrate are determined by the epitaxial structure. To evaluate the leakage current within the epitaxial structure, buffer breakdown measurements are commonly used. As shown in Figure 2-2 inset, the buffer breakdown voltage of an AlGaN/GaN-on-Si wafer is typically measured between two isolated contact terminals when the leakage current reaches a defined value (e.g. 1 mA/mm).

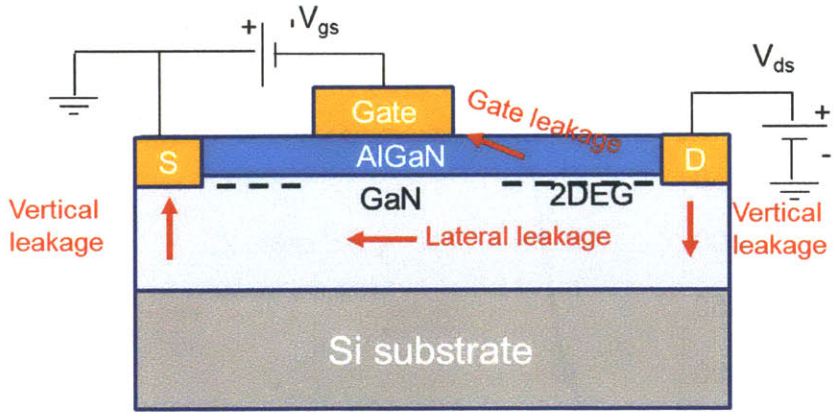

Figure 2-1. Illustration of off-state leakage current in an AlGaN/GaN HEMT.

Figure 2-2 shows an example of measured buffer breakdown voltage as a function of the contact distance for an AlGaN/GaN heterostructure grown on Si substrate. The breakdown voltage first increases with the contact distance. This is due to the increase of the lateral resistance in the GaN epitaxial layer (epi-layer) between the two contacts at larger distance. For the same lateral leakage current, more voltage is dropped laterally.

When the distance between the two contacts is larger than 12 μm, the buffer breakdown voltage reaches a plateau and remains constant even when the contact separation increases to 35 μm. The saturation of buffer breakdown voltage indicates that there is a parasitic leakage path which shorts the lateral resistance of the GaN epi-layer. It turns out that the parasitic

leakage path is in the Si substrate. When the contact distance is large enough (larger than 12 μm in the case shown in Figure 2-2), current flows vertically to the Si substrate from the contact at high voltage, across the distance between the contacts through the Si and then vertically back to the other contact at ground potential. Since the Si substrate is very thick and has much higher conductivity than the GaN epi-layer, the lateral voltage drop in Si can be ignored. In fact, it has been demonstrated (see section 2.5) that after removing the Si substrate, buffer breakdown voltage no longer saturates [Lu2010Sep2, Srivastava2010]. As a result, the vertical leakage determines the maximum breakdown voltage in an AlGaN/GaN transistor on Si substrate. Therefore it is very important to understand the vertical leakage mechanism, which can promote new designs to overcome the limitation of breakdown voltage in these devices.

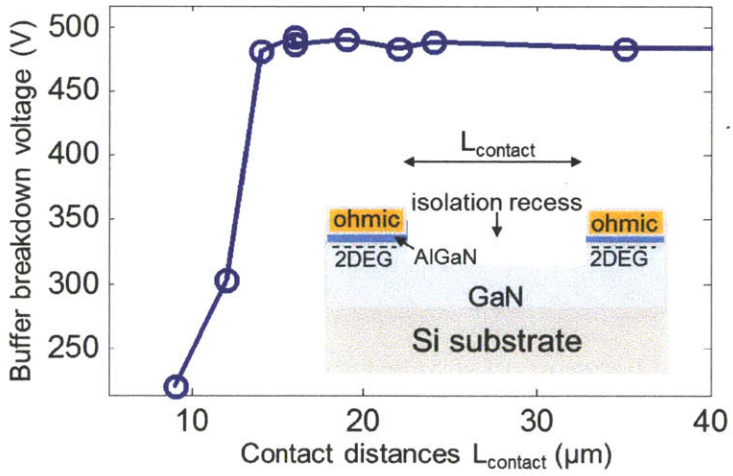

Figure 2-2. Buffer breakdown voltage as a function of contact distance measured in an AlGaN/GaN heterostructure grown on Si substrate with total epi-layer thickness of 2 μm. The inset schematic shows the testing device structure with Si substrate at floating potential. The breakdown voltage is defined as the voltage drop between the contacts at 1 mA/mm leakage current.

2.3 Vertical Leakage Mechanism in AlGaN/GaN-on-Si Transistors

In order to understand the vertical leakage mechanism, vertical current-voltage (I-V) and capacitance-voltage (CV) measurements on AlGaN/GaN-on-Si wafers are conducted. A new model—trap-limited space-charge impact-ionization model—is developed and shows good agreement with the experimental results. Based on the new model, a breakdown voltage design guideline is provided for AlGaN/GaN-on-Si devices.

2.3.1 Vertical I-V and CV Characterization

- **Device Fabrication**

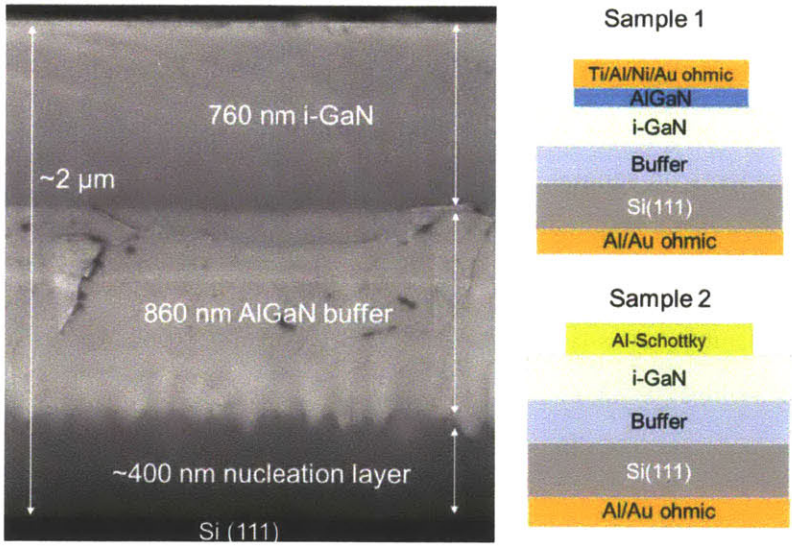

Figure 2-3. Cross-section scanning-electron-microscope (SEM) image of the wafer used in the study and schematics of two samples prepared for the electrical characterization.

The AlGaN/GaN-on-Si wafer used in this study has a 18 nm $Al_{0.26}Ga_{0.74}N$ barrier, ~0.76 μm undoped GaN layer, ~0.86 μm graded AlGaN buffer and ~0.4 μm nucleation layer on a 4-inch 500-μm-thick Si(111) substrate. The total epi-layer thickness is 2±0.1 μm measured from the cross-section scan-electron-microscope (SEM) image in Figure 2-3. Two samples were prepared. Sample 1 has standard Ti/Al/Ni/Au alloyed ohmic contacts formed on the

AlGaN layer surface followed by mesa-isolation etching to remove the 2DEG region outside the contacts. Sample 2 has aluminum Schottky contacts evaporated to the surface after removing the 2DEG by 50-nm-deep dry etching to eliminate the surface leakage current. Al/Au ohmic contacts were formed on the backside of the Si substrate for the measurement of vertical leakage current. The purpose of the Schottky-contact sample is to study the effect of the Ti/Al/Ni/Au alloyed contact on the leakage current characteristics. As shown later on in this section, some of the vertical leakage current characteristics are associated with the contact formation.

- **Measurement Results**

In order to determine the conductivity and doping type of the Si substrate, the 2-μm AlGaN/GaN epi-layer was removed by dry plasma etching and subsequently ohmic contacts formation on the exposed Si surface. As shown in Figure 2-4, the vertical conductance measurement on the 500-μm-thick Si shows an average resistivity of about 400 Ω•cm, which is small enough to ignore the vertical voltage drop across the Si substrate in the vertical leakage measurements on sample 1 and 2 (see Figure 2-3). MIS-cap structure with 210 nm Nitride-buffer layer (after etching about 0.8 μm of the AlGaN/GaN epi-layer) was fabricated to extract the doping type of the Si substrate. As shown in Figure 2-5, the CV measurement shows that the Si substrate is p-type and the MIS-cap with 210 nm buffer layer has carrier inversion at bias voltage of 25 V.

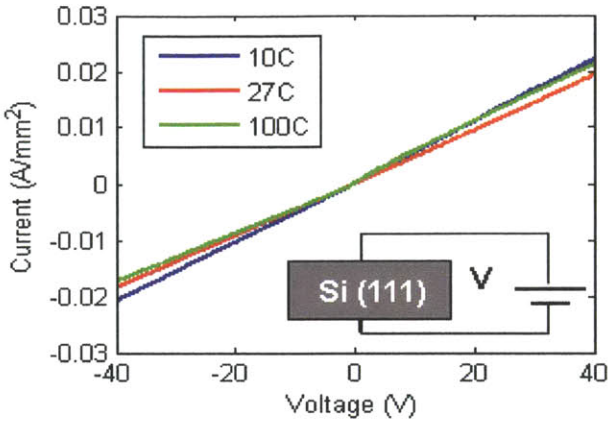

Figure 2-4. Vertical conductance measurement of the Si(111) substrate obtained by removing the GaN epi-layer.

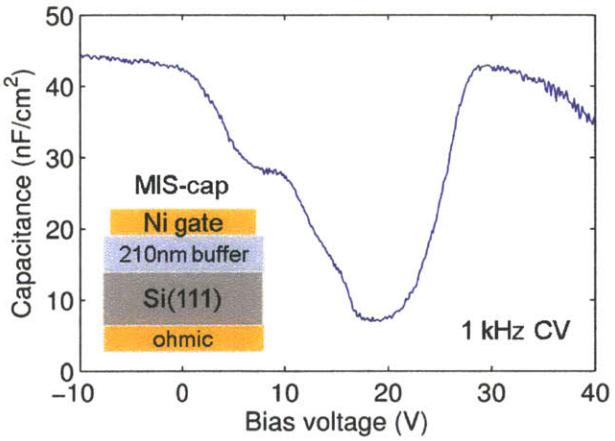

Figure 2-5. 1 kHz CV measurement of the MIS-cap structure on Si(111) substrate.

The vertical current-voltage characteristics of the Ti/Al/Ni/Au ohmic-contact sample (sample 1) and Al-Schottky sample (sample 2) are shown in Figure 2-6. In each sample, several devices were measured. For clearity, Figure 2-6 plots the representative characteristics of the devices. The vertical leakage is asymmetric for the ohmic-contact sample (sample 1). As shown in Figure 2-6(a), at the positive bias, the leakage current has a "turn-on" voltage (defined by linear extrapolation of leakage current to zero) around 100 V while at the negative bias, the turn-on voltage is about -300-340 V. The leakage current also

has different temperature response. At the positive bias, the leakage increases with temperature while at negative bias, it decreases at higher temperature and the leakage-turn-on voltage shifts to more negative value. One the other hand, the Schottky-contact sample (sample 2) has a leakage-turn-on voltage at positive bias of 400 V (see Figure 2-6(b)), 300 V higher than that of the sample 1 but has a similar leakage characteristics at negative bias.

The vertical capacitance-voltage (CV) characteristics of these two samples are shown in Figure 2-7. The capacitance at zero bias is 6 nF/cm^2, which is about 0.13 times of the capacitance of the MIS-cap capacitor shown in Figure 2-5, close to the ratio of the epi-layer thickness (210 nm / 2 μm) in both structures. The CV curve of the Schottky-contact sample also shows depletion and inversion characteristics of the p-type Si substrate at positive bias around 200 V. On the other hand, the capacitance of the ohmic-contact sample starts to increase at positive bias of 100 V, which is due to the on-set of the leakage current (see the inset of Figure 2-7(a)). The drop of the capacitance from its maximum value concurred with the saturation of the leakage current. These vertical leakage characteristics are analyzed in detail in the next section.

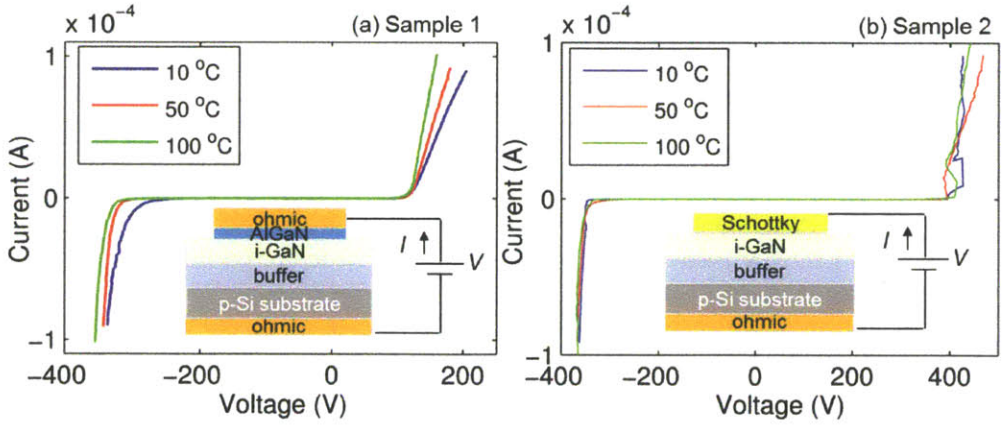

Figure 2-6. Vertical GaN-Si leakage measurement with (a) ohmic-contact sample 1 and (b) Al-Schottky-contact sample 2 at substrate temperature of 10°C, 50°C and 100°C. The top-contact size is 100 μm×50 μm.

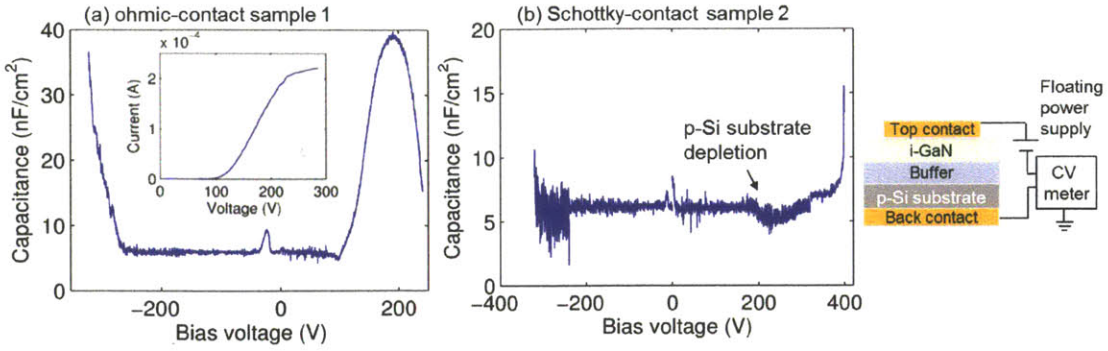

Figure 2-7. Vertical CV measurements with (a) ohmic top contact and (b) Schottky top contact on GaN-on-Si sample at 15 kHz. The top contact has a circular shape with a diameter of 180 μm. Inset in (a) shows the corresponding vertical I-V characteristics. The schematic shows the measurement setup.

The nitride-semiconductor epi-layer has very high resistivity due to low carrier concentration. The intrinsic carrier density in the epi-layer can be estimated from the vertical leakage current shown in Figure 2-6. For example, at a bias voltage of 100 V (either positive or negative), the leakage current in both devices is less than 1 μA (20 mA/cm^2 when normalized by the contact area) and the average electric field in the epi-layer is 500 kV/cm. At this electric field, the conduction band electrons should reach a saturation velocity v_{sat} of 2×10^7 cm/s [Frahmand2001]. Using equation $J = n_e q v_{sat}$, the maximum electron density n_e is estimated to be less than 10^{10} cm^{-3}. With such a low density of free carriers, the epi-layer is equivalent to an insulator between the top contact and the Si substrate in the vertical CV measurement shown in Figure 2-7. In order to conduct higher current through the epi-layer at the leakage-turn-on bias voltage in Figure 2-6, more carriers are needed. The following sections will discuss the origin of this increased carrier density in the epi-layer under high bias voltage conditions.

2.3.2 Trap-Limited Space-Charge Model (TLSC Model)

In a lightly doped semiconductor or insulator, carriers can be injected from electrodes into the semicondutor or insulator at large voltage bias [Lampert1956]. The low carrier density GaN epi-layer satisfies this carrier injection condition. When negative voltages are applied to the ohmic- or Schottky-contacts, electrons are injected into the epi-layer from the contacts. Electrons can also be injected from the Si substrate when positive voltages are

applied to these contacts with respect to the Si substrate. Since the Si substrate of our sample is p-type doped, an electron inversion layer needs to be formed at the epi-layer/Si interface before the injection can happen. This is observed in the CV measurement in Figure 2-7.

The injected carriers (electrons in our case) form a space-charge region in the epi-layer and create an electric-field distribution. The current carried by the injected carriers is called space-charge-limited (SCL) current. Its current-voltage relationship can be derived from Poisson equations. Assuming the drift current is dominant (which can be satisfied at relatively large bias conditions when the diffusion current is much smaller than the drift current), the space-charge-limited electron current is

$$J = qnv_e$$

In the low-field regime, the electron velocity v_e is μE, where E is electric field. In the high-field regime, v_e is the saturation velocity v_{sat}. In the study of the vertical leakage current in our samples, the high-field regime is more relavent to our understanding of device breakdown voltage. Therefore, in the following analysis, we will focus on the velocity saturation condition.

Using current density continuity (i.e. without current crowding effect), the injected electrons are uniformly distributed in the epi-layer under velocity saturation condition at high electric field (E > 100 kV/cm). As a result, the electric field strength in the epi-layer linearly increases with distance as shown in Figure 2-8. (For electron injection from the Si substrate, it is similar to the schematics in Figure 2-8 but with E-field in opposite direction.)

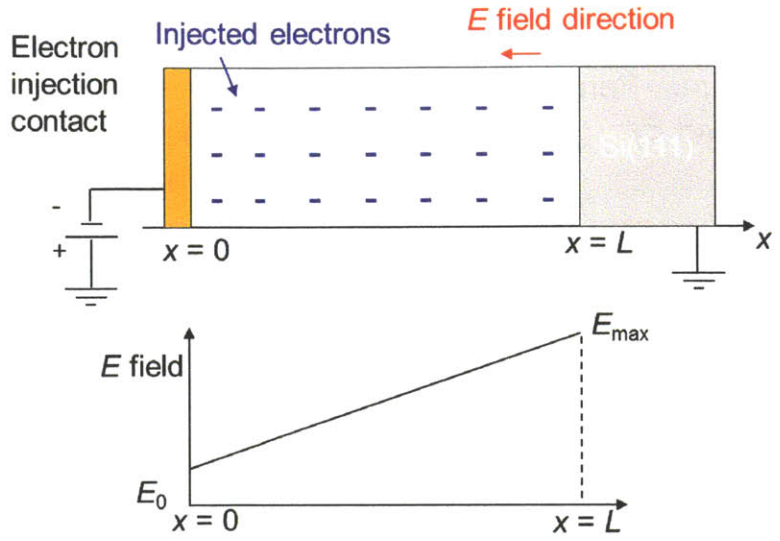

Figure 2-8. Schematics of the injected electrons uniformly distributed in the epi-layer at negative bias on the contact in the velocity saturation regime. The injected electrons create a linearly increasing electric field.

From Poisson equation $\nabla^2\psi = qn/\epsilon_s$, the voltage across the space-charge-current region is:

$$V = E_0 L + \frac{J}{2\epsilon_s v_{sat}} L^2$$

where L is the length of the space-charge region (the epi-layer thickness in our case); ϵ_s is semiconductor dielectric constant; E_0 is the injection electric field at the contact.

When traps exist in the semiconductor, they can hinder the flow of injected carriers. The corresponding current under the influence of traps is termed as trap-limited space-charge current [Lampert1956]. For example, in the case of a high density of deep traps (see Figure 2-9), the injected electrons have to fill the traps before they can conduct current.

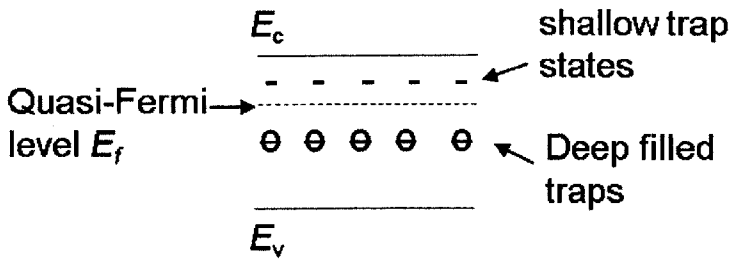

Figure 2-9. Band diagram illustrates the position of quasi-Fermi-level with respect to shallow and deep traps.

The trap-limited space-charge current model described in [Lampert1956] can be adapted to the case of high electric field using saturation velocity for the carriers. Given an electron trap energy level at E_t with density N_t, and assuming that the electrons [8] in the conduction band are in quasi-thermal equilibrium with the trap states, the electron density in the conduction band is given by Boltzmann distribution

$$n = N_c \exp(-\frac{E_c - E_f}{kT})$$

where E_f, is the quasi-Fermi-level.

The density of occupied trap states is given by Fermi-Dirac distribution

$$n_t = \frac{N_t}{1 + \exp([E_t - E_f]/kT)}$$

The current density in the velocity saturation regime is

$$J = qnv_{sat}$$

Including the traped charges, the Poisson equation is

$$\nabla^2\psi = q(n + n_t)/\epsilon_s = q\theta n/\epsilon_s$$

where $\theta = 1 + n_t/n$.

[8] Here we consider the case of electron injection into the semiconductor from contacts. Similar derivation can be extended to holes with electron traps replaced by hole traps.

For uniformly distributed trap density, the voltage-current relation can be derived using the Poisson equation and current density equation with the injection electric field of E_0 at the contact:

$$V = \frac{\theta L^2}{2\epsilon_s v_{sat}} J + E_0 L$$

When $E_t - E_f \gg kT$, θ is approximately a constant, $1 + \frac{N_t}{N_c} \exp(\frac{E_c - E_t}{kT})$, and V is linear with J.

The voltage derived above is under the condition of uniformly distributed traps between $x = 0$ and $x = L$. Now we discuss the case of non-uniform trap densities. In the simplest example shown in Figure 2-10, the trap desnity N_{t1} between $x = 0$ and $x = L_1$ is different from the trap density N_{t2} between $x = L_1$ and $x = L$, with $N_{t1} < N_{t2}$. The traps in both regions have the same energy level of E_t. Similar to the derivation in the case of uniform trap density, we have the voltage-current relation:

$$V = \frac{\theta_1 L_1^2}{2\epsilon_s v_{sat}} J + \frac{\theta_2 (L - L_1)^2}{2\epsilon_s v_{sat}} J + \frac{\theta_1 L_1 (L - L_1)}{\epsilon_s v_{sat}} J + E_0 L_1$$

Substituting $\theta_1 = 1 + n_{t1}/n$ and $\theta_2 = 1 + n_{t2}/n$ in the equation, we have

$$V = \left[1 + \left(\frac{L_1}{L} n_{t1} + \frac{L - L_1}{L} n_{t2}\right)\frac{1}{n}\right] \frac{L^2}{2\epsilon_s v_{sat}} J + E_0 L$$

$$= \frac{\tilde{\theta} L^2}{2\epsilon_s v_{sat}} J + E_0 L$$

where $\tilde{\theta} = 1 + \left(\frac{L_1}{L} n_{t1} + \frac{L - L_1}{L} n_{t2}\right)\frac{1}{n}$. Since the traps are at the same energy level E_t, applying the Fermi-Dirac distribution, we have

$$\tilde{\theta} = 1 + \frac{1}{n}\left(\frac{L_1}{L} N_{t1} + \frac{L - L_1}{L} N_{t2}\right) \frac{1}{1 + \exp\left(\frac{[E_t - E_f]}{kT}\right)}$$

$$= 1 + \frac{\tilde{N}_t}{1 + \exp([E_t - E_f]/kT)} \frac{1}{n} = 1 + \frac{\tilde{n}_t}{n}$$

We arrive at an effective trap density $\tilde{N}_t$:

$$\tilde{N}_t = \frac{L_1}{L} N_{t1} + \frac{L - L_1}{L} N_{t2}$$

Using the effective trap density, non-uniform trap distributions can be converted to the case of uniform trap desnity with the same voltage-current relation as before. It is easily seen in Figure 2-10 that the corresponding effective electric field has a lower maximum value at $x = L$ than the actual value under the condition of $N_{t1} < N_{t2}$ or higher than the actual value for $N_{t1} > N_{t2}$.

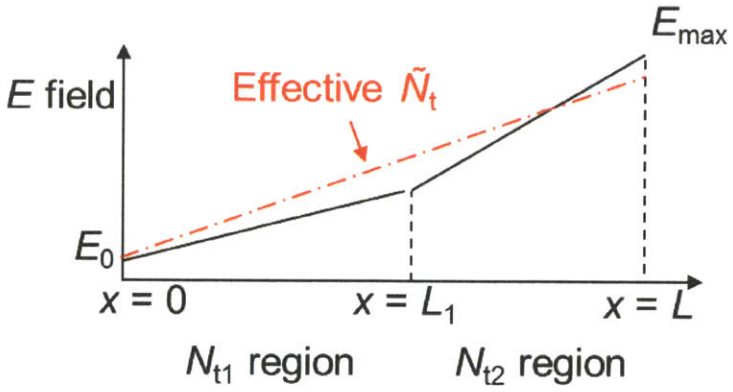

Figure 2-10. Schematic of electric field in the TLSC model with different trap density in two regions with $N_{t1} < N_{t2}$.

To illustrate the characteristics of the trap-limited space-charge (TLSC) current, *I-V* curves are calculated by applying the TLSC model to a 2-μm GaN layer with uniformly distributed traps at three energy levels of 0.55 eV, 0.4 eV and 0.3 eV below the conduction band edge with $E_0 = 0$, as shown in Figure 2-11. An electron saturation velocity of 2×10^7 cm/s is used. The trap energy levels, trap densities and E_0 value used in the calculation are chosen only for illustration purpose.

As shown in Figure 2-11(a), the TLSC current has a "turn-on" characteristic, which is due to the trap filling process. Plotted in the log-log scale in Figure 2-11(b), the curves show a linear relation between V and I with $\log I / \log V = 1$, as expected for $E_t - E_f \gg kT$. When the trap at E_c - 0.55 eV is filled, the current increases at a faster rate until the quasi-Fermi

level approaches the other two trap levels (e.g. $E_t - E_f \sim kT$) at E_c - 0.3 eV and E_c-0.4 eV. Then the current-voltage curves show a "power law" characteristic.

At higher temperature, the TLSC current increases, as shown in Figure 2-11. An important feature in the temperature dependence of TLSC current shown in the log-log scale in Figure 2-11(b) is that not only the curve shifts upwards but also its slope ($d\log I$ / $d\log V$) decreases at higher temperature.

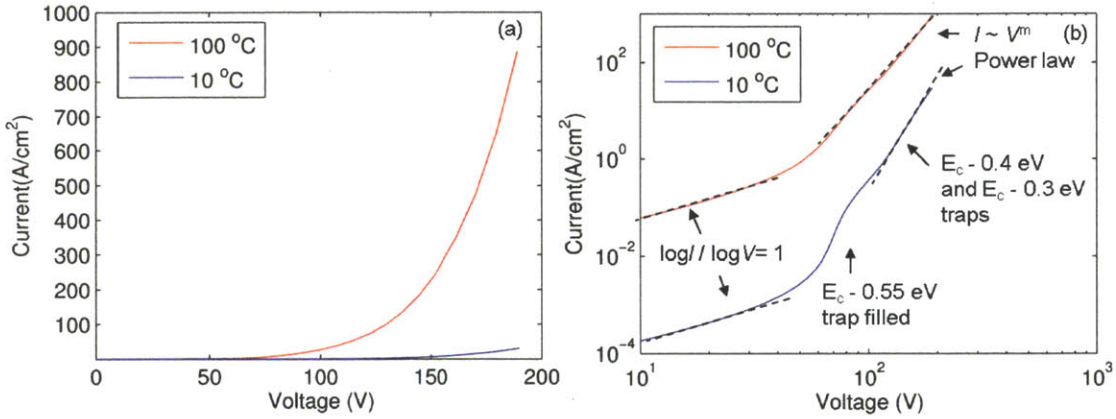

Figure 2-11. Calculated TLSC current in 2 μm GaN layer at 10 °C and 100 °C with three trap levels: E_c-0.55 eV, E_c-0.4 eV and E_c-0.3 eV. All have a density of 2×10^{16}cm^{-3} except the E_c-0.3 eV trap having a density of 3×10^{16}cm^{-3}. The results are plotted in linear scale (a) and in log-log scale (b).

We now use the TLSC model derived in the velocity saturation regime to characterize the vertical leakage current in our samples. A general form of the TLSC current-voltage relation can be written in the following equations for our samples:

$$V = V_0 + \frac{qL^2}{2\epsilon_s}\sum_{i=1}^{K}\frac{\widetilde{N}_{t,i}}{1+\exp\left(\frac{[E_{t,i}-E_f]}{kT}\right)} + \frac{L^2}{2\epsilon_s v_{sat}}J$$

where there are K numbers of different trap energy levels $E_{t,i}$ with uniformly distributed effective trap density $\widetilde{N}_{t,i}$ for each trap level; L is the epi-layer thickness which is 2 μm for the ohmic-contact sample and 1.95 μm for the Schottky-contact sample (there is 50 nm

recess in the Schottky-contact sample); ϵ_s is the epi-layer dielectric constant which is approximately equal to the GaN dielectric constant of 10.4; current density $J = qN_c \exp\left(-\frac{E_c - E_f}{kT}\right) v_{sat}$ which determines the Fermi-level position; V_0 is voltage above which the TLSC current can be measured; For example, at low bias voltages less than V_0, the current may not be space-charge limited but rather follows the ohmic law or is limited by the contact injection (e.g. thermionic emission or tunnel from the Schottky contact). V_0 also includes the voltage term $E_0 L$ due to the contact injection electric field E_0.

Since the measured vertical leakage current density J is less than 2.5 A/cm^2, $\frac{L^2}{2\epsilon_s v_{sat}} J$ term in the above equation is smaller than 3 mV and can be ignored. As a result, the equation is further simplified:

$$V \approx V_0 + \frac{qL^2}{2\epsilon_s} \sum_{i=1}^{K} \frac{\widetilde{N}_{t,i}}{1 + \exp\left(\frac{[E_{t,i} - E_f]}{kT}\right)}$$

The measurement data were fitted using the above equation by least-square method (see the Matlab-code in Appendix D) with V_0 and effective trap density $\widetilde{N}_{t,i}$ as the fitting parameters. Trap energy levels were fixed at 0.85 eV, 0.8 eV, 0.75 eV...0.3 eV below the conduction band edge E_c. The fitting results are shown in Figure 2-12. For each data point in Figure 2-12, the current density determines the Fermi-level position, with which the trap density $\widetilde{N}_{t,i}$ and V_0 are adjusted to match the bias voltage.

The extracted fitting parameters are shown in Table 2-1. Most of them have tight confidence bound (starting with different initial values for these fitting parameters, the least-square fitting always gives the same results) except for the non-zero trap densities at shallow trap level of 0.3 eV below E_c. This is due to the limited maximum leakage current density measured in the samples which corresponds to quasi-Fermi-levels at least 0.37 eV below the E_c (calculated from the Boltzmann statistic equation). The fitting to 6 different J-V curves all gives a major trap level between 0.6 eV and 0.5 eV below E_c, as shown in Table 2-1. This trap level has been reported in the literature [Pernot2008]. It can be observed in Table 2-1 that only the 50 °C measurement data give a non-zero value for V_0, especially for the Schottky-contact sample. The reason for this is not clear at this moment. The relatively high

leakage current noise floor prevents further investigation of the V_0 as it limits the fitting to bias voltages above 200-250 V for the ohmic-contact sample and 250-300 V for the Schottky-contact sample. Extending the usable data to voltages lower than 200 V with higher current desnity resolution will provide more clues to question on the V_0.

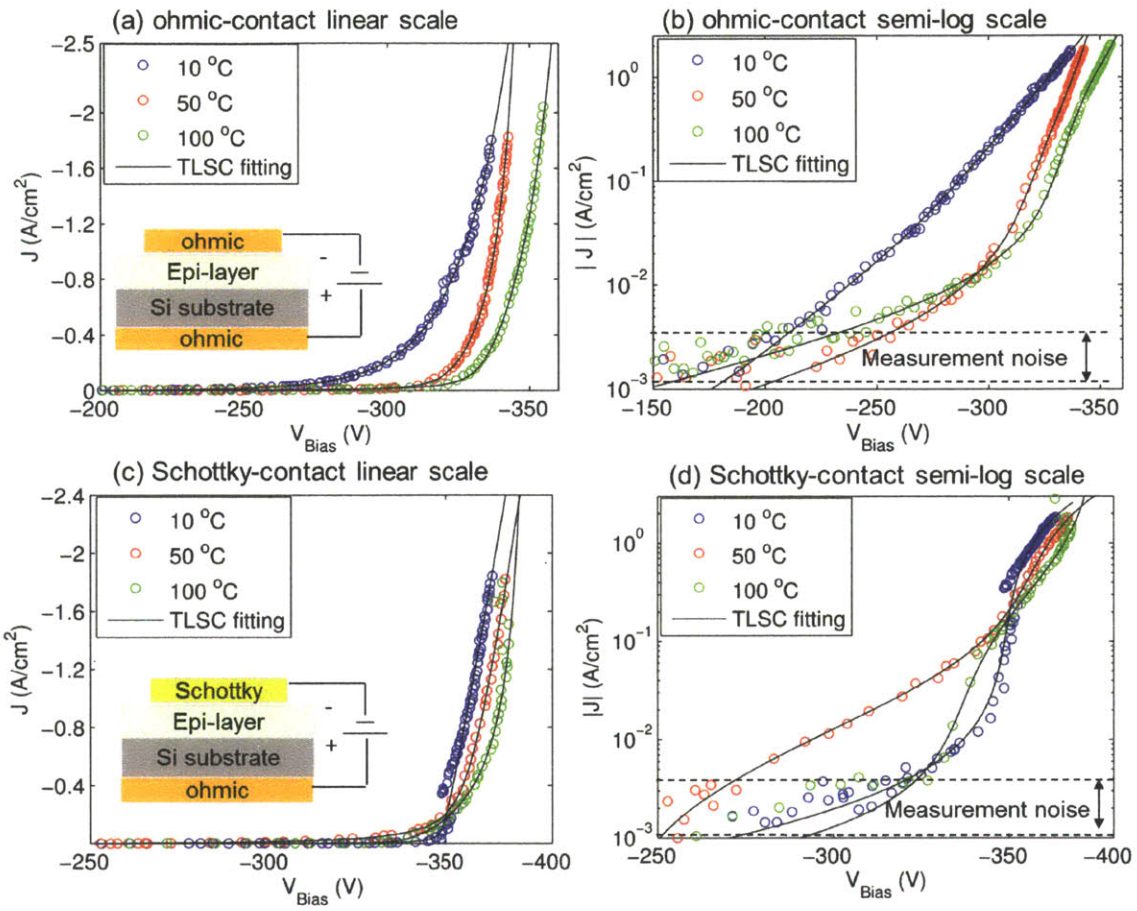

Figure 2-12. Fitting to the vertical leakage current measured on both ohmic-contact and Schottky-contact samples at negative bias: (a) ohmic-contact sample plotted in linear scale (b) and semilog scale; (c) Schottky-contact sample plotted in linear scale (d) and semilog scale.

The negative temperature coefficient of the leakage current shown in Figure 2-12 is in contradiction to the TLSC current, which should have positive temperature coefficient. There are two possibilities: 1) the decrease of saturation velocity of electrons with increasing temperature [Albrecht1998] can cause the leakage current to decrease at higher temperatures;

2) if the leakage current has impaction ionization component, increasing the temperature will suppress the current due to the negative temperature coefficient of the impact ionization rate (see section 0). In fact, the maximum electric field strength calculated from the fitting (with linearly-increasing electric field profile from the uniform effective trap density $\widetilde{N}_t$) is higher than 3 MV/cm for bias voltages lower than -300 V. For non-uniform trap distribution with higher trap density near the Si substrate, the maximum electric field will be even larger as shown in Figure 2-10. For such high electric field, impact ionization effect should be considered. In the following sections, the TLSC model is further modified to include the effect of impact ionization.

Table 2-1. Extracted V_0 and effective $\widetilde{N}_t$ at different trap levels by least-square fitting to the vertical leakage measurement data of the negative biased ohmic-contact and Schottky-contact samples using the TLSC model.

Ohmic-contact	$\widetilde{N}_t$ (10^{16}/cm^{-3}) at E_c-E_t (eV)												
	V_0 (V)	0.85	0.8	0.75	0.7	0.65	0.6	0.55	0.5	0.45	0.4	0.35	0.3
10 °C	0	0	0	0	0	0	5.16	0.68	1.81	0.92	0.95	1.36	0
50 °C	59.1	0	0	0	0	5.56	1.82	0	0.25	0.72	0	0	3.16
100 °C	0	0	0	6.01	3.54	0	0	0.02	1.25	0	0	0	0
Schottky-contact	$\widetilde{N}_t$ (10^{16}/cm^{-3}) at E_c-E_t (eV)												
	V_0 (V)	0.85	0.8	0.75	0.7	0.65	0.6	0.55	0.5	0.45	0.4	0.35	0.3
10 °C	0	0	0	0	0	0	7.84	2.73	0	0	0	0	7.28
50 °C	237.7	0	0	0	0	0	1.33	2.26	0	0	0	4.49	7.75
100 °C	0	0.21	9.96	0	0	0	0.15	1.05	0	0	0	0	0

2.3.3 Impact Ionization Model

Under high enough electric field, carriers in a semiconductor layer can gain sufficient energy to generate electron-hole pairs in the semiconductor by collisions with valence electrons. The impact ionization process is characterized by the ionization rate α, which is the average number of electron-hole pairs produced by an electron per centimeter travelled in the direction of electric field [McKay1954]. Assuming the same impact ionization rate for electrons and holes, electron multiplication by impact ionization through a region with width of W shown in Figure 2-13 can be written as [Sze&Ng]:

$$1 - \frac{1}{M} = \int_0^W \alpha dx$$

where $M = J / J_{n0}$ is the multiplication factor with J_{n0} for the initial electron current and J for the total current, as shown in Figure 2-13.

Given a saturation velocity v_e and without hole current injection at $x = W$, as shown in Figure 2-13, the multiplication factor can be written as the ratio of electron densities at $x = 0$ and $x = W$:

$$M = J / J_{n0} = n/n_0$$

This carrier multiplication is an important signature of impact ionization as opposed to Zener emission which does not have carrier multiplication effect.

When the integration of impact ionization rate over the space-charge region with width W, in which the electric field is confined, equals to unity, M becomes infinite. This is defined as the avalanche breakdown condition. Under this condition, the large amount of generated carriers can modify the electric field in the space-charge region, in a way that increasing the current in the semiconductor requires lower voltage than the avalanche voltage, i.e. the material exhibits a negative differential resistance [Gunn1956].

The impact ionization rate α is a strong function of electric field E [Sze1966]:

$$\alpha = A\exp(-b/E^m)$$

This rate decreases with increasing temperature due to the increased scattering and reduced carrier mean free path. As a result, the avalanche breakdown voltage has positive temperature coefficient (i.e. higher breakdown voltage at higher temperature).

From the impact ionization rate, the avalanche breakdown voltage can be calculated. For example, the avalanche breakdown voltage for one-sided abrupt junction is [Sze1966]

$$V_{BD} = \epsilon_s E_m^2 / 2qN_B$$

where ϵ_s is semiconductor dielectric constant, N_B is doping concentration and E_m is the maximum electric field at avalanche breakdown, which is also called the critical electric field or breakdown field.

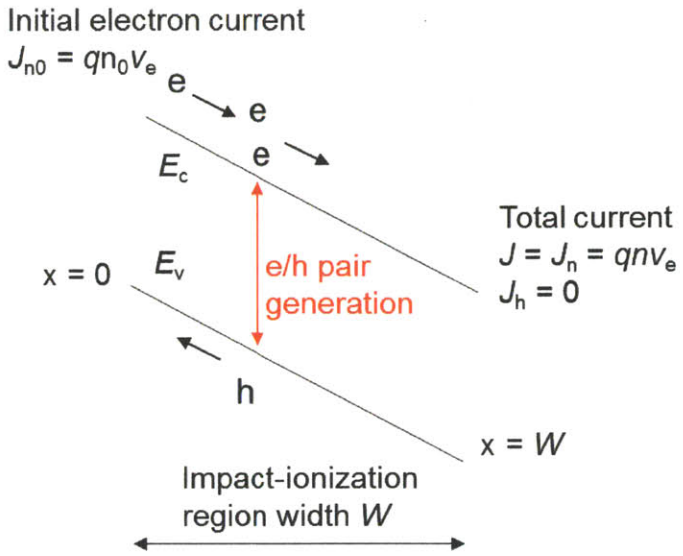

Figure 2-13. Illustration of impaction ionization initiated by electron current in an impact ionization region of width W.

To illustrate how electric field affects the impact ionization rate and current, we calculate the impact ionization current in the 2-μm epi-layer of our device under two conditions: a) a uniform electric field (i.e. $E(x)$ = constant for all x), and b) a linearly increasing electric field $E(x) = E_{peak}\,x/W$. The impact ionization rate in GaN is obtained from the empirical equation [Kunihiro1999]:

$$\alpha_n = 2.9 \times 10^{18} \exp(-3.4 \times 10^7/E)$$

where the electric field E is in V/cm.

Due to the lack of published studies on the impact ionization rate of holes, we will assume it is the same as for electrons. This assumption agrees well with the work of [Oguzman1997] at high electric fields. As a result, we can use the equation:

$$1 - \frac{1}{M} = \int_0^W \alpha_n dx$$

Using an electron injection current of $J_0 = qn_0v_e$ with $n_0 = 10^{10}$ cm^{-3} and electron saturation velocity $v_e = 2\times10^7$ cm/s, the impact ionization current can be calculated by:

$$J = MJ_0 = Mn_0v_e$$

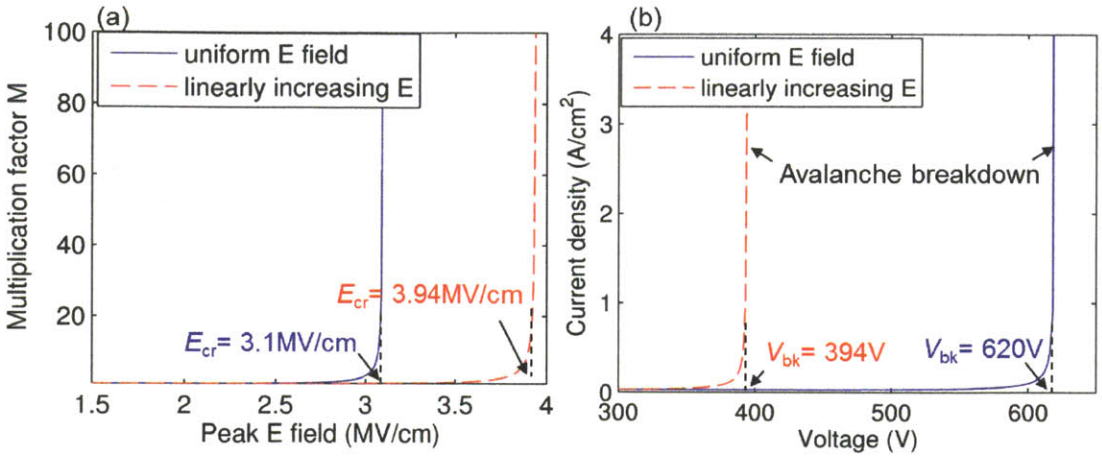

Figure 2-14. (a) Calculated impact ionization multiplication factor M as a function of peak electric field; and (b) corresponding current density as a function of voltage across a 2 μm GaN epi-layer.

The calculated multiplication factor M, and current density J as a function of peak electric field is shown Figure 2-14. The electric field profile greatly affects the critical electric field. In the case of uniform E field in GaN, E_{cr} = 3.1 MV/cm and in the case of linearly increasing E field, E_{cr} = 3.94 MV/cm. For both cases there is almost no impact ionization when E field is less than 2 MV/cm. As shown in Figure 2-14(b), the calculated avalanche breakdown voltage V_{bk} in a 2-μm-thick GaN is 620 V for the uniform E field case and 394 V for the linearly increase E field case.

It is important to note that the impact ionization needs to be initiated by a non-zero initial current. In the vertical GaN-on-Si leakage measurement, this initial current can be provided by carrier injection from the contacts or from the Si substrate, which is subject to the space-charge effect. As a result, both the impact ionization and the trap-limited-space-charge effects are needed to model the vertical leakage current in the GaN-on-Si devices. In the following section, a trap-limited space-charge impact-ionization (TLSCII) model is derived.

2.3.4 Trap-Limited Space-Charge Impact-Ionization Model (TLSCII Model)

In this section, the TLSC model in section 2.3.2 is modified to include the effect of impact ionization. This new model is called the trap-limited space-charge impact-ionization (TLSCII) model.

The proposed model is based on the fact that the impact ionization rate is a strong function of electric field. Because of the increasing electric field in space-charge region as shown in Figure 2-15 (assuming uniform traps), most of the impact ionization is confined to a small region between $x = L_1$ and $x = L$ near the maximum electric field.

As shown in Figure 2-15, the electron density at the $x = L_1$ boundary of the impact ionization region is n_0. At the other boundary of the impaction ionization region ($x = L$), the electron density becomes $n = M \times n_0$. The multiplication factor can be calculated assuming the same impact ionization rate for both electrons and holes and the impact ionization is initiated by electron injection from contact without hole injection from Si substrate:

$$1 - \frac{1}{M} = \int_0^L \alpha_n(E)dx \cong \int_{L_1}^L \alpha_n(E)dx \tag{2-1}$$

Because there is no hole injection from the Si substrate, the total current density at $x = L$ is given by:

$$J = qnv_e = qMn_0v_e \tag{2-2}$$

where v_e is electron saturation velocity, which is approximately 2×10^7 cm/s in GaN.

At $x = L_1$, the generated holes, with a density of p, flow toward the electron injection contact. The current at $x = L_1$ is:

$$J = qn_0v_e + qpv_h$$

where v_h is hole saturation velocity, which is 5×10^6 cm/s in GaN [Oguzman1996].

Applying the total current density equation (2-2) in the above equation, we have the hole density p at $x = L_1$:

$$p = \frac{(M-1)n_0 v_e}{v_h} \tag{2-3}$$

If we ignore the electron-hole recombination in the region between $x = 0$ and $x = L_1$, from electron/hole current continuity, the electron and hole densities are constant from $x = 0$ to $x = L_1$ with values n_0 and p, respectively. This is a good approximation in pre-avalanche breakdown conditions, where there are relatively small amount of generated holes.

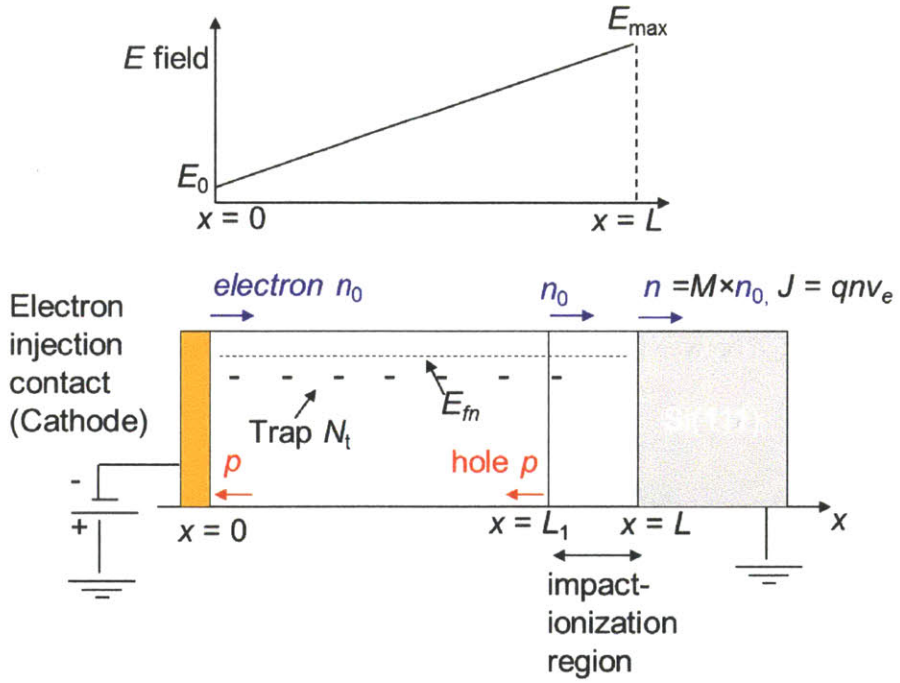

Figure 2-15. Illustration of the trap-limited space-charge impact-ionization (TLSCII) model with negative bias on the contact with respect to the Si substrate. The impact ionization is initiated by electron injection.

The electric field can be calculated following the same arguments from section 2.3.2: the electrons in the conduction band are in quasi-thermal equilibrium with the trap states at energy level E_t and with density of N_t. The quasi-Fermi-level is labeled as E_{fn} in Figure 2-15. Using Fermi-Dirac distribution, the electron density n_0 is then given by:

$$n_0 = N_c \exp(-\frac{E_c - E_{fn}}{kT}) \tag{2-4}$$

The density of occupied trap states (negatively charged) is

$$n_t = \frac{N_t}{1+\exp([E_t - E_{fn}]/kT)} \tag{2-5}$$

With uniform effective trap density, the electric field profile shown in Figure 2-15 is

$$E(x) = \frac{q(n_0 - p + n_t)}{\epsilon_s} x + E_0 \tag{2-6}$$

with a maximum value E_{max} at $x = L$.

The effect of the generated carriers on the electric field within the impact ionization region between $x = L_1$ and $x = L$ is ignored especially in the pre-avalanche condition when relatively small amount of electron-hole pairs are generated and most of the oppositely charged electrons and holes in this region cancel the electric field from each other.

The voltage applied between the ohmic contact and the Si substrate (see Figure 2-15) is

$$V_{Bias} = \frac{(E_{max} + E_0)L}{2} \tag{2-7}$$

The set of coupled nonlinear equations (2-1)-(2-7) can be solved numerically to get the current-voltage relation. Since the measured vertical leakage current density is less than 2.5 A/cm^2, using the hole current equation $J_h = qnv_h = J - J_n < J$ we have the estimated hole density p of less than 3.1×10^{12} cm^{-3}, which is much smaller than the trapped electron density n_t (on the order of 10^{16} cm^{-3}). Therefore the hole density p in equation 2-6 can be ignored, which significantly simplifies the numerical calculation. In the next section, we apply the TLSCII model to analyze the measured data.

2.3.5 Vertical Breakdown of AlGaN/GaN-on-Si Structures: Negative Bias Condition

In this section, the TLSCII model is used to analyze the vertical leakage current under negative biases through the AlGaN/GaN-on-Si epi-layer in the ohmic-contact and Schottky-contact samples.

Since very little is known about the temperature dependence of the impact ionization rate in wurtzite GaN, room temperature impaction ionization rate is used for all the TLSCII model calculations. Monte Carlo simulation of zinc-blende GaN showed small temperature coefficient of impact ionization rate for electric field larger than 2 MV/cm [Tirino2003]. We suspect similar behavior applies to wurtzite GaN. The electron saturation velocity is assumed to be constant with temperature based on reference [Albrecht1998] which shows that the electron saturation velocity in GaN reduces by less than 10% from 300K to 400K. Constant saturation velocity is also assumed for the holes. As a result, we will not study the temperature dependence of the leakage current due to the limited information on the material properties. However it is not likely due to the reduction of electron saturation velocity at high temperature to cause the reduction in the leakage current in the ohmic contact sample.

Similar to section 2.3.2, the vertical leakage current measured on both ohmic-contact and Schottky-contact samples at negative bias voltages were fitted with the TLSCII model using the least-square method (see the Matlab-code in Appendix D). The injection electric field E_0 is calculated by $E_0 = V_0/L$ using the extracted V_0 in section 2.3.2. Therefore, the only fitting parameters are the effective trap densities. The trap energy levels were chosen to be the subset of the ones used in section 2.3.2 to reduce redundant zeros as shown in Table 2-2.

Table 2-2. Extracted effective $\widetilde{N}_t$ at different trap levels by least-square fitting to the vertical leakage measurement data of the negative biased ohmic-contact and Schottky-contact samples using the TLSCII model. Dash means the corresponding E_t is not used in the fitting.

Ohmic-contact	$\widetilde{N}_t$ (10^{16}/cm^{-3}) at E_c-E_t (eV)											
	0.85	0.8	0.75	0.7	0.65	0.6	0.55	0.5	0.45	0.4	0.35	0.3
10 °C	-	-	-	-	0	5.05	0.86	1.68	1.08	0.68	2.24	0
50 °C	-	-	-	0	5.57	1.81	0	0.26	0.76	0	0	2.02
100 °C	-	0	6.03	3.56	0	0	0	1.36	0.56	0	-	-
Schottky-contact	$\widetilde{N}_t$ (10^{16}/cm^{-3}) at E_c-E_t (eV)											
	0.85	0.8	0.75	0.7	0.65	0.6	0.55	0.5	0.45	0.4	0.35	0.3
10 °C	-	-	-	-	0	8.7	1.86	0	0	0	2.21	-
50 °C	-	-	-	-	0	1.33	2.26	0	0	0	5.93	-
100 °C	3.19	6.95	0	0	0	0.36	1.24	0	2	-	-	-

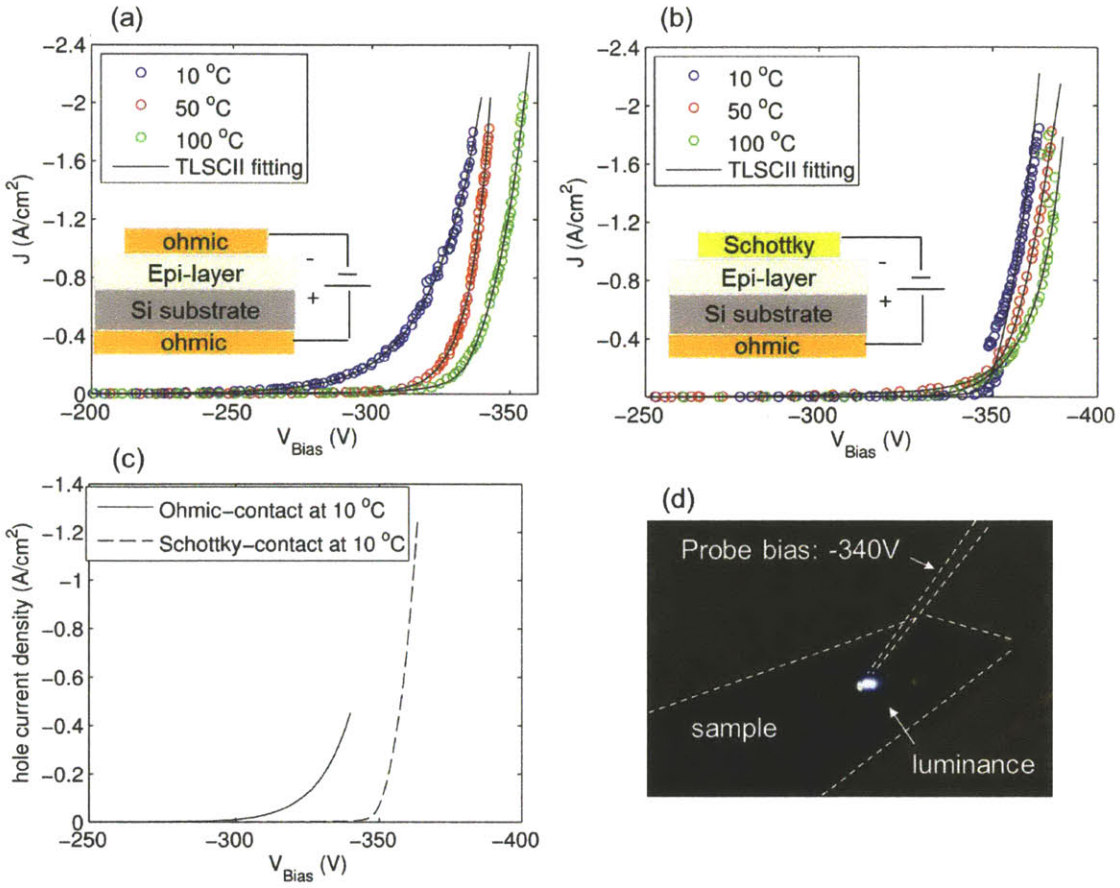

Figure 2-16. TLSCII model fitting to the measured vertical leakage current at negative bias conditions on (a) ohmic-contact sample and (b) Schottky-contact sample. (c) Extracted hole current density from the TLSCII model at 10 °C (d) Digital camera picture of luminance from the ohmic-contact sample at bias voltage around -340 V.

The fitting results are shown in Figure 2-16(a) and (b) with the fitting parameters listed in Table 2-2. Compared to the results from the TLSC model, there are small adjustments to the trap densities due to the effect of the impact ionization. Due to the strong function of the impact ionization rate on the electric field, the fitting converges much easier when the data points include lower voltages at which there is no impact ionization, which is the case for the ohmic-contact sample. For the Schottky-contact sample, the data points used in the fitting are all at high voltage and high electric field regime. As a result, the convergence is sensitive to the initial value used in the fitting. Therefore, it is preferred to have the data points in the range without impact ionization to extact the trap information using the TLSC model and the

avalanche breakdown voltage can be estimated based on the TLSC model when the calculated electric field strength approaches the critical electric field of the semiconductor. This approach is used in section 2.3.7 to calculate the maximum breakdown voltages in GaN-on-Si wafers.

The calculated hole-current density at 10 °C due to the impact ionization is shown in Figure 2-16(c). The hole current increases faster for the Schottky-contact sample due to higher electric field than in the ohmic-contact sample. This hole-current density is calculated from the linearly increasing electric field profile with the uniform effective trap densities, which by no means is accurate as the actual trap density is probably non-uniform. Nevertheless, a sustaining luminance was observed as shown in Figure 2-16(d). The electro-luminance picture was taken at an applied voltage of -340 V at room temperature. Since the GaN bandgap energy corresponds to a wavelength of about 360 nm, invisible to human eyes, the visible bright color of the electro-luminance suggests there is photon emission from defect states which have lower energy than the GaN bandgap energy. This defect-state photon emission is probably due to the recombination of the trapped electrons in the defect states with the holes generated from the impact ionization traveling towards the contact as shown in Figure 2-15.

2.3.6 Vertical Breakdown of AlGaN/GaN-on-Si Structures: Positive Bias Condition

When positive voltage is applied to the top contact with respect to the Si substrate, electrons can be injected from the Si substrate. Because the Si substrate is p-type, an inversion layer has to be formed at the epi-layer/Si interface before the electrons are injected from the Si substrate, as shown in the band diagram in Figure 2-18.

We first analyze the forward-bias leakage characteristics of the Al-Schottky contact devices. From the vertical CV measurement shown in Figure 2-7(b), the inversion in the p-type Si substrate starts at about 240±10V. The injection electric field can be estimated:

$$E_0 = \frac{V_{inv}}{L_{epi}} = \frac{240\text{V}}{2\mu\text{m}} = 1.2\ \text{MV/cm}$$

Using the estimated injection electric field, the *J-V* characteristics of Al-Schottky contact sample at the positive bias can be calculated ignoring the voltage drop in the depletion region in the Si substrate. Figure 2-17 compares measurement data with the calculation result (Only

the 50 °C case is plotted for illustration purpose). Although the the calculation has about the same leakage onset voltage as in the measured data, it deviates from the measurement shortly after the leakage current is turned on. As discussed below, this deviation can be explained by a limited electron generation rate in the p-type Si depletion region.

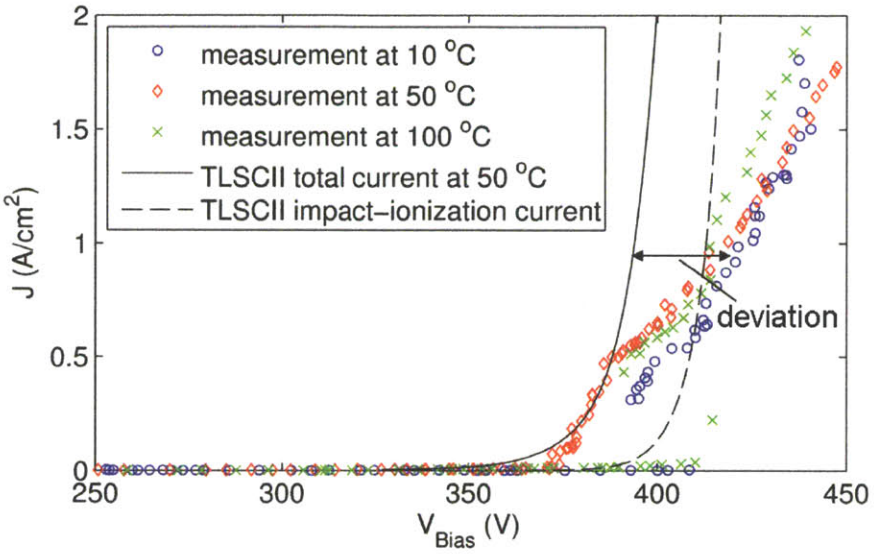

Figure 2-17. TLSCII model calculation result fitting to the measurement data of Al-Schottky contact sample under positive bias condition.

Since the current is carried by the electrons injected from the Si substrate, it will be limited by the electron generation rate in the p-type Si substrate depletion region, as shown in Figure 2-18. The electron generation-rate limited current can be derived from the steady state condition:

$$\frac{dn}{dt} = \frac{1}{q}\frac{dJ_n}{dx} + G = 0$$

Using the Boundary conditions $J_n(x = 0) = J$, $J_n(x = W) = 0$, we have

$$J = q\int_0^W G dx \tag{2-8}$$

where G is the electron generation rate in the depletion region of the p-type Si substrate; W is the depletion region width.

Using current continuity condition, the electron density n_0 in the GaN epi-layer associated with the injection electron current in Equation (2-8) can be calculated in the velocity saturation regime:

$$n_0 = \frac{J}{qv_e} = \frac{1}{v_e}\int_0^W G dx \tag{2-9}$$

Combine equation (2-9) with equations (2-2) to (2-7) from section 2.3.4, current-voltage relation can be solved with the knowledge of generation rate G and electric field profile inside the depletion region of the Si substrate.

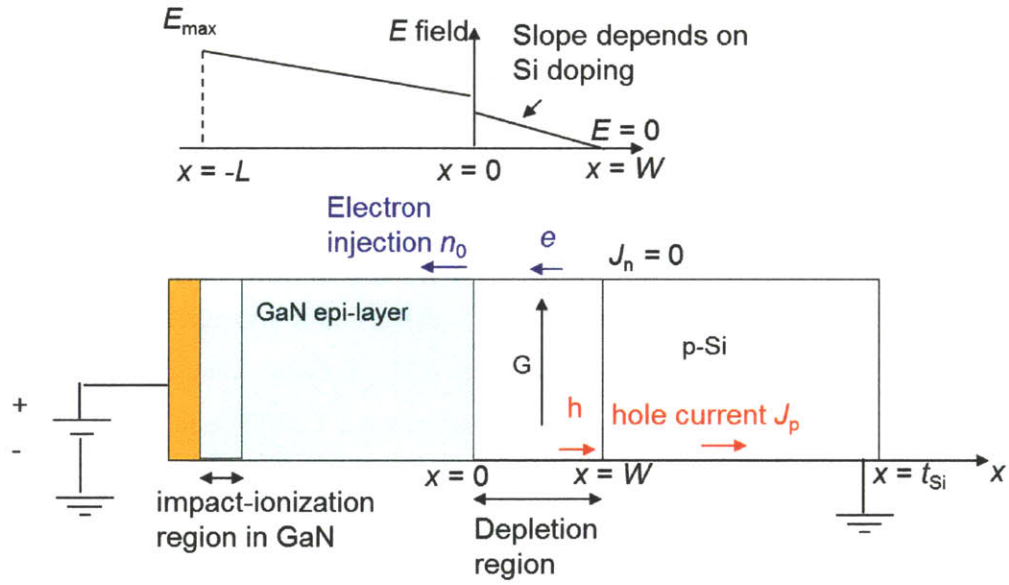

Figure 2-18. Illustration of the electron injection from p-Si substrate at positive bias condition where the electron injection is limited by the generation rate G in the depletion region of the p-type Si substrate.

For the lack of information on G, we will qualitatively discuss two breakdown situations:

Leakage current limited by the traps in GaN epi-layer. When there are deep-level traps in GaN epi-layer, the current carried by the injected electrons from the Si substrate is

suppressed. After these deep-level traps are filled, leakage current increases until it is limited by the electron generation in the depletion region of the p-type Si substrate.

Leakage current limited by electron generation in p-type Si. This situation occurs when deep-level traps in the GaN epi-layer is filled or there are only shallow traps which do not pose a limitation to the leakage current. As a reulst, the leakage current is limited by electron generation in the depletion region in the p-type Si substrate. This current is determined by equation (2-8), from which we can calculate the conduction band electron density in GaN epi-layer using equation (2-9). Then the qausi-fermi level position and the occupied trap density can be calculated with equations (2-4) and (2-5). Electric field in GaN epi-layer can also be determined from the coupled equations (2-1), (2-3), and (2-6) with the knowledge of the Si-substrate electron-injection electric field E_0, which is determined by the doping profile and depletion width of the p-type Si substrate. By integrating the electric field in both the GaN epi-layer and the Si depletion region, we have the vertical voltage drop across the sample, which is the sample bias voltage. Before significant impact ionization occurs in the GaN epi-layer, the leakage current is limited by the electron generation in the depletion region in the p-type Si substrate. As the bias voltage increases, avalanche breakdown occurs in the GaN epi-layer.

From Figure 2-18, it can be seen that the maximum electric field E_{max} is underneath the contact on the epi-layer surface, where most of the impact-ionization takes place when E_{max} is high enough. As a result, luminance from the edge of the Schottky-contact can be observed, as shown in Figure 2-19 where the image was taken by a CMOS camera mounted to a microscope on top of the device. Since the metal is not transparent to the light, the luminance can only be seen from the metal edges. Due to the limitation of measurement setup, the spectrum of this luminance was not measured.

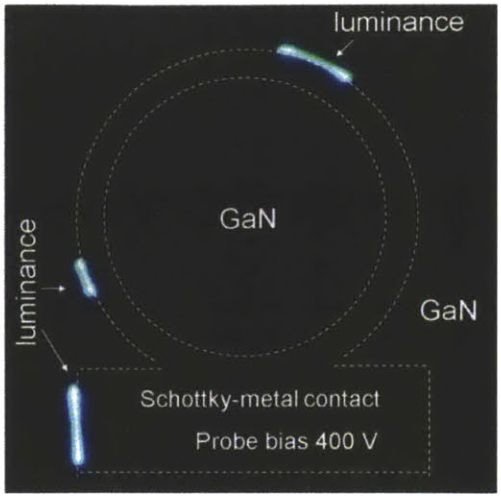

Figure 2-19. CMOS camera image showing the luminance from the edge of an Al-Schottky-contact device biased at about 400 V with respect to the Si substrate measured at room temperature.

However, the model does not readily apply to the positive biased ohmic-contact sample, which shows a much lower vertical leakage onset voltage (100V) than that of the Schottky-contact sample. A few possibilities are considered. First, if we assume the same inversion layer in Si is formed for the ohmic-contact sample as in the Schottky-contact sample, then electron injection from Si substrate at bias voltage of only 100 V would require reducing the distance between the ohmic-contact and the Si substrate to about 0.8-1 μm. This is too small to have a reverse bias breakdown voltage of more than 300 V. Alternatively, if we assume that the metal diffusion from the ohmic contact creates a shorting path for the leakage current, we would also expect a much lower breakdown voltage in the reverse bias measurement.

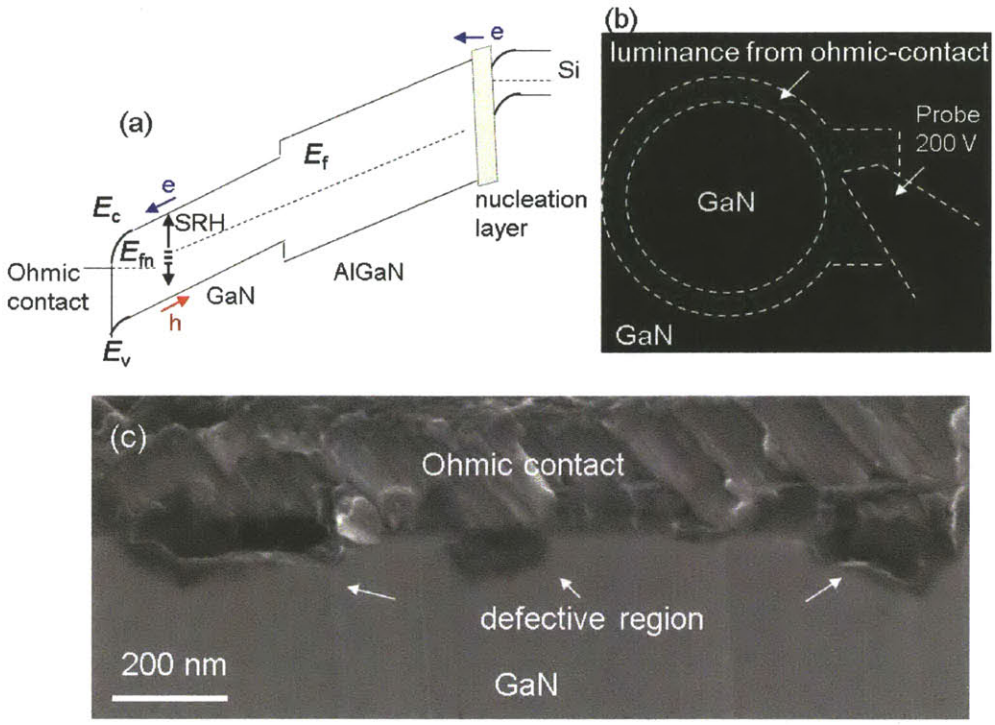

Figure 2-20. (a) Band diagram of forward biased ohmic contact illustrating the SRH generation at defect states created by the ohmic contact; (b) CMOS camera image of luminance from ohmic-contact metal at 200 V bias; (c) Cross-section scan-electron-microscope (SEM) image of the ohmic contact on GaN used in the study.

A possible explanation for the ohmic-contact forward bias leakage current characteristics is shown in Figure 2-20. It assumes SRH electron-hole pair generation in the GaN from the defects created by the ohmic contact formation (see Figure 2-20(c)). The generated holes flow to the Si substrate and induce electron injection from the p-type Si substrate at lower voltage. As shown in Figure 2-20(b), luminance is observed from the ohmic contact biased at 200 V. The luminance is concentrated at the ohmic contact but its intensity is weak compared to the strong luminance from the impact ionization shown in Figure 2-16(d) and Figure 2-19. As a result long camera integration time is required to observe this luminance. Unlike the Schottky-contact case, the luminance is not blocked by the ohmic metal, which has many holes and grains, as seen in the image in Figure 2-20(b). Because of the difficulty to couple this low intensity luminance to a spectrometer, we were not be able to measure the full spectrum of the luminance. However, since the luminance is visible to human eyes, it has

photon energies less than the GaN bandgap energy, which is probably due to the defect luminance of GaN [Reshchikov2005]. The proposed mechanism is also consistent with the positive temperature coefficient of the leakage current in Figure 2-6(a). However, the creation of these defect states by the ohmic contact needs further investigation.

2.3.7 Guideline for the Maximum Breakdown Voltage Design of GaN-on-Si Wafers

Although it has been observed that the buffer breakdown voltage of GaN-on-Si wafers increases with the epi-layer thickness [Selvaraj2009, Ikeda2008, Visalli2009] and the concentration of impurities such as Carbon [Kato2007] and Fe [Choi2006], there has been no attempt to quantitatively model this phenomenon. In this section, we present for the first time a quantitative model for the maximum breakdown voltage of the GaN-on-Si wafers as a function of the epi-layer thickness and trap density. This will provide a guideline for the design of GaN-on-Si wafers, whose buffer breakdown voltage is the upper limit of AlGaN/GaN HEMTs fabricated on the GaN-on-Si wafers.

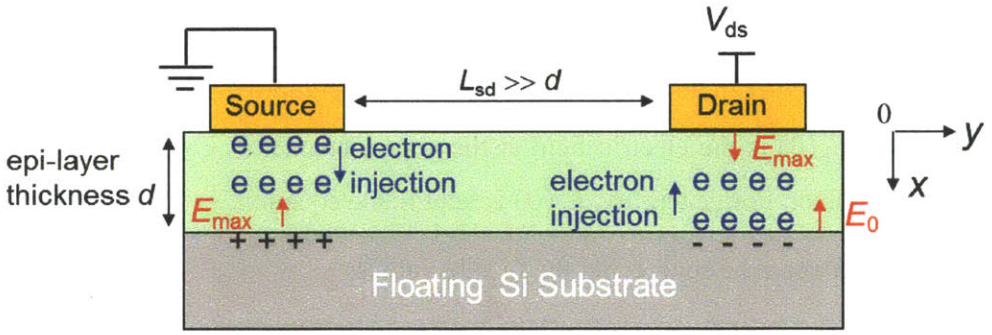

Figure 2-21. Schematic of a buffer-breakdown test structure on a GaN-on-Si wafer with the source-drain distance L_{sd} much larger than the epi-layer thickness d.

Figure 2-21 shows the schematic of a typical buffer-breakdown-test structure on a GaN-on-Si wafer. When the source-drain distance L_{sd} is much larger than the epi-layer thickness d, vertical leakage between the source/drain contacts and the Si substrate limits the maximum breakdown voltage of the GaN-on-Si wafer (see section 2.2). With the Si substrate at a

floating potential, the maximum breakdown voltage between the drain and source contacts is the buffer breakdown voltage of the GaN-on-Si wafer.

We consider the general case in which the epi-layer has an arbitrary trap density distribution of $N_t(x)$, where x is the position coordinate in the vertical direction as shown in Figure 2-21. With floating Si substrate, electrons from the source contact are injected into the epi-layer. Assuming that the density of traps epi-layer is large so that the trapped electrons $n_t(x)$ is much larger the free electron density n.

From Poisson equation, the electric field distribution between the source contact and Si substrate is

$$E_S(x) = E_S(0) + \int_0^x \frac{qn_t(x_1)}{\epsilon_{epi}} dx_1$$

The maximum electric field at the source side is at the bottom of the epitaxial layer (at $x = d$) as shown in Figure 2-21, which has the form of

$$E_{max-source} = E_S(d) = E_S(0) + \int_0^d \frac{qn_t(x_1)}{\epsilon_{epi}} dx_1$$

where ϵ_{epi} is the epi-layer dielectric constant, which can be approximated by GaN dielectric constant of 10.4; $E_S(0)$ is the electric field at the source contact at $x = 0$, which is equal to zero for ohmic contact. For generality, $E_S(0)$ is kept in the equation.

The voltage between the source and the Si substrate is:

$$V_{Si\text{-}source} = \int_0^d E_S(x)dx = E_S(0)d + \int_0^d \left(\int_0^x \frac{qn_t(x_1)}{\epsilon_{epi}} dx_1 \right) dx$$

At the drain side, electrons are injected from the Si substrate. Similar to the source side, the electric field betwee the drain contact and the Si substrate can be derived from the Poisson equation[9]:

---

[9] Here we assume an ideal contact such as the Schottky contact instead of the abnormal ohmic contact which has high leakage current at relatively low forward bias voltage as shown in section 2.3.6.

$$E_{\mathrm{D}}(x) = E_{\mathrm{D}}(d) + \int_{x}^{d} \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1$$

where $E_{\mathrm{D}}(d)$ is the injection electric field from the Si substrate to the epi-layer labelled as E_0 in Figure 2-21.

The maximum electric field at the drain side is underneath the drain contact (at $x = 0$) as shown in Figure 2-21, which has the form of

$$E_{\mathrm{max-drain}} = E_{\mathrm{D}}(0) = E_{\mathrm{D}}(d) + \int_{0}^{d} \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1$$

The voltage between the drain contact and the Si substrate is:

$$V_{\text{drain-Si}} = \int_0^d E_{\mathrm{D}}(x)dx = E_{\mathrm{D}}(d)d + \int_0^d \left(\int_x^d \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1 \right) dx$$

If the TLSC leakage current density (determined by the quasi-Fermi-level position relative to the conduction band edge E_c) is the same in the epi-layer underneath both the source and drain contacts, e.g. by having the same contact area, the trapped electron density $n_t(x)$, determined by Fermi-Dirac distribution, will also be the same in the epi-layer underneath both the source and drain contacts. The drain-source voltage V_{ds} can then be written as

$$V_{ds} = V_{\text{Si-source}} + V_{\text{drain-Si}}$$

$$= E_{\mathrm{S}}(0)d + E_{\mathrm{D}}(d)d + \int_0^d \left(\int_0^x \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1 + \int_x^d \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1 \right) dx$$

$$= \left(E_{\mathrm{S}}(0) + E_{\mathrm{D}}(d) + \int_0^d \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1 \right) d$$

Replacing $E_{\mathrm{S}}(0) = 0$ for the source ohmic-contact and $E_{\mathrm{D}}(d) = E_0$ for the injection electric field from the Si substrate as shown in Figure 2-21, we have

$$V_{ds} = \left(E_0 + \int_0^d \frac{qn_t(x_1)}{\epsilon_{\mathrm{epi}}} dx_1 \right) d = E_{\mathrm{max-drain}} d$$

The maximum electric field at the drain contact is also the overall maximum electric field in the epi-layer. When $E_{\text{max-drain}} = E_{cr}$, we have the maximum breakdown voltage which does not depend on the trap density distribution:

$$V_{\text{bk}} = E_{\text{cr}} d \tag{2-10}$$

In the derivation of the maximum breakdown voltage in equation 2-10, the lateral voltage drop in the Si substrate is much smaller than V_{bk} and therefore is ignored.

From $E_{\text{max-drain}} = E_{cr}$, we also have equation:

$$\int_0^d n_t(x)dx = \frac{\epsilon_{\text{epi}}(E_{\text{cr}} - E_0)}{q} \leq \int_0^d N_t(x)dx$$

where the $\int_0^d N_t(x)dx$ is the areal trap density, which has a minimum value of $\epsilon_{\text{epi}}(E_{\text{cr}} - E_0)/q$ for the maximum electric field in the epi-layer to reach the critical electric field. With $E_0 = 0$ and $E_{\text{cr}} = 3.9$ MV/cm, the areal trap density is around 2.2×10^{13} cm^{-2}.

The minimum required areal trap desnity for the avalanche breakdown is a constant value which decreases when increasing the electron injection electric field E_0 at the Si substrate. However increasing E_0 will reduce E_{cr} which lowers the breakdown voltage. In the extreme case of uniform electric field when $E_0 = E_{\text{cr}}$, the minimum areal trap density is zero and E_{cr} is lowered to 3.1 MV/cm for 2 μm epi-layer thickness (see section 0). Because the change in E_{cr} is smaller than the change in the minimum areal trap density as a function of E_0, increasing E_0 is a good method in reducing the required epi-layer trap density. Since the above derivation does not depend on the trap distribution in the epi-layer, the trap concentration profile can be tailored to avoid the trapping of carriers in the channel layer of transistors fabricated on the wafer with little effect on the maximum buffer breakdown voltage.

The average trap concentration $\widetilde{N}_{\text{t}}$ in the epi-layer is:

$$\widetilde{N}_{\text{t}} \equiv \frac{1}{d}\int_0^d N_t(x)dx \geq \frac{\epsilon_{\text{epi}}(E_{\text{cr}} - E_0)}{qd} = \frac{\epsilon_{\text{epi}}(E_{\text{cr}} - E_0)E_{cr}}{qV_{bk}}$$

which is inversely proportional to breakdown voltage and decreases with higher E_0.

Using the critical electric field of 3.94 MV/cm calculated from section 0 for a linearly increasing electric field, the maximum breakdown voltage as a function of epi-layer thickness and corresponding average trap density is plotted in Figure 2-22.

As shown in Figure 2-22(a), the BV vs. epi-thickness data reported from [Ikeda2009], [Selvaraj2009], [Visali2009] and [Lu2010Apr] are all within the calculated avalanche breakdown limit. Among these data sets, the one from [Ikeda2009] is closest to the calculated limit. It is suspected because of the large amount of carbon doping as high as $10^{19}cm^{-3}$ in the devices reported in [Ikeda2009], the avalanche breakdown condition can be met. The doping density in the devices from [Lu2010Apr] is unknown but is presumably above the required trap density as the reported BV is also very close to the theoretical limit. On the other hand, the data sets from [Visali2009] and [Selvaraj2009] are much lower than the theoretical limit. This is likely due to insufficient trap density in the epi-layer.

As shown in Figure 2-22(b), the average trap density is lower (e.g. 3×10^{16} cm^{-3} for 3 kV breakdown voltage) for high voltage devices. Increasing the injection electric field E_0 also helps to lower the required trap density. It should be mentioned that according to the TLSCII model in section 2.3.4, the trap energy level also plays an important role. If there are only shallow traps, a large leakage current can be carried by free electrons in the conduction band before avalanche breakdown. In order to suppress this leakage current, a trap level of at least 0.5 eV below the conduction band edge is needed to have the leakage current density less than $0.02A/cm^2$ at room temperature.

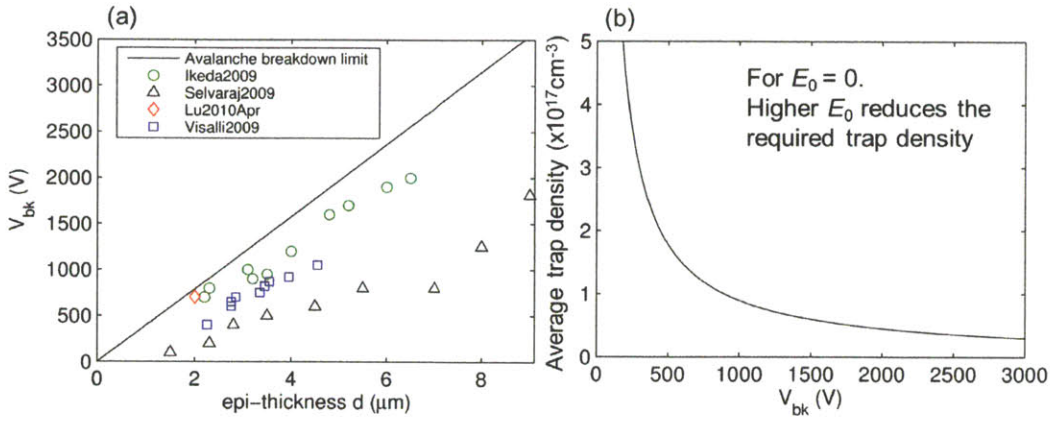

Figure 2-22. (a) Calculated avalanche breakdown voltage as a function of total epi-layer thickness on Si substrate with comparison to literature reported data; (b) Average trap density as a function of avalanche breakdown voltage for zero electron injection field from Si substrate ($E_0 = 0$). Increasing E_0 results in a decreased trap density.

2.4 Schottky-drain Technology

As shown in section 2.3.6, a positive-biased ohmic contact has large leakage to the Si substrate and reduces the transistor breakdown voltage. Figure 2-23 shows the potential of the Si substrate during a typical GaN buffer breakdown measurement. The voltage distribution between the drain and source ohmic-contacts is not uniform. There are higher voltage drops between the Si substrate and source contacts than between the drain and the Si substrate. This is due to the abnormal ohmic leakage current characteristics described in section 2.3.6. We have also shown in section 2.3.6 that the Schottky contact has higher vertical breakdown voltage. As a result, we have proposed the use of a Schottky-drain technology to improve device breakdown voltage [Lu2010Apr].

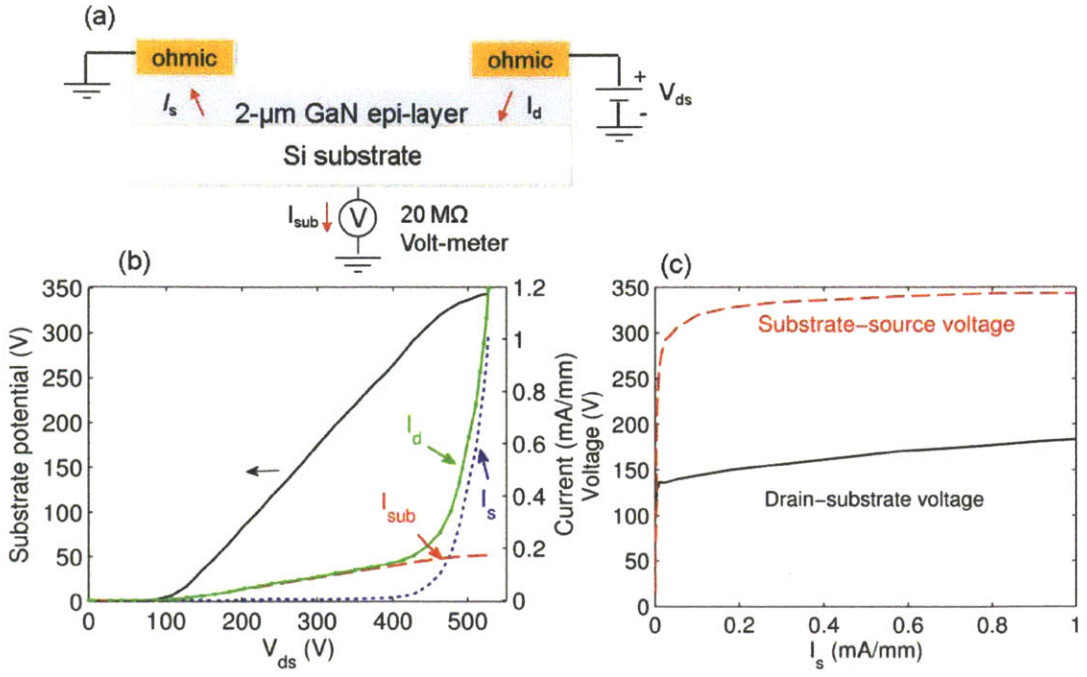

Figure 2-23. Si substrate potential measurement: (a) schematic of the measurement setup; (b) measured substrate potential as a function of V_{ds} with three leakage current components; (c) voltage distribution among the source, drain and Si substrate.

2.4.1 Device Fabrication

Both Schottky-drain and conventional ohmic-drain HEMTs were fabricated on the same wafer used in the study of vertical leakage measurement in section 2.3. The total epi-layer thickness is 2 μm. For the conventional HEMTs, Ti/Al/Ni/Au alloyed ohmic source and drain contacts were formed after 870 °C annealing for 30 s in N_2 atmosphere. In the Schottky-drain HEMTs, unannealed Ti/Au metallization was used for the drain contact. Prior to this metallization, a 10 nm recess was performed on the $Al_{0.26}Ga_{0.74}N$ barrier by low energy BCl_3/Cl_2 plasma in an electron cyclotron resonance (ECR) system to reduce the series resistance and turn-on voltage of the Schottky-drain contacts. Then, 150 nm mesa isolation was achieved by BCl_3/Cl_2 plasma etching. Finally, Ni/Au/Ni Schottky gates were formed by evaporation. Both the ohmic-drain and Schottky-drain devices were simultaneously fabricated on the same wafer and in very close proximity from each other. These devices have a gate length (L_g) of 2 μm, gate-to-source spacing (L_{gs}) of 1.5 μm and gate-to-drain

spacing (L_{gd}) varying from 5 to 20 μm. For the buffer breakdown characterization, no gate was formed between the source and drain contacts.

2.4.2 DC Characterization

Figure 2-24 shows the effect of the 10-nm recess in AlGaN on the Schottky contact characteristics. Not-only the differential resistance of the Schottky contact is improved but also the turn-on voltage is reduced. Because the AlGaN layer has high resistance, the thinner AlGaN layer in the recessed Schottky contact results in the reduced differential resistance. The reduction in turn-on voltage could be due to the changing in the Fermi-level pining positions at the Ti/AlGaN Schottky interface after the recess etching which results in a reduced Schottky barrier height.

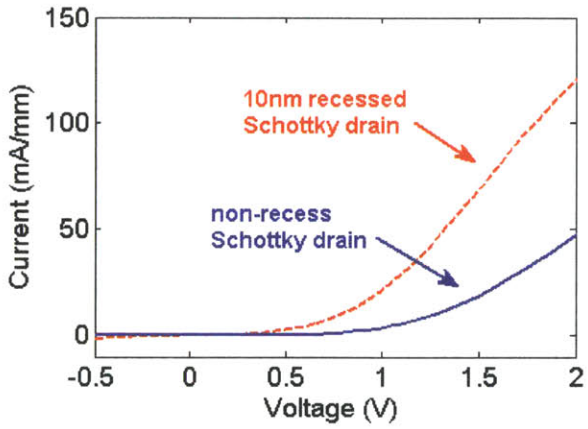

Figure 2-24. : I-V characteristics of Schottky-drian contact with and without recess etching on AlGaN.

The buffer lateral breakdown voltage of the ohmic-drain and the Schottky-drain devices was measured in structures where a 150 nm-deep recess was performed between the source and drain contacts to eliminate the 2DEG (inset in Figure 2-25(a)). The Si substrate was floating during the measurement. Figure 2-25(a) shows the typical lateral breakdown I-V curves of a conventional ohmic-drain and a Schottky-drain devices with 14 μm source-to-drain distance (L_{sd}). The Schottky-drain device shows 150 V higher breakdown voltage (at drain leakage current of 1 mA/mm) than the ohmic-drain device, reaching 700 V, which is

close to the predicted maximum breakdown voltage on 2 μm epi-layer-on-Si wafer in section 2.3.7. Figure 2-25(b) shows the breakdown voltages for different source-to-drain distances. Vertical current leakage from the GaN buffer to the Si substrate causes the breakdown voltage saturation.

The three-terminal breakdown voltages of the ohmic-drain and Schottky-drain HEMTs were measured at V_{gs} = -8 V, enough to pinch off the devices which have a threshold voltage of -2 V. On average, the Schottky-drain devices show more than 100V higher breakdown voltage than the ohmic-drain devices.

Due to the turn-on voltage of the Schottky contact, the on-resistance of the Schottky-drain transistors is higher than the standard ohmic-drain transistors for breakdown voltage below 400 V (Figure 2-25(b)). Because the Schottky-drain transistors can achieve the same breakdown voltage as the ohmic-drain HEMTs with shorter gate-to-drain spacing, they have lower specific R_{on} than the standard HEMTs for V_{bk} > 400 V. Some of the applications where these unidirectional devices could be used include Silicon-Controlled-Rectifier (SCR) or Gate-Turn-Off thyristors (GTO).

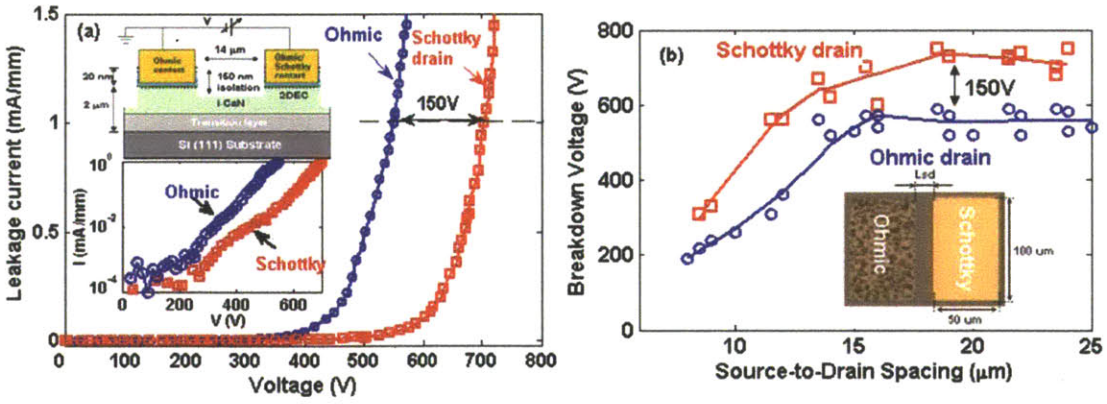

Figure 2-25. (a) Buffer lateral leakage current of the ohmic-drain and Schottky-drain devices with 14 μm contact spacing; The inset shows the leakage current in semi-log scale and the measurement configuration; (b) buffer lateral breakdown voltage as a function of source-to-drain spacing.

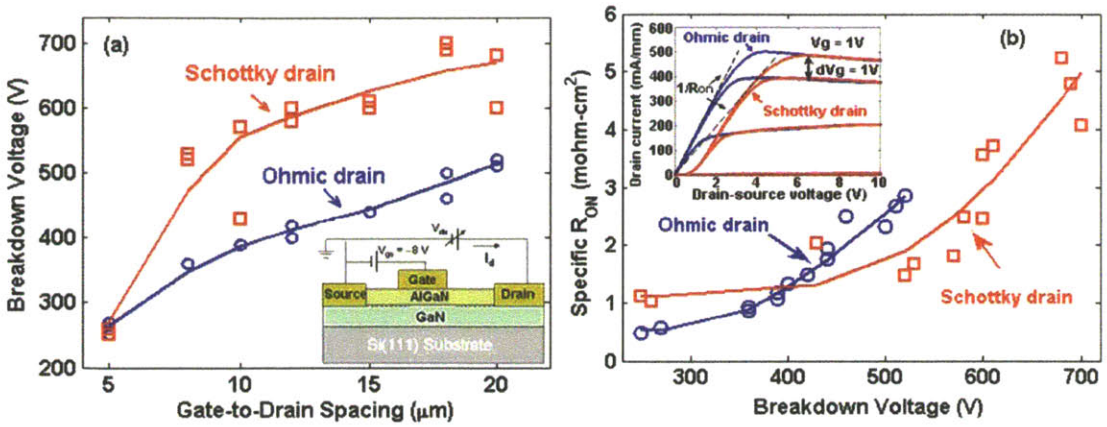

Figure 2-26. (a) Three-terminal breakdown voltages as a function of gate-to-drain distances; (b) Specific R_{on} as a function of breakdown voltages. The inset picture is the I-V curves of the ohmic-drain and Schottky-drain devices with L_g = 2 μm, L_{gs} = 1.5 μm and L_{gd} = 10 μm.

2.5 Si Substrate Removal Technology

It is shown in section 2.3.7 that the avalanche breakdown voltage of GaN-on-Si wafers is proportional to the epi-layer thickness. For example, to have a breakdown voltage of 1200 V, at least 3 μm epi-layer is needed with a minimum trap density of 7×10^{16} cm^{-3}. However the growth of thick buffer on Si substrate can cause large wafer bow, cracking in GaN film, and high thermal resistance, while the incorporation of carbon and iron in the buffer can cause the carrier trapping in AlGaN/GaN HEMTs [Klein2001 and Rudzinski2006], which increases device dynamic on-resistance (see Chapter 4).

In this section, a new substrate-transfer technology will be presented. By transferring AlGaN/GaN HEMTs onto an insulating substrate, the limitation of the Si substrate can be eliminated.

2.5.1 Device Fabrication

As shown in Figure 2-27(a), standard AlGaN/GaN HEMTs were first fabricated on the same AlGaN/GaN-on-Si wafer as in section 2.3. After the Ti/Al/Ni/Au ohmic contacts formation, mesa isolation and Ni/Au/Ni gate deposition, the top surface of the sample (Ga face) was bonded to a Si carrier wafer by adhesive bonding method with Benzocyclobutene (BCB) as the adhesive layer (Figure 2-27(b)). The sample surface was planarized after

spinning on a thick layer of BCB and compressing it onto the Si carrier wafer at temperature of 130 °C to force the reflow of BCB. The sample was then cured at 250 °C for 1 hr to harden the BCB. After bonding to the carrier wafer, the Si(111) substrate where the epi-layer is grown on was removed by SF_6 plasma etching, exposing the N-face surface of the 2-μm-thick GaN/AlGaN buffer. In order to have access to the ohmic and gate contacts at the Ga-face surface, the exposed N-face surface of the sample was then bonded to a glass wafer with BCB using the same method (Figure 2-27(c)). Finally the Si carrier wafer was released by SF_6 and SF_6/O_2 plasma etching as shown in Figure 2-27(d). At this point, the standard AlGaN/GaN HEMTs have been successfully transferred to the insulating glass substrate.

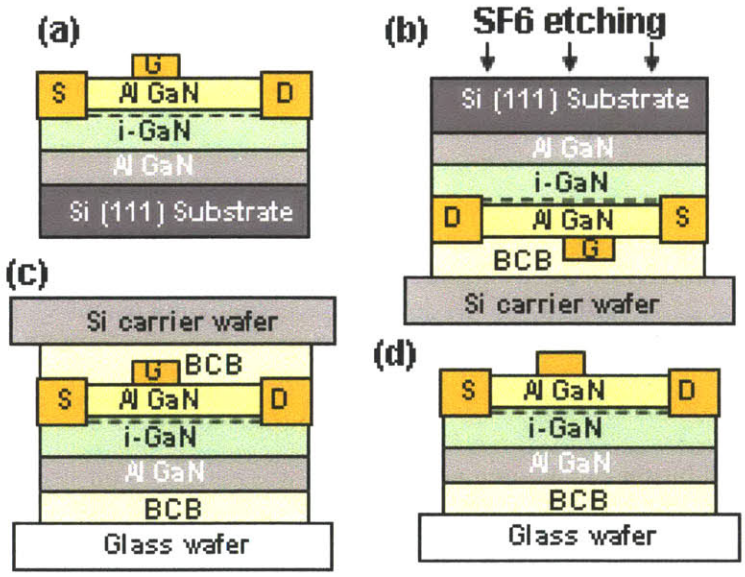

Figure 2-27. Process flow of the substrate transfer technology. (a) Standard AlGaN/GaN HEMTs are fabricated; (b) Device surface is bonded to a Si carrier wafer and Si (111) substrate is removal by SF_6 plasma etching; (c) the N-face surface of the exposed GaN/AlGaN buffer is then bonded to a glass wafer; (d) After releasing the Si carrier wafer, the device is successfully transferred to the glass wafer.

2.5.2 Device Characterization

The DC characteristics of an AlGaN/GaN-on-glass HEMT after the substrate transfer are compared with that of an AlGaN/GaN-on-Si HEMT before the substrate transfer in Figure

2-28(a). The maximum drain current of the AlGaN/GaN-on-glass HEMT drops by about 35% and the self-heating effect becomes more sever, which is due to the high thermal resistance of the BCB bonding material and the glass substrate. As shown in Figure 2-28(b), reducing the measurement temperature and applying pulsed drain bias increases device maximum current.

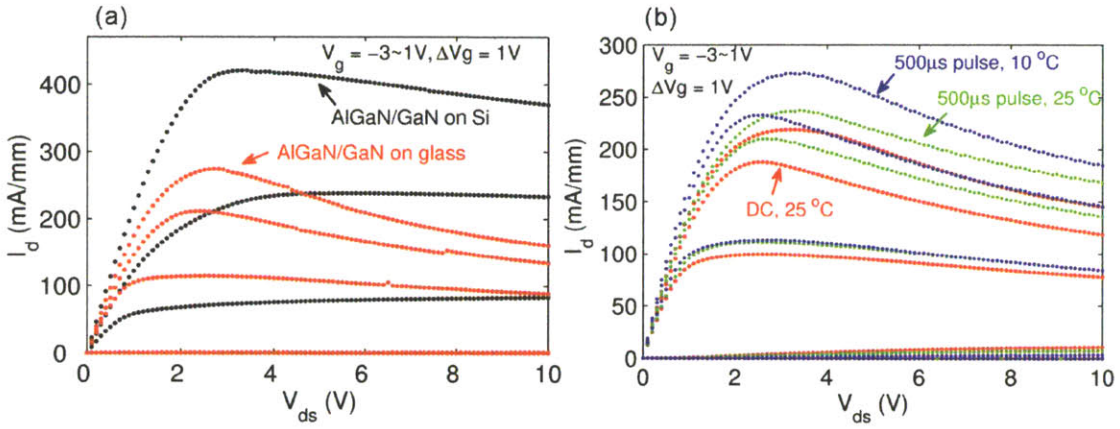

Figure 2-28. (a) I_d-V_d characteristics of AlGaN/GaN-on-glass after the substrate transfer and of AlGaN/GaN-on-Si before substrate transfer measured in DC bias condition; (b) I_d-V_d characteristics of an AlGaN/GaN-on-glass device measured at DC and 500-μs/200-ms drain pulse conditions at 25 °C and 10 °C. All devices have same dimensions with L_g = 2 μm, L_{gs} = L_{gd} = 1.5 μm.

The two-terminal buffer breakdown voltage (V_{bk}) was measured on structures where source and drain contacts were isolated by 150-nm-deep BCl_3/Cl_2 plasma etching as shown in Figure 2-29. The breakdown voltage is defined as the voltage when the leakage current reaches 10 μA/mm. As shown in Figure 2-29, the breakdown voltage of the devices on the Si substrate saturates at 500 V. Without vertical leakage path, the devices transferred to the glass substrate show no breakdown voltage saturation.

By fitting the data of V_{bk} as a function of L_{sd} in the devices transferred to the glass wafer, a power law relation $V_{bk} \sim L_{sd}^{1.5}$ is extracted with the exponential coefficient in a 95% confidence bound of (1.38, 1.62). This dependence seems to suggest the space-charge-limited (SCL) current in low field mobility regime (see section 2.3.2), where the current can be expressed as $J = 9\varepsilon\mu V^2/8L^3$ (ε_s is the dielectric constant; μ is carrier mobility; V is applied

voltage, and L is the distance between the two contacts). After rearranging, $V = \sqrt{8J/9\epsilon\mu}L^{1.5}$, where voltage and the distance between two contacts has a power law relation for a constant current. However, the lateral electric field between the two contacts is too high to satisfy the assumption of the low field mobility for GaN. On the other hand, carrier transport on semiconductor surface is not the same as in the bulk (the case in the vertical leakage measurement). The dangling bonds and contaminants on the surface can result in large number of localized states which resemble the organic semiconductor, where carrier transport is by hopping from one site to another. It could be possible that the breakdown voltage measured in Figure 2-29 is surface leakage current limited. More experiment data are needed to confirm the presence of the SCL current and test the hypothesis of surface leakage.

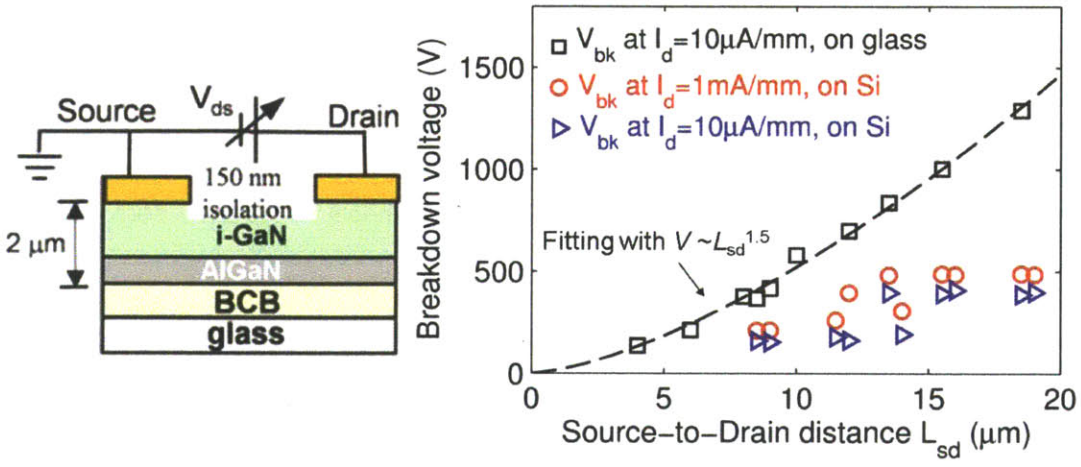

Figure 2-29. Two-terminal buffer breakdown voltage as a function of L_{sd} of devices before and after being transferred to a glass wafer. The data of the device transferred to the glass substrate can be fitted with a power law to the order of 1.5.

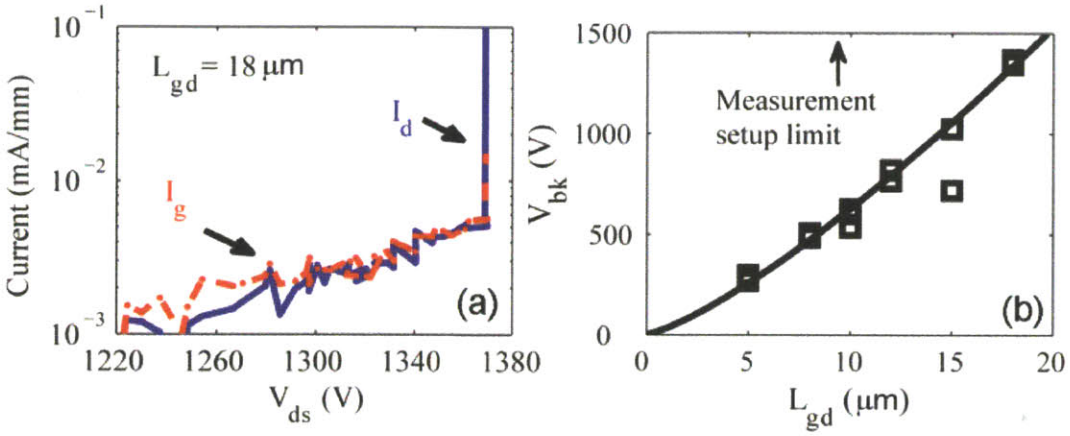

Figure 2-30. a) Three-terminal leakage current for an AlGaN/GaN HEMT on glass with L_{gd} = 18 μm at V_{gs} = - 8 V. For V_{ds} < 1220 V, the leakage current is below the sensitivity of the measurement setup (1 μA/mm). (b) Three-terminal V_{bk} as a function of L_{gd}.

The three-terminal V_{bk} of the AlGaN/GaN-on-glass HEMTs was measured at V_{gs} = -8 V. As shown in Figure 2-30(a), a device with L_{gd} = 18 μm shows a V_{bk} of 1370 V at I_d = 10 μA/mm. As the drain-to-source leakage is negligible, the drain-to-gate leakage limits the breakdown in these devices. V_{bk} as a function of L_{gd} is shown in Figure 2-30(b). More than 1500 V breakdown can be achieved.

To further improve this technology, substrates with higher thermal conductivity such as amorphous AlN can be used. Other bonding material which can provide better thermal conduction than the BCB but also have good electrical isolation needs to be investigated.

2.6 Conclusion

Vertical current conduction in the Nitride-semiconductor epi-layer between the Si substrate and device contact limits the maximum attainable breakdown voltage in AlGaN/GaN transistors grown on Si substrates. The study in this chapter explains for the first time this vertical conduction mechanism with a new trap-limited space-charge impact-ionization model. The vertical current is caused by electron injection from device contact (in negative contact bias condition) or the Si substrate (in positive contact bias condition). The injected electrons also create an electric field distribution in the epi-layer, which induces impact ionization when the electric field strength is large enough (above 2.5 MV/cm). Traps

in the epi-layer play an important role in changing the electron quasi-Fermi level positions. High density deep traps reduce free electrons in the conduction band, suppressing vertical leakage current until impact ionization occurs. The TLSC model developed in the velocity saturation regime is useful to extract trap energy levels. Combining the TLSC model with the impact ionization, the TLSCII model, can be used to calculate the maximum breakdown voltage of a GaN-on-Si wafer. It is derived that the maximum buffer breakdown voltage in a GaN-on-Si wafer is proportional to its epi-layer thickness and it does not depend on the impurity doping profile. The minimum impurity areal density is a constant and as a result, its volume concentration is inversely proportional to the breakdown voltage. Literature data are compared with the prediction and showed a good agreement.

An injection-rate-limited model was also developed to describe the electron injection from p-type Si substrate, which can be limited by the electron generation rate in the depletion region of the p-type Si substrate.

Asymmetric leakage current is observed on ohmic contact depending on its bias voltage polarity. The leakage current is much higher for positive bias than negative bias on the ohmic contact. It is suspected that it is due to the defect states created by the ohmic metal annealing which form the SRH generation centers.

With the understanding of the breakdown mechanism, two device technologies are developed to increases the GaN-on-Si device breakdown voltages. The Schottky-drain technology integrates an AlGaN/GaN Schottky-diode in series with an AlGaN/GaN HEMT by replacing the drain ohmic-contact with a Schottky-contact to eliminate the high leakage current associated with the drain ohmic contact. A new substrate-transfer technology has also been developed. By removing the Si substrate and transfer the GaN epi-layer onto an insulating substrate, the breakdown voltage characteristics of GaN transistors is significantly improved.

Chapter 3 Normally-off GaN Transistors

This chapter presents three novel transistor structures—an integrated dual-gate structure, a tri-gate structure and a GaN-etch-stop structure—for high performance normally-off GaN transistors. Device design, fabrication and measurement results are presented. Device physics of each structure is analyzed from the measurement data and simulation.

3.1 Introduction

Due to the polarization-induced 2DEG, AlGaN/GaN HEMTs typically have a negative threshold voltage, thus being depletion-mode (D-mode or normally-on) devices. To use these transistors in power electronics applications, an additional negative power supply or a normally-off transistor in a cascode configuration are needed in the circuit (Figure 3-1). Both of these approaches greatly increase the complexity and cost of power electronic circuits. Therefore normally-off enhancement-mode (E-mode) GaN transistors are highly desirable. In addition, normally-off transistors also increase the system reliability and safety by reducing the chances of short circuit.

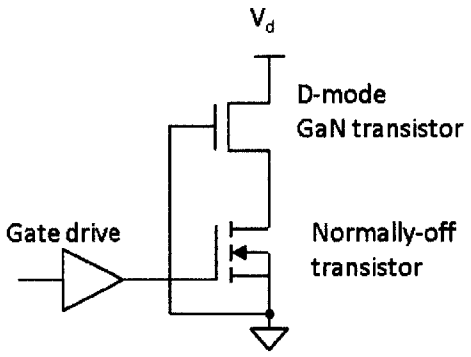

Figure 3-1. Circuit schematic of a D-mode GaN transistor in a cascode configuration with a normally-off transistor.

3.2 Review of Normally-off GaN Transistor Technologies

Several technologies to fabricate normally-off GaN transistors have being proposed in the literature. For example, following the conventional CMOS technology, GaN n-channel MOSFETs fabricated on p-type GaN buffer can achieve normally-off operation [Irokawa2004, Huang2006]. However, due to the high annealing temperature of Si implants in GaN [Cao1998] and poor electron mobility in the channel inversion layer, these devices are difficult to fabricate and have very high on-resistance. With high electron mobility and charge density, the AlGaN/GaN heterostructure has a great potential for high performance normally-off transistors. In this section, four types of AlGaN/GaN-based normally-off technologies shown in Figure 3-2 are reviewed.

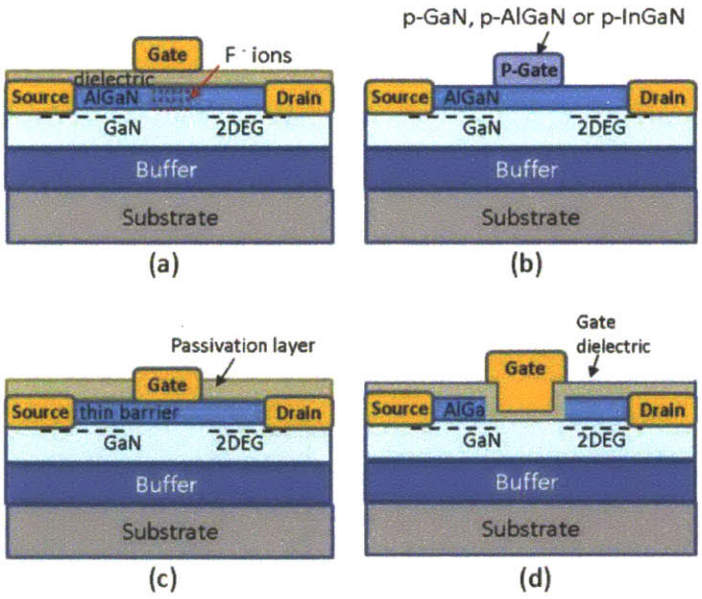

Figure 3-2. Normally-off AlGaN/GaN transistors fabricated by: (a) fluorine-treatment technology, (b) p-type gate technology, (c) surface potential engineering technology, and (d) gate-recess technology.

3.2.1 Fluorine-treatment Technology

Fluorine-based plasma treatment underneath the gate region has been used to make E-mode AlGaN/GaN HEMTs [Cai2005, Chu2011], as shown in Figure 3-2(a). It is believed that the negatively charged fluorine ions F^- introduced into the AlGaN layer during the fluorine-based plasma treatment on the surface deplete the 2DEG in the channel, converting the D-mode AlGaN/GaN HEMT into an E-mode device [Yuan2008]. Thermal stress studies showed the F-plasma treated E-mode AlGaN/GaN HEMTs are stable at 200 °C for more than 80 days [Mizuno2007]. At higher temperatures, negative shifts of threshold voltage are observed [Wang2009]. Threshold voltage instability in high field stress and gate over-drive conditions has also been reported in these devices [Yi2007, Ma2010]. Other than the Fluorine plasma, E-mode AlGaN/GaN HEMTs by hydrogen-plasma treatment have also been demonstrated, however they show similar threshold voltage instability issues [Lu2009].

3.2.2 P-type Semiconductor Gate Technology

Another type of normally-off E-mode AlGaN/GaN HEMTs is the p-GaN, p-AlGaN or p-InGaN gated AlGaN/GaN transistors [Hu2000, Suh2006a, Uemoto2007, Shimizu2008], as shown in Figure 3-2(b). Due to the built-in potential between the p-type gate and the channel, the 2DEG underneath the gate is depleted at zero gate bias, forming a normally-off transistor. However, in order to have high threshold voltage, the thickness of the AlGaN barrier and its Al composition are limited due to its polarization charges which cause negative shifts of flat band voltage. In order to have a positive threshold voltage with a p-GaN gate, the maximum negative shifts caused by the AlGaN polarization should be less than the GaN band gap of 3.42 eV. For example, to have a threshold more than 1 V, $Al_{0.26}Ga_{0.74}N$ thickness should be less than 10 nm. As a result there is a trade-off between the device access resistance and the threshold voltage: low access resistance with high 2DEG density outside the gate results in low threshold voltage, while high threshold voltage results in high access resistance. These devices also have limited gate voltage swing because of large forward gate leakage current when the gate-to-channel p-n junction is turned-on. As a result, threshold voltage above 1 V and high device current density are difficult to achieve in this structure.

3.2.3 Surface Potential Engineering Technology

A third approach to fabricate E-mode devices is by changing the surface potential of the AlGaN barrier with dielectrics [Ohmaki06, Higashiwaki07, Medjdoub10], as shown in Figure 3-2(c). It has been observed that the deposition of a thin dielectric on the surface of AlGaN/GaN HEMTs increases their 2DEG density [Green00, Arulkumaran04]. The E-mode transistors fabricated by this approach start with a very thin AlN or AlGaN barrier layer structure such that there is almost no 2DEG at the heterojunction interface. Then the surface of these devices is covered with a passivation dielectric layer except the gate region to increase the 2DEG in the access regions outside of the gate. Since the change of surface potential by the deposition of dielectric layer is limited, the major drawbacks of this technology are its marginal positive threshold voltage and very low voltage swing. Reproducibility of the surface potential is also a potential problem.

3.2.4 Gate-recess Technology

Since the 2DEG in the AlGaN/GaN HEMTs is induced by the net polarization charge at the heterojuction [Ambacher2000] and its density depends on the AlGaN barrier thickness [Ibbetson00], recess-etching of the AlGaN barrier in the gate region reduces the density of 2DEG and shifts the device threshold voltage to positive values [Lanford05, Saito06]. There has been a great progress in recessed-gate E-mode AlGaN/GaN HEMTs. Combing the gate recess with gate dielectric (Figure 3-2(d)), devices with threshold voltage larger than 2 V have been demonstrated [Oka2008, Kanamura2010, Lu2010Sep1]. The recessed-gate metal-insulator-semiconductor HEMTs (MIS-HEMTs) have low gate leakage and high drain current density [Kanamura2010, Im2010, Lu2010Sep1] thanks to the gate dielectric and large forward gate-bias capability.

Despite the advantages of recessed-gate E-mode AlGaN/GaN MIS-HEMTs over other technologies, there are also several challenges. One of the major challenges is in gate recess etching. Because of the need for directionality in gate recess, chlorine-based plasma dry-etch is commonly used to recess the AlGaN barrier [Pearton1993, Buttari2003]. The plasma dry-etch damages the semiconductor surface, increases surface roughness and reduces channel electron mobility. Another concern is the uniformity of dry etching across a wafer and among different batches of wafers. Variations in recess depth cause non-uniformity in the threshold

voltages of the recessed-gate AlGaN/GaN transistors. The control of dielectric-semiconductor interface quality also poses a great challenge. The gate-dielectric/normally-off-channel interface trap density has a tremendous impact on device performance. High interface trap density causes large hysteresis in the device threshold voltage and reduces carrier density in the channel.

In this thesis, new transistor structures are developed to address the major challenges in the recessed-gate E-mode AlGaN/GaN MISFETs. In section 3.3, a dual-gate normally-off AlGaN/GaN MISFET is presented. By integrating an E-mode sub-micron recessed-gate GaN transistor with a high voltage D-mode AlGaN/GaN HEMT, the dual-gate transistor minimizes the impact of the poor channel mobility in the recessed-gate region without compromising the overall device breakdown voltage and threshold voltage. In section 3.4, a tri-gate E-mode AlGaN/GaN MISFET is presented, which has more than two orders of magnitude reduction in the device off-state leakage, demonstrating a truly normally-off operation. In section 3.6, an etch-stop barrier structure is presented, which significantly improves the recess-etching uniformity, dielectric/semiconductor interface quality and effective channel mobility. Electrostatic, piezoelectricity and CV simulations of these new device technologies are performed to understand their device physics.

3.3 Dual-gate Normally-off GaN Transistors

Due to the dry etching damage, recessed-gate normally-off MIS-HEMTs have low channel mobility. For example, the maximum channel mobility of GaN MISFETs reported in the literature is in the range of 120-225 $cm^2V^{-1}s^{-1}$ [Oka2008, Im2010], which is 7-10 times smaller than the 2DEG mobility in AlGaN/GaN HEMTs. As a result, high channel R_{ch} has a large impact in the total on-resistance of these recessed-gate normally-off MIS-HEMTs. Because R_{ch} is proportional to the gate length L_g with $R_{ch} = L_g / \mu_e n_{sh}$, shrinking the recessed-gate length can effectively reduce the impact of the channel resistance. However, transistors with short channel length have low breakdown voltages due to the drain-induced-barrier-lowering (DIBL) effect, causing punch-through leakage between the drain and the source.

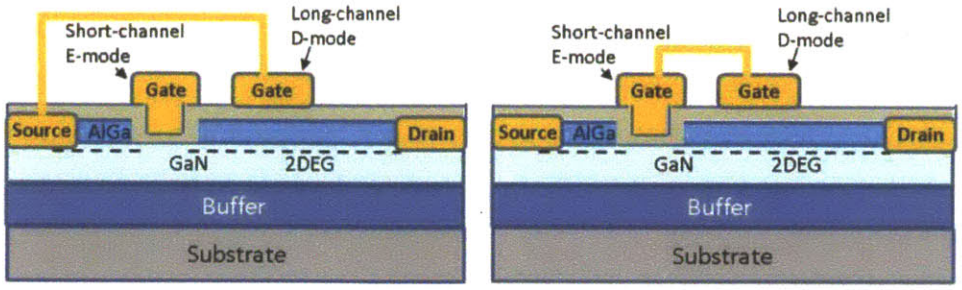

Figure 3-3. Dual-gate normally-off AlGaN/GaN transistor designs in two different gate configurations.

A dual-gate structure is designed in order to reduce the channel resistance while maintain high breakdown voltage. As shown in Figure 3-3, a short-channel E-mode gate is in cascode configurations with a long-channel D-mode gate. Since the E-mode channel length is short, its impact on the total resistance is small. In the off-state at V_{gs} = 0 V, the 2DEG underneath the D-mode gate is depleted because of the self-biasing effect due to the cascode normally-off channel at the source side. As a result, the normally-off channel is shielded by the D-mode gate from high drain voltage and only sees the pinch-off voltage of the D-mode gate.

When the two gates are connected together (Figure 3-3 right), the structure can be further simplified as shown in Figure 3-4. Silvaco-ATLAS device simulation of potential profile shows the screening effect of the D-mode gate. At V_{ds} = 100 V, there is only 3.1 V dropped across the E-mode channel. To design this device correctly, the D-mode gate pinch-off voltage $V_{\text{pinch-off}}$ has to be smaller than the punch-through voltage of the E-mode channel $V_{\text{punch-through}}$.

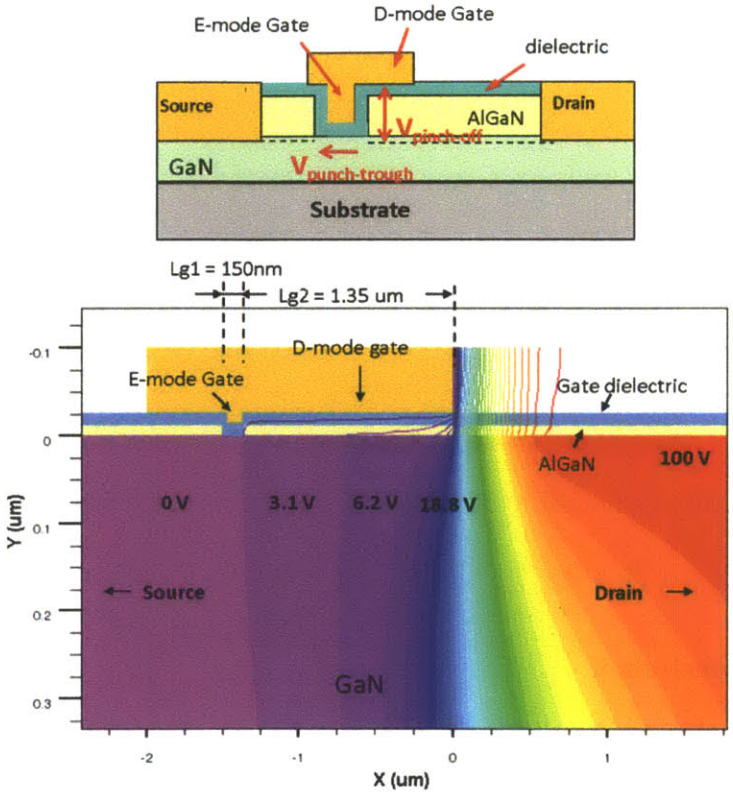

Figure 3-4. Schematic of integrated dual-gate normally-off transistor and simulation of potential profile at drain voltage of 100 V.

3.3.1 Device Fabrication

The normally-off integrated dual-gate transistors were fabricated on a 17 nm $Al_{0.26}Ga_{0.74}N$/GaN heterostructure grown on 4 inch Si (111) substrate with a total epi-thickness of 2 μm. After the standard Ti/Al/Ni/Au alloyed ohmic contacts and mesa isolation etching, a short E-mode gate (L_g = 95±10 nm) was patterned with electron beam lithography and the AlGaN barrier was fully recessed with low damage BCl_3/Cl_2 plasma etching. 14 nm Al_2O_3 gate dielectric was then deposited by atomic layer deposition followed by 90 s rapid thermal anneal in N_2 atmosphere at 700 °C. Finally, a 2-μm-long Ni/Au/Ni gate was deposited overlapping with the first gate-recess region. The 2 μm gate was shifted 1 μm towards the drain side (as shown in the SEM image in Figure 3-5) to support the drain voltage and the gate metal was annealed at 500 °C for 3 min. The transistors have a gate width of 100 μm and a gate-to-source spacing (L_{gs}) of 2 μm with gate-to-drain spacing (L_{gd})

varying from 5 μm to 18 μm. Standard D-mode transistors were also fabricated at the same time as a reference on the same sample without the gate recess.

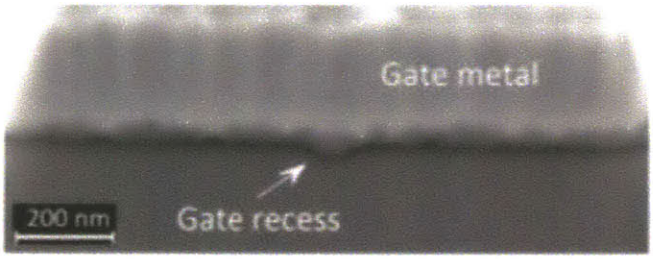

Figure 3-5. Cross-section SEM image of the gate recess in the dual-gate normally-off transistor.

3.3.2 DC Characterization

The DC characteristics of a normally-off dual-gate device with L_{gd} = 5 μm are shown in Figure 3-6. The device has a maximum drain current of 434 mA/mm at V_{gs} = 7 V of the E-mode dual-gate device is 434 mA/mm and a threshold voltage of 2.9 V (extracted from transconductance g_m-linear extrapolation [Tsuno1999]). The D-mode device has a threshold voltage of -3.5 V. Due to the D-mode gate screen effect, 3.5 V will be the maximum voltage drop across the 95 nm normally-off channel in the integrated dual-gate transistor. The maximum transconductances (g_m) of the integrated dual-gate E-mode transistor and standard D-mode transistor are 143 mS/mm and 134 mS/mm respectively. The rolling-off of the g_m after the peak value is caused by voltage drop on the source-access resistance and mobility degradation at high forward gate bias voltages [Sun1980, Smorchkova1999]. Despite the degraded MIS-interface mobility, the E-mode transistor still has slightly higher g_m due to the small E-mode gate length and closer gate-to-channel distance.

The I_d-V_{ds} characteristic of the dual-gate transistor has two knee voltages as shown in Figure 3-6(a), which is a unique feature for the dual-gate operation. The first knee voltage is at $V_{ds} = V_{gs} - V_{th,E\text{-}mode}$, where $V_{th,E\text{-}mode}$ = 2.9 V is the E-mode gate threshold voltage. The second knee voltage is at $V_{ds} = V_{gs} - V_{th,D\text{-}mode}$, where $V_{th,D\text{-}mode}$ = -3.5 V is the D-mode gate

threshold voltage. The output conductance between the knee-voltages is due to the short channel effect of the 95 nm E-mode channel.

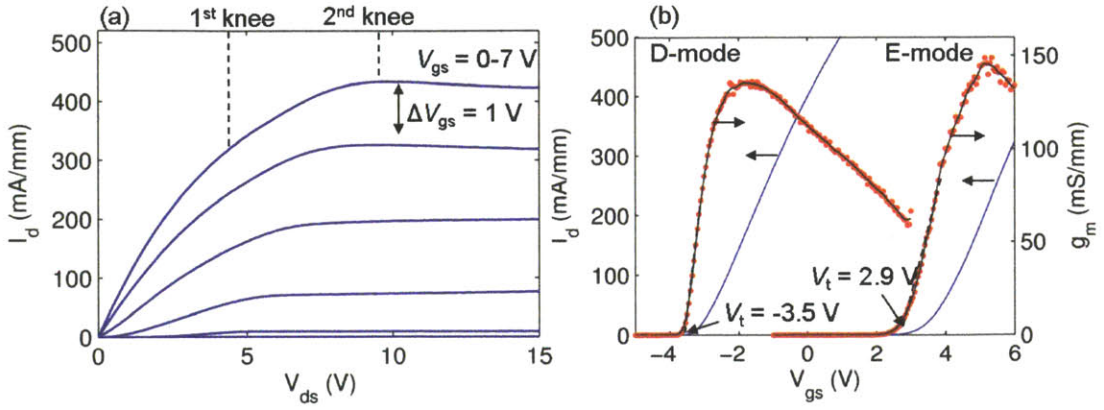

Figure 3-6. (a) I_d-V_{ds} characteristics of an integrated dual-gate E-mode device with L_{gd} = 5 μm; (b) Transfer characteristics of the E-mode device compared to a D-mode device of the same structure without gate recess. The E-mode device is biased at V_{ds} = 12 V and the D-mode device is biased at V_{ds} = 10 V

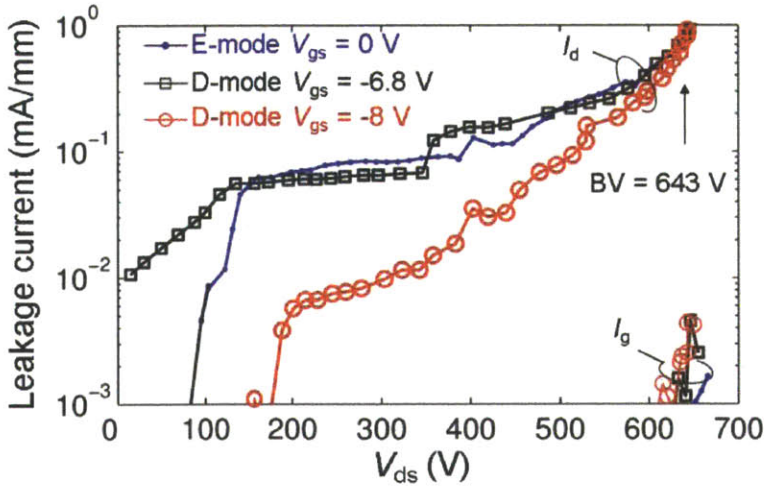

Figure 3-7. Three-terminal breakdown measurement of an E-mode device at V_{gs} = 0 V and a D-mode device at V_{gs} = -8 V and -6.8 V. Both devices have L_{gd} = 8 μm. The current resolution in the measurement setup is 1 μA/mm.

A maximum 643 V three-terminal breakdown voltage (defined at I_d = 1 mA/mm with V_{gs} = 0 V) is measured on a dual-gate E-mode device with L_{gd} = 18 μm as shown in Figure 3-7. Its specific on-resistance ($R_{sp,on}$) is 4.3 mΩ•cm^2. The breakdown characteristics of a standard D-mode device with the same L_{gd} biased at V_{gs} = -8 V and -6.8 V are compared with that of the E-mode device in Figure 3-7. Both the E-mode and D-mode devices have the same breakdown voltage at I_d = 1 mA/mm, which is limited by the Si substrate (See Chapter 3). However, the E-mode device has higher drain leakage current than the D-mode device biased at V_{gs} = -8 V (with $V_{gs} - V_{th}$ = -4.5 V) but has a similar leakage current plateau when the D-mode device is biased at -6.8 V (with $V_{gs} - V_{th}$ = -3.3 V). As a result, it is suspected the relatively high leakage current plateau (0.1 mA/mm) is due to a parasitic parallel leakage path underneath the channel. The energy barrier in the E-mode channel at V_{gs} = 0 is insufficient to block this leakage. In fact, this problem is also observed in other normally-off GaN transistors reported in the literature [Suh2006b, Oka2008, Kanamura2010]. As shown in section 3.4, the leakage current is reduced by using a 3D tri-gate structure with improved gate control of the channel.

3.3.3 Characterization of Recessed-gate Channel

To study the damage induced by the gate recess, devices with different recessed gate lengths have been fabricated. Figure 3-8 shows the on-resistance of these devices, calculated from the *I-V* characteristics at V_{gs} = 7 V, as a function of recessed-gate length. E-mode channel sheet resistance of 32.5 kΩ/sq is extracted from the slope of the curve, which is 70 times of the 2DEG sheet resistance (470 Ω/sq) of the D-mode device. However, because of the small recessed-gate length (95 nm), the E-mode channel contributes only 17% of the total device resistance of E-mode device with a breakdown voltage of 643 V. This demonstrates that dual-gate structure allows the decoupling of the E-mode operation region (E-mode gate) from the voltage blocking region (D-mode gate), which significantly improves the overall device on-resistance and the maximum current.

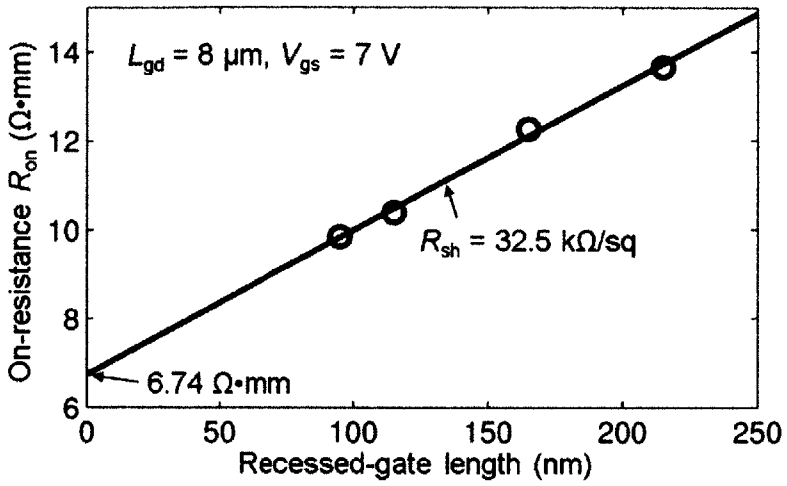

Figure 3-8. R_{on} as a function of recessed-gate lengths. The extrapolation to zero recessed-gate length gives a resistance of 6.74 ohm-mm, which is the R_{on} (6.76 Ω-mm at V_{gs} = 7 V) of a standard D-mode device with the same dimensions.

The field-effect electron mobility of the dual-gate E-mode MISFET can be calculated using the standard MOSFET equation for the drift current in linear operation region:

$$I_d = \frac{W\mu_{EF}C_{ox}}{L_g}(V_g - V_t - 0.5V_d - R_sI_d)(V_d - R_dI_d)$$

where R_s and R_d are the source and drain parasitic resistance in series with the channel, C_{ox} is the Al_2O_3 gate dielectric capacitance, μ_{EF} is the field-effect mobility, W is the gate width and L_g is the recessed-gate length. At small drain voltage V_d = 0.1 V, the maximum drain current I_d is typically around 10 mA/mm in these devices. Ignoring the voltage drop on the parasitic resistance, the drain current and transconductance are

$$I_d \cong \frac{W\mu_eC_{ox}}{L_g}(V_g - V_t - 0.5V_d)V_d$$

$$g_m = \frac{W\mu_{FE}C_{ox}}{L_g}V_d$$

The field-effect mobility can be calculated from equation [Schroder]:

$$\mu_{FE} = \frac{g_mL_g}{WC_{ox}V_d}$$

From CV measurements on Schottky contact AlGaN/GaN diode (C_{HEMT}) and Al_2O_3-AlGaN/GaN MIS-diode ($C_{MISHEMT}$), the Al_2O_3 gate capacitance can be calculated from $C_{ox} = C_{HEMT}C_{MISHEMT}/(C_{HEMT} - C_{MISHEMT})$. With the extracted gate capacitance of C_{ox} = 480 nF/cm^2, μ_{FE} is calculated as shown in Figure 3-9, with a maximum value of about 12 cm^{2}V^{-1}s^{-1}.

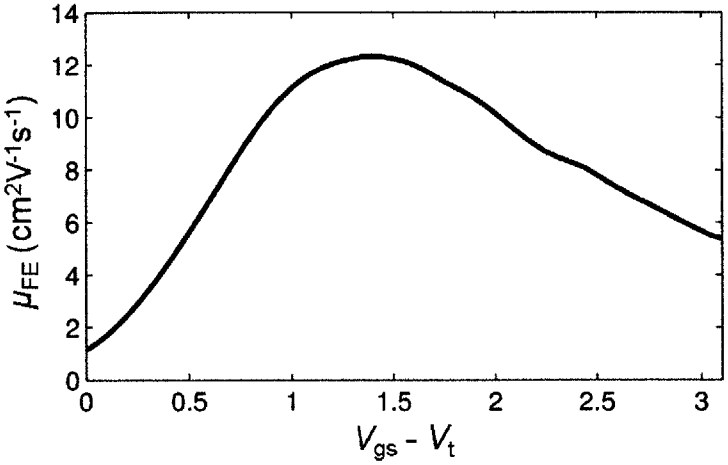

Figure 3-9. Field-effect mobility μ_{FE} and saturation mobility μ_{sat} of the E-mode dual-gate transistor calculated from g_m-V_d characteristics at V_d = 0.1 V and 12 V.

It should be noted that the calculated field-effect mobility is smaller than the actual channel effective mobility due to the assumption of a constant mobility in the calculation of g_m (instead of a decreasing one with increasing gate voltage) and the over-estimation of gate-channel capacitance by using the oxide capacitance C_{ox}. However, the calculated peak μ_{FE} is much lower than the mobility of the 2DEG (1045±79 cm^2/V·s) in the D-mode transistors. This degradation of channel mobility is expected due to the dry etch damage during the gate recess process. In section 3.5, an etch-stop wafer structure with low damage gate-recess process will be introduced, which result in an order of magnitude improvement in channel mobility of recessed-gate normally-off MISFETs.

3.4 Tri-gate Normally-off GaN Transistors

In the previous section, a parasitic leakage current path underneath the E-mode channel is suspected to be the cause of the relatively high leakage current (0.1 mA/mm) in the dual-gate normally-off GaN transistor. However, the leakage problem in normally-off GaN transistors has not been appreciated and device breakdown voltages are generally reported at a leakage current in the 0.1-1 mA/mm range in the literature [Suh2006b, Oka2008, Kanamura2010]. For high voltage power electronics applications, this leakage current is unacceptable. For example, a 50mΩ/600V AlGaN/GaN transistor would have a total gate width of approximately 100 mm (assuming the transistor has a source-to-drain distance of 10 μm with a typical contact resistance of 0.5 Ω·mm on a AlGaN/GaN wafer with a sheet resistance of 400Ω/sq). If the off-state leakage current of this transistor was 1 mA/mm, it would have 100 mA at 300 V drain bias (assume half of the rating voltage in real application), which would dissipate 30 W power! Therefore normally-off GaN transistors with leakage current of 1 μA/mm or less are required.

In this section, a 3D tri-gate structure is presented to reduce the off-state leakage current in normally-off GaN transistors. By combining a 3D tri-gate structure with the dual-gate design, we are able to achieve normally-off GaN transistors with a breakdown voltage as high as 565 V at a drain leakage current of 0.6 μA/mm [Lu2012].

3.4.1 Device Fabrication

The tri-gate normally-off GaN MISFETs were fabricated on a GaN-on-Si wafer grown by metal-organic chemical vapor deposition (MOCVD). The wafer structure consists of a 2 nm GaN cap layer / 18 nm $Al_{0.26}Ga_{0.74}N$ barrier / 1.2 μm i-GaN / 3.3 μm superlattice buffer. The device fabrication starts with mesa isolation and Ti/Al/Ni/Au ohmic contact formation. 250 nm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 was deposited as the etch mask for dry-etching of GaN. A 660 nm wide notch was etched into the SiO_2 for the pre-definition of the tri-gate region as shown in Figure 3-10(a). Interference lithography with 325 nm HeCd laser on a Lloyd's mirror setup (see schematic in Figure 3-10(e)) was then used to form gratings on the sample surface with a period of 300 nm. The sample was then etched by Cl_2-based electron-cyclotron-resonance reactive ion etching (ECR-RIE) to form the trench

structures in Figure 3-10(b) using SiO_2 as etching mask. A 120-nm-long normally-off region was then formed by a 30-nm-deep recess on top of the trench structure as shown in Figure 3-10(c). After the recess, the sample surface was cleaned by O_2 plasma followed by a rapid thermal annealing (RTA) at 600 °C and 1 min $HCl:H_2O$ wet etch. A gate dielectric stack of 9 nm SiO_2/7 nm Al_2O_3 with the SiO_2 interfacing the GaN was deposited by atomic layer deposition (ALD) at 250 °C immediately after a UV-Ozone surface treatment. Finally, a 2-μm-long Ni/Au gate electrode was deposited covering the tri-gate region as shown in Figure 3-10(d). The cross section SEM image of the tri-gate structure in Figure 3-10(d) shows a sidewall height of 250 nm and a top channel width of 90 nm. The sample was then annealed at 500 °C for 150 s in N_2 ambient to improve the gate dielectric quality. As a reference, standard D-mode planar-gate AlGaN/GaN HEMTs and recessed-gate GaN transistors with the same recess depth of 30 nm were fabricated together with the tri-gate normally-off GaN MISFETs on the same sample. The reference devices have the same gate dielectric and process conditions as the tri-gate transistors.

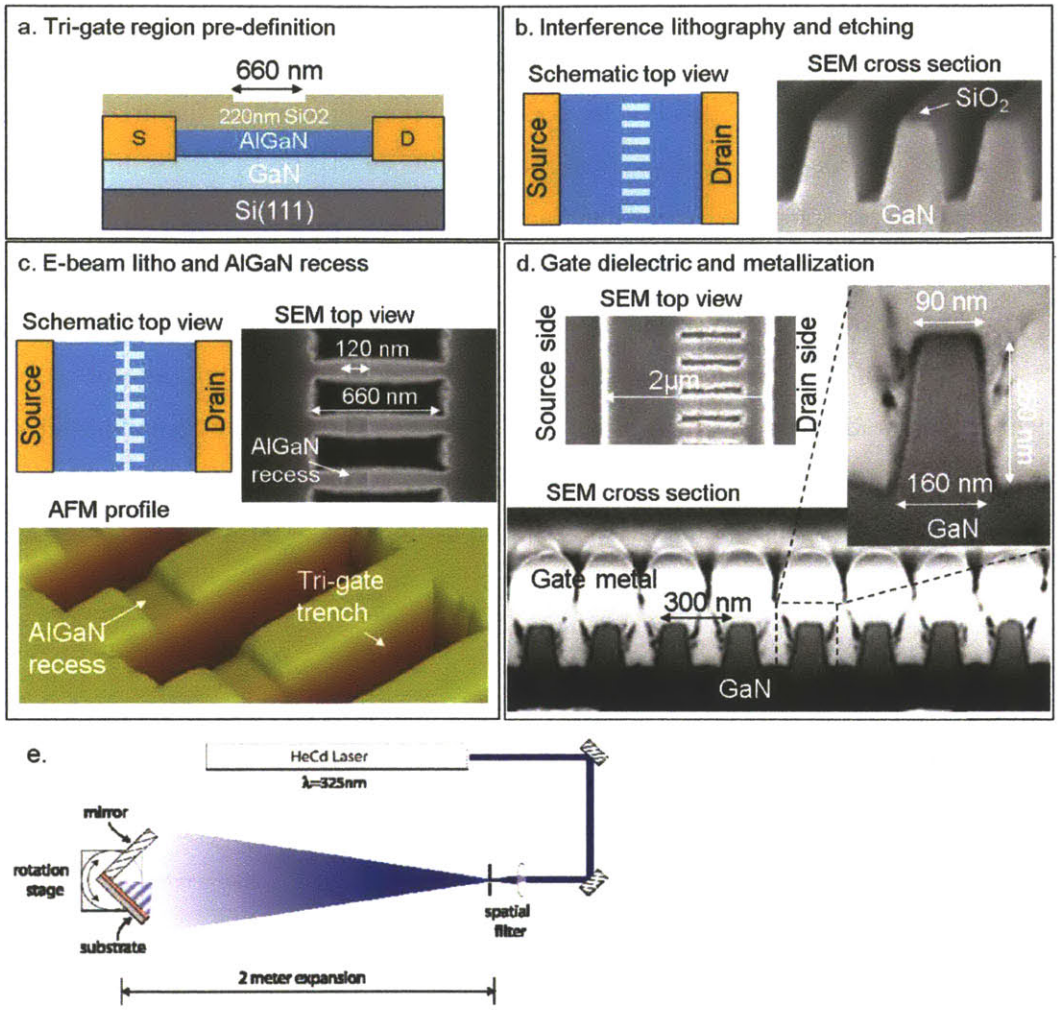

Figure 3-10. Tri-gate device fabrication: (a) PECVD SiO_2 mask deposition and 660 nm tri-gate region pre-definition etching; (b) Interference lithography and subsequent dry etching; (c) 120-nm AlGaN gate-recess region lithography and recess-etching. Atomic-force-microscope (AFM) image shows the profile; (d) gate dielectric deposition and gate metallization. The cross-section scanning-electron-microscope (SEM) images show the dimensions of the tri-gate channel structure which has a period of 300 nm. The top channel width is 90 nm and the sidewall height is 250 nm. (e) Schematic of the Lloyd's mirror interference system used in the fabrication (source: Nano Structures Laboratory Lloyd's mirror interference lithography user manual).

3.4.2 DC Characterization

The DC characteristics of the tri-gate normally-off GaN MISFET are shown in Figure 3-11. The results are normalized by the width of the ohmic contacts (W = 100 μm) rather than

the effective channel width to take into account the actual size of the device. The tri-gate normally-off MISFET has a steep sub-threshold slope and a very low off-state leakage current, indicating a very good gate control of the channel by the tri-gate structure. Averaging over 16 devices, the tri-gate normally-off GaN MISFETs have a threshold voltage of 0.80±0.06 V, extrapolated from the transfer characteristics as shown in Figure 3-11(a) [Schroder]. The drain leakage current is 0.3 mA/mm and 1 μA/mm for V_{gs} = 0.80 V and 0.53 V, respectively, at V_{ds} = 5 V. The tri-gate normally-off MISFETs have a minimum sub-threshold slope of 86±9 mV/decade at V_{ds} = 1 V with an on/off current ratio of more than 8 orders of magnitude. The tri-gate normally-off MISFETs also have very small hysteresis. The average hysteresis in the threshold voltage is 0.05 V, measured from the bi-directional voltage sweep in the transfer characteristics in Figure 3-11(a).

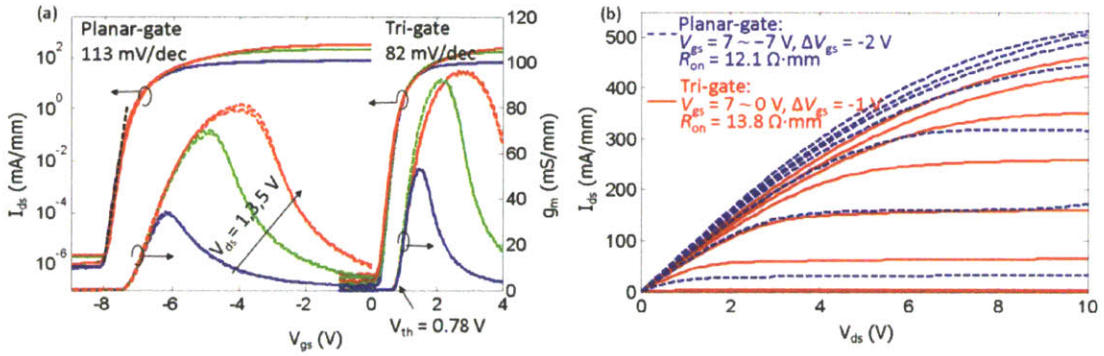

Figure 3-11. Comparison of a tri-gate normally-off GaN MISFET with a standard planar-gate D-mode GaN transistor: (a) transfer characteristics at V_{ds} = 1, 3, and 5 V with bi-direction gate sweep; (b) I_d-V_{ds} characteristics. Both devices have L_{gs} = 1.5 μm, L_g = 2 μm, L_{gd} = 10 μm and W = 100 μm

The SiO_2/GaN interface trap density (D_{it}) can be estimated from the sub-threshold slope equation

$$S = \frac{kT}{q}\ln(10)\,(1 + \frac{C_s + C_{it}}{C_{ox}})$$

where C_s is the GaN semiconductor capacitance; C_{it} is the SiO_2/GaN interface trap capacitance; and C_{ox} is gate dielectric capacitance extracted subtracting the Schottky-gate

HEMT capacitance from a MISHEMT capacitance (see section 3.3.3 for detail). Using the measured sub-threshold slope S = 86±9 mV/decade and C_{ox} = 0.33 μF/cm^2, the minimum D_{it} in the sub-threshold operation regime of the device is estimated by

$$D_{it} = \frac{C_{it}}{q} < \left(\frac{qS}{kTln(10)} - 1\right) C_{ox}$$

which gives a D_{it} of approximately $1.2 \times 10^{12} cm^{-2} eV^{-1}$.

The improved channel confinement of the tri-gate structure is effective in reducing the short channel effects of the sub-micron recessed-gate GaN MISFET. As shown in Figure 3-12, a conventional recessed-gate MISFET with a gate length of 160 nm suffers from short channel effects, such as degraded sub-threshold slope, significant drain-induced barrier lowering (DIBL) and increased sub-threshold current with higher V_{ds} voltage while the tri-gate GaN MISFET of 120 nm channel length has a constant sub-threshold slope and stable sub-threshold current.

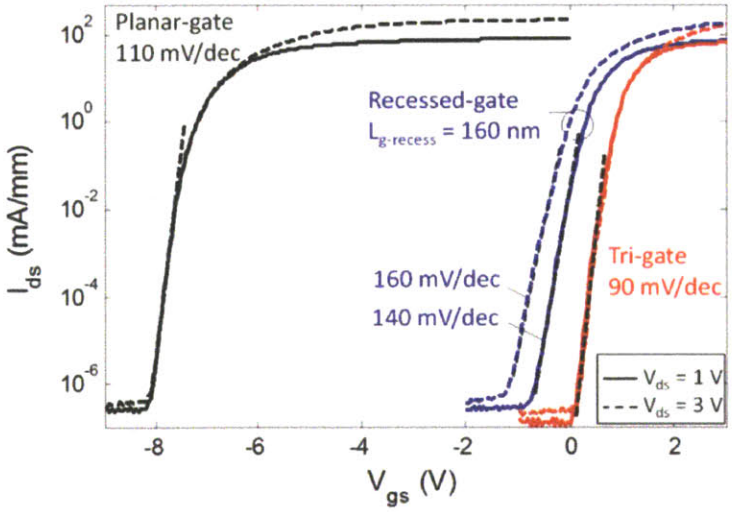

Figure 3-12. I_{ds}-V_{gs} characteristics of the tri-gate normally-off MISFET compared with the standard planar-gate transistor and the recessed-gate MISFET with recessed-gate length of 160 nm. All the devices have the same dimensions with L_{gd} = 8 μm and are biased at V_{ds} = 1 V (solid) and 3 V (dashed).

Surprisingly, even after removing the entire thickness of the AlGaN barrier with the 30-nm-deep gate recess in the recessed-gate MISFETs (see Figure 3-12), the device still has relatively high drain leakage of 28 μA/mm at V_{gs} = 0 V and V_{ds} = 1 V. Apparently this 30-nm-deep gate recess did not create enough barrier height in the conduction band to block the electrons and make a completely normally-off device. This could be due to the positive charges at the gate dielectric/GaN interface. High density of positive charges at dielectric/III-nitrides interface has been reported [Ganguly2011, Esposto2011]. We have also observed increase of leakage current on the plasma etched GaN surfaces after dielectric deposition. On the other hand, the tri-gate structure is able to shift the threshold voltage of the conventional recessed-gate device in the positive direction, reducing the I_{ds} below 0.5 nA/mm as shown in Figure 3-12. The effect of the tri-gate structure on the positive shift of the threshold voltage is investigated in section 3.5.

The breakdown voltage of the tri-gate normally-off GaN MISFETs was measured using an Agilent B1505A high voltage semiconductor analyzer on a Cascade Tesla probe station. As shown in Figure 3-13, breakdown voltage as high as 565 V was measured at a drain leakage current of 0.6 μA/mm and V_{gs} = 0 V on a device with L_{gd} = 10 μm. The device had a gate-dielectric hard breakdown. The specific on-resistance $R_{on,sp}$, calculated from the active area between source and drain and 2 μm transfer length from each contact, of several tri-gate normally-off GaN MISFETs is plotted in Figure 3-14. Compared to the previous results, the new device demonstrates much lower off-state leakage current with a breakdown voltage higher than 200 V.

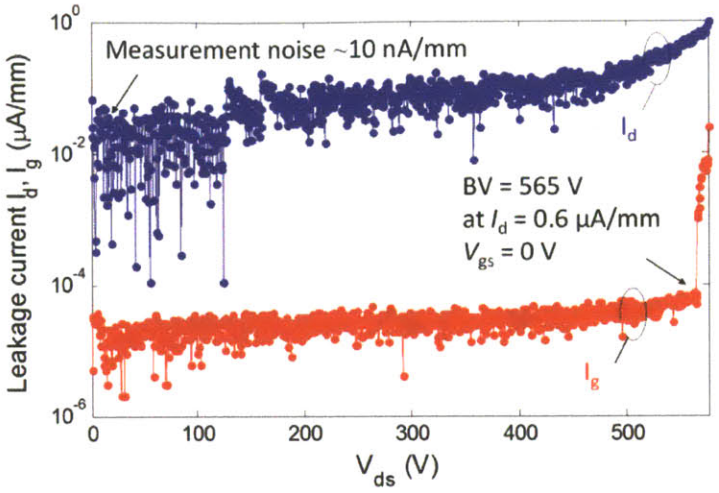

Figure 3-13. Three-terminal BV measurement of the tri-gate normally-off GaN MISFET with L_{gd} = 10 μm at V_{gs} = 0 V.

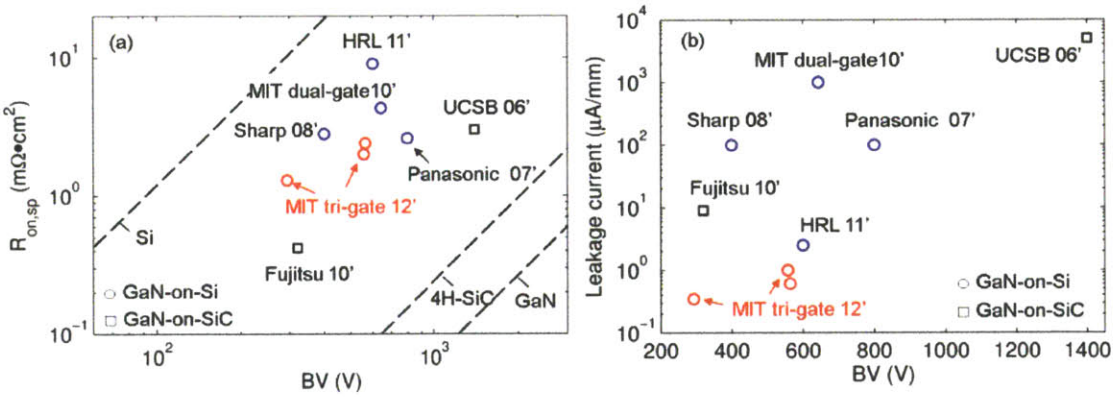

Figure 3-14. (a) Specific on-resistance ($R_{on,sp}$) *vs.* breakdown voltage (BV) and (b) leakage current *vs.* BV of the tri-gate normally-off GaN MISFETs and other normally-off GaN devices in the literature with BV measured at V_{gs} = 0 V.

3.4.3 Characterization of Tri-gate Channel Resistance

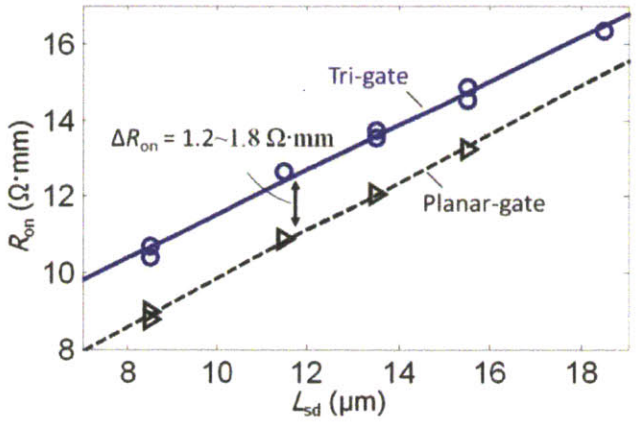

Figure 3-15. R_{on} as a function of source-to-drain distance L_{sd} extracted at V_{gs} = 7 V. The R_{on} of normally-off tri-gate devices is on average 1.2-1.8 Ω·mm higher than that of standard planar-gate devices.

The sheet resistance of tri-gate channel $R_{sh\text{-}trig}$ is calculated to estimate the impact of the sidewall to the electron mobility of the 2DEG. As shown in Figure 3-15, R_{on} of the normally-off tri-gate MISFETs are on average 1.2-1.8 Ω·mm higher than that of the standard planar-gate D-mode transistors. The higher R_{on} is expected because for every 300 nm of the device width, 210 nm AlGaN/GaN channel was removed as shown in the SEM cross-section of the device in Figure 3-10(d). The increase of R_{on} can be written as

$$\Delta R_{on} = R_{on\text{-}trig} - R_{on\text{-}planar} = \left(\frac{R_{sh\text{-}trig}}{\alpha} - R_{sh}\right) L_{trig}$$

where R_{sh} is the sheet resistance of planar device; α is the fill factor of each tri-gate in the 300 nm period (defined as the ratio between tri-gate channel width and its period); and L_{trig} is the tri-gate length. Using ΔR_{on} = 1.2-1.8 Ω·mm, R_{sh} = 570 Ω/sq, α = 90nm/300nm = 0.3 and L_{trig} = 660 nm, the calculated average sheet resistance of each tri-gate channel is around 716-989 Ω/sq, which is 1.3-1.7 times of the sheet resistance in the planar-gate device. Considering there is also a 120-nm-long 30-nm-deep gate recess in the tri-gate region (see the AFM image in Figure 3-10(c)), the actual tri-gate channel resistance should be even lower. In fact, it will be shown in section 3.5.4 that the electron mobility in each tri-gate channel is close to the 2DEG mobility in the planar AlGaN/GaN HEMTs. Therefore by reducing the length of

tri-gate region and increasing the fill-factor, R_{on} of the normally-off tri-gate MISFETs can be further reduced.

3.5 Impact of Sidewall-gates on Tri-gate AlGaN/GaN Transistors

In order to further improve the device performance and optimize the tri-gate structure, the impact of the tri-gate sidewalls on device gate capacitance and channel mobility needs to be understood. For this study, new tri-gate AlGaN/GaN devices with different tri-gate channel lengths and tri-gate sidewall heights were fabricated. Current-voltage (I-V) and capacitance-voltage (CV) characterization with 2D electrical and mechanical simulations are used to understand the electrostatic, mechanical and transport properties of the tri-gate AlGaN/GaN channels.

3.5.1 Device Fabrication

Long channel tri-gate transistors and capacitors were fabricated with tri-gate channel length of 3 μm, 5 μm, 10 μm, 15 μm and 20 μm. There are 4 batches of samples with different sidewall heights of 70 nm, 120 nm, 200 nm and 350 nm. In addition to these tri-gate transistors, large tri-gate capacitors with tri-gate channel length between 40 μm and 100 μm were also fabricated for the extraction of gate capacitance. All the devices were fabricated on the same wafer consisting of a 2-nm-GaN cap layer / 18-nm-$Al_{0.26}Ga_{0.74}N$ barrier / 1.2 μm i-GaN / 3.3 μm $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ superlattice buffer / Si substrate. The virgin wafer has a 2DEG density of $9.3\times10^{12}/cm^2$ and mobility of 1660 $cm^2V^{-1}s^{-1}$ from Hall measurement. Each tri-gate structure has a channel width of 150 nm with a period of 370 nm as shown in Figure 3-16. Unlike the normally-off tri-gate transistor in section 3.4, these devices do not have the additional gate recess shown in Figure 3-10(c). As a result, they are normally-on devices due to the 2DEG induced at the AlGaN/GaN interface. All the devices have 18 nm SiO_2 gate dielectric deposited by ALD.

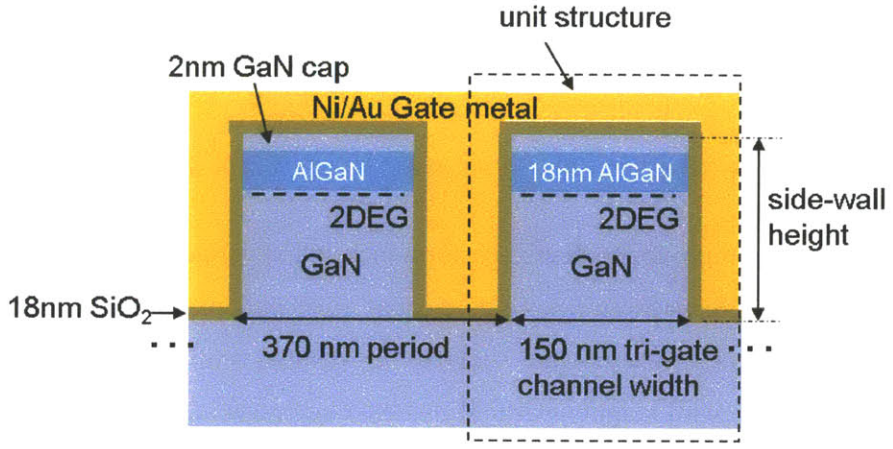

Figure 3-16. Cross-section schematic of the tri-gate channel of the fabricated devices.

3.5.2 DC Characterization

Transfer characteristics of the tri-gate transistors with different sidewall heights are compared with a planar-gate transistor in Figure 3-17. The tri-gate devices have a large positive threshold voltage shifts compared to the planar-gate device. When the tri-gate sidewall height increased from 70 nm to 350 nm, the threshold voltage further shifted in positive direction for about 1.3 V. The threshold voltage is saturated at a sidewall height of 200 nm and even shift to the negative direction for 0.2 V when the height increased from 200 nm to 350 nm.

It should be highlighted that the transfer characteristics of the planar-gate transistors have large variations among different devices but they all showed poor subthreshold slopes and large negative pinch-off voltages between -9 V and -11 V. The one shown in Figure 3-17 is a typical characteristic of these planar-gate transistors. On the other hand, the transfer characteristics of the tri-gate transistors have much smaller variations and the trend in the change of threshold voltages as a function of tri-gate heights is consistent in all the devices. The abnormal subthreshold slope of the planar gate devices at large negative gate bias (between -11 V and -4 V) may involve non-thermal equilibrium processes, such as ionization of deep SiO_2/GaN-cap interface states, which is irrelevant at the operating voltages of tri-gate devices (i.e. between -4 V and 1 V).

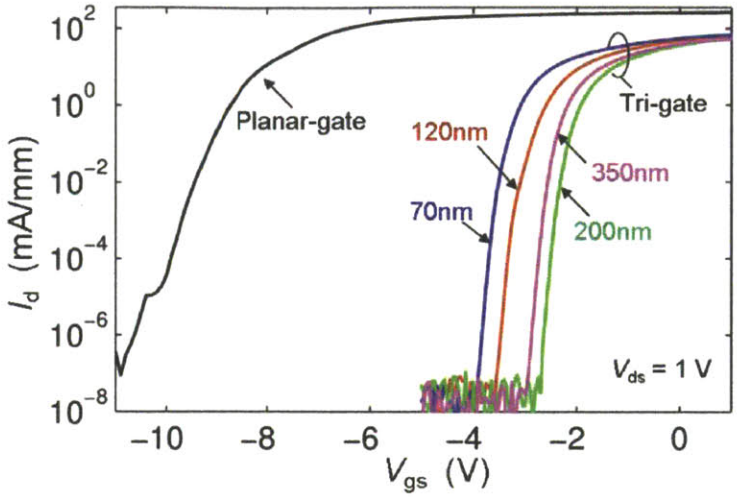

Figure 3-17. Transfer characteristics of a planar-gate transistor (gate length of 10 μm) and tri-gate transistors (tri-gate length of 15 μm) with side-wall height of 70 nm, 120 nm, 200 nm and 350 nm at V_{ds} = 1 V. The current is normalized by the channel width which is 150 nm for every 370 nm width for tri-gate transistors and 100 μm for planar-gate transistor. V_{gs} is stepped from negative to positive direction.

Quasi-static capacitance voltage (QSCV) measurement was performed on the large area tri-gate and planar-gate capacitors. The voltage step is 0.25 V with a ramping time of 80 ms. The capacitance is normalized by the area of the top gate, which has a width of 150 nm for each unit tri-gate structure as shown in the schematic in Figure 3-18. The QSCV characteristics are consistent with the transfer characteristics (e.g. same trend in the turn-off voltages between -4 V and -3 V of the tri-gate capacitors is observed). The QSCV curve of the planar-gate capacitor also shows stretched behavior which is consistent with the abnormal subthreshold characteristics of the planar-gate transistors. The tri-gate QSCV curves have two shoulders, with a first increase of capacitance between -4 V and -3 V and a second increase between -1 V and 0 V, as shown in Figure 3-18.

The tri-gate capacitance behavior can be analyzed from its component capacitors as shown in the schematic of a unit structure in Figure 3-18. The capacitance of each tri-gate unit structure, C_{unit}, consists of a top channel capacitor C_{top}, a side-wall capacitor $C_{\text{side-wall}}$ and a bottom capacitor C_{bottom}:

$$C_{\text{unit}} = S_{\text{top}}C_{\text{top}} + S_{\text{side-wall}}C_{\text{side-wall}} + S_{\text{bottom}}C_{\text{bottom}}$$

where C_{top}, $C_{side\text{-}wall}$ and C_{bottom} are the capacitance per area (in the unit of F/m^2) and S_{top}, $S_{side\text{-}wall}$ and S_{bottom} are the top channel, side-wall and bottom channel areas for each unit structure.

Normalizing by the top channel area S_{top} gives the normalized tri-gate capacitance C_{trig} measured in the QSCV measurements:

$$C_{trig} = \frac{C_{unit}}{S_{top}} = C_{top} + \frac{C_{side\text{-}wall} S_{side\text{-}wall}}{S_{top}} + \frac{C_{bottom} S_{bottom}}{S_{top}}$$

$$= C_{top} + \frac{2h_{side\text{-}wall}}{W_{top}} C_{side\text{-}wall} + \frac{W_{period} - W_{top}}{W_{top}} C_{bottom}$$

where the top-channel width W_{top} = 150 nm; the side-wall height $h_{side\text{-}wall}$ = 70 nm to 350 nm; and the width of each unit tri-gate structure W_{period} = 370 nm.

Before presenting a detailed study of the contribution of each capacitance components in the tri-gate structure in the next section 3.5.3, an estimation of these capacitors based on the simple parallel plate capacitor model can be used to qualitatively explain a few important points in the CV characteristics of the tri-gate capacitor.

The top channel capacitance can be estimated using the capacitance value of planar-gate in Figure 3-18: C_{top} = 143 nF/cm^2. The maximum side-wall and bottom capacitance can be estimated by the gate oxide capacitance. With the ALD SiO_2 thickness of 18 nm and a dielectric constant of 4.5 (determined from CV measurement and simulation in section 3.5.3), we have the maximum estimated value: $C_{bottom} = C_{side\text{-}wall} = C_{ox}$ = 221 nF/cm^2.

If we assume that the bottom capacitor does not contribute to the total tri-gate capacitance, then we have:

$$C_{trig} = C_{top} + \frac{2h_{side\text{-}wall}}{W_{top}} C_{side\text{-}wall} = 143 + \frac{2h_{side\text{-}wall}}{150\ \text{nm}} 221$$

For $h_{side\text{-}wall}$ = 70 nm, maximum C_{trig} = 349 nF/cm^2; for $h_{side\text{-}wall}$ = 350 nm, maximum C_{trig} = 659 nF/cm^2. These values are much smaller than the measured tri-gate capacitance at bias voltage of 3 V. Therefore, the bottom capacitance must contribute to the total tri-gate capacitance and it should start electron accumulation around 0 V for $h_{side\text{-}wall}$ = 70 nm and less than 0 V for $h_{side\text{-}wall}$ = 350 nm.

If we include the contribution of C_{bottom},

$$C_{\text{trig}} = C_{\text{top}} + \frac{2h_{\text{side-wall}}}{W_{\text{top}}} C_{\text{side-wall}} + \frac{W_{\text{period}} - W_{\text{top}}}{W_{\text{top}}} C_{\text{bottom}}$$

For $h_{\text{side-wall}}$ = 70 nm, maximum C_{trig} = 673 nF/cm^2; for $h_{\text{side-wall}}$ = 350 nm, maximum C_{trig} = 1499 nF/cm^2. These values are very similar to the measurement results in Figure 3-18.

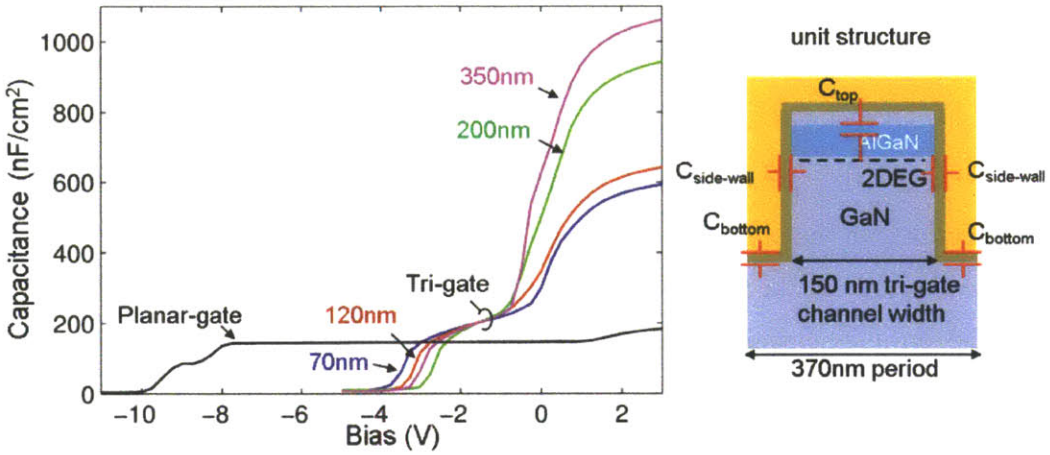

Figure 3-18. Quasi-static CV measurement of tri-gate capacitors with side-wall height of 70 nm, 120 nm, 200 nm and 350 nm and planar-gate capacitors. Bias votlage was swept from negative to positive direction. The cross-section schematic of one unit tri-gate structure shows the capacitor components of C_{top}, $C_{\text{side-wall}}$ and C_{bottom}. The capacitance is normalized by the top channel area.

3.5.3 CV Simulation

The tri-gate device CV characteristics are simulated by solving Schrodinger-Poisson equations using device simulator nextnano3. The simulated capacitance is calculated using the equation:

$$C = dQ/dV$$

There are two choices in choosing the Q. When free electron (or hole) charge $Q_{\text{n}} = qn$ is used, we can denote the capacitance as C_{n}:

$$C_n = dQ_n/dV$$

When the total charge $Q_{total} = Q_n + Q_t$, including both electron charge and trap charge, the capacitance can be denoted as:

$$C_{total} = dQ_{total}/dV$$

In actual CV measurement, depending on the measurement frequency f and trap life time τ, a fraction of trap charge αQ_t is measured, where α is a function of frequency. The capacitance measured by the CV technique, denoted by C_{AC} is:

$$C_{AC} = d(\alpha Q_t + Q_n)/dV$$

When $\tau \gg 1/f$, $\alpha \cong 0$ and $C_{AC} = C_n$, which is called high frequency capacitance C_{hf}; when $\tau \ll 1/f$, $\alpha \cong 1$ and $C_{AC} = C_{total}$, which is called low frequency capacitance C_{lf}.

When $0 < \alpha < 1$, $C_n < C_{AC} < C_{total}$. Using either C_{total} or C_n to fit the measurement C_{AC} will cause errors. In the simulation of the tri-gate capacitance, C_n is used to fit the QSCV measurement result. In the discussion of the changes in threshold voltages of the tri-gate devices, the error asscioated with the CV fitting does not affect the conclusion. In the estimation of the tri-gate channel electron mobility, the error will cause an underestimation due to the overestimation of the free electron density, which gives a lower bound to the channel mobility.

In the nextnano3 CV simulation, thermal equilibrium is always assumed so that the calculated results are static solutions. When a AlGaN/GaN capacitor is biased at large negative bias voltages, the simulation would give hole accumulation. However, in actual device CV measurement, no inversion is observed in a AlGaN/GaN structure at room temperature without UV illumination because the device does not reach the thermal equilibrium condition during a CV sweep. In order to simulate this non-equilibrium condition with a equilibrium solution from the simulator, the bandgap of the semiconductor can be increased to eliminate the effect of the valance band.

III-nitride-semiconductor parameters used in the CV simulation are tested in another GaN MISFET structure as well (see section 3.6.4). They give good agreement between the measurement and simulation results. The detail of the III-Nitride-semiconductor parameters used in the simulation can be found in Appendix B along with the nextnano3 simulation codes in Appendix C. The parameters of the SiO_2 gate dielectric are based on reference

[Robertson2006]. It has a band gap of 9 eV and conduction band offset to GaN of 2.56 eV. The Ni/SiO_2 barrier height is 3.7 eV according to reference [Deal1966]. The dielectric constant of the ALD SiO_2 is estimated to be around 4.5 from CV measurement. However, only the ratio of its thickness to dielectric constant matters in the simulation. The uncertainty in the ALD SiO_2 parameters such as its band gap and band alignment can cause small variation on the estimated dielectric interface charge density. However it does not affect the observed trend and conclusions in the simulation.

One important factor in III-Nitrides system that requires special attention is the polarization property. In III-Nitrides, net charge exists when polarization dipole moment has non-zero divergence $\rho = -\nabla \cdot p$ or is interrupted at material interfaces, where p is the polarization dipole moment. As a result, there are net polarization charges at AlGaN/GaN interface and on c-plane surface. For the heterostructure used in this section, the net-polarization charges in the planar-gate device are illustrated in Figure 3-19(a), assuming that the $Al_{0.26}Ga_{0.74}N$ is lattice-matched to GaN buffer. Besides the polarization charges at the AlGaN/GaN and GaN/AlGaN interfaces, there is a large negative polarization charge of -2.21×10^{13}q/cm^2 at the SiO_2/GaN interface, which arises from GaN spontaneous polarization.

Without donor states or SiO_2/GaN interface positive charges, the band diagram of the planar-gate device would look like the one in Figure 3-19(b). The Fermi-level would be at the valence band edge of the GaN-cap layer. However photoreflectance measurements of the electric field strength in several AlGaN/GaN structures coupled with device Schrödinger-Poisson simulation estimated that the surface potentials ($\Phi_B = E_c - E_f$ at the surface of AlGaN) are 0.53-0.56 eV [Winzer2003], 0.6-0.7 eV [Winzer2004] and 1-1.7 eV [Kudrawiec2004]. The surface potential of a 3-nm-GaN-cap/23-nm-$Al_{0.22}Ga_{0.78}N$/GaN structure was also estimated to be around 0.25 eV in [Waltereit2009]. The band diagram shown in Figure 3-19(b) is obviously in contradiction with these measurement results. In fact, surface states exist at semiconductor surface due to dangling bonds [Van de Walle2007] and surface contamination such as oxygen adsorption [Dong2006]. Surface states have been proposed to be the donors for the 2DEG at the AlGaN/GaN heterojuntion and they have positive charges when ionized [Ibbetson2000]. As a result, the SiO_2/GaN-cap interface states are important fitting parameters in the CV simulation. The surface states which cannot be

modulated by the gate bias (too slow or outside of the band gaps) are regarded as fixed charges in the simulation. Surface states which can be modulated by the gate bias are extracted from the deviation of the CV curve from its ideal shape. By changing the SiO_2/GaN-cap interface charges in the simulation, the surface potential in the GaN-cap layer can be adjusted. As shown in Figure 3-19(c), by adding positive charges to the SiO_2/GaN-cap interface, conduction band edge at the surface of GaN-cap layer is now close to the Fermi-level.

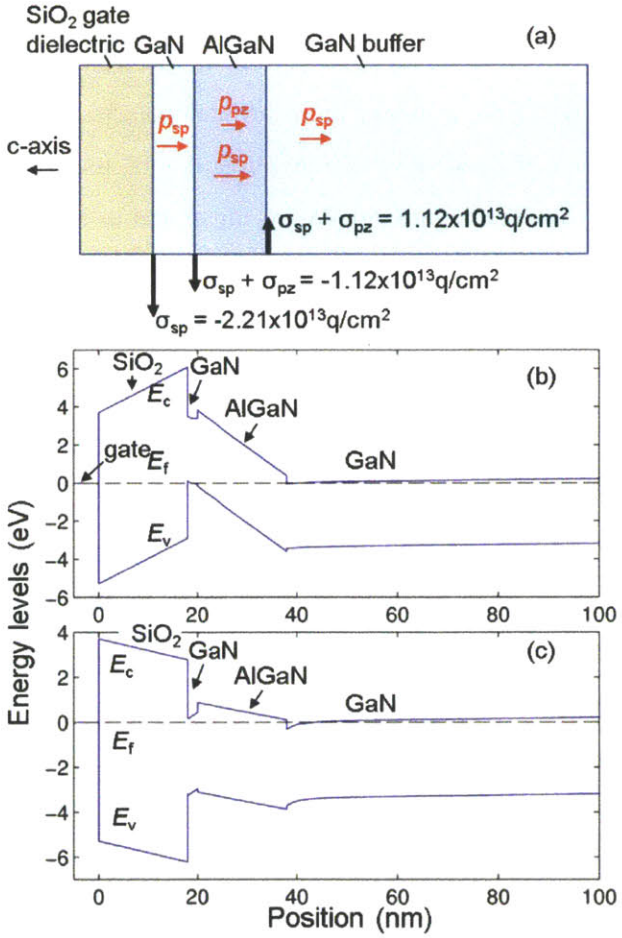

Figure 3-19. (a) Net polarization charges and polarization dipole moments in the SiO_2/GaN/$Al_{0.26}Ga0_{.74}N$/GaN structure with AlGaN lattice matched to GaN; (b) Band diagram of the planar-gate device without SiO_2/GaN-cap interface charges and (c) with appropriate positive charge added to the SiO_2/GaN-cap interface.

• **Planar-gate CV Simulation**

The planar-gate capacitor CV characteristic was first simulated to verify device parameters which will be used later in the tri-gate device simulation. Using a positive SiO_2/GaN-cap interface fixed charge density of $3.14\times10^{13}cm^{-2}$ and ALD SiO_2 dielectric constant of 4.5, the simulated planar-gate CV curve fits well with the measurement data as shown in Figure 3-20. Its band-diagram at zero bias condition is shown in Figure 3-19(c) with E_c-E_f = 0.15-0.2 eV at GaN-cap layer surface. The accuracy of the calculated surface potential, including those estimated in references [Winzer2003, Winzer2004, Kudrawiec2004 and Waltereit2009], is subjected to the accuracy of key material parameters such as the band alignment, band gap, dielectric constants and polarization properties. It should be noted that in the planar-gate device CV simulation, electron trapping is *not* required to fit the CV curve for bias voltages between -7.3 V and 0.8 V, which means there are either no trap states between E_v+0.5 eV and E_c-0.15 eV at GaN-cap surface or these states are too slow to respond to the QSCV sweep.. Nevertheless, the voltage range that is relevant to the study of the tri-gate devices, especially the shifts in threshold voltage, is between -4 V and 0 V. requires special treatment which is not the focus this section and it does not affect the study of the pinch-off voltages in the tri-gate devices either.

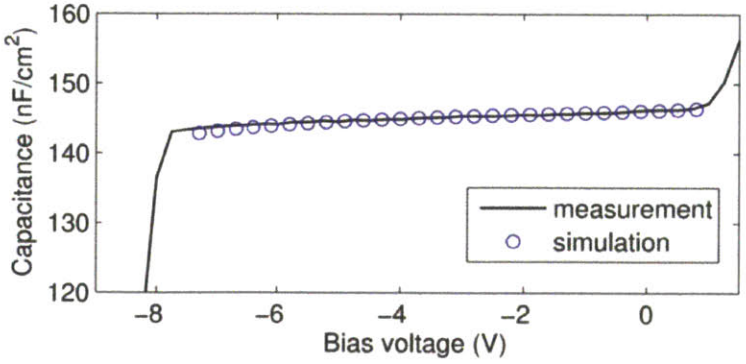

Figure 3-20. Simulated CV characteristics of planar-gate device fitted well with the measurement result.

- **Tri-gate CV simulation**

Based on the material parameters verified by the planar-gate device CV simulation, we begin this section with the simulation of the tri-gate device with 70 nm sidewall height, from which the electrostatic characteristics of the tri-gate structure in general can be understood. Since it is also shown in section 3.5.5 that there are negligible changes in the piezoelectric charges among the tri-gate devices with different sidewall heights, we will be able to understand the impact of strain relaxation on the CV characteristic from the simulation of the 70-nm-side-wall tri-gate device.

First, we start the CV simulation of the 70-nm-side-wall tri-gate device by using the same fixed positive charges at the interface of SiO_2/GaN-cap as in the planar-device and assuming ideal SiO_2/sidewall interface without any traps or interface charges. As shown in the CV curve in Figure 3-21 with open-circles, the simulated tri-gate CV curve has a pinch-off voltage (at which the capacitance drops to zero) at -7 V, shifted 3 V comparing to the planar-gate device. This shift of pinch-off voltage is purely due to the depletion of the 2DEG from the sidewall gates in the tri-gate device. To be noted that neither strain relaxation nor the traps at the side-walls is included in the simulation at this point.

Strain relaxation is then added to the simulation while keeping the same amount of SiO_2/GaN-cap interface positive charge density as in the planar-gate device. Partial strain-relaxation with a reduction of piezoelectric charge at AlGaN/GaN interface by about 2×10^{12} q/cm^2 was first introduced based on the piezoelectricity simulation results in section 3.5.5. As shown in the CV curve in Figure 3-21 (crosses), the pinch-off voltage increases further by approximately 0.5 V compared to the simulation with full strain (open circles). This shift of pinch-off voltage is due to the reduction of built-in voltage in the AlGaN barrier layer from the reduced piezoelectric charges. Since the piezoelectricity simulation in section 3.5.5 only gives an estimation of the strain in the device before the deposition of gate dielectric, the exact amount of strain in the fully-fabricated tri-gate devices is not known. However, we can look at the extreme case where the strain is assumed to be fully relaxed in AlGaN. By setting the piezoelectric charge to zero, the simulated CV curve is shown in Figure 3-21 represented by diamond symbols, which has a pinch-off voltage of about -5.8 V. It is still about 2 V smaller than the measurement result.

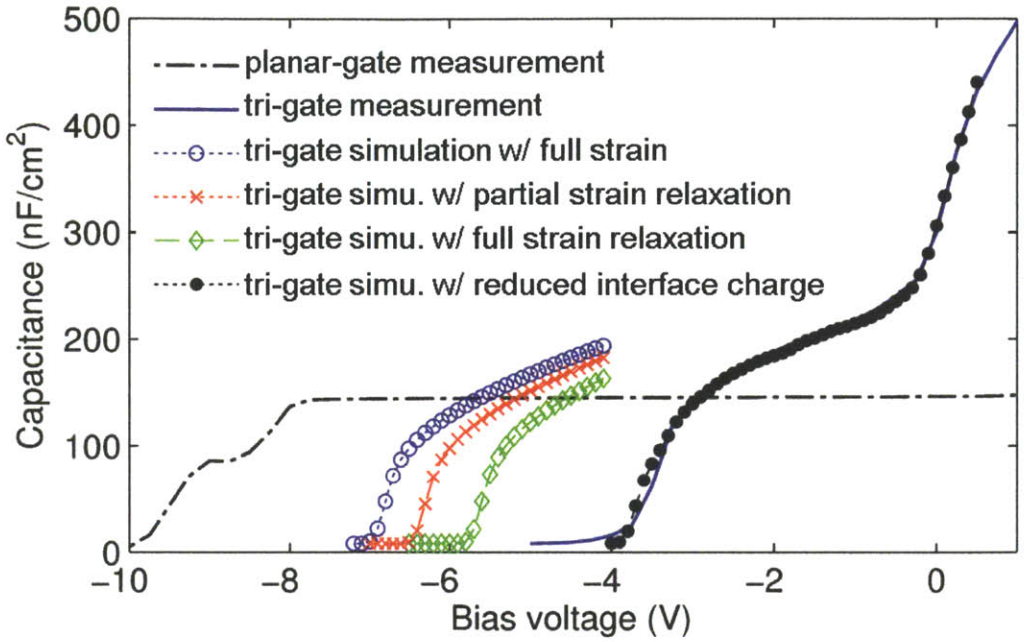

Figure 3-21. Measured and simulated CV curves of 70-nm-sidewall tri-gate device. The different CV simulations compare the impacts of the tri-gate sidewalls, strain relaxation and SiO_2/GaN-cap interface charges on the shift of pinch-off voltage. Open circle is the tri-gate simulation with full strain and the same interface positive fixed charge as in the planar-gate device; Cross and diamond are the results by reducing the piezoelectric charges due to strain relaxation; Filled-circles represent the simulation fitted to the measurement by changing the SiO_2/GaN-cap interface positive charges. Planar-gate CV curve is for comparison purpose.

In order to match the measured CV characteristic of the 70-nm-side-wall tri-gate device, the density of positive fixed charges at the SiO_2/GaN-cap interface has to be reduced. This is consistent with the "surface donor" model proposed by Ibbetson *et al.* [Ibbetson2000]. The reduction in piezoelectric charges in AlGaN due to strain relaxation in the tri-gate device (see section 3.5.5) can cause the change in band bending which affects the amount of ionized donor states at the SiO_2/GaN-cap interface. We can hypothesize that the impact of the strain relaxation on tri-gate AlGaN/GaN devices is through modulation of the ionized donor states. Similar argument was also used in reference [Winzer2003] in order to explain the change of measured electric field in AlGaN layer when the strain was changed by thermal expansion. By assuming a Fermi-level pinning at the GaN-cap layer surface at the same position as in

the planar-gate device (E_c - 0.2 eV), the fitting to the measured CV curve (see Figure 3-21 filled circles) can uniquely determine the SiO_2/GaN-cap interface fixed charge density and the value of piezoelectric charge in the relaxed AlGaN. As a result, it is determined that for the 70-nm sidewall tri-gate device, the SiO_2/GaN-cap interface positive charge has a density of 2.76×10^{13} q/cm^2 (lower than 3.14×10^{13} q/cm^2 in the planar-gate device). The piezoelectric charge in AlGaN is also decreased by 4.63×10^{12} q/cm^2. Considering there is 4.91×10^{12} q/cm^2 piezoelectric charge in the fully strain $Al_{0.26}Ga_{0.74}N$ on GaN, it indicates that most of the strain in the AlGaN layer of the 70-nm sidewall device is relaxed. The fitting of the CV curve in the -3 V to -0.5 V bias voltage range also requires sidewall trap states. However, the trap density and energy level cannot be uniquely determined, which requires multi-frequency measurement. In the simulation, as fewer amount of traps as possible is used for the fitting of the CV curves. The creation of miniband structures due to quantum confinement can be neglected in this 2D simulation because of relatively large device dimensions. In the bias voltage range of the simulation (between pinch-off and 0.5 V), the quantization effects have almost no observable changes to the simulated CV curves.

The conduction band edge of the 70-nm-side-wall tri-gate device at gate bias voltage of 0 and -3 V is shown in Figure 3-22. At gate bias of 0 V, 2DEG is formed at the AlGaN/GaN interface. Due to the side-gate contacts, the depletion region width (defined at half maximum electron density) of the 2DEG from each side-wall is approximately 7 nm. At gate bias of -3 V, the 2DEG density shrinks laterally from the tri-gate sidewalls with an increase of the side-wall depletion region width, which can also be seen in the 2D electron density distribution in Figure 3-23. As a result, the conduction band in the tri-gate channel has a parabolic shape in the horizontal direction. Apparently, the sidewall gates deplete the 2DEG more effectively than the top gate. This is because the sidewall-gate-to-channel distance is smaller than that of the top gate due to the absence of the AlGaN barrier. Before the 2DEG lateral depletion width increases to the thickness of the AlGaN barrier, the side-wall gates will predominately deplete the 2DEG in the channel. Therefore, in the AlGaN/GaN tri-gate devices with small channel width, the side-wall gates will have full control of the channel, which is the case in the 90-nm-channel-width tri-gate transistors demonstrated in section 3.4. Another observation from Figure 3-22(c) is that the conduction band-to-Fermi-level distance increases in the y-axis direction away from the AlGaN/GaN interface and this is the reason why the tri-

gate normally-off transistors have very low off-state leakage current as shown in section 3.4.2.

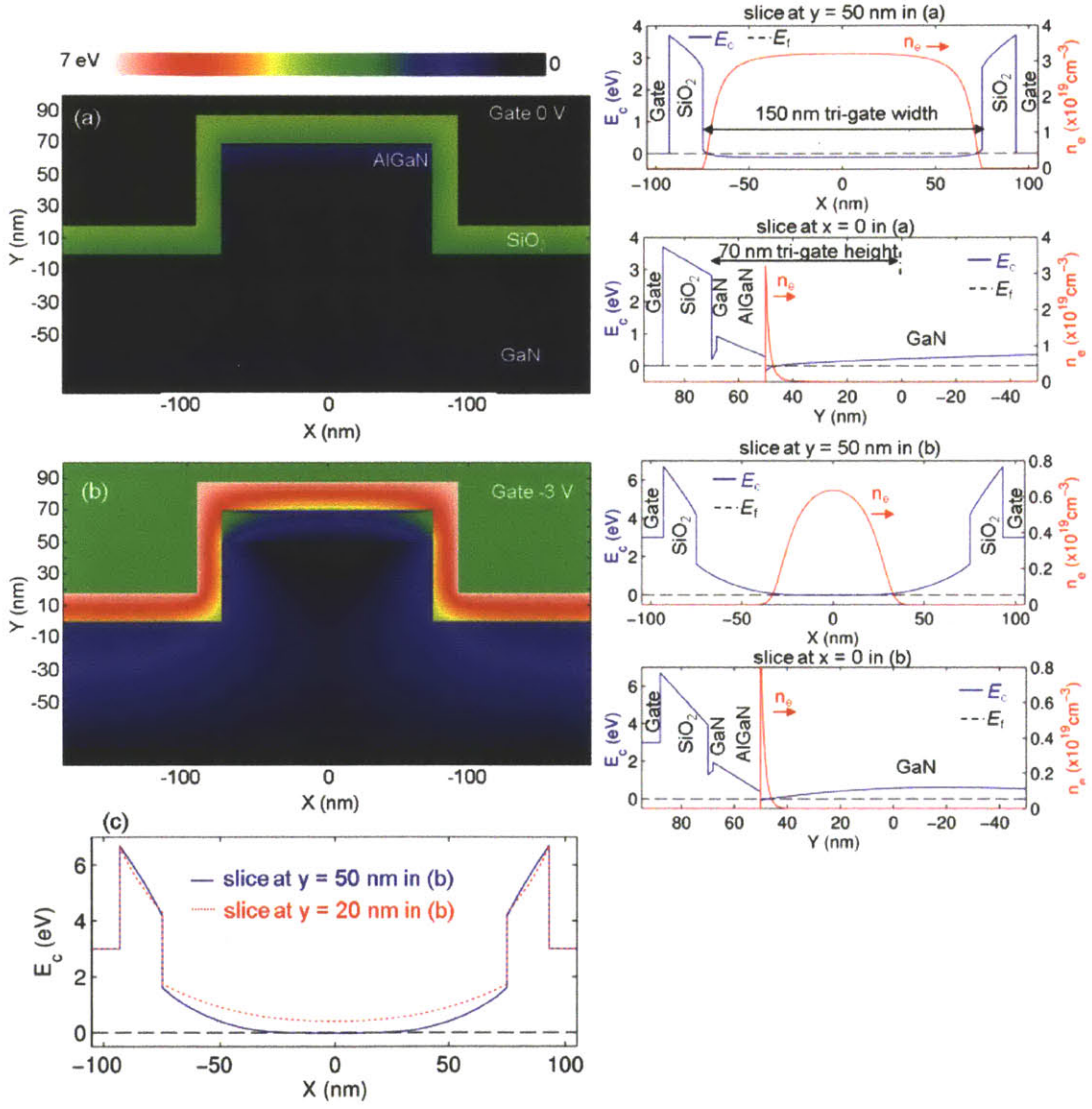

Figure 3-22. Simulated 2D plots of the conduction band edge of the 70-nm-side-wall tri-gate device at gate bias of 0 (a) and -3 V (b) with 1D slices at X = 0 and Y = 50 nm positions. The plot in (c) compares the conduction band energy at y = 50 nm and 20 nm positions in (b).

From the electron density distribution in Figure 3-23, some features in the tri-gate CV characteristic (see Figure 3-21) can be understood. Firstly, the tri-gate device has larger

capacitance per top channel area than the planar device between the gate bias of 0 V and -3 V. This is due to the contribution of the side-gate-to-channel capacitance. The fast decrease of the capacitance between 0 V and -3V is due to the lateral depletion of 2DEG by the sidewall gates which in turn reduces the sidewall-gate-to-channel capacitance. Secondly, the increase of capacitance between bias voltage of 0 V and 1 V is due to the electron accumulation and electron trapping at the SiO_2/GaN interface at the bottom of each tri-gate trenches, as shown in Figure 3-23, which is predicted in section 3.5.2 from geometry arguments. The electron accumulation at this etched bottom surface is only possible because of the existence of positive charges (with a density of $2.28\times10^{13}q/cm^2$) at the SiO_2/GaN interface. As the electrons at this bottom SiO_2/GaN interface are expected to have very poor mobility due to the dry etching damages, this tri-gate trench bottom parasitic capacitance needs to be reduced. For gate bias voltage above 0.5 V, electrons at the AlGaN/GaN interface start to overcome the AlGaN barrier and accumulate at the SiO_2/GaN-cap interface. As a result, electrons do not accumulate on the tri-gate sidewalls in the region below the AlGaN barrier.

As predicted from the piezoelectric simulation in section 3.5.5, there is very little change in strain and piezoelectric charge of the AlGaN barrier when tri-gate sidewall height increases from 70 nm to 350 nm. In fact, with the same Fermi-level pinning position at the GaN-cap layer surface and piezoelectric charge in AlGaN as that used in the 70-nm-sidewall tri-gate device, the simulation predicts the measured pinch-off voltages with relative high accuracy in the measured QSCV results of the 120-nm and 200-nm-sidewall tri-gate devices, as shown in Figure 3-24. (Within the tri-gate height measurement error, using a 110-nm-sidewall instead of 120-nm-sidewall in the simulation gives better match to the measurement.) The discrepancy between the simulation and the measurement on the 350-nm-sidewall tri-gate device is probably due to the side-wall deep donor states, as large upward band bending is observed at about 100 nm below the AlGaN/GaN interface. Nevertheless, the simulation indeed predicts a saturation of pinch-off voltage at the 350-nm side-wall height. The general agreement between the simulation and the measurement shows the self-consistency of the simulation model.

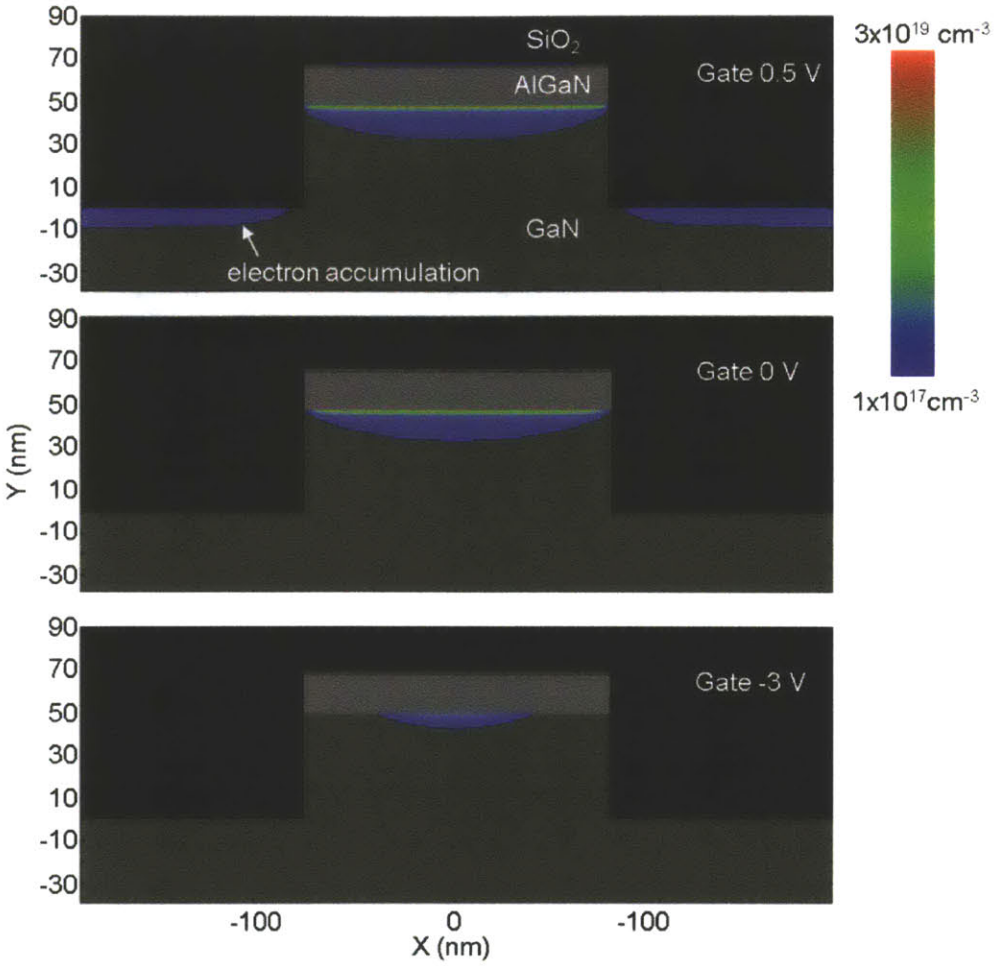

Figure 3-23. Electron density of the 70-nm-side-wall tri-gate device at gate bias of 0.5 V, 0 V and -3 V.

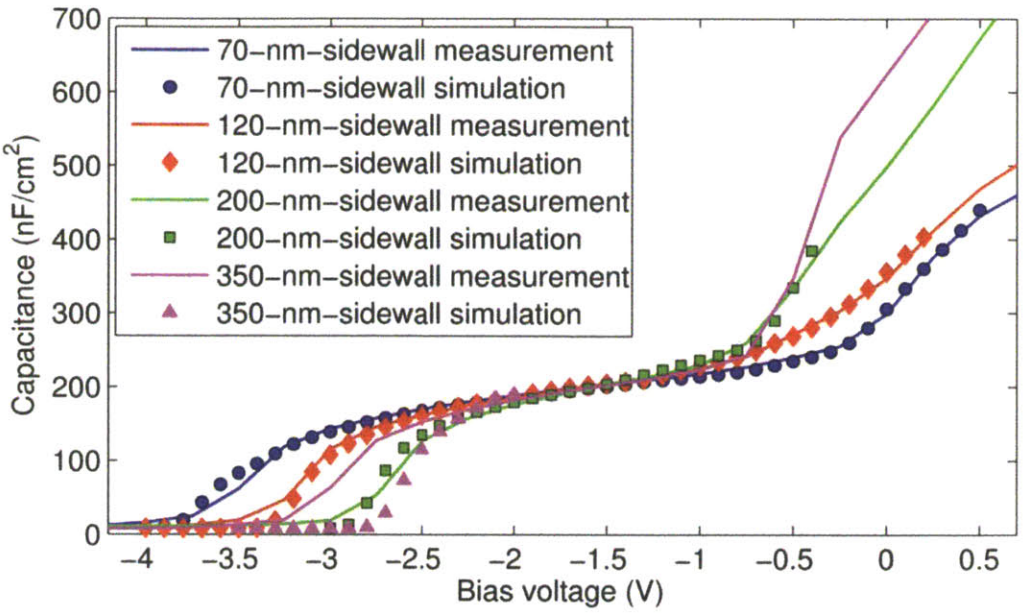

Figure 3-24. Simulated and measured CV curves of tri-gate devices with side-wall heights of 70 nm, 120 nm, 200 nm and 350 nm.

The mechanism for the positive shift of pinch-off voltage as a function of tri-gate side-wall height is due to the increase of sidewall-gate-to-2DEG capacitances (see Figure 3-25) which increases the effect of the sidewall depletion of the 2DEG at the AlGaN/GaN interface. The decreased coupling between the 2DEG and the bottom of the sidewall gates at larger sidewall height causes the saturation of the sidewall-gate-to-2DEG capacitance and thus the pinch-off voltage in the CV curves. The simulated capacitance in Figure 3-25 is for each tri-gate unit structure shown in the inset and normalized in tri-gate length direction. As a result, paralleling more tri-gate channels will increase the device overall gate capacitance. On the other hand, reducing the tri-gate height and channel length will decreases the overall gate capacitance.

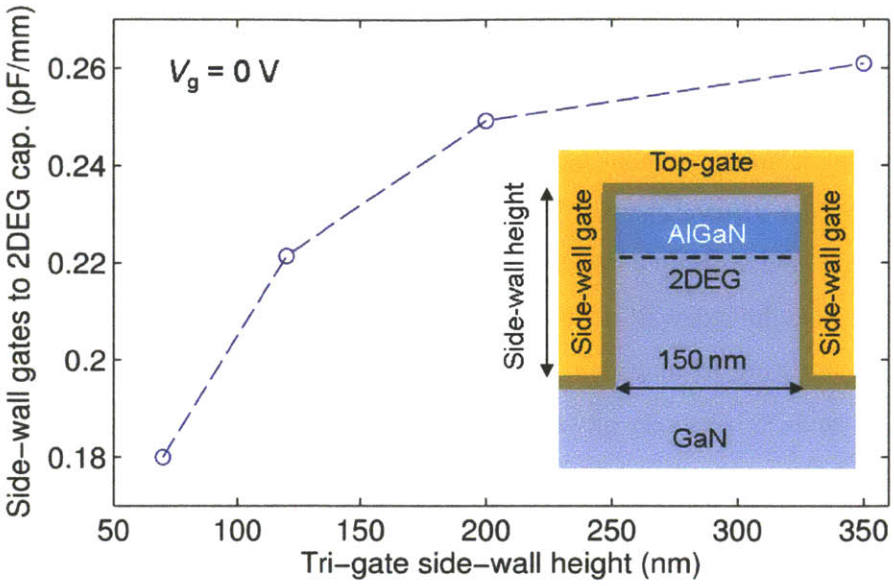

Figure 3-25. Simulated sidewall-gates (one pair) to 2DEG capacitance of each tri-gate structure unit shown in the inset schematic at $V_g = 0$ V. The capacitance is normalized to the tri-gate length direction perpendicular to the cross-section schematic inset. The simulation assumes an ideal side-wall interface without trap states.

3.5.4 Tri-gate Channel Mobility

Effective electron mobility μ_e in the AlGaN/GaN tri-gate transistor channel can be calculated from the tri-gate channel sheet resistance $R_{\text{sh-trig}}$ and 2DEG density $n_{2\text{DEG}}$:

$$\mu_e = \frac{1}{qn_{2\text{DEG}}R_{\text{sh-trig}}}$$

The tri-gate channel resistance can be extracted by measuring R_{on} of tri-gate devices with different tri-gate length L_{trig}. As shown in Figure 3-26(a), R_{on} of the tri-gate transistors have a nonlinear characteristic with the tri-gate length, probably due to the non-uniform strain distribution along the tri-gate length. However, for tri-gate length above 10 μm, R_{on} has good linearity with L_{trig} and therefore we use this region for $R_{\text{sh-trig}}$ extraction.

The channel 2DEG density can be obtained from the simulation fitting to the measured CV curves, as shown in Figure 3-24. As mentioned in section 3.5.3, traps at the sidewall and bottom trenches of the tri-gate structure are needed to fit the overall CV curve (near $V_g = 0$ V). Besides, the trap density cannot be uniquely determined by fitting to a single frequency

CV measurement (QSCV in this case) either. In order to estimate the 2DEG density, the simulation result of the 70-nm-side-wall tri-gate device is used which has the lowest amount of required traps on the sidewall (with an areal density of $2\times10^{11}/cm^2$) and smallest influence (close to none) from the trench-bottom parasitic capacitance for $V_g < 0$ V. As shown in Figure 3-26(b), the tri-gate channel 2DEG density at $V_g = 0$ V is $4\times10^{12}/cm^2$, about half of the planar-gate device 2DEG density of $8.8\times10^{12}/cm^2$. This is mainly due to the strain relaxation because the sidewall depletion width at $V_g = 0$ V is only about 7 nm (see section 3.5.3). It is interesting to note that the simulated 2DEG density of the planar-gate device shown in Figure 3-26(b) is very close to the Hall-measured 2DEG density of $9.3\times10^{12}/cm^2$ in the virgin wafer. It seems that the deposition of ALD SiO_2 gate dielectric on the planar-gate device does not cause significant change to the ionized surface donor states.

The 2DEG mobility of the 70-nm-side-wall tri-gate transistor is shown in Figure 3-26(c), which has a maximum value of 1258 $cm^2V^{-1}s^{-1}$ at a 2DEG density of $4\times10^{12}/cm^2$, which is slightly lower than the 2DEG mobility of 1660$cm^2V^{-1}s^{-1}$ density of $9.3\times10^{12}/cm^2$ in the virgin wafer. Considering the mobility may be slightly underestimated due to some amount of trapped electrons in the QSCV measurement, it can be postulated that the fabrication of the tri-gate sidewalls does not cause significant degradation to channel mobility. The increase of mobility with the 2DEG density is due to the screening of ionized impurities and dislocations [Dang1999]. As will be shown in section 3.6, the 2DEG mobility in the AlGaN/GaN system will decrease at higher density.

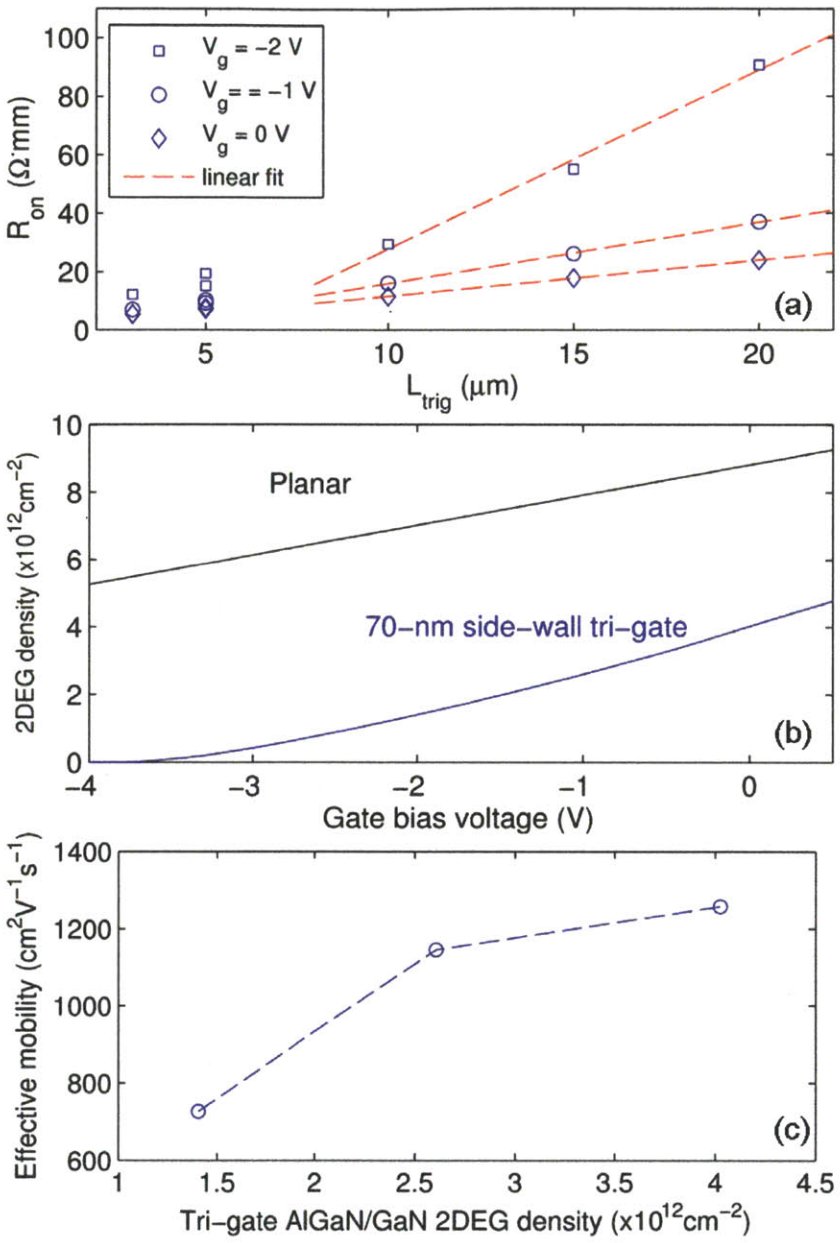

Figure 3-26. (a) R_{on} as a function of tri-gate length L_{trig}; (b) simulated 2DEG density with planar-device as a reference; (c) calculated effective 2DEG mobility; of the 70-nm-side-wall tri-gate transistors.

3.5.5 Strain Relaxation in Tri-gate Structure

Lattice matched $Al_{0.26}Ga_{0.74}N$ grown on GaN has tensile strain with a piezoelectric charge density of $4.41\times10^{12}cm^{-2}$ [see Appendix B]. Similar to the strain relaxation through cracking

in GaN films [Tripathy2002], the tensile strain of AlGaN barrier layer could relax through the surfaces at the sidewalls of the tri-gate structures, which can change the piezoelectric charge in AlGaN. Since the 2DEG in the AlGaN/GaN heterostructure is a function of polarization charges [Ambacher2000], the change of the strain in the AlGaN/GaN tri-gate structure is suspected to have an impact on the density of the 2DEG and the threshold voltage of tri-gate devices. In this section, strain relaxation in the tri-gate structures with sidewall heights of 70 nm, 120 nm, 200 nm and 350 nm is studied. First, Raman scattering measurements were used to determine the strain in the GaN buffer region, whose results are then used as a boundary condition for the finite-element piezoelectric calculation to determine the strain and piezoelectric polarization charge in the AlGaN barrier layer of the tri-gate structures.

- **Raman measurements**

Raman spectroscopy can be used to study the mechanical stress in materials due to the linear relation between the stress and Raman peak shifts [Anastassakis1970]. In this section, Micro-Raman spectroscopy was used to investigate the strain in tri-gate structures. The Raman spectra were measured using a WITec Confocal Raman microscope with an excitation laser wavelength of 532 nm in backscattering geometry configuration. The focal point of excitation laser has a diameter of around 320 nm using an objective with a numerical aperture (N.A.) of 0.9 in air. Raman spectra of planar AlGaN/GaN device are shown in Figure 3-27. The observed Raman phonon modes are GaN E_2 (high), GaN A_1 (LO) and the Si Raman peak from the substrate. The spectra data were fitted with Lorentzian to extract the center frequency and full-width half-maximum (FWHM) of each peak. The GaN E_2 (high) mode is broadened as shown in Figure 3-27, consisting of two Lorentzian peaks. One peak has higher intensity and smaller FWHM of 5.7±0.2 cm^{-1} and the other one has lower intensity, larger FWHM of 14.4±0.5 cm^{-1} and blue shifted, as shown in Figure 3-27(a). The low intensity peak is believed to be the E_2 Raman signal from the superlattice AlGaN buffer since its intensity increases as the excitation laser focus is moved towards the substrate from the surface as shown in Figure 3-27(b). The large FWHM of the buffer E_2 Raman signal is also expected due to large amounts of defects in the buffer layer. On the other hand, the higher intensity and narrow FWHM (indicating good crystal quality) E_2 peak (Figure 3-27(a))

originated from the 1.2 μm i-GaN channel layer. Its intensity decreases as the excitation laser focus is moved towards the Si substrate (Figure 3-27(b)). For all the Raman spectra data, the laser was focused close to the device surface to maximize the Raman signal from the GaN channel layer. Unfortunately, due to the small thickness of the 18 nm AlGaN barrier layer, its Raman signal is too weak to be extracted from the spectrum, as the difference in the E_2 GaN phonon mode frequency of devices with and without AlGaN layer is only 0.3 cm^{-1}, within the measurement error.

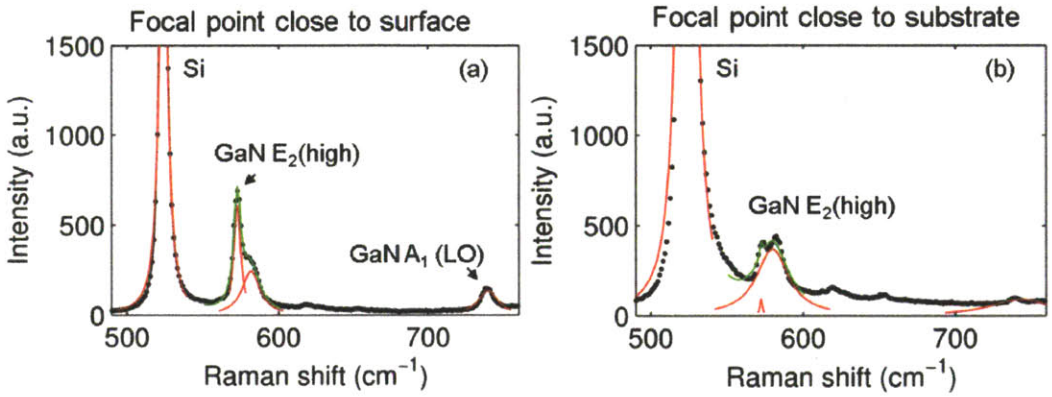

Figure 3-27. Raman spectrum of the planar AlGaN/GaN-on-Si(111) sample (a) with laser focal point in the GaN channel layer; (b) with the laser focal point in the buffer layer. The dots are the measurement data; the red-solid lines are Lorentzian fitting; the green-colored line is the total fitting curve by two Lorentzians.

The Raman spectra were calibrated by setting the Si Raman peak position to its theoretical value of 520 cm^{-1}. In fact, the Si Raman shift at 523.97±0.05 cm^{-1} from the Si(111) substrate is the same, within the measurement error, as the one at 523.99±0.06 cm^{-1} of a bare Si(100) wafer used as a reference, which indicates the Si(111) substrate has very small stress from the AlGaN/GaN epitaxial layers grown on it.

The Raman shift of the GaN E_2 (high) phonon mode as a function of the tri-gate sidewall height is shown in Figure 3-28. The planar device GaN E_2 (high) peak is at 569.1±0.3 cm^{-1}, which is blue shifted compared with strain-free bulk GaN E_2 (high) peak at 568 cm^{-1} [Perlin1992]. As a result, compressive stress of 0.26 GPa and compressive strain of 0.05% in

the GaN channel layer can be calculated using the relation between the biaxial stress and E_2 Raman shift from reference [Kisielowski1996]

$$\Delta\omega = -4.2\ \mathrm{cm^{-1}GPa^{-1}}\sigma_1$$

and the stress-strain relation derived in Appendix A

$$\sigma_1 = \left(C_{11} + C_{12} - \frac{2C_{13}^2}{C_{33}}\right)\epsilon_1 = 476\mathrm{GPa}\ \epsilon_1$$

where $\Delta\omega$ is the change of frequency of GaN E_2 Raman mode compared to stress free GaN; σ_1 is the biaxial stress in the basal plane and ϵ_1 is the biaxial strain.

As the sidewall height of the tri-gate structure increases, the E_2 (high) phonon frequency red shifts by 0.6 cm^{-1} to 568.5±0.2 cm^{-1} at a sidewall height of 350 nm. Because the 0.05% compressive strain in GaN channel layer only changes the piezoelectric polarization by $3\times10^{11}cm^{-2}$ compared to the stress free GaN channel layer, the stress in GaN channel layer is ignored in the finite-element simulation and it does not affect the trend observed in the piezoelectric simulation.

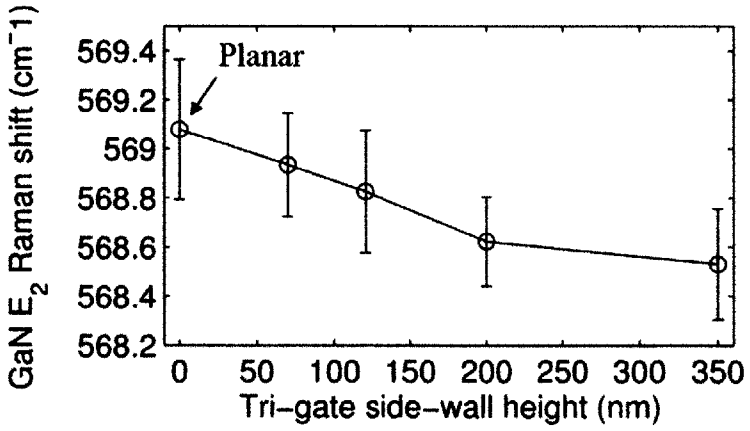

Figure 3-28. GaN E_2 (high) Raman shifts as a function of tri-gate side-wall heights. Each data point is averaged from 15-20 measurements.

- **Finite-element Piezoelectricity Simulation**

Finite-element piezoelectricity simulation was performed to study the relaxation of tensile stress in AlGaN layer of the tri-gate devices using COMSOL Multiphysics simulation software. Since the tri-gate channel length in the study (ranging from 15 um to 100 um) is much longer than its width (150nm), 2D cross-section simulation is sufficient. The detailed elastic and piezoelectricity equations used in this simulation can be found in Appendix A. The configuration of boundary conditions is shown in Figure 3-29. The bottom boundary which is 400 nm deep from the surface is a fixed boundary (clamped without movement in both directions) to simulate the nearly strain free GaN channel layer measured in Raman spectroscopy. The depth of 400 nm is merely an estimation based on the focal point depth of the Raman excitation laser and its variation do introduce changes to the simulation results. However, for a qualitative illustration purpose, it is sufficient to demonstrate the trend in the strain relaxation. The nitride semiconductors are treated as ideal without considering the effects of surface defects produced during fabrication, as they are difficult to model and estimate. As shown in Figure 3-29, the simulated structure represents the tri-gate devices right after the formation of the tri-gate structures and before the deposition of ALD SiO_2 and gate metallization. In order to simplify the extraction the piezoelectric polarization charges at the AlGaN and GaN interfaces, the surface of GaN-cap layer and both sides of AlGaN layers are grounded with same potential. As a result the electric field in these layers is zero so that the electric field coupling in the piezoelectricity equation is eliminated. To compensate this effect, "improper" piezoelectric constants [Bernardini2001] are used in the simulation (See Appendix B).

By setting the $Al_{0.26}Ga_{0.74}N$ layer the initial basal-plane strain to 0.00632 and the c-plane strain to -0.0033 (positive sign–tensile, negative sign–compressive), which correspond to the planar device situation, the relaxation of the strain in AlGaN is simulated as shown in Figure 3-30. The relaxation of the basal tensile strain of AlGaN layer causes the bending of the material.

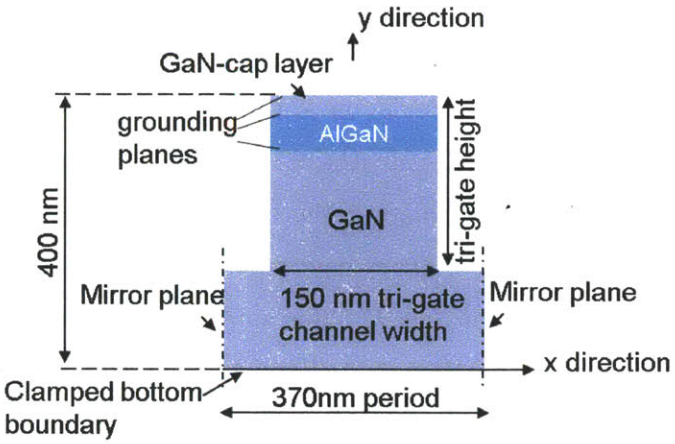

Figure 3-29. Schematic of boundary conditions used in the finite-element piezoelectricity simulation.

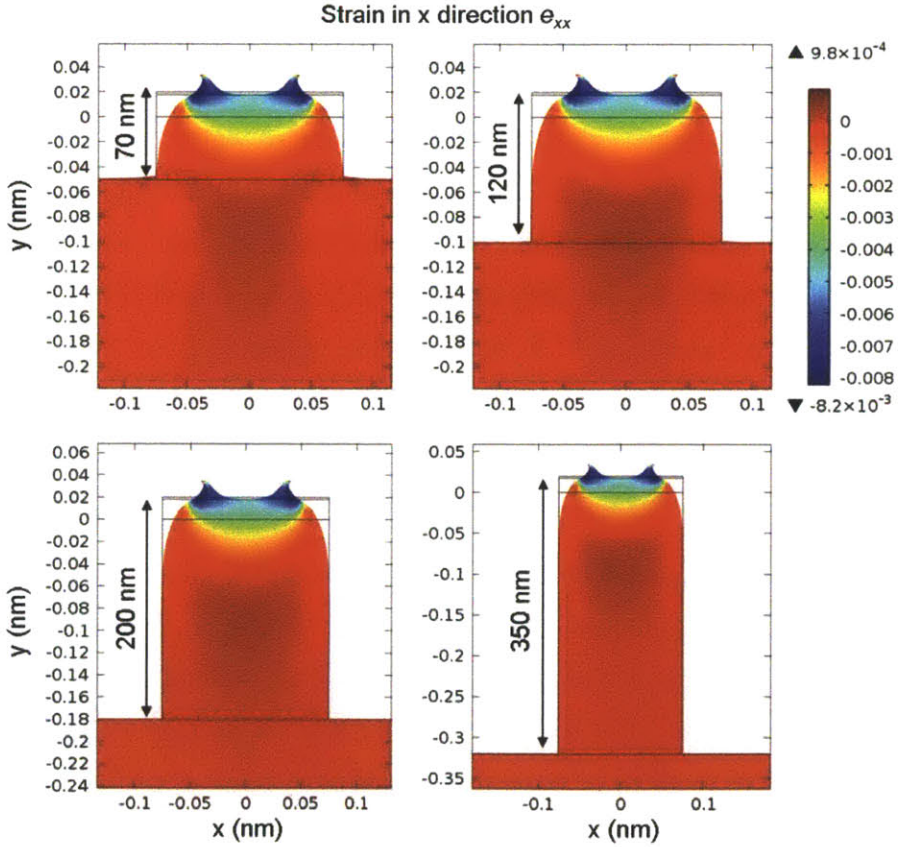

Figure 3-30. Simulated x-axis strain component e_{xx} of the tri-gate structure with different side-wall heights.

Average piezoelectric charges at the interfaces of AlGaN/GaN and GaN-cap/AlGaN and at surface of GaN are extracted from the simulation as shown in Figure 3-31(a). A positive piezoelectric charge of about 1.76-1.77×10^{12}cm^{-2} is formed at the surface of GaN-cap layer because of compressive stress originated from the relaxed AlGaN layer. On the other hand, the positive net piezoelectric charge at AlGaN/GaN interface and negative piezoelectric charge at GaN-cap/AlGaN interface are reduced when the tensile strain in AlGaN is relaxed. Compared to the planar device, the change of piezoelectric charge at AlGaN/GaN interface of tri-gate device with 70 nm side-wall height is about 2×10^{12}cm^{-2}. As tri-gate height increases the change in the piezoelectric-induced charge is very small, less than 2×10^{10}cm^{-2}.

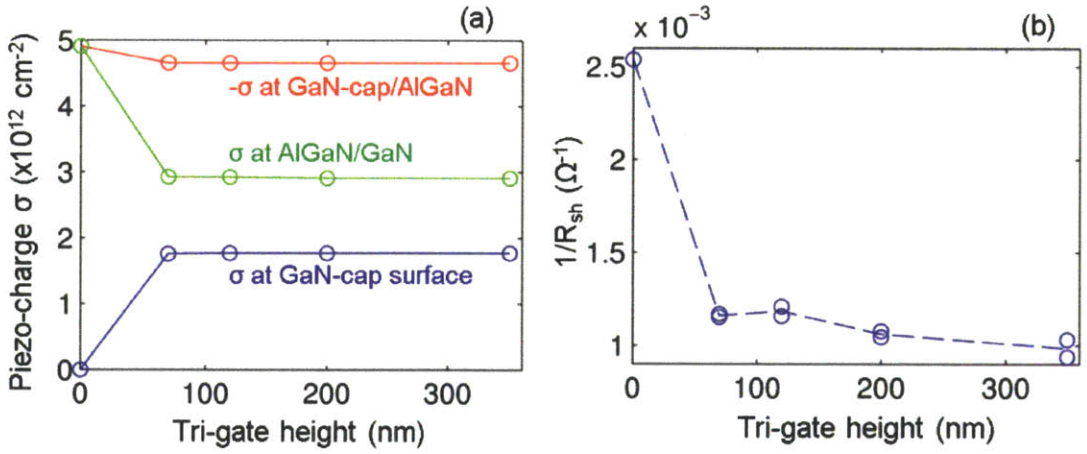

Figure 3-31. (a) Simulated piezoelectric charge density as a function of tri-gate height at interfaces of GaN-cap/AlGaN and AlGaN/GaN and at the surface of GaN-cap layer; (b) inverse of sheet resistance of tri-gate channel as a function of tri-gate height before deposition of gate dielectric. The dashed line is to guide the eyes. Sheet resistance R_{sh} was measured with halogen lamp light illumination on the devices to reduce the side-wall depletion. Tri-gate height of 0 represents the planar device.

The sheet resistance of tri-gate devices before deposition of ALD SiO_2 gate dielectric was measured with illumination of a halogen lamp to reduce the sidewall depletion width. The inverse of the sheet resistance (proportional to 2DEG density) is plotted in Figure 3-31(b). It has a similar shape to the one in Figure 3-31(a) where the largest change appears between the

planar device and 70-nm-side-wall tri-gate device and the change from 70 nm to 350 nm tri-gate heights are small. However, there is no direct linear relation between the polarization charge and the 2DEG density in the AlGaN/GaN structure where surface potential plays an important role. A quantitative analysis of the charge density in tri-gate channel is presented in section 3.5.3.

3.6 GaN Etch-Stop Barrier Structure

As shown in section 3.3 and 3.4, gate recess is a very important process technology for fabricating normally-off AlGaN/GaN HEMTs. In addition, gate recess has been used to reduce short channel effects and improve the current gain cut-off frequency (f_t) in RF AlGaN/GaN HEMTs [Chung2010]. Since both GaN and AlGaN are very inert to wet chemical etchants, chlorine-based dry etching is typically used for gate recess. There are however two major drawbacks in dry plasma etching: 1) it causes plasma damage creating high density of defect states and degrading the channel mobility in the recessed region as seen in both the dual-gate and tri-gate normally-off MISFETs in the previous sections; 2) due to the changes in plasma etch rate, it is difficult to control the recess depth precisely by a timed etching, which causes a variation in the transconductance (g_m) and threshold voltage (V_{th}). This problem becomes even more challenging when multiple devices with different gate lengths are recessed together, as the etching rates are different for different recessed-gate aspect ratios. In this section, a new transistor barrier structure is presented to address the major drawbacks of the conventional gate recess technology.

As shown in Figure 3-32(a), the new transistor structure consists of 22 nm GaN:Si cap layer with ~6×10^{18} cm^{-3} Si doping / 1.5 nm AlN / 3 nm $Al_{0.15}Ga_{0.75}N$ on top of GaN channel. The n-GaN is the carrier donor layer which provides electrons in the channel. The role of the 1.5 nm AlN layer is to shift the conduction band of the n-GaN upwards by as much as 1.5 V thanks to its strong polarization-induced electric field, resulting in a 2DEG density of $7.1\pm0.1\times10^{12}$ cm^{-2}. The AlN also serves as an etch-stop layer for fluorine-based dry-etching of the n-GaN cap layer due to the non-volatility of aluminum fluoride (AlF_3) [Buttari2004]. The 3 nm $Al_{0.15}Ga_{0.75}N$ spacer prevents the gate dielectric in the recessed-gate MISFET from contacting the GaN channel directly, which minimizes interface state density and improves channel mobility. The 3 nm $Al_{0.15}Ga_{0.75}N$ spacer has a 0.24 eV conduction band offset with

respect to the GaN channel layer, which helps to confine most of the channel electrons at the $Al_{0.15}Ga_{0.75}N$/GaN interface and further increases the channel mobility in this device, as compared with the conventional GaN E-mode recess-gate MISFETs.

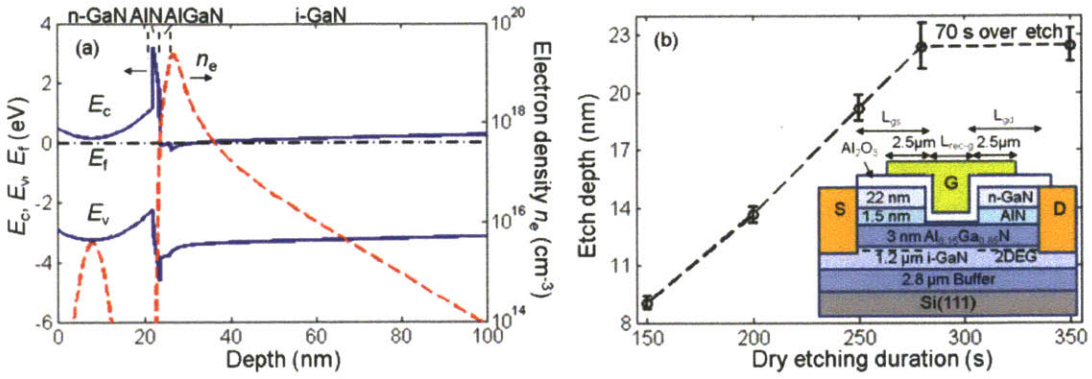

Figure 3-32. (a) Band structure and electron density profile of the new wafer structure. (b) Recess depth as a function of etch duration. The depth was measured by atomic force microscope (AFM). Inset shows the relevant dimensions of a recessed-gate GaN MISFET.

3.6.1 Device Fabrication

The new transistor structure was grown on a 4 inch Si substrate by metal-organic chemical vapor deposition. It consists of a 22 nm GaN:Si cap layer with 3-6×10^{18} cm^{-3} Si doping / 1.5 nm AlN / 3 nm $Al_{0.15}Ga_{0.85}N$ / 1.2 μm i-GaN / 2.8 μm buffer / p-type Si(111) substrate (Figure 3-32(b) inset). As shown in the band structure (simulated by *nextnano*[3] 1D Schrödinger-Poisson solver) in Figure 3-32(a), the n-GaN layer is depleted with a maximum electron density of less than 10^{16} cm^{-3}. Hall measurement shows a sheet resistance of 579±11 Ω/sq and two-dimensional-electron-gas (2DEG) mobility of 1529±18 $cm^2V^{-1}s^{-1}$ with a sheet charge density of 7.1±0.1×10^{12} cm^{-2}. The device fabrication starts with mesa isolation and Ti/Al/Ni/Au ohmic contact formation. To fabricate the recessed-gate transistors, the n-GaN cap in the recessed-gate region was selectively etched over the AlN layer by fluorine-based electron-cyclotron-resonance reactive ion etching (ECR-RIE). Due to the non-volatility of aluminum fluoride (AlF_3) [Buttari2004], high etch selectivity of GaN over AlN is achieved for the gas flow rates of 5 sccm BCl_3/ 35 sccm SF_6 at 35 mtorr with 100 W ECR power and

100 V DC bias. To ensure uniform and complete removal of the n-GaN layer, a 350 s etch was used with 70 s over-etching, as shown in Figure 3-32(b). The surface of the AlN layer was then oxidized by low energy oxygen plasma descum and wet etched by 1 min dip in tetramethylammonium hydroxide (TMAH) at room temperature to remove the dry etching damage. TMAH is chosen over KOH-based AlN etchant [Mileham1995] to prevent possible potassium ion contamination. After 10 min UV-ozone and $HCl:H_2O$ solution surface cleaning [Sohal2010], a 10 nm Al_2O_3 gate dielectric was then deposited by atomic layer deposition (ALD) at 250 °C and annealed at 500 °C for 1min in forming gas. A Ni/Au gate electrode was deposited covering the recessed-gate region with 2.5 μm overhang length as shown in Figure 3-32(b) inset. The sample was then annealed in forming gas at 400 °C for 5 min to reduce the positive fixed charge in Al_2O_3 [Shin2010]. As shown in Figure 3-32(b) inset, the recessed-gate transistors have a recessed-gate length ($L_{rec\text{-}g}$) varying from 3 to 20 μm.

3.6.2 Surface Characterization

X-ray photoelectron spectroscopy (XPS) measurement was used to analyze the chemical composition of the surface of the recessed region of the GaN MISFET. The XPS measurement uses Al K-α X-ray radiation at a take-off angle of 90° with a sampling depth of 3-10 nm. After the BCl_3/SF_6 dry plasma etching, large amount of fluorine was found at the sample surface as shown in Figure 3-33. The fluorine from the dry-etch step was significantly reduced after the O_2 plasma treatment followed by 1 min TMAH wet etch in room temperature as shown in the in Figure 3-33(b).

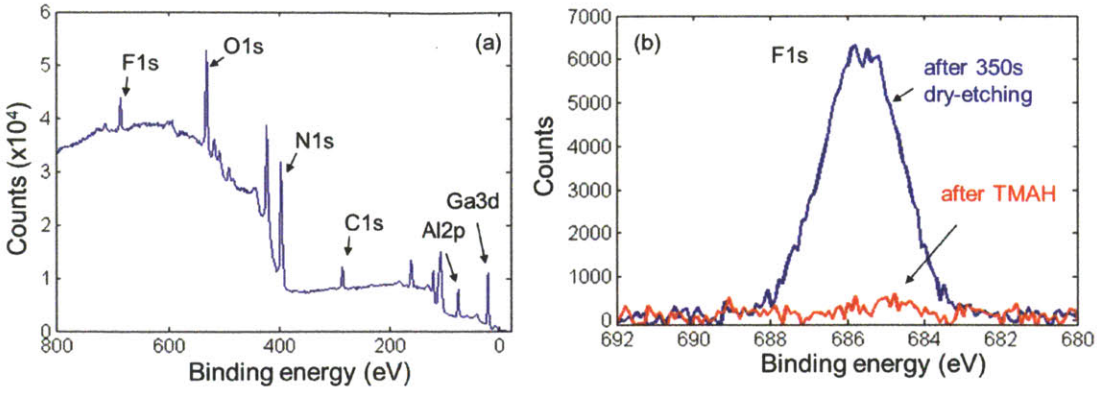

Figure 3-33. XPS measurement of the sample surface (a) after the 350s BCl3/SF6 dry etching; (b) showing the reduction in F1s signal after O_2 plasma treatment and 1 min TMAH wet etch.

From the XPS atomic ratio Al2p / (Al2p + Ga3d) calculated from Al2p and Ga3d core level spectra, the etching of the 1.5 nm AlN with TMAH and the effect of the UV-ozone/HCl surface cleaning can be studied. As shown in Figure 3-34, the Al2p atomic ratio decreases with the etch time of the sample in 70°C TMAH solution after the 350 s BCl3/SF6 dry etch. This indicates that at 70°C the TMAH etches the crystalline AlN. It is also selective over the $Al_{0.15}Ga_{0.85}N$ as seen in Figure 3-34 where the Al atomic percentage stays constant after 40 min etch. We have also confirmed that at room temperature the TMAH barely etches the crystalline AlN. However, by oxidizing the AlN surface with O_2 plasma and a subsequent wet etch in room temperature TMAH solution, a monolayer of AlN can be removed, as shown in Figure 3-34. Three cycles of oxidation/TMAH removes the 1.5 nm AlN layer, giving the same Al atomic ratio as the one after 40 min 70 °C TMAH wet etch. Therefore, each oxidation/TMAH cycle etches 0.5 nm AlN corresponding an atomic layer of AlN with a lattice constant of 4.98 Å in c-axis. As a result, after one cycle of O_2 plasma oxidation/TMAH wet etch and UV-ozone/HCl:H_2O surface cleaning steps (XPS data shown in Figure 3-34), the remaining thickness of the AlN layer is 0.5 nm. The ALD Al_2O_3 was then deposited on top of the 0.5 nm AlN layer. As shown in device simulation in section 3.6.4, the 0.5-nm-thick AlN layer creates a large conduction band off-set with respect to the $Al_{0.15}Ga_{0.85}N$, which is another barrier for the electrons that overcome the $Al_{0.15}Ga_{0.85}N$ layer at large forward bias conditions.

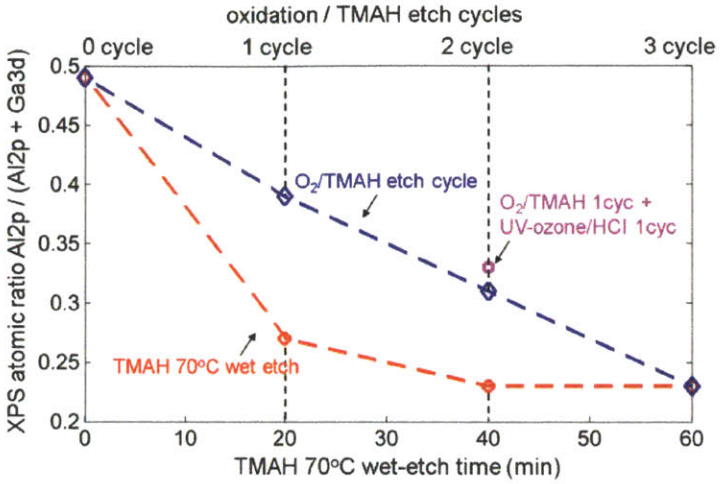

Figure 3-34. XPS atomic ratio of Al2p / (Al2p + Ga3d) as a function of TMAH wet-etch time at 70 °C (red circles) and as a function of oxidation / TMAH etch cycles (diamonds). The zero point in x-axis is after 350 s BCl_3/SF_6 dry etching removing the n-GaN layer. A data point (square) also shows the result after 1 cyc of O_2/TMAH followed by 1 cyc of UV-ozone/HCl.

3.6.3 DC Characterization

The DC characteristics of the recessed-gate GaN MISFET are shown in Figure 3-35. The device threshold voltage (V_{th}) is extracted from equation $V_{th} = V_{gsi} - 0.5V_{ds}$ [Schroder], where V_{gsi} is the interception voltage from the linear extrapolation of I_d-V_{gs} curve in Figure 3-35(a). Small drain voltage (V_{ds} = 0.1 V) is applied to ensure the device is in linear operation region. Averaging over 13 devices, the recessed-gate GaN MISFETs have a V_{th} of 0.30±0.04 V. The average sub-threshold slope is 62±1 mV/decade. The bi-directional gate voltage sweep in the transfer characteristics in Figure 3-35(a) shows less than 10 mV hysteresis in the threshold voltage. The recessed-gate transistor has a similar on-resistance (R_{on} = 10 Ω·mm) as the planar-gate transistor with the same source-to-drain distance (L_{sd} = 11 μm), as shown in Figure 3-35(b). The relatively low maximum drain current of both devices is due to the large gate length (8 μm in planar-gate device and 3 μm in recessed-gate device) and gate-to-source distance (1.5 μm in planar-gate device and 4 μm in recessed-gate device), relatively low

2DEG density (7.1×10^{12} cm^{-2}) and high contact resistance (1.2 Ω·mm) of the non-optimized ohmic contact technology.

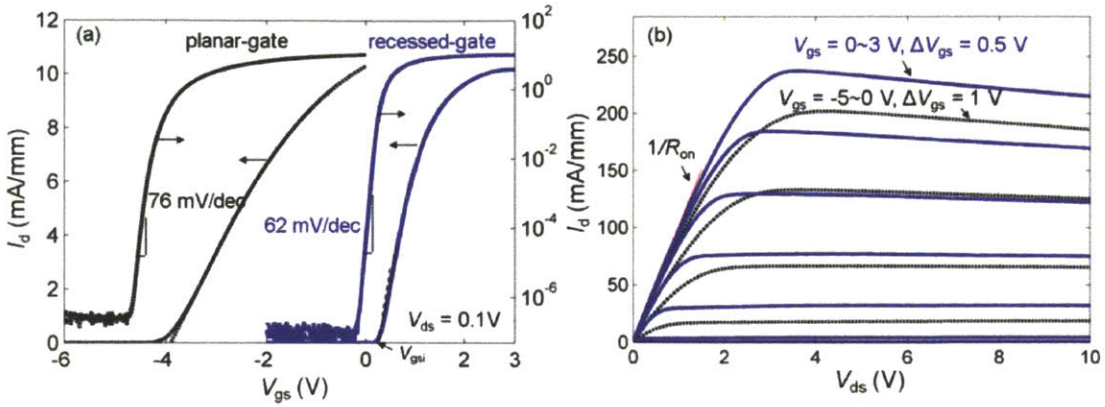

Figure 3-35. (a) I_d-V_{gs} characteristics at V_{ds} = 0.1 V with bi-directional gate sweep; (b) I_d-V_{ds} characteristics. The recessed-gate transistor has $L_{rec\text{-}g}$ = 3 μm and L_{gs} = L_{gd} = 4 μm. The planar-gate transistor (dashed line) has the same Lsd with L_g = 8 μm and L_{gs} = L_{gd} = 1.5 μm.

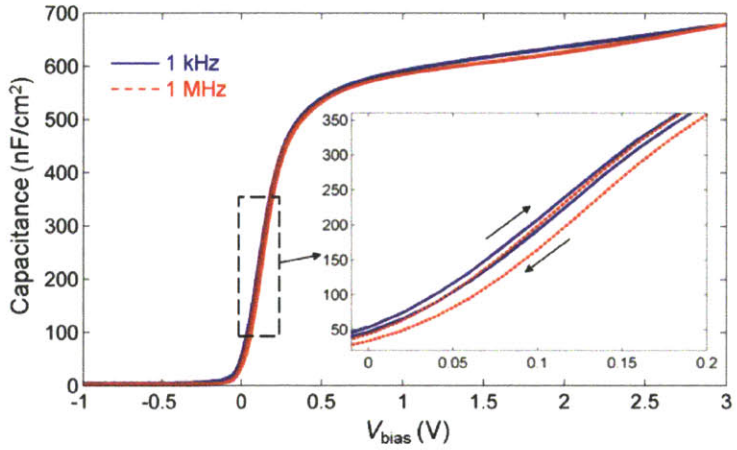

Figure 3-36. C-V characteristics of the recessed-gate capacitor measured at 1 kHz (solid line) and 1 MHz (dashed line) with bi-directional sweeps. Inset zooms in the dashed rectangular region.

To study the Al_2O_3/AlN interface trap density, capacitance-voltage (CV) characteristics (Figure 3-36) were measured on recessed-gate capacitors after subtracting the parasitic

capacitance from the gate-2DEG overlapping region (Figure 3-32(b) inset). The CV characteristics have very low frequency dispersion between 1 kHz and 1 MHz and small hysteresis under bi-directional CV sweeps, which indicates very low Al_2O_3/AlN interface trap density in the recessed-gate region.

The effective channel electron mobility of the GaN normally-off MISFETs, μ_e, as a function of gate-to-source voltage (V_{gs}) can be extracted from $\mu_e = 1 / (qN_{sh}R_{ch})$ where q is the electron charge (1.6×10^{-19} C), R_{ch} is channel sheet resistance and N_{sh} is channel accumulation charge density (in cm^{-2}). R_{ch} was extracted from the slope of the R_{on} *vs.* $L_{rec\text{-}g}$ curves in Figure 3-37(a). N_{sh} was extracted by integrating the 1 MHz CV characteristic in Figure 3-36: $qN_{sh} = \int_{-\infty}^{V_{GS}} CdV$ [Schroder]. R_{ch}, N_{sh} and μ_e are summarized in Table 3-1 along with gated-Hall measurement data from the recessed-gate van de Pauw structure.

Table 3-1. Channel resistance R_{ch} (Ω/sq), charge density Q_{ch} ($\times10^{12}$ cm^{-2}) and electron mobility μ_e ($cm^2V^{-1}s^{-1}$) as a function of V_{gs} (V) extracted from DC/CV measurements and gated-Hall measurement. R_{ch} is too large at V_{gs} = 1 V to give a reliable Hall measurement.

	R_{ch}		N_{sh}		μ_e	
V_{gs}	DC	Hall	CV	Hall	effective	Hall
1	2367±126	-	2.90±0.11	-	911±60	-
1.5	1195±60	1114±134	4.75±0.11	4.2±0.4	1100±61	1336±205
2	829±81	783±56	6.67±0.11	5.8±0.4	1131±112	1376±137
2.5	695±87	679±20	8.65±0.11	7.1±0.3	1040±131	1296±67
3	677±90	683±11	10.71±0.13	8.2±0.3	862±115	1116±45

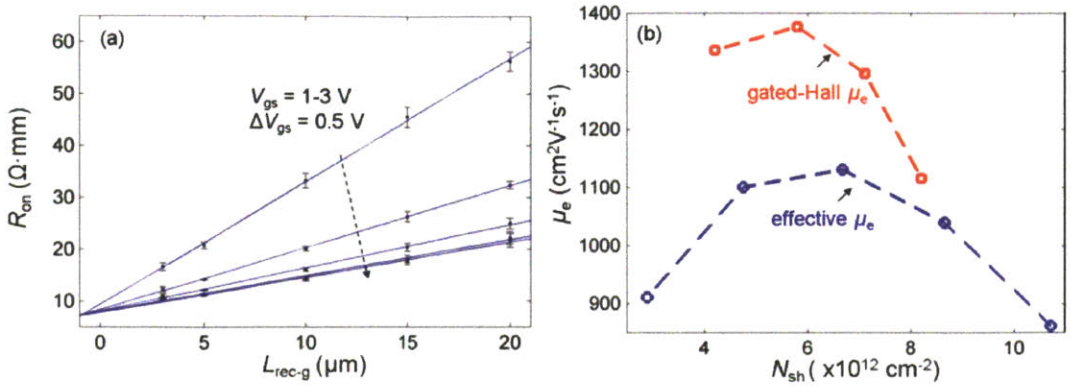

Figure 3-37. (a) R_{on} as function L_{rec-g} at V_{gs} = 1 to 3 V. The slope of each curve gives R_{ch}. (b) μ_e as a function of N_{sh} of the recessed-gate GaN MISFET extracted from DC/CV measurements and gated-Hall measurement.

The extracted R_{ch} from DC characteristics agrees with the gated-Hall measurement. However the extracted N_{sh} from CV measurement is larger than the gated-Hall measurement and the difference grows as V_{gs} increases. As shown in the device simulation in the next section, this is because at higher V_{gs} voltages, an increasing number of the channel electrons overcome the AlGaN barrier and accumulate at the AlN/$Al_{0.15}Ga_{0.85}N$ interface. Since these electrons have low mobility due to alloy scattering and interface roughness scattering [Dang1999, Sun1980], they contribute little to the channel current and make no change to R_{on} even at high gate voltages (Figure 3-37(a)). Therefore the gated-Hall measurement gives a lower 2DEG density at the $Al_{0.15}Ga_{0.85}N$/GaN interface than the value extracted from the CV characteristics.

Figure 3-37(b) plots μ_e as function of 2DEG density N_{sh}. The increase of μ_e at low N_{sh} is due to the reduced carrier scattering by the ionized impurities and dislocations which are screened with more channel charges [Dang1999]. The decrease of μ_e at high N_{sh} is due to the increased alloy scattering and the interface roughness scattering [Smorchkova1999]. The maximum effective mobility is 1131 cm^{2}V^{-1}s^{-1}, which is 10 times higher than the previously reported results on normally-off GaN MISFETs [Oka2008, Im2010, Lu2010Sep1].

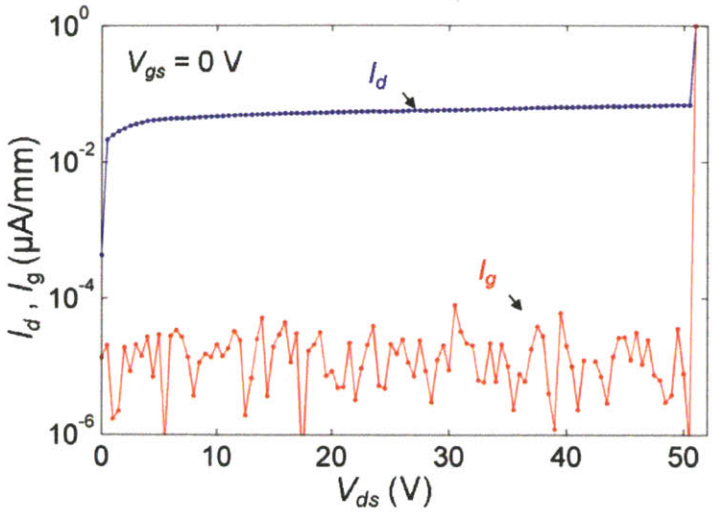

Figure 3-38. Three-terminal BV measurement of the recessed-gate normally-off GaN MISFET with $L_{rec\text{-}g}$ = 3 μm, L_{gd} = 13 μm at V_{gs} = 0 V.

The three-terminal breakdown voltage (BV) was measured on the recessed-gate GaN MISFET with V_{gs} = 0 V and $L_{rec\text{-}g}$ = 3 μm and L_{gd} = 13 μm (Figure 3-38). A breakdown voltage of 50 V was measured for a drain leakage current of 68 nA/mm. The breakdown was caused by the gate dielectric breakdown at the drain side of the gate. As a result, the device is shorted between the drain and the gate while the gate-to-source dielectric remains intact, with the normally-off channel still blocking the drain from the source.

3.6.4 CV Simulation

To better understand the device operation, CV characteristics of the normally-off GaN MISFETs with the etch-stop structure are simulated by solving 1D self-consistent Schrodinger-Poisson equations with the device simulator nextnano3. Although there are some variations in the reported parameters of III-Nitride semiconductors in the literature, they produce only small differences in the simulation results. A set of parameters that produce the best simulation results was chosen and their details can be found in Appendix B with the nextnano3 simulation code in Appendix C.

The calculated net polarization charges $\sigma_{net} = \sigma_{SP} + \sigma_{PZ}$ at $Al_{0.15}Ga_{0.85}N$/GaN and AlN/ $Al_{0.15}Ga_{0.85}N$ interfaces are $+6.06\times10^{12}q/cm^2$ and $+5.98\times10^{13}q/cm^2$, where $q = 1.6\times10^{-19}$ C.

There is also a large negative polarization bound charge of $-8.71\times10^{13}q/\text{cm}^2$ at the surface of AlN.

ALD Al_2O_3 band gap of 6.4 eV was used in the simulation [Nguyen2008]. The conduction band offset of Al_2O_3 on GaN is 2.1 eV according to references [Robertson2006, Esposto2011]. The barrier height for Ni/Al_2O_3 interface is 3.5 eV [Afanas'ev2002]. Because the photoresist developer (AZ422) contains TMAH which etches a few nanometers of Al_2O_3 during gate lithography, the exact thickness of Al_2O_3 is unknown. However, only the ratio of dielectric constant to the thickness of Al_2O_3 matters in the simulation. As a result, a dielectric constant of 8 was used based on reference [Afanas'ev2002] and the thickness of Al_2O_3 was used as a fitting parameter around the value measured by ellipsometer.

- **Simulation Results**

The simulated CV characteristics of the normally-off MISFET with the etch-stop structure is shown in Figure 3-39. The simulated CV characteristics match very well the measured results. The simulated low-frequency (LF) CV curves takes into account all the charges including both accumulated electrons and Al_2O_3/AlN interface trap charges (C_{total} as in section 3.5.3), while the simulated high-frequency (HF) CV only takes into account the free electrons (C_n as in section 3.5.3). By matching the simulation with the measurement results, the Al_2O_3 thickness is determined to be 8.3 nm, instead of the 10 nm measured by ellipsometer after ALD. This discrepancy indicates that about 1.7 nm Al_2O_3 was etched by photoresist developer during gate lithography step. Instead of a nominal 3 nm $Al_{0.15}Ga_{0.85}N$, 2.5 nm $Al_{0.15}Ga_{0.85}N$ is used to have the best fitting to the measurement. The small 0.5 nm of one atomic layer thickness difference is reasonable considering the variation of epi-layer thickness from the MOCVD growth.

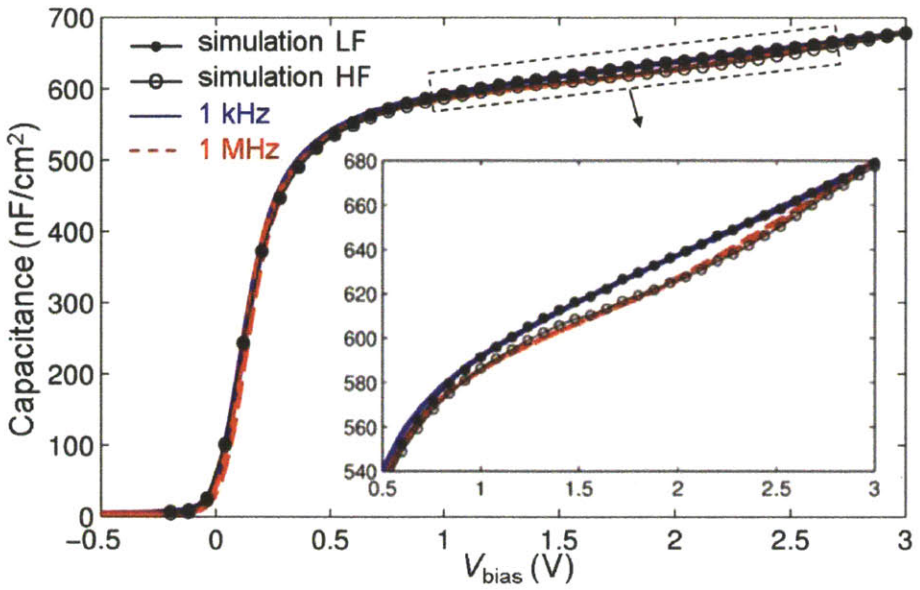

Figure 3-39. Simulated low-frequency (LF) and high-frequency (HF) CV characteristics match with measured 1kHz and 1MHz CV curves. Inset zooms in the dashed rectangle region, showing the dispersion caused by interface states.

Consistent with the surface donor model presented in section 3.5.3, positive charges at the Al_2O_3/AlN interface are also needed in the simulation to fit the device threshold. These positive charges have a density of $2.3\times10^{13}q/cm^2$ with an uncertainty less than $4\times10^{12}q/cm^2$ due to variations in the reported band gap, band alignment and polarization parameters of III-Nitride semiconductors. ALD Al_2O_3/III-Nitrides interface positive charges were also reported at the Al_2O_3/AlN interface ($6\times10^{13}q/cm^2$ [Ganguly2011]) and at Al_2O_3/GaN interface ($4.6\times10^{12}q/cm^2$ [Esposto2011]). These positive charges could be the ionized donor states according to the surface donor model. However, their origin is unlikely to be the mid-gap donor states at E_v + 3.1 eV reported in reference [Miao2009], which is below the Fermi-level as shown in the band diagram in Figure 3-40. Other possibilities are surface states due to the surface contaminants such as absorbed oxygen which are not considered in [Miao2009].

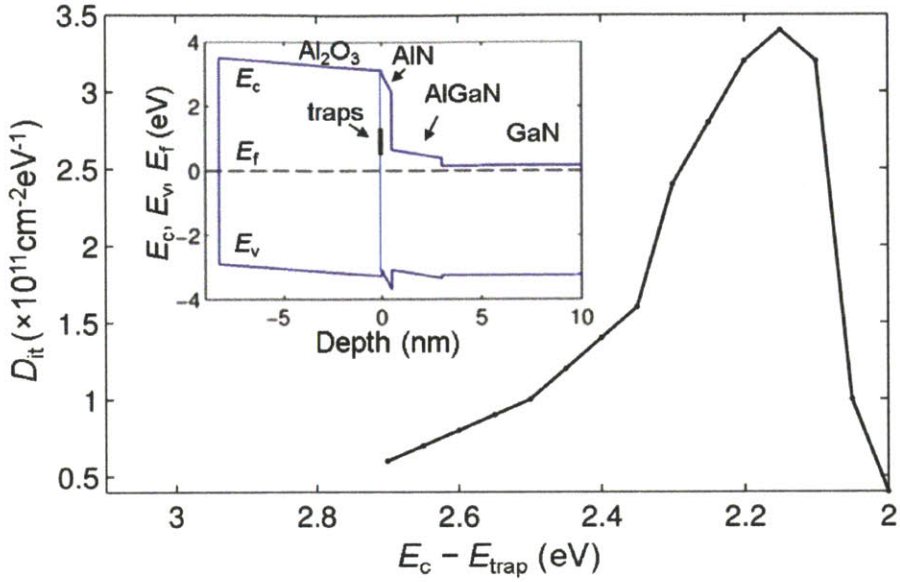

Figure 3-40. Al_2O_3/AlN interface trap density (D_{it}) *vs.* energy level relative to conduction band edge of AlN (E_c-E_{trap}). The inset shows the location of the traps in the band structure of the device at zero bias voltage.

In order to reproduce the frequency dispersion in the CV characteristics (shown in the inset of Figure 3-39), Al_2O_3/AlN interface traps were included in the simulation. The interface trap density (D_{it}) extracted from simulation is shown in Figure 3-40. The majority of the traps are located between 2.1 eV and 2.4 eV below the conduction band edge of AlN (or 3.7-4 eV above valance band maximum) with a maximum value of 3.4×10^{11}cm^{-2}eV^{-1} at 2.15 eV. The uncertainty of the trap location can be as large as 0.3 eV due to the variance in the reported band alignment in III-nitride semiconductors. There are only limited studies in the literature on the surface states of AlN. Using first-principles calculations, Miao *et al.* reported unoccupied states at approximately 1 eV below conduction band edge for a clean AlN surface [Miao2009]. On the other hand, Northrup *el al.* reported surface states at about 4 eV above the valance band maximum [Northrup1997] but the band gap of AlN in their calculation was only 4.1 eV. The discrepancy between our result and the literature is probably because of the differences in the Al_2O_3/AlN interface in our device and the clean free surface of AlN assumed in the calculations in [Miao2009].

The electron distribution in the device at V_{gs} of 0, 1 V, 2 V and 3 V are shown in Figure 3-41. At V_{gs} = 1 V, the electrons are accumulated at the $Al_{0.15}Ga_{0.85}N$/GaN interface. At V_{gs} = 2 V, some electrons overcome the conduction band barrier of $Al_{0.15}Ga_{0.85}N$. At V_{gs} = 3 V, even more electrons are injected into the $Al_{0.15}Ga_{0.85}N$ layer and accumulate in the triangular quantum well at the AlN/$Al_{0.15}Ga_{0.85}N$ interface.

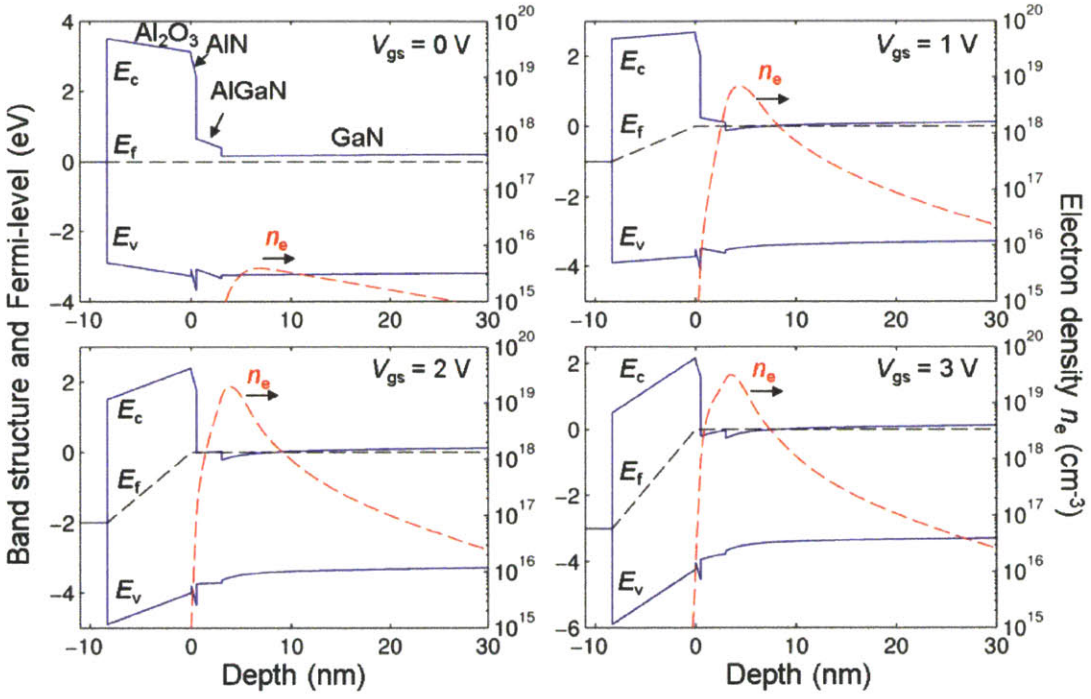

Figure 3-41. Simulated band diagram and electron density at V_{gs} = 0, 1, 2 and 3 V.

As a result, the total accumulated electrons can be divided into two groups based on their location. One group is located in the GaN, primarily at the $Al_{0.15}Ga_{0.85}N$/GaN interface and the other group is in $Al_{0.15}Ga_{0.85}N$. As shown in Figure 3-42, the electron density in GaN starts to saturate at V_{gs} = 2 V with increasingly more electrons inside $Al_{0.15}Ga_{0.85}N$. Due to alloy scattering and Al_2O_3/AlN interface roughness scattering, electrons in $Al_{0.15}Ga_{0.85}N$ have low mobility and contribute little to channel current. As a result, the gated-Hall measurement mainly probes the electrons in GaN. Indeed the electron sheet density from the gated-Hall measurement matches well with the simulated electron density in GaN as shown in Figure

3-42. This again proves the high accuracy of the simulation. Unfortunately, the electron mobility in $Al_{0.15}Ga_{0.85}N$ layer cannot be reliably determined due to the relatively large standard deviations in the sheet resistance shown in Table 3-1.

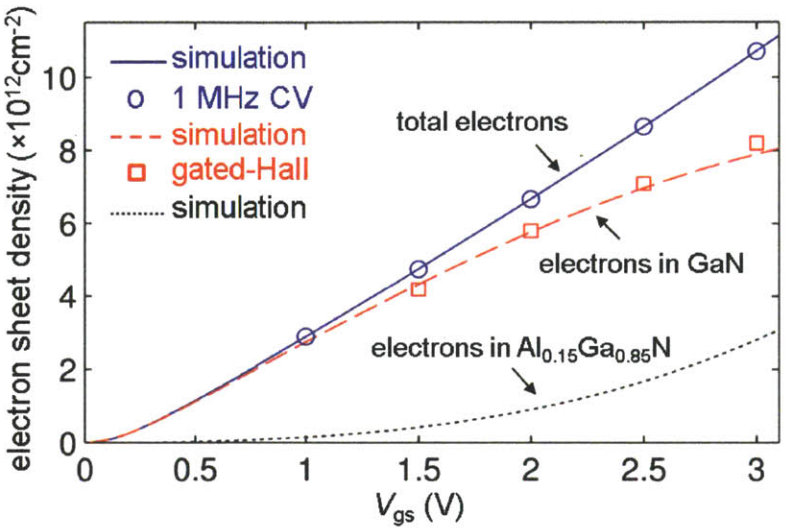

Figure 3-42. Simulated sheet electron density inside GaN and $Al_{0.15}Ga_{0.85}N$ with measured sheet electron density from 1 MHz CV and gated-Hall measurements.

From the simulation, we can also identify the potential problem with the scaling of gate dielectric thickness. As shown in the flat band diagram in Figure 3-43, the large residual electric field in Al_2O_3 is oriented towards the gate causing the conduction band of Al_2O_3 to tilt upwards. As a result, increasing the thickness of Al_2O_3 will shift the flat-band voltage in the negative direction resulting in a negative threshold voltage. This is undesirable for high voltage normally-off power transistors which require thick gate dielectric and large positive threshold voltage. The origin of the electric field in the Al_2O_3 is the large positive charge at the Al_2O_3/AlN interface. The negative shifting of flat-band voltage as a function of increasing thickness of ALD Al_2O_3 has also been observed in ALD Al_2O_3/AlN/GaN MIS-HEMT [Ganguly2011] and ALD Al_2O_3/n-GaN MISFET [Esposto2011]. It is therefore very important to understand the origin of the large positive charge at the ALD Al_2O_3/III-Nitride

interface in order to successfully fabricate normally-off power transistors with large threshold voltage.

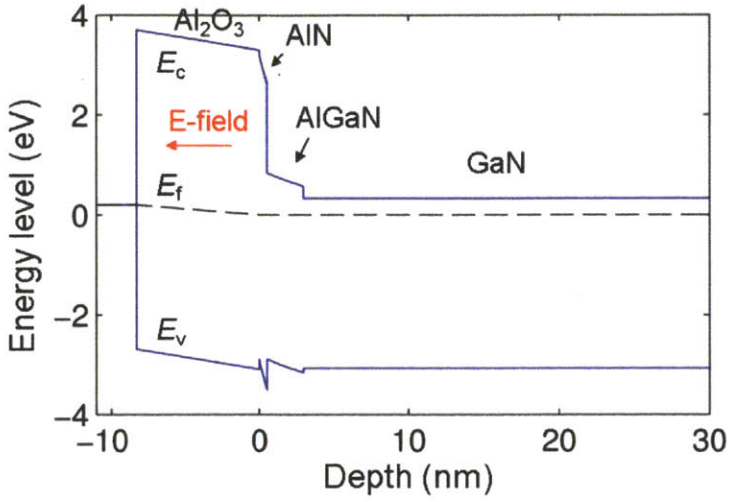

Figure 3-43. Band diagram at flat-band condition showing the electric field (E-field) direction in Al_2O_3.

3.7 Conclusion

In summary, the three novel transistor structures presented in this chapter has addressed three major obstacles in the development of high performance normally-off GaN transistors.

The idea in the design of the dual-gate structure is to decouple the device threshold voltage from its breakdown capability by integrating a two transistor cascode circuit into one transistor so that the high-resistive E-mode channel region can be minimized while the device breakdown voltage is still high. Transistors fabricated using the dual-gate structure demonstrated high threshold voltage (V_t = 2.9 V), high current density (I_{dmax} > 400 mA/mm) and breakdown voltage of 643 V (at I_d = 1 mA/mm). However these devices have high off-state leakage current (about 0.1 mA/mm), which is identified as a common problem in normally-off GaN transistors due to the parasitic leakage path underneath the E-mode

channel. These transistors also have very low channel mobility due to the recess-etch damage and poor dielectric/channel interface.

The tri-gate normally-off transistor solved the leakage issue and demonstrated a true normally-off operation with a leakage current as low as 0.6 μA/mm at breakdown voltage of 565 V. 2D piezoelectric and electrical simulations of AlGaN/GaN tri-gate transistors show that the reduction of the piezoelectric charge in the AlGaN layer due to the its relaxation of tensile strain is the major cause in the large positive threshold voltage shifts in these devices. The impact of the piezoelectric effect in AlGaN on device threshold voltage is through the modulation of the surface positive charge or ionized surface donor states. By assuming the surface Fermi-level pinning in the device model, the simulation self-consistently reproduces the measured changes in the threshold voltage of the tri-gate transistors of different sidewall heights.

The electrostatics of the tri-gate AlGaN/GaN is also understood. The 2DEG at the AlGaN/GaN interface in the tri-gate transistors is predominantly depleted from the sidewall gates due to the closer distance of the sidewall-gate to the channel. No sidewall channel is observed (except at the interception of the 2DEG and the sidewall). The capacitance of the sidewall-gate has saturation characteristics with increasing sidewall height because of the decreased electrical coupling between the bottom side of the sidewall and the 2DEG. The extracted channel electron mobility in the tri-gate AlGaN/GaN tranasistors showed less than 25 % reduction compared to that of the virgin AlGaN/GaN wafer, which indicates that the fabrication of the sidewall do not cause significant degradation to the 2DEG mobility.

Finally, the design of the GaN-etch-stop structure solves the fundamental issue in the conventional gate recess technology. The fabricated normally-off transistors using the GaN-etch-stop technology demonstrated high uniformity in device threshold voltage (0.30±0.04 V) and subthreshold slope (62±1 mV/decade). The device also has good gate-dielectric interface quality with a maximum D_{it} of $3.4\times10^{11}cm^{-2}eV^{-1}$ extracted from CV measurement and simulation. Device CV simulation shows that the conduction band offset at $Al_{0.15}Ga_{0.85}N$/GaN interface is able to keep most of the electrons from injecting into the low mobility $Al_{0.15}Ga_{0.85}N$ region. As a result, a record effective mobility of 1131 $cm^2V^{-1}s^{-1}$ is demonstrated for the first time in the recessed-gate normally-off GaN transistors. The CV

simulation is also able to predict the Hall measurement results with very high accuracy, which has built the foundation for precise device modeling of GaN transistors.

Chapter 4 Dynamic On-resistance Measurement

This chapter presents a new measurement technique for extracting the dynamic on-resistance of transistors. Using this technique, the dynamic on-resistance of commercial GaN power transistors under soft- and hard-switching conditions has been measured for the first time.

4.1 Introduction

It has been observed that the output current and on-resistance of radio-frequency (RF) and high voltage AlGaN/GaN high-electron-mobility transistors (HEMTs) depend on the switching frequency and bias conditions. For example, as shown in Figure 4-1, when an AlGaN/GaN HEMT is switched from the high voltage off-state to the on-state, its on-resistance R_{on} becomes larger and its output current lower than that measured at low voltage DC conditions. The R_{on} measured under switching conditions is typically called dynamic R_{on}, while the reduction in current is referred to as current collapse. When the switching frequency and the off-state voltage are increased, the dynamic R_{on} and the current collapse increase. As a result, the performance of AlGaN/GaN is greatly degraded.

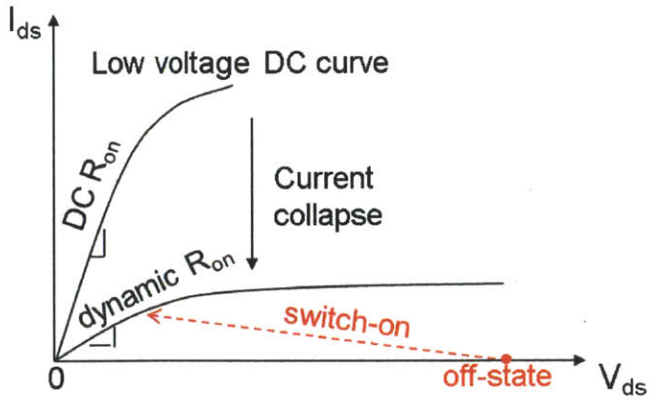

Figure 4-1. Illustration of current collapse and increase of dynamic on-resistance R_{on} when an AlGaN/GaN HEMT is switched-on from high voltage off-state to on-state.

It is believed that this problem is caused by charge trapping in the buffer and on the surface of AlGaN/GaN HEMTs [Klein2001, Rudzinski2006, Binari2001, Vetury2001, Koley2003, Verzellesi2005, Gao2012]. As illustrated in Figure 4-2, these trapped electrons can deplete the two-dimensional-electron-gas (2DEG) in the channel, causing current collapse and the increase of dynamic R_{on}.

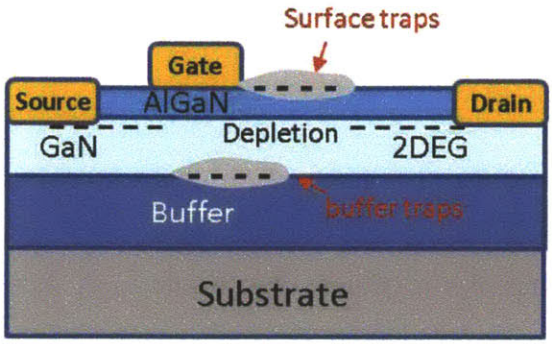

Figure 4-2. Illustration of charge trapped on the surface and in buffer of an AlGaN/GaN HEMT.

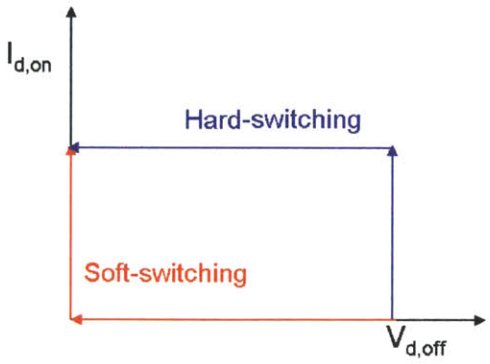

Figure 4-3. Illustration of the current-voltage trace during the turn-on transition of a power transistor in hard-switching and soft-switching circuits. The turn-off transition is time reverse of the trace.

Typical methods for characterizing the trapping effects in AlGaN/GaN HEMTs are gate-lag and drain-lag measurements [Binari2002, Verzellesi2005]. Pulsed I-V measurement

systems capable of pulsing gate and drain independently have become increasingly valuable due to their flexibility in biasing the transistors under arbitrary bias points [McGovern2005]. However, these measurement techniques do not create an environment identical to the one in the circuit where the transistors are actually going to be used. The ability to extract the transistor dynamic R_{on} in real time within a circuit is of a great value for circuit designers as it can give more realistic device parameters for designing the circuit. In section 4.2, an in-circuit dynamic R_{on} characterization method is presented.

Another goal of this chapter is to study the effect of transistor switching characteristics on its dynamic R_{on}. As shown in Figure 4-3, in hard-switching power converters (e.g. buck/boost converters), the transistor has lossy switching transitions, during which both high voltage and high current are applied to the transistor simultaneously, a phenomenon commonly referred to as current-voltage overlapping. As a result, the transistors in these circuits have a large number of hot electrons during the switching transition. On the other hand, in soft-switching circuits (e.g. zero-voltage switching (ZVS) circuit), the current-voltage overlapping is avoided so that no switching loss is present. Therefore, the soft-switching transistor only experiences the off-state voltage stress but not the hot electrons. Since hot electrons have been suspected as one of the sources for electron trapping in AlGaN/GaN HEMTs [Meneghini2011], by comparing the dynamic R_{on} of GaN transistors operating in both switching conditions, we are able to differentiate the effect of channel hot electrons from the effect of high off-state biases on device dynamic R_{on} [Mizutani2003].

In section 4.2, a new dynamic R_{on} measurement technique is presented. In section 4.3 and 4.4, the dynamic R_{on} of commercial GaN power transistors in soft-switching and hard-switching circuits is studied.

4.2 Dynamic R_{on} Measurement Technique

The dynamic R_{on}, which we describe with the symbol $\tilde{R}_{on}$, can be calculated by $\tilde{R}_{on} = \tilde{V}_{dson}/\tilde{I}_{dson}$, where $\tilde{V}_{dson}$ and $\tilde{I}_{dson}$ are the on-state drain-to-source voltage and drain current during dynamic operations. Once $\tilde{V}_{dson}$ and $\tilde{I}_{dson}$ are measured, $\tilde{R}_{on}$ can be calculated. However, it is challenging to determine $\tilde{V}_{dson}$ of the switching transistor in the presence of a large voltage swing. During dynamic operation, the drain voltage can swing between

hundreds of volts in the off-state and several millivolts in the on-state. Direct measurement of $\tilde{V}_{dson}$ using oscilloscope voltage probes either gives poor accuracy or causes saturation of the oscilloscope channel.

To accurately measure $\tilde{V}_{dson}$, a voltage clamping circuit is designed. As shown in Figure 4-4(a), a 200 V Si MOSFET IRF620 was used for the voltage clamping. The gate of the Si MOSFET is biased at a constant voltage V_g above its threshold voltage V_{th}. When the device-under-test (DUT) is in the off-state with high V_{ds}, the source voltage of the IRF620 is clamped at $V_g - V_{th}$ due to the high impedance of the reverse biased diodes, which creates a self-bias to the IRF620. When the DUT is in the on-state with low V_{ds}, the IRF620 transistor is turned on, providing a low impedance path between the drain of the DUT and the source of the IRF620. As a result, $\tilde{V}_{dson}$ of the DUT can be measured with high resolution.

The drain-to-source capacitive coupling of the clamping transistor can result in large displacement current through its C_{ds} during the rising and falling transitions of the drain voltage (V_{ds}) of the DUT. When $dV_{ds}/dt > 0$, the displacement current flows to the source of the clamping transistor, which can cause a large voltage spike. To reduce the voltage spike, a Zener diode is used as shown in Figure 4-4(a), limiting the voltage spike to the Zener voltage. When $dV_{ds}/dt < 0$, the displacement current flows in the opposite direction. Two Schottky diodes are used as shown in Figure 4-4(a) to allow the flow of this current. Another function of the Schottky diodes is to avoid the forward turn-on of the Zener diode, whose reverse recovery can be slow. The 10 Ω resistor is used for damping the ringing effect in the circuit due to wire inductances. In this particular circuit, the voltage clamping range is 200 V and $\tilde{V}_{dson}$ can be measured as fast as 1 μs after the DUT is switched on. Transistors with higher breakdown voltage and lower current rating than the IRF620 can be used to increase the voltage range and the speed of the clamping circuit.

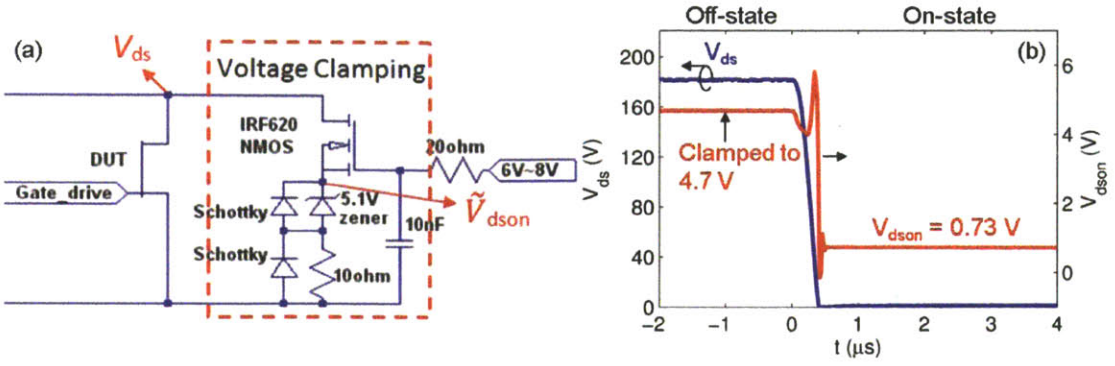

Figure 4-4. (a) Voltage clamping circuit for V_{dson} measurement; (b) measured voltages from the voltage clamping circuit.

Figure 4-4(b) shows the measurement result of the voltage clamping circuit. The off-state drain voltage of 180 V was clamped to 4.7 V. As a result, the on-state voltage of 0.73 V can be measured with high accuracy. The $\tilde{R}_{on}$ measurement error in the setup is estimated to be between 5 mΩ and 10 mΩ.

4.3 Dynamic R_{on} Extraction in Soft-switching and Hard-switching Circuits

Commercial normally-off GaN transistors (EPC1012) were used to study the impact soft-switching and hard-switching on the $\tilde{R}_{on}$ of GaN devices. A Si IRF620 MOSFET with similar current and voltage ratings as the GaN transistors was used as a reference. The most relevant parameters of these devices are compared in Table 4-1. The EPC1012 GaN transistor not only has much lower R_{on} but also smaller capacitance and gate charge than the Si transistor. The $R_{on}\times Q_g$ figure of merit of EPC1012 is only 1.2% of that of IRF620.

Table 4-1. Comparison of datasheet value of IRF620 and EPC1012.

	IRF620	EPC1012
BV (V)	200	200
R_{on} (Ω)	0.8 @ V_{gs} = 10 V I_d = 2.5 A	0.07 (Max 0.1) @ V_{gs} = 5 V I_d = 5A
I_d (A)	5	3
Min V_{th} (V)	2	0.7
Max V_{gs} (V)	± 20	-5 ~ 6
C_{iss} (pF)	260	110
C_{oss} (pF)	100	80
C_{rss} (pF)	30	7.5
Q_g (nC)	14	1.9

4.3.1 Gate Driver Circuit

A gate driver circuit with low output impedance was built with a PMOS Si transistor (Si2319DS) and a NMOS Si transistor (PMV117EN) as shown in Figure 4-5. The gate driver circuit shown in Figure 4-5 can output a maximum voltage of 10 V. Its typical output wave form is shown in Figure 4-6.

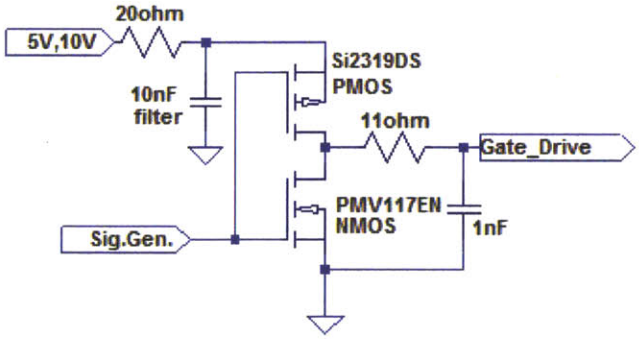

Figure 4-5. Gate drive circuit diagram.

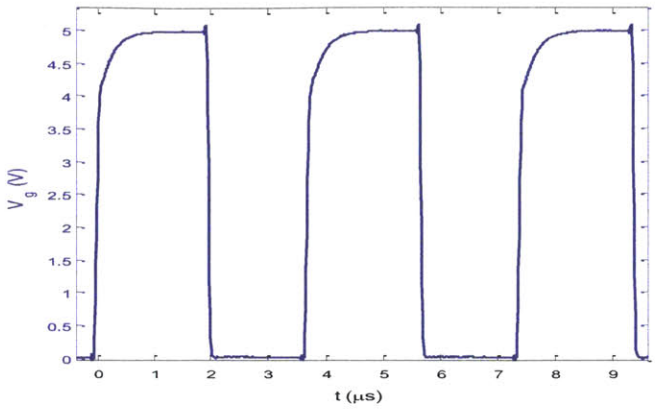

Figure 4-6. Gate drive output waveform at 5 V.

4.3.2 Dynamic R_{on} in Soft-switching Condition

The soft-switching circuit implementing zero-voltage-switching of the DUT is shown in Figure 4-7. The on-state drain current of the DUT is calculated by $\tilde{I}_{dson} = I_1 + I_2 - C d\tilde{V}_{dson}/dt$, where the current I_1 and I_2 were measured using an Agilent N2893A current probe and an Agilent DSO6054A oscilloscope. In the soft-switching measurement, the term $C dV_{ds,on}/dt$ was smaller than 5 mA. Therefore, this term can be ignored and the on-state drain current can be approximated by $\tilde{I}_{dson} \approx I_1 + I_2$.

Before the soft-switching experiment, the DC I_d-V_d characteristics of the fresh GaN transistors and Si MOSFETs were measured to determine their DC R_{dson}, which are 0.05 Ω and 0.64 Ω respectively, well below the typical values indicated in the datasheet.

Figure 4-8 shows the EPC1012 GaN device soft-switching waveforms at a peak V_{ds} voltage of 150 V with switching frequency of 300 kHz. The on-state and off-state durations in each switching cycle are 2 μs and 1.3 μs, respectively. The device is switched on only when its drain voltage drops to zero, realizing a zero-voltage switching.

The dynamic R_{on}, $\tilde{R}_{dson}$, is plot as a function of the off-state peak voltage, V_{ds}, in Figure 4-9, normalized by the DC R_{on}. It is measured 2 μs after the peak V_{ds} voltage is reached. As shown in Figure 4-9, the $\tilde{R}_{on}$ of the GaN transistor increased more than 3 times over its DC R_{on}, due to the off-state stress-induced trapping [Mizutani2003] and possibly transistor

degradation. On the other hand, the ratio between the dynamic R_{on} and DC R_{on} of the Si MOSFET is within 1.1, which is expected for Si MOSFETs.

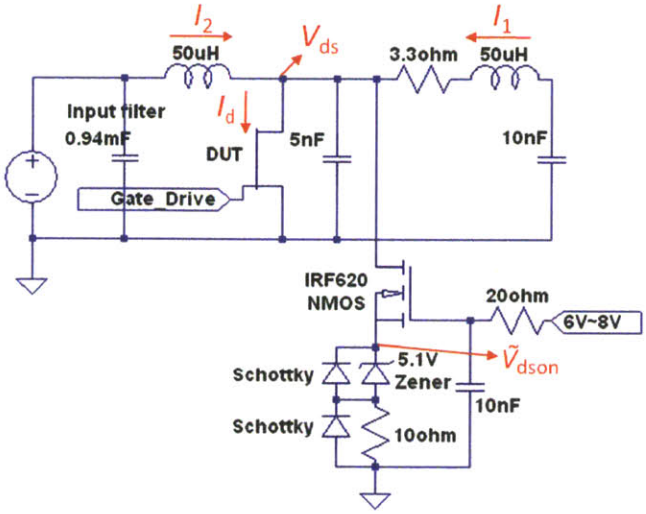

Figure 4-7. Soft switching circuit diagram.

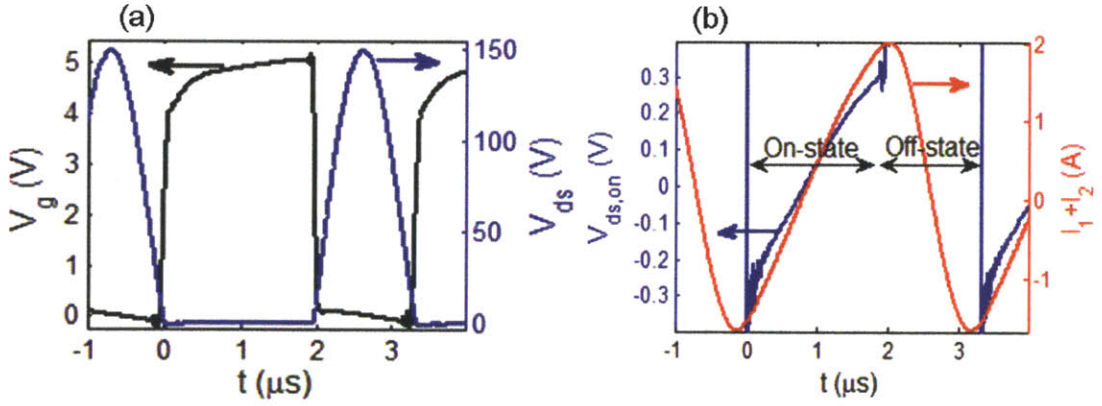

Figure 4-8. Soft-switching waveforms of GaN transistor (a) V_g and V_{ds} (b) V_{dson} and I_1+I_2 waveforms.

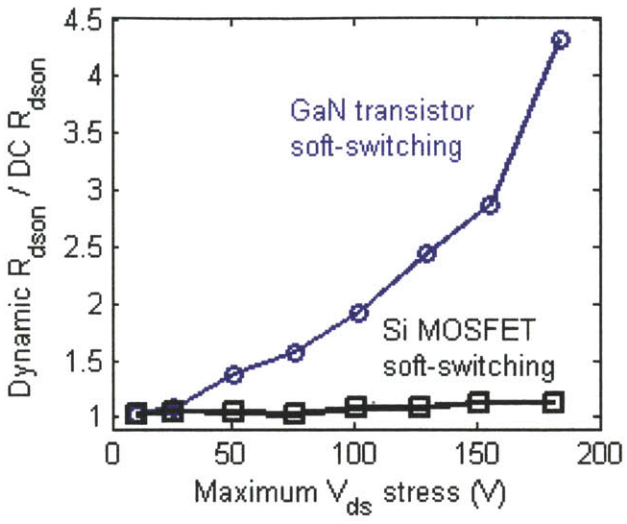

Figure 4-9. Normalized dynamic R_{on} of the GaN transistor and Si MOSFET in soft-switching condition at 2 μs after the peak V_{ds} stress.

4.3.3 Dynamic R_{on} in Hard-switching Condition

In contrast to the soft-switching circuit, a hard-switched power transistor has switching losses due to the overlapping of high V_{ds} with high I_{ds} during the switching transient. Therefore, in addition to the off-state V_{ds} stress, the device also experiences a pulse of high voltage and high current overlap during its switching transient, which could cause additional trapping or degradation due to the hot electrons in the GaN transistor channel.

A hard-switching circuit was built as shown in Figure 4-10 to study the effect of switching loss on the GaN transistor dynamic R_{on}. The load resistor R_{Load} in Figure 4-10 was adjusted to maintain the on-state drain current around 1 A. The 100 nF capacitor with the 400 Ω resistor and Schottky diode form an input filter to prevent the overshooting of the drain voltage. Before the hard switching experiment, the DC R_{on} was measured on fresh GaN transistors. The DUT was turned on for 15 μs in every 1 ms period to reduce self-heating. Figure 4-11 shows the turn-on and turn-off transient waveforms of the GaN transistor with off-state V_{ds} set to 150 V. Due to the overlapping of high I_d with high V_{ds}, the switching loss in Figure 4-11 is 3.6 μJ per switching cycle with peak power of 20 W and 46 W for the turn-on and turn-off transients respectively.

The dynamic R_{on}, $\tilde{R}_{on}$, measured 2 μs and 10 μs after the device was switched on is shown in Figure 4-12. $\tilde{R}_{dson}$ experienced a more than 3-fold increase over its DC R_{on} value at V_{ds} of 180 V. In addition, $\tilde{R}_{dson}$ decreased with time after the device was turned on, indicating a detrapping transient. On the other hand, the dynamic R_{on} of the Si MOSFETs is same as its DC R_{on} value.

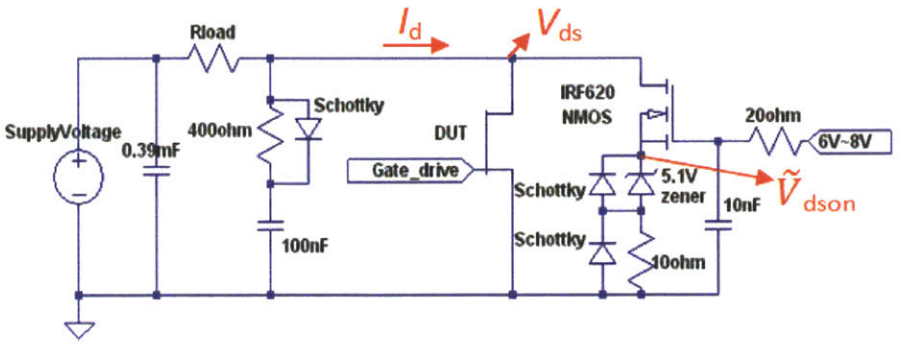

Figure 4-10. Hard-switching circuit diagram.

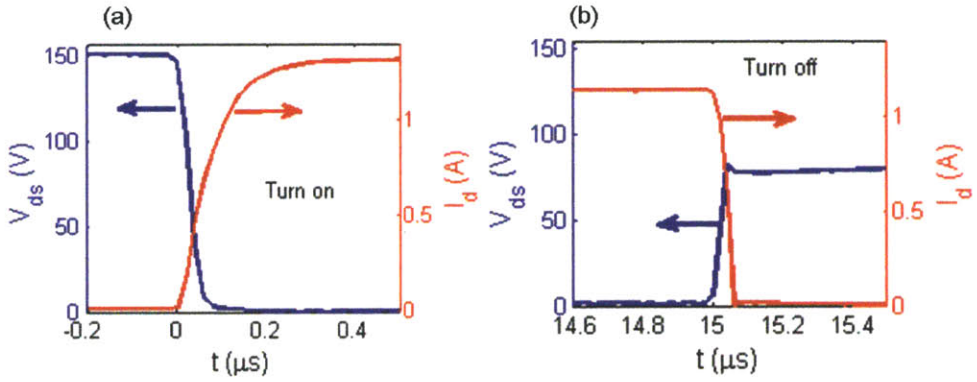

Figure 4-11. GaN transistor hard switching V_{ds}, I_d waveforms in (a) turn-on transient and (b) turn-off transient at 150 V V_{ds} stress. The V_{ds} rises to 150 V in (b) with a RC time constant of 40 μs of the input filter.

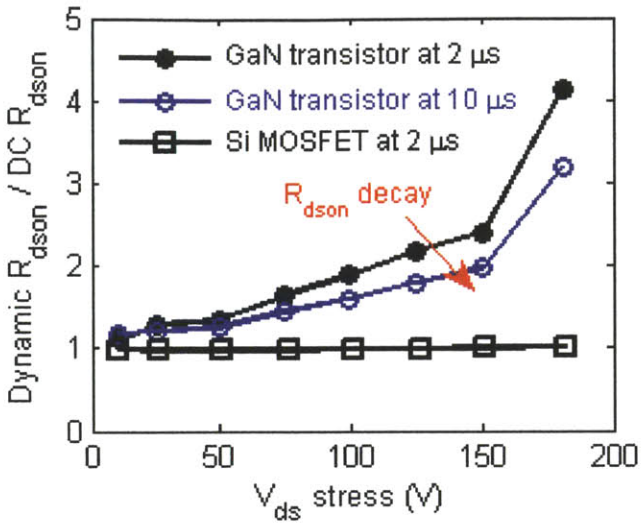

Figure 4-12. Normalized dynamic R_{on} of the hard-switched GaN transistor and Si MOSFET at 2 µs and 10 µs after the devices were switched on.

4.4 Effect of Soft-switching and Hard-switching on Dynamic R_{on}

The increase of the dynamic R_{on} from the initial DC R_{on}, $\Delta R_{on} = \tilde{R}_{on} - R_{on}$, is plotted in Figure 4-13(a) for both hard-switching and soft-switching GaN transistors. The dynamic R_{on} was measured at 2 µs after reaching the peak off-state voltage for the soft-switching transistor and at 2 µs after turn on for the hard-switching transistor. This ensures that the data is taken at the same moment after the maximum drain voltage stress on these transistors.

As shown in Figure 4-13(a), the ΔR_{on} in both devices increases almost linearly with the off-state peak V_{ds} until 150 V and then has a sharp rise at 180 V. The difference in ΔR_{on} between the hard-switching and soft-switching GaN transistors is very small (less than 15 mΩ) for peak V_{ds} below 150 V. At 180V, the difference between the two increases to 43 mΩ, with ΔR_{on} in the hard-switching transistor 24% higher than the soft-switching transistor. As shown in Figure 4-13(b), the I_d-V_{ds} trace during turn-on transient in hard-switching transistor produces 2.8 µJ power loss with peak power of 34 W at about 72 V.

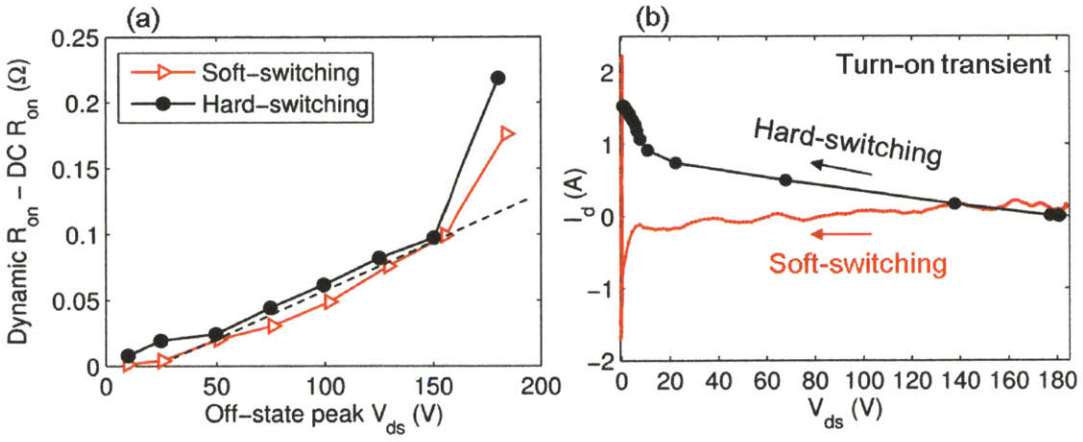

Figure 4-13. (a) ΔR_{on} of GaN transistors measured at 2 μs after the off-state peak V_{ds} in hard- and soft- conditions; (b) turn-on transient V_{ds}-I_d traces from off-state voltage of 180 V.

In order to undertand whether the larger ΔR_{on} of the hard-switching transistor at 180 V is due to the Joule heating effect of the power loss in the turn-on transient, a 10 nF capacitor was attached between the drain and source of another GaN transistor (fresh device) to increase the switching loss in the hard-switching test as shown in Figure 4-14(b). For an off-state voltage of 50 V, the transistor with 10 nF output capacitor had a turn-on switching loss of 12.5 μJ with peak power of 300 W due to the surge of the drain current as shown in Figure 4-14(c). However, even with this large switching loss, the device has the same ΔR_{on} as those of the soft-switching transistor and hard-switching transistor without the 10 nF external capacitor. Therefore, the observed higher ΔR_{on} at off-state peak V_{ds} = 180 V in the hard-switching transistor in Figure 4-13(a) is not related to the Joule heating effect, but to the hot electron effect. However, it cannot be concluded at this point whether these hot electrons were simply trapped in the device or created more defects.

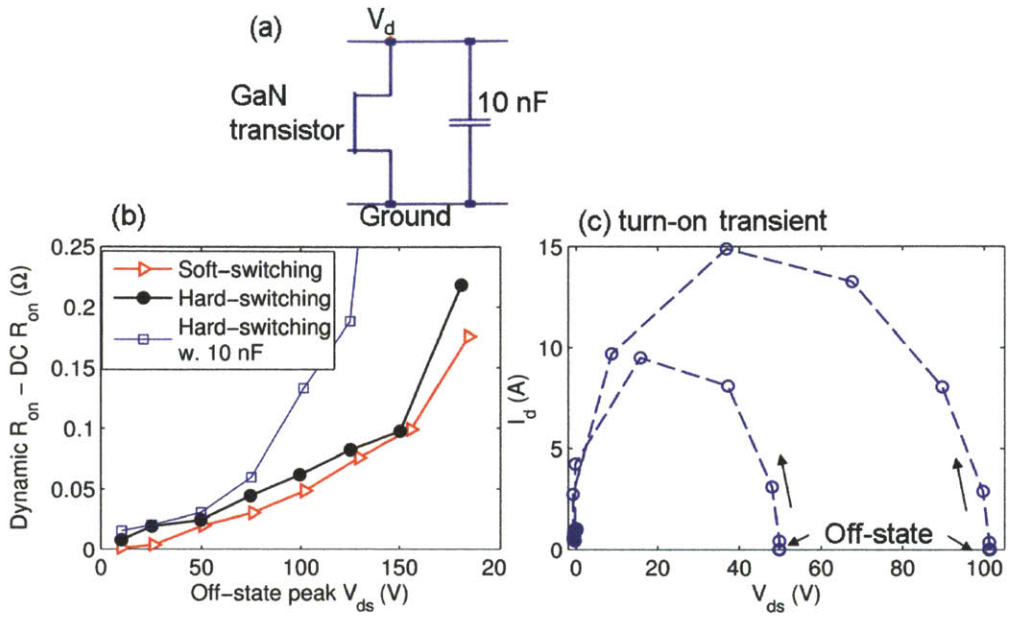

Figure 4-14. (a) circuit diagram of the connection of 10 nF capacitor; (b) increase of dynamic R_{on} measured at 2 μs after the peak V_{ds}; (c) I_d-V_{ds} traces of the hard-switching GaN transistor with 10 nF external capacitor during turn-on transient.

For the hard-switching GaN transistor with 10 nF external capacitor, R_{on} increases very rapidly when off-state V_{ds} voltage is larger than 75 V, as shown in Figure 4-14(b). The mechanism of the dramatic increase of dynamic R_{on} is not clear. It could be that the large instantaneous current (15 A as shown in Figure 4-14(c) for 100 V off-state voltage) carries a much higher density of hot electrons than in the device without 10 nF external capacitor so that the hot electron trapping effect can be more pronounced at even lower voltages (but still needs to be larger than 75 V). Another possibility for the degradation is defect generation by the intense heating effect of the high instantaneous pulse current. Further investigation of the switching loss on the device dynamic R_{on} is needed.

4.5 Conclusion

A new technique to extract the dynamic R_{on} of power transistors under soft- and hard-switching operation has been developed. By using a voltage clamping circuit, the on-state drain voltage and, with it, the dynamic on resistance can be measured accurately.

The effect of the switching loss on dynamic R_{on} of a hard-switching GaN transistor is studied by comparing it to a soft-switching GaN transistor. Both devices show the same amount of increase in dynamic R_{on} until a large enough voltage is reached (in this case 180 V). In addition, the degradation in the dynamic R_{on} is accelerated by increasing the switching losses in the transistor.

The dynamic response of the clamping circuit can be further improved by optimizing the circuit components so that 50 ns or better resolution of dynamic on-resistance can be extracted. With this time resolution, very fast trapping/detrapping process can be studied which can promote the understanding of the dynamic behavior in AlGaN/GaN HEMTs.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

To summarize, this thesis tackles three major challenges in AlGaN/GaN high voltage power switches.

The first challenge is to improve the breakdown voltage of the AlGaN/GaN-based power switches fabricated on Si substrates. A trap-limited space-charge impact-ionization model (TLSCII model) has been developed to explain the vertical breakdown mechanism in these devices. The vertical current is caused by electron injection from device contacts or the Si substrate. The injected electrons also create an electric field in the epi-layer, which induces impact ionization when the electric field is above 2.5 MV/cm. A high density of deep traps in the epi-layer plays an important role in suppressing the vertical leakage current by reducing free electrons in the conduction band until impact ionization occurs. It is also observed that the standard alloyed ohmic contact in the AlGaN/GaN transistors has an asymmetric leakage characteristic—leakage occurs at much lower voltage at positive bias than at negative bias. It is suspected this phenomenon is due to hole generation at the defects created by the alloyed ohmic contact. With the understanding of the breakdown mechanism, two device technologies, the Schottky-drain technology and the substrate-transfer technology, are developed to increases the breakdown voltage of GaN-on-Si devices.

The second challenge is to fabricate high-performance enhancement-mode (E-mode) normally-off GaN power switches. Three novel transistor structures were demonstrated. The first one is a dual-gate normally-off AlGaN/GaN MISFET, which minimizes the impact of the low channel mobility in the recessed-gate region without compromising the overall device breakdown voltage and threshold voltage. The second one is a tri-gate normally-off AlGaN/GaN MISFET, which has more than two orders of magnitude reduction in the device off-state leakage, demonstrating a truly normally-off operation. The third one is an etch-stop barrier structure, which significantly improves the recess-etching uniformity, dielectric/semiconductor interface quality and effective channel mobility.

The third challenge is to improve the stability and reliability of AlGaN/GaN HEMTs in switching conditions. A new technique has been developed to accurately extract the in-circuit dynamic R_{on} of power transistors under soft- and hard-switching operations, which allows future understanding and minimization of the dynamic on resistance in power switches.

This thesis increases the understanding and enriches the design toolbox of AlGaN/GaN-based power switches. These advances will hopefully improve the performance of the GaN-based power switches to the next level.

5.2 Future work

Built upon the work of this thesis, some future research directions are suggested in this section.

5.2.1 Improving device breakdown voltage

With the understanding of the breakdown mechanism in GaN devices on Si substrate, new device structures can be designed quantitatively using the TLSC model. For example, the concentration profile of buffer traps can be engineered to reduce trapping effect on the device on-resistance. Another proposed technology is to restrict electron injection from Si substrate.

5.2.2 Higher threshold voltage normally-off device

One immediate improvement in AlGaN/GaN normally-off HEMT can be achieved by combining the tri-gate structure with the etch-stop barrier design. However, the large positive dielectric/semiconductor interface charge poses another challenge to the scaling of device threshold voltage. As shown in the simulation of etch-stop barrier structure, the positive dielectric interface charge causes negative threshold voltage shifts with increasing dielectric thickness. The origin of the positive charge needs to be understood. The "surface-donor" model proposed by Ibbeson et al. does not indicate where the surface donor comes from and how it impacts device CV characteristics. The accurate device CV model developed in Chapter 3 can be used to study these surface donors.

5.2.3 Understanding Trapping and Degradation Mechanism in AlGaN/GaN HEMTs

Further experiments can be designed to understand the hot electron effect using the dynamic R_{on} extraction method in hard- and soft-switching circuits shown in Chapter 4. The hard-switching losses can be controlled by tailoring the inductive load in the circuit to have desirable voltage-current overlapping in the switching transient.

Appendix A Elasticity and Piezoelectricity in III-Nitride Semiconductors

- **Elastic Property**

From the linear elasticity theory, the relation between the stress σ_j and strain ϵ_j is

$$\sigma_i = C_{ij}\epsilon_j \text{ with } i,j = 1, 2, 3 \ldots 6 \tag{A-1}$$

where C_{ij} is the material elastic constant and by Voigt notation $(\sigma_1, \sigma_2, \sigma_3, \sigma_4, \sigma_5, \sigma_6) = (\sigma_{xx}, \sigma_{yy}, \sigma_{zz}, \sigma_{yz}, \sigma_{xz}, \sigma_{xy})$. The Einstein summation convention is used such that $C_{ij}\epsilon_j$ means $\sum_{j=1}^{6} C_{ij}\epsilon_j$.

The nitride semiconductor of hexagonal crystal structure has elasticity matrix as the following:

$$C = \begin{bmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{13} & 0 & 0 & 0 \\ c_{13} & c_{13} & c_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2}(c_{11} - c_{12}) \end{bmatrix}$$

Rewrite equation (A-1) in matrix form:

$$\begin{pmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{pmatrix} = C \begin{pmatrix} \epsilon_1 \\ \epsilon_2 \\ \epsilon_3 \\ \epsilon_4 \\ \epsilon_5 \\ \epsilon_6 \end{pmatrix}$$

The elastic property of Nitride semiconductors used in this thesis are tabulated in Table A-1.

Table A-1 Elastic constants (GPa) [Wright1997]

	C_{11}	C_{12}	C_{13}	C_{33}	C_{44}
AlN	396	137	108	373	116
GaN	367	135	103	405	95
InN	223	115	92	224	48

For an epitaxial nitride film grown on a foreign substrate, if we ignore the hydrostatic stresses generated from point defects, the dominant stresses are biaxial basal stresses:

$$\sigma_3 = 0$$

$$\sigma_1 = \sigma_2 = (C_{11} + C_{12} - \frac{2C_{13}^2}{C_{33}})\epsilon_1$$

- **Piezoelectricity**

The Wurtzite III-Nitride semiconductors have strong polarization along the c-axis and their piezoelectricity can be written in the strain-charge formula as [Cady1964]:

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & 0 & 0 & 0 \\ s_{21} & s_{22} & s_{23} & 0 & 0 & 0 \\ s_{31} & s_{32} & s_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & 2(s_{11} - s_{12}) \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} 0 & 0 & d_{31} \\ 0 & 0 & d_{32} \\ 0 & 0 & d_{33} \\ 0 & d_{24} & 0 \\ d_{15} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$$

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} \epsilon_{11} & 0 & 0 \\ 0 & \epsilon_{22} & 0 \\ 0 & 0 & \epsilon_{33} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$$

To avoid the confusion between the dielectric constant and strains, new symbols are used where $\{T_i\}$ is stress, $\{S_i\}$ is strain, $\{D_i\}$ is electric displacement, $\{E_i\}$ is the electric field strength, $[s_{ij}]$ is the compliance matrix at constant electric field, $[d_{ij}]$ is the piezoelectric strain

coefficients (direct piezoelectric effect) and $[\epsilon_{ij}]$ is the dielectric constant matrix. As before, Voigt notation is used.

For III-Nitride hexagonal crystal system of C_{6V} point group, we also have $s_{12} = s_{21}$, $s_{13} = s_{31}$, $s_{22} = s_{11}$, $s_{23} = s_{13}$, $s_{55} = s_{44}$, $s_{66} = 2(s_{11}-s_{12})$. $d_{31} = d_{32}$, $d_{24} = d_{15}$.

The compliance matrix is the inverse of the elastic constant matrix,

$$[s_{ij}] = [c_{ij}]^{-1}$$

The piezoelectric strain coefficients d_{jk} and the piezoelectric coefficients e_{ij} have the following the relationship

$$[e_{ij}] = \begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{24} & 0 & 0 \\ e_{31} & e_{32} & e_{33} & 0 & 0 & 0 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{13} & 0 & 0 & 0 \\ c_{13} & c_{13} & c_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2}(c_{11} - c_{12}) \end{bmatrix}$$

where $e_{31} = e_{32}$, $e_{24} = e_{15}$ for Hexagonal III-Nitride semiconductors.

The piezoelectric coefficients of III-Nitrides are listed in Table A-2.

Table A-2 Spontanious polarization (C/m^2) and piezoelectric coeffeicients (C/m^2)

	P_{sp}	e_{33}	e_{13}	e_{15}
AlN	-0.090	1.5	-0.53[a]	-0.42[c]
			-0.62[b]	
GaN	-0.034	0.67	-0.34[a]	-0.29[c]
			-0.37[b]	
InN	-0.042	0.81	-0.41[a]	-
			-0.45[b]	

[a]Ref. [Bernadini2001]: improper piezoelectric coefficients (without electric field coupling)

[b]Ref. [Bernardini2001]: proper piezoelectric coefficients (used in electromechanical simulation)

[c]Ref. [Guy2000] and calculated from $e_{15} = d_{15}c_{44}$

Appendix B Parameters of III-Nitride Semiconductors for CV Simulations

The polarization charges of III-Nitride semiconductors are composed of spontaneous and piezoelectric polarizations:

$$\sigma_{\text{polar}} = \sigma_{\text{SP}} + \sigma_{\text{PZ}}$$

• Spontaneous Polarization

The nonlinear spontaneous polarization (P^{SP} in C/m^2) of $Al_xGa_{1-x}N$ ($0 \le x \le 1$) used in the simulation is based on reference [Fiorentini2002]:

$$P^{\text{SP}}_{Al_xGa_{1-x}N} = -0.09x - 0.034(1-x) + 0.019x(1-x)$$

• Piezoelectric Polarization

The piezoelectric polarization (P^{PZ} in C/m^2) of $Al_xGa_{1-x}N$ ($0 \le x \le 1$) also shows nonlinearity [Fiorentini2002]. It is calculated according to Vegard's law using the equations from reference [Fiorentini2002]:

$$P^{\text{PZ}}_{Al_xGa_{1-x}N} = xP^{\text{PZ}}_{\text{AlN}} + (1-x)P^{\text{PZ}}_{\text{GaN}}$$

where $P^{\text{PZ}}_{\text{AlN}}$ and $P^{\text{PZ}}_{\text{GaN}}$ are the piezoelectric polarizations of the relevant binary compounds in $Al_xGa_{1-x}N$.

$$P^{\text{PZ}}_{\text{AlN}} = -1.808\varepsilon + 5.624\varepsilon^2 \text{ for } \varepsilon < 0,$$

$$P^{\text{PZ}}_{\text{AlN}} = -1.808\varepsilon - 7.888\varepsilon^2 \text{ for } \varepsilon > 0,$$

$$P^{\text{PZ}}_{\text{GaN}} = -0.918\varepsilon + 9.541\varepsilon^2$$

The bi-axial basal strain ε of $Al_xGa_{1-x}N$ pseudomorphicly grown on GaN buffer is

$$\varepsilon = (a_{\text{GaN}} - a_{\text{AlGaN}})/a_{Al_xGa_{1-x}N}$$

where a_{GaN} is the lattice constant of GaN and $a_{Al_xGa_{1-x}N}$ the lattice constant of unstrained $Al_xGa_{1-x}N$ which follows Vegard's law:

$$a_{Al_xGa_{1-x}N} = xa_{AlN} + (1-x)a_{GaN}$$

with $a_{AlN} = 3.112\text{Å}$ and $a_{GaN} = 3.189\text{Å}$ [Bernardini2001].

It is worth noting that the full piezoelectric equation has coupling between the electric field and the strain as seen in Appendix A. The piezoelectric equations listed here are in the decoupled forms which take into account the electric field effect with the piezoelectric constants, so called "improper" piezoelectric constants [Bernardini2001].

The nonlinear piezoelectricity of the $Al_xGa_{1-x}N$ is believed to be more accurate than the linear piezoelectricity calculated based on reference [Bernardini2001]. However, they in general only differ by less than 10% for the commonly used Al percentage up to 30% as shown in.

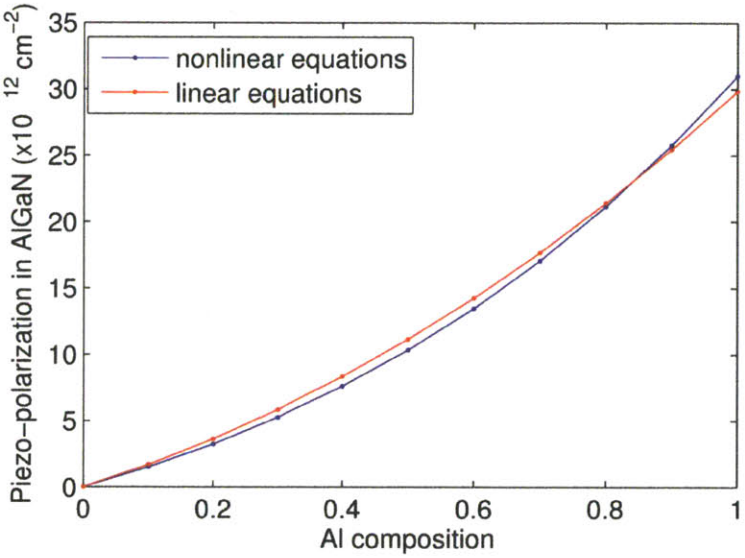

Figure B-1. Comparison between nonlinear and linear polarization calculations.

- **Bandgap, Band Alignment, Dielectric Constants and Effective Masses**

The band-gap of $Al_xGa_{1-x}N$ is calculated using a bowing factor of 0.71 eV [Dridi2003] and band-gap parameters of GaN and AlN from [Ambacher2002]

$$E^{g}_{AlGaN}(x) = 6.13x + 3.42(1-x) - 0.71x(1-x)$$

The band alignment between $Al_xGa_{1-x}N$ and GaN is calculated using a conduction band offset factor of 0.75 [Martin1996]

$$\Delta E^{C}_{AlGaN}(x) = 0.75(E^{g}_{AlGaN}(x) - E^{g}_{GaN})$$

Dielectric constant $\epsilon^{33}_{AlGaN}$of $Al_xGa_{1-x}N$ is calculated from linear interpolation of the dielectric constants of AlN (10.31 [Bernardini1997]) and GaN (10.4 [Barker1973]):

$$\epsilon^{33}_{AlGaN}(x) = 10.31x + 10.4(1-x)$$

Dielectric constant $\epsilon^{11}_{AlGaN}$of $Al_xGa_{1-x}N$ is based on the reference [Ambacher1998]:

$$\epsilon^{11}_{AlGaN}(x) = 9x + 9.5(1-x)$$

The conduction band (Γ valley) effective mass of $Al_xGa_{1-x}N$ is calculated from linear interpolation using the data from reference [Vurgaftman2003]:

$$m^{//c}_{AlGaN}(x) = 0.32x + 0.2(1-x)$$

$$m^{\perp c}_{AlGaN}(x) = 0.3x + 0.2(1-x)$$

Appendix C Nextnano3 CV Simulation Codes for Tri-Gate and GaN-Etch-Stop Structure Devices

- **70-nm-Sidewall Tri-gate 2D CV Simulation Codes**

```
$numeric-control
 simulation-dimension  = 2
 zero-potential        = no
 varshni-parameters-on = no  !Band gaps dependence of temperature.
 lattice-constants-temp-coeff-on = no
 piezo-constants-zero  = no
 pyro-constants-zero   = no
 newton-method     = Newton-3
 nonlinear-poisson-iterations   =  100
 nonlinear-poisson-residual  =  2.0d-9
$end_numeric-control

$simulation-dimension
 dimension   = 2        ! 2D simulation
 orientation = 1 0 1    ! x-z space
$end_simulation-dimension

$global-parameters
 lattice-temperature = 300d0    ! 300 Kelvin
$end_global-parameters

$simulation-flow-control
 flow-scheme         = 2
 strain-calculation  = homogeneous-strain
$end_simulation-flow-control

$domain-coordinates
 domain-type            = 1 0 1  ! again: x-z axis
```

```
 x-coordinates           = -185d0 185d0
 z-coordinates           = -90d0 100d0
 pseudomorphic-on        = GaN
 growth-coordinate-axis = 0 0 1    ! specify in x-y-z cordinate
 hkil-x-direction  =  1   0 -1   0
 hkil-z-direction  =  0   0   0   1
 crystal-type          = wurtzite
$end_domain-coordinates
!****** REGIONS AND CLUSTERS *************!
$regions
 region-number = 1   base-geometry = rectangle   region-priority = 1
! gate metal
 x-coordinates = -185d0 185d0
 z-coordinates = 0d0   100d0
 region-number = 2  base-geometry = rectangle  region-priority = 2
! oxide
 x-coordinates = -93d0 93d0
 z-coordinates = 0d0 88d0
 region-number = 3   base-geometry = rectangle   region-priority = 3
! oxide
 x-coordinates = -185d0 185d0
 z-coordinates = 0d0 18d0
 region-number = 4   base-geometry = rectangle   region-priority = 4
! 2nm GaN cap
 x-coordinates = -75d0 75d0
 z-coordinates = 68d0 70d0
 region-number = 5   base-geometry = rectangle   region-priority = 5
! 18nm AlGaN
 x-coordinates = -75d0 75d0
 z-coordinates = 50d0 68d0
 region-number = 6   base-geometry = rectangle   region-priority = 6
! 50nm tri-gate GaN
 x-coordinates = -75d0 75d0
 z-coordinates = 0d0 50d0
```

```
 region-number = 7   base-geometry = rectangle   region-priority = 7
! GaN substrate
 x-coordinates = -185d0 185d0
 z-coordinates = -80d0 0d0
 region-number = 8   base-geometry = rectangle   region-priority = 8
! substrate metal
 x-coordinates = -185d0 185d0
 z-coordinates = -90d0 -80d0
$end_regions

$grid-specification
 grid-type       = 1 0 1   ! x-z
 x-grid-lines    = -185d0  -93d0  -75d0  -74.9d0   -74.8d0   -40d0
0d0    40d0    74.8d0   74.9d0   75d0   93d0    185d0
 x-nodes         =       29     9       2        2        19       39
39       19       2        2       9      29
 x-grid-factors =      1d0     1d0    1d0      1d0     0.98d0
0.99d0   1.01d0  1.02d0    1d0    1d0     1d0     1d0
 z-grid-lines    = -90d0 -80d0  -79d0  -30d0   -5d0   -0.2d0  -0.1d0
0d0  18d0   30d0   50d0   50.1d0   50.2d0   55d0   67.8d0   67.9d0
68d0   69.8d0   69.9d0   70d0   88d0   100d0
 z-nodes         =       2      3    29      19      9      2       2
17     9     29      2       2          14     19       2       2
3        2        2      8       2
 z-grid-factors =       1d0    1d0  1.02d0  1d0    1d0    1d0
1d0    1d0    1d0  0.99d0   1d0     1d0      1.02d0  1d0      1d0
1d0   1d0     1d0      1d0   1d0      1d0
$end_grid-specification

$region-cluster
 cluster-number = 1   region-numbers = 1         ! gate
 cluster-number = 2   region-numbers = 2 3       ! oxdie
 cluster-number = 3   region-numbers = 4         ! GaN cap
 cluster-number = 4   region-numbers = 5         ! AlGaN
 cluster-number = 5   region-numbers = 6         ! tri-gate GaN
 cluster-number = 6   region-numbers = 7         ! buffer GaN
 cluster-number = 7   region-numbers = 8 9
! back ohmic contact, 9 is the default region
```

```
$end_region-cluster
!****** END REGIONS AND CLUSTERS
!****** MATERIALS AND ALLOY PROFILES
$material
 material-number = 1           ! gate
 material-name   = Metal-wz
 cluster-numbers = 1
 material-number = 2
 material-name   = Al2O3   ! change it to SiO2 parameters
 cluster-numbers = 2
 material-number = 3
 material-name   = GaN        ! default is wz
 cluster-numbers = 3 5 6
 material-number = 4
 material-name   = Al(x)Ga(1-x)N    ! default is wz
 alloy-function  = constant
 cluster-numbers = 4
 material-number = 5
 material-name   = Metal-wz         ! back ohmic
 cluster-numbers = 7
 crystal-type    = wurtzite
$end_material

$alloy-function
 material-number        = 4
 function-name          = constant
 xalloy                 = 0.26d0    ! Al0.26Ga0.74N
$end_alloy-function

!Shift all the valance band energy by -5eV to avoid hole
accumulation
! GaN parameters:
! E_c = E_v    + E_gap(hh) + Delta1 + Delta2  =
!     = -0.726 + 3.39     + 0.010  + 0.00567 = 2.67967 eV (300K)
$binary-wz-default
```

```
 binary-type       = GaN-wz-default   ! read in the default data
 apply-to-material-numbers   = 3 4
 piezo-electric-constants   = 0.67d0   -0.34d0   -0.29d0
![C/m^2]  e33, e31 , e15
 pyro-polarization         =  0d0       0d0      -0.034d0
![C/m^2] O. Ambacher and Vurgaftman2
 static-dielectric-constants          = 9.5d0  9.5d0  10.4d0
 elastic-constants      =  367d0    135d0     103d0 ! White
                           405d0    95d0
! C11,C12,C13,C33,C44
 conduction-band-energies  = 2.694d0 6.190d0 6.490d0
! Eg=3.42 Ambacher
 valence-band-energies       = -5.726d0
 band-shift               = 0d0
 absolute-deformation-potentials-cbs = 0d0  0d0  0d0
 uniax-vb-deformation-potentials     = 0d0   0d0   0d0
                                       0d0  0d0   0d0
$end_binary-wz-default

! AlN parameters:
$binary-wz-default
 binary-type    = AlN-wz-default
 apply-to-material-numbers   = 4
 piezo-electric-constants     = 1.5d0   -0.53d0   -0.42d0
 pyro-polarization                    =  0d0       0d0      -0.090d0
 static-dielectric-constants          = 9d0   9d0   10.31d0
 elastic-constants                    =  396.0d0   137.0d0   108.0d0
                                         373.0d0   116.0d0
 conduction-band-energies    = 4.604d0 5.710d0  5.41d0
! 300K for Eg=6.13eV by Ambacher
 valence-band-energies   = -6.526d0
 band-shift              = 0.12d0
! To have the 0.75 factor bandalign
 absolute-deformation-potentials-cbs = 0d0  0d0  0d0
 uniax-vb-deformation-potentials     = 0d0   0d0   0d0
```

```
                                        0d0   0d0    0d0
$end_binary-wz-default

$ternary-wz-default
 ternary-type = Al(x)Ga(1-x)N-wz-default
 apply-to-material-numbers    = 4
 bow-pyro-polarization      = 0d0       0d0      -0.019d0   ! [C/m^2]
 bow-conduction-band-energies  = 0.71d0    0.80d0    0.61d0
 band-shift   = 0.035d0 ! To have the 0.75 factor bandalign

$end_ternary-wz-default

! SiO2: replacing Al2O3 values
! SiO2 Eg=9eV. Conduction band-offset on GaN = 2.56 eV
! Ev = -0.726(GaN Ev)+3.42(GaN Eg)+2.56-9(SiO2 Eg) = -3.746 eV (300K)
! E_c = E_v    + E_gap          = 5.254 eV
$binary-wz-default
 binary-type                  = Al2O3-wz-default
 apply-to-material-numbers    = 2
 piezo-electric-constants      = 0d0    0d0    0d0
 pyro-polarization        =   0d0        0d0        0d0
 static-dielectric-constants = 4.5d0   4.5d0   4.5d0
! for ALD SiO2 dielectric constant
 conduction-bands           = 3
 conduction-band-masses     = 0.156d0   0.156d0   0.156d0 !GAMMA
                                        1.420d0   0.130d0   0.130d0 !L
                                        0.5d0     0.5d0     0.5d0 !X
 conduction-band-degeneracies         = 2         8         6
 conduction-band-nonparabolicities    = 0d0       0d0       0d0
 conduction-band-energies     = 5.254d0    5.84d0   7.59d0
! only simulates gama band, so put X band energy to Gama
 valence-bands          = 3
 valence-band-masses    = 0.537d0   0.537d0   0.537d0
                                        0.153d0   0.153d0   0.153d0
                                        0.234d0   0.234d0   0.234d0
```

```
 valence-band-degeneracies            = 2        2        2
 valence-band-nonparabolicities       = 0d0      0d0      0d0
 valence-band-energies                = -8.746d0
 band-shift                      = 0d0
 absolute-deformation-potentials-cbs = 0d0      0d0      0d0
uniax-vb-deformation-potentials     = 0d0   0d0   0d0
                                      0d0   0d0   0d0
 uniax-cb-deformation-potentials      = 0d0      0d0      0d0
 absolute-deformation-potential-vb    = 0d0
 varshni-parameters                   = 0.00d0   0.00d0   0.00d0
                                        0.00d0   0.00d0   0.00d0
! optical-dielectric-constant          = 3.5d0
 lattice-constants                    = 0.54304d0 0.54304d0 0.54304d0
 lattice-constants-temp-coeff         = 0d0      0d0      0d0
 elastic-constants                    =  87d0     7d0      7d0
                                         87d0     58d0
$end_binary-wz-default
!****** END MATERIALS AND ALLOY PROFILES
!****** DOPING AND IMPURITIES
$doping-function
 doping-function-number      = 1   ! GaN buffer background doping
 impurity-number             = 1
 doping-concentration        = 0.001d0    ![*10^18cm^-3]
 only-region                 = -75d0  75d0  0d0  50d0
 doping-function-number      = 2   ! GaN buffer background doping
 impurity-number             = 1
 doping-concentration        = 0.001d0    ! [*10^18cm^-3]
 only-region                 = -185d0  185d0  -80d0  0d0
 doping-function-number      = 3    ! GaN buffer pinning
 impurity-number             = 2
 doping-concentration        = 200d0      ! [*10^18cm^-3]
 only-region                 = -185d0  185d0  -80d0  -79d0
!--------GaN cap surface positive charge
 doping-function-number      = 4
 impurity-number             = 3
```

```
 doping-concentration       = 1350d0
 only-region                = -75d0  75d0  69.8d0  69.9d0
!--------mesa surface positive charge
 doping-function-number     = 5
! SiO2/GaN-mesa surface positive charge
 impurity-number            = 4
 doping-concentration       = 1080d0
 only-region                = -185d0  -75d0  -0.2d0  -0.1d0
 doping-function-number     = 6
 impurity-number            = 4
 doping-concentration       = 1080d0
 only-region                = 75d0  185d0  -0.2d0  -0.1d0
!--------mesa etch surface traps -----
 doping-function-number     = 7
 impurity-number            = 5
 doping-concentration       = 5d0
 only-region                = -185d0  -75d0  -0.2d0  -0.1d0
 doping-function-number     = 8
 impurity-number            = 5
 doping-concentration       = 5d0
 only-region                = 75d0  185d0  -0.2d0  -0.1d0
 doping-function-number     = 9
 impurity-number            = 6
 doping-concentration       = 13d0
 only-region                = -185d0  -75d0  -0.2d0  -0.1d0
 doping-function-number     = 10
 impurity-number            = 6
 doping-concentration       = 13d0
 only-region                = 75d0  185d0  -0.2d0  -0.1d0
 doping-function-number     = 11
 impurity-number            = 7
 doping-concentration       = 7d0
 only-region                = -185d0  -75d0  -0.2d0  -0.1d0
 doping-function-number     = 12
 impurity-number            = 7
```

```
 doping-concentration       = 7d0
 only-region                = 75d0  185d0  -0.2d0  -0.1d0
!--------------change piezocharges-------------------------
 doping-function-number     = 13
 impurity-number            = 8
 doping-concentration       = 210d0
 only-region                = -75d0  75d0  69.8d0  69.9d0
 doping-function-number     = 14
 impurity-number            = 8
 doping-concentration       = 14d0
 only-region                = -75d0  75d0  67.8d0  67.9d0
 doping-function-number     = 15
 impurity-number            = 9
 doping-concentration       = 288.08d0
 only-region                = -75d0  75d0  50.1d0  50.2d0
!--------------side wall traps-----------------------------
 doping-function-number     = 16
 impurity-number            = 10
 doping-concentration       = 2d0
 only-region                = -74.9d0  -74.8d0  0d0  50d0
 doping-function-number     = 17
 impurity-number            = 10
 doping-concentration       = 2d0
 only-region                = 74.8d0  74.9d0  0d0  50d0
 doping-function-number     = 18
 impurity-number            = 11
 doping-concentration       = 1.4d0
 only-region                = -74.9d0  -74.8d0  0d0  50d0
 doping-function-number     = 19
 impurity-number            = 11
 doping-concentration       = 1.4d0
 only-region                = 74.8d0  74.9d0  0d0  50d0
 doping-function-number     = 20
 impurity-number            = 12
 doping-concentration       = 1.4d0
```

```
 only-region                = -74.9d0  -74.8d0  0d0  50d0
 doping-function-number     = 21
 impurity-number            = 12
 doping-concentration       = 1.4d0
 only-region                = 74.8d0  74.9d0  0d0  50d0
 doping-function-number     = 22
 impurity-number            = 13
 doping-concentration       = 3.3d0
 only-region                = -74.9d0  -74.8d0  0d0  50d0
 doping-function-number     = 23
 impurity-number            = 13
 doping-concentration       = 3.3d0
 only-region                = 74.8d0  74.9d0  0d0  50d0
 doping-function-number     = 24
 impurity-number            = 14
 doping-concentration       = 2d0
 only-region                = -74.9d0  -74.8d0  0d0  50d0
 doping-function-number     = 25
 impurity-number            = 14
 doping-concentration       = 2d0
 only-region                = 74.8d0  74.9d0  0d0  50d0
!--------sidewall deep donor-------------------------
 doping-function-number     = 26
 impurity-number            = 15
 doping-concentration       = 7d0
 only-region                = -74.9d0  -74.8d0  0d0  50d0
 doping-function-number     = 27
 impurity-number            = 15
 doping-concentration       = 7d0
 only-region                = 74.8d0  74.9d0  0d0  50d0
$end_doping-function

$impurity-parameters

 impurity-number            = 1
```

```
 impurity-type                = n-type
 number-of-energy-levels      = 1
 energy-levels-relative       = -100.d0
 degeneracy-of-energy-levels  = 2
 impurity-number              = 2
 impurity-type                = p-type
 number-of-energy-levels      = 1
 degeneracy-of-energy-levels  = 4
 impurity-number              = 3          ! GaN-cap fixed charge
 impurity-type                = n-type
 number-of-energy-levels      = 1
 energy-levels-relative       = -100.d0
 degeneracy-of-energy-levels  = 2
 impurity-number              = 4
 impurity-type                = n-type
 number-of-energy-levels      = 1
 energy-levels-relative       = -100d0
degeneracy-of-energy-levels  = 2
!------------ mesa etch surface traps ---------------
 impurity-number              = 5
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 8.27d0
 degeneracy-of-energy-levels  = 4
 impurity-number              = 6
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 8.32d0
 degeneracy-of-energy-levels  = 4
 impurity-number              = 7
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 8.37d0
 degeneracy-of-energy-levels  = 4
```

```
!----------change of piezo charges------------------
 impurity-number              = 8
 impurity-type                = n-type
 number-of-energy-levels      = 1
 energy-levels-relative       = -100d0
 degeneracy-of-energy-levels  = 2
 impurity-number              = 9
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = -100d0
 degeneracy-of-energy-levels  = 4
!----------sidewall traps----------------------
 impurity-number              = 10
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 7.22d0
 degeneracy-of-energy-levels  = 4
 impurity-number              = 11
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 7.37d0
 degeneracy-of-energy-levels  = 4
 impurity-number              = 12
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 7.52d0   ! 3.42-0.9eV
 degeneracy-of-energy-levels  = 4
 impurity-number              = 13
 impurity-type                = p-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 7.62d0
 degeneracy-of-energy-levels  = 4
 impurity-number              = 14
impurity-type                = p-type
 number-of-energy-levels      = 1
```

```
 energy-levels-relative       = 7.72d0
 degeneracy-of-energy-levels  = 4
!---------------sidewall deep donor--------------------
 impurity-number              = 15
 impurity-type                = n-type
 number-of-energy-levels      = 1
 energy-levels-relative       = 2d0
 degeneracy-of-energy-levels  = 2

$end_impurity-parameters
!****** QUANTUM ******************!
$quantum-regions
 region-number          = 1
 base-geometry          = rectangle
 region-priority        = 1
 x-coordinates          = -75d0 75d0
 z-coordinates          = 0d0 73d0
$end_quantum-regions
$quantum-cluster
 cluster-number         = 1
 region-numbers         = 1
 deactivate-cluster     = yes
$end_quantum-cluster

$quantum-model-electrons
 model-number                          =  1
 model-name                            =  effective-mass
 cluster-numbers                       =  1
 conduction-band-numbers               =  1
 number-of-eigenvalues-per-band        =  8
 separation-model                      =  eigenvalue
 maximum-energy-for-eigenstates        =  1d0
 quantization-along-axes               =  1 0 1
 boundary-condition-001                =  Neumann
$end_quantum-model-electrons
```

```
$poisson-boundary-conditions
 poisson-cluster-number      = 1
 region-cluster-number       = 1                  ! gate
 boundary-condition-type     = Schottky
 schottky-barrier            = 3.7d0
! [Volt] SiO2 electron affinity = 0.9eV. Ni work function=5.2eV
 applied-voltage             = -4d0
 contact-control             = voltage
 poisson-cluster-number      = 2
 region-cluster-number       = 7                 ! drain
 boundary-condition-type     = ohmic
 applied-voltage             = 0d0
 contact-control             = voltage
$end_poisson-boundary-conditions
$voltage-sweep
 sweep-number              = 1
 sweep-active              = yes
 poisson-cluster-number    = 1
 step-size                 = 0.1d0
 number-of-steps           = 52
 data-out-every-nth-step   = 1
$end_voltage-sweep
!****** OUTPUT ******************!
$output-bandstructure
 destination-directory                  = band_struc1/
 conduction-band-numbers                = 1      ! Gama band
 valence-band-numbers                   = 1 2 3
! 1=heavy hole; 2=light hole; 3= split-off hole
 potential                              = yes
 electric-field                         = yes
$end_output-bandstructure

$output-densities
 destination-directory                  = densities1/
 electrons                              = yes    ! [1e18 cm-3]
```

```
 holes                                  = yes  ! [1e18 cm-3]
 charge-density                         = yes
 piezo-electricity                      = yes
 pyro-electricity                       = yes
 interface-density                      = yes
 integrated-density                     = yes
 effective-density-of-states-Nc-Nv      = no
$end_output-densities

$output-current-data
 destination-directory                  = current1/
 current                                = no
 fermi-levels                           = yes
 mobility-out                           = no
 IV-curve-out                           = no
 recombination                          = no
$end_output-current-data
!***** OUTPUT STRAIN ******************!
$output-strain
 destination-directory                  = strain1/
 strain                                 = yes
 strain-simulation-system               = yes
$end_output-strain
```

- **GaN-Etch-Stop Structure 1D CV Simulation Codes**

```
$numeric-control
 simulation-dimension           = 1
 zero-potential                 = no
 varshni-parameters-on          = no
 lattice-constants-temp-coeff-on = no
 piezo-constants-zero           = no
 pyro-constants-zero            = no
 newton-method                  = Newton-3
 nonlinear-poisson-iterations   =  300
 nonlinear-poisson-residual     =  2.0d-9
```

```
$end_numeric-control

$simulation-dimension
 dimension   = 1
 orientation = 0 0 1
$end_simulation-dimension

$global-parameters
 lattice-temperature = 300.0d0
$end_global-parameters

$simulation-flow-control
 flow-scheme         = 2
 strain-calculation  = homogeneous-strain
$end_simulation-flow-control

$domain-coordinates
 domain-type            = 0 0 1
 z-coordinates          = -15d0 108.5d0
 pseudomorphic-on       = GaN
 growth-coordinate-axis = 0 0 1
 hkil-x-direction  =  1  0 -1  0
 hkil-z-direction  =  0  0  0  -1
 crystal-type         = wurtzite
$end_domain-coordinates

$regions
 region-number = 1   base-geometry = line   region-priority = 1
! gate
 z-coordinates = -15d0     -8.3d0
 region-number = 2     base-geometry = line   region-priority = 2
! Al2O3 gate dielectric
 z-coordinates = -8.3d0      0d0
 region-number = 3     base-geometry = line  region-priority = 3
! AlN
```

```
 z-coordinates = 0d0       0.5d0
 region-number = 4     base-geometry = line    region-priority = 4
! AlGaN
 z-coordinates = 0.5d0       3d0
 region-number = 5   base-geometry = line    region-priority = 5
! GaN substrate
 z-coordinates = 3d0       103.5d0
 region-number = 6     base-geometry = line    region-priority = 6
! drain
 z-coordinates = 103.5d0      108.5d0
$end_regions

$grid-specification
 grid-type       = 0 0 1
 z-grid-lines    = -15d0 -8.3d0  -0.1d0  0d0   0.01d0   0.13d0
0.49d0  0.5d0  0.51d0   2.9d0  3d0  3.1d0  33.5d0  50d0  102.5d0
103.5d0  108.5d0
 z-nodes     =  2     19        3     3       9       11       3
3      29       3      3     59      39     29       9        2
 z-grid-factors = 1d0   1d0      1d0   1d0      1d0     1d0   1d0
1d0    1d0   1d0    1d0   1.02d0   1.04d0  1d0     1d0      1d0
$end_grid-specification

$region-cluster
 cluster-number = 1    region-numbers = 1    ! Metal
 cluster-number = 2    region-numbers = 2         ! Al2O3
 cluster-number = 3    region-numbers = 3       ! AlN
 cluster-number = 4    region-numbers = 4        ! AlGaN
 cluster-number = 5    region-numbers = 5         ! GaN
 cluster-number = 6    region-numbers = 6  7  !(7 = default) Metal
$end_region-cluster

$material
 material-number = 1
 material-name   = Metal-wz
 cluster-numbers = 1
```

```
 material-number = 2
 material-name   = Al2O3                    ! Al2O3
 cluster-numbers = 2
 material-number = 3
 material-name   = AlN                      ! AlN
 cluster-numbers = 3
 material-number = 4
 material-name   = Al(x)Ga(1-x)N              ! default is wz
 alloy-function  = constant
 cluster-numbers = 4
 material-number = 5
 material-name   = GaN
 cluster-numbers = 5
 material-number = 6
 material-name   = Metal-wz
 cluster-numbers = 6
 crystal-type    = wurtzite
$end_material

$alloy-function
 material-number        = 4
 function-name          = constant
 xalloy                 = 0.15d0             ! Al0.15Ga0.85N
$end_alloy-function

$binary-wz-default
 binary-type                = GaN-wz-default
 apply-to-material-numbers  = 4 5
 piezo-electric-constants           = 0.67d0   -0.34d0   -0.29d0
 pyro-polarization                  =  0d0       0d0      -0.034d0
 static-dielectric-constants        = 10.4d0  10.4d0  10.4d0
 elastic-constants                  =  367d0    135d0     103d0
                                       405d0    95d0
 conduction-band-energies           = 2.694d0 6.190d0 6.490d0
valence-band-energies              = -0.726d0
```

```
 band-shift                              = 0d0
 absolute-deformation-potentials-cbs = 0d0   0d0   0d0
 uniax-vb-deformation-potentials      = 0d0    0d0    0d0
                                          0d0   0d0    0d0
$end_binary-wz-default

! AlN parameters:
$binary-wz-default
 binary-type                  = AlN-wz-default
 apply-to-material-numbers    = 3 4
 piezo-electric-constants      = 1.52d0    -0.56d0    -0.42d0
 pyro-polarization                    =  0d0         0d0        -0.090d0
 static-dielectric-constants          = 10.31d0    10.31d0    10.31d0
 elastic-constants                    =  396.0d0    137.0d0     108.0d0
                                         373.0d0    116.0d0
 conduction-band-energies     = 4.604d0 5.710d0   5.41d0
 valence-band-energies                = -1.526d0
 band-shift                            = 0.12d0
! 0.75 band alignment factor
 absolute-deformation-potentials-cbs = 0d0   0d0   0d0
 uniax-vb-deformation-potentials      = 0d0   0d0    0d0
                                          0d0   0d0    0d0
$end_binary-wz-default

$ternary-wz-default
 ternary-type = Al(x)Ga(1-x)N-wz-default
 apply-to-material-numbers    = 4
 bow-piezo-electric-constants            = 0d0       -0.52d0      0d0
 bow-pyro-polarization                   = 0d0       0d0       -0.019d0
 bow-conduction-band-energies            = 0.71d0     0.80d0    0.61d0
 band-shift                              = 0.023d0
! To have the 0.75 factor bandalign
$end_ternary-wz-default

! ALD Al2O3 with Eg=6.4eV. Conduction band-offset on GaN = 2.1 eV
```

```
! Ev = -0.726(GaN Ev)+3.42(GaN Eg)+2.1-6.4(Al2O3 Eg) = -1.606 (300K)
! E_c = E_v    + E_gap(lh) + ...          = 4.794 eV

$binary-wz-default
 binary-type                 = Al2O3-wz-default
 apply-to-material-numbers   = 2
 piezo-electric-constants     = 0d0   0d0   0d0
 pyro-polarization                    =  0d0       0d0       0d0
 static-dielectric-constants = 8d0  8d0  8d0
! for ALD Al2O3 dielectric constant
 conduction-band-energies    = 4.794d0 5.710d0  5.41d0
 valence-band-energies               = -1.606d0
 band-shift                          = 0d0
 absolute-deformation-potentials-cbs = 0d0      0d0      0d0
 uniax-vb-deformation-potentials     = 0d0   0d0   0d0
                                       0d0   0d0   0d0
$end_binary-wz-default

$doping-function
 doping-function-number        = 1     ! GaN substrate doping
 impurity-number               = 1
 doping-concentration          = 0.001d0
 only-region                   = 3d0   103.5d0
 doping-function-number        = 2      ! Al2O3 positive charge
 impurity-number               = 2
 doping-concentration          = 2420d0
 only-region                   = 0.02d0   0.12d0
 doping-function-number     = 3         ! buffer trap
 impurity-number            = 3
 doping-concentration       = 200d0
 only-region                = 102.5d0  103.5d0
 doping-function-number     = 4
 impurity-number            = 4
 doping-concentration       = 0.2d0
 only-region                = 0.02d0  0.12d0
```

```
doping-function-number      = 5
impurity-number             = 5
doping-concentration        = 0.5d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 6
impurity-number             = 6
doping-concentration        = 1.6d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 7
impurity-number             = 7
doping-concentration        = 1.7d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 8
impurity-number             = 8
doping-concentration        = 1.6d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 9
impurity-number             = 9
doping-concentration        = 1.4d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 10
impurity-number             = 10
doping-concentration        = 1.2d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 11
impurity-number             = 11
doping-concentration        = 0.8d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 12
impurity-number             = 12
doping-concentration        = 0.7d0
only-region                 = 0.02d0  0.12d0
doping-function-number      = 13
impurity-number             = 13
doping-concentration        = 0.6d0
```

```
 only-region                = 0.02d0  0.12d0
 doping-function-number     = 14
 impurity-number            = 14
 doping-concentration       = 0.5d0
 only-region                = 0.02d0  0.12d0
 doping-function-number     = 15
 impurity-number            = 15
 doping-concentration       = 0.45d0
 only-region                = 0.02d0  0.12d0
 doping-function-number     = 16
 impurity-number            = 16
 doping-concentration       = 0.4d0
 only-region                = 0.02d0  0.12d0
 doping-function-number     = 17
 impurity-number            = 17
 doping-concentration       = 0.35d0
 only-region                = 0.02d0  0.12d0
$end_doping-function

$impurity-parameters
 impurity-number               = 1
 impurity-type                 = n-type
 number-of-energy-levels       = 1
 energy-levels-relative        = -100d0
 degeneracy-of-energy-levels   = 2
 impurity-number               = 2
 impurity-type                 = n-type
 number-of-energy-levels       = 1
 energy-levels-relative        = -100d0
 degeneracy-of-energy-levels   = 2
 impurity-number               = 3
 impurity-type                 = p-type
 number-of-energy-levels       = 1
 energy-levels-relative        = 3.17d0
 degeneracy-of-energy-levels   = 4
```

```
impurity-number              = 4
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2d0
degeneracy-of-energy-levels  = 2
impurity-number              = 5
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.05d0
degeneracy-of-energy-levels  = 2
impurity-number              = 6
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.1d0
degeneracy-of-energy-levels  = 2
impurity-number              = 7
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.15d0
degeneracy-of-energy-levels  = 2
impurity-number              = 8
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.2d0
degeneracy-of-energy-levels  = 2
impurity-number              = 9
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.25d0
degeneracy-of-energy-levels  = 2
impurity-number              = 10
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.3d0
degeneracy-of-energy-levels  = 2
```

```
impurity-number              = 11
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.35d0
degeneracy-of-energy-levels  = 2
impurity-number              = 12
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.4d0
degeneracy-of-energy-levels  = 2
impurity-number              = 13
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.45d0
degeneracy-of-energy-levels  = 2
impurity-number              = 14
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.5d0
degeneracy-of-energy-levels  = 2
impurity-number              = 15
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.55d0
degeneracy-of-energy-levels  = 2
impurity-number              = 16
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.6d0
degeneracy-of-energy-levels  = 2
impurity-number              = 17
impurity-type                = n-type
number-of-energy-levels      = 1
energy-levels-relative       = 2.65d0
degeneracy-of-energy-levels  = 2
```

```
$end_impurity-parameters

!****** QUANTUM
$quantum-regions
 region-number          = 1
 base-geometry          = line
 region-priority        = 1
 z-coordinates          = -0.5d0 50d0
$end_quantum-regions

$quantum-cluster
 cluster-number         = 1
 region-numbers         = 1
 deactivate-cluster     = no
$end_quantum-cluster

$quantum-model-electrons
 model-number                           = 1
 model-name                             = effective-mass
 cluster-numbers                        = 1
 conduction-band-numbers                = 1    ! Gama band
 number-of-eigenvalues-per-band         = 10
 separation-model                       = eigenvalue
 maximum-energy-for-eigenstates         = 1d0
 quantization-along-axes                = 0 0 1
 boundary-condition-001                 = Dirichlet
$end_quantum-model-electrons

$quantum-model-holes
 model-number                           = 1
 model-name                             = effective-mass
 cluster-numbers                        = 1
 valence-band-numbers                   = 1
 number-of-eigenvalues-per-band         = 1
 separation-model                       = eigenvalue
```

```
 maximum-energy-for-eigenstates          = 1d0
 quantization-along-axes                 = 0 0 1
 boundary-condition-001                  = Dirichlet
$end_quantum-model-holes

$poisson-boundary-conditions
 poisson-cluster-number          = 1       ! Gate
 region-cluster-number           = 1
 applied-voltage                 = -0.2d0
 boundary-condition-type         = Schottky
 schottky-barrier                = 3.5d0
 contact-control                 = voltage
 poisson-cluster-number          = 2            ! insulator
 region-cluster-number           = 2
 boundary-condition-type         = Fermi-linear
 Fermi-linear-reference-clusters = 1 3
 poisson-cluster-number          = 3        ! AlN
 region-cluster-number           = 3
 applied-voltage                 = 0.0d0
 boundary-condition-type         = Fermi
 contact-control                 = voltage
 poisson-cluster-number          = 4            ! AlGaN
 region-cluster-number           = 4
 applied-voltage                 = 0.0d0
 boundary-condition-type         = Fermi
 contact-control                 = voltage
 poisson-cluster-number          = 5             ! GaN
 region-cluster-number           = 5
 applied-voltage                 = 0.0d0
 boundary-condition-type         = Fermi
 contact-control                 = voltage
 poisson-cluster-number          = 6      ! Source/Drain
 region-cluster-number           = 6
 applied-voltage                 = 0.0d0
 boundary-condition-type         = ohmic
```

```
 contact-control                  = voltage
$end_poisson-boundary-conditions

$voltage-sweep
 sweep-number                          = 1
 sweep-active                          = yes
 poisson-cluster-number                = 1
 step-size                             = 0.08d0
 number-of-steps                       = 44
 data-out-every-nth-step               = 1
$end_voltage-sweep

!****** OUTPUT
$output-bandstructure
 destination-directory                 = band_struc1/
 conduction-band-numbers               = 1
 valence-band-numbers                  = 1 2 3
 potential                             = yes
$end_output-bandstructure

$output-densities
 destination-directory                 = densities1/
 electrons                             = yes
 holes                                 = no
 charge-density                        = yes
 ionized-dopant-density              = no
 piezo-electricity                     = no
 pyro-electricity                      = no
 interface-density                     = yes
 subband-density                       = no
 integrated-density                    = yes
$end_output-densities

$output-1-band-schroedinger
 destination-directory                 = sg_1band1/
```

```
 sg-structure                                = yes
 conduction-band-numbers                     = 1
 cb-min-ev                                   = 1
 cb-max-ev                                   = 10
$end_output-1-band-schroedinger

$output-current-data
 destination-directory                       = current1/
 current                                     = no
 fermi-levels                                = yes
 mobility-out                                = no
 IV-curve-out                                = no
 recombination                               = no
$end_output-current-data

$output-material
 destination-directory = material_parameters/
 doping-concentration  = doping_concentration1D.dat
$end_output-material
```

Appendix D Matlab Least-Square Fitting Codes for TLSC and TLSCII Models

- **TLSC Model Least-Square Fitting**

```
close all
clear all
clc
path='file location\';
file = dir([path '*neg*100C.TXT']);
filenames = {file.name};

S=100e-4*50e-4;%cm2 area
%basic parameters:
%electron charge:
q=1.6e-19;
%vaccum dielectric constant
ep0 = 8.85e-12;
k = 1.38e-23;
%electron saturation velocity:
ve = 2e7;%cm/s
%hole saturation velocity:
vh = 5e6;%cm/s
% GaN dielectric constant:
ep_gn=10.4;
%Temperature
T = 273.15+100;% K
%GaN effective density of state
Nc = 4.3e14*T^1.5;%cm^-3

for N = 1:length(filenames)
    A = load([path filenames{N}]);
    name = filenames{N};
```

```
  %read in data that needs to be fitted:
    V0 = abs(A(:,1)); %V
    I0 = abs(A(:,2)/S); %A/cm2

    % Fermi-level:
    Ef = -1:0.002:-0.36;%eV
    % electron density:
    n = Nc*exp(Ef*q/k/T);%cm^-3
    %current:
    J = q*n*ve;%A/cm2
%GaN thickness:
    tgan0 = 2;%um thickness

%Acceptor Trap energy
    Et = [-0.85,-0.8,-0.75,-0.7,-0.65,-0.6,-0.55,-0.5,-0.45,-0.4,-
0.35,-0.3];
    numEt = length(Et);

    %nonlinear optimization
    % Accepter trap density:x1e16
    Nt0 = 2*ones(1,numEt);
    Vi0 = 100;
    %with initial Vi:
    X0=[Vi0,Nt0];
    LB=[0,zeros(1,numEt)];
    UB=[300,ones(1,numEt)*11];

    options = optimset('TolFun',1e-12,'TolX',1e-12,...
    'MaxFunEvals',5000);
    X=X0;

  for M=1:3
    X0=X;
[X,resnorm,~,exitflag,output]=lsqnonlin(@(x)TLSCfun(x,T,tgan0,Ef,Et,
n,V0,I0),X0,LB,UB,options)
    Vi = X(1);
```

```
    Ei =Vi/tgan0*1e-6*1e4;%MV/cm
    tgan=tgan0*1e-6;%m
    Nt=X(2:end);%1e16cm-3

   for i=1:length(Ef)
        nt = Nt./(1+exp((Et-Ef(i))*q/k/T))*1e16;%cm^-3
        % max electric field:
        nt_total(i) = sum(nt);
        Emax(i) = q*tgan*(n(i)+nt_total(i))*1e6/ep0/ep_gn/1e6*1e-
2+Ei;%MV/cm
        %voltage:
        V(i) = (Emax(i)+Ei)*1e6*1e2*tgan/2;
    end
    figure
    plot(V0,I0,'o b',V,J,'k -')
  end
end

function y=TLSCfun(X0,T,tgan,Ef,Et,n,V0,I0)
%Nt is the trap desnity array in unit of 1e16cm-3
%tgan is in meter
%Ef is fermi energy. Reference potential Ec = 0
%Et is trap energy
%basic parameters:
%electron charge:
q = 1.6e-19;
%vacuum dielectric constant
ep0 = 8.85e-12;
k = 1.38e-23;
%electron saturation velocity:
ve = 2e7;%cm/s
% GaN dielectric constant:
ep_gn=10.4;

J = q*n*ve;%A/cm2
```

```
 Ei =X0(1)/tgan*1e-2;%MV/cm
 tgan=tgan*1e-6;%m
 Nt=X0(2:end);%1e16cm-3

%J is increasing order. So pick the stopping point:
S1 = find(J<min(I0)/1.5,1,'last');
S2 = find(J > 1.2*max(I0),1,'first');

V = zeros(1,S2-S1+1);

for i=S1:S2
    nt = Nt./(1+exp((Et-Ef(i))*q/k/T))*1e16;%cm^-3
    % max electric field:
    Emax = q*tgan*(n(i)+sum(nt))*1e6/ep0/ep_gn/1e6*1e-2+Ei;%MV/cm
    %voltage:
    V(i-S1+1) = (Emax+Ei)*1e6*1e2*tgan/2;
end

J=J(S1:S2);
% pick I0 to find it in J and fit V
y = zeros(1,length(I0));

for i=1:length(I0)
   [~,IX] = min(abs(I0(i)-J)/I0(i));
   y(i) = V(IX)-V0(i);
end
end
```

- **TLSCII Model Least-Square Fitting**

```
close all
clear all
clc
path='file location\';
file = dir([path '*neg*100C.TXT']);
```

```
filenames = {file.name};

S=100e-4*50e-4;%cm2 area
%basic parameters:
%electron charge:
q=1.6e-19;
%vaccum dielectric constant
ep0 = 8.85e-12;
k = 1.38e-23;
%electron saturation velocity:
ve = 2e7;%cm/s
%hole saturation velocity:
vh = 5e6;%cm/s
% GaN dielectric constant:
ep_gn=10.4;
%Temperature
T = 273.15+100;% K
%GaN effective density of state
Nc = 4.3e14*T^1.5;%cm^-3

for N = 1:length(filenames)
    A = load([path filenames{N}]);
    name = filenames{N};
  %read in data that needs to be fitted:
    V0 = abs(A(:,1)); %V
    I0 = abs(A(:,2)/S); %A/cm2

    % Fermi-level:
    Ef = -1:0.002:-0.36;%eV

    % electron density:
    n0 = Nc*exp(Ef*q/k/T);%cm^-3

    %GaN thickness:
    tgan0 = 2;%um thickness
```

```
    %injection E field
    Ei0 = 0;%kV/cm

    %nonlinear optimization
    %Acceptor Trap energy
    Et = [-0.85,-0.8,-0.75,-0.7,-0.65,-0.6,-0.55,-0.5,-0.45,-0.4,-
0.35,-0.3];
    numEt = length(Et);
    %nonlinear optimization
    % Accepter trap density:x1e16
    Nt0 = 2*ones(1,numEt);
    X0=Nt0;
    LB=zeros(1,numEt);
    UB=ones(1,numEt)*9;
%     Vi0 = 59.1162; % Vi0 calculated from TLSC model
%     Vi0=237.7;
      Vi0=0;
    options = optimset('TolFun',1e-12,'TolX',1e-
12,'MaxFunEvals',8000,'MaxIter',1000);

    X=X0;
  for K=1:3
    X0=X;%take previous result as new starting point

[X,resnorm(K),~,exitflag,output]=lsqnonlin(@(x)TLSCIIfun(x,T,tgan0,E
f,Et,n0,V0,I0,Vi0),X0,LB,UB,options);

    Vi =Vi0;%MV/cm
    Ei =Vi/tgan0*1e-6*1e4;%MV/cm
    tgan=tgan0*1e-6;%m
    Nt=X;%1e16cm-3

    nt = zeros(1,length(Ef));
    for i=1:length(Ef)
        nt(i) = sum(Nt./(1+exp((Et-Ef(i))*q/k/T)))*1e16;%cm^-3
```

```
    end
    M = ones(1,length(n0));
    Emax = zeros(1,length(n0));
    % positions:
    x= 0:tgan/100:tgan;%in m

    for i=1:length(n0)
        %ignore the effect of p:
        E = q*(nt(i)+n0(i))*1e6/ep0/ep_gn*x/1e6*1e-2+Ei;% in MV/cm
        % impact ionization
        alpha = 2.9e8*exp(-3.4e7./(E*1e6));%/cm
        M(i)=1./(1-trapz(x*1e2,alpha));%convert x to cm
        %max E field: in MV/cm
        Emax(i) = q*(nt(i)+n0(i))*1e6/ep0/ep_gn*tgan/1e6*1e-2+Ei;
        if q*n0(i)*M(i)*ve > 1.1*max(I0)
            break;
        end
    end

    %current:
    J = q*n0(1:i).*M(1:i)*ve;%A/cm2
    J0=q*n0(1:i)*ve;%A/cm2 avalanche inducing electron current
    Jh = J-J0; %hole current

    %voltage:
    V = (Emax(1:i)+Ei)*1e6*1e2*tgan/2;%trapzoidal shape

    figure
    plot(V,J,'k -',V,Jh,'m --',V0,I0,'b o')

  end
end


function y = TLSCIIfun(X0,T,tgan,Ef,Et,n0,V0,I0,Vi0)
```

```
%basic parameters:
%electron charge:
q = 1.6e-19;
%vacuum dielectric constant
ep0 = 8.85e-12;
k = 1.38e-23;
%electron saturation velocity:
ve = 2e7;%cm/s
%hole saturation velocity:
vh = 5e6;%cm/s
% GaN dielectric constant:
ep_gn=10.4;

%Nt is the only fitting parameters
tgan = tgan*1e-6;%m
Nt = X0;
E0inj = Vi0/tgan*1e-8;%MV/cm

nt=zeros(1,length(Ef));
for i=1:length(Ef)
    nt(i) = sum(Nt./(1+exp((Et-Ef(i))*q/k/T)))*1e16;%cm^-3
end

% multiplication factor:
M=ones(1,length(n0));
Emax=zeros(1,length(n0));

S1 = find(n0<min(I0)/q/ve/1.5,1,'last');%find the starting point

% positions:
x= 0:tgan/100:tgan;%in m

for i=S1:length(n0)
%ignore the effect of p:
E = q*(nt(i)+n0(i))*1e6/ep0/ep_gn*x/1e6*1e-2+E0inj;% in MV/cm

% impact ionization
```

```
alpha = 2.9e8*exp(-3.4e7./(E*1e6));%/cm
M(i)=1./(1-trapz(x*1e2,alpha));%convert x to cm

%max E field:
Emax(i) = q*(nt(i)+n0(i))*1e6/ep0/ep_gn*tgan/1e6*1e-2+E0inj;% in MV/cm
S2=i;
if q*n0(i)*M(i)*ve > 1.2*max(I0)%stop if J is larger than max(I0)*1.2
    break;
end
end

J = q*n0(S1:S2).*M(S1:S2)*ve;%A/cm2
V = (Emax(S1:S2)+E0inj)*1e6*1e2*tgan/2;%trapzoidal shape

% pick I0 to find it in J and fit V
y=zeros(1,length(I0));
for i=1:length(I0)
   [~,IX] = min(abs(I0(i)-J)/I0(i));
   y(i) = V(IX)-V0(i);
end
end
```

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