CMOS Passive Pixel Imager Design Techniques

by

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Abstract

CMOS technology provides an attractive alternative to the currently dominant CCD technology for implementing low-power, low-cost imagers with high levels of integration. Two pixel configurations are possible in CMOS technology: active and passive. The active pixel requires a minimum of three transistors to convert light to voltage. The passive pixel, on the other hand, consists of a single transistor, and its output is in the form of charge. Column-parallel opamps are used to amplify the charge to a voltage output. The main advantage of the passive pixel is a higher fill factor in a given pixel geometry. This advantage becomes increasingly important as we scale to smaller pixel sizes. The higher fill factor comes at a high cost as the charge output on the high impedance node of the column line is susceptible to disturbances, namely a parasitic current and temporal noise. The goal of this thesis is to determine the source and effects of the disturbances on the image sensor characteristics and the repercussions for scaling to high-density arrays.

A signal-dependent parasitic current composed of optically-generated carrier diffusion, blooming and subthreshold currents contaminates the pixel output. This parasitic current is detrimental to the imager because a few bright pixels can affect the rest of the pixels on the column line, resulting in bright vertical stripes on the image. A correlated-double sampling circuit in a differential architecture is used to remove the effects of the parasitic current. Column fixed-pattern noise is maintained below 1.5% for the linear illumination range of the imager.

A noise analysis reveals the opamp read noise is the dominant source of temporal noise. The effects of the sample-and-hold readout circuit on the output-referred opamp read noise are modeled and closely match the measured noise. The output read noise power is directly proportional to the vertical resolution of the imager and inversely proportional to the pixel area, resulting in a strong dependence between noise and pixel density.

This co-dependence is further analyzed in a scaling model where the fill factor, noise and dynamic range are observed for varying pixel size and vertical resolution over three fabrication technologies. The fill factor decreases with pixel size, and is highest for the technology with the smallest feature size, $0.18\mu m$. The noise increases with decreasing pixel size and increasing vertical resolution and has the best performance in the $0.18\mu m$ technology. The dynamic range decreases with pixel density, but has a strong dependence on the power supply voltage of the technology.

Thesis Supervisor: Charles G. Sodini
Title: Professor of Electrical Engineering

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Dedication

I dedicate this thesis to Uchan and Twooey.

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Chapter 1

Introduction

1.1 Motivation

The increased demand for affordable consumer digital cameras has led camera manufacturers to look beyond the mature, but costly, Charge-Coupled Devices (CCD) technology to alternative methods in solid-state imaging, such as CMOS image sensors [1], [2]. CMOS imagers can be integrated with analog and digital functional blocks in a standard CMOS process leading to significant cost reductions [3]. Additional benefits include random access readout and low power consumption [4].

In addition to low cost and low power, the consumer digital camera market demands high spatial resolution [5] in order to match the quality of high-definition images produced with film cameras. Since the cost of an imager is directly proportional to silicon area, the combination of low cost and high resolution specifications can be achieved with a high-density imager containing more pixels per unit area. The reduction in pixel area, however, results in lower fill factor, or ratio of photodiode to pixel area for a given technology. Most CCD and CMOS imagers currently use microlenses to improve the collection efficiency of shrinking pixels. While they provide a temporary solution, microlenses are costly and their efficiency is beginning to reach limits for small pixels [6].

Recent efforts to achieve high fill factors in small pixel area have focused on reducing the number of transistors and contacts per pixel [7], [8]. Active pixel sensors (APS) using capacitively coupled bipolar transistors are also a viable option for high density arrays [9], but require a costly BiCMOS process and suffer from fixed-pattern noise (FPN) values as high as 10% [10].

The CMOS passive pixel presents a promising alternative to the active pixel for achieving a high fill factor in small pixel geometries. Similar to the history of the single-transistor DRAM cell [11], the passive pixel has the potential to make high-density imaging arrays available at a lower cost. For a given technology and fill factor, the passive pixel can achieve a higher pixel density. Conversely, for a given technology and pixel density, the passive pixel yields a larger fill factor. Consisting of a single transistor for readout and row select, the passive pixel has the added advantage of a lower pixel FPN and a linear transfer function. Fill factors as high as 80 % have been reported for a CIF format passive pixel imager [12].

The advantages of using a passive pixel for its higher fill factor come at a high cost. Since charge-to-voltage conversion does not occur within the pixel, the charge signal becomes extremely sensitive to disturbances on the column line. Additional implants and fabrication steps can be used to reduce these disturbances [13], [14], but the increase in cost and complexity does not justify the use of a passive pixel imager. The goal of this thesis is to identify the source/s of the disturbances, quantify its effects and determine the limitations it poses on scaling to high-density arrays.

One of the disturbances manifests itself in the form of a leakage current, or parasitic current, at each column line. Three mechanisms are identified as the causes of this current: optically-generated carrier diffusion, blooming and subthreshold currents. The effects of this current are catastrophic to the output signal as a few bright pixels can contaminate the output of all pixels on the column line, leading to bright vertical streaks in the image. Column FPN measurements demonstrate a correlated double-sampling (CDS) circuit in a differential architecture is effective in removing the effects of the parasitic current.

An additional problem that limits the signal-to-noise ratio (SNR) of passive pixels for large imaging arrays is the temporal noise. In this thesis, the temporal noise is decomposed into the basic components: read noise, reset noise and dark current shot noise. Measurements indicate that the opamp read noise is the main contributor to the noise. The read noise of the amplifier, which is not present in active pixels, is amplified by the loop gain of the output circuit, $\frac{C_{line}}{C_{fb}}$, where C_{line} is the parasitic capacitance of the column line and C_{fb} is the feedback capacitance. Since C_{line} is proportional to the number of rows per column and C_{fb} is designed to match the pixel capacitance, the closed-loop gain which amplifies the column amplifier noise is unusually high for passive pixel output circuits, i.e. > 50, and therefore limits the SNR for low light levels and the dynamic range of the imager.

The severity of the temporal noise becomes obvious when scaling to higher density arrays. An increase in the number of rows leads to an increase in the loop gain through the line capacitance. A smaller pixel size further exacerbates the problem by decreasing the feedback capacitance and thus increasing the loop gain. The scaling of both parameters therefore result in higher noise. Designing in a smaller fabrication technology (i.e. $0.18\mu m$) can alleviate the noise problems by increasing the pixel capacitance through a higher fill factor, and decreasing the line capacitance with smaller row select transistors. The lower power supply voltage, however, significantly reduces the dynamic range.

1.2 Thesis Organization

Chapter 2 provides a brief background on the passive pixel and a derivation of the expression relating photons and output voltage. The passive pixel structure and amplifier specifications are also discussed. A comparison between the active vs. passive pixels is given.

Chapter 3 introduces the sources of parasitic current and illustrates its effects on the pixel output. A CDS circuit in a differential architecture is then presented. FPN measurements quantify the efficiency of the CDS circuit and an image demonstrates the effects of the parasitic current have been completely removed.

The temporal and FPN sources are listed in Chapter 4. The effect of each noise source on the output voltage is explained and noise measurements are presented for a number of circuit parameters.

The limits of the passive pixel when scaling for high-density arrays are illustrated in Chapter 5. The effects of decreasing pixel size and increasing vertical resolution on the pixel fill factor, temporal noise and dynamic range are observed for three fabrication technologies.

Chapter 6 concludes this thesis with a list of contributions and ideas for future work.

Chapter 2

Passive Pixel

This chapter begins with a background of previous work done on the passive pixel. A typical CMOS passive pixel architecture is then presented. The pixel operation is divided into two parts: light-to-charge conversion, and charge-to-voltage amplification. The final result is an expression between the photon flux and the output voltage. Second order effects, such as image lag, finite opamp gain and opamp offset voltage, are also considered. The implementation of a CMOS passive pixel is described in Sec. 2.6. Advantages and disadvantages of three different photodiode implementations are discussed. An explanation of the effects of pixel and parasitic line capacitance on opamp specifications is also presented.

A comparison between the active and passive pixel is given. Three advantages, mainly a larger fill factor, lower pixel fixed-pattern noise (FPN) and a linear transfer function, are cited as the motivation for this thesis. A larger fill factor is usually achieved with the passive pixel since it requires a single transistor, leaving plenty of pixel area for photon sensing. The lower pixel FPN is attributed to the simplicity of the passive pixel. In contrast with the active pixel, the passive pixel does not have any amplification or level shifting within the pixel, making it independent of device mismatches from pixel to pixel. Finally, the passive pixel uses a voltage-independent poly-to-poly capacitor, rather than the photodiode depletion capacitance, for the charge-to-voltage conversion, leading to a linear transfer function.

2.1 Background

The passive pixel has a long history, longer than CCD's and the active pixel, dating back to 1967. G. P. Weckler was the first to implement a photodiode with an MOS process and operate it in integrating mode [15]. P. J. W. Noble followed him a year later with a 10-by-10 array with an integrating charge amplifier [16]. Both Weckler's and Noble's designs were limited by the dark current and high parasitics, not to mention FPN and blooming, of the technology at the time.

Almost thirteen years later, Hitachi reported the implementation of a 320 x 244 passive pixel sensor with high sensitivity and a FPN suppressing circuit. Using an additional P^+ implant, S. Ohba et. al. successfully reduced the FPN by 20 dB [13]. Hitachi later combined the passive pixel with a three-phase horizontal bulk charge-transfer device, similar to the ones used by CCD's at the time. Using a hybrid circuit made up of enhancement-mode and depletion-mode transistors, H. Ando et. al. were able to isolate the high column line capacitance in order to limit the read noise of the output amplifier [14].

Profitting from the advances in VLSI technology in 1989, R. H. Wyles integrated a full column-parallel architecture in which one capacitive feedback transimpedance amplifier is used to read each column [17]. Prior to this point, column-parallel architectures had been difficult to implement since the readout circuits were too bulky to pitch-match the pixel. Shortly thereafter, D. Renshaw and P. B. Denyer reported on the integration of computational and control functions with 786 x 576 passive pixel arrays in a CMOS $0.8\mu m$ technology [18].

More recently, W. Hoekstra et. al. published a CIF format (352(H) x 288(V)) passive pixel array in a CMOS $0.5\mu m$ technology, achieving a fill factor of 80% [12]. Despite the high fill factor it represents, the passive pixel has been dismissed as "noisy" and "unscalable" for visible range imagers [19], [20].

2.2 Architecture

Fig. 2-1 shows the architecture of a simple passive pixel imager, consisting of a pixel array, output circuit and row/column decoders [18]. The pixel array is read out in a typical raster-scan fashion. An entire row is selected for readout simultaneously and the corresponding charge from each pixel appears on the respective column line. The multiplexer then selects

one column at a time for charge-to-voltage conversion by the capacitive-feedback amplifier.

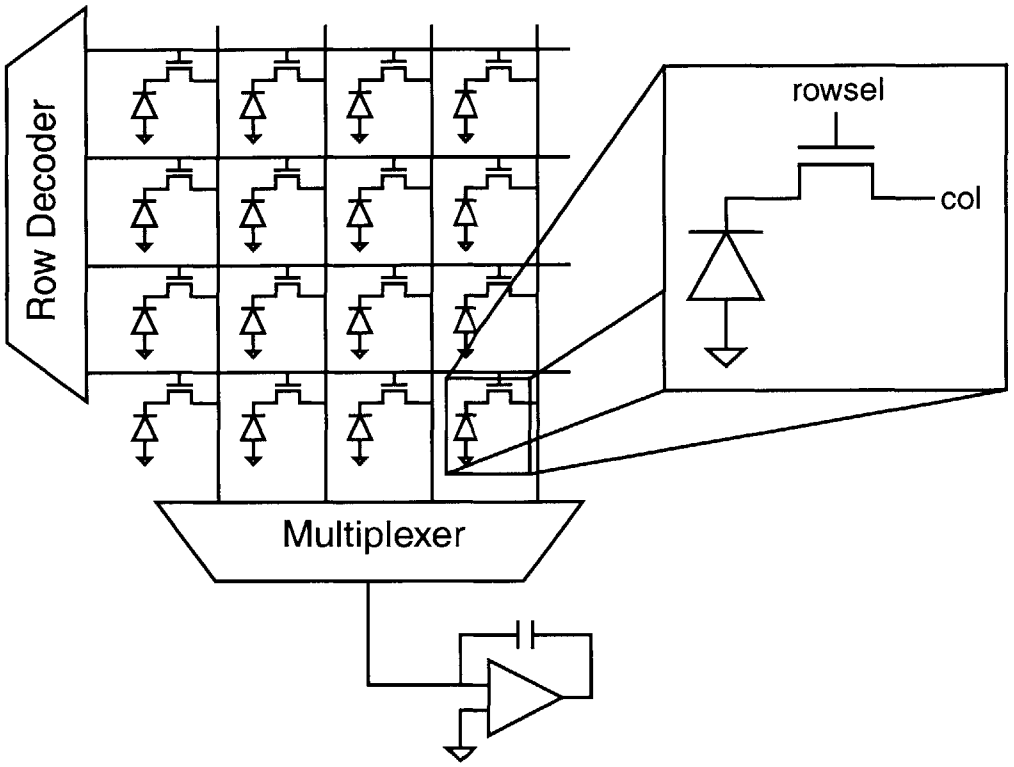


Figure 2-1: Simple Passive Pixel Architecture.

2.3 Pixel Operation - From photons to electrons

Pixel photocurrent arises when photons exhibiting an energy higher than the bandgap energy of the material (1.1 eV for Silicon) generate electron-hole pairs, as shown in figure 2-2. The electric field at the edge of the depletion region of the photodiode then separates the electron-hole pairs and the corresponding electrons and holes are collected in the N-well and P-substrate respectively.

The amount of charge collected in the N-well depends on the location of the generated carriers. If the carriers are generated right at the edge of the depletion region, they will be immediately separated and collected. If, on the other hand, the photon is absorbed in the N-well or P-substrate, the carriers will have to diffuse to the depletion region before they can be collected. Depending on the doping profile and surface trap density of the material,

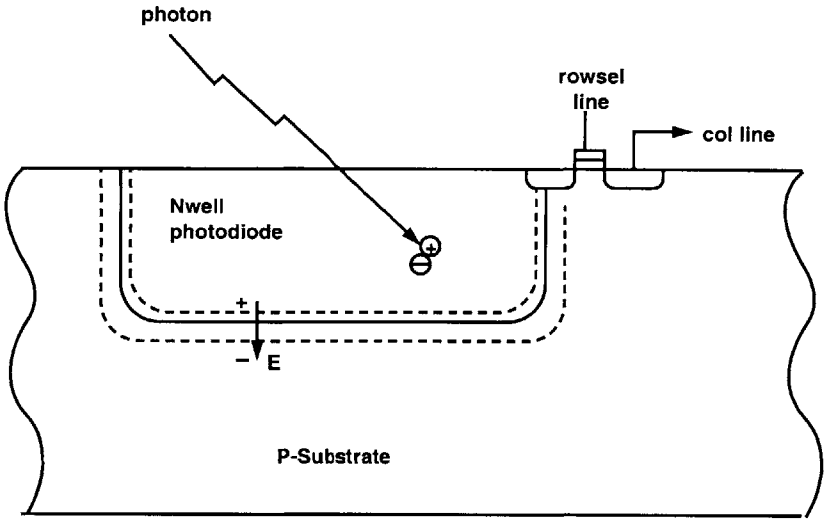


Figure 2-2: Cross-section of passive pixel with N-well to P-substrate photodiode.

some carriers will be lost to recombination.

Since the photocurrent is much too small to measure accurately, it must be integrated over a period of time. The collected pixel charge during a single integration period, T_{int}, for a particular wavelength, λ, can be expressed as:

$$Q_{pix}(\lambda) = q \cdot \eta(\lambda) \cdot N_{ph}(\lambda) \tag{2.1}$$

where q is the charge per unit electron, $\eta(\lambda)$ is the quantum efficiency of the device, and $N_{ph}(\lambda)$ is the number of photons impinging on the device.

2.3.1 Quantum efficiency

The quantum efficiency (QE), $\eta(\lambda)$, is defined as the number of collected electrons per pixel divided by the number of photons impinging on the device. It is linearly proportional to the fill factor since the latter determines the ratio of photons hitting the photo active region. The photons that hit the metal-covered area of the pixel are reflected back. The QE is a function of the wavelength of the light as well as the structure and geometry of the pixel. Short wavelengths are absorbed near the surface of the photodiode, whereas longer wavelengths penetrate deeper into the Silicon. The doping profile of the material will then

determine the probability of the generated carriers being collected by the photodiode.

The total quantum efficiency of the pixel can be written to reveal its linear relationship with the fill factor:

$$\eta(\lambda) = \eta_o(\lambda) \cdot FF \tag{2.2}$$

where η_o is independent of the pixel fill factor. The pixel fill factor, FF, is defined as the ratio of the drawn photodiode area to the total pixel area.

2.3.2 Photon Count

The number of photons impinging on a pixel, N_{ph}, is calculated by dividing the optical power per unit area (P) at the surface of the device by the energy of a single photon (E_{ph}) at wavelength λ. The total number of photons, of a particular wavelength, impinging on a pixel during an integration time, T_{int}, is then:

$$N_{ph}(\lambda) = \frac{P(\lambda)}{E_{ph}(\lambda)} \cdot T_{int} \cdot A_{pix} \tag{2.3}$$

The energy of a photon is expressed by:

$$E_{ph}(\lambda) = \frac{hc}{\lambda} \tag{2.4}$$

where h is Planck's constant ($6.626x10^{-34} Js$) and c is the speed of light ($3x10^8 m/s$).

Combining equations 2.3 and 2.4, we get an expression for the total number of photons:

$$N_{ph}(\lambda) = \frac{P(\lambda) T_{int} A_{pix} \lambda}{hc} \tag{2.5}$$

The number of photons impinging on the photodiode for wavelength λ, is then proportional to the optical power, integration time and pixel area.

2.3.3 Photon-to-electron pixel gain

The pixel charge can now be rewritten by substituting equation 2.1 with equations 2.2 and 2.5.

$$Q_{pix}(\lambda) = \frac{q \cdot FF \cdot T_{int} \cdot A_{pix}}{hc} \cdot \lambda \eta_o(\lambda) P(\lambda) \tag{2.6}$$

We can define the light-to-charge gain of a pixel for a particular wavelength as the collected charge per optical power per wavelength.

$$G_{ph-q} = \frac{Q_{pix}}{\lambda P(\lambda)} = \frac{q \cdot FF \cdot T_{int} \cdot A_{pix}}{hc} \eta_o(\lambda) \tag{2.7}$$

for $400nm < \lambda < 1100nm$.

This formula tells us that the gain from light-to-pixel charge depends on the quantum efficiency, pixel fill factor, integration time and pixel area. An increase in any one of these terms will directly result in a higher gain. The quantum efficiency is optimized and predetermined by the choice of photodiode and process flow. The fill factor depends on pixel design and pixel area. Integration time can be traded off for higher dark current shot noise, to a maximum of 1/frame rate. Pixel area is usually constrained by total die size and spatial resolution. As the spatial resolution of an imager increases, A_{pix} and T_{int} tend to decrease, thereby accentuating the importance of high quantum efficiency and high fill factor.

2.3.4 Total pixel charge

The total pixel charge can be calculated by taking the integral of equation 2.6 over the imaging wavelength range for the material,

$$Q_{pix,tot} = \frac{q \cdot FF \cdot T_{int} \cdot A_{pix}}{hc} \int_{\lambda_1}^{\lambda_2} \lambda \cdot P(\lambda) \cdot \eta_o(\lambda)\, d\lambda \tag{2.8}$$

for $\lambda_1 = 400nm$ and $\lambda_2 = 1100nm$ for Silicon.

2.4 Pixel Readout - From electrons to Volts

When a column is selected by the multiplexer for pixel readout, we get the circuit configuration shown in Fig. 2-3 [16]. The pixel is shown in the shaded area with *rowsel* as the access signal and *col* as the pixel output. Node *col* has a parasitic capacitance, C_{line}, due to the drain-to-bulk and gate-to-drain capacitance of all row-select transistors connected to the column line as well as the metal-to-substrate capacitance of the line.

If the rowsel signal is pulsed for a time period much shorter than the settling time of the opamp, the readout cycle can be separated into four phases: output circuit reset (I),

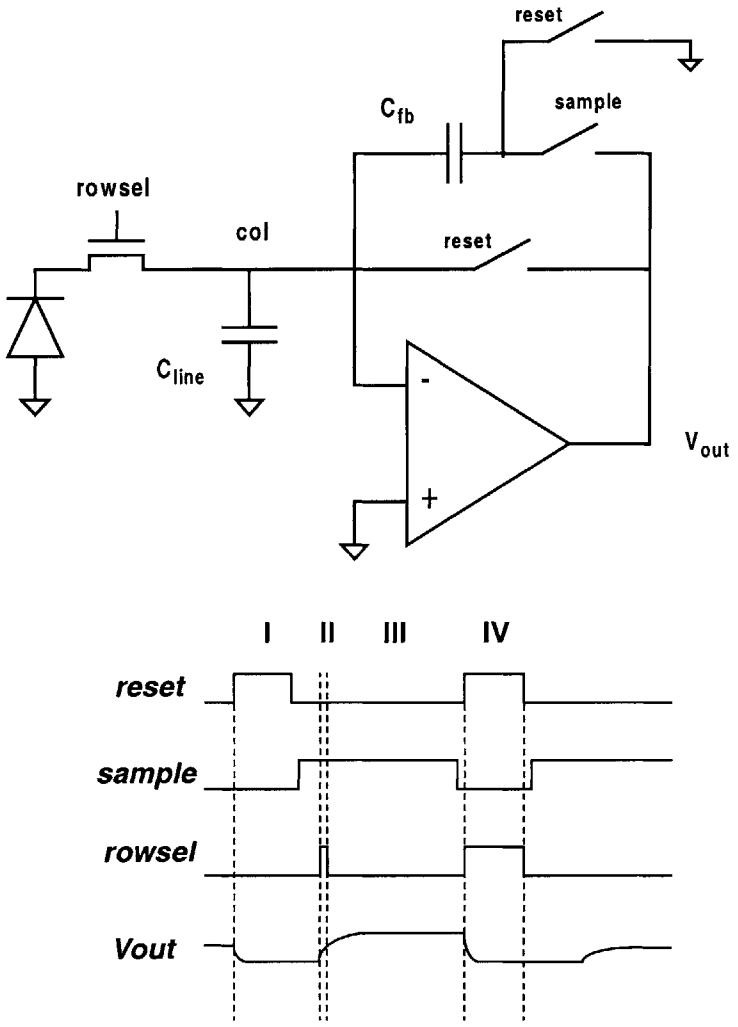


Figure 2-3: Single-Ended Passive Pixel Readout Circuit and Clock Phases.

pixel charge transfer (II), opamp settling (III), and pixel reset (IV).

2.4.1 Output circuit reset

During the output circuit reset phase, the opamp is in unity gain feedback and capacitors C_{fb} and C_{line} are reset (Fig. 2-4). The pixel, represented by a capacitor with a constant photocurrent I_{pix}, is integrating charge. The total charge in the system at the end of this phase is simply the integrated pixel charge, Q_{pix}.

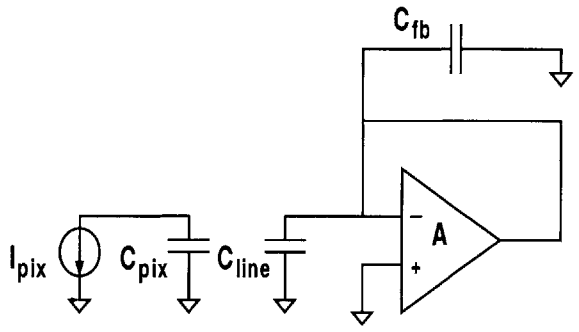


Figure 2-4: Output Circuit Reset Phase.

2.4.2 Pixel charge transfer

Since the pulse of the rowsel signal is much shorter than the settling time of the opamp, the opamp cannot react fast enough, and can be neglected during this phase (Fig. 2-5). When the row-select switch is closed, the pixel charge is shared between C_{pix}, C_{line} and C_{fb}. The total pixel charge transferred onto the output circuit is then:

$$Q_{trans} = Q_{pix} \cdot \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \tag{2.9}$$

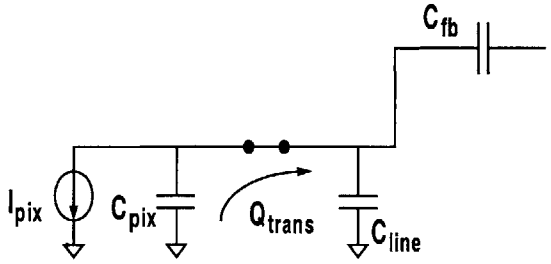


Figure 2-5: Pixel charge transfer.

2.4.3 Opamp settling

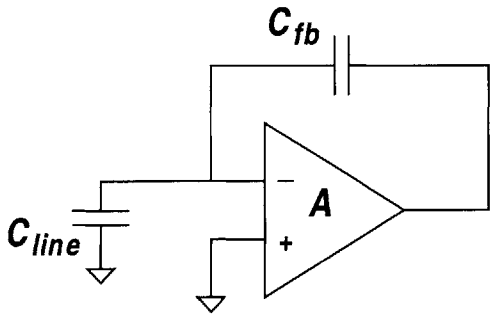


Figure 2-6: Opamp settling.

Once the row-select switch is open again, the pixel is isolated from the output circuit (Fig. 2-6). The charge on C_{line} from the previous phase changes the negative input voltage (v^-) slightly. Since this is a virtual ground node, the opamp will transfer all of the charge to the feedback capacitor in order to return to its reset voltage. When the opamp finishes settling, the output voltage is equal to the negative input voltage plus the voltage on C_{fb}.

$$V_{out} = v^- + \frac{Q_{trans}}{C_{fb}} \tag{2.10}$$

and

$$V_{out} = A(v^+ - v^-) \tag{2.11}$$

where A is the DC open-loop gain of the amplifier. Combining equations 2.9, 2.10 and 2.11, we have:

$$V_{out} = \frac{Q_{pix}}{C_{fb}} \cdot \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \cdot \frac{A}{A+1} \tag{2.12}$$

showing a linear relationship between the pixel charge and output voltage. Unlike the active pixel, where the pixel charge is converted to voltage through the voltage-dependent pixel capacitance, the charge-to-voltage conversion in the passive pixel is accomplished with the poly-to-poly capacitor C_{fb} and is therefore independent of the signal level.

Note that there are two additional factors in equation 2.12 which can attenuate the

signal and introduce fixed pattern noise. The first term, $\frac{C_{line}+C_{fb}}{C_{line}+C_{fb}+C_{pix}}$, is due to the charge sharing between C_{pix}, C_{line} and C_{fb}. Figure 2-7 shows the pixel output for different values of C_{pix}. For the case where $C_{pix} = C_{line} + C_{fb}$, only 50% of the signal is transferred from the pixel to the output circuit. As C_{pix} becomes smaller than $C_{line} + C_{fb}$, however, a larger portion of the pixel charge is transferred onto the feedback capacitor. For the case where $C_{pix} = 0.01(C_{line} + C_{fb})$, the transferred charge is 99% of the pixel charge. The capacitor ratio will depend heavily on process and layout.

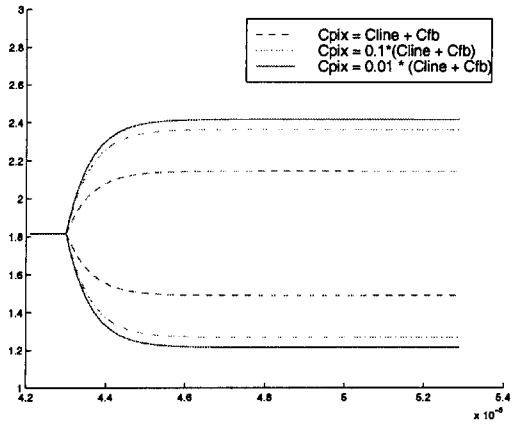


Figure 2-7: Pixel output for different ratios of $\frac{C_{line}+C_{fb}}{C_{line}+C_{fb}+C_{pix}}$.

The second term, $\frac{A}{A+1}$, depends on the open-loop gain of the amplifier. Naturally, a high value of A minimizes the attenuation and mismatch between columns. For a gain of 10,000, this factor is 0.9999. Ideally, this gain would be infinite, but for a realistic system, the gain should be kept as high as the technology will allow. Section 4.7.2 discusses the effects of mismatches in these terms on the fixed-pattern noise of the imager.

A useful term in the imaging world is the conversion gain, or total voltage per electron collected. The conversion gain for the passive pixel is simply:

$$CG = \frac{q}{C_{fb}} \cdot \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \cdot \frac{A}{A+1} \qquad [V/e^-] \tag{2.13}$$

2.4.4 Pixel reset

The fact that the charge transfer is not 100% efficient indicates that the fraction of the pixel charge not transferred onto the output circuit remains in the pixel. Instead of resetting the

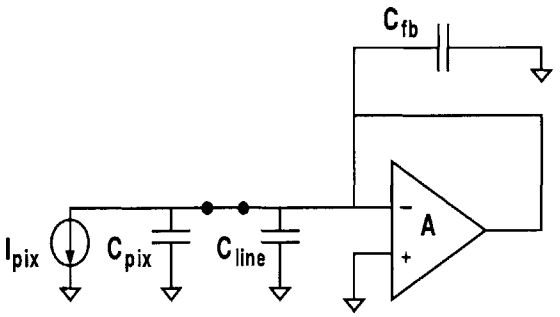


Figure 2-8: Active reset to prevent image lag.

pixel charge to zero, the pixel reset charge is:

$$Q_{reset} = Q_{pix}(T^-) \cdot \frac{C_{pix}}{C_{pix} + C_{line} + C_{fb}} \tag{2.14}$$

where $Q_{pix}(T^-)$ is the pixel charge from the previous frame.

For video images, if there is a bright-to-dark transition in the image, a significant amount of charge will be left in the pixel and image lag will be visible. A simple way to avoid this problem altogether is to reset the pixel actively as shown in figure 2-8. Since the opamp is in the unity-gain configuration, the pixel will be reset to the common mode voltage of the amplifier.

2.4.5 Offset voltage cancelling

The opamp offset voltage, due to mismatches in the device sizes, is a non-ideality that is cancelled by the reset and readout method. The non-ideal opamp can be modeled by an ideal opamp with a source containing the offset voltage, v_{os}. Figures 2-9 and 2-10 illustrate this model during the reset and sample phases respectively.

During the reset phase, the offset voltage is stored on C_{line} and C_{fb}, and the charge on these capacitors can be expressed as:

$$Q_{C_{line}}(reset) = C_{line} \cdot v_{os} \tag{2.15}$$

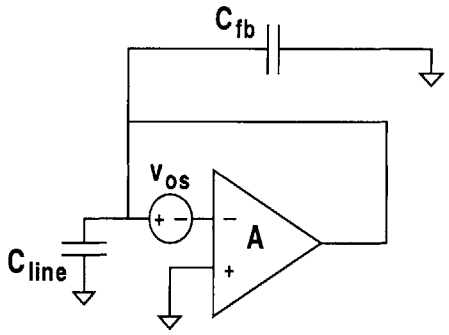


Figure 2-9: Reset phase with opamp offset voltage.

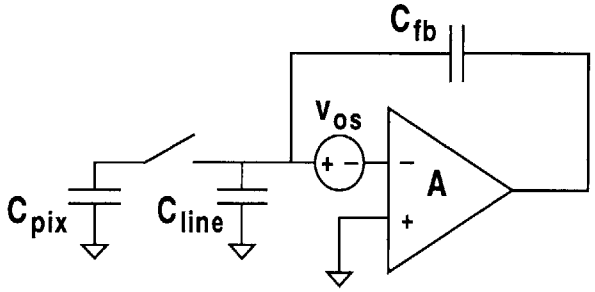


Figure 2-10: Sample phase with opamp offset voltage.

$$Q_{C_{fb}}(reset) = C_{fb} \cdot v_{os} \tag{2.16}$$

The negative and positive inputs can be considered equal since we are dealing with an ideal opamp. The charge on C_{line} during the sample phase remains the same as during the reset phase. The feedback capacitor holds the charge due to the offset in addition to the transferred pixel charge:

$$Q_{C_{line}}(sample) = C_{line} \cdot v_{os} \tag{2.17}$$

$$Q_{C_{fb}}(sample) = C_{fb} \cdot v_{os} + Q_{trans} \tag{2.18}$$

Since the charge on C_{line} does not change between the reset and sample phases, none of the offset voltage is transferred to C_{fb}. Furthermore, the offset voltage on C_{fb} cancels the opamp offset voltage, leading to an output completely free of any offset voltage.

$$V_{out} = \frac{Q_{pix}}{C_{fb}} \cdot \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \cdot \frac{A}{A+1} \tag{2.19}$$

2.5 Imager Performance

The performance of an imager can be measured by its responsivity, or the output voltage for a given light intensity over an integration period, often given in terms of Volts per lux per second. This term is often used because it combines many of the parameters described in previous sections, namely the pixel fill factor, pixel size and quantum efficiency. In some cases, the conversion gain and any amplification or attenuation factors in the signal path are also included in the responsivity.

Fig. 2-11 shows a responsivity plot illustrating the relationship between the number of signal and noise electrons collected at the pixel for varying illuminations levels [21]. The output signal increases linearly with illumination until it reaches a saturation level. The photonic shot noise, which arises from the probabilistic process of carrier generation, is proportional to the square root of the signal level. The noise floor determines the minimum signal that can be detected. The intersection of the noise floor and responsivity curves is known as the sensitivity of the imager.

This plot helps us understand how the signal-to-noise ratio (SNR) varies with illumination. For low levels of illumination, the noise floor dominates and the SNR is simply $\frac{signal}{noisefloor}$. As the illumination increases, the photonic shot noise becomes the dominant noise source and the SNR is given by $\sqrt{signal}$.

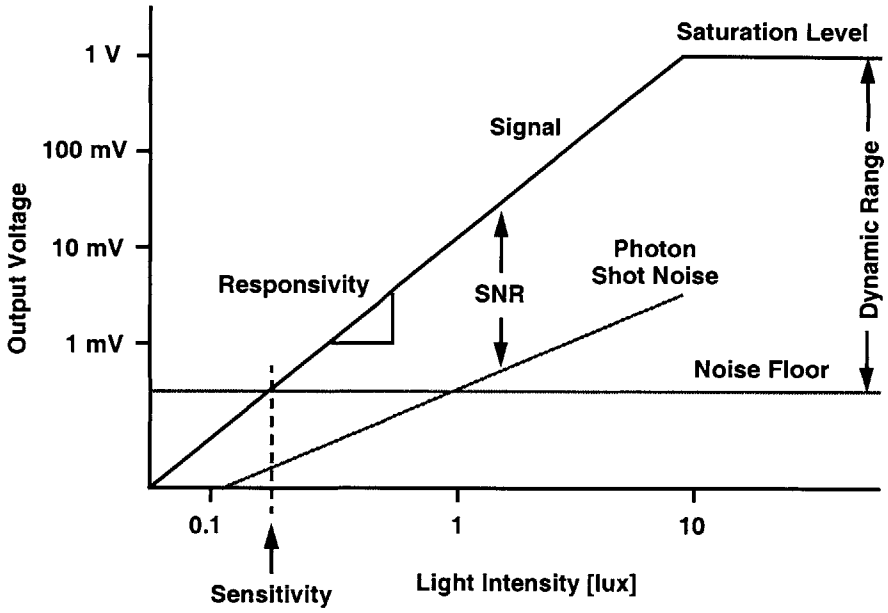


Figure 2-11: Pixel signal and noise sources over varying light intensity.

2.6 Pixel Structure

2.6.1 Photodiode Implementation

A standard CMOS process on p-type substrate provides three different possibilities for photodiodes:

- N-diffusion-to-P-substrate photodiode (fig 2-12) consists of the same heavily-doped n-type material used as the source/drain region of a standard MOSFET. Its high doping concentration and shallow junction result in low quantum efficiency for blue light [22]. In silicided processes, opaque silicide deposited on the N-diffusion regions further degrades the quantum efficiency over the entire spectrum.

- N-well-to-P-substrate photodiode (fig 2-13) has been proven to have superior quantum efficiency and lower dark current than its N-diffusion counterpart and it is not affected by silicide. More strict design rules apply for this photodiode since the N-well has the tendency to expand during processing. N-well-to-N-well spacing and minimum N-well

geometry rules limit the minimum pixel size and fill factor.

- P-diffusion to N-well (fig 2-14) collects holes rather than electrons. This photodiode has the drawbacks of the two structures previously discussed. It has the high doping concentration and shallow junction of the N-diffusion photodiode and the bulkiness of the N-well, limiting its quantum efficiency, pixel size and fill factor.

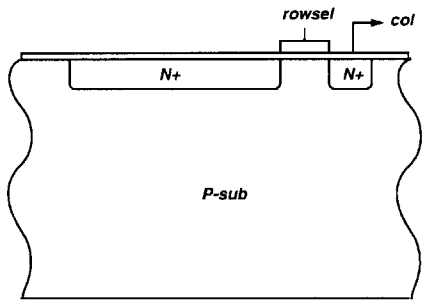


Figure 2-12: Passive Pixel Cross Section with N-diffusion to P-substrate photodiode.

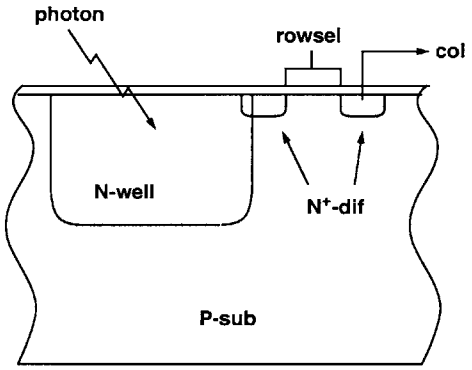


Figure 2-13: Passive Pixel Cross Section with N-well to P-substrate photodiode.

2.6.2 Pixel Capacitance

In designing a passive pixel, it is particularly important to calculate the pixel capacitance. The pixel capacitance tells how much voltage change the photodiode will see for each collected electron. This value will also be used to determine the feedback capacitance and

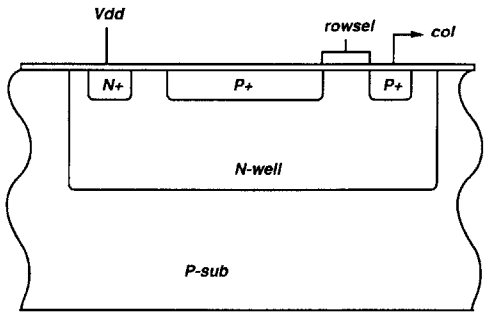


Figure 2-14: Passive Pixel Cross Section with P-diffusion to N-well photodiode.

consequently the required bandwidth of the amplifier.

The pixel capacitance can be calculated from the junction capacitance, C_j, and sidewall capacitance, C_{jsw}, of the photodiode and the gate-to-drain capacitance of the row-select transistor, C_{gd}.

$$C_{pix} = C_j A_{pd} + C_{jsw} P_{pd} + C_{gd} \tag{2.20}$$

where A_{pd} and P_{pd} are the area and perimeter of the photodiode, respectively. For large geometry pixels, C_j dominates, but as the pixel becomes smaller, C_{jsw} and C_{gd} begin to have a bigger effect.

The junction capacitance, in units of Farads per unit area, is determined by the doping profile of the material and the reverse bias of the junction.

$$C_j = \sqrt{\frac{q\epsilon}{2(\phi_{bi} - V_D)\frac{N_A + N_D}{N_A N_D}}} \tag{2.21}$$

where ϵ is the permittivity of Silicon, ϕ_{bi} is the built-in potential of the junction, and V_D is the reverse-bias voltage of the photodiode.

C_{jsw}, is the junction capacitance of the sidewall of the photodiode. It has the same form of C_j, but it is calculated separately because the doping profile ($N_A(x)$ and $N_D(x)$) along the sidewall is different from the bottom lateral junction. Furthermore, the units of C_{jsw} are usually given in terms of Farads per unit length since this term is integrated over the depth of the junction, x_j.

$$C_{jsw} = \int_0^{x_j} \sqrt{\frac{q\epsilon}{2(\phi_{bi} - V_D)\frac{N_A(x)+N_D(x)}{N_A(x)N_D(x)}}}\, dx \tag{2.22}$$

The gate-to-drain capacitance is the result of the overlap capacitance and fringing fields between the gate and the drain diffusion underneath.

$$C_{gd} = WC_{gdo} \tag{2.23}$$

where W is the width of the row select device, and C_{gdo} is the gate-to-drain capacitance per unit length.

$$\begin{aligned} C_{pix} =& A_{pd}\sqrt{\frac{q\epsilon}{2(\phi_{bi} - V_D)\frac{N_A+N_D}{N_A N_D}}} \\ &+ P_{pd}\int_0^{x_j} \sqrt{\frac{q\epsilon}{2(\phi_{bi} - V_D)\frac{N_A(x)+N_D(x)}{N_A(x)N_D(x)}}}\, dx \\ &+ WC_{gdo} \end{aligned} \tag{2.24}$$

The pixel capacitance is generally set by the choice of photodiode (N-well vs. N-diff), choice of pixel (active vs. passive), fill factor and pixel area. The N-diffusion photodiode has a larger capacitance than the N-well photodiode due to its higher doping concentration. The passive pixel has a larger capacitance than the active pixel due to its higher fill factor. A larger pixel area obviously increases the charge capacity.

The change in pixel voltage during an integration period is limited to the pixel reset voltage, V_{pixrst}.

$$\Delta V_{pix} = \frac{Q_{pix}}{C_{pix}} < V_{pixrst} \tag{2.25}$$

V_{pixrst} is usually the common-mode voltage of the amplifier, or half of the power supply voltage.

2.6.3 Parasitic Column Line Capacitance

Looking back at figure 2-1, we see that each column line is connected to the drain of the row-select transistors of all the pixels on the column. The capacitance of each drain

region consists of a gate-to-drain capacitance, C_{gd}, and a drain-to-bulk capacitance, C_{db}. In addition to the row-select transistor parasitic capacitance, there is a metal-to-substrate capacitance, C_{met}.

The line capacitance can thus be calculated with the following formula:

$$C_{line} = m \cdot [C_{db} + C_{gd} + C_{met}] \tag{2.26}$$

where m is the number of rows in the array. The first two terms typically dominate the value of C_{line}.

Equation 2.19 suggests that a high value of C_{line}, with respect to C_{pix}, improves the output signal. This improvement is the only positive side to a large C_{line}. As explained in subsequent sections, this parasitic capacitance limits the scaling of the number of rows per column, or vertical resolution, in a passive pixel imager. Section 2.7.2 will show the square relationship between bandwidth and number of rows, m. Additionally, Chapter 4 will cover in detail the detrimental effects of C_{line} on the output noise.

2.6.4 Feedback Capacitance

Assuming perfect charge transfer from the pixel to the feedback capacitor, C_{fb}, the charge storage capacity of C_{pix} and C_{fb} must be similarly matched:

$$Q_{pix,max} = Q_{fb,max} \tag{2.27}$$

$$C_{pix} \cdot V_{pixrst} = C_{fb} \cdot V_{sw} \tag{2.28}$$

where V_{sw} is the maximum voltage swing at the output of the amplifier.

The feedback capacitance is then directly proportional to the pixel capacitance, and must therefore be scaled appropriately:

$$C_{fb} = \frac{C_{pix} V_{pixrst}}{V_{sw}} \tag{2.29}$$

The value of the feedback capacitance, C_{fb}, is very important since it determines the conversion gain of the imager. The conversion gain, or output voltage per collected electron, can be simplified from Eq. 2.13 under the assumption that $C_{line} + C_{fb} >> C_{pix}$ and $A >> 1$:

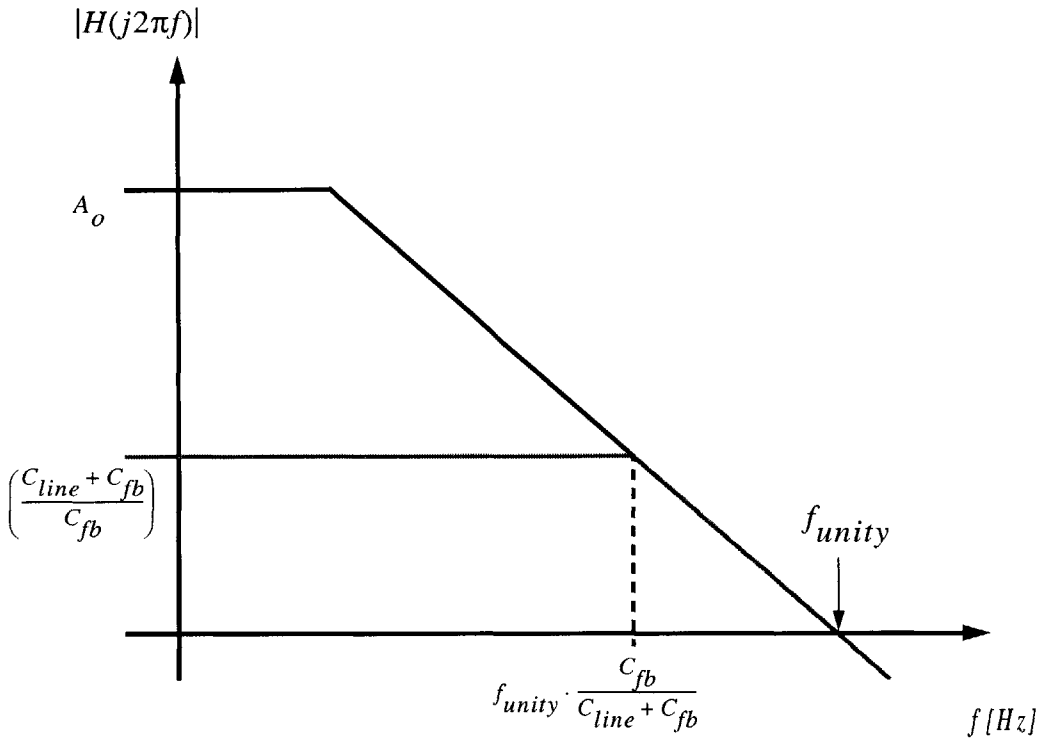


Figure 2-15: Opamp transfer function.

$$CG = \frac{q}{C_{fb}} \qquad [V/e^-] \tag{2.30}$$

2.7 Amplifier Specifications

In order to meet the specified frame rate for a particular spatial resolution, we must ensure that the opamp has enough open loop gain, bandwidth and output voltage swing.

2.7.1 DC Gain

The black line in figure 2-15 shows the Bode plot of the transfer function of the opamp. At low frequency it has a gain of A_o and at higher frequencies, the gain decreases with a single-pole rolloff and becomes unity at the unity-gain frequency, f_{unity}. The gray line traverses the closed loop gain of the output circuit, $\frac{C_{line}+C_{fb}}{C_{fb}}$, and has a pole at $f_{unity} \cdot \frac{C_{fb}}{C_{fb}+C_{line}}$. In order to minimize the attenuation of the transferred charge (refer to Eq. 2.19), A_o should be kept as high as the technology will allow.

2.7.2 Bandwidth

The required unity gain bandwidth of the closed-loop system can be derived from the settling time. The setting time is simply:

$$T_{settle} < \frac{1}{2m \cdot F_{imager}} \tag{2.31}$$

where m is the number of rows per column and F_{imager} is the refresh rate of the imager. The factor of two is specific to the case where one opamp is shared between two columns. The settling time is now used to give us the time constant, τ:

$$T_{settle} = ln(2^a) \cdot \tau \tag{2.32}$$

$$\tau < \frac{1}{2m \cdot F_{imager} \cdot ln(2^a)} \tag{2.33}$$

for a-bit intensity resolution.

The time constant gives us the location of the first pole, f_{3db}:

$$f_{3db} > \frac{1}{2\pi\tau} = \frac{2m \cdot F_{imager} \cdot ln(2^a)}{2\pi} \tag{2.34}$$

The unity-gain frequency can now be determined by multiplying the first pole frequency by the closed-loop gain:

$$f_{unity} > \frac{F_{imager} \cdot m \cdot ln(2^a)}{\pi} \frac{C_{line} + C_{fb}}{C_{fb}} \tag{2.35}$$

Since C_{line} is proportional to the number of rows, m, the unity-gain frequency is actually proportional to the square of m.

2.7.3 Output Swing

The output swing of an amplifier is the maximum voltage range of the output. It is important to know its value a priori such that the maximum charge storage in C_{fb} will match that of C_{pix} as stated in section 2.6.4. The output swing should be maximized to the limit of the technology.

2.8 Passive vs. Active Pixels

2.8.1 Active Pixel Sensor

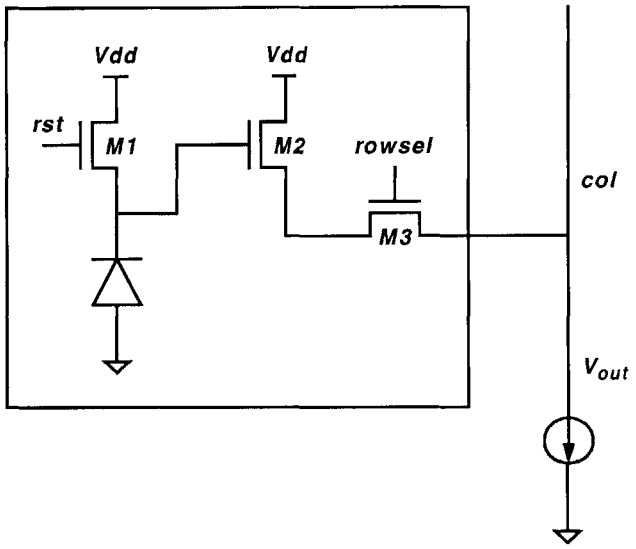


Figure 2-16: Active pixel sensor schematic.

The architecture of the active pixel sensor (APS) is similar to that of the passive pixel (Fig. 2-1). Rather than converting the charge-to-voltage at the bottom of the array, however, each pixel has its own amplifier or buffer. A schematic of an example active pixel is shown in Fig. 2-16. Three transistors and four signal lines (rst, rowsel, Vdd and col) are required for the simplest functionality. Transistor M1 resets the photodiode voltage to $V_{dd} - V_{T_{M1}}$ where $V_{T_{M1}}$ is the threshold voltage of device M1. As light shines on the sensor, the photodiode voltage will decrease depending on the light intensity:

$$V_{pd} = V_{dd} - V_{T_{M1}} - \frac{Q_{pix}}{C_{pd} + C_{gd_{M2}}} \tag{2.36}$$

The relationship between the photodiode voltage and pixel output voltage will be:

$$V_{out} = V_{pd} \cdot \frac{g_m}{g_m + g_{mb}} - V_{T_{M2}} - \sqrt{\frac{2I_D}{(\frac{W}{L})_{M2}\mu_n C_{ox}}} \tag{2.37}$$

Combining Eqns. 2.36 and 2.37, we get:

$$V_{out} = \left(V_{dd} - V_{T_{M1}} - \frac{Q_{pix}}{C_{pd} + C_{gd_{M2}}}\right)\left(\frac{g_m}{g_m + g_{mb}}\right)_{M2} - V_{T_{M2}}(V_{out}) - \sqrt{\frac{2I_{out}}{\left(\frac{W}{L}\right)_{M2}\mu_n C_{ox}}} \tag{2.38}$$

The first term is the photodiode voltage multiplied by the gain of the source follower, $\frac{g_m}{g_m+g_{mb}}$. Since the source cannot be tied to the bulk in an N-well process, the back-gate effect lowers the gain. The second term comes from the offset of the source follower. The threshold voltage of M2 is also affected by the back-gate effect and will be a function of the source-to-bulk voltage, or V_{out} in this case.

2.8.2 Passive Pixel Advantages

There are three main advantages for using a passive pixel:

1. Larger fill factor - Due to the simplicity of the passive pixel, it can be layed out in a small area, yet leaving enough photodiode area for light sensing. The result is a large ratio of photodiode-to-total pixel area, also known as fill factor. Figures 2-17 and 2-18 show the layouts of a passive and active pixels respectively. The white area is the photodiode and the gray lines represent metal interconnect.

   For a given area, it is obvious that the passive pixel has a higher fill factor. This trend becomes more visible in small pixel geometries. Fill factors as high as 80% have been reported for passive pixels [12], compared with 30% for active pixels of similar geometry and technology.

2. Lower pixel-to-pixel fixed pattern noise (pixel FPN) - Any mismatches in pixel geometry, dark current, and device characteristics will lead to pixel FPN. Both, active and passive pixels are vulnerable to mismatches in geometry and dark current. Depending on the dominant source of mismatch, the passive pixel may have better pixel FPN performance than the active pixel since its output does not rely on perfectly matched threshold voltages and device geometry. Correlated Double-Sampling techniques can be used to remove FPN in both, active and passive pixels.

3. Linear transfer function - The charge-to-voltage conversion in a passive pixel is achieved

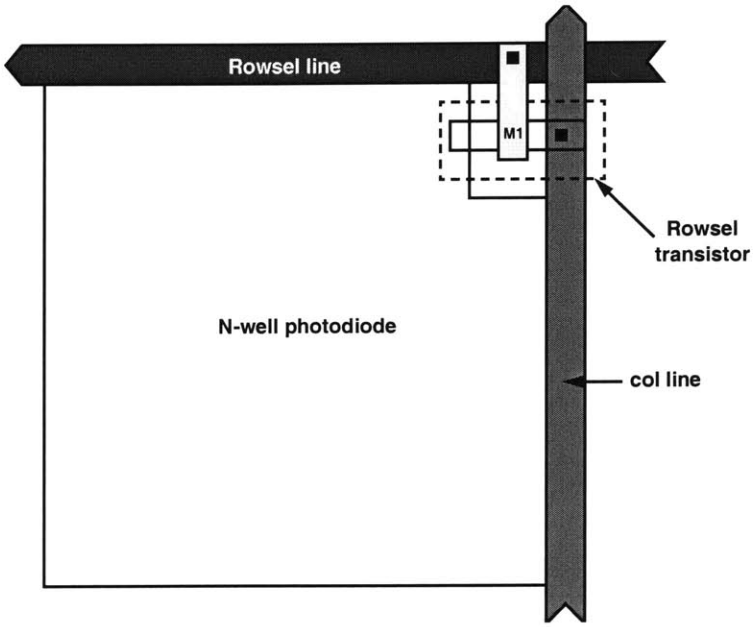


Figure 2-17: Layout of passive pixel with N-well to P-substrate photodiode.

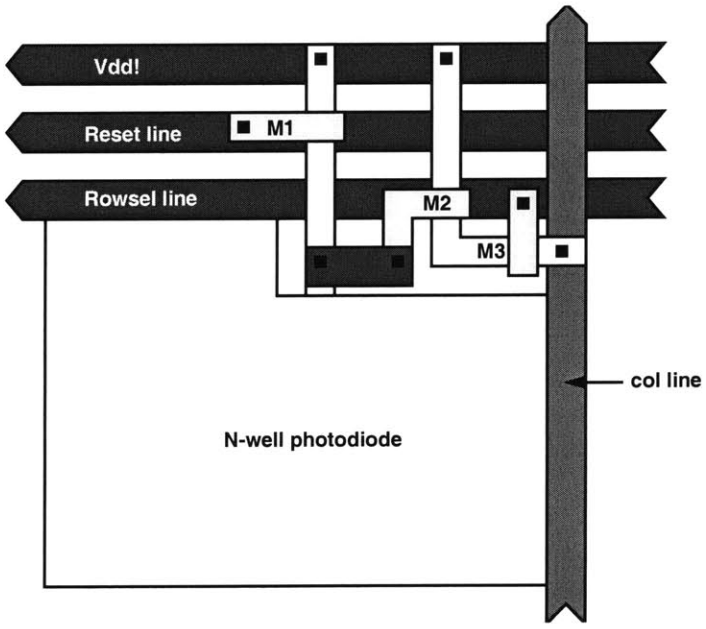


Figure 2-18: Layout of active pixel with N-well to P-substrate photodiode.

via a voltage-independent (poly-to-poly) feedback capacitor, C_{fb}, leading to a linear transfer function. In contrast with the passive pixel, the active pixel makes use of the signal-dependent photodiode capacitance for its charge to voltage conversion. As a

result, the active pixel has a non-linear transfer function.

Chapter 3

Parasitic Current

The passive pixel has been plagued by a signal-dependent parasitic current at each column line. The effects of this current are catastrophic to the output signal as a few bright pixels on the column line can contaminate the output of all pixels on the same column, leading to bright vertical streaks on the image. This chapter identifies three sources of this parasitic current: optically-generated carrier diffusion, blooming and subthreshold current. A test chip shows the effects of the parasitic current are detrimental to the imager. A solution at the architecture and circuit level is explained and the efficiency of the circuits is quantitatively demonstrated with fixed-pattern noise (FPN) measurements. A sample image illustrates the effects of the parasitic current are no longer visible.

3.1 Sources of parasitic current

The passive pixel is sensitive to disturbances on the column line because its output is in the form of charge. There are three main sources of parasitic currents contaminating the charge signal [13]. The first one is a signal-dependent current caused by diffused optically-generated carriers in the substrate. The second one, also known as blooming, occurs when high illumination causes the photodiode to substrate junction to become forward-biased, activating a parasitic bipolar junction transistor (BJT). The last source of parasitic current is due to subthreshold currents in the row-select transistor when the photodiode voltage goes below $0V$ during events of high illumination. These parasitic currents, which are also present in active pixels, are catastrophic for passive pixels because the column line is a high impedance node.

3.1.1 Optically-generated carrier diffusion

A signal-dependent parasitic current is caused by optically-generated electrons in the substrate which diffuse to the reverse-biased junction of the column line (see Fig. 3-1). During the sample phase, the column line collects the parasitic charge from all pixels connected to the column line, in addition to the integrated charge from the selected pixel.

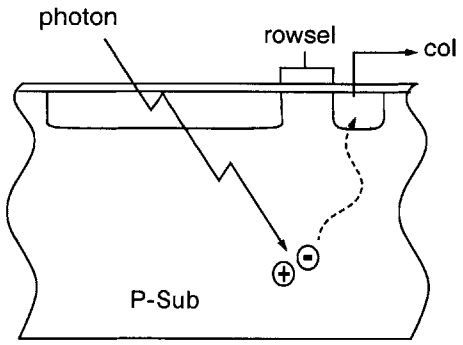


Figure 3-1: Optically-generated electrons diffuse to column line.

3.1.2 Blooming

Blooming occurs during an event of high illumination, when a photodiode saturates and its voltage drops below $0V$. At this point, photocurrent will leak from the column line to the photodiode through a parasitic lateral NPN BJT, as illustrated in Fig. 3-2. Photogenerated electrons will be injected into the substrate where they will diffuse to the reverse-bias junction of the column line.

3.1.3 Subthreshold current

A second leakage path during high illumination exists through the subthreshold current of the row-select transistor. Increases in V_{gs} of this transistor, due to a negative voltage on the photodiode, will result in exponential increases in the subthreshold current. Fig. 3-3 illustrates this mechanism.

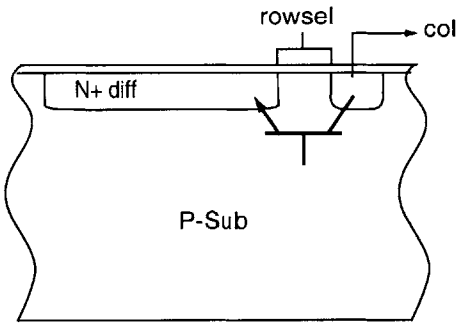


Figure 3-2: Blooming mechanism.

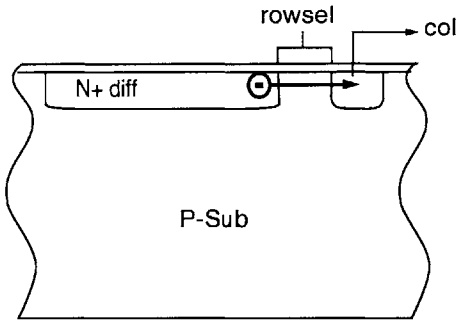


Figure 3-3: Subthreshold conduction currents.

3.2 Effects of parasitic current

The combined effects of the parasitic current described above will add a second term to the output voltage expression shown in Eq. 2.19:

$$V_{out} = \left[Q_{pix} + \sum_{i=1}^{m} I_{p_i} \cdot T_{sample} \right] \cdot \frac{1}{C_{fb}} \tag{3.1}$$

assuming $C_{line} + C_{fb} >> C_{pix}$, infinite open loop gain, and zero offset voltage. I_{p_i} is the parasitic current of pixel i, m is the number of pixels on the column line and T_{sample} is the pixel sample time, as illustrated in Fig. 2-3. The pixel output now depends on the parasitic current of all other pixels on the column line, creating cross-talk between pixels far away in the array.

The parasitic current expression of each pixel depends on the pixel charge, Q_{pix}:

$$I_{p_i} = I_{dif_i} \qquad Q_{pix} < C_{pix} \cdot V_{cm} \tag{3.2}$$

$$I_{p_i} = I_{dif_i} + I_{bloom_i} + I_{sub_i} \qquad Q_{pix} > C_{pix} \cdot V_{cm} \tag{3.3}$$

where $C_{pix} \cdot V_{cm}$ is the maximum charge storage in a pixel, I_{dif_i} is the diffused carrier parasitic current, I_{bloom} is the blooming current and I_{sub_i} is the subthreshold current. In other words, the parasitic current of a particular pixel consists of the diffused carrier current if the pixel is not yet saturated (Eq. 3.2). Once a pixel is saturated, its parasitic current will also have the blooming and subthreshold current terms (Eq. 3.3).

3.2.1 Implementation of Test Chip

A test chip was fabricated in a CMOS $0.8\mu m$ process to observe the effects of the parasitic current. An array of 256 rows by 4 columns was implemented in the column-parallel differential architecture depicted by figure 3-4. A single row is made up of an even row and an odd row. The differential readout requires that an even row of pixels be read out with an odd row of dummy cells, and viceversa. In order to prevent even and odd rows from crossing, the pixel layout was interlaced.

At the end of an integration period, a row of pixels is selected for readout along with a row of "dummy" (dark) cells. After the rowsel signal is pulsed high, the pixel charge is transferred to its respective feedback capacitor and the voltage due to the difference between the sensing and dummy columns appears at the output of each amplifier.

The column parallel architecture is essential for passive pixels. Had a single opamp been used as the output circuit, we would be challenged with the situation described in figure 3-5. When the rowsel signal is pulsed high, the charge from each pixel is transferred onto its respective column line. The charge on each column line is then exposed to the parasitic current until it is selected for readout by the multiplexer. The last column to be selected (col 256 per se) will then integrate a much higher amount of parasitic charge than the first column (col 1). A gradient will be visible in the image and depending on the light intensity, a number of columns will certainly saturate before the signal can be read out.

A differential amplifier was chosen over a single-ended one to reject any common mode

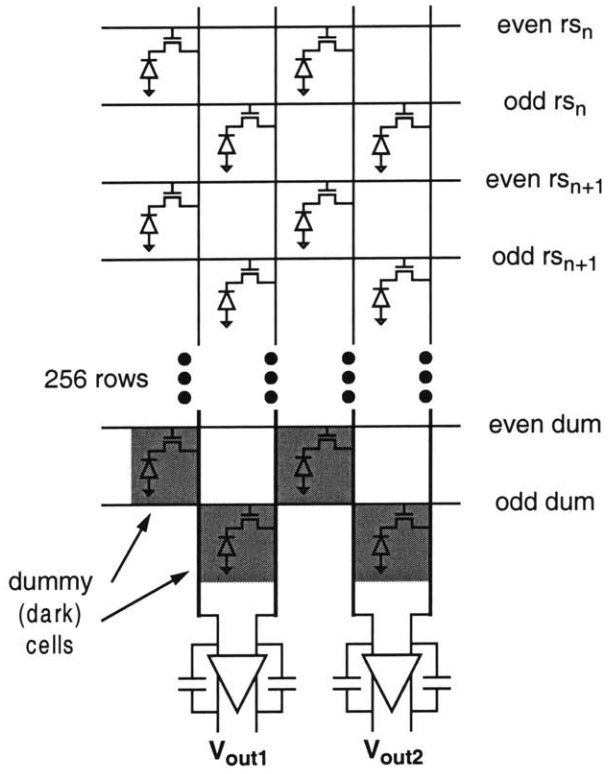


Figure 3-4: Column-parallel differential passive pixel architecture for test chip.

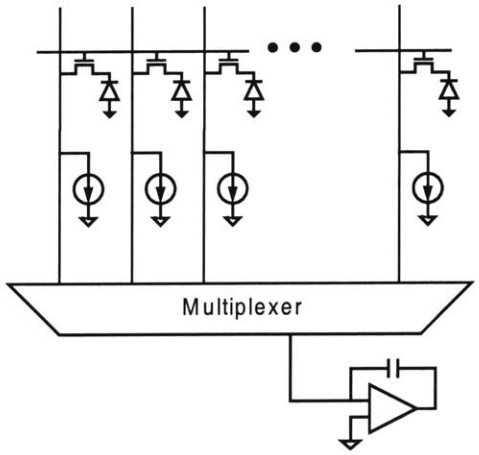


Figure 3-5: Parasitic current effects on column 256 much higher than those of column 1 with single opamp readout.

disturbances. Since the differential amplifier only detects the difference in charge between the inputs, the parasitic current that is common between two columns would not appear at the output. It was then necessary to introduce a mismatch in the layout of the columns in order to accentuate the effects of the parasitic current.

The layout illustrated in figure 3-6 introduces a mismatch between column 1 and column 2. Column 2 is surrounded by pixels on the left and right. Column 1, however, only has pixels on its right and a metal shielded guard rail to its left. We therefore expect a higher parasitic current on column 2 than on column 1. The difference in light environments gives rise to a parasitic current difference.

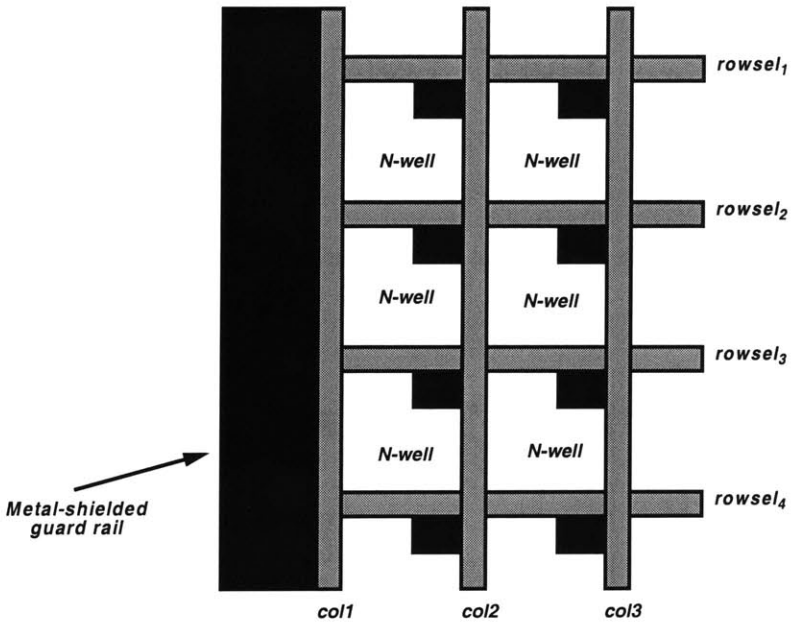


Figure 3-6: Layout mismatch of differential architecture to accentuate effects of parasitic current.

Columns in the middle of the array will not contain these layout mismatches. It should be noted, however, that differences in parasitic current can be expected when the columns are exposed to different levels of illumination.

3.2.2 Test Chip Results

The output voltage between columns 1 and 2 is expected to have the form:

$$V_{out} = \frac{1}{C_{fb}} \cdot \left[I_{pix} T_{int} + \Delta \sum_{i=1}^{256} I_p \cdot T_{sample} \right] \tag{3.4}$$

where

$$\Delta \sum_{i=1}^{256} I_p = \sum_{i=1}^{256} I_{p1} - \sum_{i=1}^{256} I_{p2} \tag{3.5}$$

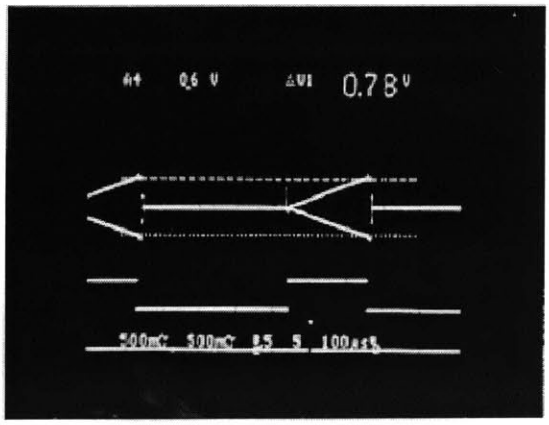
The first term in Eq. 3.4 is due to pixel charge and the second term is due to parasitic charge. Q_{pix} has been replaced by the product of the pixel current, I_{pix}, and integration time, T_{int}.

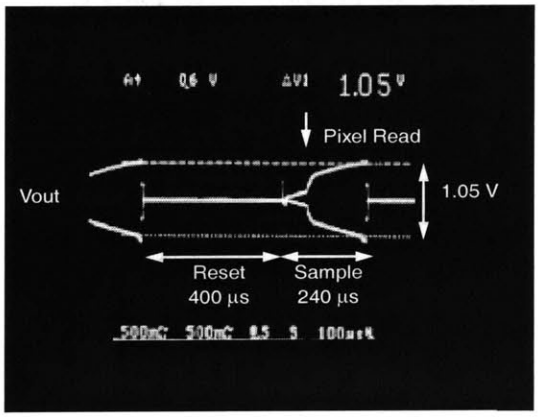
In order to appreciate the magnitude of the parasitic current, the integration time for both signal and parasitic current were maintained on the same scale. The array was subjected to uniform illumination, and the intensity was regulated such that all pixels were operating in their linear region (i.e. no saturated pixels).

Fig. 3-7 shows the output voltage with $T_{int} = 640\mu s$ and $T_{sample} = 240\mu s$ for three different scenarios. In the first one, no pixels are selected for readout. The outputs are flat during the reset phase, but diverge during the entire sample phase, indicating the presence of the parasitic current. When a pixel from column 2 and a dummy cell from column 1 are selected for readout, we get the scenario shown in the second figure. The outputs are flat during the reset phase, but begin to diverge at the beginning of the sample phase. The pixel charge is then superimposed on the parasitic current. The outputs then continue to diverge until the end of the sample phase. The last figure shows the output voltage when a pixel on column 1 and a dummy cell on column 2 are selected. The pixel charge on column 1 works against the parasitic charge on column 2 and the output switches directions during the pixel readout. The outputs then continue to diverge in the original direction.

Since blooming and subthreshold current effects are well understood, the test chip was designed such that only the effects of carrier diffusion would be represented in the experiments. The light intensity was therefore kept under the saturation level to ensure these two mechanisms would not be triggered.

As illustrated by Fig. 3-7, the effects of the carrier diffusion alone will be severe on the





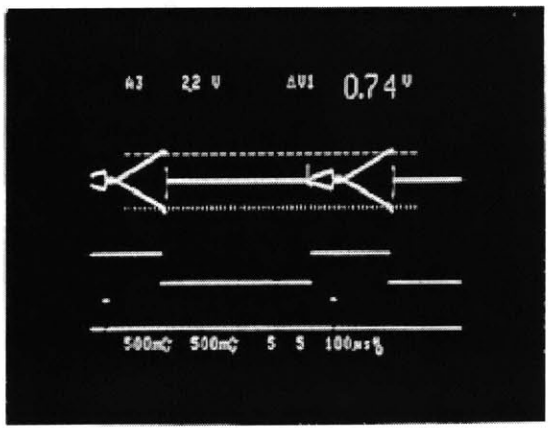


Figure 3-7: Effects of diffused carriers on pixel output with no pixels selected, pixel on column 2 selected and pixel on column 1 selected.

image since the parasitic charge of a bright pixel in one section of the array can contaminate the output of dark pixels in other rows in the column line. Bright vertical streaks will be the result of a couple of bright pixels on the column line. Furthermore, the dynamic range of the imager will be limited by the constant discharge of the parasitic charge on the amplifier inputs.

3.3 Removal of parasitic current

While anti-blooming techniques have been widely used for passive pixels in the past [18], [23], the diffused carrier parasitic current has been overlooked as part of the inherent signal degradation of passive pixels. In this work, two strategies are used to remove the effects of all three elements of the parasitic current [24]. The first is at the architectural level where the differential readout between a pixel and a dummy cell rejects the parasitic current that is common between the two columns. In large arrays, this factor is the most significant since neighboring columns are exposed to similar illumination levels. The second part consists of removing effects due to mismatch between neighboring columns by utilizing a correlated double sampling circuit.

3.3.1 Architecture level

Fig. 3-8 shows the column-parallel architecture with differential pixel readout used to remove the parasitic current common between two columns. The architecture is similar to that shown in Fig. 3-4. In order to scale to a full-size 256X256 array, a row decoder and multiplexer were added. Needless to say, rather than introducing mismatches in the layout, special care was taken to minimize them.

3.3.2 Circuit level

A Correlated-Double Sampling (CDS) circuit illustrated in Fig. 3-9, was used to remove the effects of the parasitic current due to mismatches between neighboring columns. The parasitic current is modeled as a constant current source at the column line node. I_{p1} represents the parasitic current on column 1 while I_{p2} is the parasitic current on column 2. The pixel is shown as a photodiode and the dummy cell is depicted by a photodiode in a shaded box.

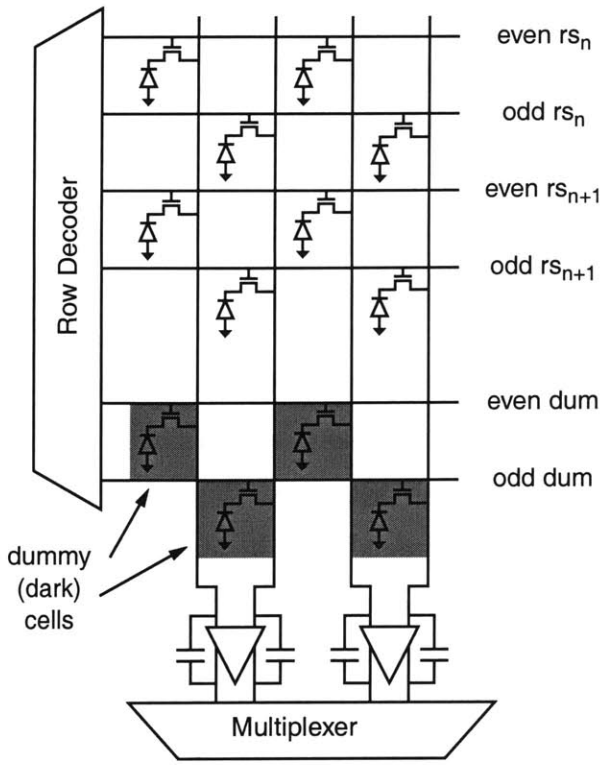


Figure 3-8: Differential Passive Pixel Architecture.

The operation of the CDS is divided into four phases:

1. Phase 1 - All CDS components are reset. The opamp is in unity gain, and capacitors C_{line1} and C_{line2} are reset to the common mode voltage of the amplifier, V_{cm}. The charge in feedback capacitors C_{fb1} and C_{fb2} is reset to zero. Meanwhile, the pixel integrates optically-generated charge.

2. Phase 2 - This is the sample phase where the feedback capacitors integrate charge from the parasitic current as well as the pixel and dummy signals. At the end of phase 2, the total charge stored in the feedback capacitors is then:

$$Q_{C_{fb1}} = Q_{pix} + Q_{p1}(\phi_2) \tag{3.6}$$

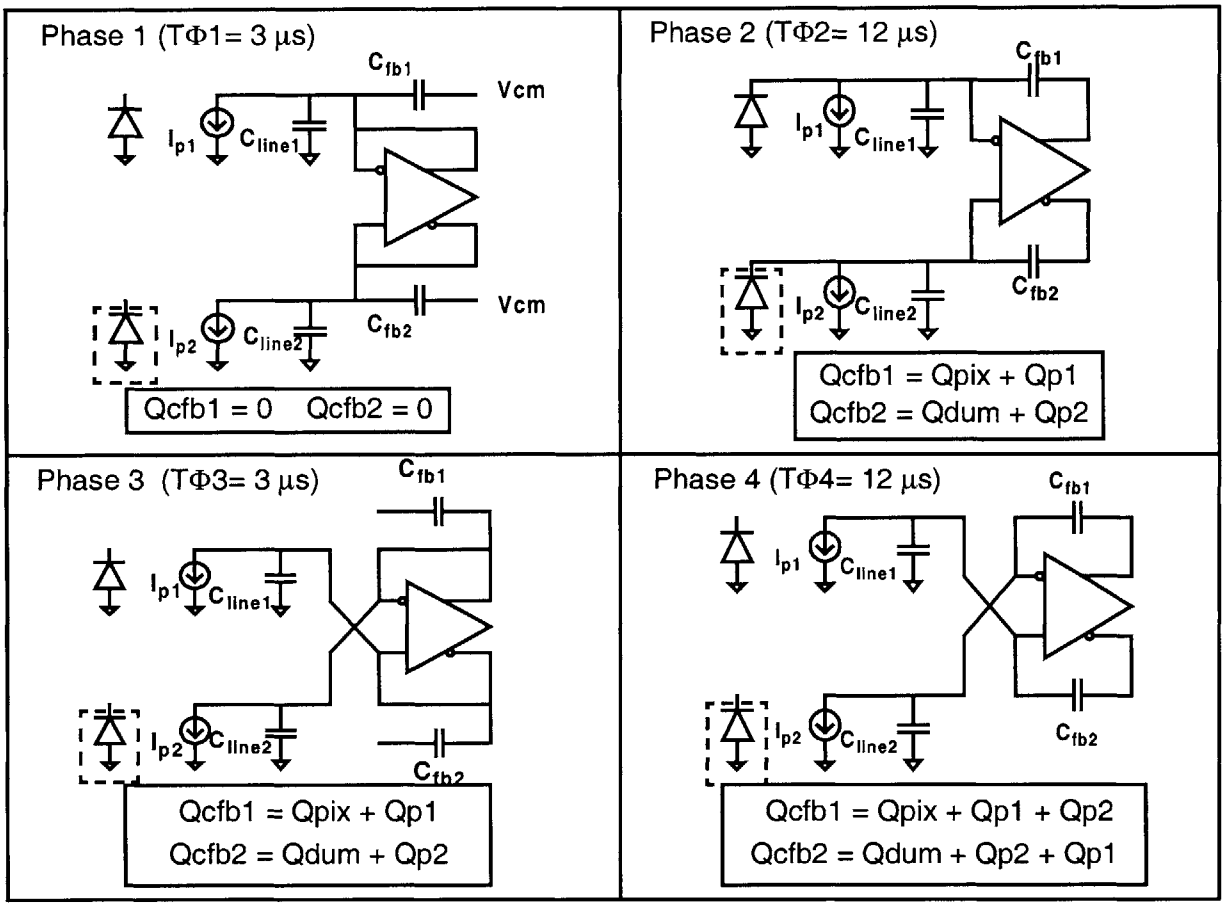


Figure 3-9: Correlated Double Sampling Circuit.

$$Q_{C_{fb2}} = Q_{dum} + Q_{p2}(\phi_2) \tag{3.7}$$

where $Q_{p1}(\phi_2)$ and $Q_{p2}(\phi_2)$ stand for the charge due to parasitic currents I_{p1} and I_{p2} during phase 2 respectively.

3. Phase 3 - During this second reset phase, the column lines are switched and the opamp is in unity-gain feedback. The feedback capacitors hold the charge from the previous phase. While this phase is not necessary to achieve the correlated double sampling, it is essential in minimizing the effects of the opamp offset voltage, as explained in section 2.4.5. At the end of this phase, the charge in the feedback capacitors remains unchanged:

$$Q_{C_{fb1}} = Q_{pix} + Q_{p1}(\phi_2) \tag{3.8}$$

$$Q_{C_{fb2}} = Q_{dum} + Q_{p2}(\phi_2) \tag{3.9}$$

4. Phase 4 - This is the second sample phase and has the same duration as phase 2. The feedback capacitors integrate the parasitic current only. The final charge in the capacitors is then:

$$Q_{C_{fb1}} = Q_{pix} + Q_{p1}(\phi_2) + Q_{p2}(\phi_4) \tag{3.10}$$

$$Q_{C_{fb2}} = Q_{dum} + Q_{p2}(\phi_2) + Q_{p1}(\phi_4) \tag{3.11}$$

The output voltage is simply the voltage difference between the two outputs:

$$V_{out} = \frac{Q_{C_{fb1}}}{C_{fb1}} - \frac{Q_{C_{fb2}}}{C_{fb2}} \tag{3.12}$$

Substituting Eqns. 3.10 and 3.11 into 3.12, we have:

$$\begin{aligned} V_{out} = & \frac{1}{C_{fb1}} \cdot \Big(Q_{pix} + I_{p1}(\phi 2) \cdot T_{\phi 2} + I_{p2}(\phi 4) \cdot T_{\phi 4} \Big) \\ & - \frac{1}{C_{fb2}} \cdot \Big(Q_{dum} + I_{p2}(\phi 2) \cdot T_{\phi 2} + I_{p1}(\phi 4) \cdot T_{\phi 4} \Big) \end{aligned} \tag{3.13}$$

where the parasitic charge has been replaced by the product of parasitic current and phase sample time. $I_{p1}(\phi 2)$ is the parasitic current on column 1 during phase 2 and $T_{\phi 2}$ is the time duration of phase 2.

We must make three important assumptions in order for the difference in parasitic current to completely cancel. The first and most important assumption is that all circuit elements are completely matched. The matching will depend on the structure and geometry of the capacitors as well as well as on the fabrication process. In particular, we need the feedback capacitors to match.

$$C_{fb1} = C_{fb2} \tag{3.14}$$

Furthermore, there cannot be a change in parasitic current between phases 2 and 4. Since the parasitic current is signal-dependent, this assumption is reasonable. It takes the imager $\frac{1}{F_{imager}}$ seconds to scan the entire array. It is therefore expected that the image will remain still for that time duration. The CDS circuit runs at least m (number of rows) times faster than the refresh rate, so the signal, and thus the parasitic current, should remain constant between $\phi 2$ and $\phi 4$.

$$I_{p1}(\phi 2) = I_{p1}(\phi 4) \tag{3.15}$$

and

$$I_{p2}(\phi 2) = I_{p2}(\phi 4) \tag{3.16}$$

Finally, the time duration of phases 2 and 4 must be equal.

$$T_{\phi 2} = T_{\phi 4} \tag{3.17}$$

If the above three assumptions hold true, the output voltage of the differential amplifier is proportional to the charge difference between the two capacitors:

$$V_{out} = (Q_{pix} - Q_{dum}) \cdot \frac{1}{C_{fb}} \tag{3.18}$$

completely removing the effects of the parasitic current.

3.4 Results

A 256X256 prototype of the passive pixel imager with CDS was implemented in a 2-poly 3-metal $0.6\mu m$ CMOS technology. Appendix A contains the details of the implementation. The improvements achieved with the differential CDS circuit are quantified in terms of FPN. 100 consecutive frames were taken with uniform illumination. Each pixel was then averaged across 100 frames to remove all random noise. The rms column FPN value was calculated by taking the standard deviation of the average value in each column. This

value was then divided by the maximum output voltage of the imager. The rms pixel FPN value was calculated by taking the average of the standard deviation within each column. Similarly, this number was divided by the maximum voltage output. This procedure was repeated for different illumination values.

Fig. 3-10 shows the column-to-column FPN, with and without the CDS circuit, taken with a 4 ms integration time, $10\mu s$ sample time at 30 frames/sec. As expected, the dark FPN values are similar at 0.4 % with and without the CDS circuit. Compared with an active pixel with column FPN of 0.3 % [3], the column FPN of the passive pixel is approximately 30% larger. This difference is caused by mismatches in charge injection and C_{fb}. The charge injection from the switches in the CDS circuit is highly dependent on device size. Any mismatches in the devices that implement the switches will lead to mismatches in charge injection. There will also be column FPN from mismatches in C_{fb} since the dark current leads to an output signal. In an APS, the dark FPN is only visible at the pixel level since that is where the charge-to-voltage conversion occurs. When comparing the pixel FPN, the passive pixel wins with an FPN value of 0.1%, or three times smaller than the active pixel (0.3 % [3]).

The FPN curve with the CDS circuit increases with illumination and levels off at approximately $12.5\mu W/cm^2$ due to pixel saturation. The FPN curve without the CDS circuit continues to increase, however, beyond the saturation level. This increase is due to a second-order effect in which the parasitic current discharges the column lines below the input range of the amplifier. This effect is visible on the image as the columns turn dark after reaching saturation. The point at which this phenomenum occurs varies for different columns, depending on the parasitic current, resulting in bright and dark vertical stripes across the array. The additional reset of the column lines during phase 3 of the CDS prevents the imager from reaching this mode. Furthermore, the switches in the CDS circuit isolate the opamp inputs from the parasitic current on the column lines during the multiplexing phase. Without these switches, the parasitic current would discharge the outputs.

Fig. 3-11 shows a sample image taken with the prototype imager with a 32 ms integration time at 30 frames/sec in a room with typical fluorescent illumination. Table 3.1 summarizes the chip characteristics. Fig. 3-12 shows the diephoto of the fabricated prototype chip.

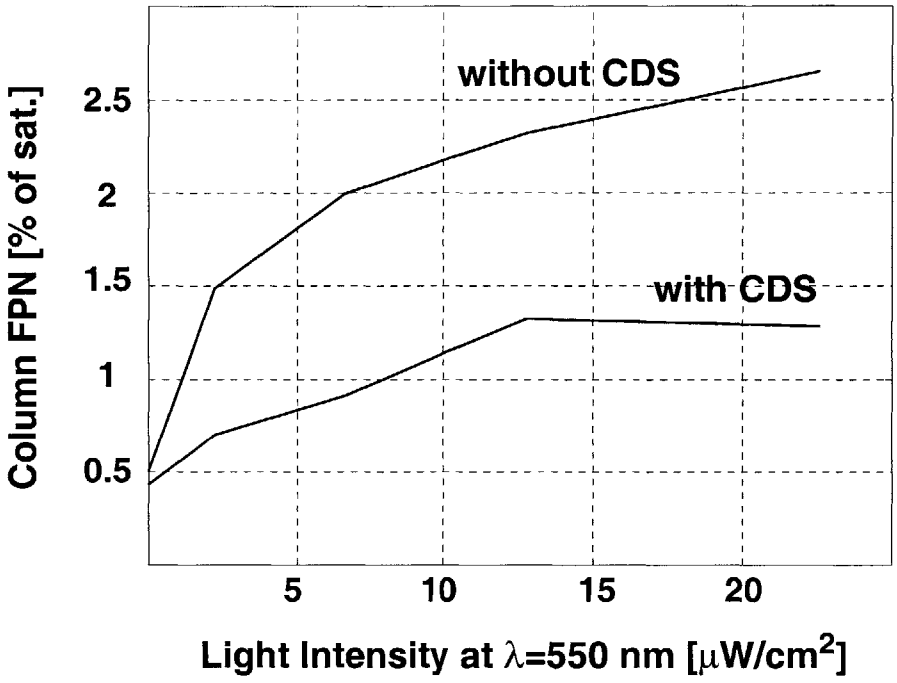


Figure 3-10: Column to Column Fixed Pattern Noise.

Table 3.1: Passive Pixel Imager Characteristics.

Technology	$0.6\mu m$ CMOS DPTM
Die Size	$8.7X6.7mm^2$
Array Size	$256X256$
Pixel Size	$20\mu mX20\mu m$
Photodetector	N-well to P-sub photodiode
Fill Factor	56 %
Frame Rate	30 fps
Supply Voltage	3.3 V
Power Dissipation	10.5 mW
Pixel-to-pixel FPN	0.1 % (dark) of sat. at 25°C
Col-to-col FPN	0.4 % (dark) of sat. at 25°C

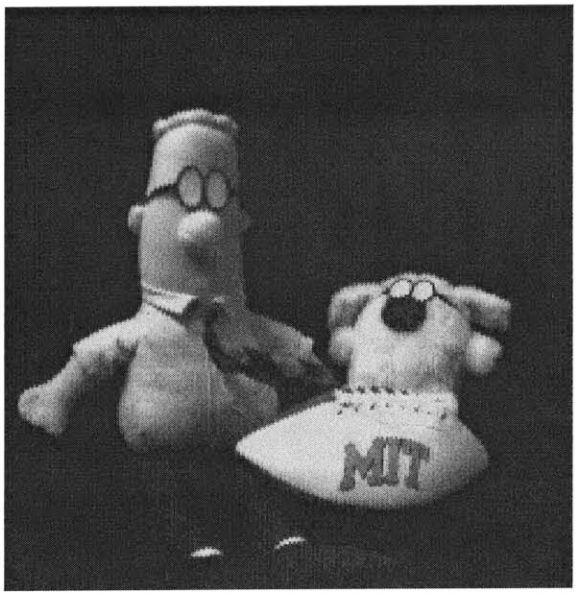


Figure 3-11: Sample image taken with passive pixel imager with CDS.

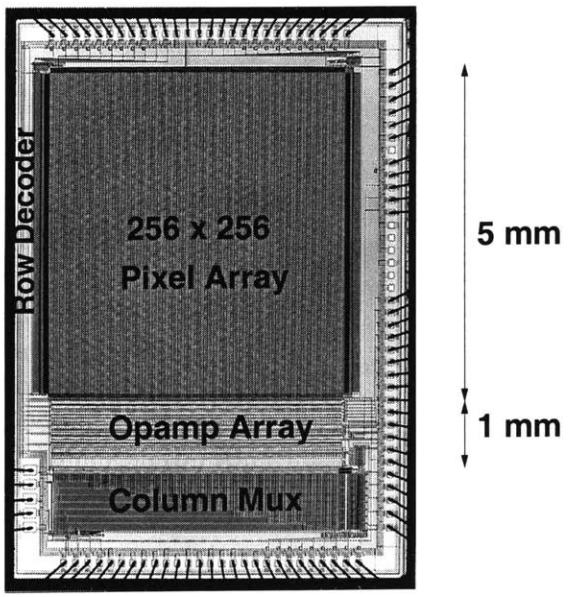


Figure 3-12: Imager Die Photo.

Chapter 4

Noise in Passive Pixels

One of the shortcomings often cited for the passive pixel is the "high temporal noise and the difficulty in increasing the array's size without exacerbating the noise" [25]. In this chapter, the temporal noise sources are identified and their effect on the output rms noise value is analyzed and measured. The noise sources are organized into the opamp read noise, reset noise, and dark current shot noise. A derivation of each noise source is given and an output-referred formula is presented. The model is then compared with noise measurements.

The sources of pixel and column fixed-pattern noise (FPN) are also analyzed. The effects of mismatch in component values, opamp offset voltage and opamp gain, on the column FPN are derived and verified with simulations.

4.1 Temporal noise sources

Fig. 4-1 shows a schematic diagram of the temporal sources of noise in the passive pixel readout circuit. Each noisy component has been modeled as a noiseless component with a noise source. The opamp read noise consists of the thermal, $\overline{v_{th}{}^2}$, and flicker, $\overline{v_f{}^2}$, noise components. The reset noise, $\overline{v_{rstpix}{}^2}$ and $\overline{v_{rstcfb}{}^2}$, more commonly referred to as kT/C noise, comes from the pixel capacitance, C_{pix}, and the feedback capacitance, C_{fb}, respectively. The leakage current of the pixel and column line junctions results in two additional noise source: $\overline{i_{dkpix}{}^2}$ and $\overline{i_{dkcol}{}^2}$.

Since these noise sources are uncorrelated, we can use superposition to analyze them individually. The total output noise can then be calculated by adding the output-referred noise powers.

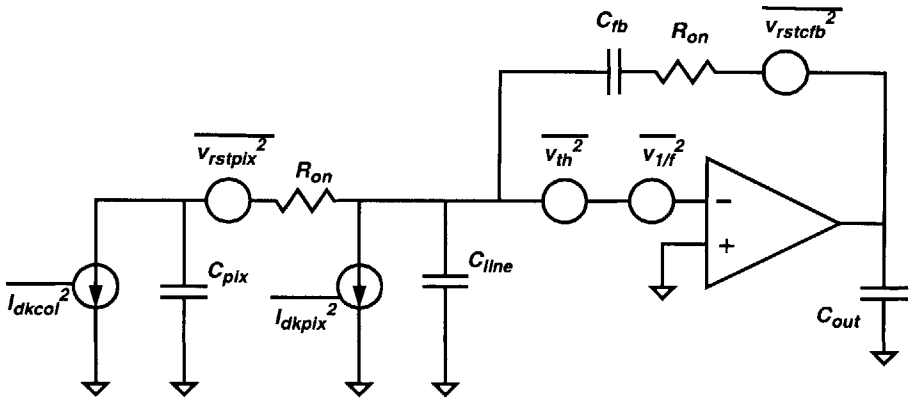


Figure 4-1: Temporal noise sources in passive pixel.

4.2 Opamp read noise

The main noise sources in the opamp are due to thermal and flicker noise. These noise sources are amplified by the loop gain and read out with an auto-zero sample-and-hold circuit. In this section, a model describing the effects of each of these operations is derived.

4.2.1 Thermal Noise

As shown in Fig. 4-2, the opamp thermal noise power is constant with frequency (white) and has a magnitude of:

$$\frac{\overline{v_{th}^2}}{\Delta f} = \frac{16 m_{th} kT}{3 g_m} \tag{4.1}$$

where m_{th} is the noise contribution factor from non-input devices in the opamp, k is Boltzmann's constant, T is temperature and g_m is the transconductance of the amplifier.

4.2.2 Flicker Noise

The flicker noise power, also known as 1/f noise, is expressed as:

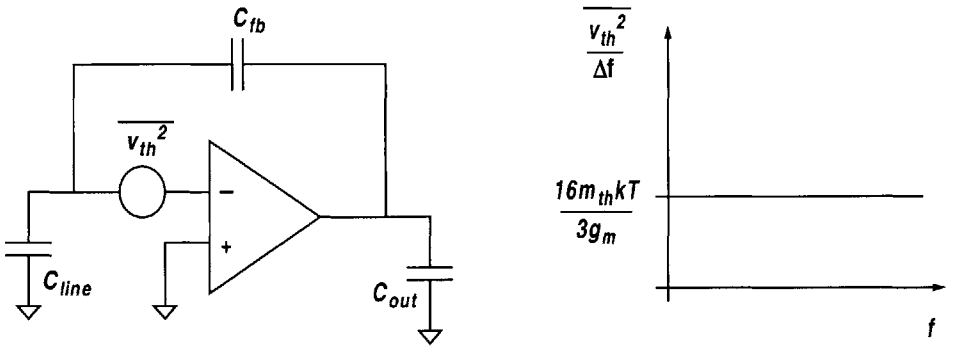


Figure 4-2: Opamp thermal noise.

$$\frac{\overline{v_{1/f}{}^2}}{\Delta f} = \frac{2K_f m_f}{WLC_{ox}{}^2} \cdot \frac{1}{f} \tag{4.2}$$

where K_f is the flicker noise factor, m_f accounts for the flicker noise from non-input devices, W and L are the width and length of the input devices respectively, and C_{ox} is the oxide capacitance. As illustrated in Fig. 4-3, the flicker noise is inversely proportional to frequency, and is therefore most significant at low frequencies.

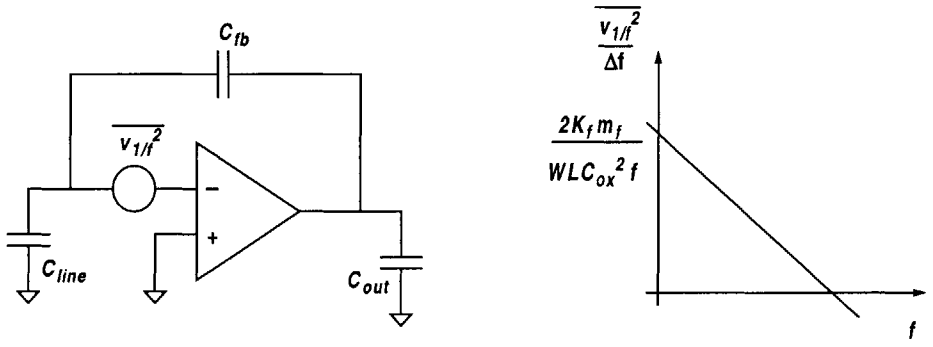


Figure 4-3: Opamp flicker noise.

4.2.3 Sample-and-hold noise model

The opamp noise is read out with the auto-zero technique shown in Fig. 4-4. During the reset phase, the opamp is in unity gain feedback and all capacitors are reset. Immediately before the end of the reset phase, the instantaneous value of the noise is stored on capacitor

C_{line}. During the sample phase, the difference between the reset value on C_{line} and the sampled noise, is transferred onto C_{fb} and appears as the output noise. Any noise at frequencies lower than the sampling frequency is thus rejected.

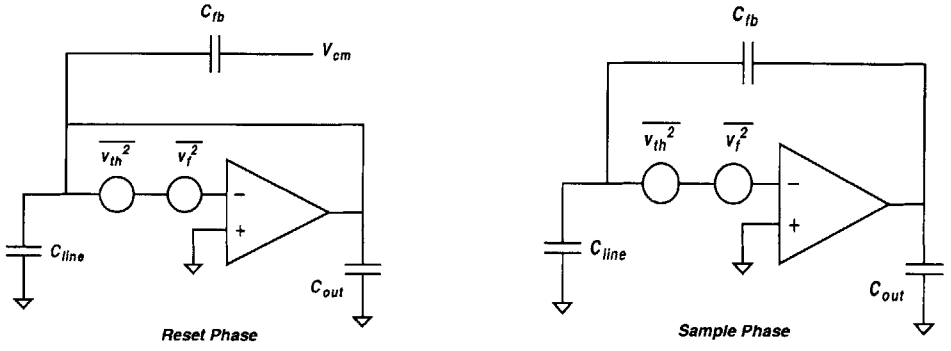


Figure 4-4: Auto-zero readout.

Time-domain model

A model containing the effects of the auto-zero sample-and-hold readout must be derived in order to arrive at an expression for the output referred opamp noise. Fig. 4-5 shows a time domain model for the opamp read noise. The flicker and thermal noise components are summed and passed through the auto-zero and loop gain transfer functions. The resulting output, $v_1(t)$, is then sampled by an impulse train with period T_s, and held for the duty cycle of that period, hT_s.

Frequency-domain model

The sample-and-hold noise model in the frequency domain is shown in Fig. 4-6. The thermal and flicker noise powers are summed and passed through the auto-zero and loop gain transfer functions, $K(f)^2$ and $L(f)^2$. The sample operation is a convolution with an infinite impulse train spaced at the sample frequency, f_s, and with magnitude ${f_s}^2$. Finally, the hold operation multiplies $\overline{v_2{}^2}$ with a sinc function.

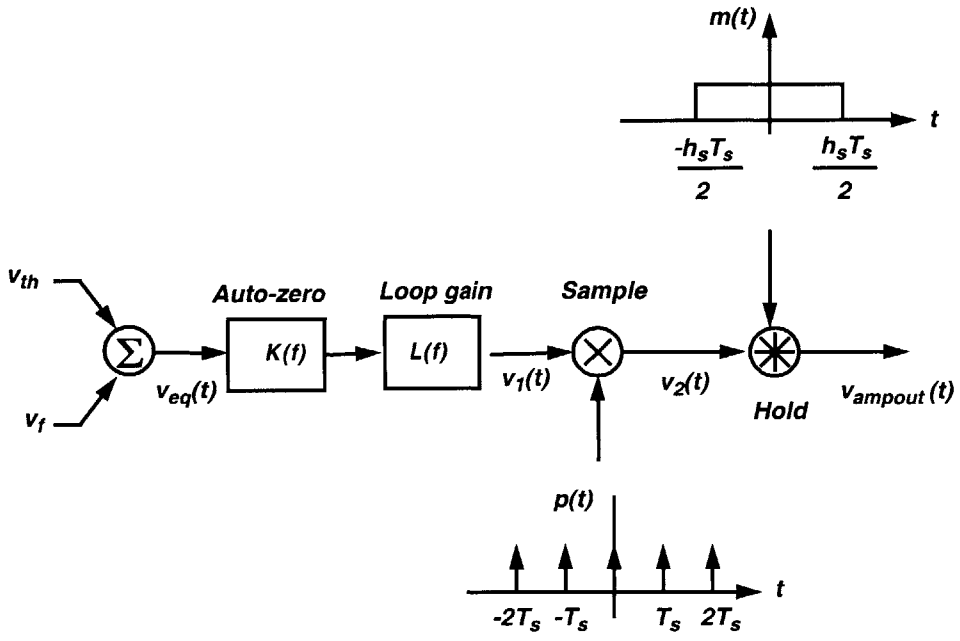


Figure 4-5: Sample-and-hold noise model in time domain.

Auto-zero and loop gain transfer function

The auto-zero function, $K(f)$ can be approximated as a differentiator [26] with a pole at the sampling frequency, f_s, as shown in Fig. 4-7.

$$K(f)^2 = \frac{2f^2}{f_s^2(1+f/f_s)^2} \tag{4.3}$$

This transfer function attenuates the noise below f_s and only passes the noise above f_s. The factor of two comes from the subtraction of two uncorrelated noise sources.

The closed-loop transfer function of the output circuit, $L(f)$, has a loop gain, G, and a pole at f_{3db}.

$$L(f)^2 = \frac{G^2}{(1+f/f_{3db})^2} \tag{4.4}$$

The product of the square of these two transfer functions is a bandpass filter, as illustrated in Fig. 4-7. We can now express the output of this bandpass filter, ${v_1}^2$ as:

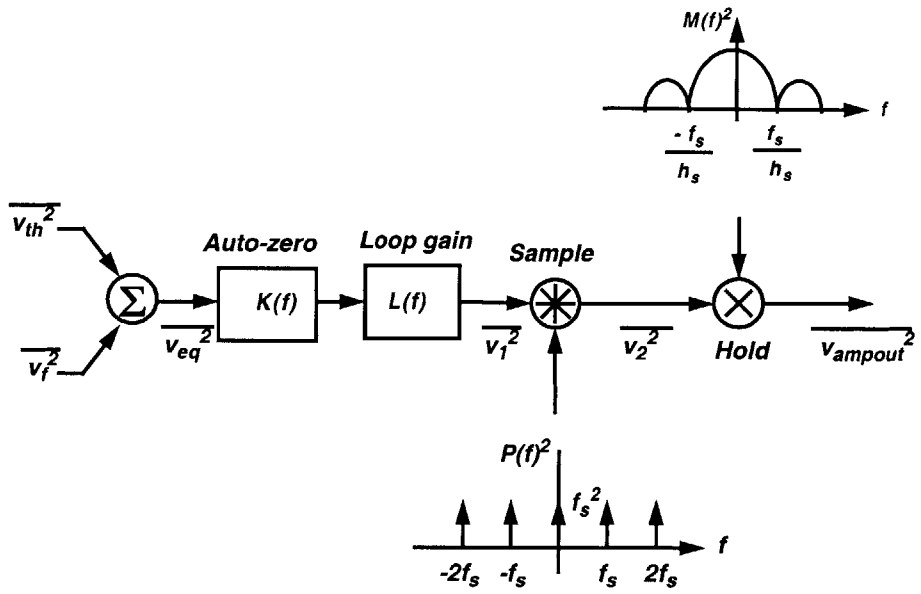


Figure 4-6: sample-and-hold noise model in frequency domain.

$$\frac{\overline{v_1{}^2}}{\Delta f} = \frac{2f^2}{f_s^2(1+f/f_s)^2} \cdot \frac{G^2}{(1+f/f_{3db})^2} \cdot \frac{\overline{v_{eq}{}^2}}{\Delta f} \tag{4.5}$$

where $v_{eq}{}^2$ is the sum of the thermal and flicker noise powers.

Fig. 4-8 shows the input and output of the bandpass filter. The input, $v_{eq}{}^2$, is shown in the left side of the figure and expressed by:

$$\frac{\overline{v_{eq}{}^2}}{\Delta f} = \frac{\overline{v_{th}{}^2}}{\Delta f} + \frac{\overline{v_{1/f}{}^2}}{\Delta f} \tag{4.6}$$

Plugging in equations 4.1 and 4.2, we get

$$\frac{\overline{v_{eq}{}^2}}{\Delta f} = \frac{16 m_{th} kT}{3 g_m} + \frac{2K_f m_f}{WLC_{ox}{}^2} \frac{1}{f} \tag{4.7}$$

The flicker noise dominates at low frequency and the thermal noise dominates at high frequency. The frequency at which the two are equal is called the corner frequency, f_c. We can rearrange this equation by making the following substitutions:

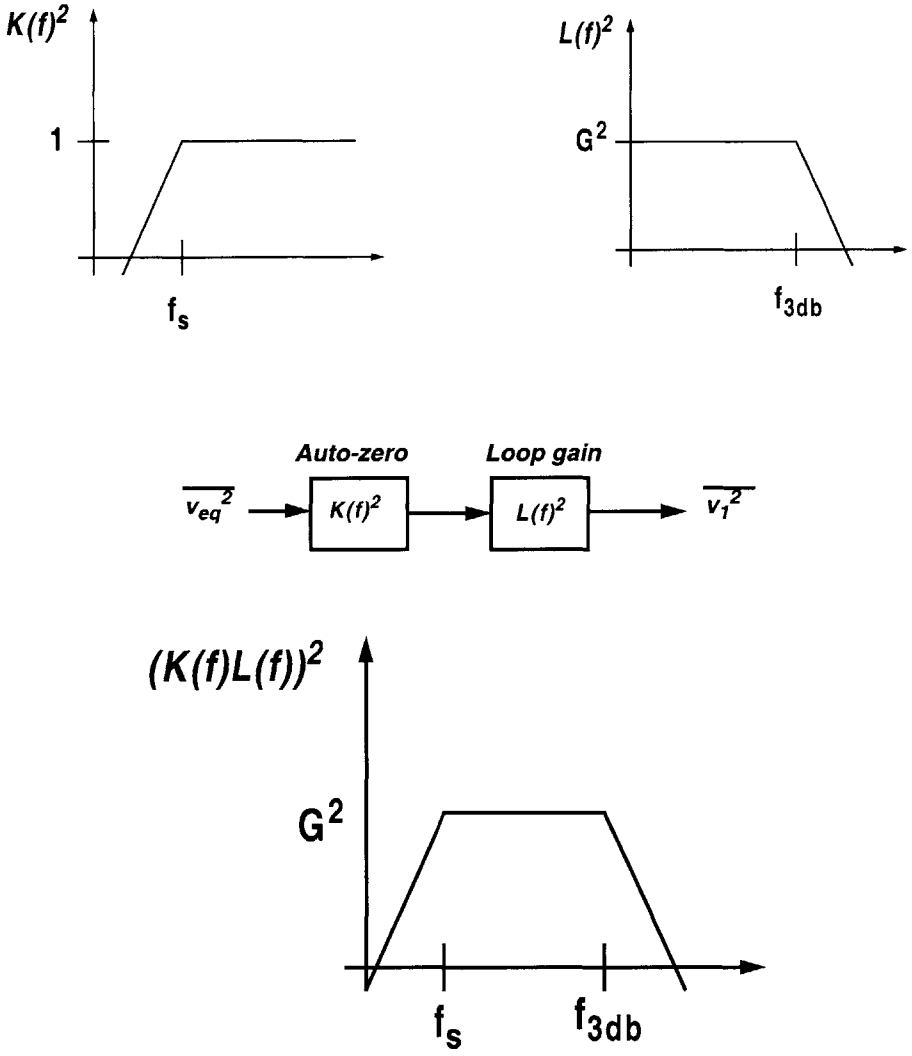


Figure 4-7: Auto-zero and loop gain transfer function.

$$S_{n0} = \frac{16 m_{th} kT}{3 g_m} \tag{4.8}$$

and

$$f_c = \frac{2 K_f m_f}{W L {C_{ox}}^2} \cdot \frac{3 g_m}{16 m_{th} kT} \tag{4.9}$$

leading to:

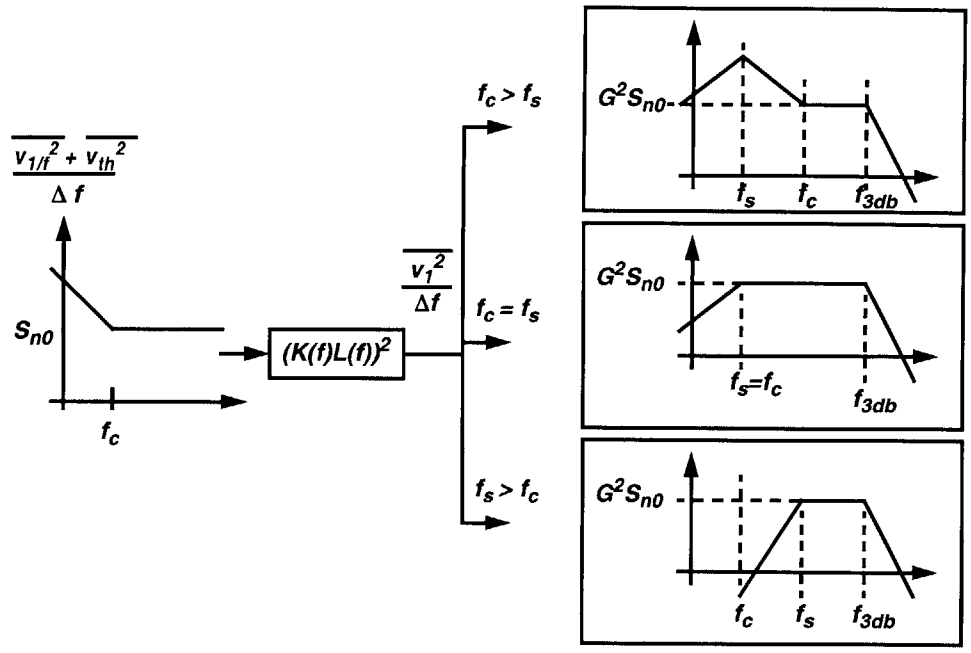


Figure 4-8: Output-referred opamp read noise.

$$\frac{\overline{v_{eq}^2}}{\Delta f} = S_{n0}(1 + f_c/f) \tag{4.10}$$

S_{n0} represents the magnitude of the high frequency noise. The output of the bandpass filter can be rewritten as:

$$\frac{\overline{v_1^2}}{\Delta f} = \frac{2f^2}{f_s{}^2(1 + f/f_s)^2} \cdot \frac{G^2}{(1 + f/f_{3db})^2} \cdot S_{n0}(1 + f_c/f) \tag{4.11}$$

When the read noise is fed into the auto-zero loop gain transfer function, there are three possible outputs depending on the relative values of f_s and f_c. For the case $f_c > f_s$, only the noise below f_s is rejected and ${v_1}^2$ looks similar to the input. On the other hand, when $f_s > f_c$, the output has the bandpass characteristics of the transfer function, $K(f)^2 \cdot L(f)^2$.

Sampled noise

The sampling operation in the frequency domain implies convolving the input with an infinite impulse train. The impulses of the train are spaced at the sampling frequency, f_s,

and have magnitude ${f_s}^2$.

$$\frac{\overline{{v_2}^2}}{\Delta f} = P(f)^2 * \frac{\overline{{v_1}^2}}{\Delta f} \tag{4.12}$$

$$P(f)^2 = f_s^2 \sum_{n=-\infty}^{\infty} \delta(f - nf_s) \tag{4.13}$$

$$\frac{\overline{{v_2}^2}}{\Delta f} = \frac{\overline{{v_1}^2}}{\Delta f} * f_s^2 \sum_{-\infty}^{\infty} \delta(f - nf_s) \tag{4.14}$$

In order to allow the opamp enough time to settle, the sampling frequency must be lower than the closed-loop bandwidth, f_{3db}. Depending on the system requirements, f_{3db} is usually at least twice the value of f_s. Since the bandwidth of the opamp read noise is higher than the sampling frequency, the undersampling leads to aliasing and the high frequency noise is "folded" back to lower frequencies.

Fig. 4-9 illustrates the effects of undersampling [27]. For simplicity, the case $f_c = f_s$ was chosen as the input, and $f_{3db} = 2f_s$. The lowest level in the output shows the convolution with the impulse at $f = 0, 4f_s$. The second level has the samples at $f = f_s, 5f_s$ and so on.

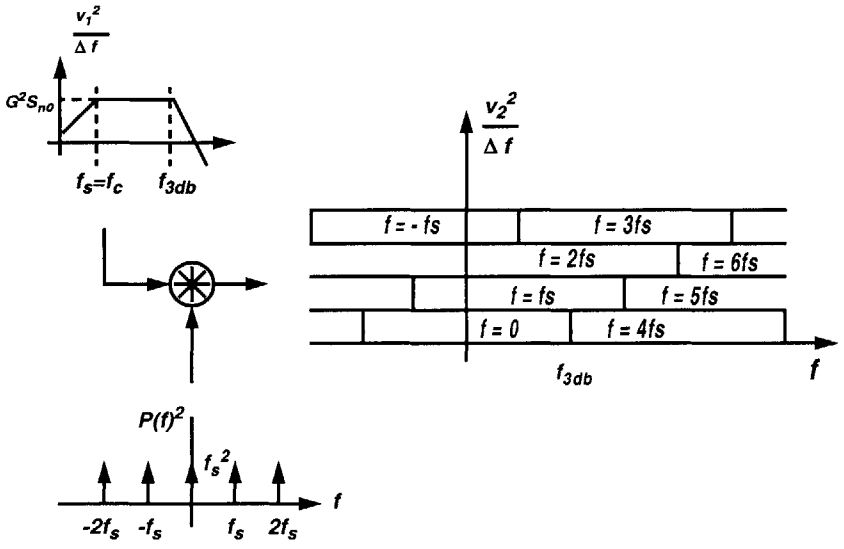


Figure 4-9: Sampled noise.

The result of the convolution of the noise with the impulse train is white noise with magnitude [28], [29], [30]:

$$\frac{\overline{v_2{}^2}}{\Delta f} = 2{f_s}^2 G^2 S_{n0}\left[\frac{\pi f_{3db}}{f_s} + \frac{f_c}{f_s}2\left(1 + ln(\frac{f_{3db}}{f_s})\right)\right] \tag{4.15}$$

The terms in brackets in equation 4.15 correspond to the folded thermal noise and flicker noise, respectively. The thermal noise is multiplied by a factor of π and the ratio of the closed-loop bandwidth and the sampling frequency. The folded flicker noise depends on the relative values of the corner and sampling frequencies. The contribution of the quotient of f_{3db} over f_s is only logarithmic and therefore not as significant as for the folded thermal noise.

Held noise

Holding the output value for a time window of the total sample period translates into multiplying by a sinc function in the frequency domain. Fig. 4-10 shows the white noise input, ${v_2}^2$, and the sinc function, $M(f)^2$.

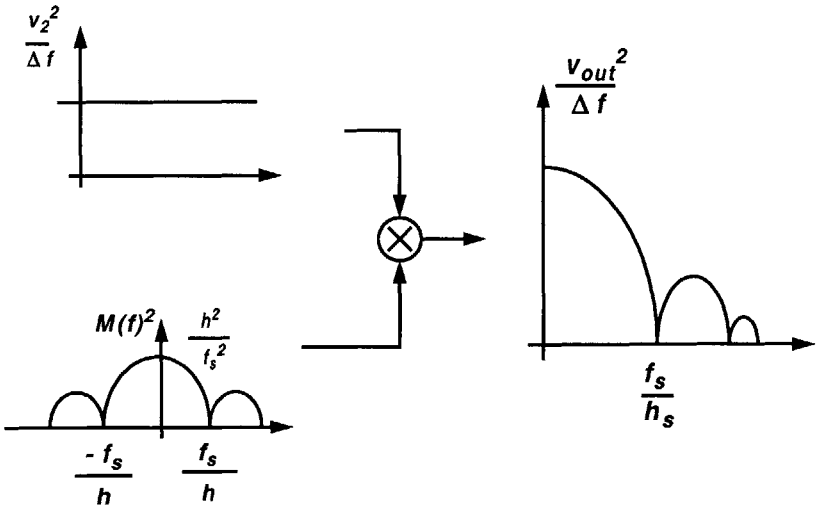


Figure 4-10: Held noise.

The total read noise power seen at the output of the system is then:

$$\frac{\overline{v_{out,read}{}^2}}{\Delta f} = M(f)^2 \cdot \frac{\overline{v_2{}^2}}{\Delta f} \tag{4.16}$$

$$M(f)^2 = \frac{h^2}{f_s{}^2}\left(sinc(\frac{h\pi f}{f_s})\right)^2 \tag{4.17}$$

where h is the duty cycle. Substituting in the expression for $v_2{}^2$ from equation 4.15:

$$\frac{\overline{v_{out,read}{}^2}}{\Delta f} = 2G^2h^2S_{n0}\left[\frac{\pi f_{3db}}{f_s} + \frac{f_c}{f_s}2(1 + ln(\frac{f_{3db}}{f_s}))\right]\left(sinc(\frac{h\pi f}{f_s})\right)^2 \tag{4.18}$$

leading to a band-limited noise spectrum. Equation 4.18 is significant because it is a general expression for any sample-and-hold system using an auto-zero readout.

4.2.4 Output-referred opamp read noise

In order to obtain an expression for the rms noise contribution of the amplifier, we take the integral of equation 4.18 with respect to f:

$$v_{out,read}{}^2 = 2G^2h^2S_{n0}\left[\frac{\pi f_{3db}}{f_s} + \frac{f_c}{f_s}2[1 + ln(\frac{f_{3db}}{f_s})]\right]\int_0^\infty \left(sinc(\frac{h\pi f}{f_s})\right)^2 df \tag{4.19}$$

$$\int_0^\infty \left(sinc(\frac{h\pi f}{f_s})\right)^2 df = \frac{f_s}{2h} \tag{4.20}$$

$$v_{out,read,rms} = \sqrt{G^2hS_{n0}\left[\pi f_{3db} + 2f_c[1 + ln(\frac{f_{3db}}{f_s})]\right]} \tag{4.21}$$

We can now apply equation 4.21 to the passive pixel readout circuit by making the following substitutions:

$$f_{3db} = \frac{1}{G}\frac{g_m}{2\pi C_{out}} \tag{4.22}$$

$$G = \frac{C_{line}}{C_{fb}} \tag{4.23}$$

$$S_{n0} = \frac{16 m_{th} kT}{3 g_m} \tag{4.24}$$

where C_{out} is the capacitor in the opamp which gives rise to the dominant pole. For a folded cascode architecture, this capacitor is the compensating capacitor and connects between the output and ground.

If we further consider that $f_{3db} >> f_c$, the folded flicker noise becomes negligible and the read noise is simplified to:

$$v_{out,read,rms} = \sqrt{\frac{8 m_{th} kT}{3 C_{out}} \frac{C_{line}}{C_{fb}}} \tag{4.25}$$

where the duty cycle, h, has been replaced by the worst-case scenario value of 100% or 1.

It is important to note that the rms noise value does not depend on the sampling frequency, f_s, nor the transconductance of the amplifier, g_m. It is simply a function of the closed-loop gain and output capacitance.

4.3 Reset noise

Reset noise is caused by the thermal noise of the channel resistance of a MOSFET switch. As shown in Fig. 4-1, there are two sources of reset noise in the passive pixel output circuit, the pixel reset noise and feedback capacitor reset noise. While both noise sources are similar, they are analyzed separately since their effects on the output node are different.

4.3.1 Pixel reset noise

As shown in Fig. 4-11, the pixel is reset to the common mode voltage of the amplifier. Each time, the pixel is reset to a slightly different value due to reset noise. That noise is read out, along with the integrated pixel charge, during the sample phase.

Since the pixel is reset via a sample-and-hold configuration, we can use the thermal contribution of equation 4.21 to calculate the pixel reset noise. The factor of 1/2 is added since there is no auto-zeroing operation in this case.

$$v_{rstpix,rms} = \sqrt{\frac{G^2 h S_{n0} \pi f_{3db}}{2}} \tag{4.26}$$

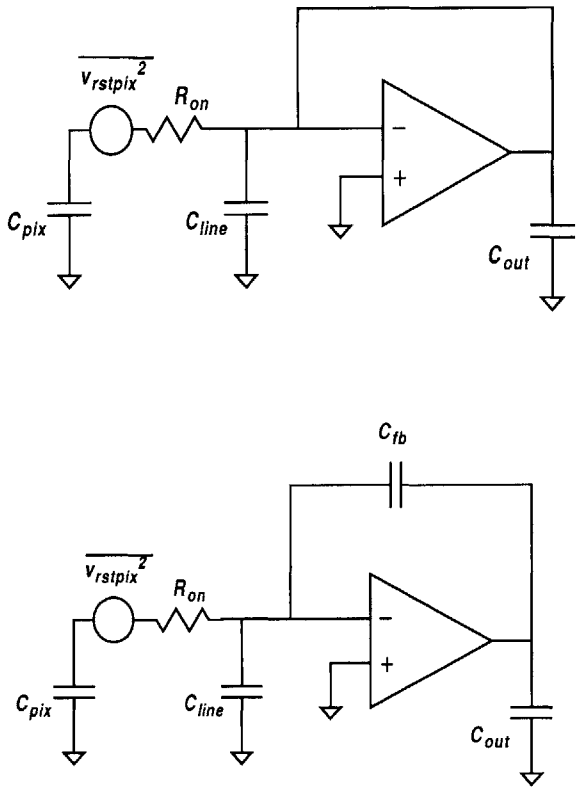


Figure 4-11: Pixel reset noise

Plugging in the values:

$$S_{n0} = 4kTR_{on} \tag{4.27}$$

$$f_{3db} = \frac{1}{2\pi R_{on} C_{pix}} \tag{4.28}$$

and $G = h = 1$, we get the following expression for the rms pixel reset noise:

$$v_{pix,rms} = \sqrt{\frac{kT}{C_{pix}}} \tag{4.29}$$

This noise value will be read out with the integrated charge, leading to an inaccurate pixel measurement. To refer this value to the output of the system, we can look back at

equation 2.12. The output voltage at the end of the sample phase is a function of capacitor ratios. We can re-write this equation as a function of the change in pixel voltage, Δv_{pix}:

$$v_{out} = \Delta v_{pix} \cdot \frac{C_{pix}}{C_{fb}} \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \cdot \frac{A}{A+1} \tag{4.30}$$

Assuming $C_{line} + C_{fb} >> C_{pix}$, and $A >> 1$, the pixel reset noise referred to the output can be expressed as:

$$v_{pixrst,rms} = \frac{C_{pix}}{C_{fb}} \cdot \sqrt{\frac{kT}{C_{pix}}} \tag{4.31}$$

4.3.2 Feedback capacitor reset noise

The feedback capacitor is reset to the common-mode voltage, V_{cm}, as shown in Fig. 4-12. The reset value on the capacitor will be different with each reset, due to the thermal noise of the reset switch, and sampled along with the pixel signal. The reset noise can be derived with the same procedure used for the pixel reset noise.

$$S_{n0} = 4kTR_{on} \tag{4.32}$$

$$f_{3db} = \frac{1}{2\pi R_{on} C_{fb}} \tag{4.33}$$

$$v_{fb} = \sqrt{\frac{kT}{C_{fb}}} \tag{4.34}$$

Since the voltage on C_{fb} is also the output voltage,

$$v_{fbrst,rms} = \sqrt{\frac{kT}{C_{fb}}} \tag{4.35}$$

4.3.3 Other sources of reset noise

While there are four capacitors shown in the reset diagram in figure 4-1, only two are considered in the noise analysis. C_{line} is at analog ground and any noise charge sampled on this node remains in this node. The reset noise on the output capacitor, C_{out}, is negligible since $C_{out} >> C_{pix}, C_{fb}$.

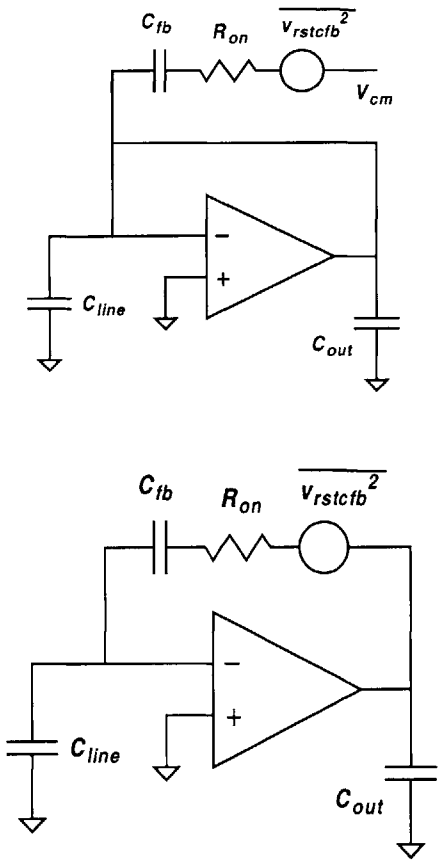


Figure 4-12: Feedback capacitor reset noise

4.4 Dark current shot noise

In the absence of light, the pixel has a non-zero output, also known as pixel dark current. Dark current mainly consists of the reverse-bias current of the photodiode and is highly process dependent. The noise associated with dark current is known as dark current shot noise, and is proportional to the square root of the dark current.

4.4.1 Pixel dark current shot noise

The pixel dark current, illustrated in Fig. 4-13 depends on the dark current density and photodiode area. The accumulated charge due to dark current is a function of the integration time. The total number of electrons due to dark current in the pixel is then given by:

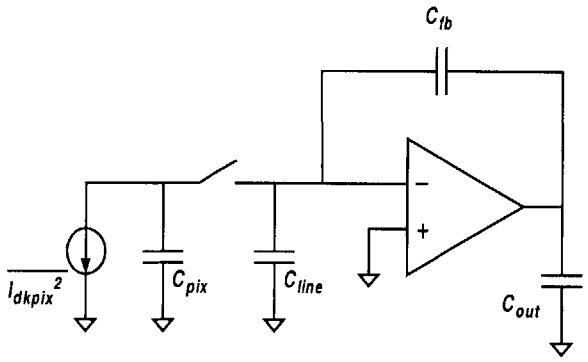


Figure 4-13: Pixel dark current shot noise

$$N_{darkpix} = \frac{1}{q} \cdot J_{dark} \cdot A_{pd} \cdot T_{int} \tag{4.36}$$

where J_{dark} is the dark current density, A_{pd} is the photodiode area and T_{int} is the integration time. The number of electrons due to dark current shot noise is then easily calculated by taking the square root of the dark current electrons:

$$N_{darkshotpix} = \sqrt{\frac{1}{q} \cdot J_{dark} \cdot A_{pd} \cdot T_{int}} \tag{4.37}$$

referred to the output in terms of voltage, we have:

$$v_{darkpix,rms} = \frac{q}{C_{fb}} \cdot \sqrt{\frac{J_{dark} \cdot A_{pd} \cdot T_{int}}{q}} \tag{4.38}$$

4.4.2 Column dark current shot noise

Similar to the pixel dark current, the column line is also exposed to dark current as it is composed of $N^+/P-sub$ junctions (Fig. 4-14). The total number of dark current electrons in the column line is:

$$N_{darkcol} = \frac{1}{q} \cdot J_{dark} \cdot m \cdot A_{sd} \cdot T_{sample} \tag{4.39}$$

where A_{sd} is the area of the source/drain region, m is the number of rows in the array and T_{sample} is the sample time for a single row. In this case, rather than using an integration

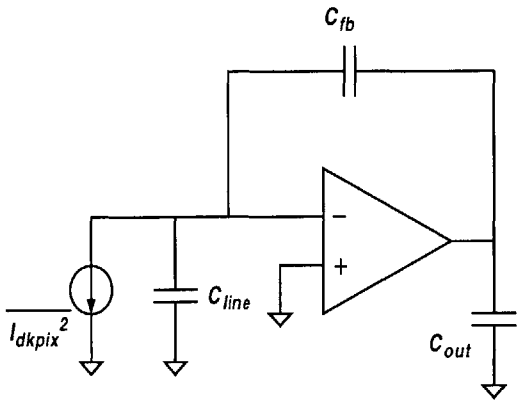


Figure 4-14: Column dark current shot noise

period, we are using a sample time which depends on the frame rate and the number of rows that need to be read out. We can now get the number of electrons due to dark current shot noise in the column line:

$$N_{darkcolshot} = \sqrt{\frac{J_{dark} \cdot m \cdot A_{sd} \cdot T_{sample}}{q}} \tag{4.40}$$

and referring it to the output:

$$v_{darkcol,rms} = \frac{q}{C_{fb}} \cdot \sqrt{\frac{J_{dark} \cdot m \cdot A_{sd} \cdot T_{sample}}{q}} \tag{4.41}$$

Total dark current shot noise

The total dark current shot noise can be obtained by taking the square root of the sum of the squares of the individual dark current shot noise sources from equations 4.38 and 4.41.

$$v_{darktot,rms} = \frac{1}{C_{fb}} \sqrt{qJ_{dark}\left(A_{pd}T_{int} + mA_{sd}T_{sample}\right)} \tag{4.42}$$

The first term in parentheses, $A_{pd}T_{int}$, corresponds to the pixel dark current and is expected to be much larger than the column dark current, $mA_{sd}T_{sample}$, since $A_{pd} >> A_{sd}$ and $T_{int} \approx mT_{sample}$.

Noise Source	Single-ended output Single readout	Differential output Correlated double sampling
$\overline{v_{read}{}^2}$	$\frac{8m_{th}kT}{3C_{fb}}\frac{C_{line}}{C_{out}}$	$\mathbf{2}\cdot\frac{8m_{th}kT}{3C_{fb}}\frac{C_{line}}{C_{out}}$
$\overline{v_{pixrst}{}^2}$	$\left(\frac{C_{pix}}{C_{fb}}\right)^2\frac{kT}{C_{pix}}$	$\mathbf{2}\cdot\left(\frac{C_{pix}}{C_{fb}}\right)^2\frac{kT}{C_{pix}}$
$\overline{v_{fbrst}{}^2}$	$\frac{kT}{C_{fb}}$	$\mathbf{2}\cdot\frac{kT}{C_{fb}}$
$\overline{v_{darktot}{}^2}$	$\left(\frac{1}{C_{fb}}\right)^2 qJ_{dark}\left(A_{pd}T_{int}+mA_{sd}T_{sample}\right)$	$\left(\frac{1}{C_{fb}}\right)^2 qJ_{dark}\left(\mathbf{2}A_{pd}T_{int}+\mathbf{2}mA_{sd}T_{sample}\right)$

Table 4.1: Passive pixel noise power for single-ended output with single readout and differential output with double readout.

4.5 Total temporal noise

Similar to the summation of the dark current shot noise, the total temporal noise at the output can be expressed by the square root of the sum of the squares:

$$v_{tot,rms} = \sqrt{v_{read}{}^2 + v_{pixrst}{}^2 + v_{fbrst}{}^2 + v_{darktot}{}^2} \tag{4.43}$$

Before substituting the value of each noise source obtained in previous sections, we must recall that those derivations were specific for single-ended output with single readout. For a differential output with correlated double sampling readout, the terms must be adjusted as shown in table 4.1.

While the differential architecture with correlated double sampling scheme described in chapter 3 is efficient in removing the effects of the parasitic current, this readout scheme has a negative effect on the total noise of the system. The differential architecture introduces a second set of components, namely C_{dum}, C_{fb2}, $J_{darkdum}$ and $J_{darkcol2}$, which come with their own sources of noise. The second sampling phase, though efficient at removing common and undesired artifacts, actually doubles the amplifier read noise since it is sampled twice. The subtraction of offsets therefore leads to the addition of noise.

The read noise gets multiplied by a factor of two due to the double sampling. Since we are dealing with a single amplifier, the differential readout does not affect the read noise. The reset noise power for both capacitors, C_{pix} and C_{fb}, doubles due to the differential readout. In this case, there are two pixel capacitors, C_{pix} and C_{dum}, and two feedback capacitors, C_{fb1} and C_{fb2}. For this calculation, it is safe to assume $C_{pix} = C_{dum}$ and $C_{fb1} = C_{fb2}$. Each capacitor is only reset once during the cycle, so the double sampling has no effect on the reset noise.

Both pixel and column dark current shot noise powers get doubled since we are taking the difference between two noise sources and thus doubling the noise.

The differential architecture is effective at completely removing the amplified ground bounce term. Since both opamp inputs are connected to column lines sitting on the same substrate, the ground bounce is not amplified. Furthermore, since the differential outputs are referenced to each other rather than to ground, any bounce is completely rejected.

Now we are ready to plug in the correct values for the differential architecture with double sampling readout:

$$v_{tot,rms} = \sqrt{2\frac{8m_{th}kT}{3C_{fb}}\frac{C_{line}}{C_{out}} + 2\left(\frac{C_{pix}}{C_{fb}}\right)^2\frac{kT}{C_{pix}} + 2\frac{kT}{C_{fb}} + \frac{qJ_{dark}}{{C_{fb}}^2}\left(2A_{pd}T_{int} + 2mA_{sd}T_{sample}\right)} \tag{4.44}$$

Reordering some terms, we can simplify:

$$v_{tot,rms} = \sqrt{\frac{1}{C_{fb}}\left[kT\left(\frac{16m_{th}C_{line}}{3C_{out}} + \frac{2C_{pix}}{C_{fb}} + 2\right) + \frac{2qJ_{dark}}{C_{fb}}\left(A_{pd}T_{int} + mA_{sd}T_{sample}\right)\right]} \tag{4.45}$$

4.6 Temporal noise measurements

The following set of data show the spectrum of the passive pixel temporal noise power. It will be useful to refer to the total noise power spectrum as the sum of the read and reset noise components:

$$\frac{\overline{{v_{out}}^2}}{\Delta f} = \frac{2h^2}{f_s}\left(\frac{16m_{th}kT}{3C_{out}}\frac{C_{line}}{C_{fb}} + \frac{2kT}{C_{fb}}\frac{C_{pix}}{C_{fb}} + \frac{2kT}{C_{fb}}\right)\cdot sinc^2\left(\frac{\pi hf}{f_s}\right) \tag{4.46}$$

We have neglected the dark current shot noise contribution since it is much smaller than the read and reset noise for this case. The noise spectrum was measured with different values of f_s, C_{line}, and C_{out}, and the results are shown in the following sections.

4.6.1 Output noise spectrum

The passive pixel temporal noise was measured using a spectrum analyzer. Fig. 4-15 shows the total output noise power spectrum for $f_s = 100kHz$. The measured data closely matches the modeled sinc function with nulls at multiples of $\frac{f_s}{h}$.

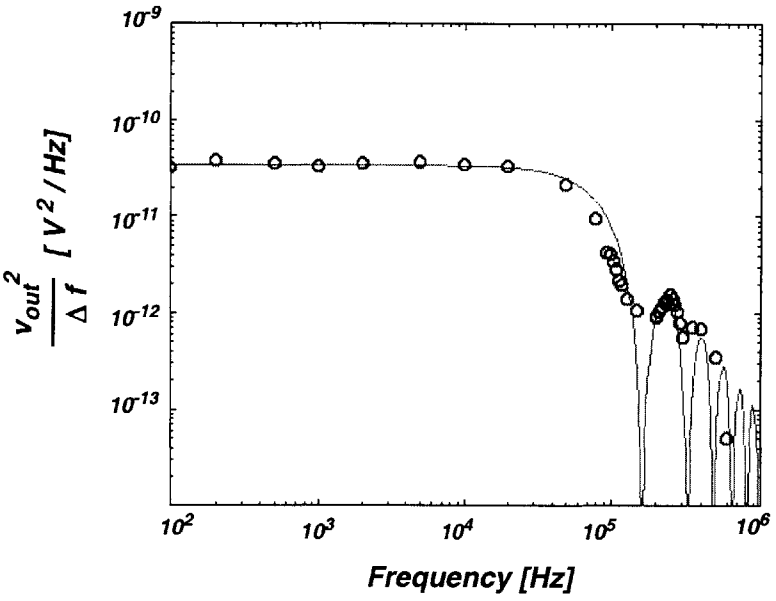


Figure 4-15: Output noise power.

4.6.2 Varying sample frequency

As expected, varying the sample frequency affects the magnitude and the frequency of the sinc function. Fig. 4-16 shows the noise spectrum for $f_s = 50kHz$ and $f_s = 100kHz$. The height of the sinc doubles from $100kHz$ to $50kHz$, but the bandwidth decreases by the same amount, leaving the integral over frequency intact.

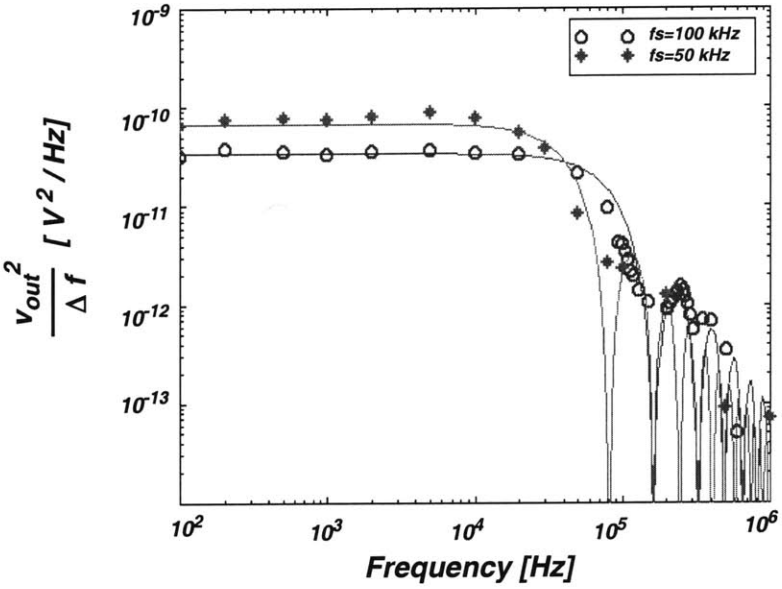


Figure 4-16: Output noise power for different values of sampling frequency.

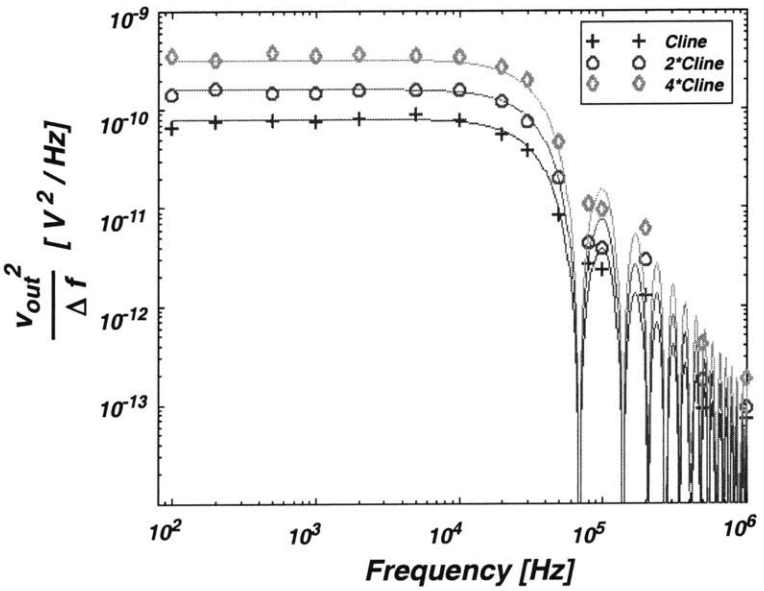


Figure 4-17: Output noise power for different values of Cline.

4.6.3 Varying C_{line}

The bit line capacitance of the column line of the pixel array, C_{line}, increases the noise spectrum through the loop gain. In Fig. 4-17, three different values of C_{line} were used to measure the noise. When C_{line} is doubled, the height of the sinc also doubles. Looking back at equation 4.46, we see there are three terms that contribute to the total noise: opamp read, C_{fb} reset and C_{pix} reset, but only the first term contains C_{line}. If doubling C_{line} doubles the noise power, we can conclude that the read noise is the most significant source of noise in the system.

We can observe the combined effects of increasing f_s and C_{line}. The noise power was measured at a low frequency ($f = 1Khz$) and plotted for different values of f_s. This was repeated for three different values of C_{line} and plotted in Fig. 4-18.

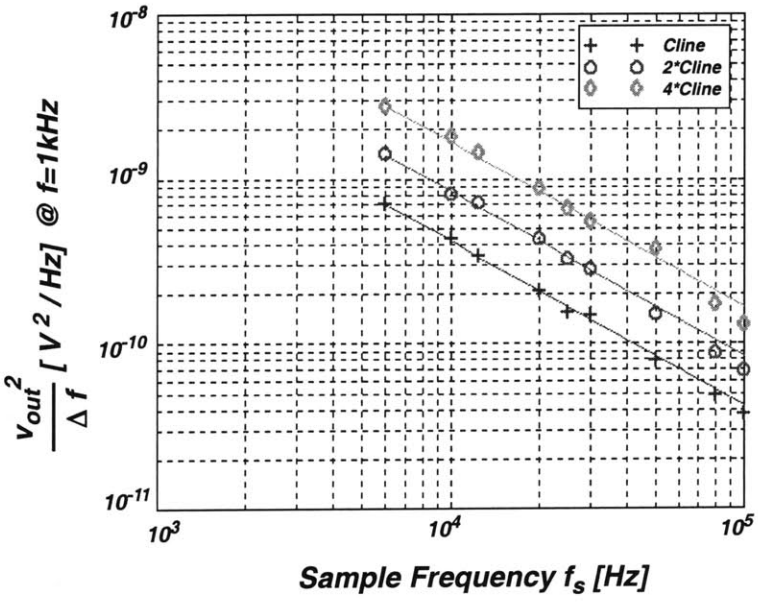


Figure 4-18: Output noise power for different values of Cline and fs..

The data was fitted with the line $1/f$ to determine if the height of the sinc indeed varies inversely proportionally to f_s. The trend was confirmed for different values of f_s and C_{line}. Additionally, we can see that the factor of two between different values of C_{line} is maintained over a wide range of sampling frequencies.

4.6.4 Varying C_{out}

The noise was measured with two different values of C_{out}. As shown in Fig. 4-19, increasing C_{out} by a factor of two decreased the noise power by a factor of two. This finding further confirms the theory that the read noise is the most significant contributor to the total noise of the system.

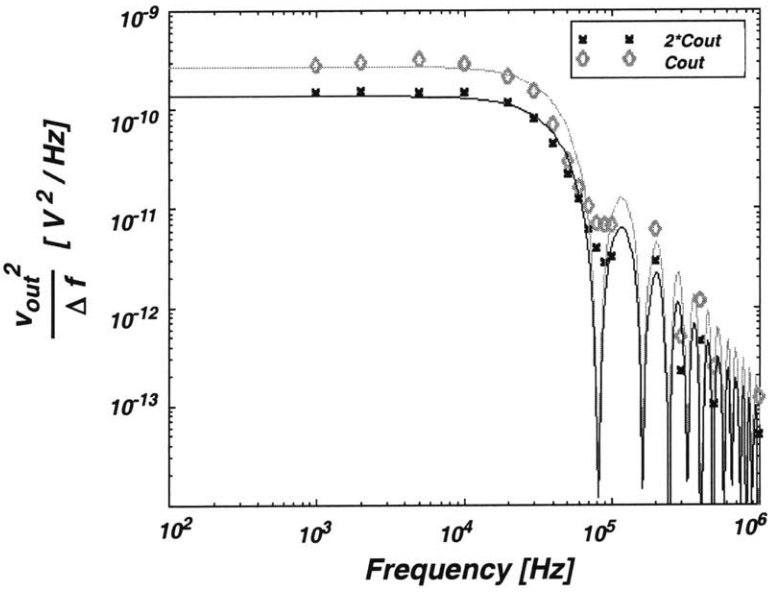


Figure 4-19: Output noise power for different values of Cout.

It is feasible to reduce the read noise by increasing C_{out}. By recalling the read noise for a differential output with CDS from Tab. 4.1,

$$v_{read,rms} = \sqrt{\frac{16 m_{th} kT}{3 C_{fb}} \frac{C_{line}}{C_{out}}} \tag{4.47}$$

we can see that the read noise is inversely proportional to the square root of C_{out}. By doubling C_{out}, we can decrease the read noise by a factor of $\sqrt{2}$. The total noise will decrease by a factor of $\sqrt{2}$, if the read noise is the dominant source of noise. By comparing with the reset noise sources in Eq. 4.46, the read noise is the dominant source of the total noise for

$$\frac{8 m_{th}}{3} \frac{C_{line}}{C_{out}} > 1 \tag{4.48}$$

In other words, we can increase C_{out} to a value of $\frac{8m_{th}}{3}C_{line}$. Beyond this point, the noise will be dominated by the reset noise sources. Fig. 4-20 shows the relationship between the total output noise over increasing values of C_{out}. The noise initially decreases with a slope of $\sqrt{2}$ and levels off at $C_{out} = \frac{8m_{th}}{3}C_{line}$.

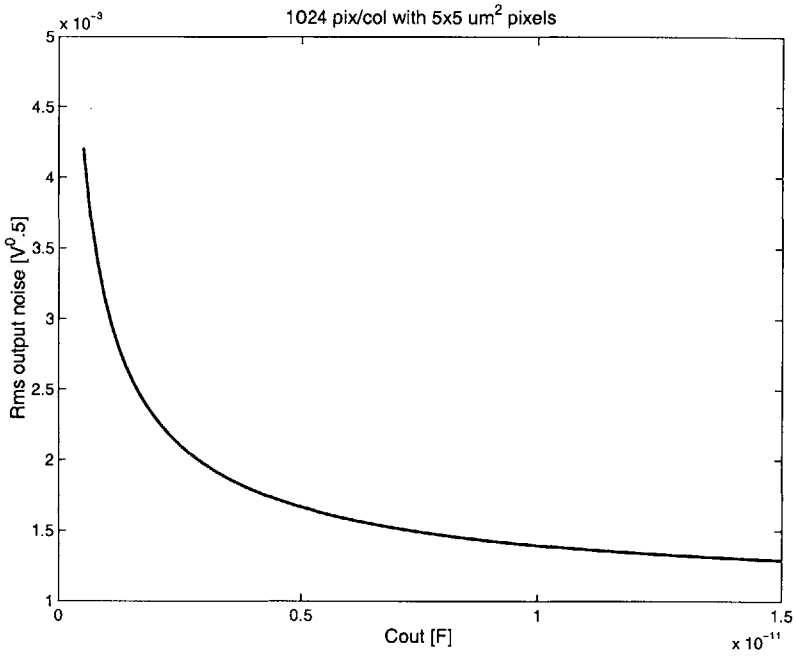


Figure 4-20: Rms output noise as a function of C_{out}.

In order to maintain a constant bandwidth while changing C_{out}, we must increase g_m by the same amount since the unity-gain bandwidth for an amplifier is set by the ratio of the transconductance and dominant capacitance (C_{out} in this case):

$$f_{unity} = \frac{g_m}{2\pi C_{out}} \tag{4.49}$$

$$g_m \alpha C_{out} \tag{4.50}$$

The transconductance can be increased by modifying the drain current or the device geometry:

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{4.51}$$

If we keep the device sizes constant, I_D must increase by the square of g_m:

$$I_D \alpha {g_m}^2 \tag{4.52}$$

It is good practice to increase the current in all legs of the amplifier equally, in order to preserve the same opamp characteristics. The total amplifier power will then increase with the current:

$$P = I_D \cdot V_{dd} \tag{4.53}$$

The relationship between power and C_{out} is then

$$P \alpha {C_{out}}^2 \tag{4.54}$$

Fig. 4-21 illustrates the quadratic relationship between power and C_{out}. Fig. 4-22 shows the relationship created between noise and power through C_{out}. The noise decreases rapidly for the first milliwatt of power and then levels off. In other words, power can be slightly increased to increase the noise performance up to a certain limit. Beyond this limit, the noise performance does not change.

4.7 Fixed-pattern noise

Fixed-pattern noise (FPN) consists of differences between pixel outputs across the array. It is constant over time but varies across space. The extra pixel functionality and column-parallelism that makes CMOS imagers so attractive is also the source of one of its biggest drawbacks, FPN. Any mismatches between circuit elements in the pixel leads to pixel-to-pixel FPN. Similarly, mismatches in the column output circuitry results in column FPN. FPN is detrimental to an imager because it is easily detected by the naked eye as a grainy image (with pixel FPN) or stripes (with column FPN), instead of the expected uniform image.

4.7.1 Pixel fixed pattern noise

The sources of pixel FPN for a passive pixel are mismatches in dark current and photodiode area. The pixel dark current is likely to vary from pixel-to-pixel, particularly if the

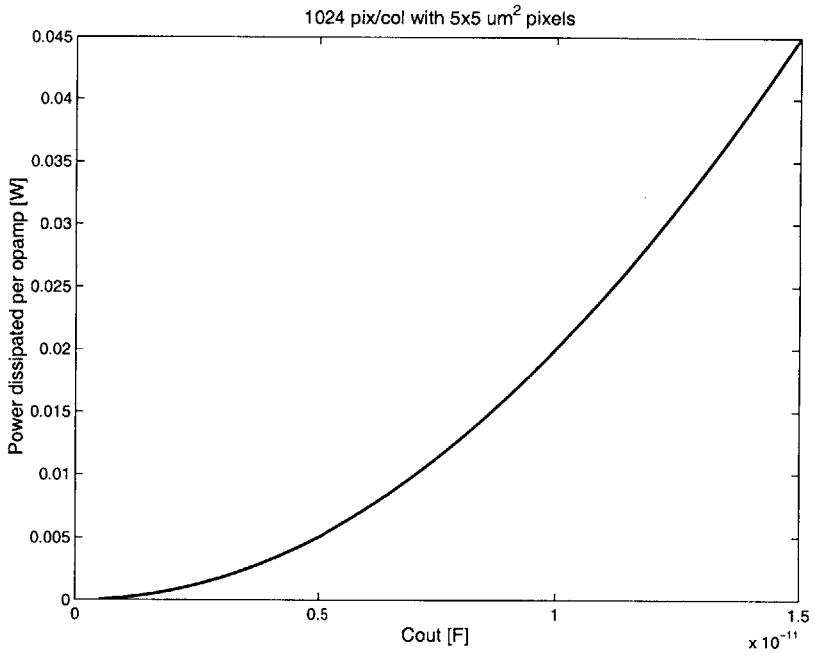


Figure 4-21: Amplifier power as a function of C_{out}.

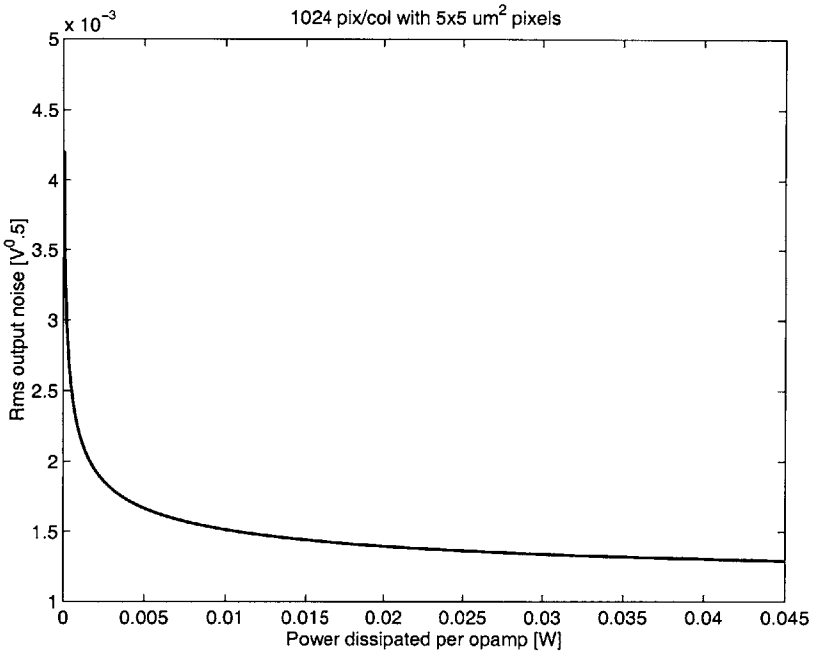


Figure 4-22: Rms output noise and power as a function of C_{out}.

Noise Source	Column FPN Contribution	Error type
A	$\frac{V_{out}}{A(A+1)} \cdot \Delta A$	gain
C_{fb}	$\frac{V_{out}}{C_{fb}} \cdot \Delta C_{fb}$	gain
C_{line}	$\frac{V_{out} \cdot C_{pix}}{(C_{line}+C_{fb}+C_{pix})(C_{line}+C_{fb})} \cdot \Delta C_{line}$	gain
C_{pix}	$\frac{-V_{out}}{C_{line}+C_{fb}+C_{pix}} \cdot \Delta C_{pix}$	gain

Table 4.2: Sources and effects of column FPN for passive pixel.

photodiode area changes. A difference in the photodiode area between two pixels will also result in different quantum efficiencies and thus different output voltages.

Unlike the active pixel, the passive pixel is not affected by variations in device parameters, such as threshold voltage. For processes where the dominant source of pixel FPN is the device mismatch, the passive pixel will achieve a lower pixel FPN.

4.7.2 Column fixed pattern noise

Column FPN is more severe in passive pixels than in active pixels since the column output circuit is more complex. Recalling equation 2.19:

$$V_{out} = \frac{Q_{pix}}{C_{fb}} \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \frac{A}{A+1} \tag{4.55}$$

Since all noise sources are uncorrelated, we can determine the column FPN by taking the partial derivatives of V_{out} with respect to each term in the equation that is common to one column, while keeping all other variables constant. The effect of a mismatch in C_{fb}, for instance, can be calculated as:

$$\frac{\partial V_{out}}{\partial C_{fb}} = \frac{Q_{pix}}{C_{fb}} \cdot \frac{C_{line} + C_{fb}}{C_{line} + C_{fb} + C_{pix}} \cdot \frac{A}{A+1} \cdot \frac{1}{C_{fb}} \approx V_{out} \cdot \frac{1}{C_{fb}} \tag{4.56}$$

$$\partial V_{out} = V_{out} \cdot \frac{\partial C_{fb}}{C_{fb}} \tag{4.57}$$

Table 4.2 lists the contributions of column fixed pattern noise from the different com-

ponents of the output circuit. All non-uniformities from column-to-column are gain terms and thus change with V_{out}.

Among the gain errors, the most significant source of column FPN comes from mismatches in C_{fb}. Any variation in C_{fb} from column-to-column will directly impact the output voltage. Simulations show that a 10% mismatch in C_{fb} results in a 9.44% difference at the output. It is therefore good practice to design C_{fb} as geometrically large as possible to minimize mismatches. The effects of mismatches in C_{line} and C_{pix} are considerably smaller than those of C_{fb}. A variation of 10% in C_{line} results in a mere 0.0591% difference at the output. Similarly, a change in C_{pix} of 10% changes the output by 0.0594%. Both variations were indiscernable in an HSPICE simulation.

The effect of a variation in the open-loop gain can be neglected since it is attenuated by a factor of A. A variation in offset voltage will appear as the only offset term in the column FPN, or as the column FPN in the dark.

The column FPN can be simplified to include the most significant term:

$$\frac{\partial V_{out}}{V_{out,max}} \approx \frac{V_{out}}{V_{out,max}} \frac{\Delta C_{fb}}{C_{fb}} \tag{4.58}$$

represents a gain error.

4.8 Performance comparison

The performance of the passive pixel designed for this thesis is compared with that of an APS [31] and a Frame-Transfer CCD (FT-CCD) [32] in Tab. 4.3. All three pixels are layed out in similar pixel area with similar technologies. The APS used in this comparison consists of 3-transistors and one N-well-to-P-substrate photodiode, and attains a fill factor of 26% in an area of $4x4\mu m^2$. The high fill factor of the passive pixel, 45%, results in a responsivity 2.5 times higher than that of the APS. The temporal noise is the biggest weakness of the passive pixel. At 1.36 mV, the passive pixel temporal noise is almost ten times larger than the noise for both the APS and CCD. We can divide the noise floor by the conversion gain to obtain a value for the sensitivity, or minimum lux that the imager can detect. The APS is found to have the highest sensitivity, as it can sense signals three times smaller than the passive pixel. The CCD follows closely with a sensitivity of $196\mu lux - sec$. As a result of the high noise floor, the dynamic range is also significantly lower for the passive pixel.

Comparison Metric	N-well Passive Pixel (1T)	N-well APS (3T)	Frame-Transfer CCD	Units
Pixel size	5 x 5	4 x 4	5.1 x 5.1	μm^2
Fill factor	45	26	—	%
Vertical resolution	512	—	1280	pixels per row
Conversion gain	16	40	23	$\mu V/e^-$
Saturated signal	36 K	30 K	40 K	e^-
Responsivity	2.7	1.1	1.17*	$V/lux \cdot sec$
Temporal noise	1.36	0.15	0.23	mV
Sensitivity	504	136	197	$\mu lux - sec$
Dynamic range	53	78	71	dB
Min. feature size	0.35	0.25	0.5	μm

Table 4.3: Performance comparison of passive pixel, APS and CCD. * Quoted value for green light was multiplied by factor of three to approximate monochrome responsivity.

Chapter 5

Scaling of passive pixels

Consumer demand for higher spatial resolution at a lower cost has pushed image sensors to achieve higher pixel density, i.e. more pixels per unit area. This higher pixel density is accomplished by shrinking the pixel size in order to accommodate more pixels in the same area. Both, smaller pixel geometries and higher resolution, present challenges for the passive pixel as they directly increase the temporal noise.

This chapter discusses the effects of scaling pixel size and resolution on the output noise over three different fabrication technologies. We start with a description of the scaling parameters. A computational model is then used to illustrate the effects of the three aforementioned parameters on the pixel fill factor, output noise and dynamic range. We close with a discussion on the tradeoffs in scaling and the fundamental limits of the passive pixel.

5.1 Scaling parameters

5.1.1 Spatial resolution

The vertical resolution was swept from 256 to 1284 pixels per column. The main component affected by the spatial resolution is the parasitic capacitance of the column line, C_{line}. As illustrated in Fig. 5-1, three capacitances make up C_{line}:

$$C_{line} = m(C_{db} + C_{gd} + C_{mb}) \tag{5.1}$$

where m is the number of pixels per column, C_{db} is the drain-to-bulk capacitance, C_{gd} is

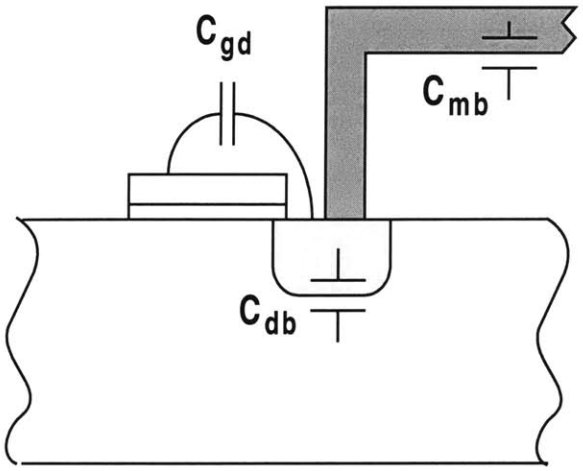


Figure 5-1: Parasitic column line capacitance components.

the gate-to-drain capacitance, and C_{mb} is the metal-to-bulk capacitance. Each capacitance can in turn be expressed as:

$$C_{db} = C_j A_{sd} + C_{jsw} P_{sd} \tag{5.2}$$

$$C_{gd} = C_{gdo} W \tag{5.3}$$

$$C_{mb} = C_m mw \cdot pp + 2C_{msw} \cdot pp \tag{5.4}$$

C_j	$N^+ - P_{sub}$ junction capacitance	$[F/\mu m^2]$
C_{jsw}	$N^+ - P_{sub}$ sidewall capacitance	$[F/\mu m]$
C_{gdo}	gate-to-drain capacitance	$[F/\mu m]$
C_m	metal2-to-substrate capacitance	$[F/\mu m^2]$
C_{msw}	metal2-to-substrate fringe capacitance	$[F/\mu m]$
A_{sd}	source/drain area of rowsel transistor	$[\mu m^2]$
P_{sd}	source/drain perimeter of rowsel transistor	$[\mu m]$
W	channel width of rowsel transistor	$[\mu m]$
mw	width of column line	$[\mu m]$
pp	pixel pitch	$[\mu m]$

$$C_{line} = m(C_j A_{sd} + C_{jsw} P_{sd} + C_{gdo} W + C_m mw \cdot pp + 2C_{msw} \cdot pp) \tag{5.5}$$

C_{line} is directly proportional to the number of pixels per column. The most significant terms in equation 5.5 are the junction capacitances associated with the drain of the row select transistor. The drain should thus be designed to be as small as the technology will allow. The pixel pitch affects C_{line} only slightly since the metal capacitance is small compared to the junction capacitance. In a CMOS $0.35\mu m$ process, 256 pixels per column result in a C_{line} of $1.2pF$.

5.1.2 Pixel size

The effects of pixel scaling on the output noise was observed for a range of pixel sizes from $4\mu mx4\mu m$ to $20\mu mx20\mu m$. The smallest pixel size of $4\mu mx4\mu m$ was chosen based on the optical limits of the lens technology [33]. The pixel size affects the output noise through the pixel and feedback capacitances, C_{pix} and C_{fb}. The pixel capacitance can be expressed as a function of the N-well to P-sub junction capacitance, C_{jnw}, and gate-to-drain capacitance, C_{gdo}:

$$C_{pix} = A_{pd} C_{jnw} + P_{pd} C_{jnwsw} + C_{gdo} W \tag{5.6}$$

where A_{pd} and P_{pd} are the area and perimeter of the photodiode, respectively. The area of the photodiode is the product of the pixel area and the pixel fill factor.

$$A_{pd} = pp^2 \cdot FF(pp, technology) \tag{5.7}$$

The photodiode area takes a double hit when the pixel size is reduced. As the pixel area shrinks, the photodiode area naturally decreases. The fill factor, however, will also decrease with the pixel area. For larger pixel geometries, the photodiode occupies most of the pixel area. On the other hand, for small pixel geometries, the pixel overhead, i.e. the rowsel transistor and metal lines, begins to take a larger fraction of the pixel area, and thus reduces the fill factor.

As mentioned in section 2.6.2, the feedback capacitance is closely linked to the pixel capacitance:

$$C_{fb} = C_{pix}\frac{V_{cm}}{V_{sw}} \tag{5.8}$$

where V_{cm} is the common mode voltage and reset pixel voltage and V_{sw} is the maximum output swing of the amplifier. C_{fb} is then directly proportional to C_{pix} and is severely affected by pixel scaling.

5.1.3 Technology

Three CMOS fabrication technologies were used to observe the scaling effects, $0.6\mu m$, $0.35\mu m$, and $0.18\mu m$. Table 5.1 lists the main differences between the processes. The power supply voltage, as well as the threshold voltages were scaled per design specifications. The only capacitance that was changed in the model was the gate-to-drain capacitance, C_{gdo}, since it is directly related to the oxide capacitance and therefore the oxide thickness. While the junction capacitances of the N-well and N-dif are also process dependent, they only depend on the square root of the lower-doped region (substrate) and were therefore kept constant with technology.

Feature	$0.6\mu m$	$0.35\mu m$	$0.18\mu m$
Minimum gate length	$0.6\mu m$	$0.35\mu m$	$0.18\mu m$
Maximum voltage	5 V	3.3 V	1.8 V
V_{Tn}	0.77 V	0.6 V	0.55 V
V_{Tp}	0.8 V	0.74 V	0.53 V
C_{gdo}	$1.6x10^{-16}F/\mu m$	$3.5x10^{-16}F/\mu m$	$4.3x10^{-16}F/\mu m$

Table 5.1: Design features for $0.6\mu m$, $0.35\mu m$, and $0.6\mu m$.

5.2 Effects of scaling

The figures of merit used to evaluate the scaling effects are pixel fill factor, output noise and dynamic range. The above three imager characteristics are the most seriously affected and pose the most difficult challenges for scaling high-density passive pixel arrays.

5.2.1 Fill factor

Pixel fill factor was calculated by laying out the passive pixel with an N-well photodiode in three different technologies over the pixel range. Fig. 5-2 illustrates the pixel fill factor as a function of pixel pitch. The passive pixel in $0.18\mu m$ technology obviously had the highest fill factor. On the other hand, it was impossible to implement a passive pixel in the $0.6\mu m$ technology with a pixel pitch below $6\mu m$. For the $0.35\mu m$ process, the fill factor decreases very quickly for pixel pitch below $8\mu m$. This slope is gentler for the case of the $0.18\mu m$ technology. The difference between the $0.18\mu m$ and $0.35\mu m$ technologies becomes more pronounced for smaller pixel geometries.

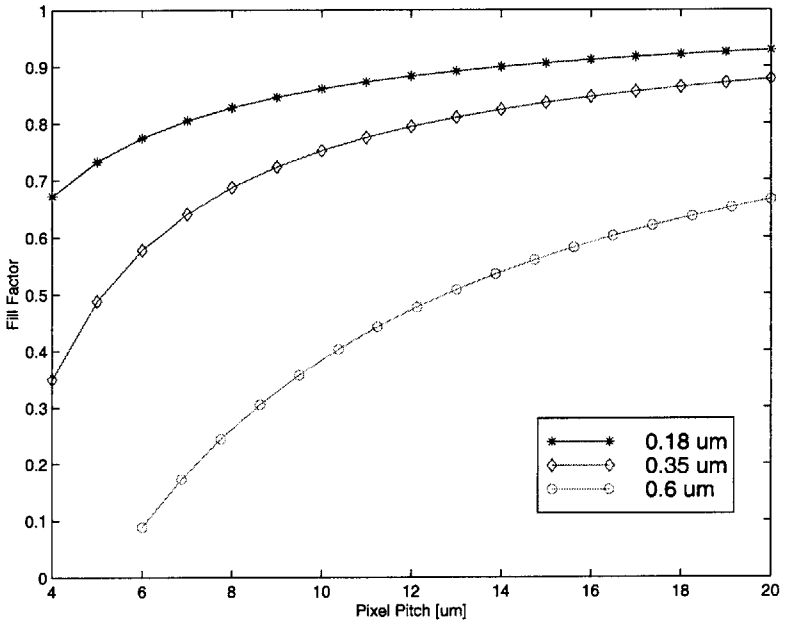


Figure 5-2: Pixel fill factor as a function of pixel pitch.

5.2.2 Output noise

The output noise was first decomposed into its three major components: read, C_{fb} reset, and C_{pix} reset noise:

$$v_{out,tot,rms} = \sqrt{(v_{out,read,rms})^2 + (v_{out,rstcfb,rms})^2 + (v_{out,rstpix,rms})^2} \tag{5.9}$$

where

$$v_{out,read,rms} = \sqrt{\frac{8kT}{C_{fb}} \cdot \frac{C_{line}}{C_{out}}} \tag{5.10}$$

and m_{th} has been replaced by the value for a folded cascode amplifier, 1.5.

$$v_{out,rstcfb,rms} = \sqrt{\frac{2kT}{C_{fb}}} \tag{5.11}$$

$$v_{out,rstpix,rms} = \sqrt{\frac{2kT}{C_{fb}} \cdot \frac{C_{pix}}{C_{fb}}} \tag{5.12}$$

$$v_{out,tot,rms} = \sqrt{\frac{2kT}{C_{fb}}(4\frac{C_{line}}{C_{out}} + 1 + \frac{C_{pix}}{C_{fb}}+)} \tag{5.13}$$

The output noise power was then observed for a single technology by varying a single parameter and keeping the other parameter fixed. This comparison provided some insight on the make-up of the noise components with the changing parameters.

The total rms noise for each technology was then plotted in a single graph in linear and logarithmic scales. The linear plot helps obtain an accurate reading, while the log plot is useful in observing trends over a wide range of values.

Pixel scaling

We can see in Fig. 5-3 that the read noise power is dominant over the range of pixel pitches, indicating $\frac{C_{line}}{C_{out}} > 1$. Note that all three noise components increase with decreasing pixel pitch since they are all inversely proportional to the square root of C_{fb}.

Figs. 5-4 and 5-5 show the total output rms noise for the three technologies with varying pixel pitch in linear and logarithmic scales, respectively. In the log scale plot, we can see that the difference in noise between the technologies is similar for large pixels, but begins to diverge for smaller pixels. The curve for $0.18\mu m$ has a slope of $\frac{1}{pp}$. Since C_{fb} is proportional to the photodiode area, or pp^2, it makes sense that the rms noise is inversely proportional to pp.

Spatial resolution scaling

Fig. 5-6 shows the noise power of the individual noise components over a range of the number of pixels per column, m. The reset noise components do not change since they

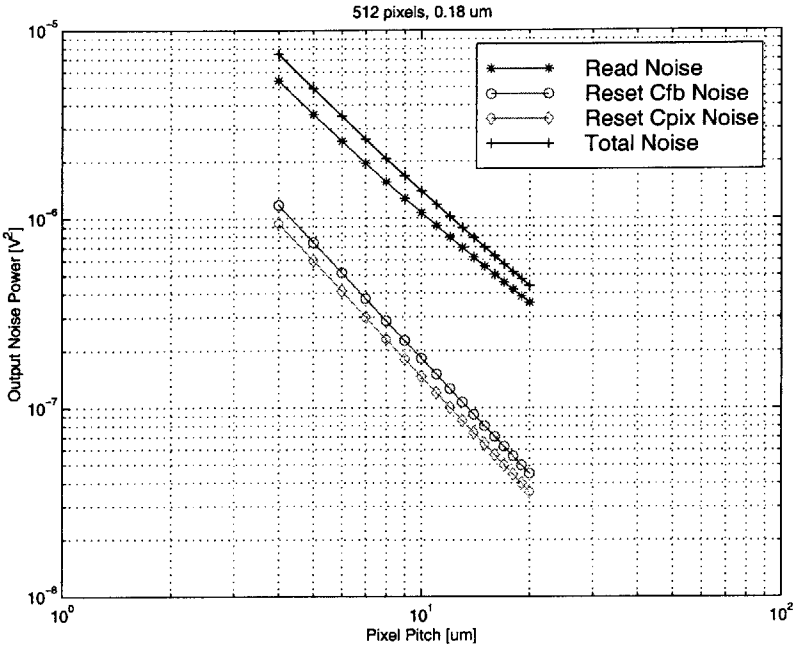


Figure 5-3: Noise components as function of pixel pitch.

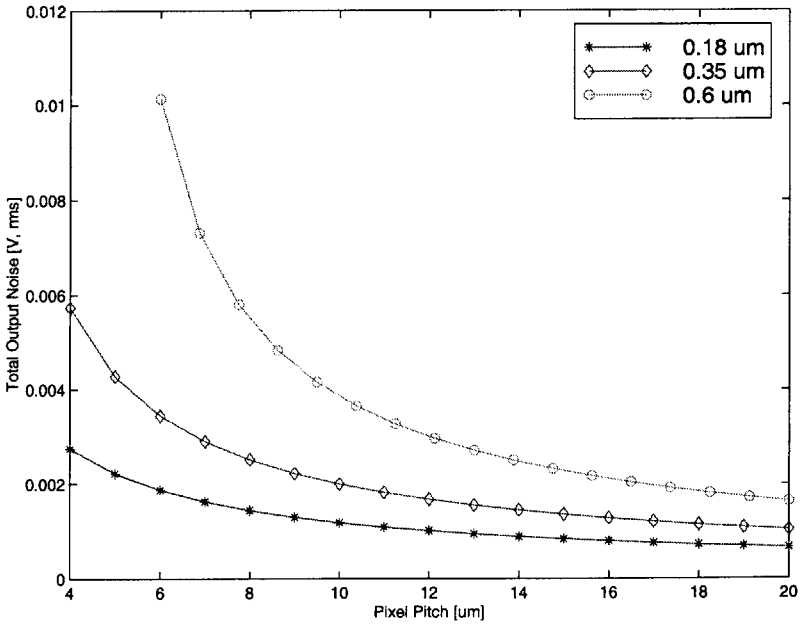


Figure 5-4: Output noise as function of pixel pitch.

are not related to m. The only value changing is the opamp read noise, which is directly proportional to C_{line}. For large m, the read noise is dominant since it is the only noise

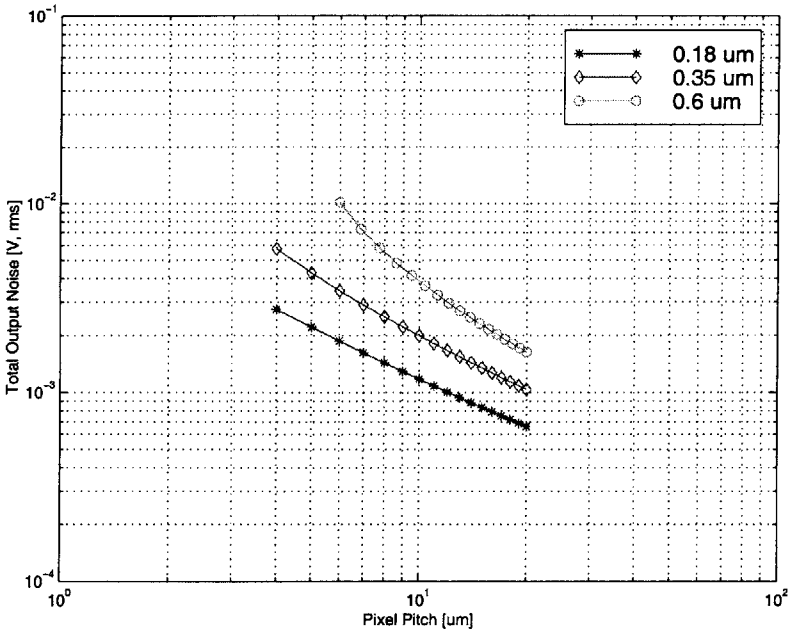


Figure 5-5: Output noise as function of pixel pitch.

component that changes with C_{line}.

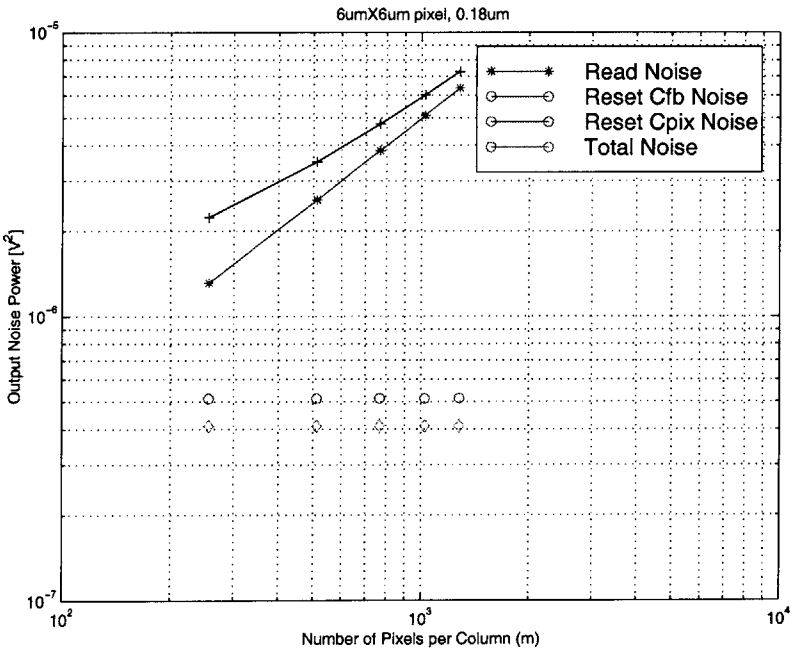


Figure 5-6: Noise components as function of spatial resolution.

Figs. 5-7 and 5-8 present the total output rms noise for the three technologies for an

increasing number of pixels. The noise follows the order of increasing technologies, since the pixel size is fixed. The logarithmic scale shows that in all three technologies, the noise changes with similar slopes.

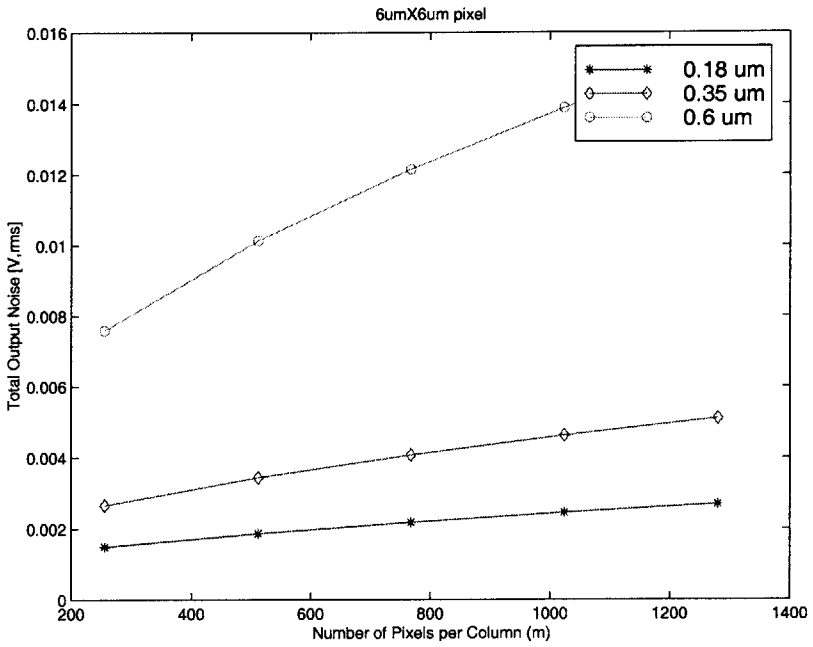


Figure 5-7: Output noise as function of spatial resolution.

5.2.3 Dynamic range

The dynamic range of an imager is defined as the maximum output swing divided by the noise floor. For the passive pixel, it can be written as:

$$DR = \frac{V_{sw}}{\sqrt{\frac{2kT}{C_{fb}}(1 + \frac{C_{pix}}{C_{fb}} + 2\frac{C_{line}}{C_{out}})}} \tag{5.14}$$

The output swing of the imager is simply the output swing of the opamp. For the sake of this study, the output swing was generalized to be:

$$V_{sw} = V_{dd} - 2V_{dsat} \tag{5.15}$$

where V_{dsat} is the voltage necessary to keep a device in the saturation regime. A value of $0.2V$ was used for V_{dsat} for all three processes. This value depends on the current and

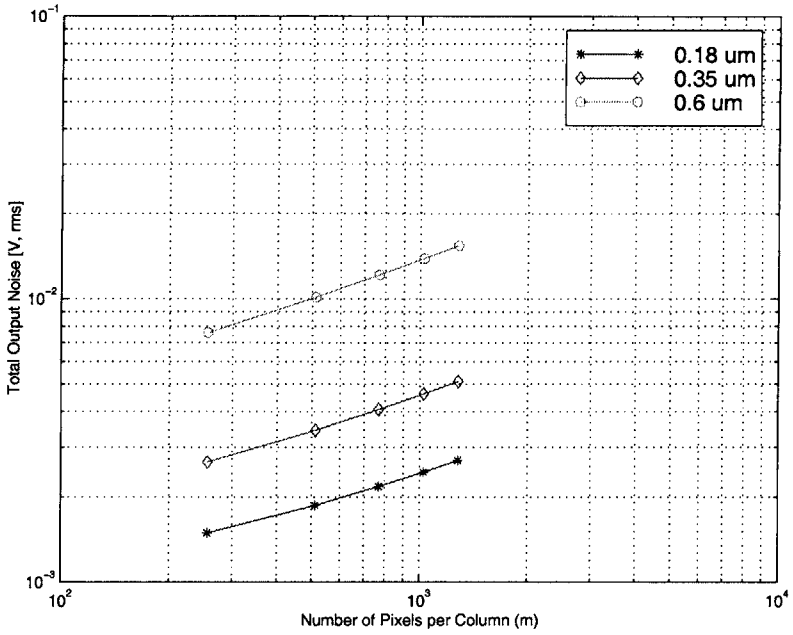


Figure 5-8: Output noise as function of spatial resolution.

device size of the amplifier.

$$DR = \frac{V_{dd} - 2V_{dsat}}{\sqrt{\frac{2kT}{C_{fb}}(1 + \frac{C_{pix}}{C_{fb}} + 2\frac{C_{line}}{C_{out}})}} \tag{5.16}$$

Pixel scaling

Fig. 5-9 shows the dynamic range as a function of pixel pitch. Surprisingly, the dynamic range for the $0.35\mu m$ technology is the highest at 52 dB for a $4\mu m x 4\mu m$ pixel and the $0.18\mu m$ has the lowest. Despite the lowest noise performance for the $0.18\mu m$ process, the loss in the output swing, due to a lower V_{dd}, results in a low dynamic range.

Spatial resolution scaling

A similar effect is noted in Fig. 5-10, which shows the dynamic range change over m. The $0.35\mu m$ has the highest dynamic range, but this time, the $0.6\mu m$ process has the lowest DR. Again, the loss in output swing in the $0.18\mu m$ is to blame for the lower DR despite better noise figures. For the $0.6\mu m$ process, even a larger output swing was not enough to salvage the dynamic range, due to higher noise.

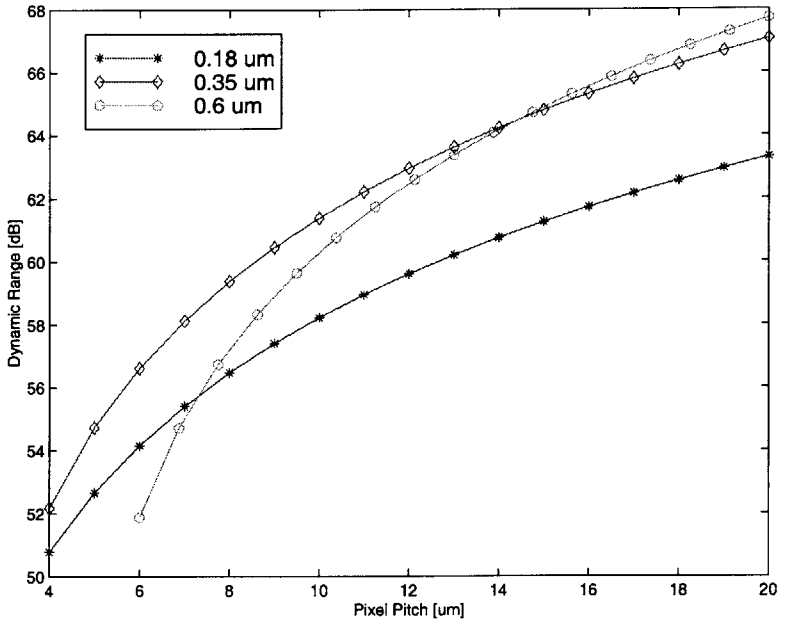


Figure 5-9: Dynamic range as function of pixel pitch.

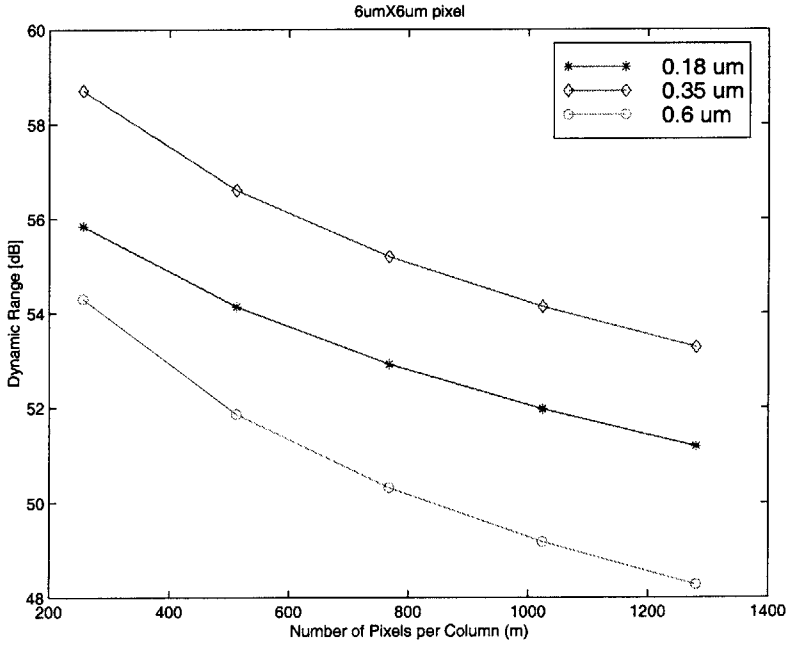


Figure 5-10: Dynamic range as function of spatial resolution.

5.2.4 Scaling summary

The noise performance of the passive pixel was analyzed over a range of pixel size ($4\mu m x 4\mu m$ to $20\mu m x 20\mu m$) and vertical resolution (256 to 1284 pixels per column). Below is a list of

the major findings of this study:

- Fill factor decreases with pixel pitch. As the pixel area decreases, the pixel overhead, i.e. transistor and metal interconnect, begins to take up a larger portion of the pixel, leaving less area for the photodiode. The fill factor can be improved for a specific pixel pitch by moving to a smaller technology. A smaller row select transistor and more compact interconnect allows more area for the photodiode and thus leads to a higher fill factor.

- The read noise is amplified by the large loop gain of the output circuit, $\frac{C_{line}+C_{fb}}{C_{fb}}$, and is therefore the dominant source of noise over the range of pixel size and resolutions investigated. An increase in the number of rows per column leads to an increase in C_{line}, and consequently an increase in the temporal noise. Scaling to a smaller pixel size affects the read noise in two ways: smaller pixel area and smaller fill factor. When the feedback capacitor is similarly scaled to maintain a constant output swing, it causes the loop gain, and therefore the noise, to increase by the same amount.

- The dynamic range is a ratio of the maximum output voltage over the total noise. While the $0.18\mu m$ technology had the best noise performance, its dynamic range was hurt by the lower power supply voltage. The highest dynamic range was achieved by the $0.35\mu m$ technology since it had the best balance between output swing and noise.

5.3 Fundamental limits

Scaling the passive pixel for high-density arrays presents two adverse effects on the noise performance. Shrinking the pixel size reduces the pixel capacitance and consequently the feedback capacitance. A higher vertical resolution results in a higher column line capacitance. By looking at the noise expression in equation 5.13, it is clear that both trends lead to an increase in noise.

Moving to a smaller technology helps reduce the total noise at the expense of the output swing. Therefore, the dynamic range does not necessarily increase with a lower technology. The best dynamic range was actually achieved by the technology with the best balance between output swing and noise.

The passive pixel reaches a fundamental limit when scaling for high-density arrays. Both scaling parameteres, pixel size and vertical resolution, are directly coupled to the noise, leading to a tradeoff between pixel density and noise.

Chapter 6

Conclusions

6.1 Thesis Contributions

This thesis present an in-depth study of the weaknesses and fundamental limits of the passive pixel for high-density imaging arrays. A signal-dependent parasitic current, temporal noise and scaling challenges were the focus of this study.

A signal-dependent parasitic current was identified in the passive pixel output. The sources were divided into optically-generated carrier diffusion, blooming and subtheshold currents. This parasitic current was found to contaminate the pixel charge at the column line, resulting in cross-talk between far-away pixels in the column line. A CDS circuit with a differential architecture was effective in removing the effects of this parasitic current.

The sources of temporal noise were identified as opamp read noise, capacitor reset noise, and dark current shot noise. The read and reset noise sources were individually modeled with a sample and hold block diagram in the frequency domain and found to closely match experimental results. Noise measurements also indicated that the opamp read noise is the main noise contribution.

The scaling of the passive pixel for high-density arrays was analyzed. The pixel fill factor, output noise and dynamic range were simulated with a computational model over a range of pixel sizes, vertical resolutions, and fabrication technologies. The noise was inversely proportional to the pixel area and directly proportional to the resolution. The dynamic range was the highest for the technology with the best balance between noise level and output swing. The findings showed that there is a strong relationship between scaling and output noise.

6.2 Future Work

Some suggestions for future work:

- The tradeoff between noise and spatial resolution can be further investigated in a high-density array by varying the spatial resolution when low noise performance is required [34]. Under low illumination conditions, the spatial resolution can be traded off for lower noise. As the illumination increases and the noise performance is no longer required, the resolution can be increased.

  Averaging a small array of nxn pixels to produce a single pixel output can reduce the noise by a factor of $\frac{1}{\sqrt{n}}$. This average function can be easily implemented in a passive pixel. The addition operation is accomplished by selecting n rows simultaneously. The division operation is easily achieved by selecting a feedback capacitor n times the original value. This will reduce the noise by another factor of $\frac{1}{\sqrt{n}}$, resulting in a total noise reduction of $\frac{1}{n}$ for a decrease of $\frac{1}{n^2}$ in the resolution.

- A second direction for future work on the passive pixel involves moving to a smaller technology, such as $0.18\mu m$, to take advantage of the higher fill factor and lower noise. The dynamic range could then be increased by exploring other opamp configurations that maximize output swing.

- Finally, on the processing side, a lowly-doped implant around the drain region of the row select transistor could be used to reduce the parasitic capacitance of the column line. The pixel layout could also be optimized by reducing transistor width and drain area. The number of drain regions could also be cut in half by sharing drain regions between vertically neighboring pixels [35].

Appendix A

Appendix A - Implementation of Diff. Architecture with CDS circuit

Fig. A-1 shows the block diagram of the imager. In addition to the pixel array, one row of light-shielded dummy cells was added at the bottom of the pixel array. The column-parallel output circuits consist of CDS circuits, even/odd select, analog buffers, a 128:1 analog mux and an additional analog buffer.

Fig. A-2 illustrates the signal path from pixel to output pads. The charge difference between the pixel and dummy cell is converted to a voltage by the CDS circuit. The voltage output of the CDS, free from the effects of the parasitic current, is muxed by the even/odd select. If the selected pixel is from an even column, signal *even* is asserted and the positive voltage output passes through a p-type transistor and the negative voltage output passes through an n-type switch. Conversely, if the selected pixel belong to an odd column, signal *even* is low. The positive voltage output, which is now lower than the negative output, goes through an n-type switch instead.

The signals are then driven by two source followers of opposite polarity. The p-type follower level shifts the low signal to a voltage $V_{TP} + \Delta V$ higher than the input. Similarly, the n-type follower shifts the high signal to a voltage $V_{TN} + \Delta V$ lower than its input.

The outputs of the source follower then go through a couple of CMOS switches when they are selected for readout by the mux. The mux outputs are driven to the output pads

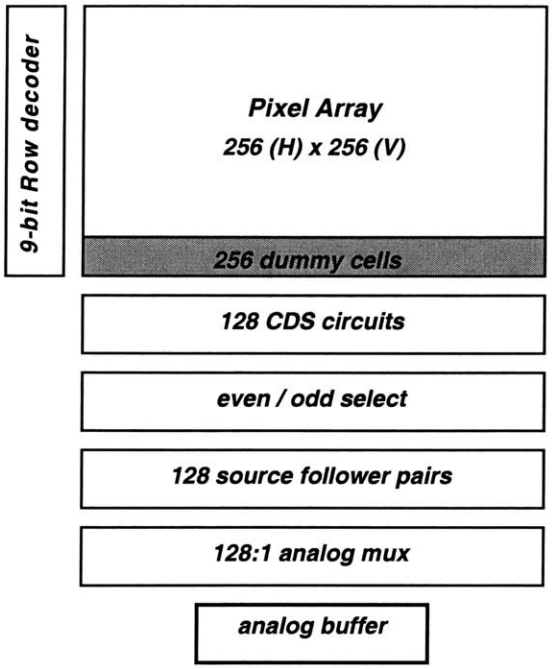


Figure A-1: Block diagram of differential passive pixel imager with CDS circuit.

by a second pair of analog buffers. The signal coming from the n-type source follower now gets shifted back down by a p-type source follower. Similarly the signal that was previously driven by a p-type source follower is now driven by an n-type source follower.

A.0.1 Pixel Design

An N-well photodiode was chosen over an N-diff photodiode for its higher quantum efficiency and lower dark current. Fig. A-3 shows the pixel layout in a $0.6\mu m$ CMOS technology. The white region represents the N-well photodiode and the black region shows the poly gate of the row select transistor. The pixel measured $20\mu m$ on the side and had a fill factor of 54 %. Fill factor was sacrifized by choosing the N-well photodiode due to the stringent N-well separation rules. A passive pixel with an N^+ diffusion photodiode in the same technology and pixel area would result in a fill factor of 87%. This high fill factor was traded off for the improved response of the N-well photodiode.

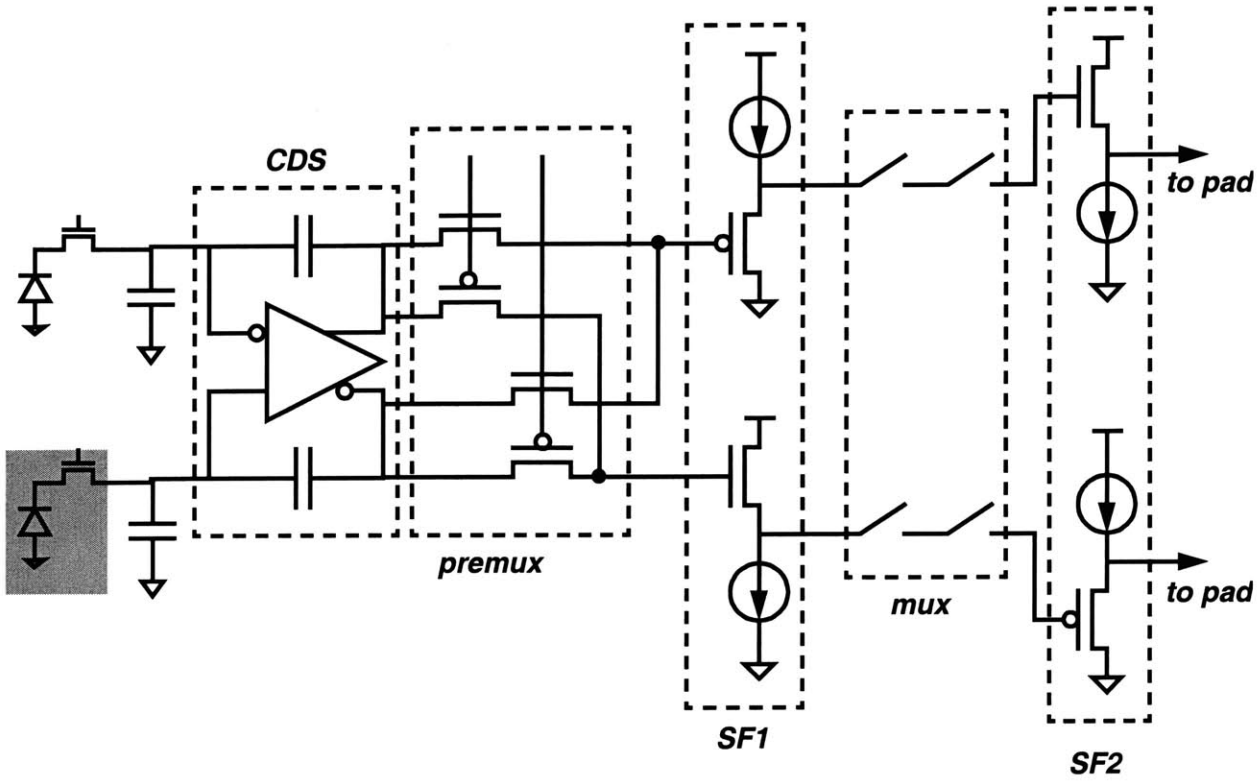


Figure A-2: Signal path of analog passive pixel imager with CDS circuit.

A section of the pixel array can be seen in Fig. A-4. The pixels are interlaced in order to prevent word lines from crossing.

A number of design rules had to be violated since a standard CMOS process does not allow the construction of abutting N-well and N-diff regions. The following list provides a summary of the design rule violations and other considerations for designing a pixel with an N-well photodiode:

- The hot N-well to N-well spacing rule prevents the depletion regions of the two N-wells from shorting together. This rule is designed for a worst-case scenario where the reverse-bias of the N-well to P-sub junction is V_{dd}. Depending on the reverse-bias of the photodiode, this rule can be relaxed to the cold N-well spacing rule.

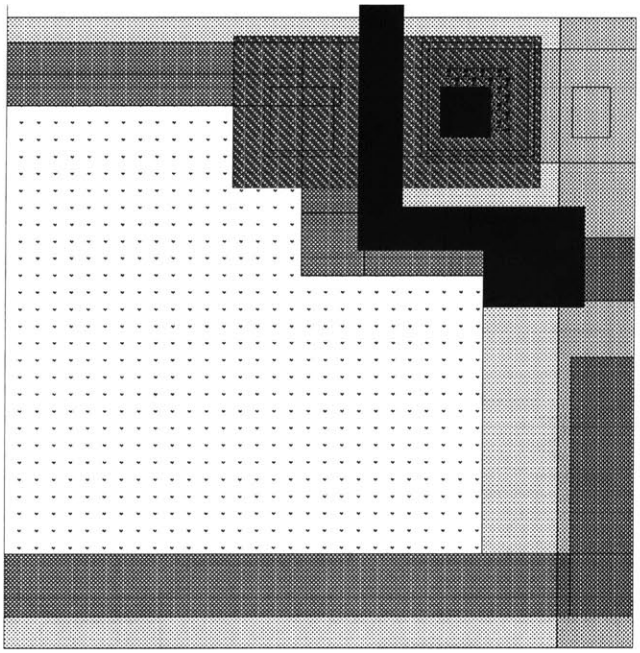


Figure A-3: Passive pixel layout with N-well photodiode

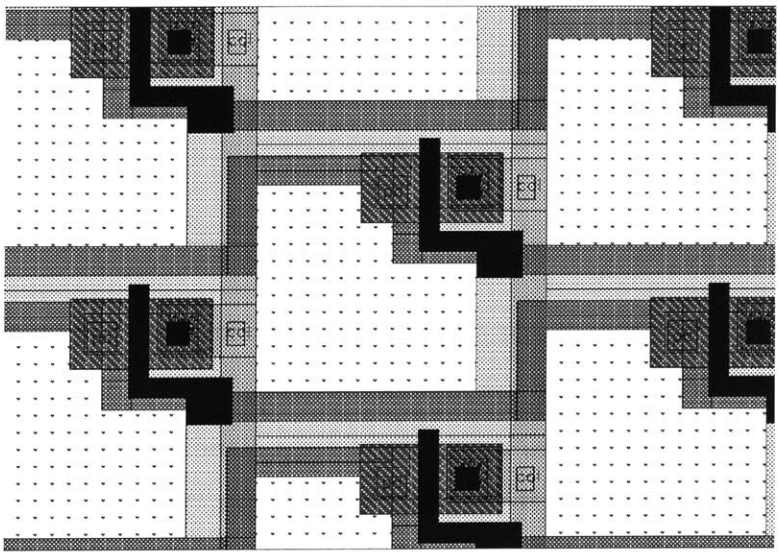


Figure A-4: Section of passive pixel array

- The N-well to N-diff spacing rule is similar to the previous rule since it prevents any shorts between the depletion regions. Furthermore, this rule is designed to prevent latch-up in digital CMOS circuits. Since the pixel array does not contain any p-type transistors, latchup is not a problem. The rule can then be relaxed to the cold N-well

to N-diff spacing.

- While there is no rule for the minimum spacing between N-well and gate poly, we must prevent the N-well from expanding under the poly gate and shorting the source and drain. This would result in a depletion mode device, which is highly undesirable for a row select transistor. In general, the cold N-well spacing rule was divided by two and considered to be the maximum N-well expansion.

- The contact to the N-well, formed by an N-diff overlap over the N-well, needs to be large enough to allow some tolerance in mask shifts. For instance, if the N-well mask shifts slightly to the left and the N-diff mask shifts slightly to the right, the overlap between the N-well and N-diff might disappear. One minimum gate length is enough to prevent this problem from taking place.

A.0.2 CDS Design

Fig. A-5 shows the schematic of the CDS circuit. Six different clocks were required to implement the CDS function. N-type transistors were used as switches wherever possible, in order to minimize the area and number of signal inversions. The only place where a CMOS switch was absolutely necessary is the node between the feedback capacitor and the opamp outputs, which are bound to swing higher than $V_{dd} - V_{TN}$.

The switches controlled by fin and connecting the opamp inputs and the feedback capacitors, were necessary to minimize any signal-dependent charge injection during the third stage of the CDS circuit. Had these switches not been included, the switches controlled by fout would need to be open during phases 1 and 3 and closed during phases 2 and 4. The charge injected into and out of this device is signal-dependent and would introduce a gain error into the CDS. By using input switches controlled by fin, charge injection still exists, but it is an offset error that is rejected as common mode to the first order.

A.0.3 Programmable Analog Buffers

Source followers (Fig. A-6) were used to buffer the high capacitance of the mux from the opamp outputs. Rather than increasing the bias currents in 128 opamps to enable each one to drive the mux capacitance, a pair of source followers with on/off control was used in an effort to conserve power.

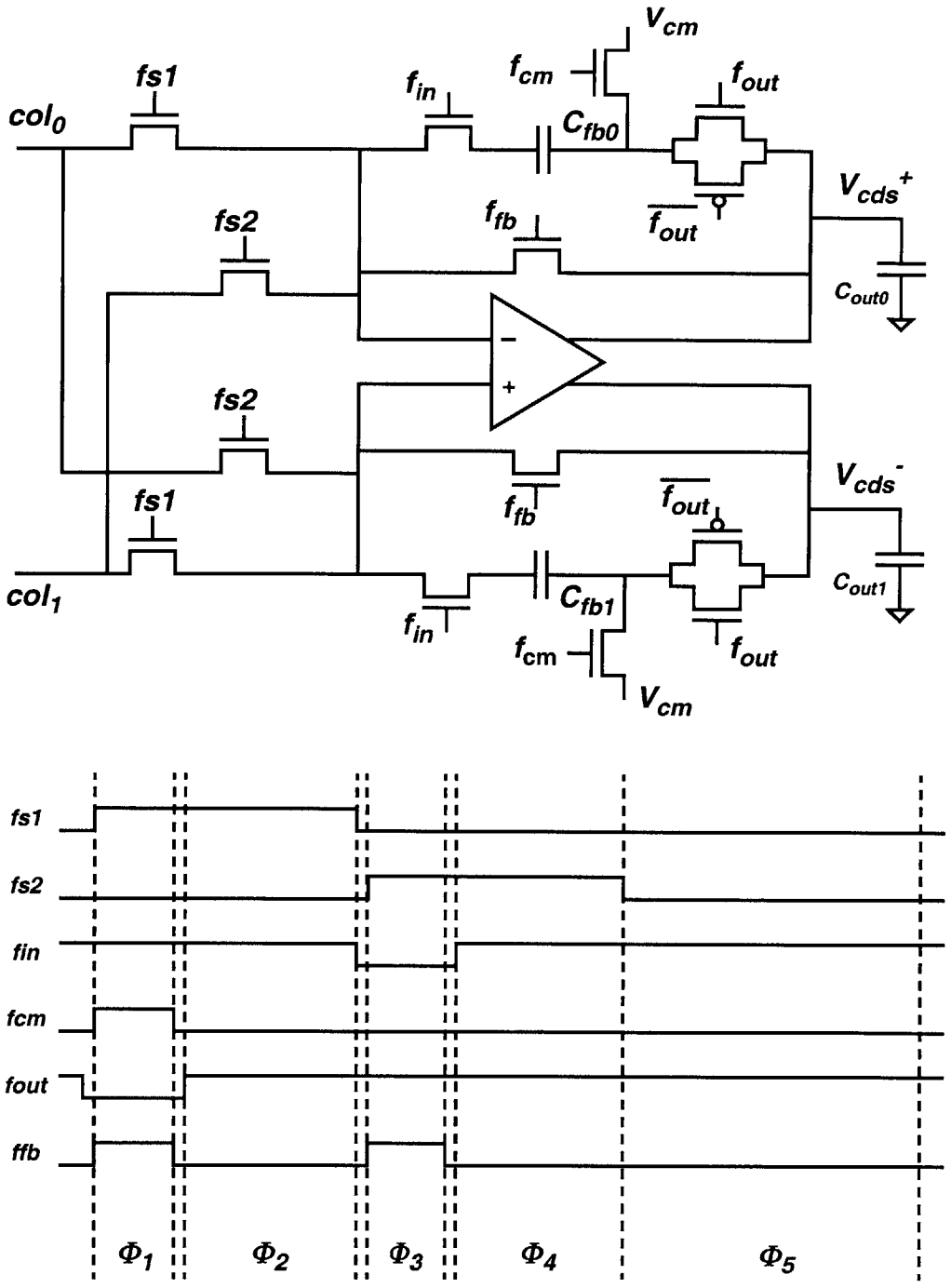


Figure A-5: CDS Schematic Diagram.

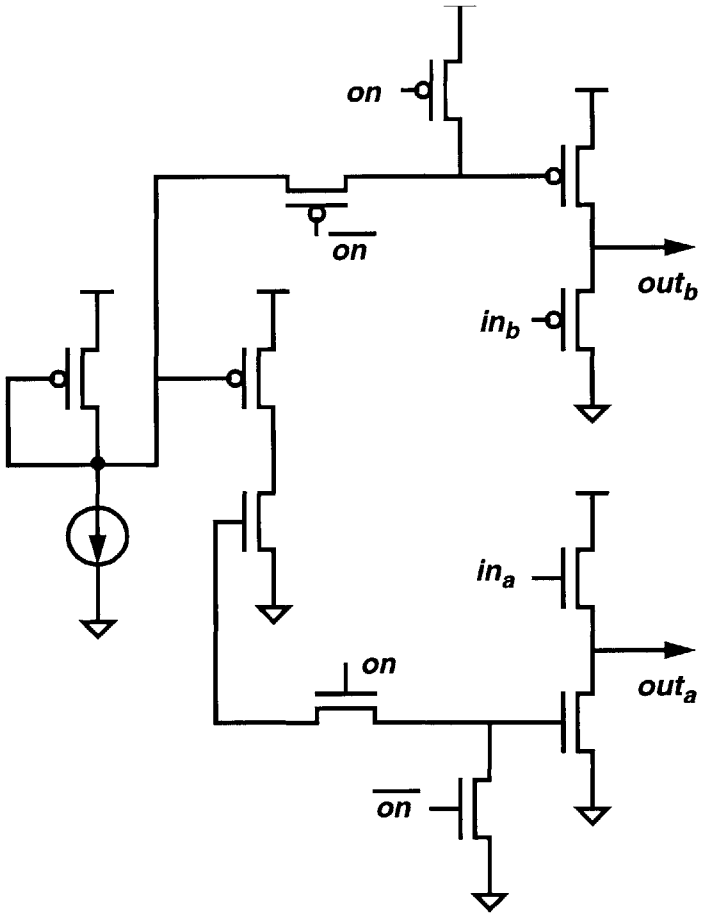


Figure A-6: Programmable Analog Buffers.

The source followers were separated into 16 groups of 8. As the mux scanned the array, one group of source followers would be activated for a short time prior to being selected. In this way, only two groups of 8 source followers, or 16 source followers total, were activated at any one time.

A.0.4 Analog Mux

The analog mux was divided into two parts: 8 16:1 muxes followed by a single 8:1 mux as illustrated by Fig. A-7. The top figure describes an 8:1 mux and the bottom figure shows a block diagram of the entire mux. In the upper diagram, each CMOS switch is controlled by an AND function of 3 address bits. Only one switch is selected at one time connecting that particular signal wtih the output. This scheme was designed to reduce the capacitance

seen by each buffer. Had a single 128:1 mux been used instead, each buffer would need to drive the diffusion capacitance of 128 transistors.

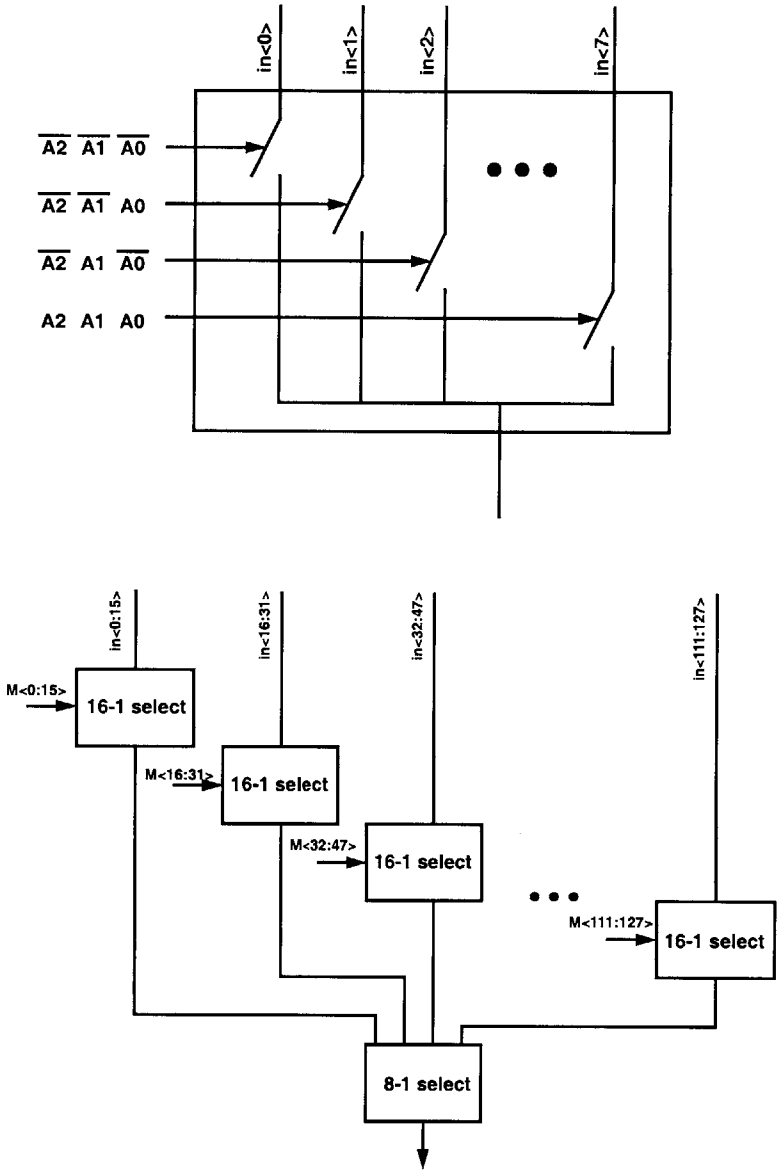
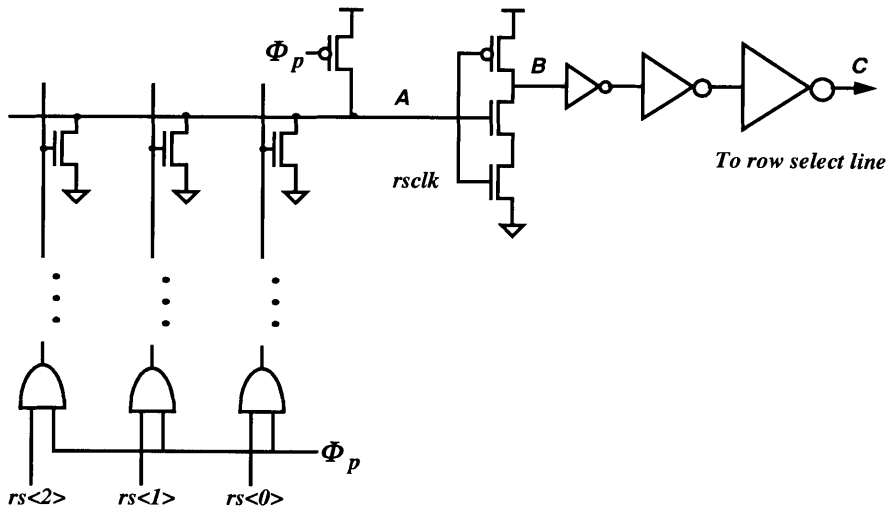


Figure A-7: Analog multiplexer.

A.0.5 Row Decoder

The schematic of a 3-bit row decoder and driver is shown in Fig. A-8. The cycle starts when ϕ_p is low and node A is precharged to V_{dd}. As soon as ϕ_p goes high, $rs < 0 : 2 >$

drive the gates of the select transistors with the assigned word. If all bits are low, node A stays high. When $rsclk$ pulses high, node B will be pulsed low, consequently driving node C to be pulsed high.



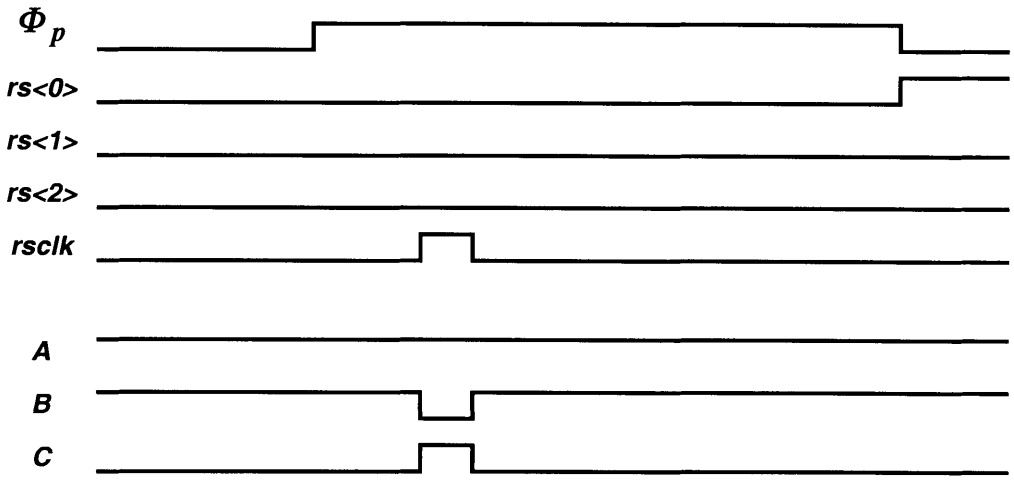


Figure A-8: Row select decoder and driver circuit.

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