Analysis of Magnetic Random Access Memory Applications

by

Allison Hernandez

B.S. Electrical Engineering (2001)

Bucknell University

Submitted to the Department of Materials Science and Engineering
in Partial Fulfillment of the Requirements for the Degree of Master
of Engineering in Materials Science and Engineering

at the

Massachusetts Institute of Technology

June 2002

© 2002 Massachusetts Institute of Technology
All Rights Reserved

Signature of Author.....
Department of Materials Science and Engineering
May 10, 2002

Certified by.....
Caroline A. Ross
Associate Professor, Department of Materials Science and Engineering
Thesis Supervisor

Accepted by.....
Harry L. Tuller
Professor of Ceramic and Electronic Materials
Chair, Departmental Committee on Graduate Students
Department of Materials Science and Engineering

MASSACHUSETTS INSTITUTE
OF TECHNOLOGY
JUN 17 2002
LIBRARIES

ARCHIVES

Analysis of Magnetic Random Access Memory Applications

by

Allison Hernandez

Submitted to the Department of Materials Science and Engineering
on May 10, 2002 in Partial Fulfillment of the Requirements
for the Degree of Master of Engineering in
Materials Science and Engineering

ABSTRACT

Magnetic Random Access Memory (MRAM) is considered to be the most viable option for nonvolatile memory in the computer industry. This need for nonvolatile computer memory has resulted in the dramatic evolution of MRAM technology in the past ten years. Currently in the latter stages of development, emphasis is being put on experiments concerning optimization of density and reduction of the switching fields of the magnetic elements.

Applications of MRAM technology are currently being explored by companies who seek to obtain relevant intellectual property in those areas. Once research is completed, companies must create a business plan that recognizes the initial, breakthrough markets and implement technology integration accordingly.

Thesis Supervisor: Caroline A. Ross
Title: Associate Professor of Materials Science and Engineering

TABLE OF CONTENTS

PART ONE: TECHNOLOGY ANALYSIS

For the last twenty years, improvements in Complementary Metal-Oxide Silicon (CMOS) technology have exceeded the expectations of manufacturers in the computer industry. The ability of Dynamic Random Access Memory (DRAM) components to double their density every eighteen months[1] has allowed the personal computer market to exceed the needs of the everyday consumer. These days, consumers buy new computers not because they need the top-of-the-line computer in order to check their email or surf the web, but because they want one. Electronics manufacturers have been able to find a way to manufacture Dynamic and Static RAM components affordably, so that even the most up-to-date computer systems may be purchased by consumers. But despite the fact that DRAM has become so reliable and affordable, there is one aspect of functionality that it cannot provide: nonvolatility.

In order to maintain data stored, DRAM components require a constant power source, and hundreds of rewrite cycles per second. When the power source is turned off, the data is lost, and must be rewritten upon restoration of the power. This problem is of particular concern to the portable electronics industry, where power efficiency and optimization of battery life is of utmost importance.

Magnetic RAM is considered to be the most viable option in the search for a nonvolatile memory solution. A combination of traditional CMOS circuitry and magnetic memory stacks, the nonvolatility of MRAM provides the low power consumption that is sought after by the portable electronics industry. The drawback to nonvolatility, however, is the added complexity that makes MRAM difficult to implement into industry.

There are many attributes of Magnetic Random Access Memory, but in order to fully understand the impact that the technology could have on various industries, one must understand the technology itself. The history and current ambitions of MRAM technology are explained in the following pages.

EARLY MRAM DESIGNS

The first step in the quest for MRAM technology was the discovery of Anisotropic Magnetoresistance (AMR)[2]. This discovery found that a single layer of NiFe exhibited a magnetoresistance when in an applied magnetic field. A change in the magnetization direction of the material within the applied field would induce a change in the overall magnetoresistance of the material itself. Although regarded as a significant principle for some time, the small resistances recorded (only on the order of 2-3%) were overshadowed by the discovery of Giant Magnetoresistance, or GMR[3,4] in the early 1990's. This technology used an alternating magnetic and non-magnetic layered design. The information would be stored in the form of a magnetization state of one of the magnetic layers, and then the relative resistance of the magnetic stack could be measured, and the bit could be detected. The current would be applied across the element (parallel to the plane of the chip) using wires at sides of the individual element, and would be read by detecting the relative resistance of the magnetic stack. This multilayer design was not optimal for MRAM implementation, however, because the fields required to switch the magnetization of the individual stacks was too high.

But GMR structures were just the beginning. The next step in the process of improving MRAM structures was the Pseudo-Spin Valve structure (PSV)[5,6]. This structure most closely resembles the modern MRAM model. The structure is depicted in Figure 1. There is a non-magnetic metallic layer sandwiched between two magnetic layers that are used to read and write the information to the cell. The bottom layer in this diagram is considered the hard, or information storage layer, and the top magnetic layer is the soft, or readout layer of the cell. The layers are usually made to be of a different thickness so that they will have different switching fields due to the resulting difference in shape anisotropy. The Magnetoresistance (MR) of these stacks typically ranges between 6% and 9%.

The information is written to the cell by flowing a current through the write wire. This current induces a field within the magnetic material that is strong enough to change the magnetization of the hard layer. The cell is written with a 1 if the magnetic field points left, and a 0 when the field points right. The cell is read by applying a sense current (not included in Figure 1), in conjunction with a positive and negative current through the digit, or read wire. The currents are chosen such that the combination of the sense current and the digit current is sufficient to switch the soft layer, but not the hard layer. The relative resistance change with respect to direction of the read current is read by a transistor.

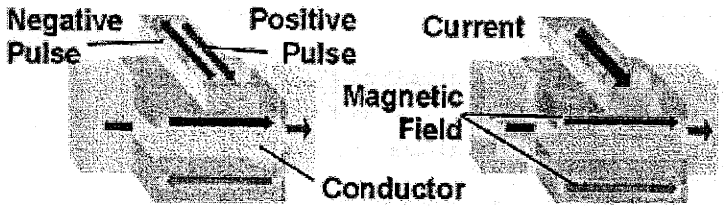

Figure 1: Diagram of a PSV Cell
Scientific American, The Magnetic Attraction, May 1999

CURRENT MRAM DESIGNS AND EXPERIMENTS

Current MRAM technology utilizes Magnetic Tunnel Junction (MTJ), with a Current-Perpendicular-to-Plane (CPP) format[7-10]. A schematic of the structure is shown in Figure 2. The structure is similar to that of a PSV cell. The top magnetic layer is used for information storage and reading. In this particular case, the magnetic layer is made up of NiFe, but a Co alloy may be used as well, and should be between 2nm and 4nm thick. The oxide layer that separates the two magnetic layers is usually formed from a non-ferromagnetic 3d, 4d, or 5d transition metal that is reacted with a N or O plasma to form the insulation. Because the thickness of the oxide layer affects the relative resistance of the magnetic stack substantially, this layer needs to be made in a very precise manner, with good uniformity and a thickness on the order of 1.0-1.5nm. The antiferromagnetic layer (in this case IrMn) is used to pin the bottom layer to a certain magnetization. This bottom layer is used as a reference to measure the resistance of the cell. The cell resistance is high or low depending on the relative

magnetization directions of the free (soft) layer with respect to the pinned (hard) layer. As in the PSV cell, the field due to a current through the contact layer is used to write information to the soft layer, but unlike the PSV cell, the seed layer is used for an electrically isolated current to hold the pinned layer to a certain polarity.

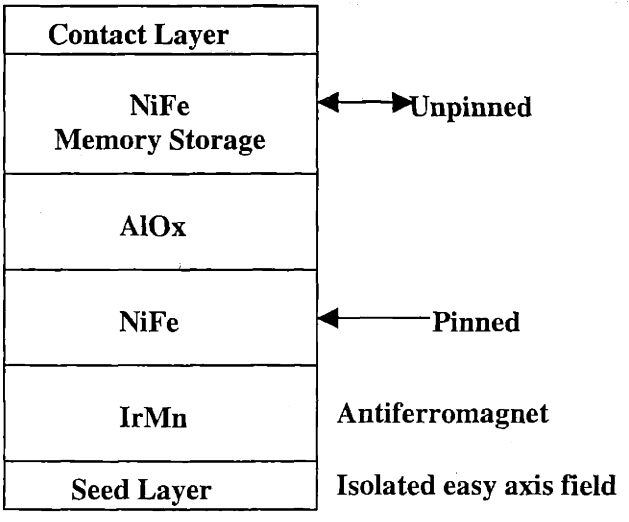

Figure 2: Construct of a Modern MRAM Structure

After the necessary circuitry and metallic interconnects are made on the silicon substrate using conventional IC fabrication methods, the magnetic stacks are formed by patterning the elements onto the substrate using a combination of Sputtering, Electron Beam Lithography and Ion Milling[11-13]. The memory structure is built on a silicon substrate. First, the metallic layers have to be sputtered onto the substrate. The patterned silicon is put into a vacuum chamber with the target material that is to be sputtered. The target is negatively biased, and then bombarded with positively biased argon atoms. The target atoms are thus ejected from the target and accelerated towards the substrate where they form into a thin layer on the order of a few atomic layers.

The next step in the array formation is optical lithography. In this step, the surface of the silicon is coated with a resist layer, and a pattern of light is shone on the surface, exposing the resist layer in the

desired pattern. Smaller features can be made using e-beam lithography. Although optical lithography can be expensive (as feature size decreases, optical lithography costs increase), the high wafer throughput that the process provides compensates for the cost. Alternative technologies such as e-beam lithography have been considered for MRAM processes because of their high accuracy and line width control, but cannot be implemented in a large scale manufacturing line because of very low throughput.

The third step in this patterning process is ion milling. This step is used to etch through the magnetic layers in the stack to expose the substrate and make the desired cell pattern. A diagram of the patterning process is shown below in Figure 3.

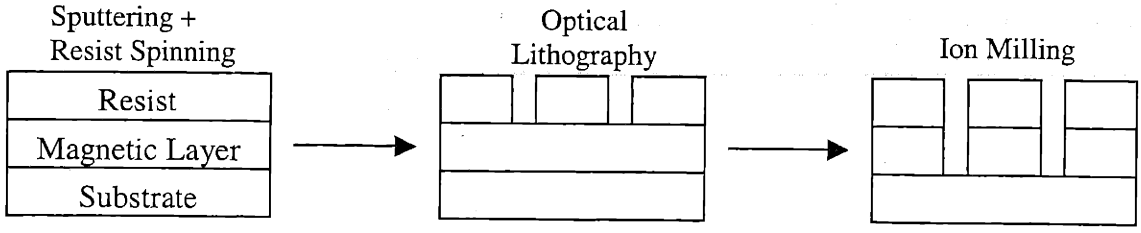

Figure 3: Patterning Process for MRAM Cells

Each cell is patterned onto a grid of crossing write wires [14]. These wires enable the cell to be written when both the row and column lines are activated by write currents. When only the row or column line is activated, the cell is what is referred to as "half-select mode" and does not switch magnetization states because the field induced by only one current is not sufficient to switch the cell. The cell switching, or coercive fields that the soft layer requires is determined during manufacturing, and the current and field parameters are set accordingly. A schematic of this writing mechanism is shown in Figure 4.

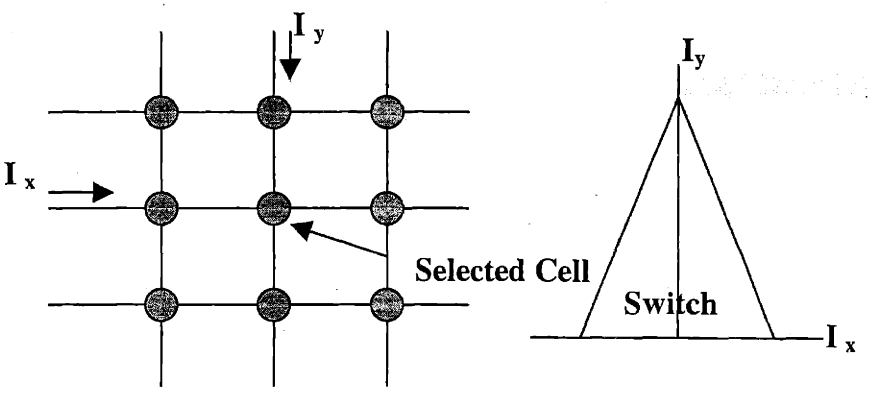

Figure 4: Schematic of Cell Write Mechanism
J. M. Daughton, Magnetoresistive Random Access Memory

One of the current barriers to implementing the MRAM design mentioned previously, is the problem of finding the right aspect ratio (the ratio of cell length to cell width) and layer sequence for the individual magnetic elements and the spacing between the elements[15,16]. Magnetic interactions between adjacent elements can cause switching errors and will therefore compromise the integrity of the memory chip itself. This magnetic behavior is influenced by the shape, size and layer thickness of the magnetoresistive stacks. There is much research being performed with respect to this matter, for the result will determine the densities of the chips that can be manufactured.

One such experiment is being carried out by Professor Caroline Ross at the Massachusetts Institute of Technology. The group worked with PSV stacks of NiFe (6nm)/Cu (4nm)/Co (4nm)/Cu (4nm) that were sputtered in the presence of a magnetic field. The purpose of sputtering the layers in a magnetic field is to orient the magnetization of the hard layer to a certain direction. Typically, switching fields for a stack of this nature should be about 10 Oe for the soft NiFe layer and 40 Oe for the hard Co layer in an unpatterned control stack. The film was first patterned into circular elements with eight and ten μm diameters. The results showed that the magnetization that was induced during the sputtering process was preserved, meaning that the circular elements still had a preferred magnetization direction. The hysteresis loop for the experiment is shown in Figure 5. The experiment also showed that the field at which the soft layer switches increases as the size of the cell decreases (when diameter was decreased

from 10μm to 8μm). This is not a positive result considering the implications. As the feature size decreases, the amount of current needed to run the cell will hopefully scale down accordingly. The increase in field (and therefore current) needed to reverse the smaller cell will undoubtedly cause problems with thermal stability in the long run.

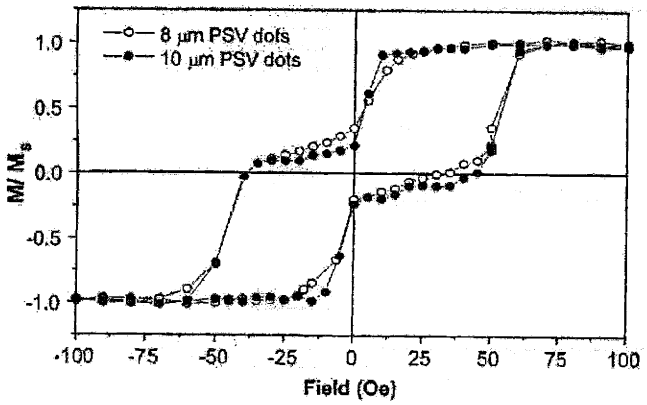

Figure 5: Hysteresis loop measurements of a large-area array of NiFe (6nm)/Cu (6nm)/Cu (4nm) square PSV elements, with widths of 8 μm and 10 μm. The applied magnetic field was parallel to the induced easy axis.
Reproduced with permission from Caroline A. Ross

The next experiment that was carried out used patterned ellipses with dimensions of 80x140nm at 125nm intervals. The magnetic behavior of the ellipses was measured once with the field parallel to the cell (in the direction of the long axis), and once with the field perpendicular (parallel to the short axis of the ellipse). For the field parallel to the long axis, the magnetization of the two layers is aligned anti-parallel at zero applied field. The switching fields for this field orientation was –1500 Oe for the hard layer and 600 Oe for the soft layer. The study found that the interaction between the dots along the short axis was negligible compared to the actual switching fields, meaning that the dots do not interfere with one another in this direction. It concluded that, overall, the cells could scale down to 100nm, but that the reduction of the switching fields would be a great challenge.

A theoretical study, conducted by Jian-Gang Zhu and Youfeng Zheng[17,18], concluded that the difference between the switching fields in various shapes of memory elements had to do with the angles

of the edges in the elements themselves. The study found that the switching field in a rectangular cell (length 0.2μm and width 0.1μm, aspect ratio of 2) was approximately 125 Oe less than that of an elliptical cell of the same dimensions and aspect ratio, meaning that cells with sharp ends have smaller switching fields that those with rounded edges. The requirement for cell corners with sharp angles poses a manufacturing problem because there is more of a chance for variation in the angles during processing. This prevents the manufacture of uniform chips. Another difficulty that Zhu and Zheng propose is that of critical density. Cells containing tapered edges are much larger than cells with rounded edges, therefore preventing higher densities. Problems such as these must be overcome before progress can be made.

One of the solutions that are currently being proposed is that of vertical magnetoresistive random access memory, or VMRAM. The design scheme is similar to that of a Magnetic Tunnel Junction (MTJ) MRAM cell, with alternating layers in which the current flow is perpendicular to the plane of the film, but the layers are formed in a ring shape. Bits are stored by magnetizing the rings in clockwise or counterclockwise directions. Like MRAM, the cells are connected in series, forming a bit line. In the case of VMRAM cells, the word lines are in pairs above and beneath the memory cells and are oriented orthogonal to each other. The current in the word lines for each pair are of equal magnitude, but opposite direction. This causes a radial magnetic field in the plane of the layers. The current through the bit line, however, causes a circular magnetic field in the plane perpendicular to the layers. Both fields aid in the switching of the memory cell. The cell is read by applying two current pulses in opposite directions through the bit line, thereby switching the soft layer of the selected memory cell and reading the magnetoresistance between the soft and hard storage layers. This dynamic readout scheme is much like that of the pseudo-spin valve cell explained in the previous section, and allows for one transistor per bit line. An illustration of the VMRAM cell is shown in Figure 6.

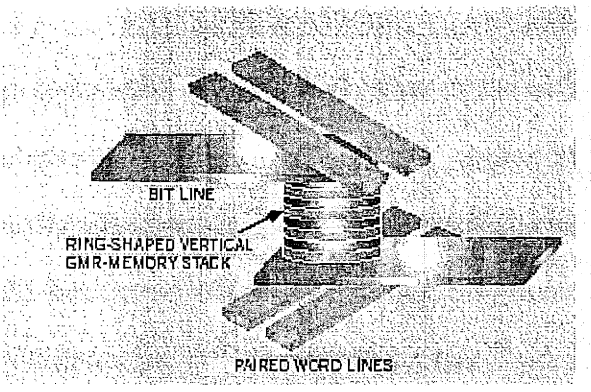

Figure 6: Illustration of aVMRAM cell
Exotic Memories, Diverse Approaches,
www.ednasia.com

There are many interesting advantages to the VMRAM design that improve upon the traditional MRAM cell design. The first, and most obvious improvement was the discovery that the magnetoresistance of VRAM surpassed that of MRAM by approximately 50%. Next, researchers claim that because of the circular magnetization pattern in the elements, the external field is zero and the interaction between adjacent cells is negligible. The circular field mode also allows for increased thermal stability because it decreases the tendency for thermally induced demagnetization. This means that manufacturers can decrease the dimensions of the cells even further without affecting the switching fields.

Although the VMRAM design seems to be an improvement on the traditional MRAM design, there are disadvantages as well. Manufacturing tolerances of the VMRAM arrays may relax with respect to the aspect ratio and spacing of the cells, but the cells require a perfect ring shape in order to function properly. Currently, there is no process capable of manufacturing these cells on a large scale such that they would be of a tolerable uniformity. Also, the VMRAM concept is much more complex than that of the traditional MRAM design, and therefore will be much harder to implement.

REQUIREMENTS FOR SUCCESS

To be competitive in the world market, MRAM technology has to meet certain criteria: it must have higher read/write speeds, comparable memory density, it must be scalable for future generations, and have low operation voltages. MRAM developers are hoping to be able to produce chips with speeds of five to ten nanoseconds, and DARPA (in conjunction with Nonvolatile Electronics) is setting their sights on a three nanosecond chip[19]. Already there have been major breakthroughs with respect to the memory density of this technology. A 256Mb chip has already been developed by IBM, and there are currently efforts being made within industry to improve upon this due to competition from other technologies such as FLASH RAM and Ferromagnetic RAM[20]. Although MRAM will not be able to compete with the densities of current DRAM technology, scientists are hopeful that this technology will be dominant in those applications that require nonvolatility and low power consumption.

PART TWO: APPLICATIONS ANALYSIS

The concept of Magnetic Random Access Memory has come to mean many things to many different companies and/or government agencies. Researchers have tailored MRAM technology to be a niche memory solution that can substitute for current memory technologies in many industrial applications. In this section, an overview of different applications for MRAM technology will be given, as well as an analysis of what applications are the most likely choices for implementation and why. Supporting evidence will be given.

RANGE OF POSSIBLE APPLICATIONS

Based on the extensive body of literature available from throughout industry and academia, the first and most obvious application of MRAM technology is in computer systems and portable electronics. This application ranges from high computation machines and industrial computers that must perform millions of computations per second, to personal machines such as desktop or laptop computers and PDAs. These systems would take advantage of many MRAM characteristics such as higher memory density, high speeds and of course, non-volatile memory. The portable electronics industry would also benefit greatly from the low power consumption and nonvolatility that MRAM allows. The smaller chip size would allow multi-function portables, such as the dual-function PDA/Cell Phone, to have a more compact package, a feature that is highly desirable in the portable electronics market. This application has important implications for both the consumer market, as well as government/military markets such as GPS systems and satellites.

Another application for GMR technology is in the sensors market. Although the MRAM technology itself is not of great use in this arena, the capability of making nano-scale MR devices is of great consequence. Sensors utilizing magnetoresistance can be integrated in to Aerospace, Biosensor, Global Positioning, and automotive systems, as well as many others. One such sensor is the Bead Array counter (BARC) that is being developed by Dr. R. J. Colton at the Naval Research Laboratory. A BARC

sensor chip is displayed in Figure 7[21,22]. This particular sensor is used to detect pathogens in the blood. The plasma that is to be tested is coated onto the sensing pad that is composed of many magnetoresistive cells. A metallic bead is then coated with a control plasma containing the pathogen that is to be detected. The bead is then placed onto the sensing pad. If the pathogen that is coated onto the bead is, in fact, in the plasma that has been coated onto the sensing pad, it will attach itself onto the bead, therefore pulling the bead closer to the pad and creating a magnetic field. This is just one type of sensor that uses MRAM elements to improve its characteristics. Like computer systems, these applications can be utilized by both the consumer and government/military markets.

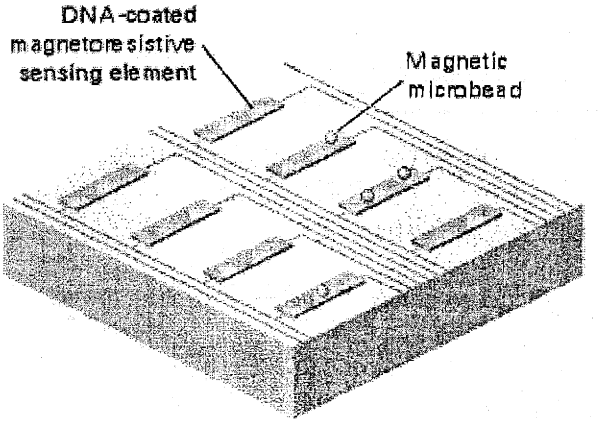

Figure 7: Design of the Bead Array Counter sensor developed by NRL
R.J. Colton, The Bead Array Counter (BARC): A Multi-analytic Biosensor on a Chip

A third application is that of Micro Electro-Mechanical Systems (MEMS)[23]. A MEMS system itself, this technology may be used to create stand-alone MEMS structures such as micro insulin pumps in the future. Closed loop biomechanical applications such as this will benefit from the nonvolatility, the new fabrication techniques that will evolve out of MRAM research, as well as its nano-scale dimensions. These devices are implanted into the body for long-term use, and require logic systems in order to carry out the necessary chemical synthesis. In this case, the functionality of the micro insulin pump will have to exceed twenty years in order to fulfill the long-term expectations of the device itself, making the

nonvolatility of MRAM technology imperative to implementation. Although not on an immediate timeline for implementation, products such as these will be looked to in the future of biomechanics.

MOST LIKELY CHOICES FOR COMMERCIALIZATION

Although there are many useful applications of MR technology, not all of them will see the push towards commercialization and implementation. The two applications that will most likely see a big push towards commercialization are computer systems/portable electronics and magnetic sensors. Both applications cover a broad range of both consumer and government needs, and are the focus of most of the research that is going on about MRAM today. According to the Mc Kinsey Diagrams, they are both new technologies that can be implemented in old markets. This indicates that the success of the new technology is driven by cost, meaning that if the specific application of MRAM technology can compete with the old technology in terms of overall cost, then the paradigm will shift. The Mc Kinsey diagram for both applications is shown below in Figure 8. Further supporting evidence will be shown in the sections to follow.

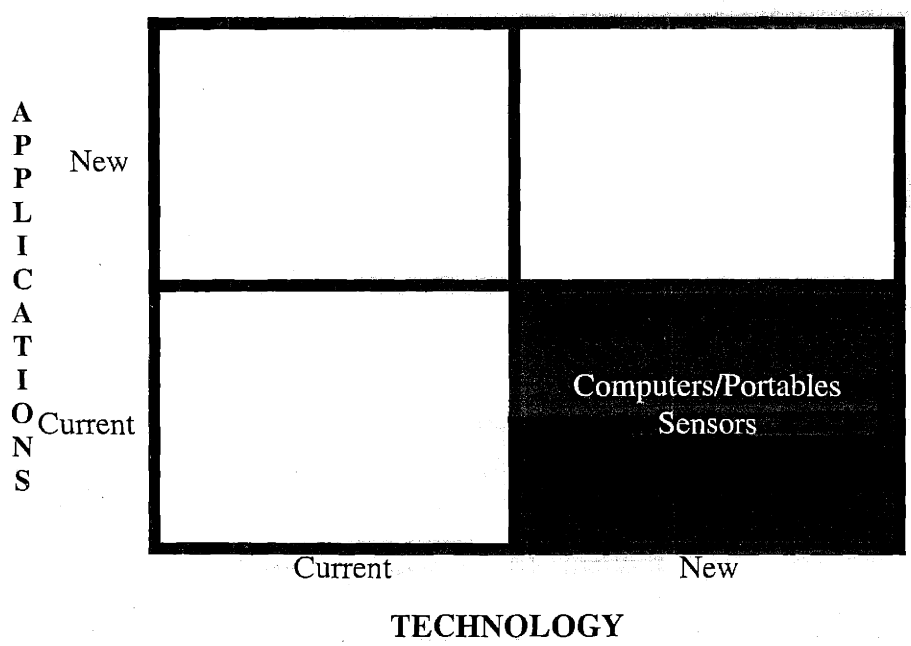

Figure 8: Mc Kinsey Diagram for Viable MRAM Applications

In contrast, MEMS applications are not likely to be seen on the commercial market in the near future. Although the technology is currently being researched, stand-alone MEMS systems are still in their infancy. In terms of its place in the market, MRAM integration into MEMS systems is a new technology fitting into a new application. According to the Mc Kinsey diagram, this application is in the "death" zone for implementation. Therefore, it is of little consequence for this analysis. The diagram for MEMS applications is shown in Figure 9.

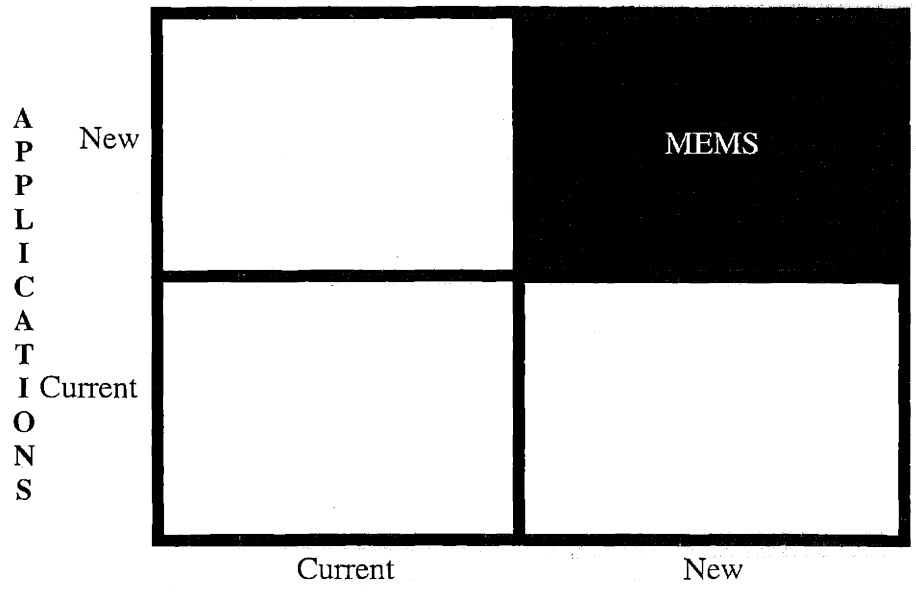

Figure 9: Mc Kinsey Diagram for Non-viable MRAM Applications

COMPETING TECHNOLOGIES

Although MRAM is being considered as a viable solution to the problem of volatile RAM, there are other alternatives that are being explored as well. Besides the entrenched DRAM technology that holds a virtual monopoly in the computer industry for computer RAM, there are two other technologies

that are emerging as possible competitors for MRAM in the non-volatile RAM market, namely FlashRAM and Ferromagnetic RAM (Fe RAM). Both of these technologies already have a strong presence in IC and smart card technology, but are currently being looked at for possible applications in the personal computer and portable electronics industry.

Flash memory technology is a solid-state storage device that uses two transistors (floating gate and a control gate) separated by an oxide layer[24-27]. The floating gate is connected to the word line through the control gate. If the contact between the two gates is intact, then a one is written to the cell. If the connection is broken, then a zero is written in the cell. To write a zero, a charge of ten to thirteen volts is applied to the floating gate through the bit line. As the charge goes through the bit line, it enters the floating gate and drains into ground. As a result of this, electrons are pushed through the floating gate and into the other side of the oxide layer. These electrons act as a barrier between the two gates, and therefore the connection between them is severed. The cell is read by a sensor that monitors the amount of charge flowing between the gates. If the amount of charge flow is above 50% of the set threshold, a one is written, a zero if it is below. The cell is erased by applying a large electric field to the chip. A schematic of a FlashRAM cell is illustrated in Figure10.

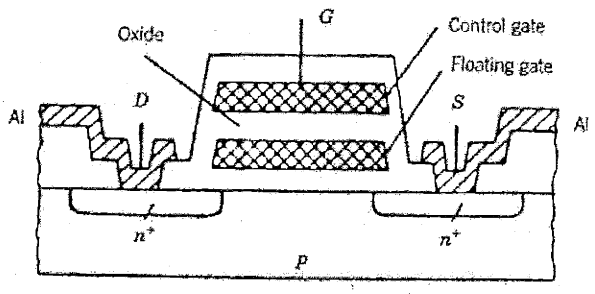

Figure 10: Simple Model of a memory cell with a control gate and floating gate.
Sorab K. Ghandhi, VLSI Fabrication Principles, Second Edition, Copyright ©1994.

Although there are advantages to using Flash technology such as fast block erasing and lower power consumption in comparison to DRAM, there are some serious disadvantages with respect to actual

RAM functions. One drawback to the design of Flash memory is its limited write endurance. In order for computer memories to be useful, they must be able to withstand at least 10^18 switching cycles[28]. FlashRAM cells, however, have thus far only shown write endurances of up to 10^6 cycles, which is not acceptable at this stage of design. Another problem with the implementation of Flash technology is the high voltages needed to operate and switch the cell's polarity. Currently, 5-13V is needed for reading and writing functions. This does not compete with the extremely low voltages that MRAM requires for functions that are less than 1V. A third disadvantage is its extremely slow program and erase times at the byte level. When Flash technologies were first implemented, they were designed with the purpose of having block write and erase functions. This gave Flash memory an advantage in products such as digital cameras and video games that utilize quick, mass programming. In contrast, computer RAM requires that memory components program and erase at the byte level, for which Flash does not have the capability. Currently, program times for Flash are on the order of milliseconds, and erase times are on the order of whole seconds. This does not compete with current write and erase times of MRAM which, as stated in Part One, are both in the nanosecond range. Overall, FlashRAM does not yet have the capability to overtake MRAM with respect to non-volatile RAM. MRAM has superior read and write performance, and requires less power to operate.

Another competitor in the non-volatile memory market is Ferromagnetic RAM, or FeRAM[29,30]. FeRAM is also a two dimensional cell, which uses a 1T/1C (one transistor/one capacitor) configuration. The design of the cell is similar to that of DRAM technology, however, the capacitors are made out of ferroelectric material. The materials are made out of ABO_3 Ferroelectric crystals, in which metal ions exist within oxygen ion lattices. The two most common ferroelectric structures are the PZT and the SBT structures shown in Figures 11a. and 11b. The non-uniformity in the lattice caused by the cations allows the metallic element to be polarized when influenced by an external electric field. Because of the configuration of the FeRAM structure, it is extremely compatible with CMOS technology, and can be integrated into circuits fairly easily in comparison to other nonvolatile memories.

The writing scheme for FeRAM technology is fairly simple. +/- Vcc is applied to the ferroelectric capacitor. The word line (WL) is selected, and a zero is written by applying zero volts to the bit line (BL) and +Vcc to the plate line (PL). To write a one, the opposite occurs and the bit line is set to +Vcc, and the plate line to zero volts. The schematic of a ferroelectric cell and writing scheme is illustrated in Figure 12.

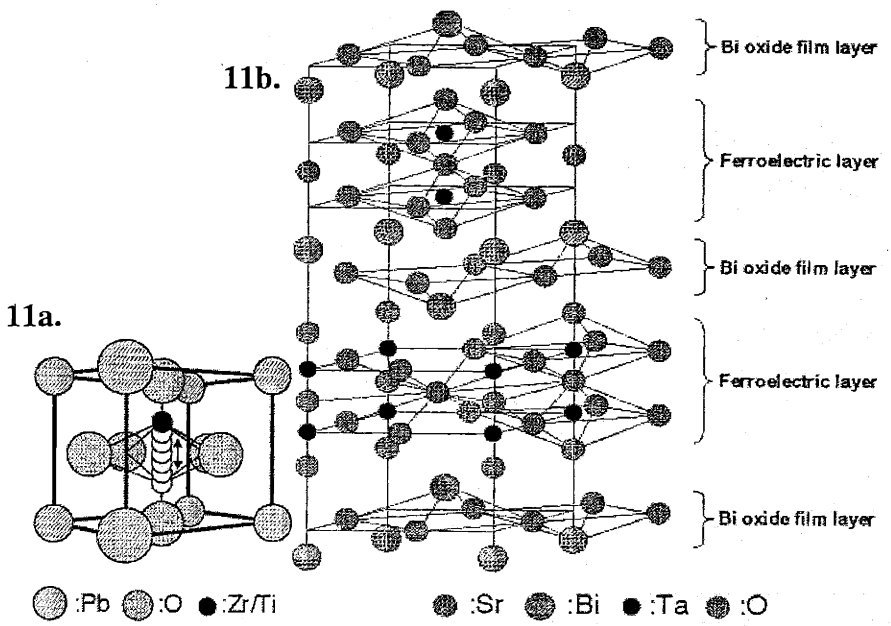

Figure 11: 11a. PbZrO3 or PbTiO3 (PZT) structure,
11b. SrBi2Ta2O9 (SBT) structure of FeRAM technology

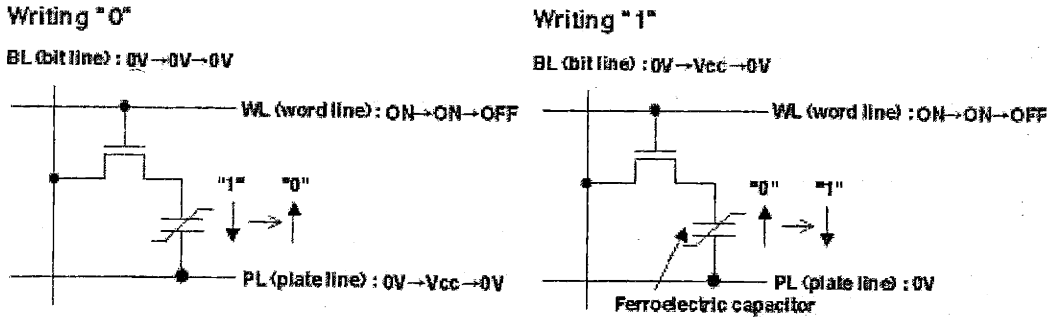

Figure 12: Schematic of a FeRAM cell and writing scheme
FRAM Guide Book, Copyright© FUJITSU LIMITED 2001

Reading the information becomes a bit more complicated, however. In order to read a given cell, the bit line has to be set to zero volts. The word line is selected, and +Vcc is applied to the plate line. This allows the data to be read from the ferroelectric capacitor. If the cell holds a zero, the polarity of the cell is not reversed, and there is no voltage change detected by the sense amplifier on the bit line. If the cell holds a one, however, the polarity of the cell is reversed, and a big change in voltage (VH) is detected. The sense amplifier is tuned so that VH = +Vcc. The cell is restored to its original polarity immediately after the read process. The bit line is charged to +Vcc as a result of the tuning of the sense amplifier, and the plate line voltage becomes zero, which causes a one to be written, as per the original write instructions. A schematic of the read process is shown in Figure 13.

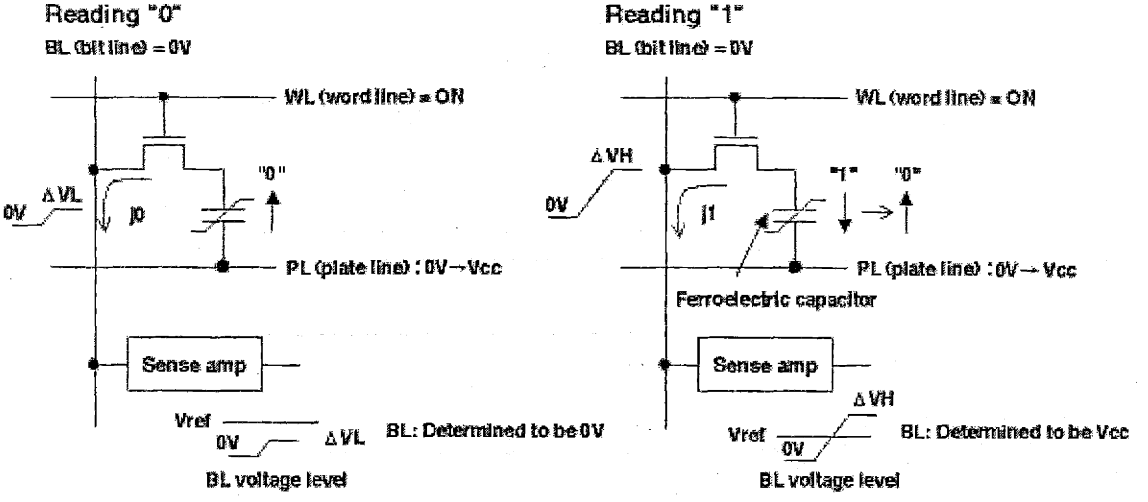

Figure 13: Schematic of FeRAM read process
FRAM Guide Book, Copyright© FUJITSU LIMITED 2001

Unfortunately, it is in this destructive read process that the problems with FeRAM occurs. As stated previously, in order to compete with Dynamic RAM technology, the nonvolatile memory components must be able to have switching endurances of about 10^18 cycles. Currently, FeRAM only has switching endurances between 10^10 and 10^12 cycles, which is not sufficient for RAM purposes.

This condition is further aggravated by the increased polarization switches caused by destructive reading in FeRAM. As a result of its switching limits, FeRAM will not be able to compete with MRAM, which is hoped to have unlimited read/write endurance[31].

Although theoretically, MRAM is considered to be a much better nonvolatile memory option than FlashRAM or FeRAM, one must remember that it is not yet on the market, and only exists as industry prototypes. Both Flash and FeRAM are currently in use within the sensor and smart card market and will continue to capture a big share of both industries as MRAM continues in its development stages.

SUPPORTING EVIDENCE: INTERVIEWS

In conducting interviews with people affiliated with MRAM research, it was important to obtain opinions of professionals that were evenly distributed throughout industry and academia. As a result of this approach, the final list of replies gathered are in Table 1[32-39].

INTERVIEWEE	AFFILIATION	AREA
Dr. Said Tehrani	Motorola Corp.	Industry
Dr. R.A. Buhrman	Cornell University	Academia
Dr. Chuck Morehouse	Hewlett Packard	Industry
Dr. Jim Daughton	NVE	Industry
Dr. Richard Colton	NRL	Government
Dr. Kwan Kwok	DARPA	Government
Dr. Barbara Jones	IBM	Industry
Dr. Caroline Ross	MIT	Academia

Table 1: List of Replies Gathered from Survey

The professionals were each emailed a list of similar questions (some were tailored to suit the individual company or agency), and the answers were compiled over a period of time. The questions that were asked were:

1. What are the potential future applications that you feel will be implemented with MRAM technology?

2. Of these applications, which do you feel will be the most likely choice for implementation?

3. What is currently limiting the development of the technology with respect to these applications?

4. What do you perceive as the primary technology competition for MRAM?

5. What advantages or disadvantages does MRAM technology have compared to this competition?

6. Do you believe that eventually MRAM will completely replace DRAM as the main RAM in personal computers?

7. Is MRAM technology as economically viable as the alternatives? How successful do you project MRAM to be in the future?

All of the interviewees believe that the most viable uses for MRAM that would be implemented in the market first were sensors and low power mobile applications. They felt that eventually MRAM would be integrated into the personal computer market, but this would take time, and a full takeover of the RAM market would not take place until MRAM could overcome mass production issues and the price could be lowered. The initial implementation of MRAM into the PC market would be for applications that required much faster computation times and be purchased by entities that could pay top dollar for equipment. All agreed that the applications that MRAM was attempting to break ground in were already in existence within the market, and the technology only sought to improve the functionality of those existing applications.

A common theme with respect to the limiting factor in the development of MRAM was the lack of uniformity of the MRAM cells when produced in mass quantities for industry. Currently, there are no manufacturing systems that are sufficient in creating high density MRAM chips with enough precision to maintain the integrity of the cells that are tested in the lab. As a result of the nonuniformity, researchers are having difficulties controlling the behavior of the individual cells enough to be able to easily

manufacture chips with high yields and high performance on a large scale. For this reason it is still extremely difficult to integrate the technology into industry because it would not fulfill market needs.

According to the experts, the two nonvolatile memory technologies that are the biggest threats to MRAM are FlashRAM, and FeRAM. Although they are not currently advanced enough to surpass MRAM technology with respect to the long-term goal of replacing DRAM, they are a significant threat in the low power portable electronics market, and already have a significant impact on the IC card industry. Dr. Said Tehrani, from Motorola Inc., brought up the fact that MRAM is also competitive with current combinations of volatile and nonvolatile memory technology. SRAM and Flash memories alone are not enough to compete with MRAM, but used together, they make a nonvolatile memory with fast read/write times. But even combined with other technologies, FlashRAM and FeRAM are still considered to be behind MRAM technology in terms of useful advantages for industry. In comparison to both FeRAM and FlashRAM, MRAM has much faster read/write and erase times, better switching endurance (as stated previously, MRAM has unlimited endurance), and is currently considered more cost effective than both its competitors in many applications.

Although other, newly developing memory technologies are in fierce competition with MRAM, the biggest competitor, by far, is volatile DRAM. To say that DRAM will be a difficult hurdle for MRAM to overcome is quite the understatement. In order for MRAM to be successful in completely replacing DRAM in computers, it must become easy to manufacture, and be cost effective as well. All of the interviewees feel that this will take time, and that MRAM will have to start small and work its way into the market slowly via niche markets. However, with respect to MRAM's success in the DRAM market, the industry professionals were much more optimistic than the professionals in academia. They felt that despite the difficulties with mass production, manufacturers will eventually find a way to increase the overall functionality and cost effectiveness of MRAM technology, and that it will eventually overtake the DRAM market. The professionals in academia, although confident that MRAM would have success in initial niche applications, were skeptical that MRAM could achieve the density and cost effectiveness of DRAM technology, and therefore would not be able to acquire its customer base.

SUPPORTING EVIDENCE: COMPETITION IN TECHNOLOGY DEVELOPMENT

When analyzing the success of a particular technology, one must take a look at the industry as a whole and assess the companies that are taking a stake in that technology. There are quite a few companies and government agencies that are devoting research and funds to MRAM research and development. Those companies are:

IBM	HONEYWELL	FUJITSU
HP	Motorola, Inc.	Matsushita
NVE	NEC	DARPA
Toshiba	NIST	Hitatchi
NRL	Cannon	Seimans

For the sake of this analysis, we are going to only look at those companies that are leading the way in technology development for nonvolatile memory. A chart summarizing those companies and their research concentrations is illustrated below in Table 2.

COMPANY	MRAM	FlashRAM	FeRAM	Portables	Computers	Sensors	Government
IBM	x	x	x	x	x		
Motorola	x	x	x	x			
Fujitsu		x	x			x	x
Non-Volatile Electronics	x				x		x
Honeywell	x				x	x	x
HP	x			x	x		
NIST/DARPA/NRL	x					x	x

Table 2: Major Competitors in Non-volatile Electronics Research

As you can see from the chart, all of the companies that are leading the way in MRAM and other nonvolatile memory and sensor research are leaders in the electronics industry itself. These entities see the paradigm shift from pure CMOS technology to nonvolatile memory in the future, and are gearing their companies toward a successful merger into the next wave of technology.

In the case of IBM, Stuart Parkin and his associates are working hard to be able to market a 256Kbit MRAM chip for computer systems by 2004[39-41]. According to the found press releases, IBM is attempting to make the chip with the "...speed of SRAM, high density and low cost of DRAM, and the nonvolatility of FlashRAM." In addition to their MRAM research, IBM is also renewing their commitment to DRAM and CMOS systems. The lithography techniques used to make CMOS components are also needed for MRAM cells, and improvement in precision and miniaturization would benefit both technologies. They realize that the two technologies, although competing for market space, are dependent upon one another. For example, MRAM cells cannot achieve the densities required for commercialization if the selection transistors cannot scale down with the rest of the cell. Currently, IBM holds many patents integral to magnetoresistive technology, and has led the competition in many of the MRAM applications that were discussed earlier. Although IBM is known for its production fabs and state of the art facilities, the company will not be manufacturing its own parts for the nonvolatile memory line. They will be outsourcing their MRAM production to Infineon Corporation.

Motorola has taken an interesting position on the important applications for MRAM, and how they are going about presenting their products to the public. According to Dr. Tehrani, Motorola, Inc. is also going to introduce products using MRAM technology in 2004, but the company will be limiting its product commercialization to PDAs, cell phones and digital cameras. In time, says Dr. Tehrani, the product base will expand to other wireless and automotive applications[42]. Motorola is also an interesting company because although they have their own researchers, such as Dr. Tehrani, they have also invested in the intellectual property of NVE[43,44]. Although reluctant to discuss issues concerning patents with anyone outside of the company, one would deduce that the Motorola does this in order to use certain aspects of NVE technology without having to worry about intellectual property issues.

Non-Volatile Electronics, headed up by CTO Jim Daughton, is also a leader in the development of MRAM technology. The company holds approximately 19 patents on MRAM technology ranging from sensor and isolator applications to RAM cell operation. Although the company does manufacture parts for sensor technology and small MRAM devices, it does not have the capability to manufacture high density MRAMs[45]. It is for this reason that NVE sells licenses to its intellectual property to other companies with this capability. So far, the company has four licensees: Honeywell (to which NVE is affiliated), Motorola, DARPA, and Agilent Technologies[46-48]. Officials in the company realized that the investment in building fabrication facilities would be too great, and decided to concentrate on building their intellectual property portfolio. Says Dr. Daughton, "We have tried to stay ahead of the field with our intellectual property with at least some success." According to press releases found on the world wide web, the company is making headway on their "mostly off systems", or sensor products and claims to have functioning MRAM technology that has switching times of 3ns, and functions on 4pJ per cell, which is 1/1000 of the power needed for EEPROM cells.

The Fujitsu Corporation is taking yet another approach to the industry switch to non-volatile RAM. They are using Flash RAM and FRAM[48-50] to get a hold on the Smart card and IC card market. According to the Fujitsu corporation press releases from October 2001, the global market for IC cards was projected to reach $35 billion by FY2001, and expected to grow at an annual rate of 30% through 2004, and the number of cards is expected to rise to 8 billion by 2005. These IC cards are used in many different capacities such as fingerprint sensors, ID cards, financial cards, mass transit and toll cards, and are expected to be utilized for e-commerce in the future. The company has also invested in opening the Fujitsu Microelectronics FRAM Center, so that more of an effort can go into improving the performance of their FRAM technology. In total, Fujitsu Corporation's sales target for the first half of the Fiscal Year 2002 is 1.5 million units per month.

Hewlett Packard is also taking advantage of the attributes of MRAM. They are looking toward replacing FlashRAM in their portable electronic devices. They are currently researching different types of magnetoresistive technologies in order to optimize their MRAM design[51,52].

The three government agencies that are shown in the chart (DARPA, NIST and NRL) also have a stake in the MRAM market. The funding from the government, which not only goes toward internal research, aids companies such as IBM, NVE and Honeywell in their endeavors as well[53-57]. Research is geared toward a multitude of MRAM computer and sensor technology to aid in improving systems such as, bio-warfare sensors, GPS and satellite systems, identification sensors, and aerospace applications.

As you can see, these companies each have different approaches to the same problem: the paradigm shift in the computer industry from pure CMOS technology to non-volatile and hybrid memory technologies. Each one of these companies had the leadership and the foresight to see that there was a limit to where CMOS components could bring the industry, and knew that there had to be a change to other technologies. As a result of this, each company sought to claim a corner of the MRAM market, and build a research base that would allow them to succeed in this new paradigm. The other companies that were not as intuitive will have difficulty gaining the manpower, expertise, and alliances that these companies have already achieved.

ANALYSIS OF ADVANTAGES/DISADVANTAGES

In reading and analyzing the body of literature on MRAM technology, it becomes apparent that this technology is the most commercially viable alternative to volatile memory, and is the wave of the future for Random Access Memory. With that said, there are disadvantages to current MRAM designs that need to be reconciled before the technology can advance from laboratories into industry. As stated previously, there is considerable variability between MRAM devices fabricated on a chip, which limits the manufacture of chips on a large scale. This means that the process is slower and more expensive because there are fewer chips being manufactured. When MRAM is first released, it will be too expensive for most people to buy MRAM-based computer systems, meaning that most of the consumers who purchase the systems are those that require high power computing and extremely fast computation times, such as research companies and universities.

Everyday consumers, on the other hand, who do not use their computer for much more than what is initially installed by the factory, would not notice the increased power or the 5ns read/write times that their computers are able to make. The only thing that they would notice is the increase in the price tag of their systems. In this respect, MRAM technology is outpacing the needs of the average consumer. As stated by Christensen in his April 8, 2002 lecture, "Our lives do not get complicated fast enough" to keep up with new technologies. Consumers are happy with the current pace of CMOS technology, and many of them are unaware of the phenomena of Moore's Law and the implications it has on the future of computing. They will not be convinced that an MRAM-based computing system is worth the price.

So this begs the question: How do manufacturers persuade consumers to want to purchase components with MRAM? Since it will take years to actually make MRAM affordable to individual consumers, how can companies introduce this new technology into their vocabulary so that when more complex systems are finally marketed they will sell immediately? The answer: start small. Companies should introduce MRAM into smaller systems such as cell phones, PDAs, and digital cameras (where the low power consumption and nonvolatility are key), and then move on to larger components like laptops, wireless and automotive systems before moving further into large scale computing systems. The smaller systems do not require the high densities that more complex systems require, and therefore can be manufactured at a lower cost. The benefits of MRAM are illustrated to the consumer, and companies have time to refine their processes while still making money from MRAM (small systems) and DRAM (complex systems). As more consumers buy MRAM products the manufacturing process, as Christensen puts it will, "make itself cheaper." After the first phase of portable electronics gains success, manufacturers can then move onto hybrid and modular/upgradeable systems that incorporate both DRAM and MRAM and then in time, MRAM would become more cost effective and phase out volatile memory in certain applications. Based on a comparison of the current advances in MRAM technology, and industry market implementation timelines, I believe that companies will essentially be forced to follow this type of scheme. The technology will not be ready for more complex systems in time for full market implementation.

Although MRAM is not ready for full implementation, and must prove itself in the computer market, it is obvious that there is a definite need for a new technology in the electronics industry. The major companies within the industry have been aware of a paradigm shift for quite sometime now, and have been searching for a technology that will overcome scalability and volatility problems, while improving upon other memory characteristics such as speed and power consumption. The current answer to these problems is MRAM technology. Not only does MRAM out perform any other non-volatile memory solution to date, it can also be very useful for other, non-memory applications, such as sensor components in many different systems. Industry competitors, as well as government agencies, have found uses for MRAM sensors in biotechnology, GPS, identification and aerospace systems. In the future, technologies such as molecular computing and Chalcogenide phase change memories may, in fact, prove to be better alternatives to high density, high speed computing, but since technologies such as these are still in their infancies, MRAM will continue to be the viable, profitable alternative for the next paradigm shift.

PART III: INTELLECTUAL PROPERTY ANALYSIS

When analyzing a technology that is rapidly approaching commercialization, one must consider the intellectual property involved with it. In the case of MRAM technology, there has been a recent push toward acquiring intellectual property in the past ten years, due to the discovery that CMOS technology will not be able to accommodate all of society's computing needs in the future. This belief that the limits in CMOS components would require a paradigm shift in the computer industry caused scientists to look toward non-volatile memory solutions, therefore inciting a resurgence in the acquisition of intellectual property for this new paradigm.

But acquiring the important patents for a new technology is not an easy task. There are many barriers that need to be overcome before scientists can reach their ultimate goal of commercialization. In technology, there is always a large barrier to overcome in order to break into a certain paradigm. Generally, once the large barrier is overcome, there is a succession of small barriers that must be passed in order to implement the new technology. MRAM technology is not an exception to this rule. The largest barrier by far concerning MRAM was the design of the memory cell itself. Once that was taken care of, new problems such as how to arrange the cells into memory arrays, how to address individual cells, and how to manufacture the chips arose. Now that MRAM technology is close to implementation in commercial applications, these smaller, yet very important barriers are currently being addressed. It is these barriers, the applications that are associated with them and the companies and individuals that work to overcome them that I will be focusing on in this stage of my analysis.

DOMINANT COMPANIES/ FORMIDABLE EXPERTISE

While searching for intellectual property concerning MRAM technology, I found that there are five companies that are frequent assignees for patents. Those companies are: Honeywell, Non-Volatile Electronics, IBM, Hewlett Packard and Motorola. These companies hold intellectual property in every aspect of non-volatile memory. Embedded within these companies and their affiliates are five individuals who are essentially the forefathers of modern MRAM cell design. They are:

James M. Daughton, Non-Volatile Electronics

Stuart Parkin, IBM

William J. Gallagher, IBM

Gary A. Prinz, Navy

Jiin-Chuan Wu, California Institute of Technology

Virtually every patent discovered by Haratani* and myself from the five aforementioned companies referenced at least one of these scientists.

Tracing the body of referenced work from these five researchers[58-66] led to the discovery that each company shares, or licenses their intellectual property to other companies within the industry with respect to the actual memory cell design. Every company in my analysis shares the same basic structure for their respective MRAM memory cell designs[67-72]:

1) A semiconductor substrate to act as a base
2) One fixed ferromagnetic layer
3) One free ferromagnetic layer with two axes of magnetization
4) One non-magnetic, insulating layer situated between and in contact with the two ferromagnetic layers
5) One anti-ferromagnetic layer to act as a pinning mechanism for the fixed ferromagnetic layer
6) The layered structure of 1-5 acts as a tunnel junction for current
7) The two ferromagnetic layers have two different coercive forces (between 10 Oe and 100 Oe), the fixed ferromagnetic layer having a much higher coercive force than the free layer
8) CMOS circuitry attached to each memory cell in order to read, address, and control the current in the respective cells

So why did these highly competitive companies allow their competitors to share the intellectual property that they discovered? The answer is simple. All of these companies, although they are fierce

* Laid the basis of the patent search for this paper.

competitors within the computer and sensors market, are affected by large paradigm changes within their industry. In order for a new paradigm to be fully implemented, all of the companies affiliated with that industry need to push the new technology. The competition that evolves from the sharing of intellectual property is what allows the new paradigm to move forward. This does involve risk, however. If the companies that are licensing out the basic intellectual property are not prepared to evolve along with the competition, they will eventually be forced out of that paradigm. It is for this reason that the five companies mentioned previously have attempted to take this basic idea of MRAM technology and transform it into a chip unique to their designers in order to get it fully operational and to market first.

INDIVIDUAL COMPANY FOCUS

After the initial barrier of finding a non-volatile memory cell that is able to store memory consistently, there are three other major barriers that must be overcome before the applications of magnetoresistive technology may be implemented. The first barrier to overcome is to refine the memory cell and its features. The companies must take the general, licensed patents and tune them to meet the parameters of their system. A second barrier is to develop the circuitry that will complement the magnetic cell arrays so that each cell may be addressed, read/sensed and written. The current to each cell must also be controlled to prevent leakage to other cells. A third barrier to implementation is the manufacturing of the cells and their circuitry components. Manufacturers of magnetoresistive technology must be able to manufacture memory and sensor arrays such that they are uniform and will not contain defects. The following is an analysis of how IBM, Honeywell, Hewlett Packard, Non-Volatile Electronics, and Motorola have addressed one or more of these barriers in their intellectual property.

The International Business Machines Corporation, or IBM, has a broad intellectual property base that is licensed out or referenced by companies throughout the industry. Headed up by Stuart Parkin and William Gallagher, IBM has become a leader in MRAM research and has enabled this new paradigm to push forward by developing intellectual property to overcome barriers to implementation. There are many advances to the general magnetoresistive cell design that IBM has made in order to improve upon

performance and reliability of this technology. Many of these improvements pertain to the tunneling layer that separates the two ferromagnetic layers[73,74]. IBM patented an extra layer, called the interface layer, into the memory cell that was to increase the spacing between the two ferromagnetic layers and cut down on the interference between them. The layer is made up of Copper, Gold or Silver, and is positioned between the non-magnetic metallic layer and the free magnetic layer. Another improvement that was made on the traditional tunnel barrier layer is to make the barrier a multilayer. This means that the barrier will consist of a layer of Aluminum Oxide as well as a layer of Manganese, which will be combined with either Nitrogen or Oxygen plasma. IBM is also getting into the magnetoresistive sensor market. It has designed a fairly simple bridge circuit using four magnetoresistive stacks. If an unknown current enters the circuit at its input, there is a corresponding output voltage from which the current can be found (from the sensed resistance in the cells)[75,76].

Honeywell, another leader in MRAM research, licenses the MRAM cell designs of James Daughton of Non-Volatile Electronics[77]. The cells are manufactured in blocks on chips so that each block can be activated by itself. The sense circuitry that Honeywell has designed to read individual cells consist of two word lines on either side of the memory cell that apply a current first in one direction, then the other to switch the magnetization of the free magnetic layer from one direction to the other. The sense lines that are attached to the cell rows then compare which direction provides the higher resistance with respect to the fixed magnetic layer. The word line currents and the drivers to select the individual cells are run by microcontrollers. There is also a controller that disables the memory cell blocks[78]. Honeywell also has a magnetic field sensor design[79]. The design includes a sensor in a bridge circuit configuration and circular magnetoresistive sensor components. This design is unique in that it incorporates not only GMR sensors, but also includes Colossal Magnetoresistive (CMR) stacks as well.

Motorola also licenses NVE MRAM technology to use in their memory arrays, however, their memory chips function differently from that of Honeywell[80,81]. This design utilizes a pair of memory modules, one reference module and one programmable module. Both modules are made up of an array of memory cells, each cell situated on an intersection of a word and bit line (word lines and bit lines being

formed in a grid, intersecting at ninety degree angles). The cells are activated by two different decoders; one decoder providing a row signal and one providing a column signal. The memory cell that is situated on the intersection of the row and column that contain the signal is thus activated. The corresponding reference cell in the reference module is also activated by the same decoder. A detector compares an output from the target memory cell with that of the reference cell. Each cell in the module also has a diode and a transistor circuit with one terminal on the ferromagnetic layers and one on the sense lines to dissipate charge and prevent leakage currents.

Like Motorola, Hewlett Packard utilizes reference cells in order to compare the difference in magneto-resistance between a one and a zero, however unlike Motorola, the reference cells are situated in the same module as the written cells. Each row and column has its own set of reference cells containing one of two magnetization states and the elements are coupled in parallel. Finally, the circuit contains decoders to activate individual cells, and sense circuitry to compare the reference values to that of the written values[82]. Another variation to the write circuitry for an MRAM chip comes in the form of Hewlett Packard's Write Circuit for Large MRAM Arrays[83]. The circuit contains switches and sense circuitry that allows for the activation of individual cells without exceeding the breakdown limits of the cells. This will supposedly prolong the write endurance of the memory cells.

Lastly, Nonvolatile Electronics Corporation (NVE) lead by James M. Daughton, is also trying to make its way into the MRAM market. With patents pertaining to both sensor and magnetoresistive memory, NVE has been successful in manufacturing and licensing technology[84-87]. With unique designs for two different types of sensors and digital memory storage, NVE is one of the only companies that has incorporated intellectual property to block other inventors above an beyond that of just the normal language of everyday patents. With their competition patenting very simple bridge circuit sensors, NVE has worked hard to patent a more complex spin dependant tunneling sensor with many sensor stacks that may be used for more advanced applications, such as biological and aerospace sensors. This very obvious advance in MR sensor applications is well beyond the capabilities of all other companies in the market,

and the very strategic intellectual property ownership of NVE will ensure that the company will continue to remain ahead of the competition.

These are just a few examples of the various types of intellectual property that various companies in the computer industry are trying to capture. The actual body of literature found on the United States Patent Office web site is too broad for the scope of this paper, but conclusions can be made from the analysis of such patents.

CONCLUSIONS

Although technology competitors such as Flash RAM and Ferromagnetic RAM are already implemented in IC and Smart Card markets, experts in industry feel that MRAM will be the next paradigm in electronics memory. As stated previously, there are currently three major barriers to implementation: refinement of MRAM cells, sense and read write circuitry design, and manufacturing tolerances. If MRAM technology can overcome these barriers (as well as others), professionals believe that MRAM will overtake the Flash RAM and Ferromagnetic RAM markets and push forward into other aspects of magnetic memory and sensor applications. The information pooled from the United States Patent Office leads me to believe that companies are working hard to overcome these barriers in order to prepare MRAM technology for the upcoming switch to hybrid MRAM/CMOS systems.

So, how does this body of intellectual property affect the way industry will push forward? The fact that virtually all electronics companies are moving toward some kind of integrated CMOS/MRAM system is a definite indication that industry is moving away from total CMOS electronics. The aggressive pursuit of magnetoresistive memory and sensor technology by the major competitors will lead the way to an eventual solution to the barriers of implementation, and the rest of the industry will be forced to follow suit. This is not to say that all of the projections of such companies are going to come to fruition. The optimism of industry competition that their respective designs will revolutionize the electronics market is just that, optimism. The MRAM designs and patents of today, although having the potential to be

successful, may or may not be the so-called future of MRAM. Only time will tell, as more and more designs actually become prototyped and then manufactured.

I believe, however, that as the MRAM market begins to take shape, and manufacturing chips becomes more and more commonplace, that portable electronics companies (the first sector that will see the shift) will be forced to change along with the paradigm. For example, If IBM and like companies standardizes their manufacturing process for MRAM chips for use in cell phones and PDAs, portable electronics companies such as Palm, Inc. and Verizon will have no choice but to buy those chips for lack of alternatives. Consumers, in turn will be forced to buy their new PDAs and cell phones with this new technology. As stated in Part Two: Applications Analysis, it is these breakthrough markets that will allow for MRAM technology to move forward throughout the industry. As consumers purchase newer components that contain MRAM systems, the manufacturing costs for the technology will become cheaper, therefore allowing for the price of complex systems to come down as well. The hope, for MRAM manufacturers, is to eventually take over said electronics markets to make way for other new paradigms in the future.

PART FOUR: ECONOMIC ANALYSIS

In order to complete the analysis of MRAM technology and its applications, one must consider the financial implications involved with getting said technology to market. In this phase of technology development, designers must come together with marketers to decide what the feasible target market should be for that technology, and how to go about reaching consumers. In the case of MRAM technology, it has already been established that the initial target markets are the portable electronics market and the IC card market. Although the projections of such companies as IBM and Motorola provide a market date of 2004 for simple, low density MRAM chips that will fulfill the needs of small portables such as cell phones and PDAs, more complex electronics applications such as laptop and desktop computers are much farther down the timeline to implementation. Regardless of immediate or distant implementation timelines, a few questions need to be answered before any technology will come to market. How much of the market can this technology obtain? How much are consumers willing to pay for the added value of this new technology? What is the timeline to profitability for those applications? These are the questions that will be answered in the following sections.

After reading the body of literature available, it is my opinion that of the $48 billion memory market – the portable electronics market being approximately 40%, or $19.2 billion[88] – MRAM will only be able to obtain a fraction of the revenues (less than 10%) within the first few years. This will be a result of the combination of a consumer lack of understanding of the technology itself, and the price increase that will be induced by the insertion of MRAM into components. In time, however, this technology will gain popularity as well as a bigger piece of the market. As more people venture to buy components with embedded MRAM technologies, the manufacturing price will decrease, and consumers understanding of the technology will increase. The combined effect will allow for eventual profitability. This trend is not unlike when original computer systems entered the market.

The IC card market, in my belief, will be slightly more difficult to enter due to the fact that the embedded technologies (Ferromagnetic RAM and Flash RAM) are also nonvolatile memory solutions, and already occupy about 1/8, or 12.5% of the existing market. Of the $3.5 billion that circulate through

the industry (a figure that is expected to grow at an annual rate of 30% through 2004) [89], I believe MRAM will only be able to obtain approximately 2-3% at best in its initial market share.

Although the portable electronics and IC card markets are considered to be the breakthrough markets for MRAM technology, there are no guarantees that it will actually obtain a big enough piece of either market to be considered profitable in the long run. The embedded technologies already have a hold on each market, and will be difficult to overtake. In the case of the portable electronics market, Dynamic RAM and Static RAM are known to be functional and reliable, and Magnetic RAM will have to prove its worth in order to maintain even a piece of the market. This is where marketing can play a major role. The function of marketers in this case is twofold: to create an interest in nonvolatile memory, as well as to educate the consumer about the technology itself. As Christensen pointed out in his lecture, consumers are happy with what they have at present. Technology today is such that it exceeds the needs of the everyday consumer, in effect "over serving the customer". In order to get those everyday consumers to feel that they require an improved system with added cost, companies need to convince them as such. In addition, consumers must be educated as to the advantages that MRAM has over its competition in order to fully understand how MRAM fits their needs. Without this information, consumers will not be able to make a value judgment on this technology.

Since MRAM technology will be a more expensive alternative to traditional systems, the question of how much consumers are willing to pay for that added value arises. The two main reasons for the additional cost of systems containing MRAM components are: the added value of having nonvolatile memory, and the added cost of the system due to manufacturing limitations. For companies manufacturing components containing MRAM technology, there are no real start-up costs. In fact, much of the equipment that is required for the manufacturing of MRAM chips is already being utilized by existing systems. Companies, such as IBM, that find that they do not have the manufacturing capacity for MRAM systems in one facility, outsource their business to another company that does have the resources (in this case Infineon), in lieu of building a new facility. The cost to manufacture is extremely high due

to high precision requirements in the sputtering of the magnetic stacks. Since more care is required in manufacturing chips, companies cannot produce the volume needed to keep the cost at a minimum.

So how much are consumers willing to pay? The simple answer: it depends on the consumer. In these breakthrough markets, the consumers that were hoping for MRAM's high density, high speed applications are going to be disappointed. The more complex applications that they are waiting for will not be around for sometime. Those who are willing to pay premium for PDAs and cell phones are most likely companies who purchase the components for employees, or businesspeople that require them for personal use. It is through these bulk orders that manufacturing costs of these portable electronics will decrease, thus allowing for a broader consumer base. Similarly, it was corporate America that allowed for the integration of the personal computer into everyday life for a broad range of consumers. The everyday consumer will continue using their "old" cell phones, PDAs and digital cameras until increased production provides the economies of scale that enable manufacturers to reduce the cost of electronics that use MRAM components.

The timeline for MRAM technology is, as stated before, much like that of the original computer systems that came out in the 1980s. It has taken industry nearly twenty years since the inception of the personal computer to achieve the capacities and functionality that DRAM and SRAM have achieved today. The optimism of those in the computer industry that say MRAM will be fully functional within the next two years may sound appealing to those of us that appreciate the magnitude of what MRAM can do for science, but has no realistic value. The reality of the situation is that, although the year 2004 will bring us functional MRAM chips, they will be simple, and of extremely low density in comparison to that of DRAM chips. The research necessary to gain full knowledge of the capabilities of MRAM still needs to be done, and will require substantial funding over and above that which has already been spent. If MRAM is going to have a big impact on the electronics industry, it will not be able to do so for at least another decade.

REFERENCES

1. Eric J. Lerner, IBM Innovation: Think Research, "Shorter Circuits", www.ibm.com.
2. J. M. Daughton, Advanced MRAM Concepts, Copyright© Feb. 7, 2001.
3. S. S. P. Parkin, et. al., J. Appl. Phys., Vol. 85, No. 8, 15 April 1999.
4. J. M. Daughton, Magnetoresistive Random Access Memory (MRAM), Copyright© Feb. 4, 2000.
5. Reference 4.
6. Scientific American, The Magnetic Attraction: A Long Race to Create Faster Memory Chips That Never Lose Data Yields Prototypes at Last, May 1999.
7. Reference 4.
8. Chih-Ling Lee, A Study of Magnetoresistive Random-Access Memory.
9. Reference 2.
10. www.almaden.ibm.com/st/projects/magneto/giantmr/
11. F. J. Castano, Y. Hao, M. Hwang, and C. A. Ross, Magnetization reversal in sub-100 nm pseudo-spin-valve element arrays, Appl. Phys Letters, Vol. 9, No. 10, 3 September 2001.
12. G. L.-T. Chiu and J. M. Shaw, Guest Editors., Optical Lithography: Introduction, IBM Journal of Research and Development, Vol. 41, No. 1/2, 1997.
13. www.bekaert.com/sinvaco/sputter.htm
14. Reference 4.
15. Reference 11.
16. F.J. Castano, Y. Hao, S. Haratani, C.A. Ross, B. Vogeli, M. Walsh, Henry I. Smith, Magentic Switching in 100 nm Patterned Spin Valves, 15 October 2000.
17. Jian-Gang Zhu and Youfeng Zheng, The Micromagnetics of Magnetoresistive Random Access Memory, Appl. Phys., Vol. 83, 2002.
18. Exotic Memories, Diverse Approaches, www.ednasia.com
19. www.darpa.mil
20. www.ibm.com
21. R.J. Colton (PI), The Bead Array Counter (BARC): A Multi-analytic Biosensor on a Chip.
22. Paul Sheehan, Rebecca Edelstein, Cy Tamanaha, Michael Miller, Li Zhong, Lloyd Whitman, Richard Colton, BARC: A Magnetoresistive Biosensor, Eighth Foresight Conference on Molecular Nanotechnology, November 13 2000.
23. www.mems-exchange.org
24. S. Tehrani, J.M. Slaughter, E. Chen, M. Durlam, J. Shi, and M. DeHerrera, Motoroa Labs, Physical Sciences Research Laboratories, Progress and Outlook for MRAM Technology, IEEE Transactions on Magnetics, Vol. 35, No. 5, September 1999.
25. Raghupathy V. Giridhar, Intel Corporation, Flash Technology Group, Flash Technology: Challenges and Opportunities, J. Appl. Phys., Vol. 35, No. 12B, Dec 1996.
26. www.howstuffworks.com/flash-memory.htm
27. Reference 24.
28. Interview with Dr. James M. Daughton of Nonvolatile Electronics, March 25, 2002.
29. FRAM Guide Book, Copyright© FUJITSU LIMITED 2001.
30. Kunio Takemitsu and Endo Nobuhiro, A Ferroelectric Memory Technology for Embedded LSI, Copyright NEC Corp. 2002.
31. Reference 17.
32. Reference 28.
33. Interview with Dr. Said Tehrani of Motorola, April 1, 2002.
34. Interview with Dr. R.A. Buhrman or Cornell University, March 28, 2002.
35. Interview with Dr. Chuck Morehouse of Hewlett Packard, March 29, 2002.
36. Interveiw with Dr. Richard Colton of the Naval Research Laboratories, March 14, 2002.
37. Interview with Dr. Kwan Kwok of DARPA, March 25, 2002.

38. Interview with Dr Caroline Ross of MIT, April 5, 2002.
39. Press Release, IBM, Infineon to Advance Revolutionary Memory Technology, East Fishkill, NY and Munich Germany, December 7, 2000.
40. IBM Newsletter, "Tell Me About MRAM", www.ibm.com
41. IBM Micro News, Second Quarter 2001, Vol. 7, No. 2.
42. Reference 33.
43. Press Release, www.nve.com, NVE Announces Watershed MRAM Patent, February 28, 2002
44. Press Release, www.nve.com, NVE Signs Agreement with Agilent Technologies, October 3, 2001
45. Reference 28.
46. Reference 44.
47. Press Release, www.nve.com, NVE Selected for Next Generation Magneto-Electronics Development.
48. FRAM is a registered trademark of Fujitsu
49. Press Release, www.fujitsu.com, Fujitsu Introduces World's First LSI Chip for Multi-function IC Cards Using Groundbreaking 0.35-micron Ferroelectric Technology, Tokyo, August 2, 2001.
50. Press Release, www.fujitsu.com, Fujitsu Establishes First MRAM Centre in Europe, Tokyo/Dreieich-Buchschlag, October 15, 2001.
51. www.hp-labs.com
52. www.hp.com, Making Room for Digital Data, November 4, 1999.
53. www.darpa.mil
54. www.nrl.gov
55. www.nist.gov
56. www.nve.com
57. www.honeywell.com
58. Patent, 5025416, Prinz, June 1991.
59. Patent, 5477482, Prinz, December 19, 1995.
60. Patent, 5640343, Gallagher et. al., June 1997.
61. Patent, 5650958, Gallagher et. al., July 1997
62. Patent, 4780848 Daughton et. al., October 1988.
63. Patent, 5251170, Daughton et. al., October 1993.
64. Patent, 5329580, Wu et. al., July 1994.
65. Patent, 5173873, Wu et. al., December 1992.
66. Patent, 5764567, Parkin, June 1998.
67. Patent, 5617071, Daughton, April 1,1997.
68. Patent, 6317376, Lung T. Tran, November 13, 2001.
69. Patent, 5734605, Zhu et. al, March 31, 1998.
70. Patent, 5640343, Gallagher et. al., June 17, 1997.
71. Patent, 5629922, Moodera et. al., May 13, 1997.
72. Reference 59.
73. Patent, 6359289, Parkin, March 19, 2002.
74. Patent, 6347049, Childress et. al., February 12, 2002.
75. Patent, 5801984, Parkin, September 1, 1998.
76. Patent, 5561368, Dovek et. al., October 1, 1996.
77. Reference 43.
78. Patent, 6134138, Yong and Zhu, October 17, 2000.
79. Patent, 6232776, Pant and Wan, May 15, 2001.
80. Patent, 5852574, Naji, December 22, 1998.
81. Patent, 5831920, Chen et. al., November 3, 1998.
82. Reference 68.
83. Patent, 6363000, Perner et. al., March 26, 2002.
84. Patent, 6168860, Daughton, January 2, 2001.
85. Patent, 6340886, Daughton, January 22, 2002.

86. Patent, 6349053, Daughton et. al., February 19, 2002.
87. Patent, 6072382, Daughton et. al., June 6, 2000.
88. Reference 43.
89. Reference 50.