A Stacked Full-Bridge Microinverter Topology for Photovoltaic Applications

by

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Abstract

Previous work has been done to develop a microinverter for solar photovoltaic applications consisting of a high-frequency series resonant inverter and transformer section connected to a a cycloconverter that modulates the resonant current into a single-phase 240 V_{RMS} utility line. This thesis presents a new stacked full-bridge topology that improves upon the previous high-frequency inverter section. By utilizing new operating modes to reduce the reliance on frequency control and allowing for the use of lower blocking voltage transistors, the operating frequency range of the HF inverter is reduced and efficiency is increased, especially at low output powers and lower portions of the line cycle. The design of an experimental prototype to test the stacked full-bridge HF inverter topology is presented along with test results that demonstrate the success of the topology. Future improvements to increase performance are also suggested.

Thesis Supervisor: David J. Perreault
Title: Professor

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I could never have finished this project without the help of several people.

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Chapter 1

Introduction

Photovoltaic solar panels have seen their development and installation increase dramatically over the past decade. As these solar panels become increasingly efficient, it becomes more important to have efficient power converters. These power converters function as inverters, converting the direct-current (DC) generated by the solar panels into alternating-current (AC) that can be directly injected into the grid. Traditionally, several solar panels are connected in series to get an output voltage greater than the line voltage, and their output is tied to a relatively high-power inverter [1].

Another approach is to individually connect each solar panel directly to the grid with a relatively low-power microinverter [2, 3, 4, 5]. Compared to using a single grid-tie inverter, microinverters benefit from more effective maximum power point tracking (MPPT) by performing MPPT at the individual panel level and also from increased robustness to failure since a single unit failure would only disable a single solar panel. This comes at the cost of increased total power converter count and reduced energy conversion efficiency, since it is more difficult to achieve high efficiency at the lower power levels and high conversion ratios associated with module-level conversion [1].

In order to compare different solar inverters, the California Energy Commission (CEC) has defined a metric for efficiency that is a weighted average of an inverter's efficiency at different output power levels, from full power down to 5% power, as shown in Table 1.1 [6]. Since solar panels are subjected to temporal changes in insolation and

Inverter Power Level	5%	10%	20%	30%	50%	75%	100%
High-Insolation Weighting Factor	0	.04	.05	.12	.21	.53	.05
Low-Insolation Weighting Factor	.03	.06	.13	.10	.48	0	.20

Table 1.1: CEC Solar Inverter Efficiency Metric

Input Voltage	16–45 V
Functional Input Voltage	22–36 V
Average Power	0–250 W
Output Voltage	240 V_{rms} $(-5\%/+10\%)$

Table 1.2: Desired Microinverter Specifications from Enphase Energy

other factors that reduce the available power, the CEC metric is a more meaningful measure of efficiency than peak efficiency. Because the metric is an average over a wide range of power levels, one cannot only optimize the efficiency at full load when designing and evaluating an inverter; one must also consider how well the converter performs over its entire output range. Note that the CEC's metric gives very little weighting to an inverter's efficiency at full power for high-insolation environments like the Southwest United States. Instead, the majority of the weighting is placed on an inverter's efficiency at 75% power.

Though the CEC metric does not place a large emphasis on efficiency at 100% load, it is still an important factor. Peak power dissipation puts constraints on the mechanical realization of the converter, especially considering size and heat extraction.

1.1 Specifications

Table 1.2 considers the inverter specifications considered for this thesis, which represent a typical requirement for a microinverter design. Microinverters must operate over a wide range of operating conditions. If partial shading causes one of the bypass diodes in the solar panel to turn on, the input voltage from the panel can drop to as much as 16 V, and at startup, the input voltage can rise to as much as 45 V at no load conditions. Although the microinverter is expected to be able to operate within
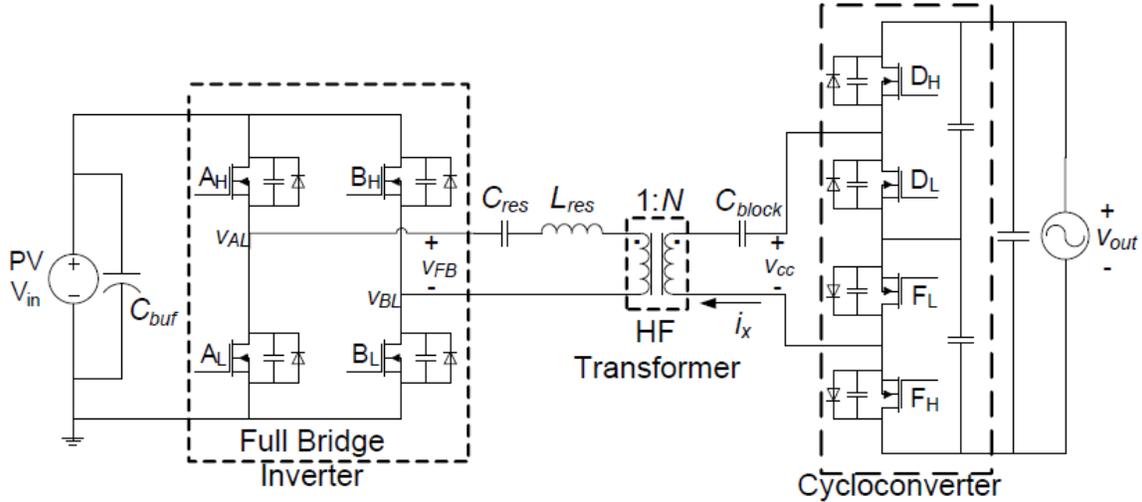
Figure 1-1: Trubitsyn et. al. Microinverter Design [7]

this range, the efficiency of the converter is only measured and optimized within the slightly narrower input voltage range of 22–36 V. In addition, the converter must be able to deliver an average output power of 0–250 W over a 240 V_{rms} mains line cycle.

1.2 Previous Work

A group of MIT researchers working under Professor David J. Perreault previously developed and tested a high-efficiency microinverter architecture based around a resonant inverter topology [1, 8, 7]. In order to reduce the size of its passive components, the resonant inverter is operated at a frequency much higher than the mains frequency, and the generated AC current is ultimately converted down to mains frequency by a cycloconverter. The researchers' complete design includes a series resonant inverter, a high-frequency step-up transformer, and a cycloconverter connected together as shown in Figure 1-1. A variant of this approach includes a series-connected buffer block for handling the power variations that arise at twice the line frequency in a single-phase high-power-factor inverter [9]. By utilizing zero-voltage switching (ZVS) in their inverter and cycloconverter switches, avoiding diode drops, and fine-tuning their control strategy [8], they were able to achieve more than 97% efficiency near full
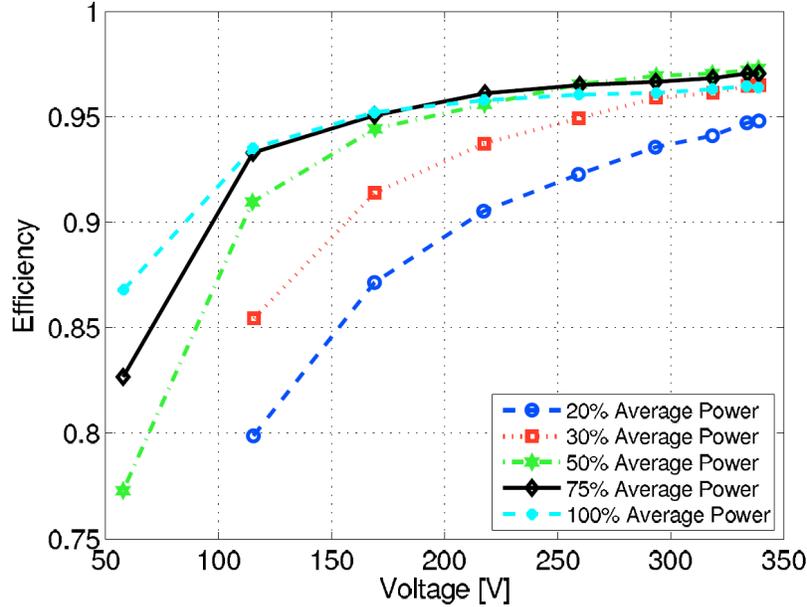
Figure 1-2: Efficiency vs. Output Power and Voltage for Trubitsyn et. al. Microinverter [10]

output power.

Though the converter had a fairly high peak efficiency, at lower output power and instantaneous line voltage levels, the efficiency of their converter dropped to as low as 80%, as shown in Figure 1-2 [10]. This was significantly due to the need to run the converter over a very large range of input voltages, output voltages, and power levels, which necessarily forced compromise given the available degrees of freedom in control. According to the CEC metric, the converter achieved a 95.9% efficiency rating. The efficiency plot suggests that the microinverter has room for improvement on the CEC metric if its performance could be improved at low output power and voltage levels.

The inverter section controls output power by regulating the resonant current i_X. The converter has a few different control handles over the resonant current, but the primary lever is the inverter's switching frequency [7]. In order to attenuate the resonant current entering the cycloconverter, the switching frequency must be increased further above resonance, increasing the reactance of the resonant tank. Because of the wide input and output range that the converter must operate over, the switching frequency can become fairly high compared to the resonant frequency ($> 7 : 1$) before
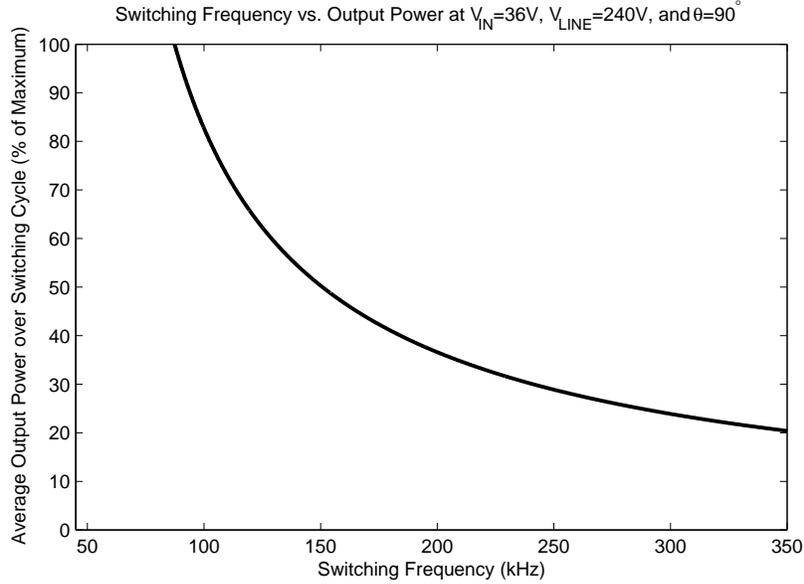
Figure 1-3: Estimate of Power vs. Switching Frequency Relationship
for Trubitsyn et. al. Converter

other techniques are used, particularly in the cases of high input voltage and/or low output power and voltage. Based on a first-order MATLAB model of the converter's operation (see section A.1), Figure 1-3 shows the high switching frequencies needed in such unfavorable cases. As the switching frequency of the converter increases, its efficiency suffers as magnetics losses, gating losses, and switching losses in the switches of the inverter and cycloconverter increase. It follows that finding a way to narrow the switching frequency range of the converter would be beneficial.

1.3   New Stacked Full-bridge Inverter Topology

Motivated by the desire to improve performance where the Trubitsyn et. al. converter suffered, a new topology for the high-frequency inverter section of the microinverter has been developed that can serve as a drop-in replacement for the old inverter section. Instead of driving a series resonant tank directly with a single full-bridge of semiconductor switches as in the previous design, the new inverter topology, shown in Figure 1-4, has a set of two stacked full-bridges that each drive

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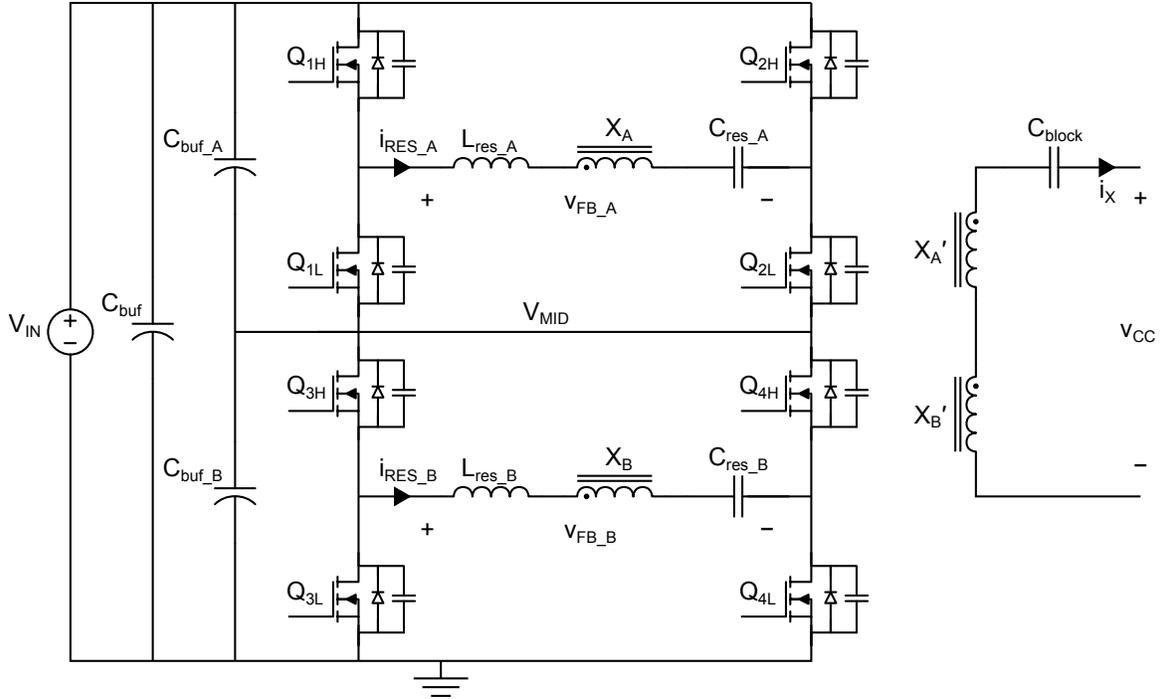
Figure 1-4: Stacked Full-Bridge Series Resonant Inverter

its own resonant tank. The input to each full-bridge is buffered by C_{buf_A} and C_{buf_B}, which each carry half of the input voltage V_{IN}. The voltage waveforms generated in the resonant tanks are stepped up by a set of transformers X_A and X_B and combined on the secondary side (X'_A and X'_B) where the resonant current i_X is injected into the cycloconverter. Note that using other types of resonant tanks, adding a series buffer block, and using other types of load networks or cycloconverters are all possible to use with this inverter. This idea of splitting the inverter into two parts provides several significant advantages over previous designs.

1.4 Thesis Scope and Organization

This thesis investigates the use of this new stacked full-bridge series-resonant inverter in the context of the microinverter application. We investigate the control handles available with the stacked full-bridge topology in order to develop a general control strategy. A prototype is designed and tested in order to demonstrate the potential of the new design and compare its performance to the previous microinverter

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design. In Chapter 2, the operation and control options of the new topology is analyzed. Much of the analysis performed in [8] and [1] still applies to the stacked full-bridge topology, but important principles and results will be repeated when crucial for understanding. Chapter 3 describes the considerations that went into designing the prototype setup used to demonstrate the new converter's operation and performance. Chapter 4 presents the experimental results measured on the inverter prototype. Finally, Chapter 5 analyzes these results and suggests future work to be carried out to optimize the converter performance.

Chapter 2

Theory and Control

This chapter will go over the theory of operation of the converter and the control levers available for controlling its output. Note that in the case where both full-bridges are operating synchronously, which will be referred to as "full-full" operation, the HF inverter operates as a full-bridge series resonant inverter. In this mode it can be used in the full microinverter in the same way as the original full-bridge. As a result, much of the analysis of the HF inverter section of the Trubitsyn et. al. microinverter made in [1] and [8] can be applied to each of the full-bridges individually in the stacked topology with minimal modifications. The pieces that are crucial for understanding the new capabilities of the stacked full-bridge topology will be brought up again as needed.

2.1   Cycloconverter Abstraction

In order to simplify analysis and testing of the approach and keep the project of reasonable scope, a simplification to the architecture was made. In most regions of the converter's operation, the cycloconverter acts as a half-wave rectifier, and from the inverter's perspective, it looks like a resistive load. As derived in [1], the effective resistance the cycloconverter presents is given by:

$$R_{ld} = \frac{\frac{2}{\pi^2} V_{line}^2}{P} \tag{2.1}$$
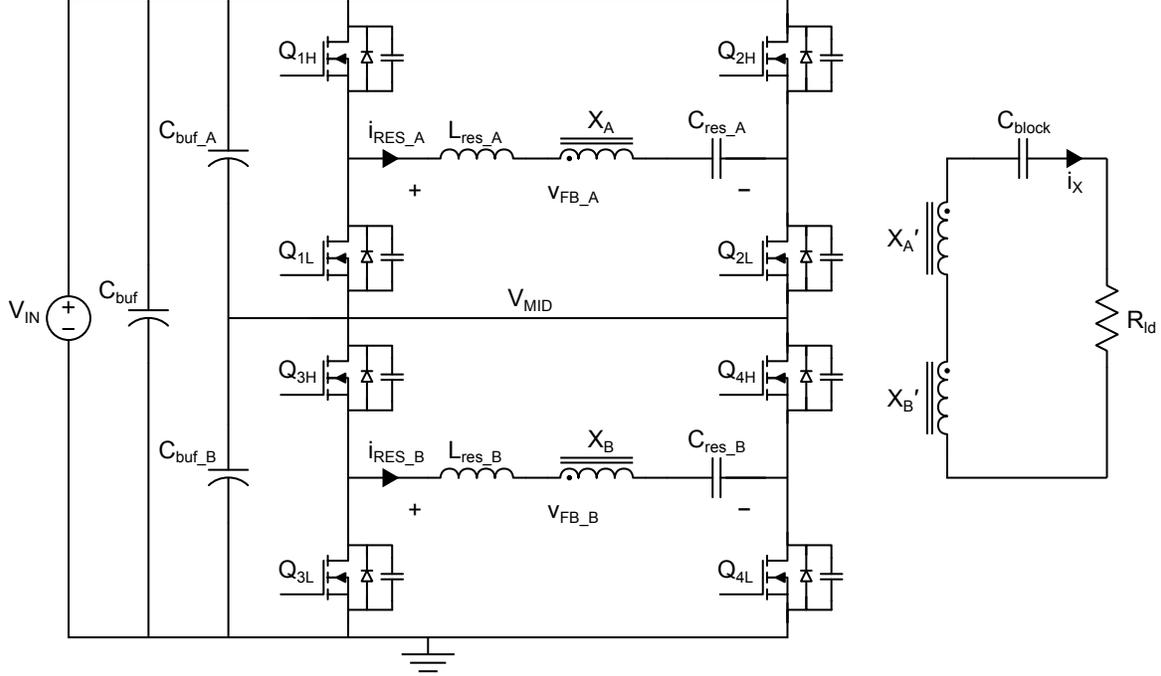
Figure 2-1: Stacked Full-Bridge Inverter with Resistive Load

where the instantaneous power $\overline{P}$ is the average power delivered over a switching cycle and V_{line} is the mains line voltage, which is approximately constant over a switching cycle. The instantaneous power and resonant current are related by:

$$\overline{P} = i_X^2 R_{ld} \tag{2.2}$$

As a result, a load resistor with value set by the line voltage and output power at the desired operating point is substituted in place of the cycloconverter with the knowledge that the analysis and evaluation of the inverter section remains valid. This simplified model can be seen in Figure 2-1.

2.2   Zero-Voltage Switching (ZVS)

The high efficiency of the microinverter relies on the condition of zero-voltage switching in the transistors of the resonant inverter, and care must be taken to ensure that the switching conditions for ZVS are always met. These conditions are thoroughly described in [11]. They can be easily summarized for this inverter in terms of a
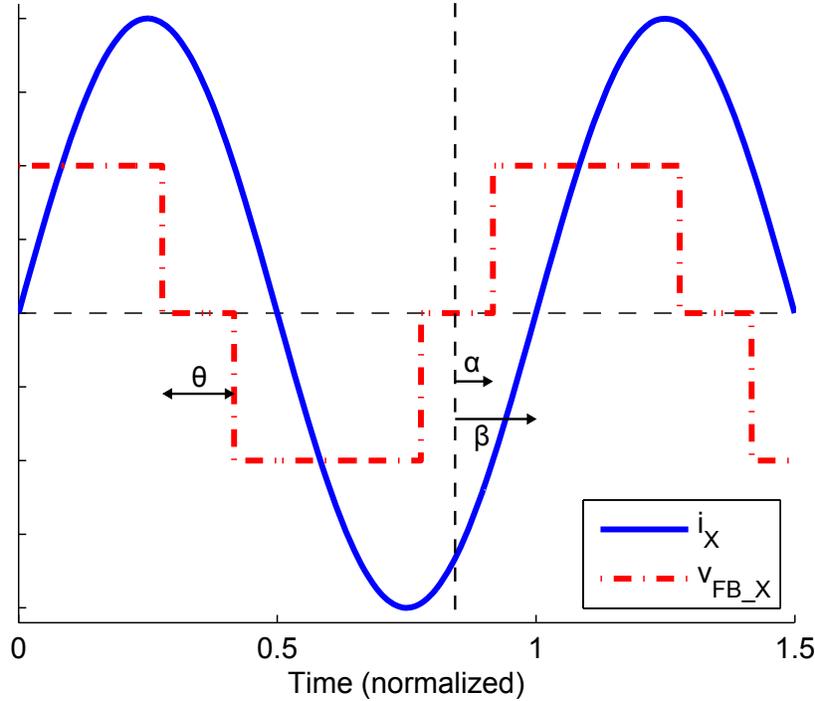
Figure 2-2: Relevant Angles for ZVS

few key angles that are defined in Figure 2-2. θ is the phase shift between the two complementary half-bridges in a full-bridge and β is the phase shift of the resonant current relative to the fundamental of the full-bridge voltage. If we define $\alpha \equiv \frac{\theta}{2}$, then as long as $\beta > \alpha$ the conditions for ZVS will be met [1].

2.3   Control Techniques

The stacked full-bridge topology provides three new control handles in addition to the already existing control handles of the Trubitsyn et. al. converter. The resonant current in each of these modes can then be further varied using frequency control and phase control among different sets of devices as is deemed optimal. Because of the relationship defined in Equation 2.2, controlling resonant current is the same as controlling output power. In order to understand the different control techniques as described below, one should note that, as shown in Figure 2-1, the proposed inverter topology is made up of two full-bridges, labeled "A" and "B". Each full-bridge is composed of two half-bridges, labeled "A1," "A2," "B3," and "B4."
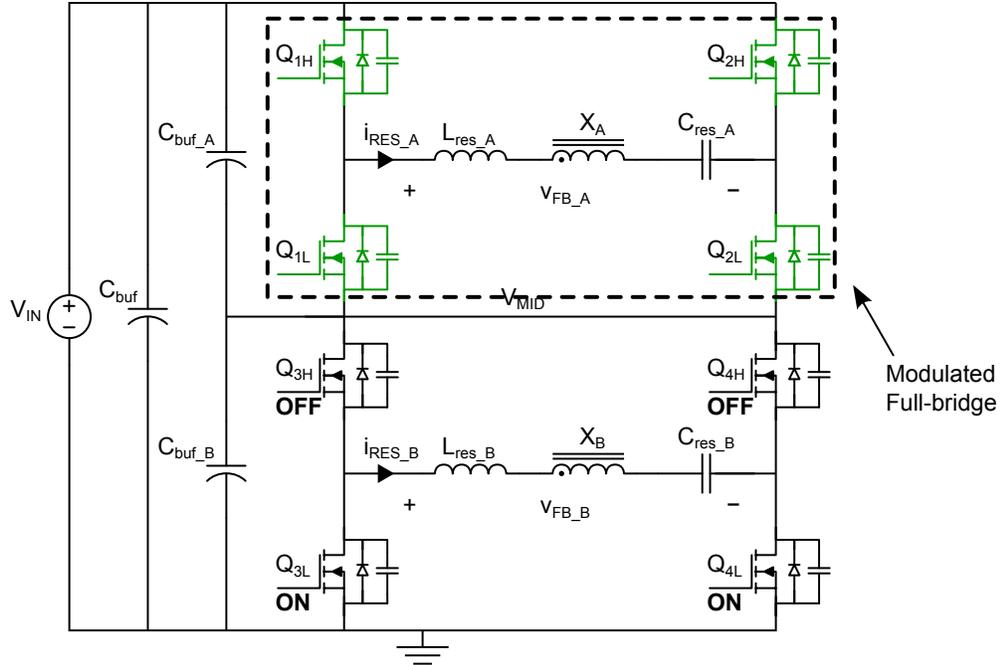
Figure 2-3: Example Full-Clamped Mode with Full-bridge B Clamped

2.3.1 Clamping a Full-bridge

By keeping switches B_{3L} and B_{4L} turned on and keeping switches B_{3H} and B_{4H} turned off, one can short out or "clamp" the primary side of the transformer winding in full-bridge B as shown in Figure 2-3. The switches in full-bridge A are then modulated as they would be in full-full mode. This mode of operation where one of the full-bridges is clamped will be referred to as "full-clamped" mode. Since the output of full-bridge B, v_{FB_B}, is clamped to zero, the resonant current i_X is only a function of v_{FB_A}. Without any increase in switching frequency, i_X is halved and the delivered power is thus reduced by a factor of four.

Note that one cannot clamp full-bridge B indefinitely as C_{buf_B} will charge while C_{buf_A} will drain, causing the midpoint voltage between the full-bridges to drift away from $V_{IN}/2$. Thus, in order to keep the midpoint voltage V_{MID} stable while in full-clamped mode, one must periodically switch which full-bridge is being modulated and which one is being clamped at some frequency lower than the switching frequency.

2.3.2 Single Half-bridge Modulation

Within each full-bridge, one can either modulate both half-bridges as in full-full mode or just one half-bridge with the other half-bridge clamped to either ground or V_{IN} as in Figure 2-4. Modulating both half-bridges allows a full-bridge to output a square wave with peak-to-peak amplitude V_{IN}. The corresponding resonant capacitor will have an average voltage of 0 V over a switching cycle.

Switching only one half-bridge in a full-bridge allows that full-bridge to output a square wave with peak-to-peak amplitude $V_{IN}/2$. In this case, the corresponding resonant capacitor will have an average voltage of $\pm V_{IN}/4$ in order to keep the average voltage across the corresponding transformer primary equal to zero. If each of the two full-bridges has only one half-bridge modulating like in Figure 2-4, then the resonant current i_X will be halved and the delivered power will thus be reduced by a factor of four. This will be referred to as "half-half" mode.

There are consequences of having a DC average voltage across the resonant capacitor. When a full-bridge changes from one half-bridge modulating (half) to two half-bridges modulating (full) or zero half-bridges modulating (clamped), the DC voltage stored on the resonant capacitor is discharged and the stored energy is lost. If this switch happens regularly, as would need to happen in a half-clamped mode or a full-half mode in order to keep V_{MID} stable, this power loss can become significant.

2.3.3 Phase Shifting between Full-bridges

When full-bridges A and B are modulated in phase, maximum power is delivered. One can introduce a phase shift between the two full-bridges as another control handle over the resonant current. There are two factors limiting how much this can be pushed in practice. First, if the phase shift is made to be too large, the conditions for ZVS described in section 2.2 will no longer be met. Second, if the full-bridges have a non-zero phase offset, the symmetry between the two full-bridges is lost and the average discharge of the two buffer capacitors C_{buf_A} and C_{buf_B} over a switching cycle will differ as shown in Figure 2-5. As a result, the midpoint voltage V_{MID} will
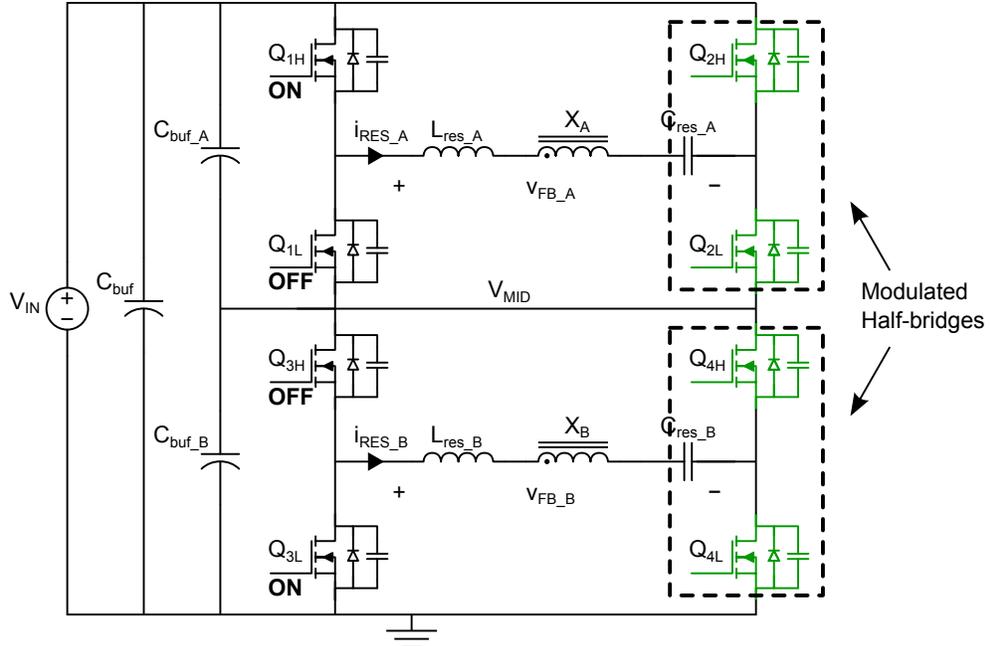
Figure 2-4: Example Control Scheme with Modulation of Half-bridges A2 and B4

start to either rise or fall. Because of the complications introduced by this second fact, this technique was not explored as a means of controlling output power, but as is described later in section 3.5.1, it can be used as a means of regulating V_{MID}.

2.3.4 Summary

Each full-bridge can either be in a full, half, or clamped state. These can be combined to make the operating modes listed in Table 2.1. Because the full-clamped mode provides the same degree of attenuation as the half-half mode without storing DC voltage on the resonant capacitor, the full-clamped mode is the more beneficial new operating mode made possible by the stacked full-bridge architecture and is a major focus of this thesis.

Whenever the converter is run in full-clamped or half-half modes, note that only four switches are being modulated compared to eight switches in full-full mode. This eliminates the switching and gating losses in the unmodulated switches, reducing the negative effects of having doubled the number of switches from the previous converter design. However, no matter what mode the converter is run in, the resonant current

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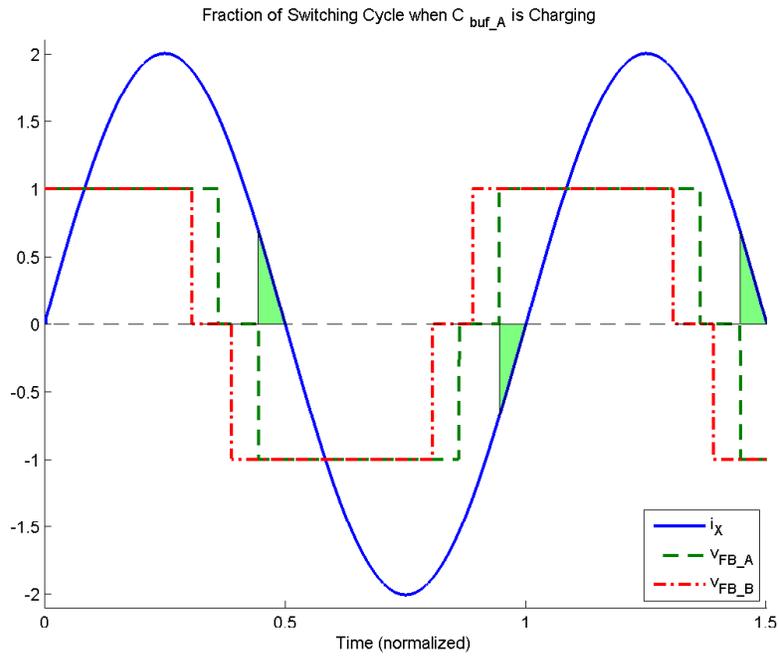
(a) C_{buf_A} is charged for a smaller portion of the switching cycle
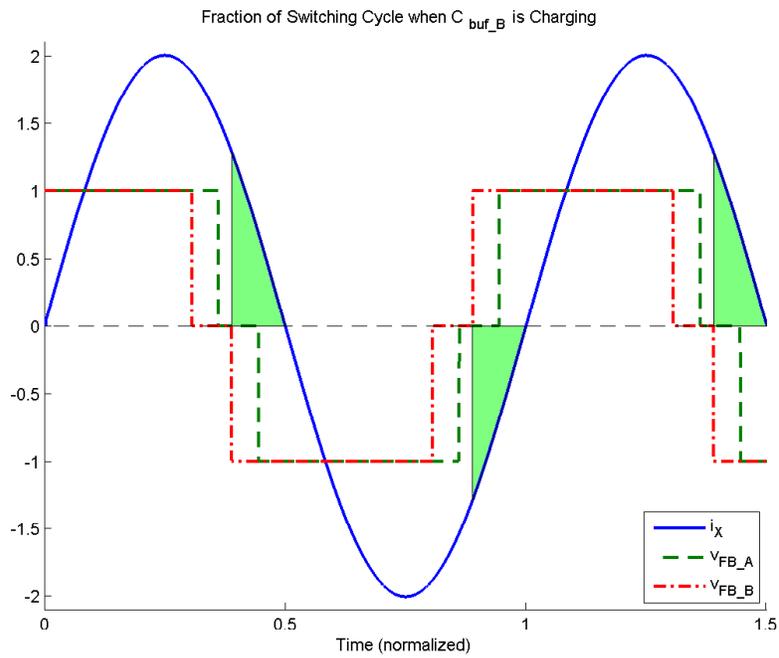
(b) C_{buf_B} is charged for a larger portion of the switching cycle

Figure 2-5: Uneven C_{buf} discharging as a result of phase shift between the full-bridges

Mode	Modulated Half-bridges	Unmodulated Half-bridges	Maximum i_X Level	Maximum $\overline{P}$ Level	Comments
Full-bridge A Full-bridge B	A_1, A_2, B_3, B_4	n/a	100%	100%	
Full-bridge A Half-bridge B	A_1, A_2, B_3	B_4	75%	56.25%	Not preferred
Full-bridge A FB B clamped	A_1, A_2	B_3, B_4	50%	25%	
Half-bridge A Half-bridge B	A_1, B_3	A_2, B_4	50%	25%	Not preferred
Half-bridge A FB B clamped	A_1	A_2, B_3, B_4	25%	6.25%	Not preferred

Table 2.1: Example Modes of Operation

L_{res}	10.29 μH
C_{res}	324 nF
$X : X'$ turns ratio	$1 : 12$
100% average power	100 W

Table 2.2: Specifications of Example Converter from Figure 2-6

will always flow through four switches, giving a mostly constant conduction loss over a switching cycle.

2.4   Benefits of Stacked Full-bridge Topology

As is described in detail in section 2.3, the stacked full-bridge topology affords new control handles to attenuate the resonant current independent of switching frequency. Using these new control modes, especially the "full-clamped" mode, the microinverter can be made to cover the required operating range with a much narrower switching frequency range. This can be directly seen in Figure 2-6, which uses a MATLAB model (see section A.2) to compare the switching frequency required in full-full mode and full-clamped mode for several different operating points of an example converter with the specifications given in Table 2.2. As discussed previously, the narrower frequency range allows for reduced losses in the entire converter and tighter optimization of its passive components.

The increased performance provides more options for the designer. One option is
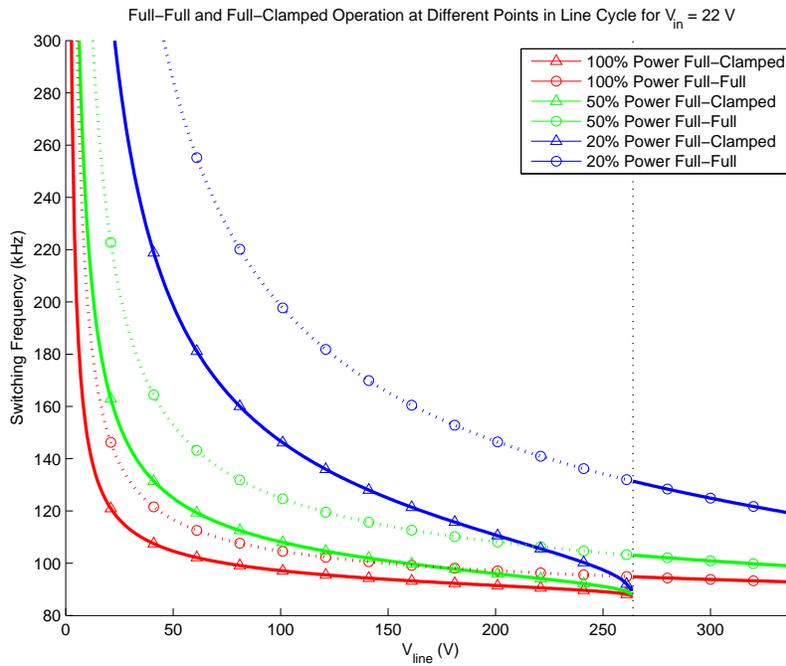
(a) Switching frequency for $V_{IN} = 22$ V. The black dashed line indicates the threshold of using full-clamped
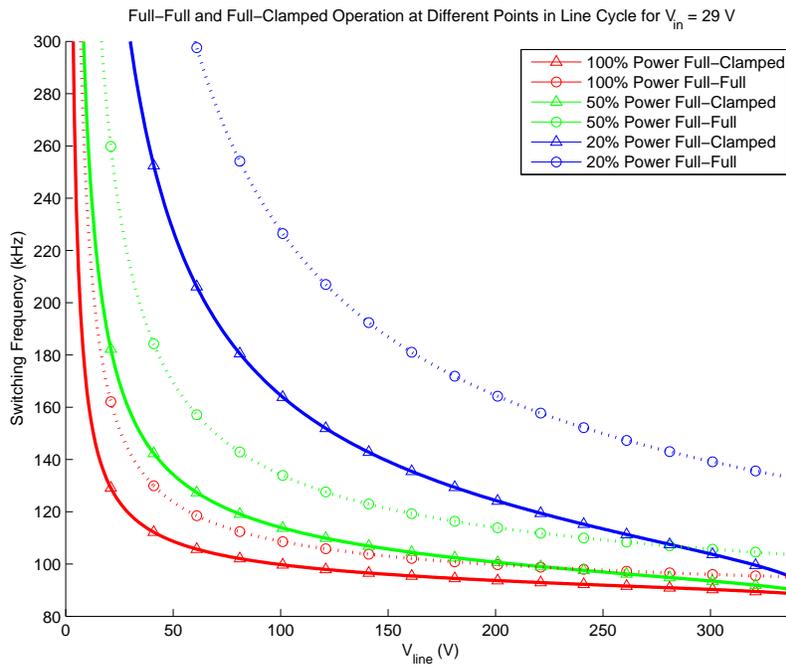
(b) Switching frequency for $V_{IN} = 29$ V. Full-clamped mode is possible for the entire range of output power and line voltage

Figure 2-6: Comparison of switching frequency in full-full and full-clamped modes for different operating points of an example converter with specifications given in Table 2.2

to maintain peak power efficiency but boost efficiency at more unfavorable operating points. One could also aim to optimize peak power efficiency to reduce size and heat extraction requirements while maintaining the same CEC efficiency. Additionally, one could potentially make a converter that is rated over a wider operating range and/or input voltage range than was previously considered feasible.

Although there are now twice as many switches as in the HF inverter of the Trubitsyn et. al. converter, each switch needs to block only $V_{IN}/2$ as opposed to V_{IN}, allowing for the use of lower-voltage, better-performing switches in the inverter section. For an ideal silicon power MOSFET, the on-state resistance and blocking voltage are related by $R_{ds-on} \propto (BV_{DSS})^{2.5}$, so doubling the number of transistors while halving the blocking voltage of each individual switch should produce a net reduction in total conduction losses in the inverter's switches [12]. Comparing the best available low R_{ds-on} transistors in the 30–40 V class to the best available low R_{ds-on} transistors in the 60–75 V class using the $\frac{R_{ds\_on} \cdot Q_g}{V_{gs}}$ metric described in section 3.1.2 shows that the relationship between R_{ds-on} and blocking voltage is closer to linear than the model predicts, but the new HF inverter still has at least 12% less total conduction loss for the same transistor size than the HF inverter of the Trubitsyn et. al. converter if the optimal transistors are selected.

The drop-in nature of the topology gives some flexibility on the manufacturing side. One could feasibly design a printed circuit board (PCB) that can be populated as either a stacked full-bridge or a single full-bridge inverter. A company could offer multiple tiers of microinverter that all use the same base PCB, allowing them to potentially save on production costs.

2.4.1 Effect of Input Voltage Specification

The input voltage range specification shown in Table 1.2 (16–45 V but 22–36 V functional range) actually makes the full-clamped mode of the new converter especially inviting. The transformers' turns ratio must be sized such that the converter can still deliver power in the worst case where the voltage across the primary is at a minimum and the voltage across the secondary is at its maximum. As derived in [1], the absolute

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minimum turns ratio can be calculated as:

$$N_{\min} = \frac{V_{line,\text{peak}}}{2V_{in,\min}} \tag{2.3}$$

For the given specifications, the minimum input voltage is 16 V and maximum line cycle voltage is $240\sqrt{2} \cdot 110\%$. Even though the microinverter efficiency is not considered when the input voltage is betwen 16–22 V, the transformer is sized such that power can still be delivered within that range. Within the range of input voltages where efficiency is actually important (22–36 V), the transformer turns ratio is thus larger than is needed by at least a factor of $\frac{22}{16}$ or 37.5%. With the Trubitsyn et. al. converter, the only practical means of compensating for the excess turns ratio is to increase the resonant tank reactance by increasing switching frequency. The full-clamped mode of the stacked full-bridge topology effectively halves the input voltage, effectively halving the transformer turns ratio and reducing the amount of resonant tank reactance needed and therefore reducing the switching frequency needed. Substituting $\frac{V_{IN}}{2}$ in for V_{IN} in Equation 2.3 shows that the use of full-clamped mode requires:

$$|V_{line}| < N \cdot V_{IN} \tag{2.4}$$

Note that this constraint does not take into account the requirements of ZVS. As $|V_{line}|$ gets close to $N \cdot V_{IN}$ for full-clamped mode or $2 \cdot N \cdot V_{IN}$ for full-full mode, the required switching frequency moves closer to the switching frequency and β moves closer to zero and eventually soft-switching is lost. The controller should add some safety factor to account for this.

2.5   Summary of Control Stategy

The goal of the control scheme of the HF resonant inverter is to minimize total losses in the microinverter at each operating point. For a given operating point, the resonant current is fixed by the input voltage and the desired output power. As a result, the conduction losses in the inverter switches and magnetics are also fixed.

The rest of the losses are composed of frequency-dependent losses like switching losses and gating losses in the inverter and cycloconverter transistors and core losses in the magnetics. As these losses all increase with frequency, the controller should try to minimize switching frequency to minimize total losses.

If the converter operates in full-clamped mode whenever the $\frac{|V_{line}|}{V_{IN}}$ ratio is small enough and makes θ as large as possible while maintaining the $\beta > \alpha$ constraint for ZVS, the switching frequency will be minimized at each operating point.

Chapter 3

Prototype Design

In order to see if the new stacked full-bridge topology performed as expected, a prototype HF inverter was designed and constructed. This chapter discusses the design of the key components of the prototype HF inverter.

3.1 Resonant Inverter Switches

3.1.1 Loss Mechanisms

There are four loss mechanisms in the transistors of the resonant inverter. The on-state resistance R_{ds_on} of the transistor causes resistive conduction losses. At any given time, regardless of operating mode, four switches will be conducting the resonant current. Noting that the resonant currents in both full-bridges are equal ($i_{RES\_A} = i_{RES\_B}$), the total conduction loss can be calculated as follows:

$$P_{\text{conduction}} = 4 \cdot i_{RES\_A}^2 \cdot R_{ds\_on} \tag{3.1}$$

There are losses in the gate drive circuitry owing to the need to charge and discharge the transistors' parasitic gate capacitances in order to turn it on or off. In full-full mode, the gate charge Q_g of each of the eight switches is dissipated once per switching cycle. In full-clamped mode, only half of the switches experience gating loss.

Although the controller must periodically switches which full-bridge is clamped, this occurs at a frequency several times lower than the switching frequency, so the effects on gating loss are negligible. The gating loss can be calculated as follows:

$$P_{\text{gating (full-full)}} = 8 \cdot Q_g \cdot V_{gs} \cdot f_{sw} \tag{3.2}$$

$$P_{\text{gating (full-clamped)}} = 4 \cdot Q_g \cdot V_{gs} \cdot f_{sw} \tag{3.3}$$

Each transistor's output capacitance C_{oss} serves as a capacitive snubber to reduce but not eliminate losses at turn-off. Note that external drain-source capacitance can be added to further reduce these losses. The losses at turn-off are proportional to the square of resonant current. With Figure 2-2 as a reference, if the inverter is controlled to keep $\beta - \alpha$ at a minimum, half of the modulated transistors will be switched near the zero-crossing of i_{RES} and can be approximated as having zero turn-off losses. The other half of the switches are switched near the peak of i_{RES}. Thus, the total turn-off losses can be approximated as:

$$P_{\text{turn-off (full-full)}} \approx 4 \cdot \frac{(i_{RES}\sqrt{2})^2 \cdot t_f^2}{24 \cdot C_{oss}} \cdot f_{sw} \tag{3.4}$$

$$P_{\text{turn-off (full-clamped)}} \approx 2 \cdot \frac{(i_{RES}\sqrt{2})^2 \cdot t_f^2}{24 \cdot C_{oss}} \cdot f_{sw} \tag{3.5}$$

There are losses due to the forward voltage of the transistor body diode in the short period before turn-on when the body diode is carrying the resonant current. If the deadtime of the PWM waveforms is properly set, this diode loss will be negligible, so it will be ignored for the purposes of analysis. Note that the resonant inverter topology is approximated as having no body diode switching losses since it is operated above resonance under zero-voltage switching [11].

3.1.2 Switch Selection

Several different transistors in the 30 V and 40 V range were explored with the goal of finding the switch that had the lowest total losses. A MATLAB script (see Appendix section A.4) estimated the total losses at several different power levels and line voltages for a converter with the same resonant tank as the final prototype. Full-clamped mode was used when possible. Ignoring all losses in the rest of the circuit, a CEC efficiency was calculated for input voltages of 22 V, 29 V, and 36 V. These three numbers were averaged to find an overall efficiency score for each transistor. The switch with the highest score was the Alpha & Omega Semiconductor AON6500 30V MOSFET driven with a V_{gs} of 4.5 V. This switch has maximum $R_{ds\_on} = 1.3$ mΩ and $Q_g = 68$ nC at $V_{gs} = 4.5$ V and $T = 25$ °C.

One can place transistors in parallel or scale up the transistor size to scale down R_{ds_on} while scaling up Q_g and C_{oss} by the same factor, trading increased gating loss for decreased conduction loss and turn-off loss. Accounting for this, the 30V/40V transistors were compared again by finding the minimum $\frac{R_{ds\_on} \cdot Q_g}{V_{gs}}$ product. In this case, the 40 V EPC2015 GaN FET easily outperforms the available silicon MOSFETS in the 30/40 V class.

The EPC2015 GaN FET was chosen for the HF inverter's switches, but they were not paralleled due to the layout complexity that would result from the sheer number of transistors required. Unfortunately, when not paralleled, the GaN transistors do not perform well with high resonant currents due to their relatively large R_{ds_on}. This was not realized until the prototype board had already been made, so in order to obtain reasonable efficiency measurements, the average power specification for the prototype was changed to 0–100 W.

3.2 Resonant Tank

The resonant frequency of the resonant tank was set at 100 kHz with a maximum operating frequency of about 300 kHz as a balance between reducing the peak flux in the RM12 and RM14 magnetic cores of the inductors and transformers and keeping

frequency-dependent losses low. From these two specifications, an L and C were chosen that gave this operating range, using the script in Appendix section A.2 to estimate the needed switching frequency for a range of operating points. Eventually, the resonant inductance was set at 9 μH and the resonant capacitance was set at 324 nF. As a result of the leakage inductance of the transformer, which was unaccounted for in tank design, the actual resonant frequency of the tank dropped to about 87 kHz.

3.2.1   Inductor

Ideally, the resonant inductors should be constructed to minimize total losses. In reality, a balance had to be made between minimizing losses and availability of components. The losses in the inductors are made up of winding losses caused by conduction losses in the inductor windings and core losses caused by eddy currents and hysteresis in the ferromagnetic core. These losses can be calulated as:

$$P_{core} \approx K \cdot f_{sw}^{\alpha} \cdot \Delta B^{\beta} \cdot (\text{core volume}) \tag{3.6}$$

$$P_{winding} = I_{rms}^2 R_{winding} \tag{3.7}$$

K	α	β
$.25 \cdot 10^{-3}$	1.63	2.45

Table 3.1: Ferroxcube 3F3 Core Parameters for 100–300 kHz range and T=100°C from [13]. Units assumed: ΔB in T, f in Hz, core volume in cm^3, core loss in mW

For the core material, Ferroxcube RM12-3F3 ferrite cores were chosen for their performance in the operating frequency range and their availability in the lab. The next step was to choose how many turns should be used, which is determined by the size of the air gap in the core. Losses were estimated using core parameters provided by Ferroxcube ([13]) and shown in Table 3.1 as well as estimates of the voltage waveform across the inductor to calculate the maximum volt-seconds applied to the inductor. The relationship between number of turns and estimated losses for one operating
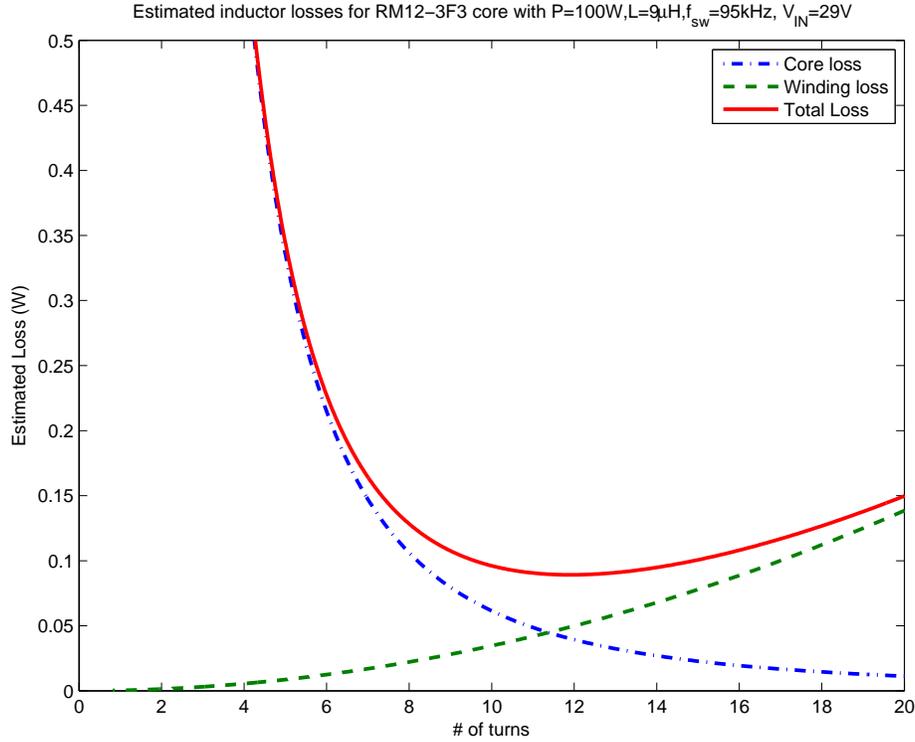
Figure 3-1: Estimated Inductor losses vs. Number of turns for $L = 9\mu H$. The script used to create this computation is in Appendix section A.3.1

point is shown in Figure 3-1 (see Appendix section A.3.1 for the script). Plotting the relationship for multiple operating points showed that the ideal number of turns was consistently between 11–13. However, RM12-3F3 cores with sufficient air gaps needed to maintain $L = 9\mu H$ with this many turns were not readily available. In the interests of time, the inductor was instead wound with only six turns on a RM12-3F3-A250 core. In order to reduce the effects of the skin effect and the proximity effect, the inductor was hand-wound with 525×40 AWG Litz wire. The final product is shown in Figure 3-2.

Using an LCR meter, the inductance and parasitic resistance of the resonant inductors were measured and recorded in Table 3.2. Note that this table does not account for the additional inductance from the leakage inductance of the transformer, which effectively adds about 1.15 μH to L_A and 1.20 μH to L_B. The slight difference in inductance demonstrates the difficulty of tightly controlling the parameters of magnetic components. Although the difference is not ideal, the effect of the asymmetry can be
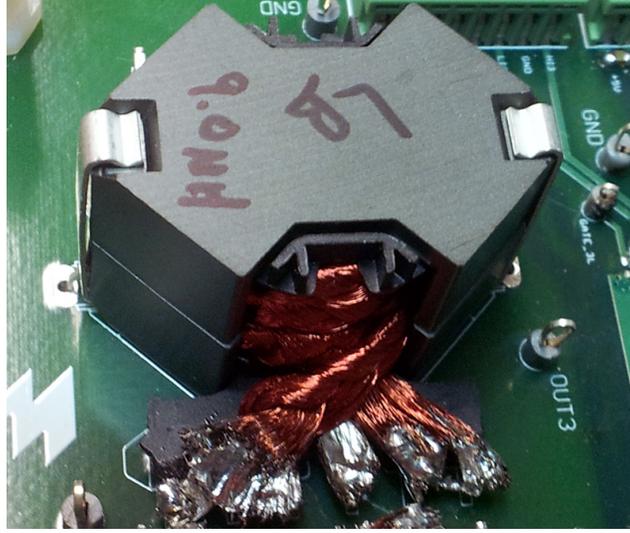
Figure 3-2: Picture of Resonant Inductor L_B

	f_{sw}	100 kHz	125 kHz	150 kHz	175 kHz	200 kHz	250 kHz	300 kHz
L_A	L (μH)	9.09	9.091	9.091	9.091	9.093	9.1	9.1
	R (mΩ)	5.5	7.5	10.5	12.5	16.5	30	40
L_B	L (μH)	9.043	9.044	9.045	9.046	9.05	9.06	9.06
	R (mΩ)	5.5	6.5	10.5	12	20	30	40

Table 3.2: Measured Parameters of Resonant Inductors

compensated for by the controller when stabilizing V_{MID}, as described in section 3.5.1.

3.2.2 Capacitor

A bank of C0G/NP0 ceramic capacitors was used for each resonant capacitor. These capacitors were chosen for their low parasitic resistance and inductance and their small variation with temperature.

3.2.3 Resistive Load

In order to test the prototype, it must be connected to a load resistor with the appropriate resistance given by Equation 2.1 as determined by the output power $\overline{P}$ and line voltage V_{line}. Let us define P_{avg} as the average power delivered over a line cycle. It can be shown that for a given P_{avg}, the load resistance R_{ld} is independent of

desired P_{avg} (W)	100	75	50	30
desired R (Ω)	116.7	155.6	233.4	389.1
measured R (Ω)	114.3	156.5	233.1	399.6
% error	-2.075	.5594	$-.1474$	2.7056

Table 3.3: Ideal and measured load resistances

Figure 3-3: Picture of load resistor corresponding to 75% power

V_{line} and inversely dependent on P_{avg}.

$$V_{line}(\theta) = 240 \text{ V}\sqrt{2}\sin\theta \tag{3.8}$$

$$\overline{P}(\theta) = 2P_{avg}\sin^2\theta \tag{3.9}$$

$$R_{ld}(\theta) = \frac{\frac{2}{\pi^2}V_{line}^2(\theta)}{\overline{P}(\theta)} = \frac{\frac{2}{\pi^2}(240 \text{ V})^2}{P_{avg}} \tag{3.10}$$

Therefore, testing different points on a line cycle for a given P_{avg} does not require one to change the value of the load resistance. The load resistors were made up Barry Industries 100 Ω 150 W model RA1000 power resistors and other thick film power resistors attached to a heat sink. These resistors were chosen for their low parasitic inductance and capacitance compared to wire-wound resistors. By making networks of the available resistors, resistances that come very close to the desired resistances corresponding to 100%, 75%, 50%, and 30% power can be formed as summarized in Table 3.3.

3.3   Transformer

Based on Equation 2.3, the minimum turns ratio for the transformers is 1 : 11.67. This was rounded up to 1 : 12 to be conservative and give some margin for ZVS.

The design process for the transformer is similar to that of the inductor. The goal is still to minimize the sum of winding losses and core losses. The main difference is that there are now two windings, the primary and the secondary. If we assign each winding half of the available winding area, each winding should have about the same winding loss. The inductor loss script can be used with some modifications (see Appendix section A.3.2) to estimate total losses in the transformer as a function of number of primary turns for a given operating point as in Figure 3-4. An ungapped RM14-3F3 core was chosen to minimize the magnetizing current and provide extra room to hold both windings.

After iterating through multiple operating points, it was found that the optimal number of primary turns was four turns. Again Litz wire was used to reduce the skin effect and proximity effect. The primary winding was made up of 4 turns of 525 × 40 AWG Litz wire, and the secondary winding is made up of 48 turns of 50 × 40 AWG Litz wire, wound over the top of the primary. Because the Litz wire was unserved and the voltage between the primary and secondary windings can be hundreds of volts, the primary winding was insulated from the secondary winding by electrical tape.

3.4   Printed circuit board (PCB)

The final prototype PCB produced is shown in Figure 3-6. A lot of attention was made to reduce the area of signal and power loops to reduce parasitic inductances, especially in the GaN transistor gate drive loops. The GaN transistor gates are very sensitive to overvoltage. Ringing due to parasitic inductance in the gate drive loop led to the destruction of many transistors and rendered the first prototype board useless. After minimizing the area of the loop, the ringing disappeared.

Figure 3-7 shows a closeup of a half-bridge and its corresponding gate drive chip.
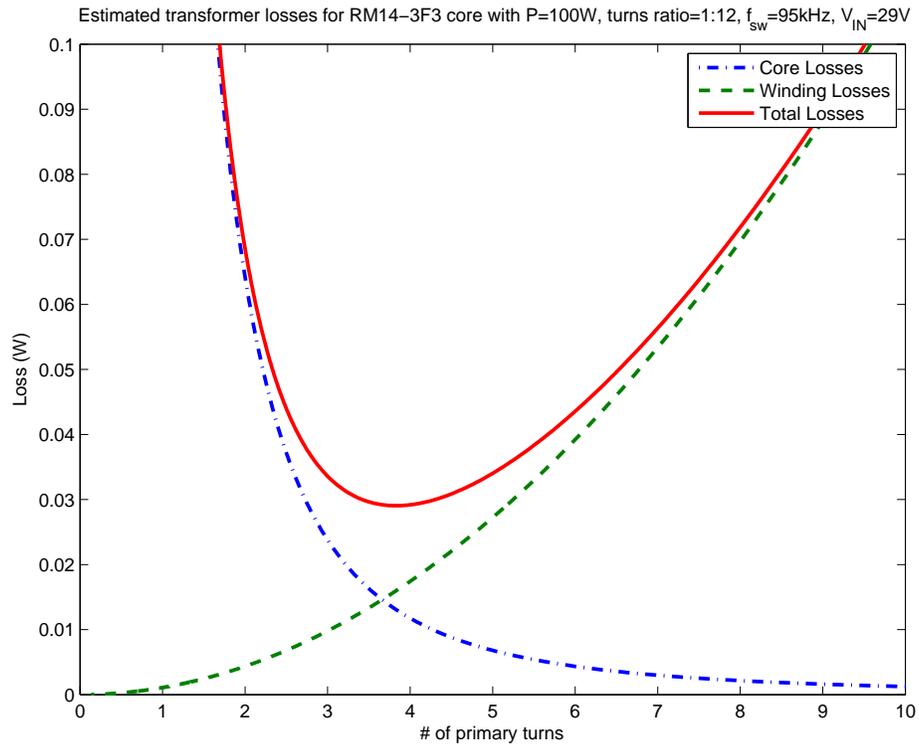
Figure 3-4: Estimated transformer losses vs. Number of primary turns for 1:12 turns ratio

Figure 3-5: Picture of Tranformer X_B
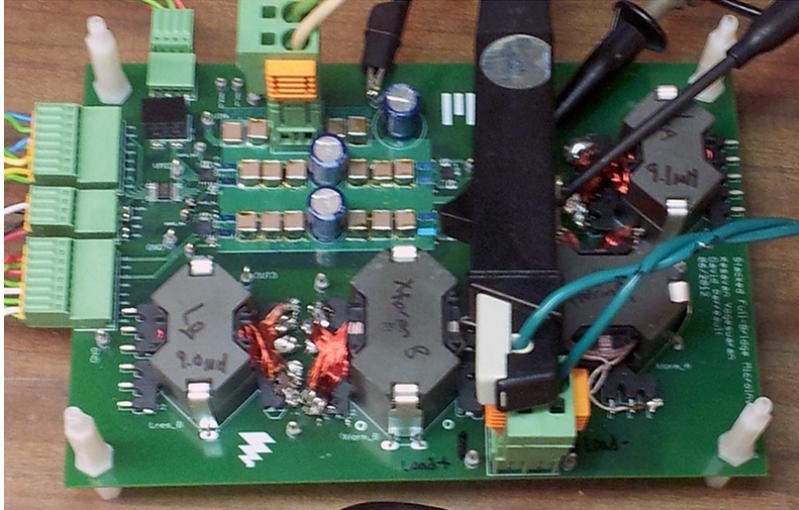
Figure 3-6: Picture of Prototype PCB

The tight gate drive requirements and complexity of the layout required the use of four copper layers. See Appendix section C to see a complete schematic and bill of materials of the final prototype, as well as images of the PCB layout.

3.5 Microcontroller

All control of the prototype is handled by a microcontroller. The Texas Instruments TMS320F28335 Delfino$^{\text{TM}}$ 32-bit microcontroller was chosen for the task because of its speed (150 MHz) and its surplus of useful peripherals like PWM's with built-in deadtime generation, ADC's, and timers. The evaluation board used is shown in Figure 3-8. The microcontroller is connected to LM5113 gate driver chips on the prototype board so that it can individually control each of the transistors on the board. On the prototype board, V_{IN} and V_{MID} are scaled down by resistor dividers and connected to the ADC of the microcontroller. All of these connections are made using twisted-pair wire in order to reduce cross-talk between the wires.

3.5.1 V_{MID} Stabilization

The controller must keep V_{MID} as close to $V_{IN}/2$ as possible. IF V_{MID} drifts too high or low, the drain-source voltage across some of the inverter's switches will
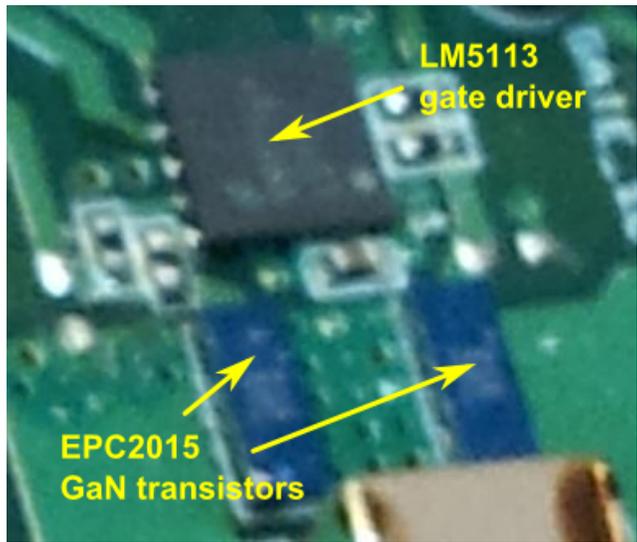
Figure 3-7: Closeup of half-bridge layout
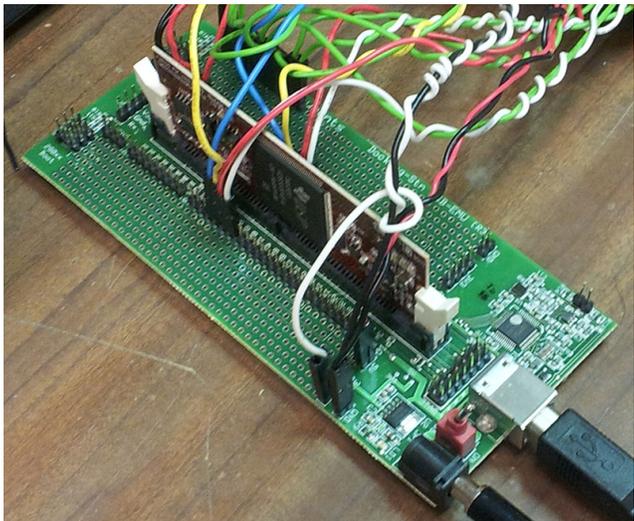
Figure 3-8: Picture of TI microcontroller evaluation board used for control

exceed their rating and destroy them. The switches are rated to block $V_{IN}/2$, not V_{IN}. V_{MID} will drift if some asymmetry between the two full-bridges arises and causes the discharge rates of C_{buf_A} and C_{buf_B} to be different.

The gate drive signals for full-bridge A must pass through a logic isolator (ADI ADUM7440ARQZ) because the bridge is referenced to V_{MID} instead of ground. This isolator has a small propagation delay (≈ 80 ns) that adds a phase shift between the full-bridges. Recalling Figure 2-5, any phase shift between the full-bridges will cause an uneven discharge between the buffer capacitors. Small differences in the values of the resonant components of each bridge also cause asymmetry.

In order to compensate and keep V_{MID} stable in full-full mode, the controller reads V_{IN} and V_{MID} every few switching cycles and depending on whether V_{MID} is too high or too low, a positive or negative phase shift is added between the full-bridges to bring it back to the center. The larger the buffer capacitors and faster the sampling frequency, the less V_{MID} will drift.

Running in full-clamped mode also introduces a huge asymmetry, and it cannot be dealt with using phase-shifting since only one full-bridge is active. The first attempt at compensating for this also sampled V_{IN} and V_{MID} every few switching cycles and switched which full-bridge is clamped and which is modulated once V_{MID} drifted out of an acceptable range around $V_{IN}/2$. On average, V_{MID} correctly remained at $V_{IN}/2$, but especially at higher power levels, the ripple in V_{MID} climbed to a few volts of peak-to-peak amplitude. Instead, the controller switches which full-bridge is clamped and which is modulated after a fixed number of cycles. This number of cycles was tweaked for each operating point—lower output powers allowed for longer time between switching—but otherwise it remained fixed.

The V_{MID} stabilization routine and the rest of the control code can be found in section B.

Chapter 4

Results

This chapter discusses the testing setup and calculations used to measure the efficiency of the HF inverter portion of the microinverter across the operating range (in particular, the CEC efficiency range). While only the HF inverter is tested (rather than a full microinverter, which includes the conversion from high-frequency down to 60 Hz), we can test the HF inverter at the operating points that would be relevant for a full microinverter, and compute an equivalent CEC efficiency for the HF inverter stage. In this chapter we measure the equivalent CEC efficiency of the inverter section and provide the measured results. In order to display the efficacy of the full-clamped mode allowed by the stacked full-bridge topology, the inverter's CEC efficiency was calculated for the case where full-clamped mode is used whenever possible. This was compared to the CEC efficiency of the HF inverter when it is always running in full-full mode. This is intended to roughly simulate the performance of the HF inverter section of the Trubitsyn et. al. converter.

4.1   CEC Efficiency Calculation

The CEC efficiency, as defined in Table 1.1, is an average of the efficiency at different power levels. To reduce the total number of measurements needed, the weights of the 20% and 10% power levels were added to the 30% power level such that the 30% power level had a weight of .21. This is justified by the fact that these two

power levels account for only a small fraction (9%) of the total CEC metric, though full-clamped mode is especially beneficial at those lower power levels.

The efficiency at each power level can be calculated as the ratio of the energy that would be delivered by the inverter to the load over a line cycle to the energy that would be supplied to the inverter over a line cycle. Input and output power of the HF inverter are measured over a set of operating points corresponding to those at different points in the line cycle, and the relative energies that would be delivered at those operating points computed by numerical integration as followed:

$$\text{Energy} = \int_0^{\frac{\pi}{2}} P(\phi) \, d\phi \tag{4.1}$$

$$\approx \sum_{n=1}^{N} \frac{1}{2}[P(\phi_n) + P(\phi_{n-1})](\phi_n - \phi_{n-1}) \tag{4.2}$$

$$P(\phi = 0) = 0 \tag{4.3}$$

In general, measurements were taken at line cycle phases of 15°, 30°, 45°, 75°, and 90°. To account for slight errors in output power, the equivalent phase angle ϕ at a given operating point was back calculated from the measured output power as:

$$P_{out}(\phi) = 2P_{avg} \sin^2 \phi \tag{4.4}$$

$$\therefore \phi = \sin^{-1}\left(\sqrt{\frac{P_{out}}{2P_{avg}}}\right) \tag{4.5}$$

4.2 Testing scheme

The CEC efficiency as described above was calculated for input voltages of 22 V and 34 V. The latter voltage was the highest possible input voltage available on the power supply used, and it is expected that the performance at this input voltage is similar to the performance at the maximum possible input voltage, 36 V. At each operating point, θ was set to give about 10° of margin for ZVS in order to minimize

the switching frequency f_{sw}. The deadtime of each half-bridge was fixed at 33.3 nanoseconds. Then, measurements were taken to measure the power supplied to and delivered by the prototype.

In order to measure power delivered into the load resistor, the RMS voltage across the load was measured with a Tektronix P5205 isolated high voltage differential probe and the RMS calculation function of the oscilloscope was used to calculate its RMS value. The impedance characteristics of the load in the range of operating frequencies were measured beforehand with an LCR meter. The load reactance was insignificant so the output power could simply be calculated as $P_{out} = \frac{V_{load}^2}{R_{load}}$ where V_{load} is the measured RMS load voltage over a switching cycle.

In order to control for resistance variation with temperature, the load resistor was left to cool to room temperature before each measurement was taken, and measurements were taken before the temperature of the load rose more than 15 °C. A large fan forced air through the load resistors' heat sink to slow the rate of temperature rise and to accelerate cooling between measurements. The load temperature was monitored via thermocouples connected to a Digi-Sense benchtop scanning thermometer.

For most of the operating points, V_{IN} came from an HP6643A power supply. When more than 6 A of input current was needed, a Kepco KLP 150-16-1.2K power supply was used. In order to measure the power delivered by the V_{IN} power supply, an Agilent 34330A precision 1 mΩ shunt was connected in series with the supply. The voltage across the shunt was measured with an HP/Agilent 34401A multimeter to determine the input current. The supply voltage was read off from the front panel display after having been verified with a HP/Agilent 34401A multimeter. A common-mode choke was connected in series with the supply to increase the accuracy and reliability of the measurements. Power to the microcontroller and gate drivers was supplied by a separate Tektronix PS280 power supply. The power delivered by this supply was not taken into account in the measurements and efficiency calculation.
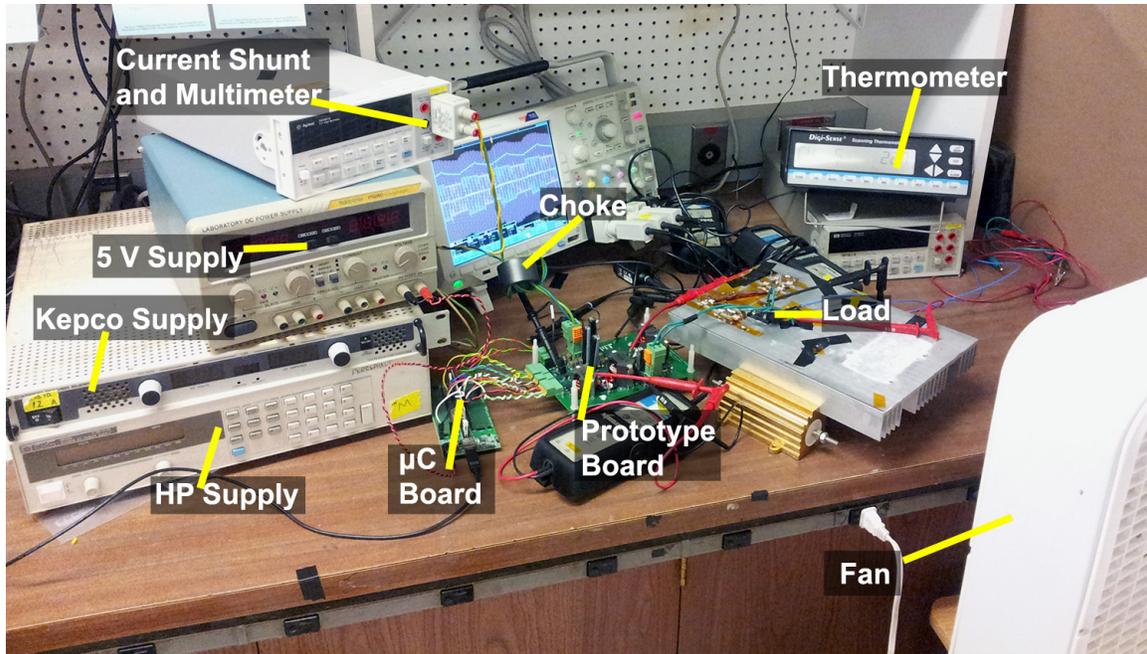
Figure 4-1: Picture of Testing setup

4.3   Data

The collected data is shown in Tables 4.1, 4.2, 4.3, and 4.4. For an input voltage of 22 V, the equivalent CEC efficiency was 90.24% when operation was limited to full-full mode and increased to 90.41% when full-clamped mode was used whenever possible. For an input voltage of 34 V, the equivalent CEC efficiency increased from 89.97% to 90.83% when full-clamped mode was used whenever possible.

When the input voltage was 22 V, there were several operating points where full-clamped mode could not be run, which correspond to the points in the line cycle where $|V_{line}| > N \cdot V_{IN}$. Whenever full-clamped mode could be used, it was always beneficial, though only marginally so when the input voltage was 22 V. The mode had a much bigger impact on efficiency when the input voltage was 34 V since the full turns ratio of the transformer was not needed.

Chapter 5 will discuss the significance of these results and suggest possible improvements for the future.

% P_{max}	Line Phase	P_{in} (W)	P_{out} (W)	f_{sw} (kHz)	$E_{tot,in}$	$E_{tot,out}$	Efficiency
	14.99°	15.76	13.37	98.68			
	30.09°	59.33	50.27	93.52			
100	45.05°	118.6	100.2	91.24	173.21	145.47	83.99%
	74.94°	223.3	186.5	89.71			
	87.09°	237.4	199.5	89.50			
	14.98°	11.29	10.02	100.27			
	30.08°	42.11	37.69	96.15			
	41.24°	74.84	65.18	93.28			
75	44.82°	84.94	74.53	92.36	125.56	110.03	87.63%
	60.01°	127.75	112.52	91.46			
	74.30°	159.54	139.02	90.58			
	86.96°	172.17	149.58	90.58			
	15.03°	7.39	6.73	117.19			
	29.90°	26.93	24.84	101.08			
50	45.02°	54.16	50.04	95.91	83.90	77.64	92.53%
	75.78°	101.24	93.97	92.59			
	90°	108.8	100.4	92.59			
	15.01°	4.37	4.02	123.36			
	30.03°	15.61	15.03	112.27			
30	44.64°	31.09	29.73	104.17	48.49	46.56	96.01%
	75.63°	58.56	56.31	98.17			
	90°	62.22	60.12	97.15			

Table 4.1: Data for $V_{IN} = 22$ V and full-full operation. The CEC efficiency is 90.2360%

% P_{max}	Line Phase	P_{in} (W)	P_{out} (W)	f_{sw} (kHz)	$E_{tot,in}$	$E_{tot,out}$	Efficiency
	15.16°	15.98	13.68	93.28			
	30.13°	58.59	50.40	89.93			
100	45.05°	118.6	100.2	91.24*	172.94	145.48	84.12%
	74.94°	223.3	186.5	89.71*			
	87.09°	237.4	199.5	89.50*			
	15.00°	11.23	10.05	98.94			
	30.04°	41.624	37.59	90.58			
	41.24°	73.546	65.18	88.24			
75	44.82°	84.94	74.53	92.36*	125.29	110.03	87.82%
	60.01°	127.75	112.52	91.46*			
	74.30°	159.54	139.02	90.58*			
	86.96°	172.17	149.58	90.58*			
	15.07°	7.28	6.76	100.00			
	30.24°	27.46	24.37	93.05			
50	45.02°	54.16	50.04	95.91*	83.86	77.63	92.58%
	75.78°	101.24	93.97	92.59*			
	90°	108.8	100.4	92.59*			
	15.01°	4.27	4.02	107.14			
	29.95°	15.29	14.95	97.40			
30	44.64°	30.98	29.73	90.36	48.36	46.56	96.28%
	75.63°	58.56	56.31	98.17*			
	90°	62.22	60.12	97.15*			

Table 4.2: Data for $V_{IN} = 22$ V and full-full & full-clamped operation. The CEC efficiency is 90.4106%. An asterisk in the f_{sw} column indicates that full-clamped mode could not be used for that operating point

% P_{max}	Line Phase	P_{in} (W)	P_{out} (W)	f_{sw} (kHz)	$E_{tot,in}$	$E_{tot,out}$	Efficiency
100	14.99°	15.84	13.38	102.74	164.97	136.98	83.03%
	29.96°	58.75	49.87	96.40			
	45.97°	124.92	103.37	93.98			
	74.22°	223.45	185.22	92.36			
	84.50°	240.14	198.16	91.91			
75	14.98°	11.39	10.02	104.46	125.35	110.06	87.80%
	30.08°	42.30	37.69	98.43			
	44.82°	84.69	74.53	95.66			
	59.49°	126.65	111.34	94.46			
	75.01°	160.38	139.96	93.05			
	86.96°	170.68	149.58	92.59			
50	15.00°	7.55	6.70	118.11	84.24	77.78	92.34%
	30.11°	27.17	25.17	106.23			
	45.02°	54.60	50.04	100.27			
	74.33°	99.72	92.70	96.90			
	90°	109.14	100.42	96.15			
30	14.99°	4.60	4.01	147.64	49.23	46.64	94.74%
	29.91°	15.88	14.91	119.05			
	44.74°	31.31	29.73	110.95			
	74.21°	58.51	55.56	106.23			
	90°	63.07	60.12	105.63			

Table 4.3: Data for $V_{IN} = 34$ V and full-full operation. The CEC efficiency is 89.9712%.

% P_{max}	Line Phase	P_{in} (W)	P_{out} (W)	f_{sw} (kHz)	$E_{tot,in}$	$E_{tot,out}$	Efficiency
100	14.95°	15.57	13.31	96.40	161.96	136.45	84.25%
	29.96°	58.00	49.87	91.91			
	45.05°	118.12	100.17	89.93			
	75.68°	224.74	187.77	87.82			
	84.50°	235.62	198.16	87.41			
75	14.98°	11.29	10.02	98.43	123.91	110.07	88.83%
	30.04°	41.99	37.59	93.28			
	44.82°	83.98	74.53	91.24			
	59.86°	126.31	112.18	89.71			
	75.01°	157.96	139.96	88.65			
	86.96°	168.06	149.58	88.24			
50	14.96°	7.40	6.66	106.23	83.68	77.82	92.99%
	30.14°	27.05	25.20	96.90			
	45.02°	53.89	50.04	93.98			
	74.33°	99.31	92.70	90.58			
	90°	108.77	100.69	89.93			
30	15.01°	4.57	4.02	127.12	44.88	42.76	95.27%
	30.08°	15.86	15.07	106.23			
	44.74°	31.25	29.73	98.94			
	74.21°	58.17	55.56	93.05			
	86.19°	62.05	59.74	92.36			

Table 4.4: Data for $V_{IN} = 34$ V and full-full & full-clamped operation. The CEC efficiency is 90.8272%.

a	−1.060µs	10.9 V
b	−23.00ns	10.9 V
	△1.037µs	△0.00 V

1	10.0 V	2	10.0 V	3	50.0 V	4	2.00 V

	Value	Mean	Min	Max	Std Dev
3 Frequency	92.44kHz	92.59k	92.03k	93.01k	233.9
4 Mean	11.0 V	10.9	10.8	11.1	50.3m
3 RMS	159 V	155	152	159	1.79

2.00µs   500MS/s   3   ∫   0.00 V
→▼0.00000 s   10k points
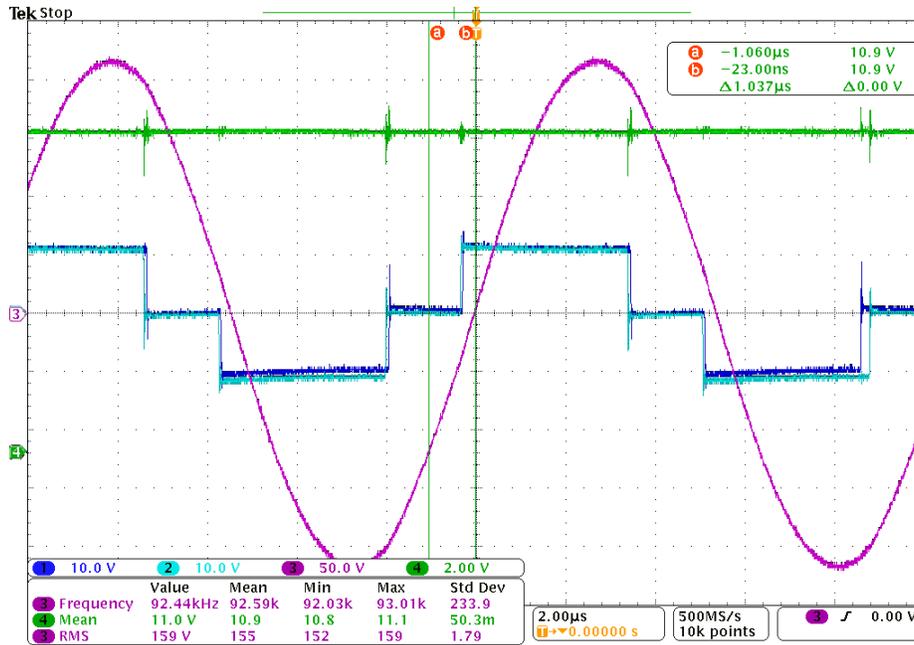
Figure 4-2: Oscilloscope waveforms showing conditions for ZVS being met for one operating point with $V_{IN} = 22$ V, $\overline{P} = 100$ W, $R_{ld} = 233.1\Omega$. magenta: v_{LOAD}, green: V_{MID}, teal: v_{FB_A}, blue: v_{FB_B}

4.4 Waveforms

Several oscilloscope waveforms showing typical converter operation were saved. Figures 4-2, 4-3, and 4-4 demonstrate ZVS conditions in the inverter's switches. Figure 4-5 shows how each full-bridge alternates between modulating and clamping in full-clamped mode.

1 5.00 V		**3** 50.0 V	**4** 1.00 V	

	Value	Mean	Min	Max	Std Dev
3 Frequency	----.Hz	No period found			
4 Mean	2.31 V	2.31	2.31	2.31	399µ
3 RMS	199 V	199	199	199	350m

40.0ns 2.50GS/s **4** ∫ 1.30 V
⊓→▼0.00000 s 10k points
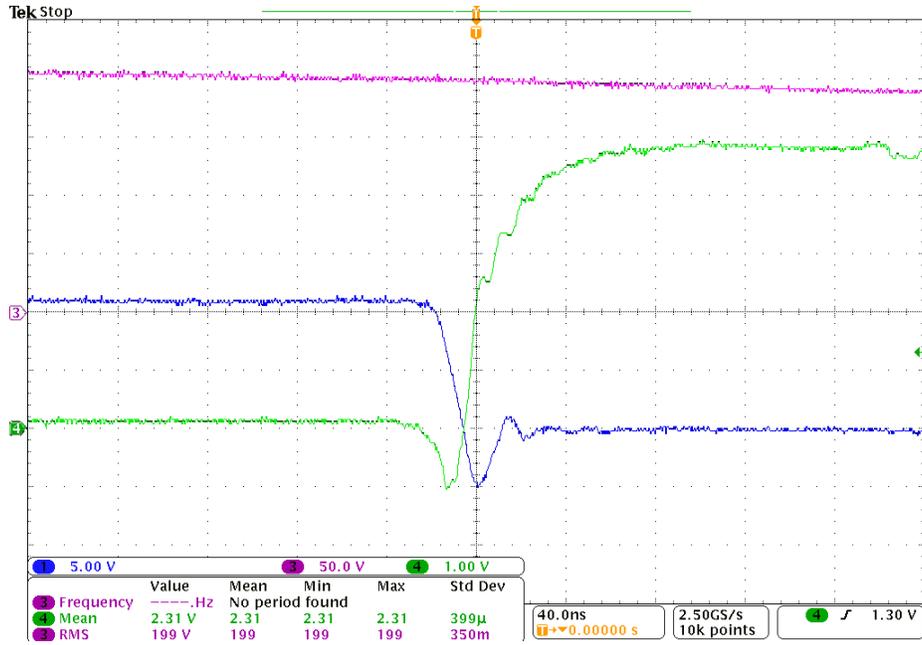
Figure 4-3: Oscilloscope waveforms showing turn-on of transistor Q_{3L} with $V_{IN} = 22$ V, $\overline{P} = 100$ W, $R_{ld} = 233.1\Omega$. Note how v_{DS} has fallen to zero before v_{GS} rises. It is noted that more detailed tuning of switch deadtime could have further reduced the conduction loss component associated with body diode conduction. magenta: v_{LOAD}, green: v_{GS}, blue: v_{DS}

1 5.00 V		**3** 50.0 V	**4** 1.00 V	

	Value	Mean	Min	Max	Std Dev
3 Frequency	23.31MHz	Low signal amplitude			
4 Mean	2.23 V	2.21	2.19	2.23	16.2m
3 RMS	201 V	200	196	201	1.91

20.0ns 2.50GS/s **4** ⌐ 1.30 V
⊓→▼0.00000 s 10k points
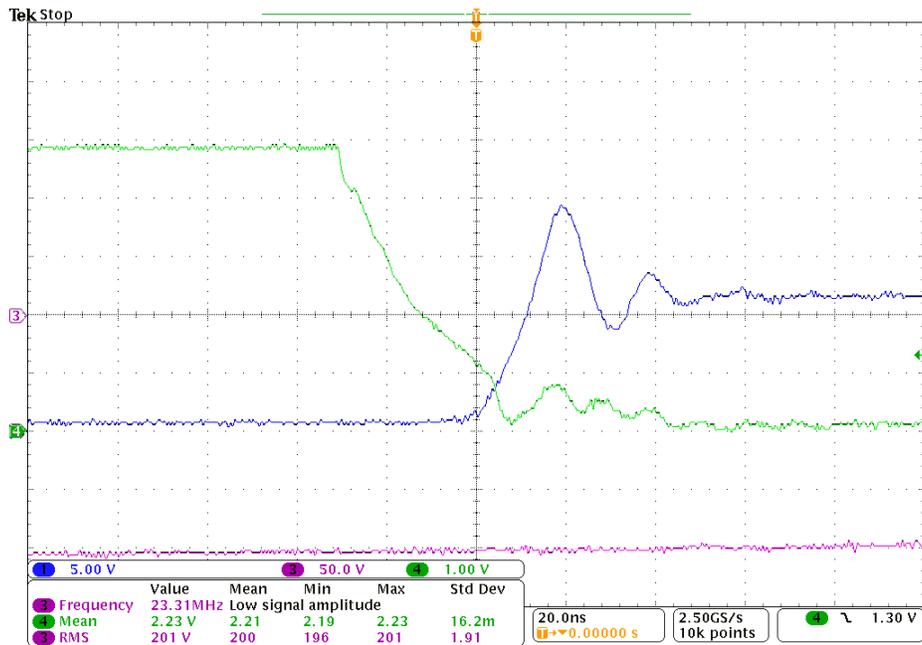
Figure 4-4: Oscilloscope waveforms showing turn-off of transistor Q_{3L} with $V_{IN} = 22$ V, $\overline{P} = 100$ W, $R_{ld} = 233.1\Omega$. Note how small the overlap between the rise of v_{DS} and the fall of v_{GS} is. magenta: v_{LOAD}, green: v_{GS}, blue: v_{DS}
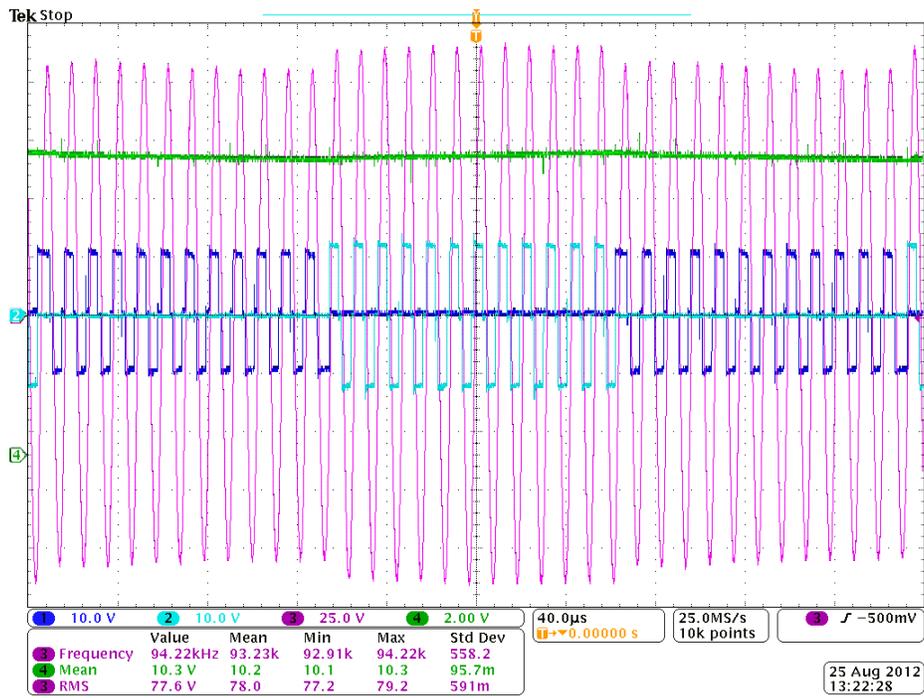
Figure 4-5: Oscilloscope waveforms from full-clamped operation with $V_{IN} = 22$ V, $\overline{P} = 26$ W, $R_{ld} = 233.1\Omega$. magenta: v_{LOAD}, green: V_{MID}, teal: v_{FB_A}, blue: v_{FB_B}

Chapter 5

Conclusions

This chapter analyzes the results recorded in Chapter 4, seeking to explain the significance of trends in the data. It also explores improvements that should be made in the future based on observations made during the measurement process.

5.1 Summary

As predicted, when full-clamped mode was introduced for each operating point, the switching frequency needed at that point decreased and the efficiency increased. These effects are summarized for 100% power, 50% power, and 30% power in Figures 5-1 and 5-2. Furthermore, as the ratio between V_{line} and V_{IN} increases (i.e., for lower instantaneous line voltages), the effectiveness of full-clamped mode in reducing switching frequency and boosting efficiency also increases. These results demonstrate that the stacked full-bridge topology successfully improves upon the previous work.

5.2 Analysis

Contrary to expectation, the results seem to indicate that the HF inverter's efficiency increases significantly as the output power $\overline{P}$ decreases. The load resistance increases in size as $\overline{P}$ decreases, and more power is dissipated in the load relative to the power dissipated in the parasitic resistances and on-state resistances in the
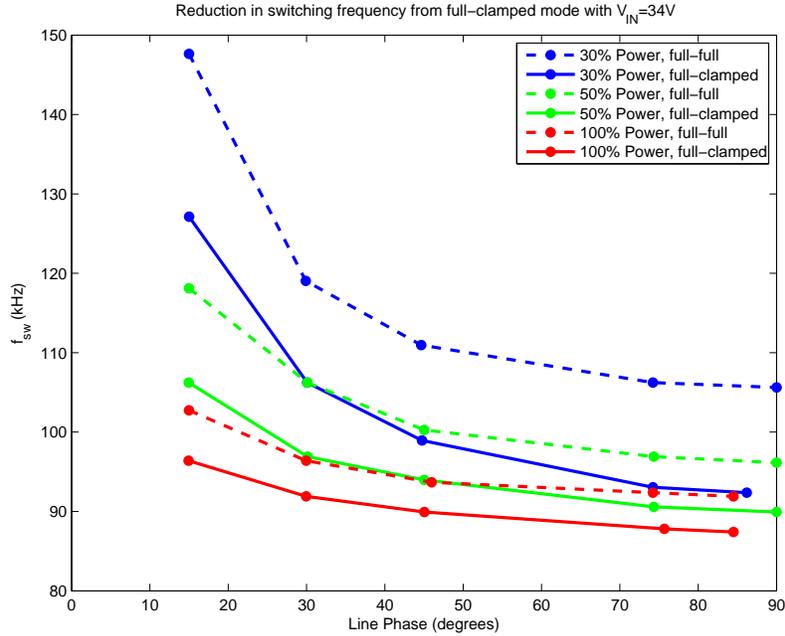
Figure 5-1: Measured reduction in switching frequency when using full-clamped mode with $V_{IN} = 34$ V

resonant current's path. However, there is another factor at play that was masked by the measurement setup. As the load resistance increases, the quality factor Q of the resonant tank decreases, so higher-order harmonics are less attenuated. In a full microinverter where the HF inverter has a cycloconverter load, how the harmonic currents are related to actual delivered power are different than in a purely resistive load. In fact, harmonic currents may generate no power whatsoever, depending on the cycloconverter voltage waveform. With a resistive load, however, all of the harmonics deliver power into the load with equal measure, so the measurements taken artificially deflate the switching frequencies—and the frequency-dependent losses in the switches and magnetics—especially at the lower output power levels. This likely explains the apparent increase in efficiency as $\overline{P}$ is decreased. It does not prevent comparisons between full-full and full-clamped mode to be made, and in fact, it has the consequence of undervaluing the benefits of using full-clamped mode at these lower output powers.

Observing full-clamped operation, particularly at higher power levels, revealed another difficulty with control. As shown in Figure 5-3, for operating points with high resonant current—a consequence of high output power—the C_{buf} capacitors drained
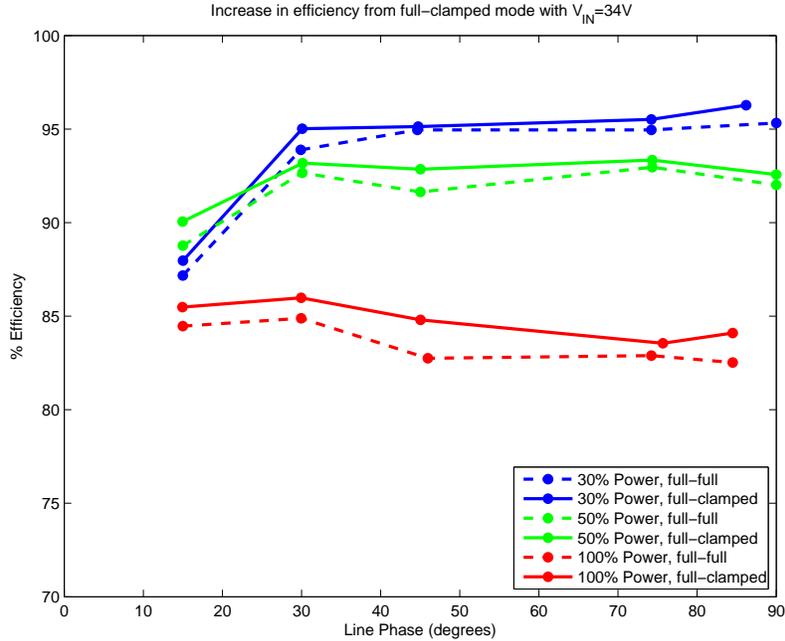
Figure 5-2: Measured increase in efficiency when using full-clamped mode with $V_{IN} = 34$ V

faster and there was both ripple and steady-state error in V_{MID}. The unbalanced state of the full-bridges had the effect of changing the power delivered to the load depending on which full-bridge was clamped and which was modulated, reducing the efficiency and benefit of the full-clamped mode. Several different control schemes were experimented with and it was found that reducing steady-state error increased efficiency by a couple of percentage points. However, a solution that combined low ripple and load steady-state error could not be found. This issue is specific to this prototype. Each full-bridge was buffered by twenty-four 22 μF ceramic capacitors and a 680 μF electrolytic capacitor, but a full microinverter system needs many times more capacitance to buffer the twice-line-frequency variation in output power. This capacitance would virtually eliminate any ripple in V_{MID} and make it much easier to control.
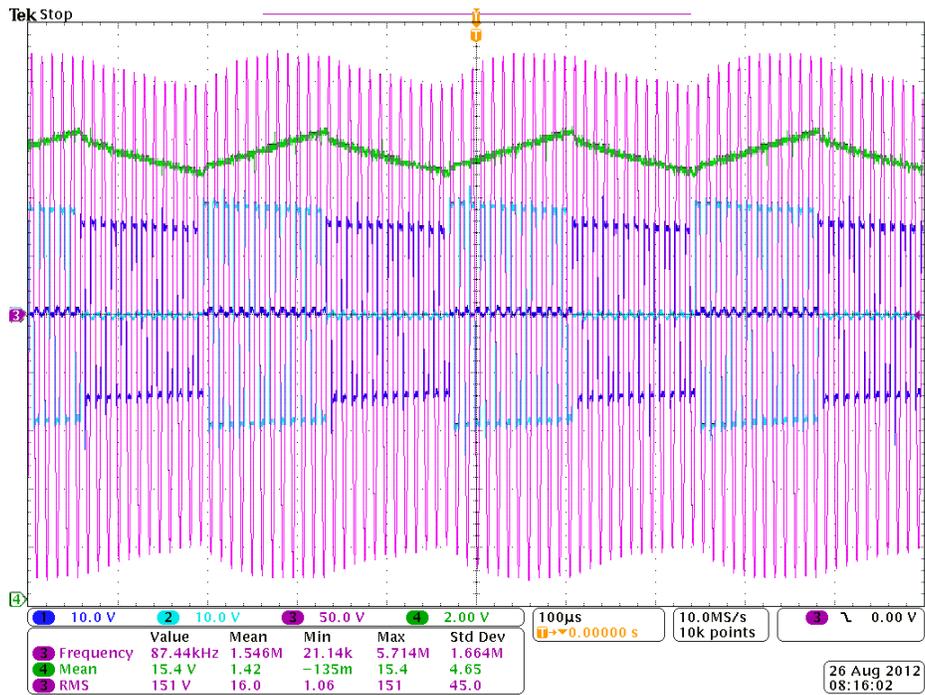
Figure 5-3: Oscilloscope waveforms showing V_{MID} ripple and unbalanced full-bridge outputs when operating at $\overline{P} = 200$ W and $V_{IN} = 34$ V in full-clamped mode. Note that the mean of V_{MID} is 1.6 V less than $V_{IN}/2$. magenta: v_{LOAD}, green: V_{MID}, teal: v_{FB_A}, blue: v_{FB_B}

5.3 Suggested Improvements for Future Work

There is some additional optimization that needs to be done to fully realize the benefits of the stacked full-bridge topology and bring the overall efficiency of the HF inverter up to more practical levels.

The magnetics design should be optimized further, especially with regards to core loss in the inductors. The inductor cores were hot to the touch after sustained operation. Also, unless it is desired to operate the converter at higher frequencies, the GaN FETs should be paralleled to minimize conduction losses, since switching losses in the transistors were insignificant. If this proves impossible due to cost constraints or layout constraints, a silicon solution is likely a better choice. As the optimal choice of switches and magnetics used is tied to the resonant frequency and Q of the resonant tank, it is possible that using a different resonant tank can result in better overall performance.

In order to stabilize V_{MID} and get the most out of the full-clamped mode of operation, more buffer capacitance should be added, and the V_{MID} and V_{IN} measurement method and stabilization routine for full-clamped mode should be optimized further. This could mean varying the frequency at which the controller switches the active full-bridge depending on the operating point or using a more sophisticated feedback loop.

Once the HF inverter design and control have been optimized further, it should be tested with a cycloconverter load so that a more complete efficiency analysis can be performed. Testing with a cycloconverter will ensure that higher-order harmonics do not corrupt the efficiency measurement and will introduce some additional frequency-dependent losses. Both of these effects should increase the benefit seen by using full-clamped mode. A cycloconverter also provides some additional control handles to use at very low output levels.

Eventually, once the full converter has been shown to work for static operating points, the control system must be modified to dynamically control the system to work with a 50/60 Hz AC line voltage.

Appendix A

MATLAB Scripts

This chapter contains MATLAB scripts that were referenced in the thesis. When multiple files are given, they should all be placed in the same folder for the scripts to work.

A.1   Switching Frequency vs. Power Output

```
%This script estimates the relationship between switching frequency and
%output power. It does not try to pick an optimal theta or to use
%full-clamped mode to minimize switching frequency. It uses the impedance
%of the resonant tank to calculate what the the power output would be for a
%given input voltage. The inductor and capacitor are assumed to be on the
%primary side.

clc

L = 3.9e-6; %Trubitsyn converter
C = 4.4e-6; %Trubitsyn conveter
Vin = 36;
theta = 90; %degrees
fres=1/(2*pi*sqrt(L*C))/1e3;

Pavg=1:.1:175; %Range of average output power to search through
Vline = 240;
N_turns = 7.5;

R=(2/pi^2*Vline^2./Pavg)/(N_turns^2); %Calculate equivalent resistive load
                                      %of cycloconverter when reflected to
```

63

```
                                %primary side

f=1e3*[45:.01:400]; %range of frequencies to search through
w=2*pi*f;
fopt = zeros(size(Pavg)); %operating frequency vector corresponding to Pavg

for k = 1:length(Pavg)
    Vr = Vin*cosd(theta/2)*R(k)./(R(k)+j*w*L+1./(j*w*C)); %Voltage across resistive load
    P = abs(Vr).^2/R(k); %power delivered to resistor
    fopt(k) = f(find(abs(P-Pavg(k))==(min(abs(P-Pavg(k))))))/1e3; %find operating frequency
end
figure(2)
plot(fopt,Pavg/175*100,'k')
xlim([45 350])
ylim([0 100])
xlabel('Switching Frequency (kHz)')
ylabel('Average Output Power over Switching Cycle (% of Maximum)')
title('Switching Frequency vs. Output Power at V_{IN}=36V, V_{LINE}=240V, and \theta=90^\circ')
```

A.2   Full-Full vs. Full-Clamped Switching Frequency Comparison

full_clamped_fsw_comparison.m

```
% full_clamped_fsw_comparison.m
% 3/07/2012
% Kesavan Yogeswaran
%
% This script plots the switching frequency required in full-full and
% full-clamped modes over the entire line cycle. Multiple lines for
% different output powers are plotted, and there is a different plot for
% each input voltage specified. The power of full-clamped mode to reduce
% switching frequency is demonstrated

clear
close all

L = 10.29e-6*144;
C = .324e-6/144;
N_turns = 12;
rds = 4.896e-3;
Qg = 10.5e-9;
```

```
Vgs = 5;
Pavg = 100;


Vin = [22 29];


for k = 1:length(Vin)

    V_thresh = Vin(k)*N_turns; %Threshold of using full-clamped


    Vout_clamped = [1:1:V_thresh]';
    Pout_clamped = Vout_clamped.^2/(240^2/Pavg)*[1 .5 .2];


    %Vout_full1 = Vout_clamped;
    %Pout_full1 = Pout_clamped;
    Vout_full = [V_thresh:1:240*sqrt(2)]';
    Pout_full = Vout_full.^2/(240^2/Pavg)*[1 .5 .2];



    fsw_clamped = zeros(size(Pout_clamped));
    fsw_full1 = fsw_clamped;
    for i = 1:length(Vout_clamped)
        fsw_clamped(i,:) = mosfet_fsw_fullclamped(rds,Qg, ...
            Pout_clamped(i,:),Vout_clamped(i),Vin(k),Vgs,L,C,N_turns);
        fsw_full1(i,:) = mosfet_fsw_fullfull(rds,Qg,Pout_clamped(i,:), ...
            Vout_clamped(i),Vin(k),Vgs,L,C,N_turns);
    end


    fsw_full = zeros(size(Pout_full));
    for i = 1:length(Vout_full)
        fsw_full(i,:) = mosfet_fsw_fullfull(rds,Qg,Pout_full(i,:), ...
            Vout_full(i),Vin(k),Vgs,L,C,N_turns);
    end


    figure(k)
    hold on
    %Hack to make legend look nice
    plot([0],[1000],'r^-')
    plot([0],[1000],'ro-')
    plot([0],[1000],'g^-')
    plot([0],[1000],'go-')
    plot([0],[1000],'b^-')
    plot([0],[1000],'bo-')


    %Plot data points
    ds = 20;
```

```matlab
    plot(downsample(Vout_clamped,ds),downsample( ...
        fsw_clamped(:,1)/1000,ds),'r^')
    plot(downsample([Vout_clamped; Vout_full],ds), ...
        downsample([fsw_full1(:,1); fsw_full(:,1)]/1000,ds),'ro')


    plot(downsample(Vout_clamped,ds),downsample( ...
        fsw_clamped(:,2)/1000,ds),'g^')
    plot(downsample([Vout_clamped; Vout_full],ds), ...
        downsample([fsw_full1(:,2); fsw_full(:,2)]/1000,ds),'go')


    plot(downsample(Vout_clamped,ds),downsample( ...
        fsw_clamped(:,3)/1000,ds),'b^')
    plot(downsample([Vout_clamped; Vout_full],ds), ...
        downsample([fsw_full1(:,3); fsw_full(:,3)]/1000,ds),'bo')


    %Connect the dots
    plot(Vout_clamped,fsw_clamped(:,1)/1000,'r-','LineWidth',2)
    plot(Vout_clamped,fsw_clamped(:,2)/1000,'g-','LineWidth',2)
    plot(Vout_clamped,fsw_clamped(:,3)/1000,'b-','LineWidth',2)

    plot(Vout_full,fsw_full(:,1)/1000,'r-','LineWidth',2)
    plot(Vout_full,fsw_full(:,2)/1000,'g-','LineWidth',2)
    plot(Vout_full,fsw_full(:,3)/1000,'b-','LineWidth',2)

    plot(Vout_clamped,fsw_full1(:,1)/1000,'r:','LineWidth',2)
    plot(Vout_clamped,fsw_full1(:,2)/1000,'g:','LineWidth',2)
    plot(Vout_clamped,fsw_full1(:,3)/1000,'b:','LineWidth',2)

    line([V_thresh V_thresh],[0 600],'Color','k','LineStyle',':', ...
        'LineWidth',1)

    xlabel('V_{line} (V)')
    ylabel('Switching Frequency (kHz)')
    title(['Full-Full and Full-Clamped Operation at Different ', ...
        'Points in Line Cycle for V_{in} = ',num2str(Vin(k)),' V'])
    ylim([80 300])
    xlim([0 240*sqrt(2)])
    legend('100% Power Full-Clamped','100% Power Full-Full', ...
        '50% Power Full-Clamped','50% Power Full-Full', ...
        '20% Power Full-Clamped','20% Power Full-Full')
    hold off
end
```

mosfet_fsw_fullclamped.m

```matlab
function fsw = mosfet_fsw_fullclamped(rds,Qg,Pout,Vout,Vin,Vgs,L,C,N_turns)
```

```
    ZVS_phase_margin = 10*pi/180; %10 degrees


    Ires_rms = Pout/Vout*pi/sqrt(2);
    Req = 2/pi^2*Vout^2./Pout;
    Z = (4/pi*Vin/sqrt(2))*N_turns./Ires_rms;


    b = -Req/L*tan(ZVS_phase_margin);
    c = -1/(L*C);
    fsw_min = (-b/2+sqrt(b.^2-4*c)/2)/(2*pi);


    if Vout > 2*(Vin/2)*N_turns   %Converter operation is impossible
        error('Vout/(Vin*N_turns) ratio too high for converter to run')
    else
        %Assume converter is running in full-clamped mode with no phase
        %shift between half-bridges
        Zhalf = Z/2;
        df = 100000;
        b = (Req/L).^2-2/(L*C)-(Zhalf/L).^2;
        c = 1/(L*C)^2;
        fsw_half = sqrt((-b/2+sqrt(b.^2-4*c)/2))/(2*pi);


        f=zeros(df+1,length(Req));
        for i = 1:length(Req)
            f(:,i) = [fsw_min(i):(fsw_half(i)-fsw_min(i))/df:fsw_half(i)]';
        end


        Ztank = 1./(1i*2*pi*f*C)+1i*2*pi*f*L+ones(df+1,1)*Req;
        Ires_rms_tank = cos(angle(Ztank)-ZVS_phase_margin)*4/pi* ...
            N_turns*(Vin/2)./abs(Ztank)/sqrt(2);


        err = abs(Ires_rms_tank-ones(df+1,1)*Ires_rms);
        min_err = min(err,[],1);


        fsw = zeros(size(Req));
        for i = 1:length(Req)
            fsw(i) = f(err(:,i) == min_err(i),i);
        end
    end
end
```

mosfet_fsw_fullfull.m

```
function fsw = mosfet_fsw_fullfull(rds,Qg,Pout,Vout,Vin,Vgs,L,C,N_turns)


    ZVS_phase_margin = 10*pi/180; %10 degrees
```

```
    Ires_rms = Pout/Vout*pi/sqrt(2);

    Req = 2/pi^2*Vout^2./Pout;

    Z = (4/pi*Vin/sqrt(2))*N_turns./Ires_rms;


    b = -Req/L*tan(ZVS_phase_margin);

    c = -1/(L*C);

    fsw_min = (-b/2+sqrt(b.^2-4*c)/2)/(2*pi);


    if Vout > 2*Vin*N_turns   %Converter operation is impossible

        error('Vout/(Vin*N_turns) ratio too high for converter to run')

    else

        %Assume both full-bridges running in phase with no phase shift

        %between half-bridges

        b = (Req/L).^2-2/(L*C)-(Z/L).^2;

        c = 1/(L*C)^2;

        fsw_full = sqrt((-b/2+sqrt(b.^2-4*c)/2))/(2*pi);


        df = 100000;

        f=zeros(df+1,length(Req));

        for i = 1:length(Req)

            f(:,i) = [fsw_min(i):(fsw_full(i)-fsw_min(i))/df:fsw_full(i)]';

        end

        Ztank = 1./(1i*2*pi*f*C)+1i*2*pi*f*L+ones(df+1,1)*Req;

        Ires_rms_tank = cos(angle(Ztank)-ZVS_phase_margin)*4/pi* ...

            N_turns*Vin./abs(Ztank)/sqrt(2);

        err = abs(Ires_rms_tank-ones(df+1,1)*Ires_rms);

        min_err = min(err,[],1);


        fsw = zeros(size(Req));

        for i = 1:length(Req)

            fsw(i) = f(err(:,i) == min_err(i),i);

        end

    end

end
```

A.3   Magnetics design

A.3.1   Inductor

```
% inductor_optimizer.m
% Kesavan Yogeswaran
%
% This script estimates the winding loss and core loss for an inductor and
```

```
% finds the optimal A_l and number of turns for a given inductance and
% operating point.

clc

P=100; %output power
Vin=29;
L=9e-6;
f=95e3; %optimize for this frequency
%Steinmetz parameters (3F3)
%P = Kfe*(B)^beta*Ac*lm
Ac = 146e-6; %core cross-sectional area RM12
lm = 56.6e-3; %core mean magnetic path length RM12
Kfe = .25e-3*f^1.63*1000; %3F3 parameters from Ferroxcube
beta = 2.45; %3F3 parameters from Ferroxcube

%Copper loss parameters
pc = 1.7e-8; %resistivity of copper (ohms m)
MLT = 61e-3; %mean length of turn RM12
Wa = 75e-6; %winding area RM12
Ku = .85*.66; %packing factor (estimate)
Itot = P/Vin/.92; %assumes 92% efficiency

%For sinusoidal voltage waveform with rms amplitude Vrms,
%lambda = Vrms*sqrt(2)/pi*1/f
Vrms = Itot*2*pi*f*L;
lambda = Vrms*sqrt(2)/pi*1/f; %peak volt-seconds across inductor
B = 0:.0001:.4;
n1 = lambda./(2*B*Ac);
Pfe = Kfe*B.^beta*Ac*lm; %core loss
Pcu = pc*lambda^2*Itot^2/(4*Ku)*MLT/(Wa*Ac^2)*1./(B.^2); %winding loss

figure(1)
plot(n1,Pfe,'-.',n1,Pcu,'--',n1,(Pfe+Pcu),'-','LineWidth',2)
legend('Core loss','Winding loss','Total Loss')
xlabel('# of turns')
ylabel('Estimated Loss (W)')
title(['Estimated inductor losses for RM12 core with P=100W,L=9\mu{}H,' ...
    'f_{sw}=95kHz, V_{IN}=29V'])

xlim([0 20])
ylim([0 .5])
Bopt = (pc*lambda^2*Itot^2/(2*Ku)*MLT/(Wa*Ac^3*lm)* ...
    1/(beta*Kfe))^(1/(beta+2))
n1opt = lambda/(2*Bopt*Ac)
```

```
Al = L/n1opt^2*1e9
```

A.3.2   Transformer

This script is largely similar to the inductor loss estimation script in section A.3.1. The only differences are that the core parameters are different because an RM14 core is used, the winding loss is now doubled to account for both windings, and the peak flux estimate is different, but everything else is the same.

```
% transformer_flux_optimizer.m
% Kesavan Yogeswaran
%
% This script estimates the winding loss and core loss for a transformer
% and finds the optimal A_l and number of primary turns for a given turns
% ratio and operating point.

clc

f=95e3; %optimize for this frequency
Pavg = 100;
Vin=29;
%Steinmetz parameters (3F3)
%P = Kfe*(B)^beta*Ac*lm
Ac = 198e-6; %core cross-sectional area (RM14)
lm = 70e-3; %core mean magnetic path length (RM14)
Kfe = .25e-3*f^1.63*1000; %3F3 parameters from Ferroxcube
beta = 2.45; %3F3 parameters from Ferroxcube

%Copper loss parameters (RM14)
pc = 1.7e-8; %resistivity of copper (ohms m)
MLT = 71e-3; %mean length of turn (RM14)
Wa = 111e-6; %Winding area (RM14)
Ku = .85*.66; %packing factor
Itot = 2*Pavg/Vin/.92; %assumes 92% efficiency

%lambda = (29/2)/(2*f); %make sure to double-check saturation
%For sinusoidal voltage waveform with rms amplitude Vrms,
%lambda = Vrms*sqrt(2)/pi*1/f
%Vrms = sqrt(2)/pi*240/(2*12)
lambda = (sqrt(2)/pi*240/(2*12))*sqrt(2)/pi*1/f;
B = 0:.0001:.4;
n1 = lambda./(2*B*Ac);
Pfe = Kfe*B.^beta*Ac*lm;
Pcu = pc*lambda^2*Itot^2/(4*Ku)*MLT/(Wa*Ac^2)*1./(B.^2);
%Pcu2 = pc*MLT*6^2*Itot^2/(Wa*Ku)
```

```
%plot(B,Pfe,B,Pcu,B,Pfe+Pcu)
plot(n1,Pfe,'-.',n1,Pcu,'--',n1,Pfe+Pcu,'LineWidth',2)
legend('Core Losses','Winding Losses', 'Total Losses')
%xlabel('B [H]')
xlabel('# of primary turns')
ylabel('Loss (W)')
title(['Estimated transformer losses for RM14-3F3 core with P=100W, ' ...
    'turns ratio=1:12, f_{sw}=95kHz, V_{IN}=29V'])

xlim([0 10])
ylim([0 .1])
Bopt = (pc*lambda^2*Itot^2/(2*Ku)*MLT/(Wa*Ac^3*lm) ...
    *1/(beta*Kfe))^(1/(beta+2))
n1opt = lambda/(2*Bopt*Ac)
```

A.4   Switch Comparison

After searching through data for several different 30 V and 40 V switches, the following promising transistors were investigated: FDMS7650, FDMS7650, PSMN1R2-30YLC, SIR640DP, BSC011N03LSI, AON6500, PSMN1R0-30YLC, EPC2015. When r_{ds_on} and Q_g data were given for multiple values of V_{gs}, the script was run for with each value of V_{gs}.

mosfet_comparison.m

```
% mosfet_comparison.m
% 7/13/2011
% Kesavan Yogeswaran
%
% This script finds the MOSFET that yields the best CEC efficiency, as
% estimated by efficiency_calc.m. Note that this may depend on L, C, and
% the number of turns.

N_turns = 12;
%script was originally written for resonant tank on secondary so we must
%reflect everything over to the secondary side
L = 10.29e-6*N_turns^2;
C = .324e-6/N_turns^2;

%parameters from the transistors are stored in MOSFETs.csv as follows:
%first column: rds_on (ohms)
```

```
%third column: Qg (nC)
%fourth column: Vgs (V)
MOSFETs = importdata('MOSFETs.csv');
MOSFETs = MOSFETs.data;


% Modes:
% 1 - Old
% 2 - New - Full-clamped when possible. Otherwise full-full
% 3 - New - Full-full
mode = 2;


max_eff = 0;
for i = 1:length(MOSFETs)
    rds = MOSFETs(i,1);
    Qg = MOSFETs(i,3)*1e-9;
    Vgs = MOSFETs(i,4);
    Coss = MOSFETs(i,5);
    tf = MOSFETs(i,6);
    eff = mean([efficiency_calc(rds,Qg,Vgs,Coss,tf,22,L,C,N_turns,mode);
        efficiency_calc(rds,Qg,Vgs,Coss,tf,29,L,C,N_turns,mode);
        efficiency_calc(rds,Qg,Vgs,Coss,tf,36,L,C,N_turns,mode)]);
    if eff > max_eff
        max_eff = eff;
        best = [rds*1e3 Qg*1e9 Vgs Coss*1e12 tf*1e9];
    end
end


max_eff %display maximum efficiency
best %display parameters of best switch
```

efficiency_calc.m

```
% efficiency_calc.m
% 7/12/2011
% Kesavan Yogeswaran
%
% This script estimates the CEC efficiency of the converter given MOSFET
% parameters. It uses mosfet_losses.m to estimate losses at different
% operating points of the inverter.
% Modes (for mosfet_losses):
% 1 - Old
% 2 - New - Full-clamped when possible. Otherwise full-full
% 3 - New - Full-full


function CEC_eff = efficiency_calc(rds,Qg,Vgs,Coss,tf,Vin,L,C,N_turns,mode)
```

```
        CEC_POWER = [10 20 30 50 75 100]/100;
        CEC_WEIGHT = [.04 .05 .12 .21 .53 .05];
        phase = pi*[.125 .25 .375 .5];


        Vline = 240*sqrt(2)*sin(phase);
        Pout_full = 250*2*sin(phase).^2; %maximum average power of 250 W


        losses = zeros(length(phase),length(CEC_POWER));


        for i = 1:length(phase)
            losses(i,1:end) = mosfet_losses(rds,Qg,Pout_full(i)*CEC_POWER, ...
                Vline(i),Vin,Vgs,Coss,tf,L,C,N_turns,mode);
        end


        Pout = Pout_full'*CEC_POWER;
        Pin = Pout+losses;
        trap = ones(length(phase),length(CEC_POWER));
        trap(end,:) = .5;


        Pout = sum(trap.*Pout);
        Pin = sum(trap.*Pin);


        eff = Pout./Pin;
        CEC_eff = sum(eff.*CEC_WEIGHT);
end
```

mosfet_losses.m

```
% Returns MOSFET losses for a given operating point. Considers conduction
% and gating losses. Accepts a vector for Pout.
%
% Modes:
% 1 - Old
% 2 - New - Full-clamped when possible. Otherwise full-full
% 3 - New - Full-full

function losses = mosfet_losses(rds,Qg,Pout,Vout,Vin,Vgs,Coss,tf,L,C,...
    N_turns,mode)


    ZVS_phase_margin = 10*pi/180; %10 degrees


    Ires_rms = Pout/Vout*pi/sqrt(2);
    Req = 2/pi^2*Vout^2./Pout;
    Z = (4/pi*Vin/sqrt(2))*N_turns./Ires_rms;


    %Find the frequency that gives a current phase shift equal to our ZVS
```

```matlab
%phase margin. This is the minimum frequency we could run at and be
%sure of soft-switching.
b = -Req/L*tan(ZVS_phase_margin);
c = -1/(L*C);
fsw_min = (-b/2+sqrt(b.^2-4*c)/2)/(2*pi);


if Vout > 2*Vin*N_turns   %Converter operation is impossible
    error(['Vout/(Vin*N_turns) ratio too high for converter to ', ...
        'run. Try increasing N_turns'])
else
    %Calculate switching frequency needed for desired output with no
    %phase-shift between half-bridges. This is the maximum switching
    %frequency we should need to operate at for this operating point.
    b = (Req/L).^2-2/(L*C)-(Z/L).^2;
    c = 1/(L*C)^2;
    fsw_full = sqrt((-b/2+sqrt(b.^2-4*c)/2))/(2*pi);

    if fsw_full < fsw_min
        error('Too close to voltage limit for soft-switching. ', ...
            'Try increasing N_turns')
    end


    %Search the frequency space for the frequency that yields the
    %correct resonant current and minimum ZVS phase margin.
    df = 100000;
    f=zeros(df+1,length(Req));
    for i = 1:length(Req)
        f(:,i) = [fsw_min(i):(fsw_full(i)-fsw_min(i))/df:fsw_full(i)]';
    end
    Ztank = 1./(1i*2*pi*f*C)+1i*2*pi*f*L+ones(df+1,1)*Req;
    Ires_rms_tank = cos(angle(Ztank)-ZVS_phase_margin)* ...
        4/pi*N_turns*Vin./abs(Ztank)/sqrt(2);
    err = abs(Ires_rms_tank-ones(df+1,1)*Ires_rms);
    min_err = min(err,[],1);


    fsw = zeros(size(Req));
    for i = 1:length(Req)
        fsw(i) = f(err(:,i) == min_err(i),i);
    end


    if mode == 1 %Old design (single full-bridge)
        cond_loss = 2*(Ires_rms*N_turns).^2 * rds;
        gate_loss = 4*Qg*Vgs*fsw;
        turnoff_loss = 2*Ires_rms.^2*2*tf^2/(24*Coss).*fsw;
    else %Stacked bridges
```

```matlab
            cond_loss = 4*(Ires_rms*N_turns).^2 * rds;
            gate_loss = 8*Qg*Vgs*fsw;
            turnoff_loss = 4*Ires_rms.^2*2*tf^2/(24*Coss).*fsw;
        end
        losses = cond_loss+gate_loss+turnoff_loss;


        if mode == 2 && Vout < 2*(Vin/2)*N_turns %Converter operation in
                                    %full-clamped mode might be possible


            Zhalf = Z/2;


            b = (Req/L).^2-2/(L*C)-(Zhalf/L).^2;
            c = 1/(L*C)^2;
            fsw_half = sqrt((-b/2+sqrt(b.^2-4*c)/2))/(2*pi);


            if fsw_half > fsw_min %Ensure soft-switching
                f=zeros(df+1,length(Req));
                for i = 1:length(Req)
                    f(:,i) = [fsw_min(i):(fsw_half(i)-fsw_min(i))/df: ...
                        fsw_half(i)]';
                end


                Ztank = 1./(1i*2*pi*f*C)+1i*2*pi*f*L+ones(df+1,1)*Req;
                Ires_rms_tank = cos(angle(Ztank)-ZVS_phase_margin)* ...
                    4/pi*N_turns*(Vin/2)./abs(Ztank)/sqrt(2);


                err = abs(Ires_rms_tank-ones(df+1,1)*Ires_rms);
                min_err = min(err,[],1);


                fsw2 = zeros(size(Req));
                for i = 1:length(Req)
                    fsw2(i) = f(err(:,i) == min_err(i),i);
                end


                cond_loss_half = 4*(Ires_rms*N_turns).^2 * rds;
                gate_loss_half = 4*Qg*Vgs*fsw2;
                turnoff_loss = 2*Ires_rms.^2*2*tf^2/(24*Coss).*fsw;
                losses = cond_loss_half+gate_loss_half+turnoff_loss;
            end
        end
    end
end
```

Appendix B

Microprocessor Code

The operating mode, switching frequency, θ, and deadtime are defined near the beginning.

```c
#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File

// Prototype statements for functions found within this file.
void InitEPwm1Example(void);
void InitEPwm2Example(void);
void InitEPwm3Example(void);
void InitEPwm4Example(void);
//interrupt void cpu_timer0_isr(void);
//interrupt void cpu_timer1_isr(void);
interrupt void epwm1_timer_isr(void);
/*interrupt void epwm2_isr(void);
interrupt void epwm3_isr(void);*/

// Global variables used in this example
Uint16 Voltage1;
Uint16 Voltage2;
Uint16 LR_PHASE_SHIFT;
Uint16 toggler;
Uint16  EPwm1TimerIntCount;
Uint16 FB_HALF_PERIOD;

#define FB_PERIOD 858 //Set timer period 75 MHz/XX
#define LR_THETA 0 //theta = half-bridge phase-shift (degrees);
//cannot be between 90-2700/FB_PERIOD or 90+3600/FB_PERIOD in full-clamped
#define FB_OFFSET 0 //Offset = XX/(150 MHz); Phase = 180*XX/TBPRD
#define DEADBAND_LENGTH_LEAD 5 //deadtime = XX/150 MHz in leading leg (2,4)
#define DEADBAND_LENGTH_LAG 5 //deadtime = XX/150 MHz in lagging leg (1,3)
#define FULL_CLAMPED_MODE 1 //0 for full-full; 1 for full-clamped

void main(void)
{
// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
   InitSysCtrl();
```

```
   EALLOW;
   #if (CPU_FRQ_150MHZ)     // Default - 150 MHz SYSCLKOUT
      #define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 150/(2*3)  = 25.0 MHz
   #endif
   #if (CPU_FRQ_100MHZ)
      #define ADC_MODCLK 0x2 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 100/(2*2)   = 25.0 MHz
   #endif
   EDIS;

   // Define ADCCLK clock frequency ( less than or equal to 25 MHz )
   // Assuming InitSysCtrl() has set SYSCLKOUT to 150 MHz
   EALLOW;
   SysCtrlRegs.HISPCP.all = ADC_MODCLK;
   EDIS;

// Step 2. Initalize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
// InitGpio();  // Skipped for this example

// For this case just init GPIO pins for ePWM1, ePWM2, ePWM3, ePWM4
// These functions are in the DSP2833x_EPwm.c file
   InitEPwm1Gpio();
   InitEPwm2Gpio();
   InitEPwm3Gpio();
   InitEPwm4Gpio();

// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW;  // This is needed to write to EALLOW protected registers
   //PieVectTable.TINT0 = &cpu_timer0_isr;
   //PieVectTable.XINT13 = &cpu_timer1_isr;
   PieVectTable.EPWM1_INT = &epwm1_timer_isr;
   EDIS;    // This is needed to disable write to EALLOW protected registers

// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals();  // Not required for this example
```

```
    InitAdc();  // For this example, init the ADC
    //InitCpuTimers();


/*#if (CPU_FRQ_150MHZ)
// Configure CPU-Timer 0
// 150MHz CPU Freq, 35 microsecond Period (in uSeconds)
// This controls how often the ADC samples Vmid and Vin


    //ConfigCpuTimer(&CpuTimer0, 150, 35); //~28.6 kHz
    ConfigCpuTimer(&CpuTimer0, 150, 20); //50 kHz
    ConfigCpuTimer(&CpuTimer1, 150, 84);
#endif


#if (CPU_FRQ_100MHZ)
// Configure CPU-Timer 0, 1, and 2 to interrupt every second:
// 100MHz CPU Freq, 1 second Period (in uSeconds)


    ConfigCpuTimer(&CpuTimer0, 100, 20);
    ConfigCpuTimer(&CpuTimer1, 100, 84);
#endif


// To ensure precise timing, use write-only instructions to write to the entire register. Therefore, if any
// of the configuration bits are changed in ConfigCpuTimer and InitCpuTimers (in DSP2833x_CpuTimers.h), the
// below settings must also be updated.

    CpuTimer0Regs.TCR.all = 0x4001; // Use write-only instruction to set TSS bit = 0
    CpuTimer1Regs.TCR.all = 0x4001; // Use write-only instruction to set TSS bit = 0
*/
    EALLOW;
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
    EDIS;

    InitEPwm1Example();
    InitEPwm2Example();
    InitEPwm3Example();
    InitEPwm4Example();

    EALLOW;
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    EDIS;

// Step 5. User specific code, enable interrupts
// Enable ADCINT in PIE
    //PieCtrlRegs.PIEIER1.bit.INTx6 = 1; //CPU TIM0
    //PieCtrlRegs.PIEIER1.bit.INTx7 = 1; //CPU TIM1
    //IER |= M_INT1; // CPU TIM0
    //IER |= M_INT13; //CPU TIM1
    IER |= M_INT3; //ePWM1
    PieCtrlRegs.PIEIER3.bit.INTx1 = 1; //ePWM1

// Enable global Interrupts and higher priority real-time debug events:
    EINT;   // Enable Global interrupt INTM
    ERTM;   // Enable Global realtime interrupt DBGM

    LR_PHASE_SHIFT = 1U*(1.0*LR_THETA*FB_PERIOD/180);
    FB_HALF_PERIOD = FB_PERIOD/2;
    toggler = 1;

    // Configure ADC
    AdcRegs.ADCMAXCONV.all = 0x0001;        // Setup 2 conv's on SEQ1
    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x3; // Setup ADCINA3 as 1st SEQ1 conv.
```

```
        AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x2; // Setup ADCINA2 as 2nd SEQ1 conv.


// Step 6. IDLE loop. Just sit and loop forever (optional):
    for(;;)
    {
        asm("          NOP");
    }


}




void InitEPwm1Example()
{

    EPwm1Regs.TBPRD = FB_PERIOD;                       // Set timer period
    EPwm1Regs.TBPHS.half.TBPHS = 0x0000;       // Phase is 0
    EPwm1Regs.TBCTR = 0x0000;                  // Clear counter

    // Setup TBCLK
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
    EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading
    EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
    EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;

    EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;

    EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load registers every ZERO
    EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
    EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
    EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;

    // Setup compare
    EPwm1Regs.CMPA.half.CMPA = FB_HALF_PERIOD;

    // Set actions
    EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;             // Set PWM1A on Zero
    EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;


    EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;           // Set PWM1A on Zero
    EPwm1Regs.AQCTLB.bit.CAD = AQ_SET;

    // Active Low PWMs - Setup Deadband
    EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
    EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
    EPwm1Regs.DBRED = DEADBAND_LENGTH_LAG; //rising edge (deadtime = XX/150 MHz)
    EPwm1Regs.DBFED = DEADBAND_LENGTH_LAG; //falling edge (deadtime = XX/150 MHz)

    //Set up interrupt
    EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;
    EPwm1Regs.ETSEL.bit.INTEN = 1;
    EPwm1Regs.ETPS.bit.INTPRD = ET_3RD;
}



void InitEPwm2Example()
{

    EPwm2Regs.TBPRD = FB_PERIOD;                       // Set timer period
    EPwm2Regs.TBPHS.half.TBPHS = LR_PHASE_SHIFT;         // Phase is 0
```

```
    EPwm2Regs.TBCTR = 0x0000;                      // Clear counter


    // Setup TBCLK
    EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
    //EPwm2Regs.TBCTL.bit.PHSEN = TB_DISABLE;          // Disable phase loading
    EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;         // enable phase loading

    EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
    EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Slow just to observe on the scope
    EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //sync flow-through


    // Setup compare
    EPwm2Regs.CMPA.half.CMPA = FB_HALF_PERIOD;


    // Set actions (switched)
    EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;             // Set PWM2A on Zero
    EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;


    EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;           // Set PWM2A on Zero
    EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;

    // Active Low complementary PWMs - setup the deadband
    EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
    EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;

    //Set deadband
    EPwm2Regs.DBRED = DEADBAND_LENGTH_LEAD; //rising edge (deadtime = XX/150 MHz)
    EPwm2Regs.DBFED = DEADBAND_LENGTH_LEAD; //falling edge (deadtime = XX/150 MHz)

    // Interrupt where we will modify the deadband
    //EPwm2Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;      // Select INT on Zero event
    //EPwm2Regs.ETSEL.bit.INTEN = 1;                 // Enable INT
    //EPwm2Regs.ETPS.bit.INTPRD = ET_3RD;            // Generate INT on 3rd event

}


void InitEPwm3Example()
{

    EPwm3Regs.TBPRD = FB_PERIOD;                             // Set timer period 75 MHz/XX
    //EPwm3Regs.TBPHS.half.TBPHS = phase/180*EPwm3Regs.TBPRD;           // Offset = XX/(150 MHz); Phase = 180*XX/TBPRD
    EPwm3Regs.TBPHS.half.TBPHS = FB_OFFSET;
    EPwm3Regs.TBCTL.bit.PHSDIR = 0; // 0 = positive phase (lags); 1 = negative phase (leads)
    EPwm3Regs.TBCTR = 0x0000;                      // Clear counter


    // Setup TBCLK
    EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
    //EPwm3Regs.TBCTL.bit.PHSEN = TB_DISABLE;          // Disable phase loading
    EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE;         // Enable phase loading ADDED
    EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
    EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Slow so we can observe on the scope

    EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //sync flow-through


    // Setup compare
    EPwm3Regs.CMPA.half.CMPA = FB_HALF_PERIOD;

    // Set actions
```

```
    EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;              // Set PWM3A on Zero
    EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;


    EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;            // Set PWM3A on Zero
    EPwm3Regs.AQCTLB.bit.CAD = AQ_SET;


    // Active high complementary PWMs - Setup the deadband
    EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
    EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;


    //Set deadband
    EPwm3Regs.DBRED = DEADBAND_LENGTH_LAG; //rising edge (deadtime = XX/150 MHz)
    EPwm3Regs.DBFED = DEADBAND_LENGTH_LAG; //falling edge (deadtime = XX/150 MHz)


}


void InitEPwm4Example()
{

    EPwm4Regs.TBPRD = FB_PERIOD;                          // Set timer period 75 MHz/XX
    //EPwm4Regs.TBPHS.half.TBPHS = phase/180*EPwm3Regs.TBPRD;          // Offset = XX/(150 MHz); Phase = 180*XX/TBPRD
    EPwm4Regs.TBPHS.half.TBPHS = FB_OFFSET+LR_PHASE_SHIFT;
    EPwm4Regs.TBCTL.bit.PHSDIR = 0; // 0 = positive phase; 1 = negative phase
    EPwm4Regs.TBCTR = 0x0000;                    // Clear counter


    // Setup TBCLK
    EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; // Count up
    //EPwm4Regs.TBCTL.bit.PHSEN = TB_DISABLE;         // Disable phase loading
    EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE;        // Enable phase loading ADDED
    EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // Clock ratio to SYSCLKOUT
    EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;          // Slow so we can observe on the scope

    EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //sync flow-through


    // Setup compare
    EPwm4Regs.CMPA.half.CMPA = FB_HALF_PERIOD;


    // Set actions (switched A and B)
    EPwm4Regs.AQCTLB.bit.CAU = AQ_SET;              // Set PWM3A on Zero
    EPwm4Regs.AQCTLB.bit.CAD = AQ_CLEAR;


    EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;            // Set PWM3A on Zero
    EPwm4Regs.AQCTLA.bit.CAD = AQ_SET;


    // Active high complementary PWMs - Setup the deadband
    EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
    EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;


    //Set deadband
    EPwm4Regs.DBRED = DEADBAND_LENGTH_LEAD; //rising edge (deadtime = XX/150 MHz)
    EPwm4Regs.DBFED = DEADBAND_LENGTH_LEAD; //falling edge (deadtime = XX/150 MHz)


}


interrupt void epwm1_timer_isr(void)
{
```

```
if(FULL_CLAMPED_MODE)
{
if(EPwm1TimerIntCount % 4 == 0)
{
if(toggler == 1)
{
// EPwm1Regs.AQCSFRC.bit.CSFA = AQ_NO_ACTION;
// EPwm1Regs.AQCSFRC.bit.CSFB = AQ_NO_ACTION;
// EPwm2Regs.AQCSFRC.bit.CSFA = AQ_NO_ACTION;
// EPwm2Regs.AQCSFRC.bit.CSFB = AQ_NO_ACTION;
// EPwm4Regs.AQCSFRC.bit.CSFA = AQ_CLEAR;
// EPwm3Regs.AQCSFRC.bit.CSFA = AQ_CLEAR;
// DELAY_US(.034);
// EPwm4Regs.AQCSFRC.bit.CSFB = AQ_SET;
// EPwm3Regs.AQCSFRC.bit.CSFB = AQ_SET;

//clamb b
EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;            // Set PWM3A on Zero
    EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;               // Set PWM3A on Zero
   EPwm4Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;            // Set PWM3A on Zero
EPwm3Regs.AQCTLB.bit.CAD = AQ_SET;
EPwm4Regs.AQCTLB.bit.CAU = AQ_SET;            // Set PWM3A on Zero
    EPwm4Regs.AQCTLB.bit.CAD = AQ_SET;

//switch a
EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;             // Set PWM3A on Zero
EPwm1Regs.AQCTLB.bit.CAD = AQ_SET;
EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;            // Set PWM3A on Zero
    EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;             // Set PWM2A on Zero
EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;            // Set PWM2A on Zero
EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;

}
else
{
// EPwm3Regs.AQCSFRC.bit.CSFB = AQ_NO_ACTION;
// EPwm3Regs.AQCSFRC.bit.CSFA = AQ_NO_ACTION;
// EPwm4Regs.AQCSFRC.bit.CSFB = AQ_NO_ACTION;
// EPwm4Regs.AQCSFRC.bit.CSFA = AQ_NO_ACTION;
// EPwm2Regs.AQCSFRC.bit.CSFB = AQ_CLEAR;
// EPwm1Regs.AQCSFRC.bit.CSFB = AQ_CLEAR;
// DELAY_US(.034);
// EPwm2Regs.AQCSFRC.bit.CSFA = AQ_SET;
// EPwm1Regs.AQCSFRC.bit.CSFA = AQ_SET;

//switch B
EPwm4Regs.AQCTLB.bit.CAU = AQ_SET;            // Set PWM3A on Zero
EPwm4Regs.AQCTLB.bit.CAD = AQ_CLEAR;
EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;            // Set PWM3A on Zero
    EPwm4Regs.AQCTLA.bit.CAD = AQ_SET;
EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;            // Set PWM3A on Zero
   EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;            // Set PWM3A on Zero
    EPwm3Regs.AQCTLB.bit.CAD = AQ_SET;

//clamp a
EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;               // Set PWM3A on Zero
```

```
    EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
    EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;                // Set PWM3A on Zero
        EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
    EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;               // Set PWM3A on Zero
        EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;
    EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;                // Set PWM3A on Zero
       EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;


}
toggler = !toggler;
}
}
else
{
    AdcRegs.ADCTRL2.bit.SOC_SEQ1 = 1; //Start ADC reading
    DELAY_US(.18);

    Voltage1 = AdcRegs.ADCRESULT0 >>4; //Vmid
    Voltage2 = AdcRegs.ADCRESULT1 >>4; //Vin

    if(Voltage1*2>Voltage2+12) //ADC offset = ~12
    {
    //lower Vmid
        EPwm3Regs.TBCTL.bit.PHSDIR = 0;
        EPwm3Regs.TBPHS.half.TBPHS = 15;//15
        EPwm4Regs.TBCTL.bit.PHSDIR = 0;
        EPwm4Regs.TBPHS.half.TBPHS = 15+LR_PHASE_SHIFT;//15
    }
    else
    {
    //raise Vmid
        EPwm3Regs.TBCTL.bit.PHSDIR = 1;
        EPwm3Regs.TBPHS.half.TBPHS = 25;
        if(LR_PHASE_SHIFT > 25) {
            EPwm4Regs.TBCTL.bit.PHSDIR = 0;
            EPwm4Regs.TBPHS.half.TBPHS = LR_PHASE_SHIFT-25;
        }
        else {
          EPwm4Regs.TBCTL.bit.PHSDIR = 1;
            EPwm4Regs.TBPHS.half.TBPHS = 25-LR_PHASE_SHIFT;
        }
    }
        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset SEQ1
}
EPwm1TimerIntCount++;

// Clear INT flag for this timer
    EPwm1Regs.ETCLR.bit.INT = 1;

    // Acknowledge this interrupt to receive more interrupts from group 3
PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}
```

Appendix C

Printed Circuit Board Design

C.1   Schematics

Figures C-1, C-2, and C-3 show a complete schematic of the final prototype PCB.

C.2   Layout

Figures C-4, C-5, C-6, and C-7 show the four copper layers of the final prototype PCB.

C.3   Bill of Materials

Table C.1 is a bill of materials showing all the components used on the final prototype PCB.
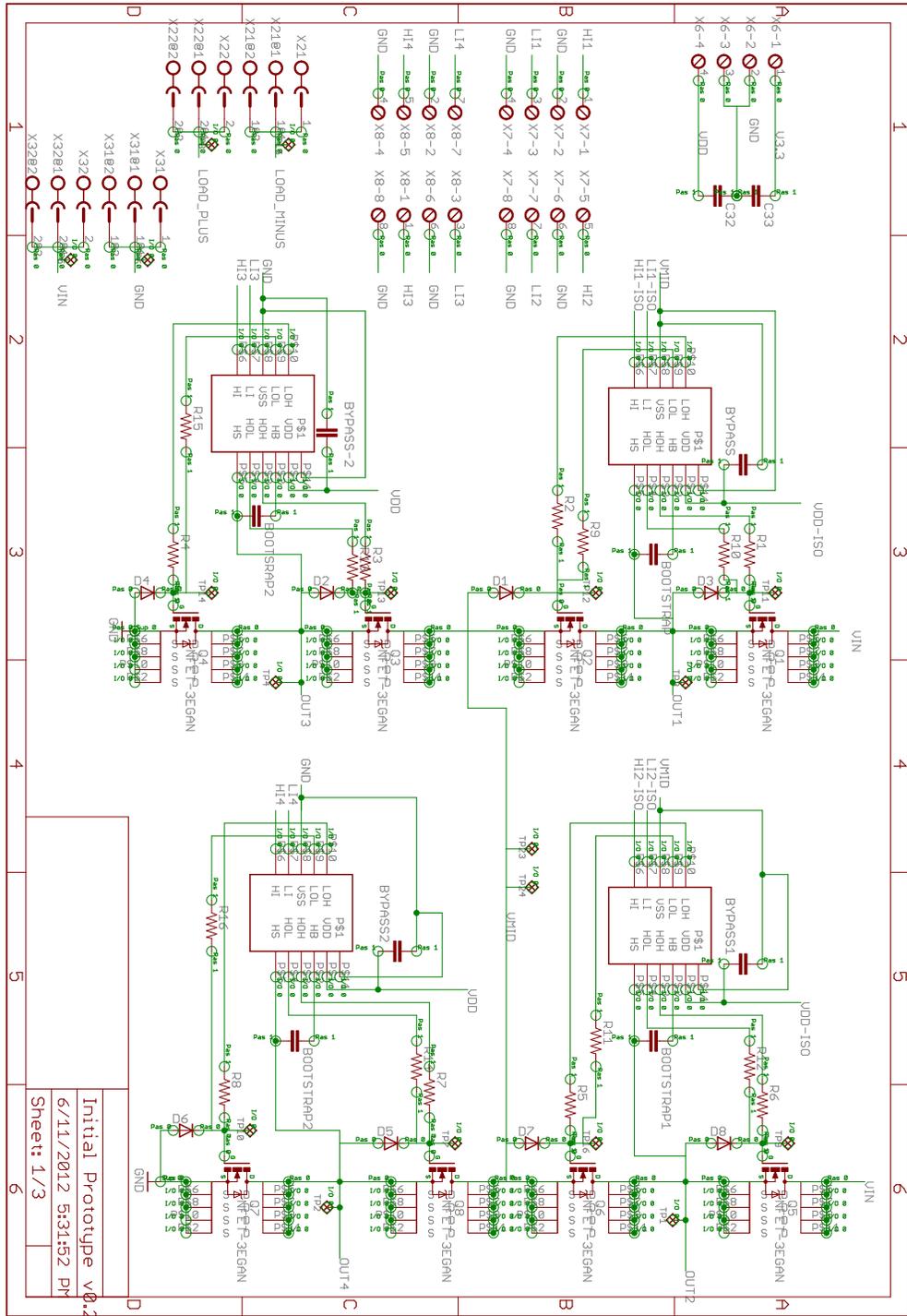
Figure C-1: Schematic 1
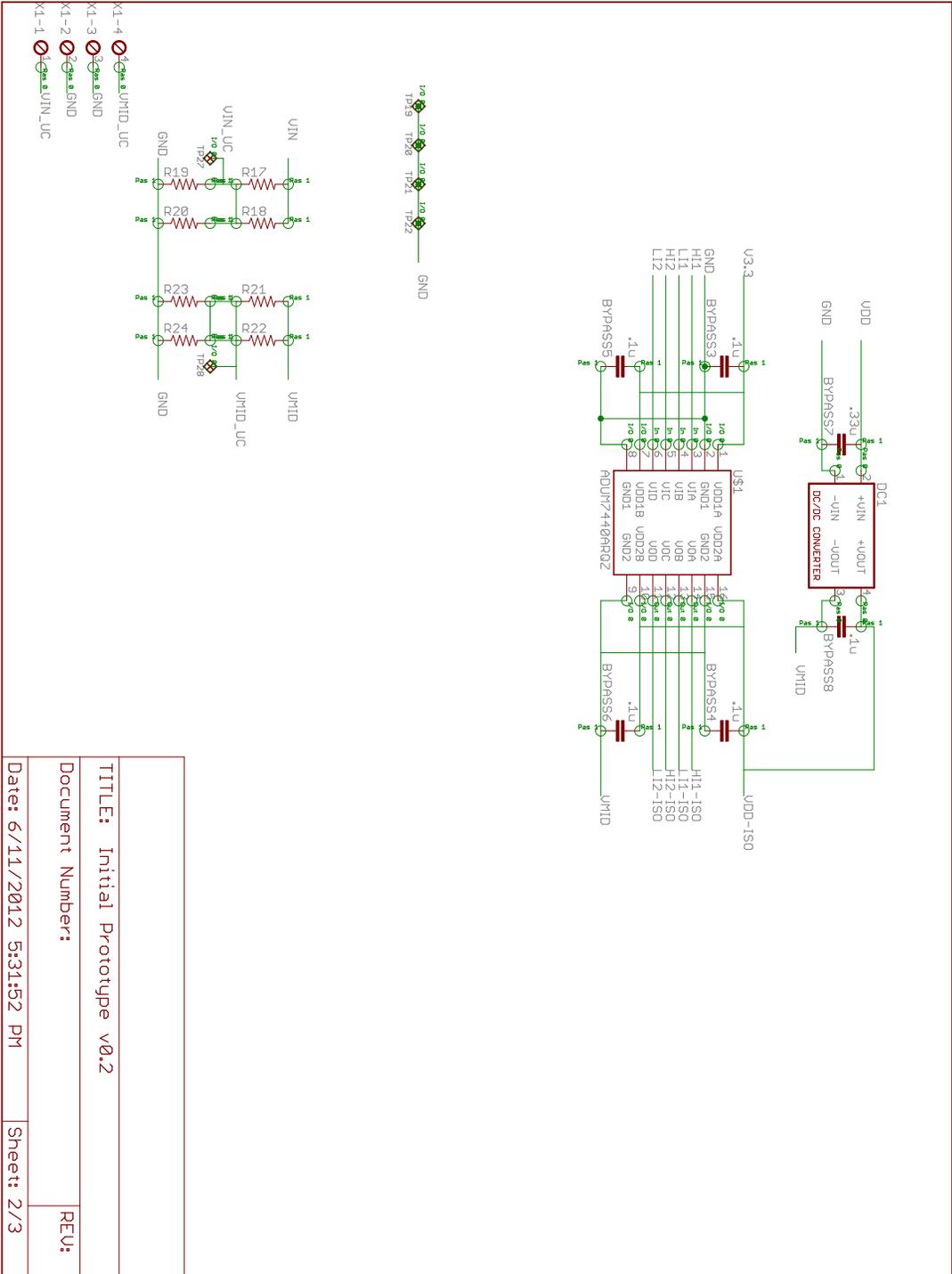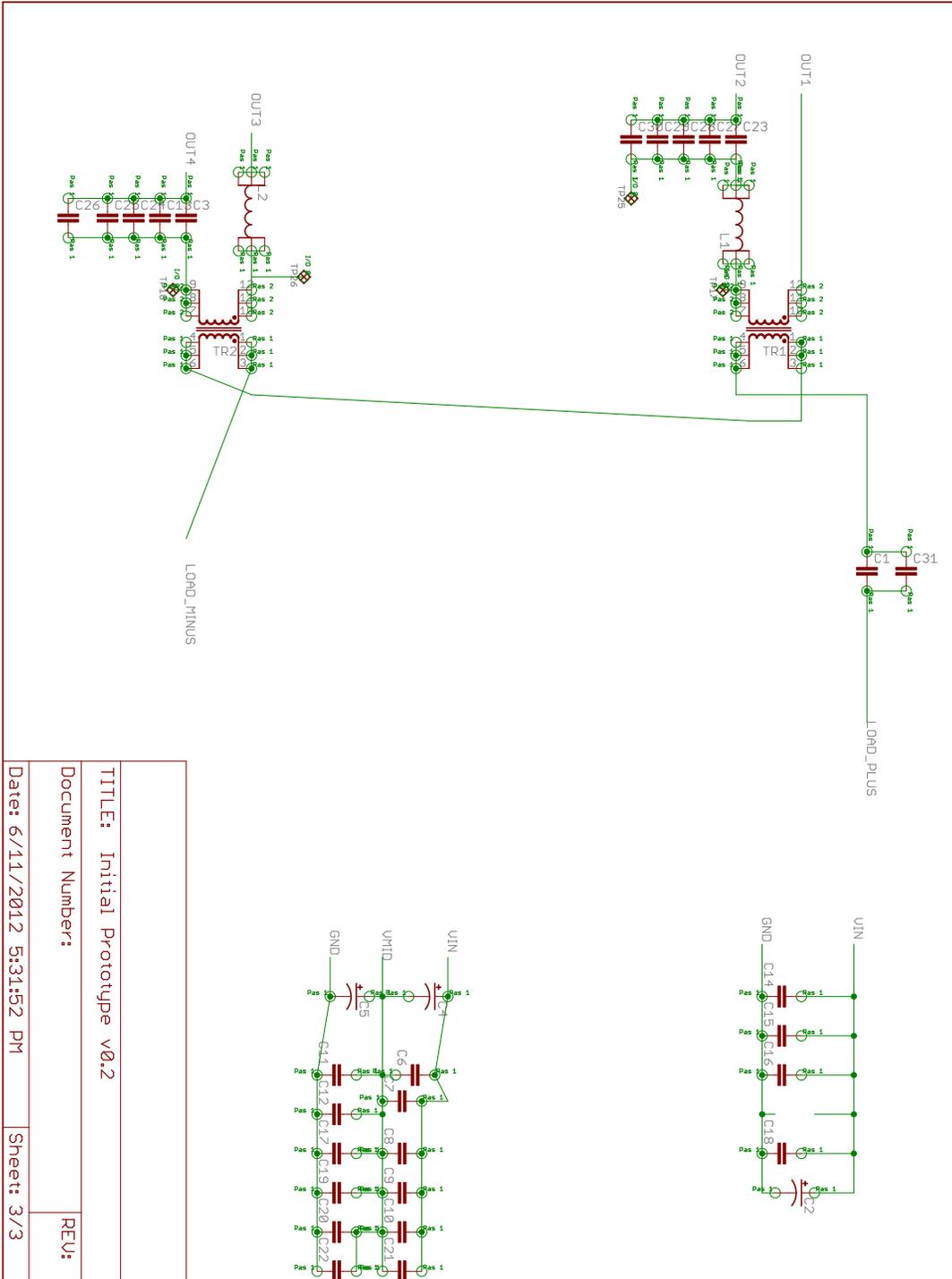
Figure C-2: Schematic 2

Figure C-3: Schematic 3
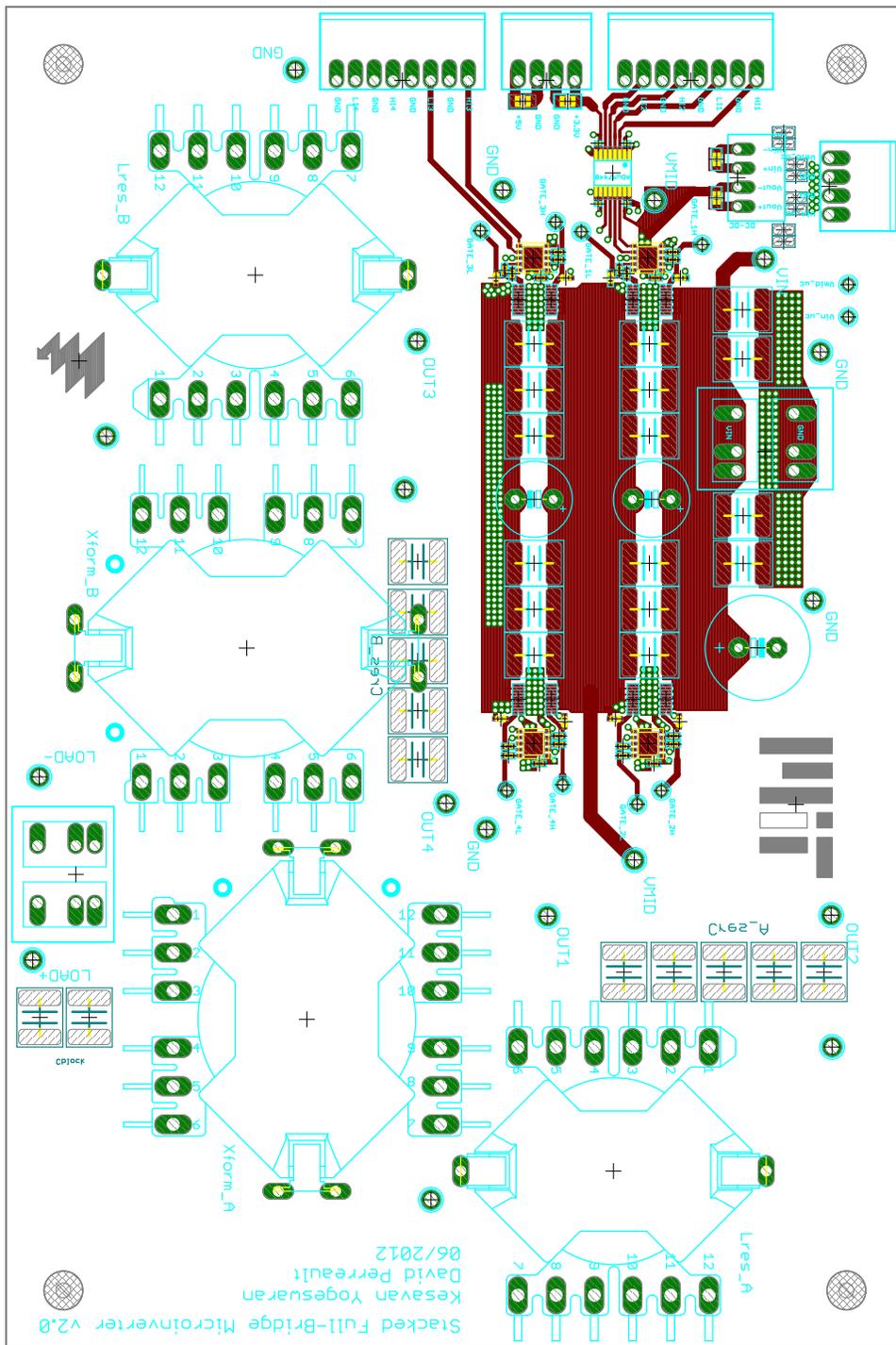
Figure C-4: Top Copper Layer

Figure C-5: Upper Middle Copper Layer
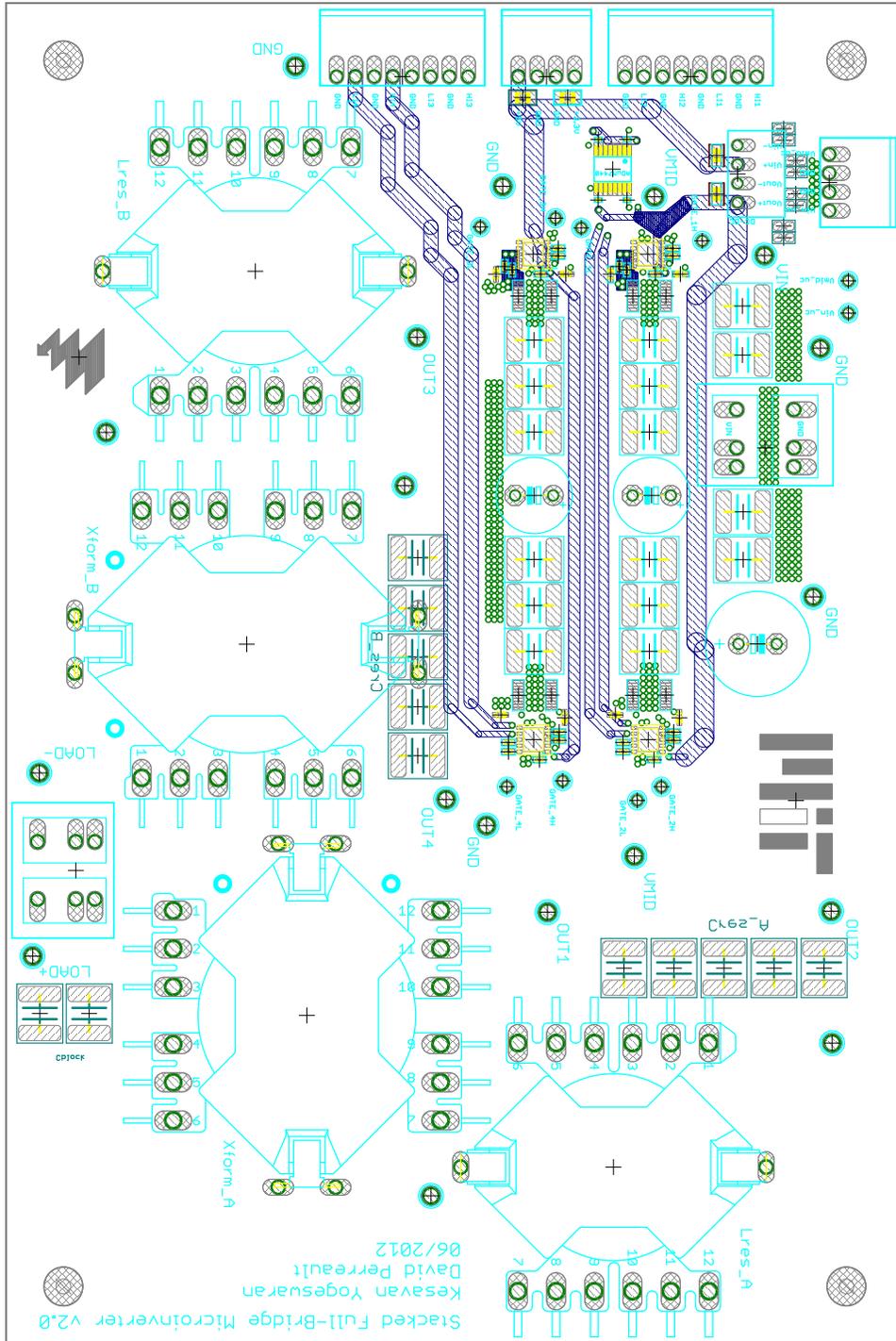
Figure C-6: Lower Middle Copper Layer
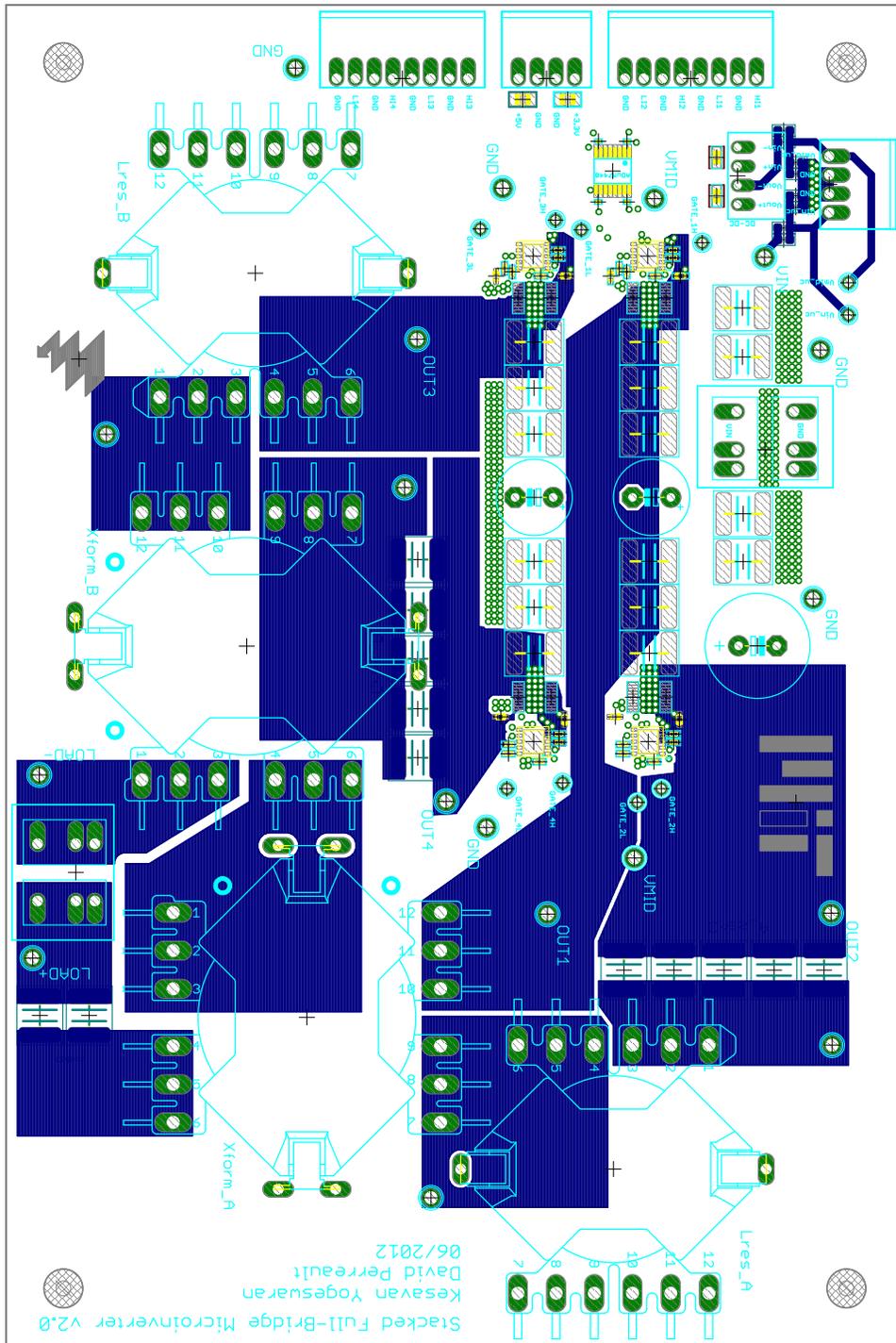
Figure C-7: Bottom Copper Layer

Part	Description	Quantity
Efficient Power Conversion EPC2015	40V GaN FETs in inverter	8
Texas Instruments LM5113	Half-bridge gate driver for GaN FETs	4
TDK C5750Y5V1H226Z	50V 22μF ceramic capacitors for buffering V_{IN} and V_{MID} and for C_{block}	68
Rubycon 63TXW680MEFC10X50	63V 680μF aluminum capacitors for buffering V_{IN} and V_{MID}	3
Recom RI-0505S	isolated 5V-5V DC-DC converter	1
Analog Devices ADUM7440ARQZ	quad digital logic isolator for gate drive signals to full-bridge A	1
TDK C0603Y5V1C103Z	logic isolator decoupling cap	4
Yageo RC0402JR-0710RL	10Ω gate resistor	16
TDK C1005X5R1C105K	16V 1μF capacitors for gate driver bypass and bootstrap	8
Kemet C2220C563J1GACTU	100V .056μF ceramic capacitors for C_{res}	4
Kemet C2220C683J1GACTU	100V .068μF ceramic capacitors for C_{res}	6
Murata GRM219R61A105KA01D	1μF buffer capacitors for 5V and 3.3V buses	2
Taiyo Yuden EMK107B7105KA-T	decoupling capacitor for outputs to microcontroller	2
TDK C1608X5R1H334K	330nF decoupling capacitor for DC-DC input	1
AVX 0603YC104KAT2A	100nF decoupling capacitor for DC-DC output	1
Yageo RC0603FR-075K49L	5.49kΩ resistors to scale down V_{IN} and V_{MID} to be read by microcontroller	2
Stackpole Electronics RMCF0603FT95K3	95.3kΩ resistors to scale down V_{IN} and V_{MID} to be read by microcontroller	2
Barry R1000-150-10X	100Ω 150W load resistor	6
Riedon PF2472-200RF1	200Ω 100W load resistor	2
Stackpole Electronics TR50JBC15R0	15Ω 50W load resistor	1

Table C.1: Bill of Materials

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