A Cost Effective ATE Calibration/Verification Solution

by

Edgar N. Chung

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degrees of
Bachelor of Science in Electrical Engineering and Computer
and Master of Engineering in Electrical Engineering and Computer Science
at the Massachusetts Institute of Technology

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ABSTRACT

This thesis describes the SD-34 system verification ASIC that will provide a cost efficient solution in calibrating/verifying ATE systems when testing high-speed memory devices. The heart of the ASIC is a High Resolution Skew Detector (HRSD) which converts in-phase as well as out-of-phase skew into a usable signal for use off-chip using a novel time-to-voltage conversion (TVC) technique. Multiple target signals are compared to a reference signal one at a time with the use of an analog multiplexer. The HRSD suffers from relatively little metastable jitter problems as compared to many other conventional phase/skew detection circuits. Overall theoretical performance is estimated to have subpicosecond resolution and a few picoseconds linearity. The ASIC will be used in an array configured on the test head such that parallelism can be added to the system verification process. This will reduce costs due to production time and may offer a superior solution for AC calibration due to its Device Under Test (DUT) level testing capability. The process used to fabricate this ASIC is Austria Mikrosysteme’s 0.8μm BiCMOS process technology.

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Chapter 1: Motivation

As memory devices rapidly approach higher speeds, the Automatic Test Equipment (ATE) systems used to test them need to improve at the same rate, if not higher. Test timing control with tens of picoseconds of accuracy at around 500 MHz was a critical milestone in the ATE industry [1]. In order to maintain this timing performance with future LSI technology, a new but cost effective milestone must be met. With the introduction of the Rambus technology, which can achieve speeds of 800 MHz, a relatively cheap calibration system will be needed in order to make these devices cost effective. Logic devices that achieve this range of performance have a luxury that memory devices cannot afford to have. Memory devices are distributed in much larger volumes, thus testing overhead for these devices more directly affects the final consumer price. Testing these state-of-the-art memory devices with expensive test equipment increases the cost of each device substantially, possibly putting these devices out of the reach of the average consumer. These tests may also be physically unachievable with current timing technology.

Another problem that plagues the ATE industry is that of system verification times. Modern ATE systems can test up to 64 devices in parallel with the ability to test 128 devices in current development. With each device having 48 pins to test, ATE systems can range anywhere between 3000 to 6000 test channels. The calibration process that reduces time-domain skews between channels is only moderately effective, therefore a different mechanism called system verification is needed in order to further fine tune the channels. Current verification processes utilize a programmable digital oscilloscope to sample waveforms from each channel through an interface board. The problem with this method is that data acquisition times for each channel can run anywhere between 5-10 seconds per channel. Add to that the time to move a robotic probe to each channel (~2 seconds) and we are looking at a total verification time of about 14 hours (average). Adding more data acquisition oscilloscope in parallel in order to reduce the verification period only increases test costs by tying up these expensive units. There are even problems of drifts in accuracy of the oscilloscope that occur over the long 14 hour time period due to temperature gradients. It is a glut of information that is unavoidable in this industry, and as the density of channels continues to increase, system verification times will only increase in cadence.

The premise of this thesis is the design and fabrication of a custom ASIC that will perform skew detections on a number of ATE test channels in parallel and provide a skew signal usable in the ATE functional block. The skew signal will be a logic level corresponding to the
polarity of the skew. This way, rather than having an expensive mechanically controlled oscilloscope step through every channel through an interface board, the ASIC can be used in place of each memory device, bypassing the interface board altogether. Each device site will be electrically connected to an ASIC by means of a ceramic substrate, allowing for multiple channels to be probed at once through the test head interface. This way, we can reduce the cost of test through parallelism, as well as decrease the time to test by eliminating the slow, serial probing process of today’s verification system. Using a fairly conservative estimate, the ASIC could reduce verification periods down to 10-20 minutes depending on the number of channels per ASIC that are available. An added benefit this ASIC provides is the ability to test at the DUT level, which puts the probe station as well as the transmission lines that connect it with the ATE system into the verification path. This is something the ATE industry has never been able to do due to physical limitations of the interface board.

The ASIC’s main function will be that of a high accuracy skew detection (HRSD) with a resolution of around a picosecond. With this kind of accuracy, in addition to the parallelism of its design, as well as the ability to test at the DUT level, this device should provide a superior, but cost-effective calibration solution for future ATE systems. The goals of this thesis project are to successfully design as well as fabricate a prototype ASIC that will provide this cost-effective solution.

The following ASIC’s HRSD circuit is largely based and extended upon part of Tai-ichi Otsuji’s Si-Bipolar Time Interval Counter LSI [2]. This circuit has been modified in order to give the added ability of measuring out-of-phase skew as well as in-phase skew. Also, much of the clock strobe circuitry as well as timing optimizations are independent of the original design. Teradyne patents have been filed for both the ASIC itself as well as the new method for verifying ATE systems using the proposed ASIC.
Chapter 2: Background

2.1 ATE Calibration and Verification

The basic architecture of a shared-resource ATE system is depicted in Figure 1.

![Shared-Resource ATE Architecture Diagram](image)

Figure 1: Shared-Resource ATE Architecture

In this type of tester, a limited number of signal resources (timing generators, pattern memory, etc.) are shared among multiple test channels through the use of a programmable switching matrix. A shared-resource architecture is ideal for testing memory devices due to the redundant nature of these tests. In this type of architecture, the Test Pattern, Format and Timing Memories provide the resources to store and send timing signals and patterns to the Formatting Electronics. The Formatting Electronics takes signals from the test memories and provides timing signals to the pin electronics. Note that all timing signals are derived from a precise crystal oscillator which allows for all timing comparisons between channels to be referenced to a single point. Each test channel of the Pin Electronics is made up of a high-speed strobed comparator and driver pair, which is used to analyze the timing of the DUT by comparing test patterns from the ATE Memory. The Timing Generator provides the strobe for all comparators, providing a method to accurately measure round trip propagation delays.

In order to compare test patterns successfully, signals that are applied to device pins along each channel must arrive at precise timing relative to each other. Transmission line

---

1 Single point referencing is common in all metric measurements and is needed to validate the empirical data.
variations, device mismatching, gaussian-modeled noise and other such anomalies will contribute small but important delays in the propagation time for each signal. Consequently, in order to control the signal timing accurately, the relative delays from channel to channel must be quantified and compensated for prior to the test. This measurement and compensation process is called ATE calibration and it must be completed before any pattern comparisons can be made between the DUT and the ATE Functional Block. While the actual details of the ATE calibration process are out of the scope of this paper, the process involves a tremendous amount of data manipulation and comparison among all channels involved in a DUT test.

The calibration mechanism is actually an integrated part of the test channel circuitry used in conjunction with the Calibration Electronics block. Through the use of switching relays, propagation times through various branches of the network can be measured and referenced to other branches. The process calibrates each test channel all the way to the DUT with lumped time-delay reasoning. Although this type of reasoning simplifies calculations, time-domain drifts in each component of the long calibration path add cumulative uncertainty into the calibration process. For this reason, ATE calibration has low to moderate accuracy with post-calibration channels having about 100-200ps time domain skews between them. Therefore, a second process called system verification must be completed after the calibration process in order to ensure a higher level of accuracy between channels. It is important to note that the system verification process must use a mechanism distinct and separate from the calibration mechanism in order to avoid cyclical reasoning. ATE system verification differs from calibration in that this process is external, providing measured empirical data to the ATE customer on an already internally calibrated system. The gathered data represents the relative skew amongst all the channels of the test system with a much higher degree of accuracy than conventional calibration. Using the gathered data, the ATE customer can perform device tests with greater precision after the delay variations among channels can be “dialed” out.

Referring back to Figure 1, the area of improvement that this ASIC will provide for is in the PIN Electronics/DUT interface. The ATE industry as a whole has had a great deal of problems in eliminating intrusive verification interfaces between the DUT and the PIN Electronics, even going so far as eliminating the Probe Station altogether as in modern schemes. This ASIC will provide a method that will eliminate intrusive interfaces, as well as provide a

---

2 Teradyne Inc. uses a calibration method which reasons out the timing errors of individual components of a signal path by lumping the error together for all components. This approach only works within a specified margin of error.
means to verify a system in a parallel fashion. A review of current verification schemes will provide a better understanding for what advantages this new method will provide.
2.2 Modern Verification Scheme

Modern verification schemes consist of a Device-Interface-Board (DIB) that connects the pin electronics of the ATE system to a mechanically controlled digital oscilloscope.

The robotic probe moves to each DIB jack where a reference edge common to all channels is sent to each output of the pin electronics module. Slight timing variations in each of the channels induces small discrepancies over all the outputs. The oscilloscope digitally acquires waveforms one-by-one for each channel output and by comparing each edge, skew distributions across all channels can be calculated.

The problem with this method is threefold. First, since this verification process is completely serial, the time it takes to acquire data and move the probe to each DIB jack in a system with thousands of channels is on the order of 14 hours. The mechanical setup needed to move the sampling oscilloscope to each channel is also very expensive as well as difficult to maintain. Secondly, drifts in accuracy can occur over the long data acquisition period. Teradyne Inc. has quantified this drift to be up to approximately 100ps over the period of the verification.
process due to temperature gradients in the DIB. Finally, this method ignores the probe station entirely due to the physical limitations of the DIB setup. This method verifies the system only up to the output of the pin electronics, ignoring the transmission lines, the probe card, and the probe pins that interface to the DUT itself. These are all items that induce more timing uncertainty into the path of test, and should be included in the verification path. By ignoring these components, the ATE customer has no guarantee on the accuracy of the test data taken from the output of the Pin Electronics to the DUT pins. This is a problem that has been very persistent in this industry and as channel densities in future ATE systems continues to increase, the plausibility of waveform acquisition though an interface board becomes much smaller. An alternative to waveform acquisition must be found in order for both system throughput and verification accuracy to increase in the near future. An analysis of the actual probe station interface will offer some insight into the possibilities obtainable by the proposed ASIC.

3 Empirical data taken from Teradyne Inc. Marlin memory test system.
2.3 Progression of ATE Probe Station

Typical ATE probe cards used for DUT level testing have had problems with large parasitic capacitances that have limited the accuracy of the timing measurements. The conventional probe cards consist of an array of pliable copper probes that are aligned to the pattern of the DUT contact pads. With over 64 devices to test with 48 pins each, the number of probes needed in a probe card is tremendous. Each metal probe is soldered to a carrier substrate, typically a circular printed circuit board (PCB) which interfaces to the probe station, and is coupled to the ATE pin electronics through transmission lines. The probe tips are usually held at low angles in order to provide enough horizontal play to remove the thin oxide film found on the DUT pads.

![Figure 3: Conventional Probe Card (cross-section)](image)

The main problem with this probe card was that of parasitics. Lead inductances of the probe tips could reach as large as 10nH while the interconnect capacitance could reach almost 20pF. This would lead to an unavoidable low-pass filter which would degrade the transient characteristics of the waveforms under test. In addition to this, the resonance of the low-pass filter could induce ringing (oscillations) in the I/O of the DUT signals. Add to this the problem of ground bounce, caused by differences in chip ground and tester ground, and it was easy to see that the probe card was a bottleneck in terms of the performance of ATE systems.

![Figure 4: Electrical Equivalent of Probe Card](image)
If the electrical characteristics of the probe card did not seem daunting enough, many mechanical problems were also inherent within this implementation. After a number of touchdowns, the probes would need to be realigned (manual labor) due to the physical stress placed on the probe tips. Considering that ATE testers are under use almost 24 hours a day, as well as the fact that there are thousands of probe needles in a probe card, the added cost of mechanical realignment was unavoidably expensive. With each of these problems, any verification process at the DUT level was impossible due to the poor frequency response and the mechanical problems associated with the probe station. This was the motivation for the use of the Device-Interface-Board, which provided a more realistic solution for system verification.

Modern ATE probe cards are vastly improved upon, with parasitics that are orders of magnitude lower than the more conventional ones. These probe cards are based on a perpendicular tungsten probe needle design that are short enough to provide only a 1 cm distance between the ATE system and the DUT. These probe tips are held together in a polyimide membrane making the realignment process much simpler. The short probe needles reduce the parasitics of the probe card considerably as well as provide a probe station that is easier to maintain due to a more robust mechanical design.

![Modern Probe Card (cross-section)](image)

Figure 5: Modern Probe Card (cross-section)

The low parasitics associated with these modern probe cards allows for direct measurements to be made at the DUT level and is the driving force behind the design of this ASIC. With the advent of the high performance probe cards, relatively high timing measurements are possible not only at the DUT level, but are now possible even at the wafer level. This added benefit will be discussed later.

The proposed ASIC will take the place of the DUT on a ceramic substrate. The probe station will then interface to the ASIC through the probe card, exactly as if a memory device was under a testing procedure. Used in this fashion, the ASIC will provide multiple skew detections among a number of test channels exactly as a memory device would “observe” the channels. This is because we are now including the probe station and the aforementioned transmission lines into the verification path. A large number of these ASICs will be placed on the substrate so that they
can be used in a parallel fashion, allowing for multiple channels to be verified at once. By doing so, we can decrease the time for a system to be verified by more than an order of magnitude. Also, since we are verifying the system all the way out to the DUT, rather than stopping at the Pin Electronics block, we are giving the ATE customers a better representation of a fully calibrated system.

The question that now remains is how accurate the skew detection of this ASIC actually is. If the resolution is too low, then the benefits reaped from the DUT-level verification will be overshadowed by the inaccuracy of the data. Examination of previous skew detection schemes will provide insight into the value of the HRSD used in the ASIC.
2.4 Progression of High Accuracy Skew Detection

There have been numerous approaches taken regarding the problem of high accuracy skew detection in the ATE industry. These approaches fall under two main categories, with the industry swaying back and forth between them over time. The first approach involves logic-oriented calibration which relies on timing-specific ASICs and logic analysis to provide the relevant skew data. The main advantage of using the “black box” approach has been that of speed. Logical expression can be calculated quickly and in most cases, provide an adequate level of resolution to be feasible in the verification and calibration process.

When logic-oriented approaches failed to meet a specified level of accuracy as test systems evolved, the industry embraced a simple brute-force data acquisition as the solution for their calibration processes. Data acquisition involves some sort of reference waveform acquisition procedure and then a data processing step. The advantage of this method is that of accuracy. When the actual voltage waveform can be seen and digitized, accuracy is only a matter of number crunching and data processing. Up until recently, the industry has been leaning towards data acquisition due to the fundamental limitations of logic analysis. But because channel densities are steadily increasing, this brute force method has become much less appealing due to the long verification times needed. Consequently, the industry is now swaying towards the direction of logic-oriented calibration once again.

Logic-oriented solutions ranging anywhere from complicated phase-locked loops to simple D flip-flop counters have been used with varying degrees of success. Each approach has its own inherent strengths and weaknesses, but as it turns out, the showstopper among all implementations is that of resolution. Understanding the problems behind these implementations offers more insight into the value of this particular ASIC. Let us briefly examine a few conventional implementations.

The first, and most standard method used for detecting skew is through the use of an array of D-flip-flop-based latching comparators using the Vernier calibration technique [3, 4]. A sampling oscillator of known frequency is input into the strobe port of all the flip-flops. A calibration oscillator of slightly differing frequency is sent through each pin electronics channel and is input to the data port of each flip-flop. Using this strategy, the reference signal simply latches a high or low value based on the skew of the two signals. This provides a beat signal for each channel and the actual skew between the two signals can be calculated from the skew seen between beat signals (Tmag) by the simple relation:
The advantage of using this technique is that relatively small skews can be "amplified" into much larger skews that are easily detectable through the use of the beat signals. The Vernier technique has been around for a long period of time, therefore many different implementations of this idea have come and gone with many different technologies (CMOS, Bipolar, etc.).

A second and equally common method for implementing a skew detector is using a simple XOR gate used in conjunction with D-flip-flops as used in the Analog devices AD9901 Phase/Frequency Discriminator [5]. This setup produces a signal with a varying pulsewidth based on the skew magnitude as well as skew polarity of the signals. Used in conjunction with a charge pump, this circuit can also provide a DC signal, useful for determining the level of skew.
involved. This circuit also acts as a frequency discriminator at skews larger than its linear range. Figure 7 shows the schematic and a simple timing diagram for this particular circuit.

![Schematic and Timing Diagram](image)

**Figure 7: Phase/Frequency Discriminator (Analog Devices AD9901)**

Ignoring the Frequency discriminator flip-flops, this circuit behaves almost like the vernier implementation except that the outputs of the reference and oscillator flip-flops are sent...
into some sort of XOR device so that a string of pulses can be produced. This string of pulses serves the purpose of creating some sort of DC value through the use of a high-frequency filter. The advantage of this particular implementation is that skew polarity as well as skew magnitude can be determined from the DC Mean Signal.

Similar to the XOR-Filter circuit, another method for implementing a skew detector comes in the form of a SET-RESET Flip-flop used in conjunction with a charge pump, as described in a MEGATEST time calibration instrument [6]. The S-R Flip Flop is configured such that the reference signal sets the Flip Flop while the target signal is input to the Reset port. Figure 8 shows a much simplified schematic.

![Figure 8: Phase/Frequency Discriminator (Analog Devices AD9901)](image)

The complementary outputs of the flip-flop control a current switch, which steers the reference current ($I_r$) to one of two paths. The average current in each path is proportional to the duty cycle of the switch, which relates directly to the time-domain skew between the two inputs. A low-pass-filter is added to one of the two current paths in order to create an output voltage proportional to the average branch current. Another current source ($I_b$) is added at the input of the LPF in order to allow for bipolar swings. The steady state output voltage can then be calculated from the expression:

$$V_{out} = Gain \cdot I_r \left( \frac{Skew}{Frequency(REF)} - \frac{I_b}{I_r} \right)$$

where Gain is the gain of the LPF. This particular implementation has the added benefit that most of the voltage dependent elements such as the current sources, switches, capacitors, etc.
have a relatively constant voltage applied to them. Therefore non-linearity is less of a problem with this circuit. Enough background on older time-interval measurement techniques has now been given in order to move on to a more rigorous analysis of the weaknesses inherent within each method.
2.5 Flip-Flop Based Limitations and Comparisons

Each of the above conventional skew/phase detector implementations suffers from one fundamental limitation due to their common use of edge triggered flip-flops. The underlying problem that plagues the linear range of each of these phase comparator implementations is that of metastability. Each skew detector relies on some sort of flip-flop to produce the valid UP and DOWN signals which are then used in the various charge pumps, filters, etc. Therefore, even if we assume ideal conditions (ideal logic gates, zero parasitic capacitances, etc.), it is the metastability of the flip-flop that limits the resolution of the overall skew detector. As the time difference between the data and the strobe transitions becomes smaller and smaller, metastable jitter will eventually produce invalid outputs. High-speed comparators run into a comparable type of accuracy problem in the form of hysteresis.

From a more analytical standpoint, if we use the Saab and Hajj average branch current analysis method [7], we can estimate the propagation delay through one of the two latches in the flip-flop. This corresponds to the minimum setup time needed to avoid corrupted outputs since the signal needs to propagate fully into the second latch before we can begin the transition of the input signal. This type of analysis will allow us to estimate the maximum level resolution that is possible with Flip-Flop based time-interval measurement techniques.

We can approximate the input edges of an ECL-based Flip-Flop as linear ramp functions with risetimes analogous to slew rate. With this approximation, we can describe an input edge with a number of variables:

\[
\phi \quad \text{Voltage swing}
\]
\[
t_{0} \quad \text{time where signal begins transition}
\]
\[
t_{1} \quad \text{time where signal reaches differential threshold (V_{th} midpoint of transition)}
\]
\[
t_{2} \quad \text{time where signal ends transition}
\]
\[
\tau_{\text{slew}} \quad \text{analogous risetime of input signal} = 2(t_{1} - t_{0})
\]
\[
V_{\text{height}} \quad \text{metastable range of switching threshold V_{th} (comparable to thermal voltage)}
\]

We can describe the output as follows:

\[
t_{0} \quad \text{time where output begins transition}
\]
\[
t_{1} \quad \text{time where output reaches midpoint of transition}
\]
\[
t_{2} \quad \text{time where output ends transition}
\]

and:
\[ \tau_d = \text{propagation delay} = t_{11} - t_{01} \]

**Figure 9: Latch Delay Description**

Assuming we can simplify the Master ECL Latch into a simple differential pair (this reasoning works because the propagation delay through the latch is valid only when the clock is high): Let us define \( \tau_d = \) Minimum time needed between strobe edge and data transition (minimum detectable skew). Using reasoning similar to Yang and Chang's bipolar delay approximation [7, 8] we can model \( \tau_d \) as follows.
The simplified Ebers-Moll model of a differential pair is shown in Figure 10. For a low to high transition, the intrinsic delay can be interpreted as the time for the dynamic base current $i_b(t)$ to inject half of the total stored excess minority charges, $Q_f = \tau_f I_{tree}$, to the base of the left transistor:

$$Q_{base}(t_{io}) = \int_{t_0}^{t_{io}} i_b(t)dt = \frac{\tau_f}{2R_c}$$

Where $Q_{base}$ is the base excess minority charge of the BJT.

It can be shown that $i_b(t)$ can be approximated by a three-segment piecewise linear function since the current switched is an exponential function of the differential input voltage.

1) Segment 1: $t_0 < t \leq t_{io}$: The differential pair does not switch at all, thus $i_b(t)$ is negligible in this interval.

2) Segment 2: $t > t_2$, where $t_2$ is the end of the input voltage transition: Both transistors are in the forward-active region and there is a relatively constant voltage drop across both diodes. For large forward $\beta$, $I_{tree} = I_{c1} + I_{c2}$, and by KCL, $i_{b1} = -i_{b2}$. This means the voltage drop across both base resistances must be the same, therefore:

$$V_1 = V_2 = \frac{\phi - 1.5\phi}{2}, \text{ and } i_b(t) = \frac{\phi}{4rb}$$
3) Segment 3: \( t_{Vh} < t \leq t_{i2} \): \( i_b(t) \) in this section is a linearly increasing function, therefore we can approximate it by the linear interpolation between the other two segments.

\[
\begin{align*}
\text{SEGMENT 1} & : 0, \\
\text{SEGMENT 2} & : \frac{\phi}{4r_b} \cdot \frac{t - t_{Vh}}{t_{i2} - t_{Vh}}, \\
\text{SEGMENT 3} & : \frac{\phi}{4r_b}.
\end{align*}
\]

From the equation (1), \( Q_{base}(t) \) can be found by integrating \( i_b(t) \) over the three segments defined above. Looking at Figure 9, we can show that \( t_{i2} = t_{i0} + \tau_{slew} \) and \( t_{Vh} = t_{i0} + (\tau_{slew}/2) [1 - (V_{height}/\phi)] \). Using these relations, we can analytically calculate the intrinsic delay through the gate:

\[
\tau_d = t_{i1} - t_{i1}
\]

\[
\tau_d = \begin{cases} 
-\tau_{slew} V_{height} \left( \frac{2 \tau_{slew} \tau_{slew} (\phi + V_{height})}{2 \phi} \right)^{1/2} & \text{for } t_{i1} + t_d < t_{i2} \\
2 \tau_{slew} \frac{r_b}{R_c} + \frac{(\phi - V_{height}) \tau_{slew}}{4 \phi} & \text{for } t_{i1} + t_d \geq t_{i2}
\end{cases}
\]

Where:
- \( \tau_f \) = forward transit time
- \( r_b \) = parasitic base resistance
- \( \tau_{slew} \) = input slew time
- \( R_c \) = Collector load resistance
- \( \phi \) = Logic swing

Using Yang and Chang’s gate delay approximation [6, 7] we can deduce the minimum time period needed to avoid metastability based on the intrinsic delay equations calculated above. (\( \tau_d \))

\[
\tau = \sqrt{\frac{2 \tau_{slew} \cdot \tau_{slew} (\phi + V_{height})/(R_c \cdot \phi)}{2 V_{height} / \phi}} \quad (1)
\]

After substituting typical bipolar device parameters,

\( \tau_f = 10.2 \text{ ps}, r_b = 285 \Omega, \phi = 400\text{mV}, V_{height} = 26\text{mV} \):
And using a $\tau_{\text{slew}} = 1.2 \text{ ns}$ and an $R_c = 650 \ \Omega$,

We find that $\tau_s = 13.9 \ \text{ps}$ minimum. Even with as low as $\tau_{\text{slew}} = 200 \ \text{ps}$, we find that $\tau_s = 5.7 \ \text{ps}$. Therefore, achieving resolution on the order of a picosecond is impossible with this configuration. This value will be compared to an analytical analysis of the proposed ASIC later in the thesis. It is clear that in order to achieve a higher degree of resolution, a circuit involving any flip-flop device is not a viable solution. The timing resolution and stability of a wide variety of time-interval measurement methods is summarized in the following table taken from Dan Porat’s, review of sub-nanosecond time-interval measurement paper [13].

<table>
<thead>
<tr>
<th>Method</th>
<th>Resolution</th>
<th>Dynamic Range</th>
<th>Long Term Stability</th>
<th>Integral Linearity</th>
<th>Differential Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Counter (Up, Down signals)</td>
<td>$&gt; 500 \text{ps}$</td>
<td>No Limit in Principle</td>
<td>Very Good</td>
<td>Very Good</td>
<td>Very Good</td>
</tr>
<tr>
<td>2. Counter + Coincidence</td>
<td>$&gt; 200 \text{ps}$</td>
<td>No Limit in Principle</td>
<td>Very Good</td>
<td>Very Good</td>
<td>Good</td>
</tr>
<tr>
<td>3. Vernier with Single Coincidence</td>
<td>$&gt; 20 \text{ps}$</td>
<td>Low</td>
<td>Very Good to Good</td>
<td>Very Good</td>
<td>Good</td>
</tr>
<tr>
<td>4. Vernier with Multiple Coincidence</td>
<td>$&gt; 200 \text{ps}$</td>
<td>Moderate</td>
<td>Very Good</td>
<td>Very Good</td>
<td>Good</td>
</tr>
<tr>
<td>5. Start-Stop</td>
<td>$&gt; 10 \text{ps}$</td>
<td>Low</td>
<td>Poor</td>
<td>Very Good</td>
<td>Good</td>
</tr>
<tr>
<td>6. Microwave</td>
<td>$\sim 1 \text{ps}$</td>
<td>Very Low</td>
<td>Poor</td>
<td>Good</td>
<td>Poor to Good</td>
</tr>
<tr>
<td>7. Proposed ASIC</td>
<td>$&lt; 3 \text{ps}$</td>
<td>No Limit in Principle</td>
<td>Good</td>
<td>Very Good</td>
<td>Very Good</td>
</tr>
</tbody>
</table>

**Table 1: Sub-nanosecond Time-Interval Measurement Comparison**

The Start-Stop method shown above involves measuring the charge of a linear capacitor in an ECL style circuit. This method cannot be feasibly implemented in an ASIC due to the sizing errors as well as the area restrictions associated with on-chip capacitors. The Microwave method involves RF modulating techniques and is only useful in situations where cost is of no consequence due to the need for a linear accelerator.

Since the proposed ASIC only provides a logic level for the ATE system to manage, the linearity of this measurement technique is limited only by the linearity of the ATE system. In most Memory Test Systems, highly linearized comparators and timing generators are used, therefore the linearity of the overall ASIC is very good. It will be shown in the design overview that the proposed ASIC involves an HRSD that suffers relatively little metastability problems, reduces overall system verification time, verifies at the DUT-level, and can achieve theoretical picosecond resolutions. Used in union with an analog multiplexer and possibly an off-chip
charge-pump circuit, this ASIC provides a superior solution for current ATE calibration and verification systems.
Chapter 3: Principle Of Operation

3.1 ASIC-Level

A high-level block diagram of the ASIC is depicted in Figure 11. The ASIC is made up of two 24:1 analog multiplexers addressed by a novel latched decoder, designed to reduce the pin count of the ASIC. Since there are 48 pins on a memory device, we will be able to probe all channels of a particular device site using a single ASIC by splitting the signals among the two multiplexers. The two multiplexers pass two selected input signals to the HRSD where an output logic level is produced corresponding to the polarity of the skew.

![Figure 11: ASIC block diagram](image)

The level-converter (LVC) blocks in the HRSD first converts the input swing (nominal 0-3V) from the two multiplexers into ~450mV ECL swings suitable for high speed processing. The ECL-converted signals are then sent to controllable inverters (INV) so that an out-of-phase skew measurement is possible with this HRSD. Out-of-phase skew measurements try and determine the time-interval separating two signals that are approximately 180-degrees out of phase. These
two signals are then sent to a differential amplifier so that a novel Time-to-Voltage-Conversion
(TVC) technique can be used in conjunction with a high-speed latch in order to provide the
necessary logic output. This new TVC technique is the heart of the ASIC and will be discussed
in much further detail later. The output of the HRSD is buffered and sent off-chip as shown in
Figure 11.

The input paths of the ASIC into the HRSD are made as passive as possible though the
use of the analog multiplexers in order to ensure the highest level of accuracy possible. Any
active elements in the path of measurement will induce error into the skew detection and because
these signals are analog in nature, no input buffers were used for the channel inputs. The input
signal degradation will be based solely on the multiplexer capacitance and the package parasitics,
which will be minimized as much as possible. The multiplexers are composed of a novel array of
T-configured MOS transmission gates as well as its CMOS decoding circuitry while the HRSD is
made up of bipolar ECL gates. For this reason, a BiCMOS fabrication process is needed. To
simplify the design further, as well as reduce the pin count, the ASIC will operate on a universal
0-5V power supply. A summary of the inputs is described in the following table.

<table>
<thead>
<tr>
<th>Signal(s)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select[0-4]</td>
<td>Address signals for the two multiplexers. These signals are buffered with a 0-3V CMOS buffer.</td>
</tr>
<tr>
<td>Select5_Enable</td>
<td>Selects multiplexer A or B. Input buffered (0-3V CMOS)</td>
</tr>
<tr>
<td></td>
<td>LOW = Mux A transparent</td>
</tr>
<tr>
<td></td>
<td>HIGH = Mux B transparent</td>
</tr>
<tr>
<td></td>
<td>(more on this later)</td>
</tr>
<tr>
<td>DUT signals [0-47]</td>
<td>Test channels for the DUT-site being verified. Half of the signals go to multiplexer A, the other half go to multiplexer B.</td>
</tr>
<tr>
<td>BIAS-A</td>
<td>Input bias for signal path A</td>
</tr>
<tr>
<td>BIAS-B</td>
<td>Input bias for signal path B</td>
</tr>
<tr>
<td>FLIP</td>
<td>Signal used for out-of-phase skew detections. This input is buffered with a 0-3V CMOS buffer. Note that this signal only applies to path B of the HRSD.</td>
</tr>
</tbody>
</table>

Table 2: Input/Output of ASIC

The **FLIP** signal controls one of the selectable inverters. Note that only one inverter is
able to invert the ECL signal in order to simplify the ASIC I/O (inverting both signals
accomplishes nothing). The two bias signals, **BIAS-A**, and **BIAS-B** are used to set a reference
voltage level for the LVC blocks. The idea is so that different input swings can be used with this ASIC, rather than a concrete 0-3V or 0-5V swing. This will be explained in further detail in the circuit overview.
3.2 System-Level

Figure 12 depicts the operational block diagram this ASIC will follow in the proposed verification process. All of the channels that comprise an ATE system are broken down into groups of 48, with each group assigned to a particular DUT. In the ATE industry, each physical point on the load board that contains a DUT and its 48 connection pads is called a device site. While it is not critical for channels from different device sites to be deskewed, it is absolutely necessary for all 48 channels of a single device site to be verified so that accurate tests can be made on the DUT.

![Operational Block Diagram](image)

**Figure 12: Operational Block Diagram**

In order to verify each device site of the ATE system, one ASIC per device site will be used to provide skew information to the system. As illustrated in Figure 12, multiple ASICs will be placed on a rigid substrate (load board) allowing for the testing of multiple groups of device site channels at once. A custom probe card will be used that will be aligned specifically to the pinouts of the ASICs used in the verification process. By doing this, we are verifying the ATE system at the DUT-level, bypassing the need for a DIB and the robotic setup altogether. The verification procedure is setup exactly like a test procedure on a DUT, thereby removing the need
for any type of intrusive verification interface. The ASIC is essentially taking the place of the DUT in order to provide device-level information to the test system.

Using available DC paths of the ATE system to address the multiplexers, each ASIC will perform a skew measurement among all 48 channels being probed. Although the ASIC only provides a logic level according to the polarity of skew involved between the two measured signals, using the Timing Generator block in conjunction with the strobed comparators will allow for quantitative data to be produced on the relative skew between the two signals. The comparators will allow the ATE system to perform a search on the transition of the ASIC’s output logic level based on the timing of the reference signal. This is enough information to provide quantitative data to the system. The probe station will interface to each ASIC and provide the means necessary for the ATE Functional Block to communicate with the ASIC. The output of each ASIC will be sent to free device site channels in the ATE system to be processed accordingly.

After sending reference edges to each channel, a relative skew distribution among all channels can be calculated. Since there are only two multiplexers, a group of two skew distributions, one for each multiplexer is enough information to deduce the relative skews among all channels tested. Since the ASIC is directly at the DUT-level, we can assure the ATE customer verifications much more accurate than those with the conventional method.

The use of the probe station in the verification path adds another exciting possibility to the current testing scheme. The ATE industry as a whole has taken dramatic steps in order to gain the ability to test at the wafer level in their current and future systems. These steps have improved the probe stations to the point where we can now probe memory wafers directly through the use of high precision probe cards as was discussed earlier. Because we are replacing the DUT with the calibration ASIC, we can extend this idea onto the wafer level. Rather than use an ASIC load board, we can instead spin an entire wafer of the verification ASICs and use this wafer in place of the load board in order to verify a wafer-level system. The complication that arises from this method is that a new probe card will need to be designed to fit the pin layout of the wafer.

Initially, the proposed ASIC will be used in a packaged form as was discussed earlier, but as the industry pushes memory testing further back in the development process, wafer level verification will be a definite possibility with this new verification scheme.
Chapter 4: Integrated Design

4.1 Process Technology and Tools

Preliminary simulations were run with device models from various fabrication processes available in order to evaluate performance. These include Taiwan Semiconductor’s (TSMC) 0.35μm MOS process, AMI’s 1.2μm BiCMOS process, Hewlett Packard’s (HP) 0.35μm MOS process, Austria Mikrosysteme’s (AMS) 0.8μm BiCMOS process, and Supertex’s 2.0μm BiCMOS process. Pure MOS processes were included just as a comparison, or benchmark for the BiCMOS processes.

Based on the preliminary simulations, the ASIC was fabricated and designed with Austria Mikrosysteme’s 0.8μm BiCMOS process due to the finer channel lengths available for the MOS devices. All bipolar devices used in the design, save for the output transistor, are double-base configured transistors due to the relatively large 0.7mA switched in each ECL gate. A summary of the BiCMOS technology for typical device parameters of this process are given in the following table.

<table>
<thead>
<tr>
<th>Symbol and Parameter</th>
<th>Conditions</th>
<th>Typical</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bipolar Devices</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_T ) - Transit Frequency</td>
<td>( V_{CE}=3 \text{ V}; I=165\mu\text{A} / \mu\text{m}^2, ) NPN</td>
<td>12 GHz</td>
</tr>
<tr>
<td>( B_{VCES} ) - Breakdown Voltage</td>
<td>NPN</td>
<td>16 V</td>
</tr>
<tr>
<td>( h_{FE} ) - Forward Current Gain</td>
<td>NPN</td>
<td>100</td>
</tr>
<tr>
<td>( V_{AF} ) - Early Voltage</td>
<td>NPN</td>
<td>32 V</td>
</tr>
<tr>
<td>( r_{bb} ) - Base Resistance</td>
<td>NPN</td>
<td>1kΩμm</td>
</tr>
<tr>
<td>( r_c ) - Collector Resistance</td>
<td>NPN</td>
<td>320Ωμm</td>
</tr>
<tr>
<td><strong>CMOS Devices</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( B_{VDSS} ) - Drain-Source Breakdown Voltage</td>
<td></td>
<td>13 V</td>
</tr>
<tr>
<td>( R_{POLY1} ) - Poly 1 Resistivity</td>
<td></td>
<td>22Ω /</td>
</tr>
<tr>
<td>( R_{POLY2} ) - Poly 2 Resistivity</td>
<td></td>
<td>67Ω /</td>
</tr>
<tr>
<td>( C_{POLY} ) - Poly/Poly Capacitance</td>
<td></td>
<td>1.77fF / μm^2</td>
</tr>
</tbody>
</table>
Due to the precise timing requirements for this ASIC, none of the standard ECL or CML cells were used from the process vendor. Instead, the design was done from the transistor-level with careful attention paid to the layout of the elements and even the traces connecting them together. The only standard cells used in the custom ASIC were the some of the CMOS D-Latch cells as well as the periphery cells because of the Electrostatic Discharge (ESD) protection and digital buffers built into them. A figure of the final layout for this ASIC as well as the package bondwire diagram can be seen in Appendix A.

The motivation for using a BiCMOS fabrication process rather than a pure MOS process becomes clear at this point. Because of the high dependence of both matching (tighter control on betas of BJT's) and gain on the overall accuracy of this ASIC, bipolar parts were needed to implement this design. It should be noted that preliminary simulations were done with Taiwan Semiconductor’s 0.35μm MOS process using resistively loaded MOS differential pairs rather than the ECL gates used in this design. Accuracy was decreased by more than an order of magnitude, and thus a MOS implementation was ruled out. With accuracy as the primary goal, high-speed bipolar parts are a necessity in this design.
4.2 Analog Multiplexers

Using a novel array of MOS transmission gates, the 24:1 Analog Multiplexer provides the ability to process 24 test channels with very low input-to-output capacitance. Matching for each path of the multiplexer is high, due to the high MOS device matching of the AMS fabrication process. A brief overview of analog switching networks is a basis for understanding the improvements made by this particular analog multiplexer.

One may argue that a controllable device that simply passes a waveform from input to output can be implemented with a single MOS transmission gate. The transmission gate provides a rail-to-rail swing, has relatively constant on-resistance (Figure 13), and is easily fabricated. Using an array of these devices could provide a simple solution to an analog multiplexer.

![Figure 13: MOS Transmission Gate On-Resistance (Enable high)](image-url)
The problem with using this approach is that the feedthrough caused by capacitively coupled input-to-output transients degrades the output signal as depicted in Figure 14A. The input-output capacitance of each of the transmission gates is large enough to cause a considerable amount of signal degradation on the output node. This node is not isolated enough from each of the multiplexer paths in order to realize an ideal analog multiplexer. Considering there are many signal paths in the multiplexer, the output signal will be severely polluted.

An improvement on the original design is an analog multiplexer composed of a series of T-configured MOS transmission gates as shown in Figure 14B. The two “horizontal” transmission gates provide the path necessary to pass the input to the output node. The grounded “vertical” transmission gate provides a path for the feedthrough to exit the circuit, without inducing any degradation on the output node.

While the T-configured multiplexer improves on the signal fidelity, the waveform slowdown caused by lumped capacitance on the output increases substantially because of the added transmission gates per signal path. Because a minimum of 24 signals needs to be processed in each multiplexer, this configuration proves unfeasible for our ASIC. A vast improvement on the T-configured multiplexer blends the ideas of the two initial designs together allowing very little feedthrough degradation as well as small lumped output capacitance. This combination allows for an ideal 24:1 Multiplexer for use in the ASIC. Figure 15 illustrates this improved design. (For purposes of illustration, this multiplexer is only 12:1)
This multiplexer consists of two groups of six “horizontal” transmission gates coupled to two “vertical” grounded transmission gates. These gates provide the exit path for the feedthrough signal. Another pair of “horizontal” gates provides the output path for the selected signal. This implementation of the analog multiplexer provides a low capacitance, low feedthrough switching network, allowing for maximum input-output signal fidelity. Note that in any selected path, there is still a chance of feedthrough from the other five transmission gates connected at their outputs. This can easily be remedied at the system-level by minimizing the activity on these five channels during a verification procedure. The 24:1 multiplexer used in this ASIC is based on this hybrid design and is a straightforward extension of the above 12:1 multiplexer.

Simulations comparing input-to-output signal degradation between the improved 24:1 multiplexer of Figure 14B and the 24:1 hybrid multiplexer can be seen in Figure 16. All comparisons were done with AMS’s 0.8µm BiCMOS process SPICE models at the Typical-Mean process corner.
Figure 16: Multiplexer Comparison

As you can see, the capacitive slowdown caused by the lumped capacitance of the T-gate multiplexer is too large to be feasible in the design. With the input signal risetime set to 1.2ns, the output risetimes are 1.277ns for the Hybrid output signal and a severely degraded 2.085ns for the T-gate output signal. The Hybrid design improves input-output capacitance by a considerable amount. With minimal signal degradation, minute feedthrough, and small on-resistance variation, the Hybrid analog multiplexer design proves well suited for the high accuracy necessary for the ASIC.
4.3 Latched Decoder

Because the ASIC consists of two 24:1 analog multiplexers, full addressing capabilities would require 5 address lines for each multiplexer, totaling 10 pins of the ASIC. Given that ATE systems have a limited amount of resources, minimizing the number of DC signals to the ASIC is a high priority. Also, the already large number of input signals of the ASIC creates a situation where the die is pad-limited rather than core-limited. This forces the use of long capacitive traces from the I/O pad ring to the inner core circuitry for each signal. Because of this, the minimization of I/O pads on the die is essential in order to keep signal degradation as small as possible.

In order to remedy this situation, two 5-bit to 24 line decoders are used to address the two multiplexers as shown in Figure 18. In order to reduce the total number of address lines, only 5 address bits are used to decode both multiplexers. The differentiation between the two decoders is handled through a set of CMOS D-Latches. A sixth bit is used to control which set of latches is transparent, holding the previous address on the other set of latches with the use of an inverter. Used this way, we can select any address from either multiplexer independently from the other multiplexer as long as we control the Select5_Enable signal properly.
The actual decoders themselves were designed in such a way that layout area and permutability were the two main issues addressed. Speed is not an issue in the operation of the decoding process because during the verification procedure, even a few nanoseconds of R-C delay in the decoder is allowable. This is because during an address change, the verification procedure lets a few dummy cycles run before any assessments are drawn. This is to ensure that the decoders and the multiplexer addresses have stabilized before a valid comparison can be made with the HRSD.

Each decoder is composed of an AND-plane of chained NMOS pull-down devices used in conjunction with a weak pull-up PMOS device. The use of a weak pull-up device increases the static power of this ASIC, but is still not enough of an issue to cause problems in an ATE verification because of the fact that the system already reserves power for the DUT’s. Simply by changing the position of the diffusion contacts, we can create different logical expressions as needed. Figure 19 illustrates the decoder design showing only the first 6 outputs. Since each isolation transmission gate (the grounded t-gate) controls a group of 6 signal transmission gates, a large 6-input NOR gate is used to select the state of this device (off if any of the 6 signal transmission gates is selected and on if none are selected). This NOR gate also controls the final pass transmission gate in the multiplexer path with opposite logic.
Not only is the AND-plane implementation of the decoder permutable, it is also very compact. The actual HRSD circuit must be physically as close to the multiplexers as possible in order to reduce the capacitive metal connections between the input of the HRSD and the output of the multiplexer. This is important in the overall skew detection process, as signal degradation interferes with the accuracy of the results. In order to achieve this, the layout of the decoder was implemented according to a style shown by Professor Chris Terman illustrated in Figure 20.
This layout strategy conserves as much area as possible by creating a regular structure for the "ROM-like" decoder. The decoder output pattern is easily changed by simply changing the diffusion contacts that create the pull-down devices. Also, make note that some of the contacts can be shared in certain instances, making this layout strategy even more compact. The polysilicon gate inputs to the pulldown devices are strapped with metal2 in order to decrease the line resistance across the decoder.
4.4 High Resolution Skew Detector

The heart of the proposed ASIC is the High Resolution Skew Detector, which will take the two selected inputs from the multiplexers and distinguish skews within a few picoseconds. The HRSD is composed of mainly Positive Emitter Coupled Logic (PECL) gates suitable for high-speed designs with relatively low transistor counts. Using PECL designs have the added advantage that the 0-5V voltage rails used to power the MOS devices can be reused in the PECL circuits. DC biasing for this circuit was done with positive-feedback Widlar voltage references. These voltage references bias the emitter degenerated current sources used for the PECL gates as well as provide DC bias voltages for the differential pairs.

As was discussed earlier, metastability has been the limiting factor on all calibration/verification systems that involve logic-oriented implementations. In order to overcome this fundamental limitation, the HRSD used in this ASIC foregoes the use of any sort of flip-flop altogether and implements a unique Time-to-Voltage Conversion (TVC) technique in order to produce the desired logic levels. This TVC technique relies heavily on the concept of timing consistency and centers on two main ideas. The first idea focuses on the finite nature of voltage risetimes of any particular signal in the system. This idea is extremely important in the operation of this circuit and is described in the following figure.

![Risetime Illustration](image)

**Figure 21: Risetime Illustration**

The figure portrays two typical voltage waveforms being compared with only a few picoseconds of skew separating them in the time-domain. In order to better illustrate the point, the time axis has been enlarged to stretch the voltage transitions. As you can see, although the skew between the two waveforms is extremely small, the voltage difference between the two signals is maintained for at least the entire risetime of the two signals. This gives us the opportunity to latch a logic level based on the voltage difference between the two signals rather
than the time-domain difference between the signals. Since the window of time to latch this signal is much larger than the actual skew of the two waveforms, the resolution of the HRSD is determined only by the voltage sensitivity of the latch, rather than the time-domain metastability of a flip-flop. This proves to be an extremely powerful idea and is exploited in this particular HRSD as will be explained fully in the circuit design.

The second idea that contributes to the timing consistency of this ASIC focuses on a synchronous design. The HRSD uses a clocked latch in order to produce the desired output level based on the polarity of the skew. In order to provide timing consistency, the clock for the latch is actually derived from one of the two input signals. This ensures that at any particular transition, the clock will always latch a valid signal. The details of this process are described in the circuit design. By making the clock a synchronous element, we eliminate the need for any on-chip clock, as well as any timing issues involved with such an implementation. A simplified schematic is shown on the following page in Figure 22 for visual purposes. The entire high-level schematic diagram is depicted in the schematic following Figure 22 on the next page. Each block in this high level schematic will be discussed separately and in much more detail.
Figure 22: Simplified HRSD Schematic
Figure 23: Complete HRSD Schematic
The entire HRSD can be broken down into functional blocks similar to the original ASIC block diagram (Figure 11). The flow of this particular circuit will be illustrated from input to output with a description of each functional block and how it affects the signals of significance.

4.4.1 DC BIASING

The entire HRSD needs only two DC voltages in order to operate correctly. These are VDD, and VDD_OUTPUT. VDD is the global power supply of the HRSD and is a nominal +5 volts DC. Note that this is also the universal power supply for the ASIC powering all of the MOS devices as well. VDD_OUTPUT is the localized power supply for the output transistor of this ASIC. Because the output transistor can pull up to as much as 23mA, a localized power supply is necessary in order to reduce global supply noise.

There are two DC signals used throughout the ASIC that are produced by the reference generator circuit shown on the following page. These are the 1.25V DC signal used to bias the current sources and the 3.9V DC used to bias the ECL gates in the design. The 1.25V DC reference is provided for by a current mirror with a high accuracy reference resistor. The reference resistor provides a highly controlled current to provide the 1.25V reference signal as shown in the schematic diagram in Figure 24. The reference is AC decoupled by a large poly-capacitor.

![Figure 24: Voltage Reference Circuit](image)
The 1.25V DC level is used to bias all current sources in the design for all the ECL gates. All gates in this particular circuit are ECL bipolar designs that are biased with 0.7mA current sources. All constant current sources, except for the ones used in the Gilbert inverters are simple DC biased, emitter degenerated transistors as shown in Figure 23.

The 3.9V DC level is used to provide the differential voltage reference for all of the ECL gates. This DC level needs to be much more stringent than the current source bias because of the sensitive timing nature of the ECL gates in the HRSD. Because of this, the 3.9V DC level is produced with a tracking circuit that is essentially, half of the differential stage of an ECL gate. Referring back to the schematic diagram on the previous page, the tracking circuit is biased with the same emitter degenerated current source as the ECL gates in the design. By putting two of the same load resistors used in the ECL gates in parallel, we ensure that the reference voltage is exactly at the midpoint of the ECL signal swing, which is a nominal 3.9V. Since the circuit is biased with the same current source as that in the entire HRSD, the 3.9V DC level will always settle at the midpoint of the ECL swing even if the voltage levels change due to process variations, temperature gradients, etc. The DC output also uses a large poly-capacitor for the purposes of AC decoupling.
4.4.2 LEVEL CONVERTERS (LVC)

The LVC blocks in the HRSD are ECL buffers as illustrated in the following schematic diagram on the following page. The load resistors are 650 Ω, producing approximately 450mV swing on the output. The output emitter-follower stage is biased with the same emitter-degenerated constant current source used throughout the design.

![Figure 26: LVC Block](image)

There are a number of LVC blocks used throughout the HRSD, each serving a different purpose. The first set of LVC blocks (lower left corner of high-level schematic) level-convert the buffered input FLIP signal and the ground signal into appropriate 450mV peak-to-peak ECL levels. This provides the two signals necessary for the GILINV blocks as will be described below. The two LVC blocks outside of the two direct input paths serve to buffer the loading on the signals caused by the clock circuitry. Although there is no clock circuitry associated with signal path B, an additional LVC block is used to provide matching load capacitance. The remaining two LVC blocks are actually part of the delay elements and are used to match the INV block in the clock circuitry path.
4.4.3 GILBERT INVERTERS (GILINV)

The ATE industry has had an increasing need to calibrate/verify signals that are not only in-phase, but out-of-phase as well. In order to measure the skew of two-signals that are approximately 180 degrees out of phase, the HRSD uses a selectable inverter as its input stage. The selectable inverter is implemented with a Gilbert Multiplier Cell used in the balanced modulator mode rather than the pure hyperbolic tangent of product mode [14]. Used in this fashion, the Gilbert Multiplier acts as an inverter and simply produces an ECL 450mV peak-to-peak output that is either an inverted or non-inverted version of the input. Note that this particular block serves as both the inverter (INV) and the initial ECL level normalizer (LVC) as illustrated in Figure 11, not to be confused with the INV block shown in the full schematic. The schematic diagram is depicted in the following figure.

![Diagram of the GILINV Block]

Figure 27: GILINV Block
The GILINV block takes the signal from the multiplexer as well as the input bias signal (BIAS-A/BIAS-B), and produces the ECL-swing output. The DC BIAS signals should be at mid-swing of the input signal in order for this block to function correctly. The idea behind using an off-chip bias is that it allows for the flexibility of testing a wide-range of input signals rather than a set 0-5V or 0-3V input swing.

A limiting factor in this circuit is the common mode-range of the input, due to the loss of headroom from the second tier of differential pairs. In order to increase the common-mode range, the current sources for the Gilbert Inverters are implemented with headroom in mind as shown in the schematic. Although this block uses the same 1.25V DC reference to bias the current source, we are instead mirroring the current in the left branch in order to bias the Gilbert Inverter. This way, at the cost of an extra transistor and a little bit more power, we increase the common-mode range of the input by approximately a volt.
4.4.4 DELAY ELEMENT

The schematic in Figure 28 shows the delay block circuit used in both the Data delays as well as the Clock Pulsewidth delay. The delay elements are simply a string of three LCML inverter gates (almost exactly the same as the LVC blocks) on which several transistor-type junction capacitances are loaded. Each gate provides a little over 100ps of time delay per block with an added 2.5ps per Base-Emitter junction capacitance (used for fine tuning purposes.)

Figure 28: DELAY Block

Timing is of critical importance in this ASIC, therefore all three delay blocks used are identical, which allows for the circuit to work correctly even with small timing errors induced by process variance. Although the absolute values of the time delays may change over the process corners, the relative values, or matching between the three delays will stay within 0.05 percent. The following table summarizes the absolute time delay variation at each process corner and at various temperatures.
<table>
<thead>
<tr>
<th>Temperature</th>
<th>Typical Mean</th>
<th>Worst-case Speed</th>
<th>Worst-case Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°C</td>
<td>320ps</td>
<td>350ps</td>
<td>300ps</td>
</tr>
<tr>
<td>25°C</td>
<td>326ps</td>
<td>360ps</td>
<td>312ps</td>
</tr>
<tr>
<td>50°C</td>
<td>335ps</td>
<td>370ps</td>
<td>320ps</td>
</tr>
</tbody>
</table>

As you can see, the delay variation is less than 50 picoseconds from process corner to corner as simulated with HSPICE. While this value may seem large in comparison to the time intervals we are trying to distinguish, it will be shown later that this is nowhere near the variation needed to throw off the accuracy of the circuit. What is important is the relative delay variation that occur between each of the three delays, most importantly, between the two Data delay elements.
4.4.5 DIFFERENTIAL AMPLIFIER

The high-speed differential amplifier (DEF) depicted in Figure 29 converts the voltage difference between the two signals into a string of pulses used in the latch block. The DEF block is an essential part of the circuit that directly affects the resolution of the skew detector.

Figure 29: DEF Block

Figure 30 shows the voltage signals that appear at the inputs of the differential amplifier for two signals that are skewed by a few picoseconds. As you can see from the simulation, even though we are dealing with skews on the order of picoseconds, the voltage difference between the two signals is maintained for at least the slew rate of the input signals (~300ps). This gives us the immense advantage of detecting a few picoseconds in a window of a few hundred picoseconds, something truly unique to this circuit. It is a subtlety that accounts for the higher degree of accuracy in this particular skew detection implementation.
Figure 30: Timing Simulation (AMS 0.8μm, All parasitics included) Pulse Width of DATA 
~400ps
4.4.6 HIGH-SPEED LATCH PAIR

The differential pulse that is generated by the DEF block is then latched by the ECL Latch shown on the schematic in Figure 31. The Latch is a typical two-tier differential ECL latch biased with the same 0.7mA current sources used throughout the design. The outputs are buffered with emitter-followers in order to increase the output resistance of the latch. The differential clock signals are one-shot pulses generated from the clock circuitry.

Figure 31: High Speed Latch (LATCH) Block

The idea behind this Time-to-Voltage Conversion (TVC) is that the Latch does not need to distinguish small changes in the time domain, which is inherently limited by device performance (flip-flop metastability). Instead, the latch needs to distinguish small changes in the voltages. This is done by opening and closing the latch with the one-shot clock signal at the precise moment the DEF produces the voltage pulse described in Figure 30.
4.4.7 CLOCK CIRCUITRY

An interesting aspect about this circuit is that it is completely self-timed, with the clock signals for the high-speed latch being derived synchronously from one of the input signals. This allows for added flexibility to the circuit, as it needs no off chip clock to operate the circuit. Referring back to Figure 22 (or 23), we can see that the one-shot clocks to the LATCH block are produced with a delay block, an ECL inverter and an ECL AND/NAND gate. The INV block is simply another ECL inverter gate that is almost exactly similar to the LVC gate, save for the output node. The AND/NAND gate is based on an older ECL design. The INV block is depicted in Figure 32 while the AND/NAND gate is shown in Figure 33.

![Diagram of INV Block]

Figure 32: Inverter (INV) Block
The one-shot clock is produced by performing a logical AND on one of the input signal edges and a delayed and inverted version of the input signal edge. This produces a one-shot pulse at the precise instant the DEF block produces the differential pulse signal corresponding to the polarity of the skew involved in the circuit. By adjusting the width of the strobe pulse as well as the strobe timing in relation to the DATA signals, we can accurately detect very small skews with this implementation. A simplified timing diagram is shown in Figure 34 for both skew polarities. The clock is being derived from the input signal IN2.
Figure 34: Simplified Timing Diagram

As you can see from the simplified timing diagram, what separates this HRSD from other implementations is that of timing consistency. Rather than using an edge triggered flip-flop, which becomes metastable with small time-domain differences of the input edges, the proposed HRSD amplifies the voltage difference between two signals first, and then latches this amplified output in order to produce the desired skew signal. The advantage of using this approach is that rather than worry about how close the target and the reference edges are in relation to each other, we can produce an amplified "difference signal" that can consistently be placed in the same relative position in the time domain. Because the latch clock is derived synchronously from one of the input signals, we can always place the clock at the precise instant the difference signal is valid. With this kind of consistency, the accuracy of the Skew Detector is not dependent on any "time ceiling" inherent within a flip-flop, rather, it is simply dependent on the gain of the differential amplifier. It is essentially converting the "time ceiling" into a "voltage ceiling" which is determined by the sensitivity of the latch. This is the crux behind the proposed HRSD and is the reason for the vast improvement over the more conventional schemes.

Using a more analytical approach, let $\tau_s =$ Skew Detection Resolution. Since the gain of the differential amplifier is directly related to the resolution of the circuit we can redefine $\tau_s$ in terms of our new implementation:
\[ \tau_s = \frac{V_{\text{height}} \cdot \tau_{\text{slew}}}{(g_m R C \phi)} \]  
(2)

Where \( \tau_{\text{slew}} \) is also a function of the gain through the LVC and GILINV blocks. Using the parameters used back in expression (1) in Chapter 2.5 for the flip-flop based implementations, we find that

\[ \tau_s = 0.71 \text{ ps}. \]

Expression (2) indicates that \( \tau_s \) is insensitive to metastable transitions and is the single reason why this circuit is superior to the other more conventional implementations. The only factors that determine \( \tau_s \) are:

1) voltage gain of the circuit
2) clock timing (accuracy of delays)
3) clock pulse width (accuracy of delays)
4) process variance (fabrication variance)
5) systematic disturbances (input signal offset, noise)

With the proper placement of the strobe signal, we can achieve a very high degree of accuracy with this particular skew detection scheme. An added advantage to this skew detection scheme is that the range of the measurement is theoretically limitless. The ASIC will provide a valid logic level based on the skew polarity for any magnitude of time-domain skew.
4.4.8 OUTPUT STAGE

The output stage for the ASIC is implemented with another differential pair and a large emitter-follower that uses a power transistor. The differential pair is biased with three times the current as the rest of the ECL gates in order to increase the voltage swing on the output of the ASIC. The schematic is illustrated in the following figure.

![Output Stage Diagram](image)

Figure 35: Output Stage
ASIC SPECIFICATIONS

All ASIC Specifications were simulated on all process corners at a temperature range of 0-60°C. Simulations can be found in Appendix C.

Power

Nominal: 0.2946 watts
Worst Case: 0.4443 watts (High Beta-Worst Case Power Process Corner)

$V_{DD}$ Tolerance: ± 5%, nominal 5V

Inputs

FLIP signal: 0V-3V CMOS ($V_{IL}$=1.3V, $V_{IH}$=1.4V)
ADDRESS signal: 0V-3V CMOS ($V_{IL}$=1.3V, $V_{IH}$=1.4V)
DUT INPUTS: $V_{IL}$=BIAS – 0.1V, $V_{IH}$=BIAS + 0.1V (BIAS is input reference)
Common mode input range (BIAS and DUT input): 1V-3.8V

Output (As will be used in ATE system)

270 Ohm Load to ground
$V_{OH}$=2.8V – 3.257V
$V_{OL}$=2.01V–2.35V

50 Ohm Load to +3V
$V_{OH}$=3.84V – 4.101V
$V_{OL}$=3.007V–3.108V

Skew Detection Resolution

Nominal: 3ps
Worst Case: 6ps

Setup Time after Address Change

Nominal: 5ns

Packaging

64-pin Ceramic Thin-Quad-Flat-Package (TQFP)
(A ceramic package was used in order to examine the die itself)
Chapter 5: Conclusions

Future work on this ASIC will be exploring the use of it as well as the new verification scheme at the wafer-level as was discussed previously. The need to push the memory testing procedure (or even logic testing procedures) earlier in the development process will motivate this evolution of ATE systems. By eliminating faulty wafer cells early, the cost of detecting faulty memory modules will significantly decrease, thereby decreasing overall costs to the consumer. The ASIC has the advantage of impacting the ATE industry not only now, but in the future as well.

Improvements to the circuit design itself could include a better design for the Multiplexer Decoder. This decoder, while very compact in size, consumes static power due to the weak pull-up devices used to encode the logic. A compact design which incorporates a true CMOS-style circuit could eliminate the static power dissipation of the decoder as well as decrease overall power of the ASIC. In addition to the decoder, the reference generator circuits could also be improved by being based on robust Bandgap Voltage Generators. These circuits provide relatively stable voltage levels regardless of process and temperature variations. Finally, the high-speed latch used in this circuit is a basic ECL latch which has relatively high sensitivity. By increasing the gain of this stage using analog circuit "tricks" the timing sensitivity of the HRSD could increase substantially. This will be looked into further in later generations of this particular ASIC.

A drawback to the new verification method itself is the fact that a new ASIC needs to be spun for every different memory device pinout. Although the probe card needles also need to realigned with every different pinout, changing this is much easier than spinning a new SD-34 ASIC for every new memory module. (New technologies in probe card alignment have been implemented using polyimide membranes.)

Overall, a novel approach to ATE verification has been researched and implemented using a new skew detection technique. This new method involves a custom BiCMOS ASIC that will possibly provide test timing resolutions orders of magnitudes higher than conventional techniques due to its low sensitivity to metastable jitter. In addition to the higher timing resolution, the ASIC will also provide parallelism to the system verification process as well as provide the possibility of verifying systems at the wafer level. This will reduce verification times from many hours, to only a few minutes. The ASIC could have an immense impact on the ATE industry as channel densities increase over time and could prove to be a significant advantage in future memory test systems.
Chapter 6: References


APPENDIX A: Layout and Bondwire Diagrams
A) DEVICE-,DRAWING NUMBER: 
B) ASSEMBLY CODE: BZZ-X 
C) SCALE: 20 / 1 
D) DIE SIZE: 
E) DIE ATTACH PAD SIZE: 280X280 mil 
F) PACKAGE TYPE/BODY SIZE: TQFP 64 LD / < 10X10X1.4 mm > 
G) BONDPAD PITCH (MIN): 
H) BOND PAD SIZE (MIN): 
I) WIRE SIZE: 
J) WAFERTHICKNESS: 
K) CAVITY (UP OR DOWN): UP 
L) REMARKS: 

QA - APPROVAL: REV.: