Thermal Characterization and Modeling

of LDMOS FETs

by

Jihye Whang

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

May 22, 2000

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Abstract

LDMOS has emerged as the preferred device technology for high power base station design in wireless phone systems. Subject to increased operating temperatures due to self-heating at high power density levels, LDMOSFETs must be thermally characterized and their thermal behavior modeled for accurate prediction of power performance and reliable circuit design. This thesis focuses on the thermal characterization and modeling of LDMOSFETs. Commonly, a simple thermal model composed of a current source representing the power dissipated in shunt with a single thermal resistance and capacitance is used to predict thermal behavior of FETs. Direct methods for determining the operating temperature and thermal resistance of transistors are mostly by optical means using IR microscope or nematic liquid crystal. However, both methods are thermal steady state measurements that require cumbersome calibration techniques and cannot be performed on encapsulated devices. A separate measurement that involves measuring the change in drain current due to self-heating is required for determining the thermal time constant and thermal capacitance. Indirect, electrical methods that exploit the dependence of a diode’s I-V characteristics on temperature have been documented for determining the thermal resistance of IGBTs and GaAs MESFETs. In this thesis, a similar method for LDMOS technology has been implemented to determine the transistor’s steady state operating temperature and the results verified against IR scans. The technique additionally captures the transient thermal behavior of the device. Measurements obtained from this technique were used to develop a multiple RC thermal sub-circuit model. The thermal sub-circuit was ultimately incorporated in Motorola’s electro-thermal model to accurately predict the electrical performance of LDMOS devices under DC, small signal, and large signal conditions.

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Acknowledgments

This work was conducted at Motorola as part of MIT’s EECS VI-A Co-operative Program. While it would be impossible to name every engineer/scientist that deserves recognition for his or her contribution, I would like to individually thank those in Motorola’s RF Modeling Group: my supervisor and mentor, Jaime Plá, Daren Bridges, Peter Aaen, Tao Liang, and Eric Shumate. This work would not have been made possible without each and every one of them. I also would like to give thanks to Roger Stout, formerly of Motorola’s Semiconductor Components Group for sharing his lab and expertise.

To my advisor, Prof. Jesús del Alamo, I thank him for his advice, guidance, and inspiration. It was his dynamic and enthusiastic teaching of Integrated Microelectronic Devices (6.720) that sparked my interest in semiconductors and convinced me to continue in the engineering profession.

To my friends, thank you for remaining my friends despite my incessant whining and complaining. In particular, I thank Daniel Rosenband, Laura Bouwman, Sandra Chung, and Susan Lindholm for making survival at MIT possible and often enjoyable.

At lastly, I thank my parents for giving me their undying love and support, and the freedom to take the long (and costly) way to where I am today.
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Chapter 1

Introduction

1.1 Background

LDMOS devices like other semiconductor devices that are designed for high power density applications are subject to significantly increased operating temperatures due to self-heating. Self-heating not only limits the reliability of the device but also degrades its power performance. In order to obtain an accurate LDMOS model for predicting power performance and for reliable transistor or circuit design, LDMOS devices must be thermally characterized and their thermal behavior incorporated in the model so that the effects of temperature on the electrical model parameters can be accounted for.

Motorola has developed an analytical nonlinear, electro-thermal model for their LDMOS devices. In the model, the electrical and thermal modeling is integrated into one model by first decoupling the electrical and thermal dependencies to obtain isothermal model parameters and their temperature dependencies and then coupling them with a thermal analog sub-circuit. The thermal sub-circuit is used to calculate the instantaneous temperature rise of the device due to self-heating and in its simplest form consists of a current source representing the power dissipated in shunt with a thermal resistance and thermal capacitance. The focus of this thesis is on the development and evaluation of techniques for extracting the thermal impedance and to investigate the impact of the thermal impedance on LDMOS devices.

Presently in industry, various methods for determining thermal resistance are used. Thermal simulations using finite element or finite difference analysis tools are commonly employed to predict thermal resistance. While measurements of real devices are avoided by performing simulations, the disadvantage of this method is that assumptions on the device structure, the power distribution throughout the device, and the boundary conditions limit their accuracy.

Direct methods of evaluating thermal resistance of power FETs are mostly by optical means, infrared microscope or nematic liquid crystal. While these tools are effective as a diagnostic tool and for reliability purposes, both methods involve cumbersome calibration procedures. In addition, a device in a capsulated plastic package cannot be subjected to the test.

Indirect, electrical methods for determining thermal resistance exist for MESFETs, HBTs, and HEMTs. For example, for GaAs MESFETs, the Schottky barrier diode being highly temperature sensitive can be used as a thermometer to obtain the thermal resistance. However, no similar method has been documented for LDMOS devices. Such an electrical method is desired since the measurement can be easily integrated into the electrical measurements already required for the model extraction.
In this thesis, all of the aforementioned procedures are developed and tested for determining thermal resistance of LDMOS devices. The thermal capacitance was also extracted to complete the thermal subcircuit for the electro-thermal model. The resulting electro-thermal model was verified under DC, small signal, and large signal conditions.

1.2 LDMOS Technology

A cross section of Motorola's LDMOS device [1] is shown in Figure 1. The device is characterized by its laterally diffused channel doping implant and lightly doped n-region. The former characteristic controls the threshold voltage and provides higher transconductance while the latter reduces the electric field at the drain. In addition, a metal field plate that overlaps the gate and is connected to the source increases the breakdown voltage and reduces the gate to drain capacitance (C_{GD}).

![LDMOS Vertical Cross Section](image)

Figure 1: Cross section of Motorola's LDMOS FET.

High performance LDMOS transistors are targeted for low as well as high voltage applications. Low and medium voltage LDMOS devices are suitable for portable applications such as analog cellular, GSM cellular, PCS, cordless phones, RF modems, cable modems and talkback pagers. High voltage LDMOS devices for high linearity designs include 28 Volt LDMOS field effect transistors (FETs) aimed at cellular and paging base station amplifiers operating at UHF, VHF, 900 MHz, and 2 GHz.

1.3 Self-Heating Effects

Self-heating effects are detrimental to the performance of high power density devices. In particular, the increased junction temperature lowers the threshold voltage (Fermi potential used to calculate V_{th} is temperature dependent) and reduces the channel mobility. The temperature dependence of channel mobility is modeled as:

\[ \mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \]  

Eqn. 1

where \( m \) is equal to 2.5 for LDMOS devices [2].

The decrease in channel mobility from thermal effects can be observed in Figure 2. The graph is a comparison of drain current vs. drain-to-source voltage obtained from pulsed DC measurements and constant DC measurements. The pulse widths of the pulse
measurements are narrow and the duty cycle is low so that self-heating effects are not introduced. The constant DC measurements exhibit pronounced thermal effects in the saturation region due to the reduced channel mobility. To the first order, the equation for the saturated drain current is:

\[ I_d = \mu(T)C_{ox}(\frac{W}{2L})(V_{gs} - V_{th}(T))^2 \]  

Eqn. 2

At higher gate voltages, the channel mobility term dominates and the saturation current decreases with increased temperature. The transconductance, \(G_m\), is decreased at higher temperatures and thus the gain is also reduced. The decrease in channel mobility due to self-heating also increases the on-resistance, \(R_{on}\), by increasing the channel resistance. A large on-resistance, which is the inverse of the slope of the IV curves in the linear region, causes output power loss and reduces efficiency. Other self-heating effects include higher breakdown voltage (impact ionization rate decreases as the temperature increases), reduced mean time between failure (MTBF), and possibility of burnout. Because these thermal effects degrade power performance of LDMOS devices, it is critical that an LDMOS model incorporates the temperature dependence of the device electrical characteristics.

**Figure 2: Constant DC vs. pulsed IV measurements.**

### 1.4 Electro-Thermal Models

To properly account for self-heating effects, semiconductor nonlinear models need to dynamically account for model parameter temperature variations. Several authors [3,4] have already reported ways to implement dynamic self-heating effects into harmonic
balance simulators with bipolar junction transistors and field effect transistors nonlinear models. The assumption behind electro-thermal models is that the heat flow problem can be completely de-coupled from calculation of the device's electrical characteristics. During the model extraction procedure, the model parameters thermal and electrical dependencies are de-coupled by extracting isothermal model parameters and their temperature dependencies. One way [3] to determine the isothermal model parameters is by measuring the devices under pulsed DC and RF conditions. Another way [4] is by performing all measurements under non-isothermal conditions, i.e., constant DC and RF excitations, and then thermally de-embed the data to arrive at an isothermal set of measurements. The electrical and thermal model are coupled using temperature mapping functions to correlate the electrical model parameters and their thermal dependencies, and a thermal sub-circuit that calculates the instantaneous temperature rise in the device.

A thermal sub-circuit representation of the temperature rise in a device is derived from the heat flow equation. The equation for heat flow is given by [5]:

\[ \nabla \cdot k(T) \nabla T(x, y, z) - \rho c \frac{dT(x, y, z)}{dt} = -P(x, y, z) \tag{Eqn. 3} \]

where \( k(T) \) is the thermal conductivity, \( T \) is the temperature, \( \rho \) is the density of silicon, \( c \) is the thermal capacity of silicon, and \( P \) is the power density. If thermal conductivity is temperature dependent, Kirchoff's transform must be used to solve the heat flow equation for the temperature rise by using the thermal conductivity at \( T = T_0 \) and then computing the actual temperature rise with the following equation:

\[ \theta = T_0 + \frac{1}{k(T_0)} \int_{T_0}^{T} k(T')dT' \tag{Eqn. 4} \]

If the thermal conductivity is a constant and one dimensional heat flow is assumed, the heat flow equation is reduced to:

\[ k(T_0) \frac{\partial^2 T}{\partial x^2} - \rho c \frac{\partial T}{\partial t} = -P(x) \tag{Eqn. 5} \]

Integrating over the region of interest and with the appropriate boundary conditions (see Appendix A), the heat flow equation becomes a first-order ordinary differential equation

\[ \frac{T - T_0}{R_{th}} + C_{th} \frac{dT}{dt} = P \tag{Eqn. 6} \]

where \( R_{th} \) and \( C_{th} \) represent the total thermal resistance and thermal capacitance.

The thermal resistance represents the active device's and its surroundings' ability to disperse the generated heat which is equal to the power dissipated, \( P = I_d V_{ds} \) in FETs. Besides the die of the active device, the metal ceramic packaging consisting of the die bond, flange, and the flange to heat sink interface, all contribute to a thermal resistance that prevents heat dissipation of the device (Figure 3). The die and the flange pose the largest resistance to heat dissipation. All components need to be thermally characterized to accurately determine the thermal resistance.
The thermal capacitance accounts for the heat capacity of all the material layers from the silicon die to the CuW package flange, and thus, determines the transient thermal behavior of the device. The thermal time constant is given by product of the thermal resistance and thermal capacitance:

\[ \tau = R_{th}C_{th} \]  \hspace{1cm} \text{Eqn. 7}

with the units of \( C_{th} \) in J/°C.

The lumped RC thermal subcircuit representation of Eqn. 6 is shown below:

![Thermal Sub-circuit diagram](image)

**Figure 4. Thermal Sub-circuit.**

In steady-state i.e. \( \frac{dT}{dt} = 0 \), the analogous Ohm's Law (V=IR) relationship for the thermal sub-circuit is:

\[ T_{\text{rise}} = T - T_0 = R_{th}P \]  \hspace{1cm} \text{Eqn. 8}

where \( T_{\text{rise}} \) is represented by \( V_{th} \) and \( P \) by \( I_{\text{therm}} \) in the circuit schematic. The unit of temperature rise, \( T_{\text{rise}} \) is °C while \( R_{th} \) is °C/Watt and \( P \) is Watts. The thermal sub-circuit can be included as the fourth port in a FET model in harmonic balance simulators such as HP-EEsof's Libra™.

A flow chart of an algorithm commonly used to couple the electrical and thermal model is shown in Figure 5. Given a reference temperature by the user, the simulation begins by evaluating the temperature dependent parameters or temperature mapping functions of the electrical model at the reference temperature. With the resulting parameter values, the electrical characteristics of the device including the power dissipated, \( I_{\text{therm}} \), is derived for the reference temperature. The obtained \( I_{\text{therm}} \) is plugged into the thermal sub-circuit to determine the temperature rise and thus the new operating temperature. This new temperature is then fed back into the electrical model and the temperature dependent
electrical parameters are recalculated at this new temperature. The harmonic balance simulation is repeated to obtain the device's electrical characteristics including $I_{therm}$. $I_{therm}$ is fed into the thermal sub-circuit and the temperature rise is once again determined. This interaction between the electrical and thermal model is iterated until the electrical characteristics converge to a solution.

![Flow chart of an algorithm used to couple electrical and thermal model.](image)

While the above algorithm best illustrates the interaction between the electrical and thermal model, it is inefficient and slows down simulations considerably. Instead, Motorola has implemented the thermal portion of the electro-thermal model such that the voltage across the thermal subcircuit, $V_{th}$, is treated as a node voltage similar to the gate-to-source voltage and drain-to-source voltage. By doing such, the drain current and charge equations in the model become functions of three voltages, $V_{th}$, $V_{gs}$, and $V_{ds}$ and computation time for simulations is decreased.
1.5 Motorola’s MRF183 Field Effect Transistor
The Motorola LDMOS transistor used in this research was the MRF183 power FET (Figure 6). The MRF183 is a 24 cell transistor, each cell being composed of 56 gate fingers with a gate width of 90 μm each. The total gate width or periphery is 120.96 mm. The transistor is packaged in the N1μ250 (Case 360B), an air cavity, metallized ceramic package. It has a CuW substrate or flange with alumina window frame. The transistor is designed to deliver 45 Watts of RF power. The product is targeted for broadband commercial and industrial applications at frequencies up to 1 GHz. The high gain and broadband performance of these devices makes them ideal for large-signal common-source amplifier applications in base station equipment.

Figure 6: MRF183 Device.

1.6 Thesis Goals and Outline
The goal of this thesis is to demonstrate an indirect, electrical method for developing a multiple RC thermal model for packaged transistors such as the MRF183. The extracted thermal model when coupled with an isothermal electrical model form an electro-thermal model that is capable of predicting RF power performance.

For complete understanding of Motorola’s LDMOS Electro-Thermal Model, details of the electrical portion of the model are first presented. The succeeding chapter begins with a description of the package electrical model and the extraction procedure. For simplicity, the package electrical model is assumed to be independent of temperature. Chapter 3 presents the isothermal electrical model of the unpackaged FET. The isothermal electrical model is composed of a small signal and large signal model adapted from commonly known MESFET models.

In Chapter 4, a single RC thermal model for the MRF183 is presented using common techniques for extraction. The results from two simulation tools and direct measurements in the form of IR scans are shown for determining the thermal resistance. A current vs. time measurement with a step input power is used for determining the thermal time constant and thus the thermal capacitance. Ultimately, the results from this section are compared to those from the indirect electrical method demonstrated in Chapter 5.

Chapter 5 describes the technique of using the intrinsic substrate/source-to-drain diode as a Temperature Sensitive Parameter (TSP). After a brief description of the general methodology and setup, the oven calibration of the MRF183 is presented to show the dependence of diode voltage on temperature for a constant diode current. Cooling curves obtained from measuring the diode voltage of a device as it cools off from thermal steady
state are then shown. These cooling curves allow the extraction of a multiple RC thermal model that is consistent with the single RC thermal model. The chapter ends with discussion on the appropriate topology for the multiple RC thermal model. Often a non-grounded capacitor thermal model is mistakenly used. However, an argument is made for a grounded capacitor thermal model to accurately describe the physical, thermal system.

In Chapter 6, the validation of the complete LDMOS Electro-Thermal Model is given. Comparison of measured and modeled CW IV is presented to show the accuracy of the drain current equation and the steady-state thermal resistance. Measurements and simulations of CW S-parameters are also included to validate the small signal model. The large signal model is validated by comparing power figures of merit such as output power, power added efficiency, gain, and IMD with loadpull measurements of the MRF183.

Finally, Chapter 7 concludes the thesis and provides a summary of the entire research. In addition, ideas for future work are also suggested. In particular, the thesis does not rigorously examine the impact of the thermal capacitance and thermal time constant on device performance. An extension of this thesis would investigate the influence of the thermal capacitance and thermal time constant on circuit envelope simulations and measurements using continuous spectra or digitally modulated spectra.
Chapter 2

Package Electrical Model and Extraction

High power RF and microwave semiconductor transistors are often supplied in metal ceramic packages due to their ability to dissipate power and heat and their mechanical robustness. At high frequencies, the package contributes parasitic effects that need to be correctly modeled to predict the electrical performance of the packaged transistor. This chapter begins by describing the equivalent circuit topology for the NIμ250 package of the MRF183 device. A typical ceramic package equivalent circuit composed of shunt capacitors for the ceramic frame and lossy inductors for bond wires is used to model the NIμ250 package. Cross interactions in the package are modeled by a cross coupling capacitor and mutual inductance.

The NIμ250 package electrical model extraction procedure including measurements is also presented in this chapter. Electro-magnetic simulations of the package and bonding wires in Ansoft HFSS™ were first conducted and subsequently verified with S-parameter measurements of the package and bonding wires. For the sake of simplicity, the package model is assumed to be independent of temperature.

2.1 Package Electrical Model

For package electrical modeling, an equivalent circuit representation of the package and bond wires is desired. The equivalent circuit for a typical metal ceramic [6] is shown in Figure 7. Cpad1 and Cpad2 represent parasitic capacitances from the drain and gate lead frames. The Ccross capacitance arises from cross coupling of the lead frames. Lg and Ld are the total gate and drain bond wire inductances respectively. A mutual inductance exists between the gate and drain wires. A finite quality factor, Q, which represents the loss from the bond wires, is also associated with the gate and the drain wires. The package model must be combined with the active device model for a complete product model.

![Figure 7: Typical Package Equivalent Circuit](image-url)
2.2 Package Electrical Model Extraction

The electrical model of the NI\u215b250 package was extracted using methods devised by Tao Liang, et. al[7]. The method involves several steps. For the typical package equivalent circuit, the S-parameters of an empty package are first obtained to extract the parasitic capacitance values, \( C_{pad1}, C_{pad2}, \) and \( C_{cross} \) (Figure 8(a)). Then, the S-parameters of the package with gate and drain wires bonded to a metal pedestal are obtained. The metal pedestal acts as a dummy for the active device and is placed and shaped such that the bond wires have the same profiles as in a real packaged transistor. With the previously extracted parasitic capacitance values fixed, the bond wire inductances and finite Q’s representing the loss due to the wires are determined (Figure 8(b)).

![Figure 8: (a) Empty package equivalent circuit (b) Package, medal pedestal and bond wire equivalent circuit.](image)

For the NI\u215b250 package, full wave electromagnetic simulations were conducted in Ansoft HFSS™, a 3D, finite element based EM solver to generate the S-parameters of the empty package and the package with 12 gate wires and 13 drain wires bonded to a metal pedestal. Based on the phases of the resulting S-parameters and the equivalent circuit topology, Libra™ was used to optimize and extract the circuit element. The values are summarized in the table below.

<table>
<thead>
<tr>
<th></th>
<th>( C_{pad1} )</th>
<th>( C_{pad2} )</th>
<th>( C_{cross} )</th>
<th>( Q_{gate} )</th>
<th>( Q_{drain} )</th>
<th>( L_{gate} )</th>
<th>( L_{drain} )</th>
<th>Mutual L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2.22 pF</td>
<td>2.22 pF</td>
<td>( 8.0 \times 10^{-4} ) pF</td>
<td>20</td>
<td>20</td>
<td>0.38 nH</td>
<td>0.36 nH</td>
<td>0.04 nH</td>
</tr>
</tbody>
</table>

Table 1: Package and bond wire equivalent circuit values for MRF183.

To validate the simulation, S-parameter measurements of an empty package, a package with only gate wires bonded to a metal pedestal, and a package with only drain wires bonded to a metal pedestal were performed. Measurements were taken using a 50 Ohm test fixture and a HP8510C vector network analyzer. A 50 Ohm test fixture was designed and constructed to measure S-parameters of the DUT. The width of the microstrip line was fixed by the NI\u215b250 package lead width (215 mils) to avoid discontinuities and fringing effects between the leads and the microstrip line. The substrate thickness and the substrate dielectric constant were determined accordingly to obtain a microstrip line characteristic impedance of 50 Ohm. The fixture consists of removable endplates that allow for calibration standards to be inserted between them, a copper heatsink, a coaxial to microstrip transition, and pin pushers to assure good RF contact with the microstrip lines. The fixture is connected to the coaxial cables that are attached to the vector network analyzer or VNA (see Figure 9).
A two-tier calibration procedure was used prior to measurements. A commercially available, 7mm coaxial TRL (Thru-Reflect Line) calibration kit was used for the outer shell calibration to the ends of the coaxial cables of the VNA. The second tier calibration was based on a multi line TRL averaging calibration described in [8]. The TRL algorithm written by Engen, et. al. [9] was used to yield the individual error boxes of each of the fixture halves. With the error boxes for the input and output fixture halves, S-parameter measurement data obtained using the fixture can be de-embedded to ultimately obtain the DUT’s S-parameters (Figure 10).

A comparison of the simulated and measured phase of the S-parameters of the empty NIµ250 package, the package with gate wires and the package with drain wires is shown in Figure 11. The measured and simulated data are in good agreement up to a frequency of 5 GHz.
Figure 11(a): HFSS simulated vs. measured $S_{11}$ of empty NIμ250 package.

Figure 11(b): HFSS simulated vs. measured $S_{22}$ of empty NIμ250 package.
Figure 11(c): HFSS simulated vs. measured gate wires bonded in NIµ250 package.

Figure 11(d): HFSS simulated vs. measured drain wires bonded in NIµ250 package.
2.3 Summary

In this chapter, the Niμ250 package electrical model and extraction were presented for the MRF183. A simple equivalent circuit consisting of shunt capacitors for the lead frames and lossy inductors for the bond wires is used to model the electrical behavior of the package. Cross interactions are also accounted for with a coupling capacitor and mutual inductance.

Extraction of the package equivalent circuit parameters was done from the phase of simulated S-parameters. Simulated S-parameters were used for extraction instead of measurements because the measurements were too noisy at high frequencies due to coupling. At lower frequencies (less than 4GHz), EM simulations of the package and bond wires in HFSS well predicted the electrical behavior as verified by S-parameter measurements. The extracted shunt capacitances were both 2.22 pF while the gate and drain bond wire inductances were 0.38nH and 0.36 nH, respectively. Cross coupling was minimal but the gate and drain wires were quite lossy with a Q of 20.

With the package electrical model completed, the next chapter describes the isothermal electrical model and its extraction for the LDMOS FET.
Chapter 3

Isothermal Electrical Model and Extraction

This chapter begins by describing the large and small signal models that make up the isothermal electrical portion of Motorola’s LDMOS model. Both the large and small signal models are based upon MESFET equivalent circuit topologies [10] with modifications relevant for silicon LDMOS FETs. At the heart of the large signal model is the drain current equation that is similar to the well-known hyperbolic tangent function developed by Walter Curtice [10]. The drain current equation used in Motorola’s electro-thermal model accounts for the dependence of the threshold voltage, large-signal gain, and breakdown voltage on temperature. The small signal model is comprised of nonlinear capacitances that are dependent on voltages and temperature and conductances.

Once the equivalent circuit topologies of the large and small signal models have been presented, the chapter continues on to describe the methodology for extracting the parameters associated with both models and to present measurements used for the extraction of the MRF183 device model. The isothermal electrical model for the LDMOS FET is derived from pulsed DC and S-parameter measurements. The parasitic resistances and inductances must be determined prior to extracting the drain current model parameters from pulsed IV measurements at various temperatures. The parasitics must also be known to calculate the equivalent circuit parameters of the small signal model from pulsed S-parameter measurements at various temperatures. A program called WINFET was developed to aid the extraction of the small signal and large signal model parameters. The charges needed to complete the isothermal, large signal model are computed by integrating the capacitances extracted for the small signal model with respect to the voltages across the capacitances i.e. $C_y = \frac{\partial Q_y}{\partial V_{ij}}$. An illustration of the isothermal electrical modeling procedure from characterization to parameter extraction to modeling of the LDMOS FET is shown in Figure 12.
3.1 Isothermal Electrical Model

3.1.1 Large Signal Model

The large signal model excluding the thermal subcircuit is shown in Figure 13. The parasitics in the model include temperature dependent resistances $R_g$, $R_d$, and $R_s$. The charges between each of the terminals i.e. $Q_{ds}$, $Q_{gs}$, and $Q_{gd}$ are functions of the voltages across them and temperature.

The drain current is modeled using a single piece, continuously differentiable function applicable in the subthreshold, triode, breakdown, and saturation regions of operation. The complete model parameters and model equations are given in Appendix B and C.

Figure 12: Isothermal electrical modeling procedure. Modified from [10].

Figure 13: Large signal model of LDMOS FET.
The model includes gate voltage dependence on drain current saturation and subthreshold conduction. Transconductance and output conductance are obtained by differentiating the $I_d$ equation with respect to $V_{gs}$ and $V_{ds}$ respectively. Subthreshold conduction is modeled using the $V_{gst}$ equation. The addition of the subthreshold conduction is important to avoid a discontinuity in derivatives of the drain current expression at $V_{gs} = V_{TO}$. Both $VBR_{eff}$ and $VBR_{eff1}$ are used to model the drain and gate voltage dependency of the drain to source breakdown current. Drain saturation current is modeled using the hyperbolic tangent function and the $V_{gst2}$ gate voltage mapping equation. Only the parasitic resistances, the threshold voltage parameter $V_{TO}$, the current gain parameter $BETA$, and the breakdown parameter $VBR$ show temperature dependency.

$$I_d = (BETA)(V_{gst^{V_{GBP}}})(1 + \Lambda_{MBDA} * V_{ds})Tanh\left(\frac{V_{ds}*ALPHA}{V_{gst}}\right)\left(1 + K1*e^{V_{Reff}}\right)$$  \hspace{1cm} \text{Eqn. 9}

3.1.2 Small Signal Model

The small signal model (Figure 14) includes the parasitics and the intrinsic FET. The small signal output conductance is captured by $G_{ds}$. The small signal transconductance, $G_m$ is accounted for by the current source $I_1$ with carrier transit time in the channel, $\tau_1$. From the large signal model, the linearization of the charges $Q_{gs}$ and $Q_{gd}$ yields the capacitances $C_{gs}$ and $C_{gd}$ respectively while the linearization of $Q_{ds}$ yields the capacitance $C_{ds}$. $C_{ds}$ represents the junction capacitance from the drain to source. Its bias dependence is described by the well-known p-n junction depletion capacitance model. Hyperbolic trigonometric functions describe the capacitances from accumulation through inversion.

![Small signal model of LDMOS FET.](image)

3.2 Isothermal Electrical Model Extraction

3.2.1 Parasitic Extraction

S-parameter measurements for parasitic extraction were taken on-wafer and over the temperatures 25 °C, 75 °C, and 125 °C using Cascade Microtech’s Summit Thermal Probing System. A single tier LRM (Line-Reflect-Match) calibration to the probe tips was performed prior to measuring.
The method used for determining the parasitic resistances $R_g$, $R_d$, and $R_s$ was developed by D. Lovelace et. al [11]. For the cold FET S-parameter measurements, the gate voltage was constant at 0 V while the drain voltage was set to the DC operating voltage of 28 V. The frequency sweep started at 0.05 GHz and went up to 26.5 GHz in 0.25 GHz increments.

Measured S-parameters were converted to Z-parameters and from Z-parameters the parasitic resistances were extracted at $\omega=0$ using the following equations [11]:

\[
\begin{align*}
\text{Re}\{Z_{11}\}_{\omega=0} &= R_x + R_g \\
\text{Re}\{Z_{12}\}_{\omega=0} &= \text{Re}\{Z_{21}\}_{\omega=0} = R_s \\
\text{Re}\{Z_{22}\}_{\omega=0} &= R_s + R_d
\end{align*}
\]

Since the resistances were extracted from on-wafer measurements of a 0.72 mm, 8 finger device, they were scaled for the 120mm device. Both the drain and source resistances are inversely proportional to gate width. The gate resistance is proportional to $Z/N^2$ where $Z$ is the total gate width and $N$ is the number of fingers. With these relations, the parasitic resistances for the 120mm devices could be calculated from the extracted parasitic resistances of the 0.72 mm device.

\[
\begin{align*}
R_{i,120mm} &= R_{i,0.72mm} \times \frac{0.72\text{mm}}{120\text{mm}} \text{ where } i=d,s \\
R_{g,120mm} &= \frac{120\text{mm}}{(56\text{ fingers} \times 24\text{cells})^2} \times \frac{(8\text{ fingers} \times 1\text{cell})^2}{0.72\text{mm}} \times R_{g,0.72mm}
\end{align*}
\]

The linear dependence of parasitic resistances on temperature is shown in Figure 15.

![Parasitic Resistances vs. Temperature](image)

Figure 15: Parasitic resistances vs. temperature.
For the LDMOS, the parasitic inductances at the gate, drain, and source are on the order of pico-Henrys. Theoretically, parasitic inductances can be extracted from the imaginary parts of the Z-parameters at high frequencies. However, since the devices are measured in a 50Ω system, the extracted inductance values are not reliable even at the maximum allowable frequency by the S-parameter test set (26.5 GHz). Thus, the parasitic inductances are not extracted but are fitting parameters in the model.

\[
\text{Im}\{Z_{11}\}_{\omega=0} = j \omega (L_g + L_s) \\
\text{Im}\{Z_{12}\}_{\omega=0} = \text{Im}\{Z_{21}\}_{\omega=0} = j \omega L_s \\
\text{Im}\{Z_{22}\}_{\omega=0} = j \omega (L_s + L_d)
\]

**Eqn. 12(a)**

**Eqn. 12(b)**

**Eqn. 12(c)**

### 3.2.2 Pulsed Measuring System

Pulsed DC and S-parameter measurements for the MRF183 transistor were conducted using HP's 85122A E20 Measurement System[12]. The setup of the measuring system is shown in Figure 16.

![HP 85122A E20 Pulsed Measuring System](image)

**Figure 16: Measurement setup for pulsed I-V and S-parameter measurements**

The pulsed modeling system consists of a DC and a RF subsystem. The DC subsystem allows IV measurements under pulsed conditions and the bias to be pulsed during RF measurements. Four power supplies (HP 6629A) providing a maximum pulsed and quiescent voltage range of ±100 V drive two pulsers (HP 85120 A). The pulsers are
capable of supplying voltages with a 200 nsec. minimum pulse width and a maximum duty cycle of 4% at the maximum pulsed current limit of 10A. The user can set a quiescent bias point and pulse bias voltages either higher or lower than the quiescent. The pulse generators (HP8110 A) synchronize the pulses, set the desire pulse width and period, and triggers for the DC and RF sampling location. The measurements are taken using four digital multi-meters (HP 3458A not shown in figure) that can be triggered to measure voltages and currents over any 2 nsec. aperture on the waveform.

The RF subsystem includes a vector network analyzer, two test sets, and two synthesized sources, one of which provides the RF stimulus to the DUT. The HP 85110A test can operate in either constant or pulsed modes from 500 MHz to 20 GHz while the HP 8515A only operates in constant mode from 45 MHz to 26.5 GHz. Bias networks that couple the RF and bias output pulsed bias DC and pulsed RF to the DUT from 400 MHz to 26.5 GHz. Both subsystems are controlled by computer with HP’s IC-CAP Modeling Software.

Short pulse widths and low duty cycles are needed to prevent self-heating of the devices. For the pulsed measurements, the pulse period was set to 1.0 msec. The pulse width of the gate voltage was 2.0 µsec. while the pulse width of the drain voltage was 2.4 µsec. The drain voltage had no pulse delay but the gate voltage had a pulse delay of 500 nsec in order to follow zero current path. To take current and voltage measurements, the multimeters were triggered 1.2 µsec into the bias pulses. An oscilloscope that is missing from the above figure monitors the voltage waveforms with respect to time.

![Figure 17: Timing of the pulsed IV and S-parameters measurements.](image)

By controlling the surrounding temperature of the device during the pulsed measurements, the junction temperature is assumed to be the same as the surrounding temperature. Temptronic’s TP04100A Thermostream System, which outputs air from –20 °C to 225 °C, was used to control the temperature of the device.
3.2.3 DC Model Parameter Extraction

Pulsed IV Measurements
DC measurements of the packaged devices were conducted at three temperatures: 25°, 75°, 125° C. The 50 Ohm test fixture built for the S-parameter measurements was used to hold and provide bias via microstrip lines to the packaged device. The fixture’s end connectors were adjoined to the pulsed system’s bias networks that prevented the device from oscillating. The RF inputs to the bias networks of the pulsed system were terminated with 50 Ohm loads for the DC measurements. The DC measurements consisted of a subthreshold, a forward breakdown, a reverse I-V, a forward I-V, and Id vs. Vgs measurement. The results of the forward I-V measurements (and simulations) for a 5mm device are shown in the Figure 18.

Drain Current Model Parameter Extraction
A Microsoft Window’s program called WINFET was developed to extract the drain source current model parameters. WINFET avoids local minima during each optimization for the ID model parameters at each temperature by globally optimizing in three dimension i.e. Vds, Vgs, and temperature. To properly account for the voltage drop across the parasitic resistances, a generalized non-linear DC solver was implemented in WINFET. By doing such, the intrinsic voltages are calculated and the ID model parameters are extracted using the intrinsic voltages.

---

Figure 18: Pulsed forward I-V measurements and simulations for a 120mm device.
**3.2.4 Small Signal Model Parameters**

**Pulsed S-parameter Measurements**

S-parameter measurements were also taken pulsed over the temperatures 25 °C, 75 °C, and 125 °C using the HP 85122A E20 Measurement System to obtain the intrinsic FET equivalent circuit parameters and their temperature dependencies. S-parameter measurements were attempted from packaged devices but even after de-embedding the fixture halves and the package S-parameters, resonances due to package and bond wire interactions appeared at high frequencies. Thus, the S-parameter measurements were taken on the wafer from which the packaged devices were obtained using the Summit Thermal Probing System. Again, a single tier LRM calibration was performed to the end probes. The only devices on the wafer that could be probed were 8 finger devices that are $1/7^{\text{th}}$ the size of a single cell (5mm gate width, 56 fingers) device.

Three sets of S-parameter measurements with varying bias conditions were taken to extract the capacitances of the small signal model. For extraction of $C_{ds}$ and $C_{gd}$, S-parameter measurements were performed with the gate voltage held constant at 5 V while the drain voltage was swept from 0 to 40 V. For the extraction of $C_{gs}$, the drain voltage was constant at 28 V while the gate voltage was swept from -3 V to 8 V. Lastly, a set of S-parameter measurements were carried out while sweeping both voltages in coarse steps. The frequency sweep on all S-parameter measurements was from 0.5 GHz to 20 GHz in 0.25 GHz steps. The following graphs show a set of pulsed S-parameter measurements used for extraction of $C_{gs}$. The gate and drain voltages are 5 V and 28 V, respectively.

![Figure 19(a): Pulsed $S_{11}$ measurements over temperature.](image)
Figure 19(b): Pulsed $S_{12}$ measurements over temperature.

Figure 19(c): Pulsed $S_{21}$ measurements over temperature.
Small Signal Equivalent Circuit Parameter Extraction

From these S-parameter measurements and with the extracted parasitic, the equivalent circuit parameters or ECP’s for the small signal model can be determined as described by Anholt [5]. First, the measured S-parameters have to be transformed into Z-parameters to de-embed the parasitics. Once, the parasitics are de-embedded, the Z-parameters are transformed into Y-parameters. The exact analytical form of the intrinsic Y-parameters is derived from the equivalent circuit shown in Figure 20. From these four equations, the ECP’s are extracted.

![Small Signal Equivalent Circuit Parameter Extraction](image)

**Figure 19(d):** Pulsed S\textsubscript{22} measurements over temperature.

**Figure 20: Intrinsic FET extraction for small signal model.**
\[ Y_{11} = \frac{\omega^2 R_{gs} C_{gs}^2}{1 + (\omega C_{gs} R_{gs})^2} + \frac{\omega^2 R_{gd} C_{gd}^2}{1 + (\omega C_{gd} R_{gd})^2} + j\omega \left( \frac{C_{gs}}{1 + (\omega C_{gs} R_{gs})^2} + \frac{C_{gd}}{1 + (\omega C_{gd} R_{gd})^2} \right) \]

Eqn. 13(a)

\[ Y_{12} = \frac{\omega^2 R_{gd} C_{gd}^2}{1 + (\omega C_{gd} R_{gd})^2} - j\omega \left( \frac{C_{gd}}{1 + (\omega C_{gd} R_{gd})^2} \right) \]

Eqn. 13(b)

\[ Y_{21} = \frac{g_m \exp(-j\omega \tau)}{1 + j\omega R_{gs} C_{gs}} - \frac{\omega^2 R_{gd} C_{gd}^2}{1 + (\omega C_{gd} R_{gd})^2} - j\omega \left( \frac{C_{gd}}{1 + (\omega C_{gd} R_{gd})^2} \right) \]

Eqn. 13(c)

\[ Y_{22} = \frac{1}{R_{ds}} + \frac{\omega^2 R_{gd} C_{gd}^2}{1 + (\omega C_{gd} R_{gd})^2} + j\omega \left( \frac{C_{gd}}{1 + (\omega C_{gd} R_{gd})^2} + C_{ds} \right) \]

Eqn. 13(d)

The gate to drain capacitance is first determined from the slope of \( \text{Im}[Y_{12}] \) for low frequencies assuming \((\omega C_{gd} R_{gd})^2 \ll 1\). The drain to source capacitance \( C_{ds} \) can then be computed as the difference between the slope of \( \text{Im}[Y_{22}] \) at low frequencies and the extracted \( C_{gd} \). Likewise, the gate-source capacitance is the difference between the slope of \( \text{Im}[Y_{11}] \) at low frequencies and the extracted \( C_{gd} \).

\[ C_{gd} = \frac{\text{Im}[Y_{12}]}{\omega} \]

Eqn. 14(a)

\[ C_{ds} = \frac{\text{Im}[Y_{22}]}{\omega} - C_{gd} \]

Eqn. 14(b)

\[ C_{gs} = \frac{\text{Im}[Y_{11}]}{\omega} - C_{gd} \]

Eqn. 14(c)

Using the above methodology, Motorola’s WINFET program automatically extracts the LDMOS FET Model ECP’s from the measured sets of small-signal 2-port S-parameters. WINFET extracts equivalent circuit model parameters versus bias and temperature for the FET topology and optimizes the ECP’s to fit over all frequencies. It outputs the optimized ECP’s for post processing to determine and fit \( C_{ds}, C_{gd}, \) and \( C_{gs} \) expressions. Since the S-parameters were measured on-wafer using 8 finger devices, 0.72mm device, the extracted ECP’s had to be scaled for the 120mm device. Figure 21 compares the modeled versus measured capacitances \( C_{ds}, C_{gd}, \) and \( C_{gs} \) for the 8 finger, 0.72mm device.

Ultimately, the extracted intrinsic capacitances \( (C_{ds}, C_{gs}, \text{and } C_{gd}) \) are integrated with respect to the voltages across them i.e. \( V_{ds}, V_{gs} \) and \( V_{gd} \), respectively, to calculate the charges \( Q_{ds}, Q_{gs}, \) and \( Q_{gd} \) as functions of bias and temperature to complete the isothermal, large signal model.
Figures 21(a): Measured vs. modeled Cds.

Figures 21(b): Measured vs. modeled Cgd.
3.3 Summary

In this chapter, the isothermal electrical model composed of the large and small signal models were presented. Both models are similar to typical MESFET models with the addition of a conductance in series with the gate to drain capacitance/charge. With the exception of the parasitic resistances and inductances, the model parameters associated with both models were extracted as functions of voltages and temperature from pulsed I-V and S-parameter measurements at various temperatures. WINFET, a Windows software developed by Motorola, aided in the extraction of the model parameters of the drain current equation and the small signal ECPs. Graphs of modeled vs. measured drain current and small signal capacitances at various temperatures were included in this chapter to show the accuracy of the models in predicting isothermal electrical performance at several temperature.

This chapter concludes the electrical portion of the LDMOS Electro-Thermal model and the remaining chapters address the thermal portion of the electro-thermal model. We begin by looking at the simplest thermal model consisting of a single thermal resistance in shunt with a thermal capacitance. Techniques commonly used in industry today to extract a single thermal resistance and capacitance are applied to the MRF183 transistor to develop a single RC thermal model.
Chapter 4

Single RC Thermal Model and Extraction

This chapter discusses various techniques for determining the thermal resistance and capacitance of a single RC thermal model and presents the results from applying these methods to the MRF183 device. The thermal resistance is first predicted from simulations in a Motorola proprietary program called DieTemp and a finite element analysis program called ANSYS. DieTemp is a C program that approximates the infinite series solution of the 3D heat conduction problem in steady state with a finite series. ANSYS, on the other hand, is a commercially available finite element analysis package capable of accounting for convection and conduction at the expense of computation time. The thermal resistance is directly calculated by measuring the average temperature of an operating MRF183 device by means of IR scans. The thermal capacitance is determined by applying a step DC bias to the device and monitoring the change in drain current with respect to time. The time the drain current takes to reach a constant, steady-state value is the thermal time constant. With the thermal resistance from our IR scans, the thermal capacitance is subsequently computed from the thermal time constant.

4.1 Thermal Resistance

4.1.1 DieTemp Simulations

DieTemp is a program based on a paper by Lindsted and Surty[13] in which the three dimensional, steady-state, heat conduction problem in a semiconductor is solved by obtaining an exact solution in terms of infinite series (see Appendix D). In the program, the infinite series solution is approximated by a finite series with the number of terms specified by the user. In addition, the following approximations are made on the boundary conditions:

1) A uniform heat flux Q over a heat generating source surface area represents the power dissipated.
2) The dimensions of the heat generating source area are defined as the channel length and the tub width for a single cell.
3) The heat spreads at a 45 degree angle from the top layer to the bottom layer.
4) An infinite heat sink is attached to the bottom of the package case such that temperature case, T_{case} is fixed.
5) No heat is lost to ambient by convection.
6) Each cell in a multiple cell transistor is assumed to thermally behave the same.
The inputs to the DieTemp program include the material properties, the dimensions of each layer and the heat generating source, the power dissipated, and the fixed case temperature. The program solves the heat conduction problem for the temperatures at the top and bottom surface of each layer. The temperature for each surface is averaged by integrating the temperature over the area and then dividing by the surface area (Eqn. 16). By calculating the average temperature change for each layer and with the power dissipated, DieTemp determines the thermal resistance of each layer using Eqn. 17. The overall thermal resistance is obtained by summing the thermal resistances of all layers.

\[
\text{Eqn. 16} \quad T_{\text{ave}} = \frac{\int \int T \, dx \, dy}{A \times B} \quad \text{for a surface with dimensions } A \times B
\]

\[
\text{Eqn. 17} \quad R_{\text{th,layer}} = \frac{T_{\text{ave, top}} - T_{\text{ave, bottom}}}{P_{\text{dis}}} \quad \text{thermal resistance of a layer}
\]

\[
\text{Eqn. 18} \quad R_{\text{th, total}} = \sum_{i=1}^{N} R_{\text{th, layer}(i)} \quad \text{where } N = \text{number of layers}
\]

For the simulation of the MRF183 transistor, only the silicon die and copper tungsten flange served as the input layers to DieTemp. Because the die bond is less than 0.5 mils thick, the die bond layer was omitted. The T$_{\text{case}}$ was anchored to 75 °C and the simulated power dissipation was 45 Watts. The resulting temperature profile at the top of the silicon die surface is shown in Figure 23. The average temperature of the top surface was 135.59 °C. The total thermal resistance of the entire structure from the top silicon die surface to the bottom case surface was 1.35 °C/Watt.
4.1.2 ANSYS Simulations

More rigorous thermal simulations to calculate temperature distribution were conducted in ANSYS. ANSYS uses the heat balance equation as the basis of thermal analysis and accounts for conduction and convection. The structure of the transistor and package is defined as finite elements with nodes. For each node, the temperature is computed with the following boundary conditions:

1) The power dissipated is simulated as a heat flux, $Q$, uniformly distributed over the die.

2) A convection boundary condition at the bottom of the package flange exists such that the base temperature of the case is constant.

Due to memory limitations, only the temperatures at the nodes on the top silicon surface are saved to a file from the simulation. Only the overall thermal resistance of the structure could be calculated by dividing the difference in temperatures of the top silicon surface and the case by the power dissipated (Eqn. 19).

$$R_{th, total} = \frac{T_{ave,top} - T_{case}}{P_{diss}}$$  \hspace{1cm} \text{Eqn. 19}

The silicon, die bond, and package layers were all simulated with the $T_{case}$ fixed at 75 °C and a power dissipation of 45 Watts. Exploiting the symmetry properties of the MRF183 transistor, only ¼ of the device was simulated to reduce computing time. The average temperature on the top surface of the die from the ANSYS simulation was 127.2 °C (calculated using Eqn. 16) and the overall thermal resistance was thus 1.16 °C/Watt.
4.1.3 CompuTherm Measurements

An Infrared Radiation (IR) Microscope based technique was used to directly determine junction temperature and thermal resistance. The instrument used was the CompuTherm III manufactured by Quantum Focus formerly known as Barnes Engineering Division/EDO. Based on a calculated or a fixed emissivity the instrument converts the radiation detected by a liquid nitrogen cooled Indium Antimonide type into temperature.

For the IR measurements, the DUTs without the package caps were uniformly coated with a high emissivity black hobby paint. Since the part was painted black a fixed emissivity of 0.95 was inputted rather than calculated by the IR instrument. The fixture with the passive components on the substrate was used to hold the DUT and apply DC bias to the DUT. With the transistor powered to approximately 45 Watts, the chuck temperature was adjusted to get a case temperature of 75 °C in thermal steady state. A thermocouple wire embedded in the fixture beneath the package monitored the case temperature. With T_{case} at 75 °C, an IR scan was taken of the DUT.
An IR scan of one of the three devices tested is shown in Figure 25.

![IR scan of a MRF183 device](image)

Figure 25: IR scan of a MRF183 device.

The average temperatures of the die surface for all three devices were calculated using the software of the CompuTherm and the thermal resistances were subsequently calculated. The measurement results are summarized in the table below.

<table>
<thead>
<tr>
<th>Device</th>
<th>$T_{\text{case}}$</th>
<th>$T_{\text{ave}}$</th>
<th>$P_{\text{diss}}$</th>
<th>$R_{\text{th}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT #1</td>
<td>75 $^\circ$C</td>
<td>147.4$^\circ$C</td>
<td>44.8 W</td>
<td>1.62$^\circ$C/W</td>
</tr>
<tr>
<td>DUT #2</td>
<td>75 $^\circ$C</td>
<td>146.6$^\circ$C</td>
<td>44.2 W</td>
<td>1.62$^\circ$C/W</td>
</tr>
<tr>
<td>DUT #3</td>
<td>75 $^\circ$C</td>
<td>146.6$^\circ$C</td>
<td>44.2 W</td>
<td>1.62$^\circ$C/W</td>
</tr>
</tbody>
</table>

Table 2: Summary of IR scan results for three devices

### 4.1.4 Comparison of Simulations and IR Scans

Although both simulation programs gave similar maximum temperatures (within 5 $^\circ$C), the average temperature and thermal resistance calculated from ANSYS was much lower. This is because DieTemp assumes that each cell of the multi-cell MRF183 transistor behaves the same thermally. ANSYS, on the other hand, accounts for the temperature gradient along the length of the die. In ANSYS, the cells at the edges of the die have lower temperatures than the center cells since there are no neighboring cells at the edges to add more heat and obstruct heat dissipation. The graph below (Figure 26) compares the junction temperature profiles along the center length of the die (along the y-axis with $x = 0$) from both simulations.
Figure 26: DieTemp vs. ANSYS.

Both simulation tools exhibited large errors in comparison to the thermal resistance values obtained from the IR scans. The table below summarizes the thermal resistance values determined from the various methods and calculates the error between the simulations and the results of the IR scans.

<table>
<thead>
<tr>
<th>Method</th>
<th>Rth</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>IR Scans</td>
<td>1.62 °C/W</td>
<td>-</td>
</tr>
<tr>
<td>DieTemp</td>
<td>1.35 °C/W</td>
<td>16.7 %</td>
</tr>
<tr>
<td>ANSYS</td>
<td>1.16 °C/W</td>
<td>28.4 %</td>
</tr>
</tbody>
</table>

Table 3: Summary of thermal resistances extracted from various methods.

The simulations are susceptible to errors because material properties that serve as inputs are difficult to define. For example, the thermal conductivity of copper tungsten given by the package vendor ranged from 1.4-2.0 W/(cm·°C). In addition, both simulation tools are based on assumptions that may not necessarily be valid. Because such inaccuracies impact the temperature calculations significantly, the simulation tools are not precise indicators of junction temperatures and thermal resistances.
4.2 Thermal Capacitance Extraction

The thermal capacitance was extracted by electrical measurements. Applying step input voltages to forward bias the FET results in an exponential change in the output drain current due to self-heating. The time constant of the exponential rise or decay function describing the output current behavior of the device is the thermal time constant of the device and can be used to calculate the thermal capacitance using Equation 7 if the thermal resistance is known.

Whether the output current exhibits an exponential rise or decay with time is dependent on the biasing condition. To the first order, Equation 2 describes the drain current in saturation where the mobility and threshold voltage are temperature dependent. For small values of gate voltages and correspondingly small currents, the threshold voltage term dominates and the decrease in threshold voltage with increasing temperature results in a positive temperature coefficient for saturation current i.e. the saturation current increases with temperature. For large gate voltages, the negative temperature coefficient of the mobility term dominates, and the saturation current decreases with temperature. For the special case dubbed the zero-temperature coefficient bias condition, the saturation current does not change with temperature as shown in Figure 27.

![Zero Temperature Coefficient Bias](image)

Figure 27: $I_d$ vs. $V_{gs}$ for zero temperature coefficient bias condition.

For the measurement of the MRF183, the device was biased below the zero-temperature coefficient, $V_{gs} < 6.015\, V$, and thus, the exponential rise in drain current due to self-heating was captured. The drain voltage was set at 28 V and a step voltage of 5 V was applied to the gate. The drain current in our setup (Figure 28) was measured as a voltage across a sampling resistor at the drain.
Attempts were made to fit an exponential equation with a single time constant to the measured voltage across the sampling resistor versus time data but the fits were poor. Instead, a simple exponential function with two time constants was used to fit the data. The longer time constant of the two is associated with the fixture and is disregarded. The shorter time constant is representative of the transient thermal behavior of the packaged device and is the desired thermal time constant. For the two measured devices, the relevant thermal time constants were relatively close at 0.234 seconds and 0.220 seconds. Plugging in the thermal resistance of 1.62 °C/Watt determined from the IR scans and the thermal time constants from the transient measurements \( \tau = 0.235 \text{ sec.} \) and \( \tau = 0.220 \text{ sec.} \) into Equation 7, the thermal capacitances are computed to be 0.144 J/°C and 0.136 J/°C, respectively. The fitted exponential function with the extracted thermal time constants and the measured voltage across the sampling resistor versus time of a MRF183 device are graphed in Figure 29.

Figure 29: Measured data vs. fitted exponential for thermal time constant extraction.
4.3 Summary

Several methods were implemented for extracting the thermal resistance and thermal capacitance for the single RC thermal model in this section. Simulations in ANSYS and DieTemp were first conducted to predict the thermal resistance. Both simulations tools gave thermal resistance values far below the result of the IR scans which was 1.62 °C/Watt. Surprisingly, the more rigorous software, ANSYS, exhibited a larger error of 28.4% compared to DieTemp’s error of 16.7 %. The source of error in both simulations most likely lies in our inability to accurately determine material properties such as thermal conductivity of CuW in conjunction with the far-reaching assumptions the simulations are based upon. Due to the complexity of thermal transient simulations, no simulations were performed for extracting thermal capacitance. Instead, the thermal capacitance was determined by performing thermal transient measurements only. Measurements of two devices resulted in thermal time constants of $\tau = 0.235$ sec. and $\tau = 0.220$ sec. With the thermal resistance extracted from IR scans, the thermal capacitances for the two measured MRF183 devices were calculated to be 0.144 J/°C and 0.136 J/°C, respectively.
Chapter 5

Multiple RC Thermal Model and Extraction

An electrical measurement for thermally characterizing packaged devices is desired to eliminate the need for cumbersome and time-consuming IR scans. The most common electrical technique presently used in industry exploits the strong diode current-voltage dependence on temperature to determining device or chip junction temperature. Diodes are specifically added to some chips for the sole purpose of sensing temperatures but often intrinsic diodes in devices can be utilized. For instance, the gate diode and Schottky diode inherent to IGBTs and GaAs MESFETs, respectively, are used as temperature sensitive parameters (TSP). This chapter demonstrates a similar method for LDMOS devices. The substrate/source-to-drain diode innate to LDMOS FETs acted as the TSP for thermal transient measurements in this research.

An oven calibration must first be performed on devices to determine the relationship between diode voltage and temperature for a constant diode current. After calibration, the devices are powered under normal operating conditions. Once thermal steady state is reached, the power is turned off and the constant diode current is injected. As the device cools, the diode voltage or temperature is monitored with respect to time. The resulting cooling curves for three MRF183 devices are presented in this chapter. They exhibit multiple time constants that are pronounced. Instead of using the single thermal resistance and capacitance model of the previous chapter, the curves are fit to a ladder network with multiple shunt thermal resistances and capacitances. The chapter ends with a discussion and comparison of the non-grounded capacitance and grounded capacitance RC network for modeling the dynamic and static thermal behavior of LDMOS devices.

5.1 Background

The general method for thermal transient measurements requires a diode calibration procedure in an oven. By varying the temperature of the oven and applying a small constant diode current to the unpowered device, the relation between the diode voltage and the temperature can be determined. The diode current must be insignificantly small to avoid self-heating. Once calibrated, the device is powered under normal operating conditions. In order to obtain the junction temperature at a certain instance, the device has to be turned off, the small diode current must be applied, and the diode voltage measured before the device cools off significantly. Because the devices have to be switched on for heating and off for measuring or sampling temperature, a thermal transient measurement using the cooling curve method is more convenient than the heating curve method.
As implied by its name, the heating curve method captures the heating of the DUT as a positive power step is applied. For the cooling curve method, the response of the DUT is a thermal decay due to a negative power step input. The heating curve method and cooling curve method are assumed to be symmetric. However, the heating curve method is much more difficult to implement in hardware and software because it requires a continuous switching of the device from heating to sampling with a low duty cycle. On the other hand, the cooling curve method only requires a single switch to the sampling mode from heating mode once the DUT has reached thermal steady state. The cooling curve method was used for the thermal transient measurements of LDMOS devices for the sake of implementation ease.

5.2 Measurement Setup

5.2.1 Configuration of Transient Measurement System

Roger Stout, RW Lawson, and David Billings of Motorola’s SCG Thermal Lab developed the hardware and software system used for the thermal transient measurements of the LDMOS devices. A diagram of their setup is shown in Figure 30.

Figure 30: SCG Thermal Lab's thermal transient measurement system.

A Macintosh Quadra computer houses the Data Acquisition (DAQ) board and drives the system using a LabView software program. The multi-channel switch box applies power to the DUT when in the heating mode and injects only minimal bias current to the diode in sampling/measuring mode. The clock switch logic box switches between two different sample clocks and generates a third clock pulse that interfaces to the multi-channel switch box.

With the clock switch logic box and the internal computer clock, the transient thermal setup is able to take data for the cooling curve at three different rates. In the first few milliseconds where the temperature is changing the quickest, a high speed burst of data is taken with the DAQ board. After the initial burst, the DAQ board is triggered at a medium clock rate. The clock for the initial high speed burst runs at 25 KHz while the
medium speed clock ticks with a frequency of 25 Hz. After a couple seconds of data has been acquired with the intermediate clock, the internal computer clock provides enough resolution to take single scans.

There is a third clock within the clock switch logic box that provides a single pulse for synchronization of the system. On the rising edge of the pulse, (1) the multi-channel transient switch box forces the DUT into sampling mode from heating mode, and (2) gates the high speed clock to the DAQ board for measurement. On the falling edge of the pulse, the medium speed clock instead of the high speed clock is gated to the DAQ board for measurement. The interaction of the three clocks is shown in the figure below. The highlighted portions of the clocks are gated to the DAQ board. (Note: Figure not drawn to scale.)

![Timing and Synchronization for Data Acquisition](image)

**Figure 31: Timing and synchronization for data acquisition.**

### 5.2.2 Oven Calibration and Transient Measurement Setup

The connections for the oven calibration of the MRF183 substrate/source-to-drain diode are shown in Figure 32. The gate and source are shorted to each other to pin $V_{gs}= 0 \text{ V}$. A 10 kOhm resistor is connected in series with the diode and a voltage of 10.7 V is applied across the series to force 1 mA diode current. The diode voltage was measured with the oven at 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C. Because the fixture for the MRF183 was built from copper, it took approximately 20 minutes for the package or case temperature to reach thermal equilibrium with the oven at each temperature. A thermocouple wire embedded between the fixture and the package monitored the case temperature.

![Oven Calibration Connections for MRF183](image)

**Figure 32: Oven calibration connections for MRF183.**

A diagram of the connections for the MRF183 device to SCG’s thermal transient measurement system is shown in Figure 33. In the heating mode, the switch box shorts the channels from the drain and gate power supplies to the DUT and opens the channels.
from the sampling supply to the diode. As in our simulations and IR scans, the drain power supply was set to the operating voltage of 28 V while the gate voltage was approximately 5 V to produce 1.6 Amps of drain current and 45 watts of power. A cold chuck underneath the copper fixture with the powered MRF183 had a fixed temperature of about 24 °C to get a case temperature of about 75 °C in thermal steady state. In the sampling mode, the heating channels to the power supplies are opened while the sampling supply switches are shorted to force current through the diode as in the oven calibration.

![Diagram](image)

Figure 33: Thermal transient setup for MRF183.

5.3 Measurement Results

The graph below (Figure 34(a)) shows the oven calibration results of the three measured MRF183 devices. The forward current density $J$ of the diode can be approximated by Eqn. 20,

$$J = qA^2\left[\frac{D_n}{N_aL_n} + \frac{D_p}{N_dL_p}\right]T^3 \exp\left(-\frac{E_g}{kT}\right)\exp\left(\frac{qV}{nkT}\right)$$  \hspace{1cm} \text{Eqn. 20}

where $E_g$ is the bandgap energy, $D_{n,p}$ are the diffusion constants for electrons and holes. $N_a$ and $N_d$ represent the acceptor and donor concentrations, and $L_p$ and $L_n$ are the diffusion lengths of the p-side and n-side, respectively. Solving for $V$ in terms of temperature and current density, the above equation can be rewritten as:

$$V = qnE_g - \frac{nKT}{q} \left[3\ln T - \ln \left(\frac{J}{C}\right)\right]$$  \hspace{1cm} \text{Eqn. 21}

with $C = A^2\left[\frac{D_n}{N_aL_n} + \frac{D_p}{N_dL_p}\right]$. Though $n$, $E_g$, and $C$ may vary slightly with temperature, the diode voltage is expected to decrease linearly with increasing temperature for reasonable values of current. This relation is visible in the calibration results of the
MRF183. Although there is very little variation from device to device, each set of data was fit to a line to obtain device-specific equations relating diode voltage and junction temperature.

![Graph of diode voltage vs. junction temperature](image)

**Figure 34(a):** Diode voltage vs. junction temperature obtained from oven calibration.

The graphs of diode voltage versus time and junction temperature versus time are shown in graphs below (Figure 34(b) and (c) respectively).

![Graph of diode voltage vs. time](image)

**Figure 34(b):** Diode voltage vs. time curves for 3 measured MRF183 devices.
The first data point in the transient measurement is 6 milliseconds into the cooling curve. The long delay in obtaining the first valid measurement is due to the bias networks at the drain and gate that are needed to suppress oscillations. The bias networks contain capacitors and ferrite beads or inductors that require time to discharge once the device has been switched from forward bias in the heating mode to reverse bias in the sampling mode. Without any data within the first 6 milliseconds of the cooling period, the thermal RC network behavior of the silicon die and the die attach is most likely absent from the measurement. However, the cooling of the package and other layers (the copper fixture and isolation sheet) is captured.

5.4 RC Network Extraction

5.4.1 Non-grounded Capacitor RC Network

A six rung RC ladder network shown in Figure 36 was used to model the transient thermal behavior of the MRF183 devices.
Mathematical equation describing the step cooling junction temperature response of the above network is:

\[ T_j = T_{\text{fixed}} + \sum_{i=1}^{6} R_i e^{-\frac{i}{\tau_i}} \]  

Eqn. 22

The R_i’s and C_i’s for the equation were optimized in an Excel spreadsheet such that the difference in the calculated junction temperature and the measured junction temperature was minimized for all time. The extracted R_i’s and C_i’s are listed in Table 4 and a graphical comparison of the measured and calculated T_j versus time for one of the tested devices is shown in Figure 37. The Root Mean Square Error (RMSE) between measured and calculated T_j was less than 0.2.

Table 4: Extracted R’s and C’s for non-grounded capacitor network.
Since there was no measured data in the first 4-5 milliseconds of the cooling curve, the steady state junction temperature which is approximated to be at time $t = 0^+$ sec. is not captured. However, the steady-state junction temperature can be estimated by assuming that the dominating thermal impedance is from the package and extending the extracted RC rung describing the package to time $t = 0^+$ sec. Using such an assumption, the steady-state junction temperatures of the three measured devices were obtained and the thermal resistances subsequently calculated as summarized in Table 5.

<table>
<thead>
<tr>
<th>Device</th>
<th>$T_j$ at $t = 0^+$ sec.</th>
<th>$R_{th}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>140.51°C</td>
<td>1.50 °C/W</td>
</tr>
<tr>
<td>#4</td>
<td>150.00 °C</td>
<td>1.71 °C/W</td>
</tr>
<tr>
<td>#11</td>
<td>145.53 °C</td>
<td>1.64 °C/W</td>
</tr>
</tbody>
</table>

Table 5: Extracted $T_j$ and $R_{th}$ from Thermal Transient Measurements

With the extracted overall thermal resistances of the packaged devices in Table 4, the rungs of the non-grounded capacitor RC network that describe only the packaged device and not the other undesired layers (i.e. fixture and isolation sheet) can be identified. If the extracted thermal resistances of the top three rungs closest to the junction, $R_1$, $R_2$, and $R_3$ in Table 4, are totaled, the sum is close to the extracted total thermal resistance. Thus, the $R$'s, $C$'s, and tau's associated with the top three rungs must represent the packaged device’s thermal transient behavior while the lower three rungs describe the thermal transient behavior of the extraneous layers. Comparing the longest thermal time constant correlated with the packaged devices, i.e. the Tau3’s in Table 6 (0.236 sec., 0.334 sec., and 0.262 sec.) to those obtained in the thermal capacitance measurements discussed in Section 4-2 (0.233 sec., and 0.220 sec.), the results are similar.
5.4.2 Grounded Capacitor RC Network

The non-grounded capacitor thermal network shown in Figure 36 is commonly misused to represent a physical, thermal system. As argued by Roger Stout, et. al[14], a more accurate network description of the fundamental heat flow equation is a grounded capacitor RC circuit shown in Figure 38.

![Grounded Capacitor RC Network](image)

Figure 38: Grounded Capacitor RC Network

The thermal capacitance of a real thermal system relates the change in temperature at each position with respect to time. The non-grounded network by adjoining neighboring capacitances instead of to ground is relating the change in temperature at each position with respect to temperatures at adjoining elements in the system. The individual R’s and C’s in a non-grounded network cannot be correlated to the physical device although the network is mathematically convenient.

The best approach to solving a grounded capacitor RC network like the three-rung circuit shown in Figure 39 is using Laplace Transforms.

![Node and element definition of 3-rung grounded capacitor RC Network](image)

Figure 39: Node and element definition of 3-rung grounded capacitor RC Network

By treating the power dissipated as a step current and the temperatures at each node as voltages, Kirchoff’s Current Law can be used to obtain three equations, one at each of the nodes.

At node 1:

\[
\frac{V_1 - V_2}{R_1} + C_1 \frac{dV_1}{dt} = I_{\text{therm}} u(t) \\
\text{Eqn. 23(a)}
\]

At node 2:

\[
\frac{V_2 - V_3}{R_2} + C_2 \frac{dV_2}{dt} = \frac{V_1 - V_2}{R_1} \\
\text{Eqn. 23(b)}
\]
At node 3:

\[
\frac{V_3 - V_{\text{fixed}}}{R_3} + C_3 \frac{dV_3}{dt} = \frac{V_2 - V_3}{R_2}
\]

Eqn. 23(c)

Taking the Laplace transform of the equations above only modifies the capacitance terms and the step current term with the following transformations:

\[
L\{C_i \frac{dV_i}{dt}\} = sC_i V_i - C_i V_i(0)
\]

Eqn. 24(a)

\[
L\{I_{\text{therm}}u(t)\} = \frac{I_{\text{therm}}}{s}
\]

Eqn. 24(b)

With all three equations transformed, the node voltages, \(V\), and the current \(I_{\text{therm}}\) can be converted to node temperatures, \(T\), and the power dissipated, \(Q\), respectively, to get the matrix relation below:

\[
\begin{bmatrix}
\frac{1}{R_1} + sC_1 & -\frac{1}{R_1} & 0 \\
-\frac{1}{R_1} & \frac{1}{R_1} + \frac{1}{R_2} + sC_2 & -\frac{1}{R_2} \\
0 & -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_3} + sC_3
\end{bmatrix}
\begin{bmatrix}
T_1 \\
T_2 \\
T_3
\end{bmatrix}
= \begin{bmatrix}
\frac{Q}{s} + C_1 T_1(0) \\
C_2 T_2(0) \\
\frac{T_{\text{fixed}}}{R_3} + C_3 T_3(0)
\end{bmatrix}
\]

Eqn. 25

The \(T_{\text{fixed}}\) term is the fixed temperature while the \(T_i(0)\) terms represent the initial node temperatures. For any N-rung grounded capacitor RC network, a N-by-N matrix can easily be derived using the aforementioned analysis.

A LabView program written by Roger Stout was used for extracting the RC’s for the thermal network description of the cooling curves of the MRF183. Given initial guesses for the R’s and C’s in a grounded capacitor RC network, the program first solves the matrix for node temperatures under powered, steady-state conditions, i.e. \(Q = 45\) Watts, \(T_{\text{fixed}} = 24\) °C, and \(T_i(0) = 24\) °C. The resulting steady-state temperature solutions are then entered as the initial conditions, \(T_i(0)\), and the power, \(Q\), is set to zero. The calculation of node temperatures is reiterated for varying time to obtain the cooling curve of the initial RC network. The R’s and C’s of the grounded RC network are then optimized from the initial guess using Newton’s Method to minimize the error between the measured and calculated data. The extracted R’s and C’s for the three measured devices are summarized in the table below.
Table 6: Extracted RC’s for grounded capacitor network.

<table>
<thead>
<tr>
<th>Name</th>
<th>From</th>
<th>To</th>
<th>Device #1</th>
<th>Device #2</th>
<th>Device #3</th>
<th>Device #4</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>diode</td>
<td>GND</td>
<td>5.57E-03</td>
<td>1.14E-02</td>
<td>5.96E-03</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>node1</td>
<td>GND</td>
<td>8.40E-02</td>
<td>1.34E-01</td>
<td>7.95E-02</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>node2</td>
<td>GND</td>
<td>3.65E-01</td>
<td>5.28E-01</td>
<td>3.37E-01</td>
<td></td>
</tr>
<tr>
<td>C4</td>
<td>node3</td>
<td>GND</td>
<td>6.29E+00</td>
<td>9.72E+00</td>
<td>6.39E+00</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>node4</td>
<td>GND</td>
<td>7.09E+01</td>
<td>9.17E+01</td>
<td>8.04E+01</td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>node5</td>
<td>GND</td>
<td>8.90E+01</td>
<td>2.24E+02</td>
<td>1.28E+02</td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>node1</td>
<td>node1</td>
<td>7.87E-01</td>
<td>6.31E-01</td>
<td>7.31E-01</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>node1</td>
<td>node2</td>
<td>4.25E-01</td>
<td>4.96E-01</td>
<td>4.23E-01</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>node2</td>
<td>node3</td>
<td>5.53E-01</td>
<td>5.09E-01</td>
<td>6.49E-01</td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>node3</td>
<td>node4</td>
<td>2.40E-01</td>
<td>2.24E-01</td>
<td>2.59E-01</td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>node4</td>
<td>node5</td>
<td>2.82E-01</td>
<td>5.74E-01</td>
<td>4.04E-01</td>
<td></td>
</tr>
<tr>
<td>R6</td>
<td>node5</td>
<td>GND</td>
<td>5.14E-01</td>
<td>2.52E-01</td>
<td>3.97E-01</td>
<td></td>
</tr>
</tbody>
</table>

5.5 Summary

In this chapter, a technique exploiting the strong dependence of diode voltage and current on temperature has been described for determining a multiple RC thermal model. The substrate/source-to-drain diode innate to LDMOS FETs was used as the temperature sensitive parameter (TSP). As shown from the oven calibration results, the substrate/source-to-drain diode voltage is inversely proportional to temperature for a constant diode current. The cooling curve captured by measuring the diode voltage as the transistor cools off from thermal steady state allowed the extraction of a multiple RC thermal model. The total thermal resistances determined from cooling curve measurements of three devices (1.50 °C/W, 1.71 °C/W, and 1.64 °C/W) were close to the total thermal resistance of 1.62 °C/W obtained from the IR scan. In addition, the thermal time constants from the three cooling curves (0.236 sec., 0.334 sec., and 0.262 sec.) were similar to those obtained in the thermal capacitance measurements discussed in Section 4-2 (0.233 sec., and 0.220 sec.).

This chapter also included a discussion on the proper topology for the multiple RC thermal model. Commonly, the capacitors in the multiple RC thermal models are not grounded and each shunt RC pair is connected in series with another set of shunt RC’s. While mathematically convenient, a grounded capacitor thermal model is more accurate for describing the physical, thermal phenomenon. In particular, the thermal capacitances should relate the change in temperature with respect to time. The non-grounded network by adjoining neighboring capacitances is relating the change in temperature at each position with respect to temperatures at adjoining elements in the system that are also changing. Since the two topologies can be made mathematically equivalent, they are interchangeable and either one of the topologies can be used to describe the multiple RC thermal model.
Chapter 6
LDMOS Electro-Thermal Model Evaluation

A rigorous validation of the LDMOS Electro-Thermal Model was performed and is presented in this chapter. The validation begins with a comparison of modeled vs. measured CW IV curves. Because the isothermal electrical model accurately predicts the pulsed IV behavior of the devices at various temperatures as shown in Chapter 3, the CW IV comparison shows how well the extracted thermal resistance predicts the operating temperature. CW S-parameters are also included to validate the small signal model. Lastly, the large signal model is evaluated using loadpull measurements performed on the MRF183. The key power figures of merit that are emphasized in the validation of the large signal model are output power, gain, efficiency, and IMD.

6.1 CW IV
Validation of the thermal subcircuit and its interaction with the electrical portion of the Electro-Thermal Model were done by comparing constant DC IV measurements to simulations using the extracted thermal resistance values. Under constant DC bias, drain-to-source current exhibits self-heating effects. Simulations of constant DC IV exercise both the thermal subcircuit for calculating instantaneous temperature and the isothermal drain-to-source current model. A comparison of the simulated and measured CW IV data provides information about the accuracy of the thermal portion of the model.

6.1.1 CW IV Measurements
CW IV measurements were taken in a setup similar to that of the thermal capacitance measurements (Figure 40). The measured voltage across the sampling resistance was converted into drain current by dividing by the sampling resistance, \( R_{\text{sampling}} = 0.0667 \text{ Ohm} \). The fixture used had the passive bias components soldered on the fixture substrate since the Hewlett-Packard bias networks cannot handle high current levels.

![Figure 40: CW IV measurement setup using a sampling resistor.](image-url)
In order to be consistent with the thermal simulations, the thermal scans, and the thermal transient measurements, the case temperature for the CW IV measurements was fixed at 75 °C. To maintain a case temperature of 75 °C even as the power dissipation changes during the IV sweeps, the temperature of the copper heatsink underlying the fixture had to be varied and controlled. By placing the Thermostream underneath the heatsink and embedding the thermocouple wire in the copper beneath the package case, the heatsink temperature could be adjusted while monitoring the case temperature. The Thermostream was computer controlled such that it varied its output air temperature and thus, the heatsink temperature to maintain $T_{case} = 75$ °C throughout the measurement.

6.1.2 CW IV Simulations

Motorola’s WINFET program was used to simulate the CW IV curves. With the model parameters of the isothermal drain-to-source current model already determined from the pulsed IV and parasitic data, only the thermal resistance was varied to produce modeled CW IV data. For each thermal resistance extracted from thermal simulations, IR scans, and thermal transient measurements, modeled CW IV data was generated. WINFET allows the user to specify a power dissipation limit such that the simulated data covers the same IV space as the measured data.

6.1.3 CW IV: Measured v. Modeled

In figure 41, the measured CW IV data and modeled CW IV data sets are graphed. As seen in the bottom graph, both models using $R_{th}$ values derived from the thermal simulations overshoot the drain-to-source current at high gate voltages. Since the modeled currents are too high when biased above the zero-temperature coefficient bias condition, the predicted temperatures are too low. This implies that both thermal simulations under-predicted the thermal resistance. Most likely the errors in both simulations (DieTemp RMSE = 0.467, ANSYS RMSE = 0.577) arise from the impreciseness of the thermal conductivity of the package material, CuW used as input. More simulations must be conducted in DieTemp and ANSYS with various thermal conductivities of CuW to obtain more reasonable thermal resistance values.

The match is much better in comparing measured and modeled CW IV using the thermal resistance extracted from the IR scan ($R_{th}$=1.62 °C/W). The model is again slightly over-predicting current at higher gate and drain voltages. Still the error between the measured and modeled is minimal (RMSE = 0.425) and as expected the IR scan is an accurate method to determine junction temperature and thermal resistance.

Lastly, we compare the measured data and modeled data using thermal resistances extracted from the three thermal transient measurements. The thermal resistance of Device #11, $R_{th}$=1.64 °C/W, gave the best fit between measured and modeled while the other two extracted values, $R_{th}$=1.50 °C/W and $R_{th}$=1.71 °C/W, were too low and too high, respectively. In general, all three thermal resistance values extracted from the thermal transient measurements produced acceptable agreement between measured and modeled.
6.2 CW Small Signal S-Parameters

6.2.1 Small Signal S-Parameter Measurements

CW S-parameter measurements for validation were taken using HP's 8510 Vector Network Analyzer. A two-tier calibration was performed prior to measuring in the 50 Ohm S-parameter fixture as described in Section 5-1 for the package electrical
measurements. A thermocouple was embedded underneath the package case to monitor the case temperature. The MRF183 was biased to the operating drain voltage of 28 V and the quiescent current of 2 mA/mm or 240mA. The case temperature was approximately 25 °C during the measurement. The fixture error boxes were de-embedded from the measured S-parameter data to obtain the DUT's S-parameters.

6.2.2 Small Signal S-Parameter Simulations
An S-parameter circuit and test bench (Figures 42(a) and 42(b)) using the MET LDMOS model were created in Libra. Blocking capacitors and inductive chokes were added to the input and output ports of the Electro-Thermal Model circuit schematic to prevent RF signals from entering the DC bias lines. The case temperature was set to 25 °C as in the measurement and the S-parameters were simulated up to 4 GHz.

![Figure 42 (a): Libra circuit schematic for S-parameter simulations.](image)

![Figure 42 (b): Libra test bench for S-parameter simulations.](image)

6.2.3 Small Signal S-Parameter: Measured vs. Modeled
Figures 43(a)-(d) compare the measured small signal S-parameters and modeled small signal S-parameters. While the magnitudes of the S-parameters show reasonable agreement, the modeled phases of the S-parameters are significantly off at high frequencies. This discrepancy may be due to the fixture used in the S-parameter measurements of the MRF183 transistor. Also, since the small signal model parameters for the MRF183 were obtained by scaling the parameters of a smaller device, scaling could also be a source of error.
Figure 43(a): Modeled vs. measured constant S-parameters (S11) for the MRF183 transistor.

Figure 43(b): Modeled vs. measured constant S-parameters (S12) for the MRF183 transistor.
Figure 43(c): Modeled vs. measured constant S-parameters (S21) for the MRF183 transistor.

Figure 43(d): Modeled vs. measured constant S-parameters (S22) for the MRF183 transistor.


6.3 Large Signal Loadpull
Loadpull measurements are commonly used for validating models of high power transistors. Loadpull systems allow a range of impedances to be presented to the device under test without using any passive components on an evaluation board. Presently, loadpull systems for handling the high power levels are primarily based on mechanical tuners. A major disadvantage of mechanical tuners is its limited impedance range and its increased error at low impedances. Since high power transistors designed for base stations such as the MRF183 exhibit low input and output impedances when optimally tuned, a method to enhance the impedance range and improve the precision of the system at low impedances is desired. One solution utilizes a quarter-wave transformer [15] to re-normalize the system impedance.

6.3.1 Large Signal Loadpull Measurements

Quarter-Wave Transformer
For the loadpull measurements of the MRF183 devices, a quarter-wave pre-matching test fixture was designed and constructed with microstrip. In the fixture, a feedline with a characteristic impedance of 50 Ohms is connected with a microstrip line of length $\lambda/4$ and of characteristic impedance of ~15 Ohms to give a load resistance of approximately 4.5 Ohms (Figure 44).

![Figure 44: Quarter Wave Transformer for Loadpull Measurements](image)

The exact characteristic impedance of the constructed quarter-wave transformer was calculated by performing Time Domain Reflectometry (TDR) simulations (Appendix E) on measured S-parameters of the lines built for the TRL calibration. The characteristic impedance of the microstrip line ($Z_1$) and the load ($Z_L$) were calculated to be 14.94 Ohm and 4.33 Ohm respectively. Fixture error boxes were obtained using a quarter-wave, multi-line TRL calibration. The algorithm used to extract error boxes for the 50 Ohm S-parameter fixture (described in section 2-1) was modified to normalize the ports facing the DUT to 4.33 Ohm for the quarter-wave transformer fixture error boxes.

Loadpull System Setup and Calibration
The complete setup for the loadpull measurements including Maury Microwave’s Automated Tuner System is shown in Figure 45. Two signal generators and power
amplifiers were required to perform two tone measurements. Missing from the figure are attenuators added to protect the instruments at high power levels and improve system accuracy.

![Diagram of Loadpull Measurement Setup](image)

**Figure 45: Loadpull Measurement Setup**

Prior to performing loadpull measurements a system calibration must be executed in order to know the exact impedances and power quantities presented to the DUT at various frequencies.

The calibration procedure began with tuner characterization. Each tuner was connected to the Vector Network Analyzer (VNA) to measure the 2-port S-parameters for a specified set of tuner positions at various frequencies. The frequencies of interest for the MRF183 device under single tone excitation are the original frequency of the input signal or the fundamental frequency of 1 GHz and its second and third harmonics (i.e. 2 GHz and 3 GHz). For the two tone measurements of the MRF183 device, the frequencies of the two input signals ($f_1=1$ GHz and $f_2=1.001$ GHz) will be so close to each other that the tuner S-parameters measured for the single tone case are assumed to be the same for the frequencies of the mixed products around the fundamental frequency and its second and third harmonics. However, the tuners must also be characterized at 1 MHz for the near-DC higher order products (e.g. $f_2-f_1$) present under two tone excitation.

Once the tuner calibration was completed, the efficiency, loss, and reflection coefficient values of the input and output power sensors were determined using the VNA to create a power sensor file. Next, the system was assembled and a zero-length thru line was connected in place of the DUT to perform a power calibration. A power calibration of the first RF source is conducted to measure the available power at the input of the source tuner over a programmed power range. In addition, the second RF source and the spectrum analyzer coupler are calibrated.

Before placing the quarter-wave pre-matching test fixture and the device into the system for measuring, the calibration was verified by measuring transducer gain with the input and output impedances set to positions all over the Smith Chart. Since S-parameters of the input sensor and tuner, the zero-length thru line, and the output tuner and sensor are all known from calibration, the transducer gain can be calculated from the cascaded S-parameters and compared to the measured transducer gain. Because the difference in measured and calculated transducer gains were less than 0.4 dB, the calibration was
sufficient. Ready for measuring, the thru line was replaced by the loadpull fixture containing a MRF183 transistor. Also, the fixture error boxes (S-parameters of the input and output fixture halves) were uploaded into the Maury software for de-embedding. De-embedding the error boxes shifts the reference plane of the measurements to the input and output leads of the device package.

**Loadpull Measurements**

With the device biased to produce a quiescent current of 240 mA \((V_{ds} = 28V, V_{gs} \sim 4.2V)\), an input power of 33dBm was applied and source pull measurements were conducted to determine the input impedance that minimizes the reflected power or return loss at the input. Good source tuner matching assures that the difference between the power delivered to the device and the available power from the RF source is minimized. With the input impedance set for the lowest return loss, loadpull measurements were subsequently performed to determine the load impedances for maximum power and maximum efficiency. With the output impedance set for maximum efficiency and power, source pull measurements had to be repeated since changing the output impedance affects the input behavior and vice versa. Loadpull and source pull measurements were iterated until a set of input and output impedances that simultaneously minimized return loss and maximized power and efficiency were determined. The resulting optimal reflection coefficients normalized to 50 Ohm are given in the table below.

<table>
<thead>
<tr>
<th>Source</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mag</td>
<td>Angle</td>
</tr>
<tr>
<td>Maximum Efficiency</td>
<td>0.97367</td>
</tr>
<tr>
<td>Maximum Power</td>
<td>0.97367</td>
</tr>
</tbody>
</table>

*Table 7: Optimal Source and Load 50 Ohm Reflection Coefficients for MRF183*

For the resulting set of input and output impedances, the power figures of merit such as output power, power added efficiency, return loss, transducer and power gain, and the intermodulation products (for two tone only) were measured under single and two tone excitation as the input power was swept. The input power was swept from -11 dBm, at which the device is still considered to be operating in the small signal regime, to 38 dBm, at which the device is at least 3 dB into compression.

**6.3.2 Large Signal Loadpull Simulations**

The circuit schematic and the single tone harmonic balance test bench used for the large signal loadpull simulations in Libra are shown in the figures (Figures 46(a) and (b)) below. The two tone simulation setup is similar except another RF source is added at the input in the test bench. The 50 Ohm reflection coefficients as listed in Table 9 are presented to the device model in the circuit schematic of Libra as S-parameter (S2P) files.
6.3.3 Large Signal Loadpull Measurements vs. Simulations

Graphs comparing measured and modeled power sweeps are shown on figures 47(a)-(d). The graphs show little differences between the measured and modeled data with the exception of gain and two-tone IMD. The transducer gain also exhibits a discrepancy of 0.5 dB to 1 dB. Marginally acceptable, the modeled transducer gain may be improved by tuning of the current gain parameter, Beta and parameters describing the gate-to-source capacitance, $C_{gs}$. The mismatch in the two-tone IMD case can be attributed to the capacitance functions that do not exactly predict the small signal performance (see Section 3.2.4). Harmonics and IMD are computed from higher order derivatives of capacitances and conductances with respect to gate and drain voltages. Harmonics and IMD are often the most difficult circuit characteristic to predict because slight
inaccuracies of the capacitance and conductance functions result in large errors in predicting the higher order derivatives. Modifications in the capacitance functions are needed to improve the accuracy of the large signal model in predicting IMD.

![Graph of P_{out} vs. P_{in}](image)

**Figure 47(a):** Modeled vs. measured output power.

![Graph of PAE vs. P_{in}](image)

**Figure 47(b):** Modeled vs. measured power added efficiency.
Figure 47(c): Modeled vs. measured transducer gain.

Figure 47(d): Modeled vs. measured output power at highest 3IMD.
6.4 Summary
In this chapter, the evaluation of the LDMOS Electro-Thermal Model is presented. Comparison of the modeled vs. measured CW IV curves confirmed that the thermal resistance values extracted from the IR scan and the diode measurements are accurate for predicting the device’s operating temperature. Although the CW S-parameter measurements contained noise from coupling, the small signal model was able to well predict the low frequency behavior. For the large signal model, the differences in the modeled vs. measured output power and power added efficiency were minimal. A discrepancy of less than 1 dB was observed in the modeled vs. measured large-signal gain. Tuning of current gain parameter, Beta and parameters describing the gate-to-source capacitance, \( C_{gs} \) may improve the modeled transducer gain. Of most concern, the large signal model under-predicted IMD by approximately 10 dBm. The error is most likely due to the small signal capacitance functions that incorrectly predict higher order derivatives needed for computing harmonics and IMD.
Chapter 7

Conclusion and Future Work

The electrical and thermal characteristics of LDMOS devices have been investigated and incorporated into Motorola's Electro-Thermal LDMOS Model using a simple thermal subcircuit. The analog thermal subcircuit consists of a current source representing the power dissipated, a thermal resistance, and a thermal capacitance, and accounts for the self-heating of the device.

Electrical characterization of the LDMOS device included pulsed IV and pulsed S-parameter measurements over several temperatures. This allowed the de-coupling of the electrical and thermal behavior of the device and the extraction of the small signal and large signal model in terms of the drain-to-source voltage, gate-to-source voltage, and temperature.

Thermal characterization involved various methods common in industry for determining the total thermal resistance from the device junction to the bottom package case of the DUT. The total thermal resistance was directly measured using an infrared radiation scan. Thermal simulations that included finite element analysis were performed to predict thermal resistance but were found to underestimate the thermal resistance. The thermal time constant was obtained from measurements involving the change in drain-to-source current due to self-heating. With the total thermal resistance determined from IR scans and the extracted thermal time constant, the thermal capacitance was computed to create a single RC thermal model.

An indirect, electrical method based on transient measurements exploiting the drain-to-substrate diode inherent in LDMOS devices was developed to accurately measure the junction temperature. This technique not only provided simultaneous information about the thermal resistance and capacitance but also allowed extraction of a multiple RC thermal model. The resulting multiple RC thermal model were consistent with the single RC thermal model.

With the extracted thermal model, Motorola's Electro-Thermal Model was validated under DC, small signal, and large signal conditions. Comparison of modeled CW IV and measured CW IV showed that the thermal resistances determined by the IR scan and the thermal transient measurements, $R_{th} = 1.62 \, ^\circ C/W$ and $R_{th} = 1.64 \, ^\circ C/W$, respectively, were most accurate. CW S-parameters were also measured and compared to the modeled. While the magnitude of the S-parameters predicted by the model fit the measured magnitude reasonably well, the phase showed considerable mismatch. Loadpull power sweeps that exercise the large signal model portion of the Electro-Thermal Model in Libra accurately predicted the output power, efficiency, and drain current. The modeled transducer and power gain was slightly lower than measured but the discrepancy is still acceptable. The figure of merit that produced the largest error between measured and modeled was the two tone IMD. Further investigation into functions describing the small-
signal model capacitances and the impedance of the subharmonic tuner termination is needed to rectify the disagreement in IMD.

Because the emphasis of this work was on the extraction of the thermal resistance and its implementation and impact on the model, future work on Motorola’s Electro-Thermal Model could include an extensive investigation on the thermal capacitance and thermal time constant. The impact of the thermal capacitance and thermal time constant is not noticeable in the measurements and simulations presented here. However, measurements and circuit envelope simulations using continuous spectra or digitally modulated signals would be significantly influenced by the thermal time constant.

In addition, the grounded capacitor RC network ladder that can be extracted from the diode measurement could be implemented into the Electro-Thermal Model. This modification would provide a physically meaningful thermal model that will be accurate in describing the thermal transient behavior of the device.
References


Appendix A: Heat Conduction

A.1 General Heat Conduction Theory

A.1.1 Three Dimensional Heat Conduction Equation

The 3-dimensional heat conduction equation is derived from the first law of thermodynamics. Conservation of energy [1] states that:

\[
\left( \text{Heat conducted into per unit time} \right)_{x=x, \ y=y, \ z=z} + \left( \text{internal heat generated per unit time} \right) = \\
\left( \text{Heat conducted out per unit time} \right)_{x=dx, \ y=dy, \ z=dz} + \left( \text{change in internal energy per unit time} \right) + \left( \text{work done by volume element per unit time} \right)
\]

Assuming that the expansion of solids due to temperature is minimal, the last term on the right side of the equation can be neglected. Mathematically, the above relation translates to:

\[
a \frac{\partial^2 T}{\partial x^2} + k \frac{\partial^2 T}{\partial y^2} + k \frac{\partial^2 T}{\partial z^2} + \dot{q} = \rho c \frac{\partial T}{\partial t}
\]

Eqn. A.1

where \( k \) is the thermal conductivity, \( \rho \) is the density, and \( c \) is the specific heat of the material. In the above equation, the thermal conductivity is assumed to be constant with respect to temperature and position.

A.1.2 One Dimensional Heat Conduction Equation

The 3-dimensional heat conduction equation can be reduced under the assumption of 1-dimensional heat flow. With the heat flowing only in the \( x \) direction (see Figure A.1), the heat conduction becomes:

\[
k \frac{d^2 T}{dx^2} + \dot{q} = \rho c \frac{dT}{dt}
\]

Eqn. A.2

A.2 RC Network Representation for One Dimensional Heat Flow

![RC Network Diagram](image)

Figure 3.1: Heat flow through a plane layer without internal heat generation

In steady state, the 1-dimensional heat flow equation reduces to:

\[
k \frac{d^2 T}{dx^2} + \dot{q} = 0
\]

Eqn. A.3

The above second order equation can be solved given several boundary conditions. The three boundary conditions are:

(a) at \( x=0 \), \( T=T_1 \).

(b) at \( x = 0 \), \( \frac{dT}{dx} = 0 \).

(c) at \( x=h \), \( T=T_2 \).

Integrating equation A.3 for temperature \( T \) yields:
\[ T = -\frac{\dot{q}x^2}{2k} + C_2 \]  
\text{Eqn. A.4}

Applying boundary condition (a) applied to the above equation gives

\[ C_2 = T_1. \]

Differentiating equation A.4 and using boundary condition (b) results in \( C_1 = 0 \).

The equation for temperature (A.4) in terms of \( x \) becomes:

\[ T = -\frac{\dot{q}x^2}{2k} + T_1 \]  
\text{Eqn. A.5}

Plugging in boundary condition (c),

\[ T_1 - T_2 = \frac{\dot{q}h^2}{2k} \]

or

\[ \frac{(T_1 - T_2)}{h^2/2k} = \dot{q} \]  
\text{Eqn. A.6}

Rewriting equation A.2, the non-steady state, 1-dimensional heat conduction equation using the above relation gives:

\[ \frac{(T_1 - T_2)}{h^2/2k} + \rho c \frac{dT}{dt} = \dot{q} \]  
\text{Eqn. A.7}

Since \( \dot{q} \) is in terms of watts per unit volume, all terms on both sides of equation A.7 have to be multiplied by the volume of the layer, \( V = A \times h \) to obtain the equation in terms of total power dissipated through the layer, \( Q \):

\[ Q = \frac{(T_1 - T_2)}{R_{th}} + C_{th} \frac{dT}{dt} \]  
\text{Eqn. A.8}

where

\[ R_{th} = \frac{h}{2kA} \quad \text{and} \quad C_{th} = \rho c V \]  
\text{Eqn. A.9}

The thermal time constant or RC product is thus:

\[ \tau = R_{th}C_{th} = \frac{h^2}{2\alpha} \]  
\text{Eqn. A.10}

where \( \alpha \) is the thermal diffusivity \( \alpha = \frac{k}{\rho c} \).
## Appendix B: MET LDMOS Model Parameters (Isothermal)

The following table contains all the MET LDMOS model parameter definitions and their units.

<table>
<thead>
<tr>
<th>PARAMETER NAME</th>
<th>PARAMETER DEFINITION</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RG_0</td>
<td>Gate Resistance Evaluated at Tnom</td>
<td>Ω</td>
</tr>
<tr>
<td>RG_1</td>
<td>Gate Resistance Coefficient</td>
<td>Ω/K</td>
</tr>
<tr>
<td>RS_0</td>
<td>Source Resistance Evaluated at Tnom</td>
<td>Ω</td>
</tr>
<tr>
<td>RS_1</td>
<td>Source Resistance Coefficient</td>
<td>Ω/K</td>
</tr>
<tr>
<td>RD_0</td>
<td>Drain Resistance Evaluated at Tnom</td>
<td>Ω</td>
</tr>
<tr>
<td>RD_1</td>
<td>Drain Resistance Coefficient</td>
<td>Ω/K</td>
</tr>
<tr>
<td>VTO_0</td>
<td>Forward Threshold Voltage Evaluated at Tnom</td>
<td>V</td>
</tr>
<tr>
<td>VTO_1</td>
<td>Forward Threshold Voltage Coefficient</td>
<td>V/K</td>
</tr>
<tr>
<td>GAMMA</td>
<td>IDS Equation Coefficient</td>
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</tr>
<tr>
<td>VST</td>
<td>Sub-Threshold Slope Coefficient</td>
<td>V</td>
</tr>
<tr>
<td>BETA_0</td>
<td>IDS Equation Coefficient. BETA Evaluated at Tnom</td>
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<td>BETA_1</td>
<td>IDS Equation Coefficient</td>
<td>1/K</td>
</tr>
<tr>
<td>LAMBDTA</td>
<td>IDS Equation Coefficient</td>
<td>1/V</td>
</tr>
<tr>
<td>VGEXP</td>
<td>IDS Equation Coefficient</td>
<td>---</td>
</tr>
<tr>
<td>ALPHA</td>
<td>IDS Equation Coefficient</td>
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<td>VK</td>
<td>IDS Equation Coefficient</td>
<td>V</td>
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<td>DELTA</td>
<td>IDS Equation Coefficient</td>
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<td>Breakdown Voltage Evaluated at Tnom</td>
<td>Volts</td>
</tr>
<tr>
<td>VBR_1</td>
<td>Breakdown Coefficient @ Vgs=0V</td>
<td>Volts/K</td>
</tr>
<tr>
<td>K1</td>
<td>Breakdown Parameter</td>
<td>---</td>
</tr>
<tr>
<td>K2</td>
<td>Breakdown Parameter</td>
<td>---</td>
</tr>
<tr>
<td>M1</td>
<td>Breakdown Parameter</td>
<td>V</td>
</tr>
<tr>
<td>M2</td>
<td>Breakdown Parameter</td>
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<tr>
<td>M3</td>
<td>Breakdown Parameter</td>
<td>V</td>
</tr>
<tr>
<td>BR</td>
<td>Reverse IDS Equation Coefficient</td>
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</tr>
<tr>
<td>RDIODE_0</td>
<td>Reverse Diode Series Resistance Evaluated at Tnom</td>
<td>Ω</td>
</tr>
</tbody>
</table>

---

1 Obtained from MET LDMOS Model Documentation by Jaime Plá
(http://mot-sps.com/models/ldmos/ldmosmodels.html)
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>RDIODE_1</td>
<td>Reverse Diode Series Resistance Coefficient</td>
<td>Ω/Κ</td>
</tr>
<tr>
<td>ISR</td>
<td>Reverse Diode Leakage Current</td>
<td>Α</td>
</tr>
<tr>
<td>NR</td>
<td>Reverse Diode Ideality Factor</td>
<td>---</td>
</tr>
<tr>
<td>VTO_R</td>
<td>Reverse Threshold Voltage Coefficient</td>
<td>V</td>
</tr>
<tr>
<td>RTH</td>
<td>Thermal Resistance Coefficient</td>
<td>°C/Watts</td>
</tr>
<tr>
<td>GGS</td>
<td>Gate To Source Conductance</td>
<td>1/Ω</td>
</tr>
<tr>
<td>GGD</td>
<td>Gate to Drain Conductance</td>
<td>1/Ω</td>
</tr>
<tr>
<td>TAU</td>
<td>Transit Time Under Gate</td>
<td>Seconds</td>
</tr>
<tr>
<td>TNOM</td>
<td>Temperature at Which Model Parameters are Extracted</td>
<td>K</td>
</tr>
<tr>
<td>TSNK</td>
<td>Heat Sink Temp.</td>
<td>°C</td>
</tr>
<tr>
<td>CGST</td>
<td>Cgs Temperature Coefficient</td>
<td>1/K</td>
</tr>
<tr>
<td>CDST</td>
<td>Cds Temperature Coefficient</td>
<td>1/K</td>
</tr>
<tr>
<td>CGDT</td>
<td>Cgd Temperature Coefficient</td>
<td>1/K</td>
</tr>
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<td>CTH</td>
<td>Thermal Capacitance</td>
<td>J/°C</td>
</tr>
<tr>
<td>KF</td>
<td>Flicker Noise Coefficient</td>
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<tr>
<td>AF</td>
<td>Flicker Noise Exponent</td>
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</tr>
<tr>
<td>FFE</td>
<td>Flicker Noise Frequency Exponent</td>
<td>---</td>
</tr>
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<td>N</td>
<td>Forward Diode Ideality Factor</td>
<td>---</td>
</tr>
<tr>
<td>ISS</td>
<td>Forward Diode Leakage Current</td>
<td>Α</td>
</tr>
<tr>
<td>CGS1</td>
<td>Cgs Equation Coefficient</td>
<td>F</td>
</tr>
<tr>
<td>CGS2</td>
<td>Cgs Equation Coefficient</td>
<td>F/V</td>
</tr>
<tr>
<td>CGS3</td>
<td>Cgs Equation Coefficient</td>
<td>V</td>
</tr>
<tr>
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<td>F/V</td>
</tr>
<tr>
<td>CGS5</td>
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<td>CGS6</td>
<td>Cgs Equation Coefficient</td>
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</tr>
<tr>
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<td>Cgd Equation Coefficient</td>
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<td>CGD4</td>
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<td>F</td>
</tr>
<tr>
<td>CDS2</td>
<td>Cds Equation Coefficient</td>
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</tr>
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<td>CDS3</td>
<td>Cds Equation Coefficient</td>
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<td>AREA</td>
<td>Gate Periphery Scaling Parameter</td>
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<td>N_FING</td>
<td>Gate Finger Scaling Parameter</td>
<td>---</td>
</tr>
</tbody>
</table>
Appendix C: MET LDMOS Model Equations

C.1 The temperature dependency of parasitic resistances is given by:

\[ R_g = R_{g\_0} + R_{g\_1} \times (T - T_{NOM}) \]
\[ R_d = R_{d\_0} + R_{d\_1} \times (T - T_{NOM}) \]
\[ R_s = R_{s\_0} + R_{s\_1} \times (T - T_{NOM}) \]

\[ T = V_{th\_rise} + V_{tsnk} + 273 = V_{th\_rise} + T_{SNK} + 273 \]

where \( T \) is the actual or total temperature (not the temperature rise) in K and \( T_{NOM} \) is the temperature at which the parameters were extracted. The value of \( V_{tsnk} \) (°C) is numerically equal to the heat sink temperature \( T_{SNK} \) (°C). Notice that even though \( R_{g_1}, R_{d_1} \) and \( R_{s_1} \) have units of Ω/K, their numerical value will be the same if the units are Ω/°C.

C.2 The forward bias drain to source current equation is given by:

\[ V_{TO} = V_{TO\_0} + V_{TO\_1} \times (T - T_{NOM}) \]
\[ BETA = BETA\_0 + BETA\_1 \times (T - T_{NOM}) \]
\[ V_{BR} = V_{BR\_0} + V_{BR\_1} \times (T - T_{NOM}) \]
\[ V_{gst1} = V_{gs} - \left( V_{TO} + (\text{GAMMA} \times V_{ds}) \right) \]
\[ V_{gst2} = V_{gst1} - \frac{1}{2} \left( V_{gst1} + \sqrt{(V_{gst1} - \text{VK})^2 + \text{DELTA}^2} - \sqrt{\text{VK}^2 + \text{DELTA}^2} \right) \]
\[ V_{gst} = VST \times \ln \left( \frac{V_{gst2}}{VST} + 1 \right) \]

\[ V_{BReff} = \frac{V_{BR}}{2} \left( 1 + \tanh[M1 - V_{gst} \times M2] \right) \]
\[ V_{BReff1} = \frac{1}{K2} \left( V_{ds} - V_{BReff} \right) + M3 \left( \frac{V_{ds}}{V_{BReff}} \right) \]

\[ I_{ds} = \left( BETA \cdot V_{gst} \cdot V_{ds} \right) \text{Tanh} \left( \frac{V_{ds} \times \text{ALPHA}}{V_{gst}} \right) \left[ l + K1 \times e^{V_{BReff1}} \right] \]

C.3 The forward bias drain to source diode is given by:

\[ V_t = \frac{k \times N \times T}{q} \]

where \( k \) is the Boltzmann's constant (8.62E-5 eV/K), \( T \) is the temperature in Kelvin, and \( q \) is the electron charge (1 eV)

---

1 Obtained from MET LDMOS Model Documentation by Jaime Plá (http://mot-sps.com/models/ldmos/ldmosmodels.html)
C.4 The reverse bias drain to source current equation is given by:

\[
Idiode\_f = \frac{(Vds\_f/BR)}{e}\]

\[
VTO = VTO\_R + VTO\_I \times (T - TNOM)
\]

\[
Vgst1 = Vgs - (VTO - (GAMMA \times Vds))
\]

\[
Vgst2 = Vgst1 - \frac{1}{2} \left( \sqrt{Vgst1^2 + (Vgst1 - YK)^2 + DELTA^2} - \sqrt{VK^2 + DELTA^2} \right)
\]

\[
Vgst = VST \times \ln \left( Vgst2 \times e^{\frac{Vgst2}{VST}} + 1 \right)
\]

\[
Ids = (BR \times Vds \times Vgst)
\]

C.5 The reverse bias drain to source diode is given by:

\[
Vt2 = \frac{k \times NR \times T}{q}
\]

\[
Ism = ISR \times \left( \frac{T}{TNOM} \right)^3 \times e^{-\left(\frac{Eg}{Vt2}\right) \times \left(1 - \frac{T}{TNOM}\right)}
\]

where \( Eg \) is the energy gap for Silicon which is equal to 1.11 [3] and T is temperature in Kelvin.

\[
Idiode\_r = Ism \times \left( e^{\frac{Vdiode\_r}{Vt2}} - 1 \right)
\]

The reverse diode's series resistance is given by:

\[
Rdiode = RDIODE \_0 + RDIODE \_1 \times (T - TNOM)
\]

C.6 The gate to source capacitance equation is given by:

\[
Cgs = (CGS1 + CGS2) [1 + Tanh(CGS6 \times (Vgs + CGs3))] + CGS4 \times (1 - Tanh(Vgs \times VGS5)) \times (1 + CGST \times (T - TNOM))
\]

C.7 The gate to drain capacitance equation is given by:

\[
Cgd = \left( CGD1 + \frac{CGD2}{1 + CGD3 \times (Vgd - CGD4)^2} \right) \times (1 + CGDT \times (T - TNOM))
\]
C.8 The drain to source capacitance equation is given by:

\[ C_{ds} = \left( C_{DS1} + \frac{C_{DS2}}{1 + C_{DS3} \cdot V_{ds}} \right) \cdot \left( 1 + C_{DST} \cdot (T - T_{NOM}) \right) \]

C.9 The noise is calculated as shown in [3], as the sum of the thermal chanel noise and the flicker noise as shown by the following equation:

\[ \frac{\sigma_{id}}{id^2} = \frac{8 \cdot k \cdot T \cdot g_m}{3} + KF \cdot \left( \frac{I_{ds}^\text{dc}}{f^\text{FF}} \right) \]

where \( g_m \) is the transconductance of the device at the operating point, \( T \) is temperature in Kelvin, and \( f \) the frequency. In addition all resistors are also modeled as thermal noise sources.

\[ \frac{\sigma_{id}}{id^2} = \frac{4 \cdot k \cdot T}{R} \]

where \( R \) is the resistance value and \( T \) is the temperature in Kelvin.

C.10 To avoid convergence problems the maximum temperature rise, \( V_{th\_rise} \) (°C) is limited to 300 °C using the following equation:

\[
V_{th\_rise} = \begin{cases} 
0 & 0 \leq V_{th\_rise} \\
V_{th\_rise} & 0 < V_{th\_rise} < 250 \\
250 + 50 \cdot \text{tanh} \left( \frac{V_{th\_rise} - 250}{50} \right) & 250 \leq V_{th\_rise}
\end{cases}
\]
Appendix D: DieTemp

DieTemp is based on the paper, “Steady-State Junction Temperatures of Semiconductor Chips” by Lindsted and Surty. In the paper, the three dimensional Laplace equation:

\[
\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0
\]

Eqn. D.1

is solved for temperature T, using several boundary conditions. For a device or chip with a width of 2A, length of 2B, thickness F, and a thermal conductivity of K, and assuming a heat flux Q over a top surface of 2C x 2D, the temperature at any point (x,y) on the junction plane is given by:

\[
T(x, y) = \frac{Q \ CD}{K \ AB} F
\]

\[
+ \sum_{m=1}^{\infty} -\frac{Q}{K \ m^2 \pi^2 A} \left( \frac{1 - \exp(2m\pi F / B)}{1 + \exp(2m\pi F / B)} \right) \left[ \sin \left( \frac{m\pi D}{B} \right) \cos \left( \frac{m\pi y}{B} \right) \right]
\]

\[
+ \sum_{n=1}^{\infty} -\frac{Q}{K \ n^2 \pi^2 B} \left( \frac{1 - \exp(2m\pi F / A)}{1 + \exp(2m\pi F / A)} \right) \left[ \sin \left( \frac{n\pi C}{A} \right) \cos \left( \frac{n\pi x}{A} \right) \right]
\]

\[
+ \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \left[ \frac{Q}{K \ mn \pi^2 \gamma} \left( \frac{1 - \exp(2m\pi F)}{1 + \exp(2\gamma F)} \right) \right] \times \left[ \sin \left( \frac{n\pi C}{A} \right) \cos \left( \frac{n\pi x}{A} \right) \sin \left( \frac{m\pi D}{B} \right) \cos \left( \frac{m\pi y}{B} \right) \right]
\]

Eqn. D.2

where

\[
\gamma^2 = \pi^2 \left[ \left( \frac{n}{A} \right)^2 + \left( \frac{m}{B} \right)^2 \right]
\]
Appendix E: Determining Characteristic Impedance Using Time Domain Reflectometry

In order to calculate the quarter-wave transformer's input and output error boxes using the TRL technique[9], the exact characteristic impedance of each line standard needs to be determined. A Matlab program written by Peter Aaen calculates the characteristic impedance of delay lines using simulated time domain reflectometry (TDR). With the measured S-parameters of a calibration line standard as input, the program generates the time domain reflection at the input port due to an incident pulse. The flowchart below describes the process of generating the reflection response due to an incident pulse using measured S-parameters of a transmission line.

![Flowchart of generating time domain response from frequency domain data](image)

The technique for determining the characteristic impedance of a transmission line is based on the theory behind time domain reflectometry. If a device under test is excited with a square pulse having a fast rise time and 1 Volt amplitude, the reflected voltage signal is equal to the reflection coefficient. Knowledge of the reflection coefficient allows the calculation of the impedance, \( Z_f \), at a specific point in time, where \( Z_0 \) is the impedance of the transmission line leading up to \( Z_T \).

\[
Z_f = Z_0 \frac{1 + \Gamma}{1 - \Gamma}
\]

Eqn. E.1

Using the above analysis, the characteristic impedance of the quarter-wave transformer and its delay line were determined. Recall from Section 7.3.1.1 that the quarter-wave transformer for the loadpull measurements was designed such that the 50 Ohm feedline was transformed down to approximately 4.5 Ohm using a microstrip line of 15 Ohm at 1 GHz. The S-parameters of a line standard built for calibration of the quarter-wave transformer was measured and convoluted with an incident pulse and the reflected voltage waveform below (Figure E.2) was performed. The incident pulse used had a 1 Volt amplitude with a 0.1 nsec rise time, 5 nsec duration time, and 0.1 nsec fall time.
The diagram in Figure E.3 traces out the possible reflection path and aids in the understanding of the reflected voltage signal. The reflection and transmission coefficients in the diagram are defined as follows [15]:

\[ F_1 = \text{partial reflection coefficient of a wave incident on a load } Z_1 \text{ from the } Z_0 \text{ line} \]
\[ F_2 = \text{partial reflection coefficient of a wave incident on a load } Z_0 \text{ from the } Z_1 \text{ line} \]
\[ F_3 = \text{partial reflection coefficient of a wave incident on a load } Z_2 \text{ from the } Z_1 \text{ line} \]
\[ T_1 = \text{partial transmission coefficient of a wave from the } Z_0 \text{ line into the } Z_1 \text{ line} \]
\[ T_2 = \text{partial transmission coefficient of a wave from the } Z_1 \text{ line into the } Z_0 \text{ line} \]

Figure E.3 Photograph of the line standard and its schematic representation illustrating reflected signal paths.
The above coefficient can be expressed as:

\[ \Gamma_1 = \frac{Z_I - Z_0}{Z_I + Z_0} \quad \text{Eqn. E.2 (a)} \]

\[ \Gamma_2 = \frac{Z_0 - Z_I}{Z_I + Z_0} = -\Gamma_1 \quad \text{Eqn. E.2 (b)} \]

\[ \Gamma_3 = \frac{Z_2 - Z_I}{Z_2 + Z_I} \quad \text{Eqn. E.2 (c)} \]

\[ T_1 = \frac{2Z_I}{Z_0 + Z_I} \quad \text{Eqn. E.2 (d)} \]

\[ T_2 = \frac{2Z_0}{Z_0 + Z_I} \quad \text{Eqn. E.2 (e)} \]

Referring back to the reflected voltage waveform reproduced in Figure E.2, there is no reflected voltage i.e. \( V = 0 \) in the first 0.5 nsec of the waveform. This corresponds to the \( Z_0 = 50 \Omega \) feedline. The first non-zero reflection that arrives in the trace is \( V_{\text{reflected}} = -0.54 \text{ V} \). This is due to the \(-15 \Omega \) line. Rewriting equation E.2(a), the exact characteristic impedance, \( Z_I \), of the line can be computed.

\[ Z_I = Z_0 \left( \frac{1 + \Gamma_1}{1 - \Gamma_1} \right) \quad \text{Eqn. E.3} \]

\[ = 50 \left[ \frac{1 + (-0.54)}{1 - (-0.54)} \right] \]

\[ = 14.94 \Omega \]

The computed impedance, \( Z_I = 14.94 \), is close to the target value of 15 \( \Omega \).

The next reflected signal that arrives at approximately 1 nsec into the trace is \( V_{\text{reflected}} = -0.93 \text{ V} \) and provides information about the impedance of the quarter-wave transformer that is presented to the device under test. The fixture was designed such that the output impedance presented to the DUT is approximately 4.5 \( \Omega \) at 1 GHz. In order to solve for this impedance, the partial transmission coefficients, \( T_1 \) and \( T_2 \), must first be calculated using equations E.2(d) and (e). Plugging in \( Z_0 = 50 \Omega \) and \( Z_I = 14.94 \Omega \) into those equations give \( T_1 = 0.46 \) and \( T_2 = 1.54 \). As shown in diagram of the signal paths (Figure E.3), the second reflected voltage that arrives is given by the equation:

\[ V_{\text{reflected}_2} = V \Gamma_1 + VT_1 T_2 \Gamma_3 \quad \text{Eqn. E.4} \]

Since \( V \) and \( V_{\text{reflected}_2} \) are known, and \( T_1, T_2 \), and \( \Gamma_1 \) have already been calculated, \( \Gamma_3 \) is the only unknown and can be solved for.

\[ -0.93 = 1 \times -0.54 + 1 \times (0.46)(1.54) \Gamma_3 \]

\[ \Gamma_3 = -0.551 \]

Subsequently, the impedance \( Z_2 \) can be computed from \( \Gamma_3 \) using equation E.1(c).

\[ -0.551 = \frac{Z_2 - 14.94}{Z_2 + 14.94} \]

\[ Z_2 = 4.33 \Omega \]

The resulting impedance was \( Z_2 = 4.33 \Omega \) which is slightly below the designed value of 4.5 \( \Omega \).