Process Design, Development and Fabrication of InAs Homojunction Converter Cells for Microscale Thermophotovoltaic Application

by

Karen Young-Waithe

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ABSTRACT

Two factors determine the amount of energy which can be extracted from a heat source by a thermophotovoltaic cell: the conversion efficiency of the cell, and the rate of transfer of the energy from the source to the cell. Existing thermophotovoltaic (TPV) converter cells realize efficiencies in the 17% - 24% range and approach their theoretical limit for efficiency. It has been recently predicted that the rate of power transfer may be greatly enhanced when the emitter and converter cell spacing is in the sub-micron range.

This thesis describes the realization of this prediction through process design, development and fabrication of the InAs converter cells. InAs has been chosen because of its optical properties, but relatively little is available in the published literature about the processing and handling of this material. Photolithographic processes were developed for InAs using several types of photoresists. Characteristics peculiar to InAs, such as extreme brittleness and high thermal conductivity impact on the mode of deposition, the bake temperatures, and the bake times of the photoresists.

Cr/Au and Ti/Au were used at different times as contact metallization to the InAs TPV cells and electron beam evaporation was the primary method used for metal deposition.

UV/Ozone oxidation was investigated as a viable method for passivating the InAs surface, and a model was developed in this thesis for III-V oxidation in a dry oxygen ambient. While the model uses the energy band theory for contact between two materials of different work functions, the same results may be obtained by employing the theories of chemical thermodynamics.

The method was applied to p-type InAs wafers using a sample with initial surface non-stoichiometry, evidenced in a 60/40 In/As surface ratio. Treated samples showed an In/As ratio that was close to unity, indicating that surface stoichiometry was restored by the UV/Ozone treatment. The passivation effects on the InAs cells have not yet been tried, but other sources report successful passivation using this method.

Abstract

The effects of prolonged, close-proximity exposure to a heat source were investigated, with special attention paid to the changes that might occur in the metallization structure and in the passivating oxide layer. With regard to temperature effects on metallization, analyses were made in this thesis from reports found in available literature. Based on these analyses, and the physical changes that occur in metals at elevated temperature, recommendations were made on possible ways to forestall adverse effects through careful processing. An analysis was made on temperature effects on the passivating oxide layer, based on the model developed in this thesis.

The conclusions summarize the progress made thus far in processing and fabricating InAs MTPV cells and highlight areas that require further investigation. Recommendations were made for future processing techniques.

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This page would not be complete without me paying tribute to one special person. Ma. Thanks for believing in me, Old Girl! I would like to say to my daughters Jodi and Chrystal: "Bless you for understanding that not always being around at bedtime didn't mean I wasn't there for you!" To Alyssa and Tony – hugs and kisses, this one is for you. Harry, thanks for warming my heart, and for making me smile. I am smiling.

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CHAPTER 1

INTRODUCTION

1.1 THE DEMAND FOR SUSTAINABLE ENERGY

Global energy demand is constantly on the rise. Terrestrial energy consumption escalates with population growth and increased standard of living, while fossil fuel resources diminish.

The need for an alternative energy source becomes even clearer as we seek to broaden our horizons. The last two decades show a heightened interest in deep space exploration: the Pioneer missions to Jupiter and Saturn; the Voyager explorations of Jupiter, Saturn, Uranus and Neptune; the Galileo mission to Jupiter; the Pathfinder's visit to Mars. The Cassini deep space probe is currently on its way to Saturn. Six thousand pounds of fuel is required if it is to reach its destination successfully and orbit the planet for four years. This amount of fuel is heavy, making it crucial that the rest of the

spacecraft is kept light enough for launch and travel. This imposes constraints on the size and weight of the electrical system used for powering equipment and for the general functioning of Cassini.

While highly efficient solar cells provided the bulk of the Pathfinder's power source, the efficiency of these arrays falls off rapidly with increasing distance from the sun. In order to meet Cassini's power requirements, solar arrays would have to be so large that the spacecraft as a whole would be too massive to launch. At significant distances from the sun, where solar arrays are not feasible, NASA currently uses Radioisotope Thermoelectric Converters (RTGs) as power sources.

An RTG consists of two parts: a source of heat and a system for converting heat to electricity. The heat source contains a radioisotope, such as plutonium-238, that becomes physically hot from its own radioactive decay. A thermoelectric converter converts this heat to electricity, using the Seebeck effect. The Galileo spacecraft used two nuclear generators, each 45 inches long, 16 inches in diameter and weighing 122 pounds.

Thermophotovoltaics (TPV) is a feasible alternative to thermoelectric energy sources for deep space exploration, and a suitable replacement for fossil fuel in terrestrial applications. Like thermoelectric power sources, thermophotovoltaic efficiencies do not depend on the distance from the sun.

Introduction

Thermophotovoltaic cells are almost four decades old and use the same solid-state process operating in solar cells; they both depend on the photovoltaic effect.

1.2 PRINCIPLES OF PHOTOVOLTAICS .[1, 2, 3]

The photovoltaic (PV) effect involves the direct conversion of photons to electricity and employs a *p-n* junction as a key element in achieving this conversion. In a *p-n* junction, holes diffuse down their concentration gradient from *p*-side to *n*-side, while electrons in the *n*-side diffuse over to the *p*-side. Charge carriers that cross the junction set up an electric field that acts as a barrier opposing the further flow of mobile carriers. As more carriers cross the junction, the barrier enlarges, making it increasingly difficult for additional carriers to cross. Eventually, equilibrium is established where, statistically, no more electrons or holes switch sides. This creates a fixed potential barrier at the junction, and it is this barrier that leads to the rectifying behavior of *p-n* diodes.

The photovoltaic effect is also based on the presence of this internal barrier. Once the junction is illuminated, electron hole pairs generated in the space-charge region are separated by the junction field. Excess minority carriers generated in the *p*- and *n*-quasineutral regions must diffuse to the junction, before they too can be separated by the field. Electrons lose energy by occupying lower conduction band levels in the *n*-type

material; similarly, holes lose energy by moving upwards to fill valence band levels in the *p*-type material. Figure 1.1 shows this effect for photogenerated charge carriers in a *p-n* junction.

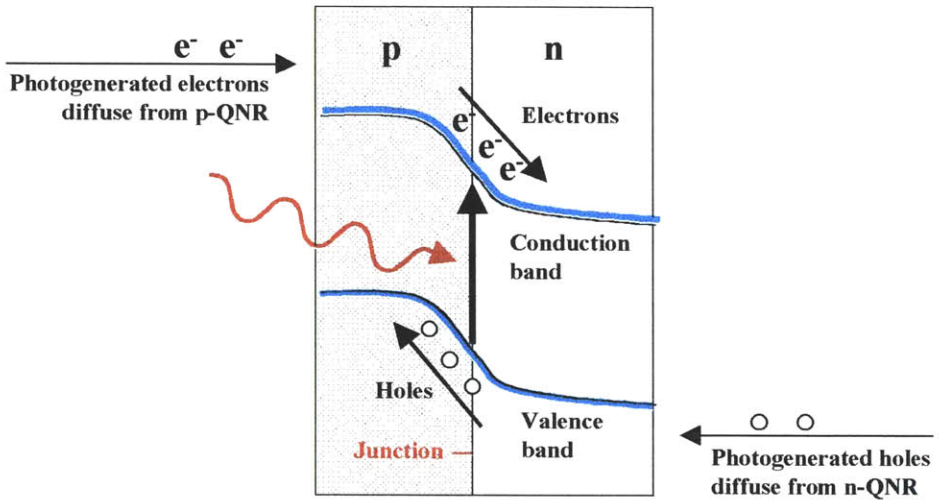


Figure 1.1: The illuminated junction: electron-hole pairs are generated. Carriers diffuse to the junction and are swept out by electric field

Carriers separate further to produce the equivalent of positive and negative battery electrodes or a photovoltaic effect. The separated charges can pass through an external resistive load connected across the potential barrier, thus transforming a portion of absorbed ionizing radiation ($h\nu > E_g$) directly into electricity.

There are several loss mechanisms. First, photogenerated carriers quickly thermalize to the edge of the band gap, losing all their energy in excess of the band gap. Second, some carriers recombine either radiatively emitting a photon or non-radiative recombination by way of impurity states before they reach the potential barrier. Eqn 1.2.1 relates the current I_L through the load to the voltage across the load

$$I_L = I_o\left\{ \left(e^{qV/kT}-1\right)+\left(e^{qV/mkT}-1\right) \right\} - I_{ph}$$

$$= I_o\left\{ \left(e^{qIR_L/kT}-1\right)+\left(e^{qIR_L/mkT}-1\right) \right\} - I_{ph} \qquad \textbf{Eqn. 1.2.1}$$

In the above expressions, I_o is the reverse dark current of the *p-n* junction; q is the charge of the electron. R_L is the load resistance (this impedance can be matched to the resistance at the maximum power point of the cell), m is the ideality factor, k is Boltzmann's constant, T is the absolute temperature, and I_{ph} is the photo generated current which would flow if the load were a short circuit. Eqn. 1.2.1 states that if the photogenerated current exceeds the dark current, power can be extracted. from the device.

1.2.1 CHARACTERISTICS IN THE ABSENCE OF ILLUMINATION

An un-illuminated, biased junction produces a current, which we will call I_{Diode}. Applying a forward bias increases the population of electron-hole pairs within the space-charge region. Recombination increases, giving rise to current, which is a sum of the diffusion current and a space charge-layer recombination-generation current.

$$I_{Diode} = I_{DIFF} + I_{RG} \qquad \textbf{Eqn. 1.2.2}$$

In Eqn. 1.2.1 above,

$$I_{DIFF} = I_o\left(e^{qV/kT} - 1\right) \qquad \textbf{Eqn. 1.2.3}$$

I_{RG} is due to recombination due to impurities in the space-charge region and is given by

$$I_{RG} = I_o\left(e^{qV/mkT} - 1\right) \qquad \textbf{Eqn. 1.2.4}$$

The recombination varies with an ideality factor *m* for which the value is around 2. In most cases, I_{RG} dominates the diffusion current, giving an ideality factor between 1 and 2, for materials with predominately non-radiative recombination. In this case, the current in Eqn.1.2.1 reduces to

$$I_L = I_o\left(e^{qV/mkT} - 1\right) - I_{ph} = I_o\left(e^{qIR_L/mkT} - 1\right) - I_{ph} \qquad \textbf{Eqn. 1.2.5}$$

If the widths of the *n*- and *p*-sides of the diode are greater than the respective minority carrier diffusion lengths L_N and L_P, then the reverse dark current is given by the Shockley equation

$$I_o = qA\left(\frac{D_N}{L_N}n_{p,o} + \frac{D_P}{L_P}p_{n,o}\right) \qquad \textbf{Eqn. 1.2.6}$$

where $n_{p,o}$ is the equilibrium concentration of minority electrons on the *p*-side of the junction and $p_{n,o}$ is the equilibrium concentration of holes on the *n*-side of the junction. On the *p*-side of the junction

$p_{n,o} = \frac{N_A}{2} + \frac{N_A}{2}\sqrt{1+\frac{4n_i^2}{N_A^2}}$,and we always have $N_A >> n_i$, so that $p_{n,o} \approx N_A$.

Assuming that Maxwell-Boltzmann statistics hold, $p_{n,o}\, n_{p,o} = n_i^2 \approx N_A\, n_{p,o}$, so that

$n_{p,o} = \frac{n_i^2}{N_A} \approx \frac{n_i^2}{p_{n,o}}$ in Eqn.1.2.6.

Similarly, on the *n*-side of the junction, $n_{p,o} \approx N_D$ and $p_{n,o} = \frac{n_i^2}{N_D} \approx \frac{n_i^2}{n_{p,o}}$. The minority carrier diffusivities and diffusion lengths may be written as

$$D_N = \frac{kT}{q}\mu_N \quad , \quad D_P = \frac{kT}{q}\mu_P$$

$$L_N = \sqrt{D_N \tau_N} \quad , \quad L_P = \sqrt{D_P \tau_P}$$

$$\frac{D_N}{L_N} = \sqrt{\frac{kT}{q}\frac{\mu_N}{\tau_N}} \quad , \quad \frac{D_P}{L_P} = \sqrt{\frac{kT}{q}\frac{\mu_P}{\tau_P}}$$

So that for minority carriers on the *p*- and *n*-side of the junction, we may rewrite the reverse saturation current as

$$I_o = An_i^2 (qkT)^{1/2}\left(\frac{1}{N_A}\sqrt{\frac{\mu_N}{\tau_N}} + \frac{1}{N_D}\sqrt{\frac{\mu_P}{\tau_P}}\right) \qquad \textbf{Eqn. 1.2.7}$$

We reiterate that this is the Shockley equation for a diode designed so that the widths of the *n*- and *p*-sides are greater than their respective minority carrier diffusion lengths L_P and L_N. In our description of the photovoltaic effect, it was pointed out that in order to generate useful photovoltage, carriers generated by photoexcitation in the *n*- and *p*-regions must diffuse to, and across the junction. As Section 1.2.3 illustrates, the ratio of the power output from a converter cell to the power into the cell increases with the number of carriers that successfully cross the junction to reach the metal contacts. This is achieved when I_o is kept low.

Equation 1.2.7 shows that I_o is a strong function of the characteristics of the material from which the converter cell is made. This equation shows that an increase in the doping concentration is one way to decrease I_o, however, over doping may reduce

carrier lifetimes as well. We also see from Eqn. 1.2.7 that I_o is small if n_i is small. For non-degenerately doped material

$$n_i^2 = N_C N_V e^{-E_g/kT} \propto m_C^{*3/2} m_V^{*3/2} e^{-E_g/kT} \qquad \textbf{Eqn. 1.2.8}$$

It seems that one should choose a relatively large E_g in order to obtain a small value for n_i and subsequently decrease I_o. There is, however, another vital point to consider. The material must be chosen based on its sensitivity to the ionizing radiation, within a given spectral range. Infrared applications with $2\mu m \leq \lambda \leq 5\mu m$ requires that E_g be small ($0.248\ \mu m \leq E_g \leq 0.62\ \mu m$). Having established a maximum E_g, Eqn.1.2.8 shows that the only other way to reduce n_i is to keep m* small. A material like InAs with its low electron effective mass and small, direct band gap (E_g = 0.36 eV at 300 K), is highly desirable.

Section 1.2.4 emphasizes that the best cell design is one that ensures that carriers generated in the *n*-and *p*-quasineutral regions will not recombine before they reach the junction. The benefits of good cell design are enhanced if the material of choice has relatively long carrier diffusion lengths. InAs with its high electron mobility (30,000 cm^2/V.sec at 300 K, compared to 1,350 cm^2/V.sec in Si[4]) is highly desirable.

1.2.2 PHOTOCURRENT

When a *p-n* junction is illuminated by photons with energies above the bandgap, electron-hole pairs are generated. This raises the electron quasi Fermi level in the *n*-type material and lowers the hole quasi Fermi level in the *p*-type. The cell becomes forward biased and current flows. The bias dependence of the photocurrent is weak and under photo-biased conditions, it is approximately the same as I_{sc}, the photocurrent at zero bias.

Figure 1.2 shows that the I-V curve for a given junction the I-V curve under illumination is the same as the "dark" curve, shifted downward with respect to the current. Short-circuit conditions occur when the load resistance $R_L = 0$ in Eqn.1.2.5, then $I_{ph} = I_{sc} = I_L$. V_{oc} can be deduced from the dark current and I_{sc}, since $I_{sc} = I_{Diode}(V_{oc})$. Under open-circuit conditions, generated photocurrent equals dark current and no current flows; $I_L = 0$ in Eqn.1.2.5.

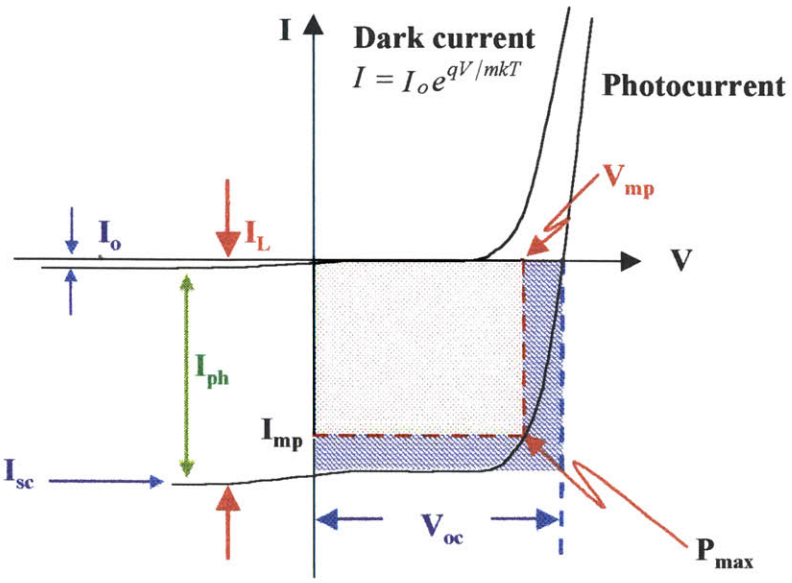


Figure 1.2: I-V characteristics of photovoltaic cell

1.2.3 EFFICIENCY

Now consider a photovoltaic cell for which the signal current flows parallel to the direction of the incident radiation of wavelength λ.

Let A be the top surface area exposed to the radiation. The maximum power generated by the photovoltaic cell with a matched-impedance load is

$$P_{out} = I_{mp} \times V_{mp} . \qquad \textbf{Eqn. 1.2.9}$$

I_{mp} and V_{mp} are the load current and load voltage at maximum power as shown in Figure 1.2.

The cell efficiency η is the ratio of the output power generated by the cell to the incident power at the front surface of the cell

$$\eta = \frac{P_{out}}{P_{in}} \qquad \textbf{Eqn.1.2. 10}$$

The incident power is

$$P_{in} = \phi_s A \frac{hc}{\lambda}(watts) \qquad \textbf{Eqn. 1.2.11}$$

ϕ_s (units of photons/cm^2*sec) is the incident flux.

From the I-V curve, the maximum efficiency is

$$\eta_{\max} = \frac{I_{mp} \times V_{mp}}{P_{in}} \qquad \textbf{Eqn. 1.2.12}$$

If we multiply through by $\frac{I_{sc} \times V_{oc}}{I_{sc} \times V_{oc}}$, it is convenient to rewrite Eqn. 1.2.12 as

$$\eta_{\max} = \frac{I_{mp} \times V_{mp}}{I_{sc} \times V_{oc}} \left(\frac{I_{sc}}{P_{in}} \times V_{oc} \right) \qquad \textbf{Eqn. 1.2.13}$$

The factor to the left is defined as the curve factor CF:

$$CF = \frac{I_{mp} \times V_{mp}}{I_{sc} \times V_{oc}} \qquad \textbf{Eqn.1.2.14}$$

which is a measure of the sharpness of the diode knee. Its value is roughly 0.8 to 0.9 for a good photovoltaic cell.

$$\eta_{\max} = CF\left(\frac{I_{sc}}{P_{in}} \times V_{oc}\right) \qquad \textbf{Eqn. 1.2.15}$$

The first term in the brackets of Eqn. 1.2.15 is governed by short-circuit conditions which occur when we set $R_L = 0$ in Eqn.1.2.5.

$$\frac{I_{sc}}{P_{in}} \rightarrow \frac{I_{ph}}{P_{in}} = \boldsymbol{R}, \qquad \textbf{Eqn. 1.2.16}$$

The cell responsivity ***R*** is a measure of the large signal response and is related to the internal quantum efficiency η_{iq} (the number of electron-hole pairs generated per incident photon) of the photocell.

The second term in Eqn. 1.2.15 is governed by open-circuit conditions; that is, setting $I_L = 0$ and $V = V_{oc}$ to obtain

$$V_{oc} = m\frac{kT}{q}\ln\left(\frac{I_{ph}}{I_o} + 1\right) \qquad \textbf{Eqn. 1.2.17}$$

The above equation implies that V_{oc} increases with the ideality factor *m*. This is not the case. I_o increases so rapidly with *m* that the maximum V_{oc} for a given I_{ph} occurs for *m*=1.

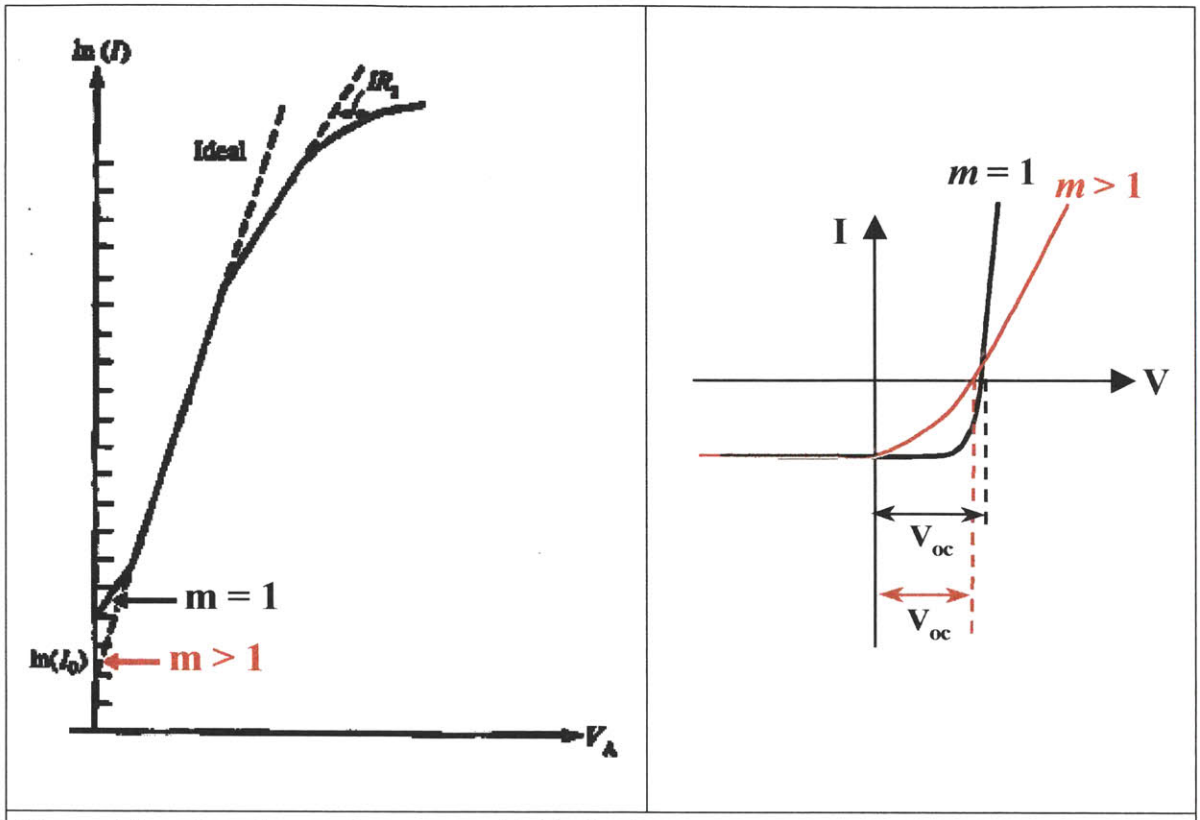


Figure 1.3: I_o and curve factor vary with ideality factor *m*.

In addition, as Figure 1.3 demonstrates, the curve factor suffers as the ideality factor increases above 1, reducing the amount of power that can be extracted from the cell.

Equations 1.2.15 through 1.2.17 indicate that there is a premium on making I_{ph} high while keeping I_o low if we want to enhance the peak conversion efficiency. There are temperature considerations: I_{ph} depends weakly on temperature, since absorption increases slightly as temperature increases. On the other hand, I_o is determined by the

availability of thermally generated minority carriers and depends strongly on temperature. Thus, V_{oc} increases with decreasing cell temperature.

1.2.4 RESPONSIVITY AND INTERNAL QUANTUM EFFICIENCY

When light impinges on the front surface of the photocell as illustrated in Figure 1.4, carriers are generated by photoexcitation. The carrier densities p and n are defined by the internal quantum efficiency η_{iq}, the photogeneration rate $A\eta_{iq}\phi_s$, the carrier lifetime τ and the cell volume V:

$$p = \frac{A\eta_{iq}\phi_s\tau_p}{V} \quad and \quad n = \frac{A\eta_{iq}\phi_s\tau_n}{V} \qquad \textbf{Eqn. 1.2.18}$$

In Equation 1.2.18, A = lw is the top surface area, d is the distance between the electrodes, ϕ_s is the photon flux that is incident upon the front surface, and the cell volume is $V = lwd$.

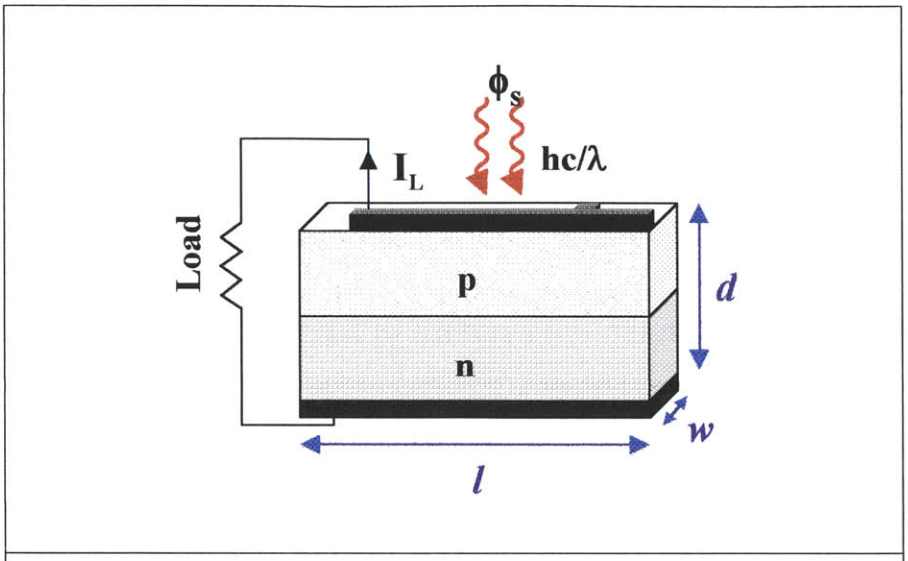


Figure 1.4: Photovoltaic cell under illumination.

When the cell is designed so that the substrate wafer forms the base of the *p-n* junction (as in Figure 1.4), the cell may be classified as a long-base diode. Minority carriers in the *p*- and *n*- quasineutral regions must diffuse to the junction, where they are swept out by the associated electric field. In Figure 1.4, minority electrons in the top layer will have their number density greatly increased due to illumination. Both the barrier region and the top surface ohmic contact are sinks for these carriers. To improve cell performance, one would seek to increase the number of photogenerated carriers that diffuse from the top epitaxial layer to the barrier. That is, on should substantially reduce the strength of the sink at the top surface ohmic contact.

The cell design in Figure 1.4 is far from optimum. Ideally, the top-surface under the ohmic contact should reflect the photogenerated minority electrons to minimize surface recombination velocity ($S_n \rightarrow 0$). A shallow high-low p^+-p or n^+-n junction serves as a reflecting surface for minority carriers by invoking the 60-mV/decade rule.

The thin n+ layer in Figure 1.5 is highly doped, so that for every order of magnitude that this doping level exceeds that of the adjacent layer, holes in the adjacent n-layer see a 60 mV reflecting barrier. To ensure that these carriers reach the junction,

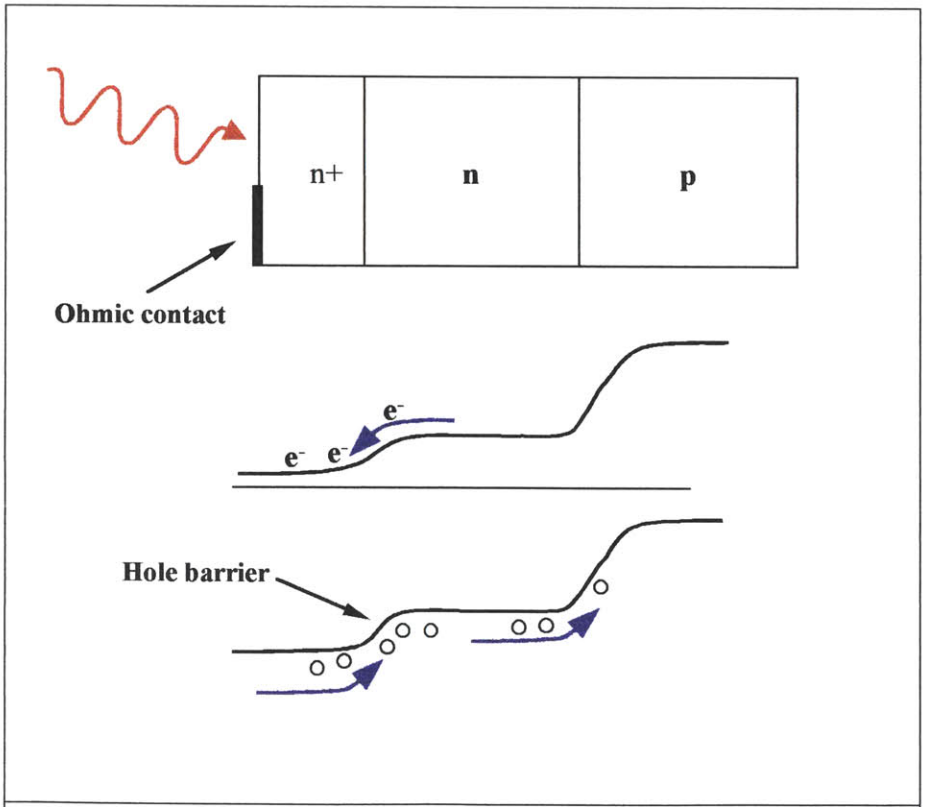


Figure 1.5: Band structure diagram demonstrates how an n^+-n high-low junction serves as a reflecting barrier to photogenerated minority holes.

we want to increase the distance over which these minority carriers diffuse without suffering recombination within the top layer. As discussed in Section 1.2.1, materials like InAs and InSb with long minority carrier diffusion lengths are highly desirable.

If we ignore impurity scattering and possible high doping effects, we may now assume that all photogenerated carriers will reach the junction. We may assume that

$$I_{ph} = qA\eta_{iq}\phi_s \qquad \textbf{Eqn. 1.2.19}$$

The responsivity at a given wavelength λ is

$$R = \frac{I_{ph}}{P} = \frac{qA\eta_{iq}\phi_s}{\phi_s Ahc}\lambda \qquad \textbf{Eqn. 1.2.20}$$

where I_{ph} is given by Eqn. 1.2.19and P is given by Eqn. 1.2.11 to give

$$R = \frac{q\eta_{iq}\lambda}{hc} \qquad \textbf{Eqn. 1.2.21}$$

The values in Eqns. 1.2.19 and ***1.2.21*** are reduced by incomplete absorption ($\lambda << E_g$ and $\lambda >> E_g$), by self-shading due to front surface contact, by optical reflectivity at the surface, by series resistance and by leakage across the junction.

1.2.5 THERMOPHOTOVOLTAICS

TPV cells generate electricity from thermal (infrared) radiation. TPV is the same solid-state process operating in solar cells, except that the source for TPV operation is

much closer, 2-3 cm, to the converter cell, and is much lower temperature than the sun, <1000 K vs. 10,000 K. The components that make up the most basic TPV systems are: the heat source, an emitting surface and an array of TPV cells. Typical TPV systems in use today are cylindrical in shape, with the emitting source at the center and the TPV converter cells along the inner surface of the cylindrical shell. This coaxial design is not new; Bruce Wedlock proposed a similar system in 1963.[5]

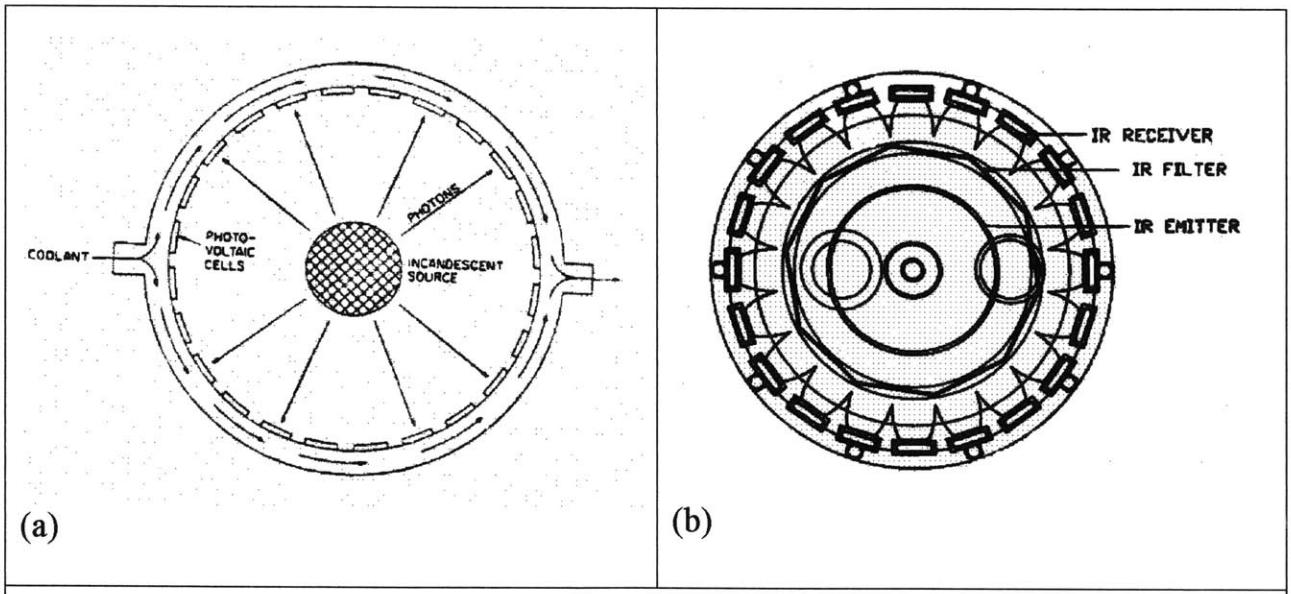


Figure 1.6: (a) Coaxial TPV converter geometry (Wedlock 1963), (b) Converter cell 1993[6]

Measured conversion efficiencies in TPV cells have climbed from 4.23% reported by Wedlock in 1963 to today's reported values of 17% - 24%. These efficiencies are remarkably close to the theoretical limit. The obvious question then is: How can we improve the power output from a TPV cell? Two factors determine the amount of energy

that can be extracted from a heat source by a thermophotovoltaic converter cell: the conversion efficiency of the cell, and the rate of transfer of energy from the source to the cell. Recent investigations into the effects of small emitter-converter cell spacing promise a significant increase in the rate of transfer of energy from source to cell, as will be described in the next chapter.

This work focuses on the process development and fabrication of InAs converter cells suitable for MTPV application. Since relatively little has been published in the open literature about the processing of InAs, a full process has been developed, including photolithography, chemical processing, metallization, and surface passivation. The application of a heat source at spacings as low as 0.2 μm poses new challenges in terms of controlling surface roughness and addressing possible temperature effects. Finally, in Chapter 6, recommendations are made with regard to additional process parameters that may improve device performance.

CHAPTER 2

MICROSCALE THERMOPHOTOVOLTAICS

2.1 ENHANCED RADIATIVE INTENSITY TRANSFER

In 1996, R.S. DiMatteo first explored the potential benefits of "microscale" radiative transfer.[7] In 1997, M.D. Whale introduced the concept of microscale thermophotovoltaic devices, which would make use of small emitter-converter spacing and subsequent radiation tunneling effects to significantly increase power transfer.[8] In 2000, J.L. Pan and K.H. Choy investigated and modeled radiation-tunneling phenomena to yield some interesting results.[9]

Pan and Choy found that when an object was brought very close to a blackbody emitter, the maximum transferred radiated heat intensity is given as n^2 times the free space Planck distribution.

$$p(\lambda,T) = n^2 * \frac{2\pi h c^2}{\lambda^5} \frac{1}{e^{hc/\lambda kT} - 1} \qquad \text{Eqn. 2.1.1}$$

Here, n is the smaller of the two indices of refraction of the blackbody emitter (BB) and the object (TPV cell). This increased radiative transfer is due to the optical or radiation tunneling effect that may be realized by approaching a high index medium to an evanescent field, allowing the conversion of the evanescent field to a propagating wave. This close-proximity effect is the basis for microscale thermophotovoltaics, and offers a distinct advantage over current TPV operation.

As Figure 2.1 illustrates, recombination centers within the black body emit infrared radiation that is incident upon the front surface at various angles. We will use the surface normal as the zero point of reference, so that radiation at normal incidence on the surface of the black body is at an angle $\theta_i = 0$ with respect to the surface normal. Rays at normal incidence within the blackbody will undergo maximum transmission, with almost no reflection. These rays will propagate into the adjacent medium, which in this case, is air, having an index of refraction $n_{air} < n_{BB}$. Rays at other angles of incident will be reflected, to some degree, back into the black body. As incident angle increases, transmission decreases until *total internal reflection* occurs for those rays incident at critical angle θ_c.

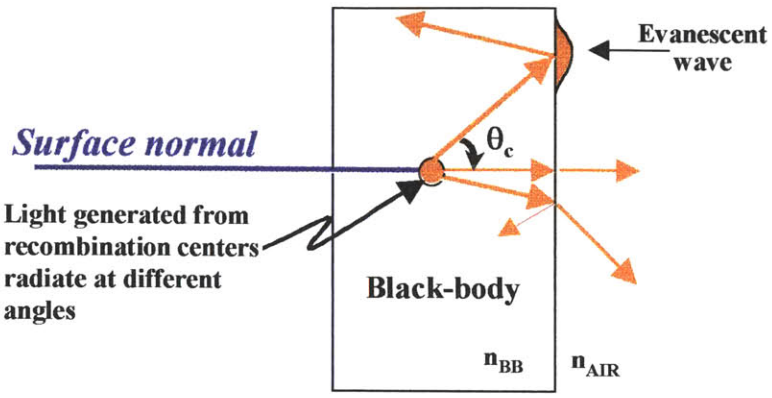


Figure 2.1: Light rays impinge upon the black body surface at different angles of incidence. Incident rays at angles less than θ_c undergo partial transmission and reflection, with total internal reflection occurring at θ_c.

All light rays impinging upon the black body at the critical angle defined by

$$Sin(\theta_c) = \frac{n_{air}}{n_{BB}} \qquad \text{Eqn. 2.1.2}$$

will be reflected back into the black body. Even though the total internal reflection is indeed total for $\theta_i \geq \theta_c$, electric and magnetic fields penetrate into the adjacent material, and an evanescent wave is created in the adjacent medium as long as $n_{BB} > n_{medium}$, as is the case when the medium is air. The field strength decreases rapidly with distance from the boundary, with the electric field falling practically to zero within a few wavelengths of the interface. Figure 2.2b shows that when another object, having an index of

refraction greater than air, is brought very close to the black body, the evanescent wave becomes a propagating wave in the third medium due to radiation tunneling. At distances comparable to those employed in TPV operation, only radiation incident angles $\theta_i < \theta_c$ will be transferred to the TPV cell. Even then, special configurations must be employed

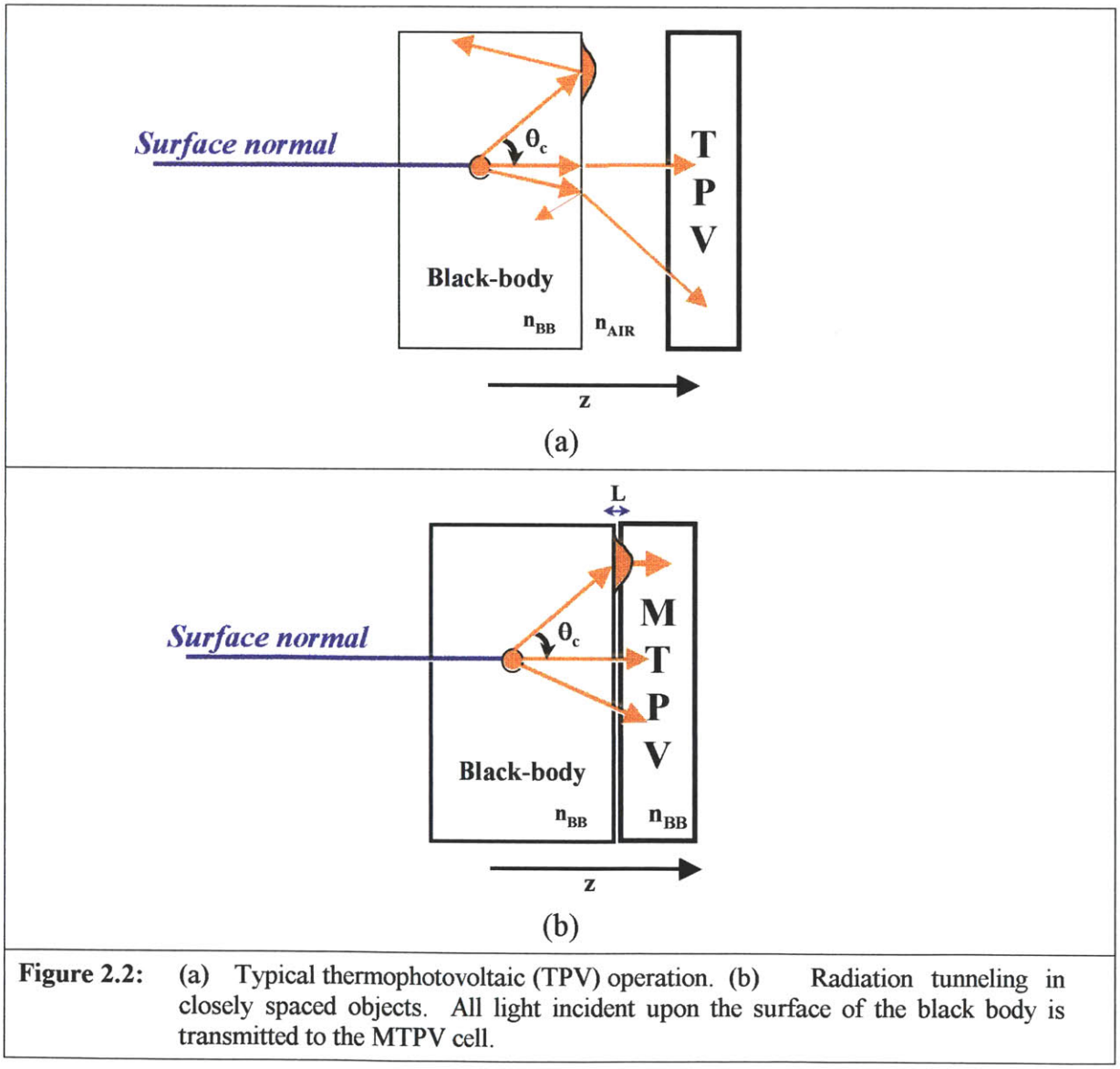


Figure 2.2: (a) Typical thermophotovoltaic (TPV) operation. (b) Radiation tunneling in closely spaced objects. All light incident upon the surface of the black body is transmitted to the MTPV cell.

to ensure that multiple beam interference does not reduce the amount of light reaches the cell under macroscale spacing.

While Figure 2.2 illustrates how the transfer from black body to TPV cell is greatly enhanced at small emitter/cell spacings, it does not explain what makes this phenomenon possible, nor does it explain the variation of this transfer with distance.

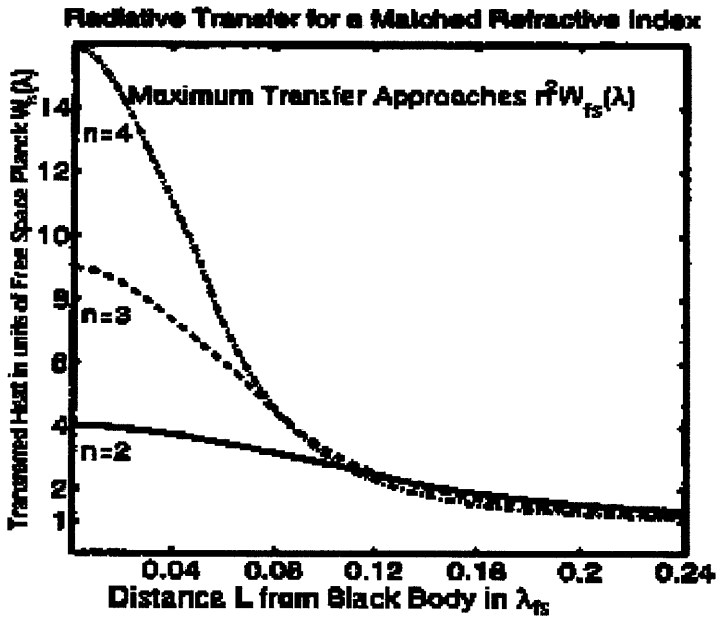


Figure 2.3: Radiative Transfer for a Matched Refractive Index,[5] $n_{TPV} = n_{BB}$.

Pan and Choy determined that corresponding to a range of incident angles for which $\theta_c \leq \theta_i \leq \pi/2$, there are n^2_{BB} optical modes within the black body, and that these modes are evanescent within the medium outside the black body. Transfer is limited by

propagation along n^2 available modes when the cell is extremely close (at a distance below the skin depth of the cell material) to the blackbody. In Figure 2.3, λ_{fs} is the free space wavelength of the radiation and the variation of this transfer with emitter/cell spacing L is given by the relation

$$L < \frac{\lambda_{fs}}{2n_{TPV}\pi} \qquad \textbf{Eqn. 2.1.3}$$

When $n_{BB} \geq n_{TPV} = n_{InAs} = 3.5$, an emitter/cell spacing of $L < 0.045\ \lambda_{fs}$ gives a maximum transfer of 12.25 times the free space Planck distribution. This value is 12.25 greater than the maximum transfer that can be realized in a perfectly designed macroscale TPV system. This formula states that for an incident wavelength of $\lambda_{fs} = 2\mu m$, an emitter/cell spacing of $L < 0.09\ \mu m$ is necessary for maximum transfer, and a spacing of $L < 0.23\ \mu m$ is required for $\lambda_{fs} = 5\ \mu m$. If one were to increase the spacing from $L < 0.045\ \lambda_{fs}$ to $L < 0.08\ \lambda_{fs}$ (0.16 μm spacing for $\lambda_{fs} = 2\ \mu m$, and 0.4 μm spacing for $\lambda_{fs} = 5\ \mu m$), then from Figure 2.3, the radiative transfer would drop to approximately 5 times the free space Planck distribution. This value is still significantly higher than one could possibly achieve outside of the microscale regime.

A review of the photovoltaic effect in Section 1.2 shows that the conversion efficiency of a TPV cell increases with the amount of power that can be extracted from

that cell. Specifically, Equation 1.2.13 shows that the output power is proportional to the product of the open-circuit voltage and the short-circuit current. While the open-circuit voltage does not vary much with light intensity, the short-circuit current increases with increasing radiative intensity. As shown in the previous discussion, microscale thermophotovoltaics promises an increase in the amount of power that can be extracted from a TPV cell.

Chapter 1 addressed the demand for sustainable energy and introduced the Radioisotope Thermoelectric Generator (RTG) as the most reliable source of power available today for deep space probes. This system performs where solar cells fail, at distances far away from the sun's rays. Like thermophotovoltaics, RTGs consist of a heat source and a system for converting heat to electricity. The main difference is that RTGs convert heat via a thermoelectric converter, which is basically a junction consisting of two different wires. A thermal electromotive force or Seebeck voltage is generated from the diffusion of electrons across this junction when the two wires are maintained different temperatures.

Semiconductors appear to be more efficient thermoelectric converters than metals, since the Seebeck coefficient is 1000 times larger in these materials than in metals. However, high temperature gradients must be maintained in order to generate a significant Seebeck voltage. It is difficult to find a semiconductor material with all the

desired properties – large enough band gap, low thermal conductivity, high Seebeck coefficient, and high carrier mobility – to create an efficient thermoelectric converter. For these reasons, efficiency remains at a low 5% - 10%, values that have not changed since the early 1960s.[10]

2.2 DISCUSSION

The Radioisotope Thermoelectric Generator (RTG) is reliable power source for deep space exploration, mainly because it converts waste heat from a constant source to electricity. While reliability is high, RTG conversion efficiencies remain low, at values that have not exceeded the 10% range for over four decades. The solar cell has proved to be a more efficient source of power, but the output from these cells diminishes greatly at increasing distances from the sun.

Thermophotovoltaic (TPV) cells have two important advantages over solar cells. First, the TPV cell offers the same reliability as the RTG, since power is generated from a constant heat source. Second, although radiation from the sun is more energetic than infrared radiation, the total power incident on a TPV cell is actually greater than that for a solar cell. This is because the TPV cell can be positioned just a few centimeters from a

radiant source, whereas the sun is about 130 million kilometers away. Current TPV efficiencies rival those of the most "high efficiency" solar cell.

Microscale thermophotovoltaic (MTPV) technology combines the reliability of the RTG and TPV cell with the compactness of the solar cell. Moreover, MTPV promises that its unique proximity effect facilitates the transfer of more power into the cell, thereby allowing significantly more power to be extracted. For these reasons, MTPV is a more attractive alternative to the RTG for deep space applications.

CHAPTER 3

PROCESS DEVELOPMENT

InAs is the material of choice for the fabrication of MTPV cells because of its optical properties. As mentioned in Chapter 1, its high electron mobility and low effective mass are some of the characteristics necessary to ensure that the maximum power can be extracted from the TPV cell. A narrow energy band gap of 0.36 eV makes this material suitable for applications in the infrared, specifically for radiation with a bandwidth in the $2\mu m \leq \lambda \leq 3.5\mu m$ range.

As discussed in the previous chapter, it is the free space wavelength of the incident radiation, as well as the refractive index of the cell material that prescribes the emitter/cell spacing that yields maximum power transfer. Emitter/cell spacings must be as small as 0.2 μm in order to observe the effects of radiation tunneling at the spectral range that matches the InAs energy band gap. In an effort to achieve these sub-micron

spacings, an experimental set-up similar to the one depicted in Figure 3.1 was designed and implemented by MIT MTPV group collaborators at Charles Stark Draper Laboratory. A piezoelectric stage serves to position the heater chip in close proximity to the TPV cell.

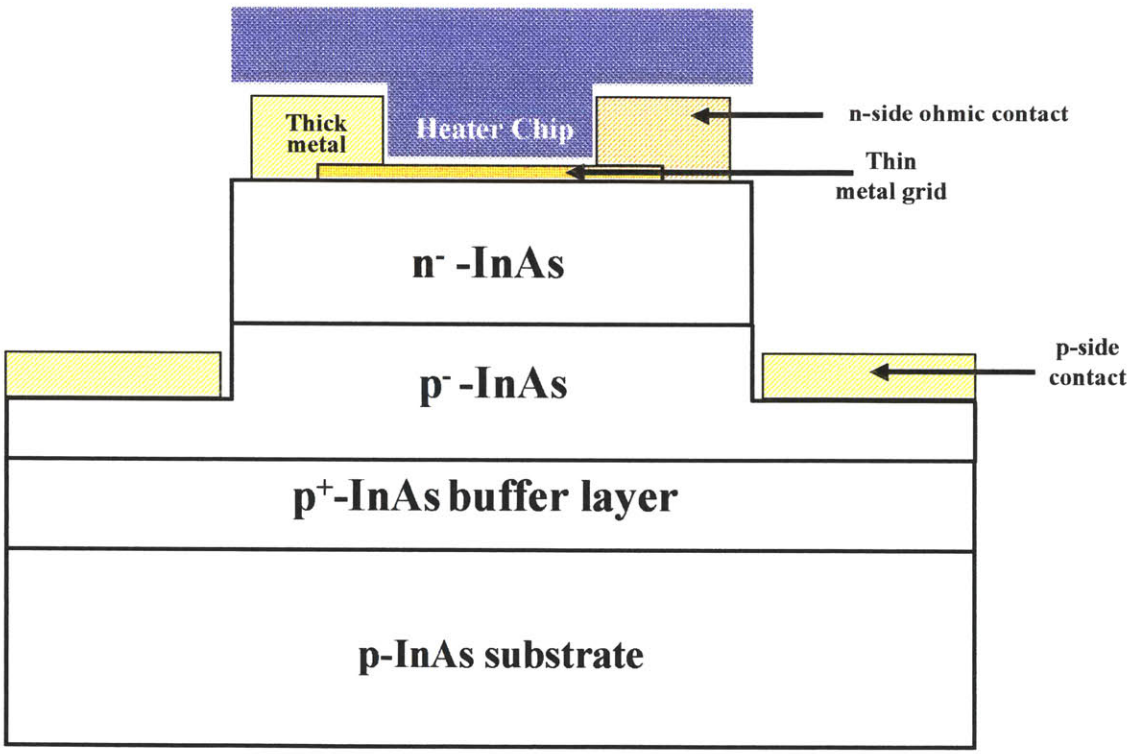


Figure 3.1: Experimental set-up for optical measurements. Wafer flatness is crucial if sub-micron emitter/cell spacings are to be realized.

The close proximity operation described above raises concerns for wafer flatness, a topic that will be addressed in Section 3.1. Device design and structure are discussed in

Sections 3.2 and 3.3. Specifically, Section 3.2 shows how the cell structure proposed in Section 1.2.4 is achieved by epitaxial growth, while Section 3.3 describes the cell parameters that govern the process flow for device fabrication. From the layout described in this section, we take note that the front contact metal is the feature that comes into closest proximity to the emitter cell (see Figure 3.1) and all care must be taken during the metallization step to ensure that surface roughness in this metal is minimized.

Section 3.4 describes the development of processes such as wet etching, photolithography and metallization. In Section 3.4.1, wet etchants for InAs have been identified and etch rates have been calibrated for those solutions that allow for better control over the etch. Issues surrounding the development of a photolithographic process for InAs are discussed in detail in Section 3.4.2, while Section 3.4.3 describes the metallization process, discussing specific advantages that one metal scheme may offer over another.

3.1 WAFER FLATNESS

Section 2.1 emphasizes how crucial it is that the substrate wafer be relatively flat, or piecewise flat if the benefits of MTPV are to be achieved. The surface of one quarter

of an InAs wafer was characterized, to determine whether it was indeed possible to fabricate devices on this substrate for close proximity operation. The surface profile was analyzed using a WYKO Phase Shift Interferometer, which measures surface roughness within 1 nm accuracy.

Figure 3.2 is a spatial contour map of a 1cm x 1 cm InAs sample, and the topology shown here is taken to be indicative of the topology of the entire wafer. The X-profile follows the terrain along the horizontal yellow line, while the Y-profile maps out the surface topography along the vertical yellow line.

The Y-profile indicates that some degree of bowing exists across the wafer. However, the heights corresponding to each contour is indicated in the color key below, and a comparison of the numbers shows that the highest points in one contour varies from the lowest point on an adjacent contour by approximately 10 nm. Such small topographical variation shows that there are no drastic fluctuations in the shape of the surface, indicating that the bowing is gradual, and the wafer surface is universally flat. The solid white box on the contour map outlines area of approximately 3.0 mm x 3.0 mm where the highest degree of flatness occurs.

A small degree of surface micro-roughness is also evident in the Y-profile. It is uncertain whether this feature is an artifact of the equipment or if it is indicative of true surface roughness. The small-scale variation indicated here is approximately 5 nm, and

is well within tolerable limits for MTPV operation. Upon physical examination of the wafer, the surface was found to be shiny, indicating that the wafer surface is flat to a fraction of wavelength of visible light.

This confirms that devices may be fabricated on these wafers for close proximity operation; however, further measures must be taken during processing to minimize any topographical variation that might occur in the area of closest contact.

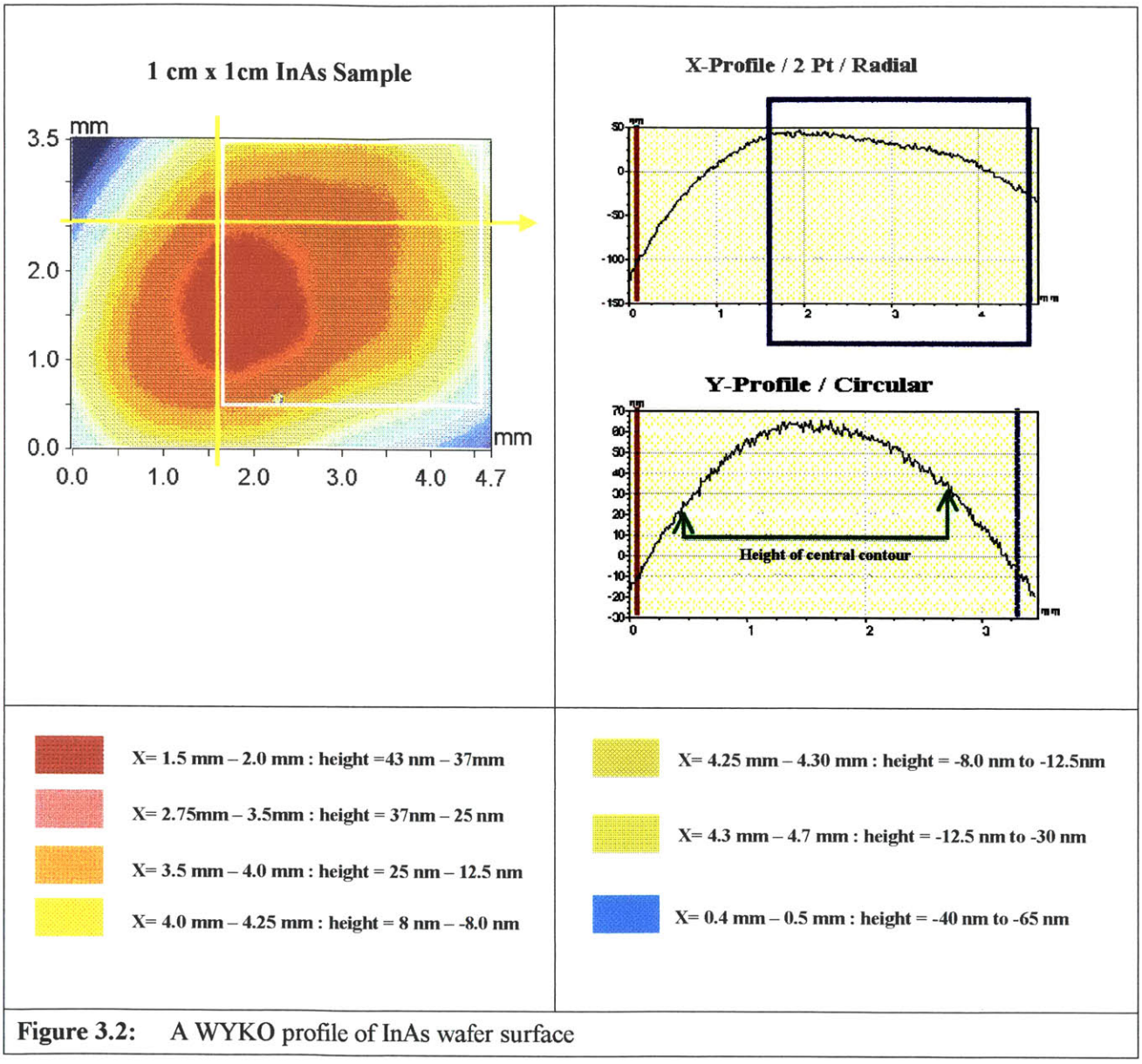


Figure 3.2: A WYKO profile of InAs wafer surface

3.2 DEVICE STRUCTURE

As discussed in Section 1.2.4 and depicted in Figure 1.5, a shallow n^+-n junction serves as a reflecting surface to minority carriers, thereby reducing the surface recombination velocity. This ensures that excess carriers generated near the surface will make it to the junction, where they are swept out by the junction field. Similarly, the p+ buffer layer prevents electrons generated in the p-region from diffusing into the bulk where they would be lost.

Again, InAs was chosen because its low carrier effective mass, high carrier mobility and long carrier diffusion lengths ensure that more excess minority carriers generated outside of the space-charge layer will reach the junction and contribute to the generation of useful photocurrent.

A device structure was designed with these material properties and specifications in mind, and MBE growth was carried out by Henry Choy and Michael Masaki using the Fonstad Group's facilities located in Building 13 at the Massachusetts Institute of Technology. The cross-section of a typical heterostructure is shown in Figure 3.3. Beryllium was used as the *p*-dopant, while Si was used to dope the *n*-side. The actual doping concentrations and the quality of the metallurgic junction must be determined empirically during the characterization process.

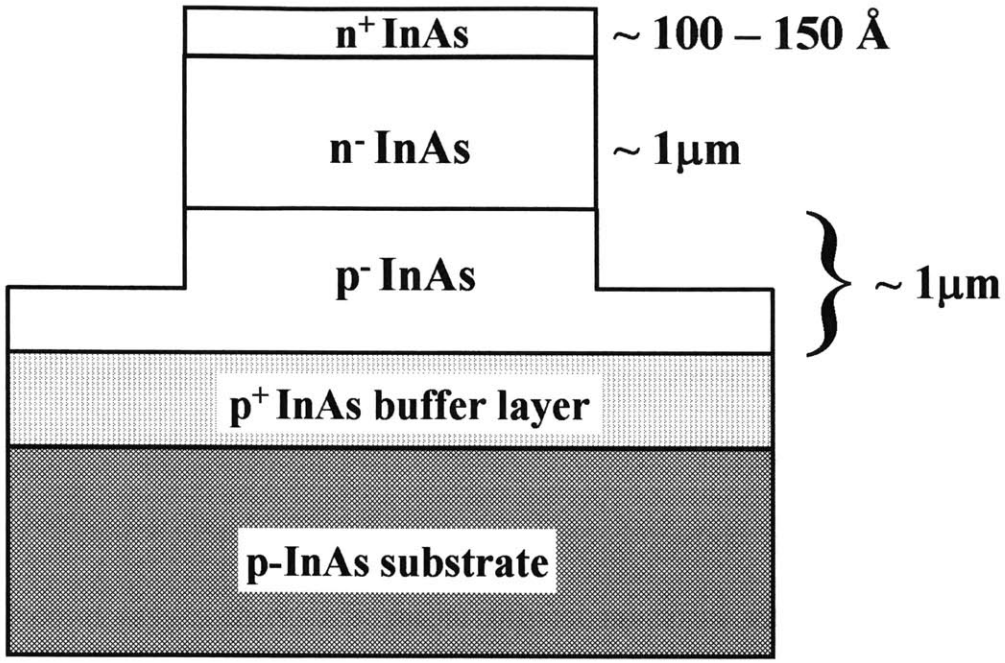


Figure 3.3: InAs p-n junction is shown with the expected doping profile and layer thickness after the junction is isolated by wet etching.

3.3 THE MASK SET

The mask set in Figure 3.4 was developed at Draper Laboratory, and was used to fabricate the MTPV cells described in the previous section. A more complex design was developed for the processing of these devices, but due to time constraints, this somewhat simpler mask set was designed in an effort to eliminate some of the processing steps. The process parameters developed here will be used in the future to fabricate more complex structures, the details of which will be described at the end of this chapter.

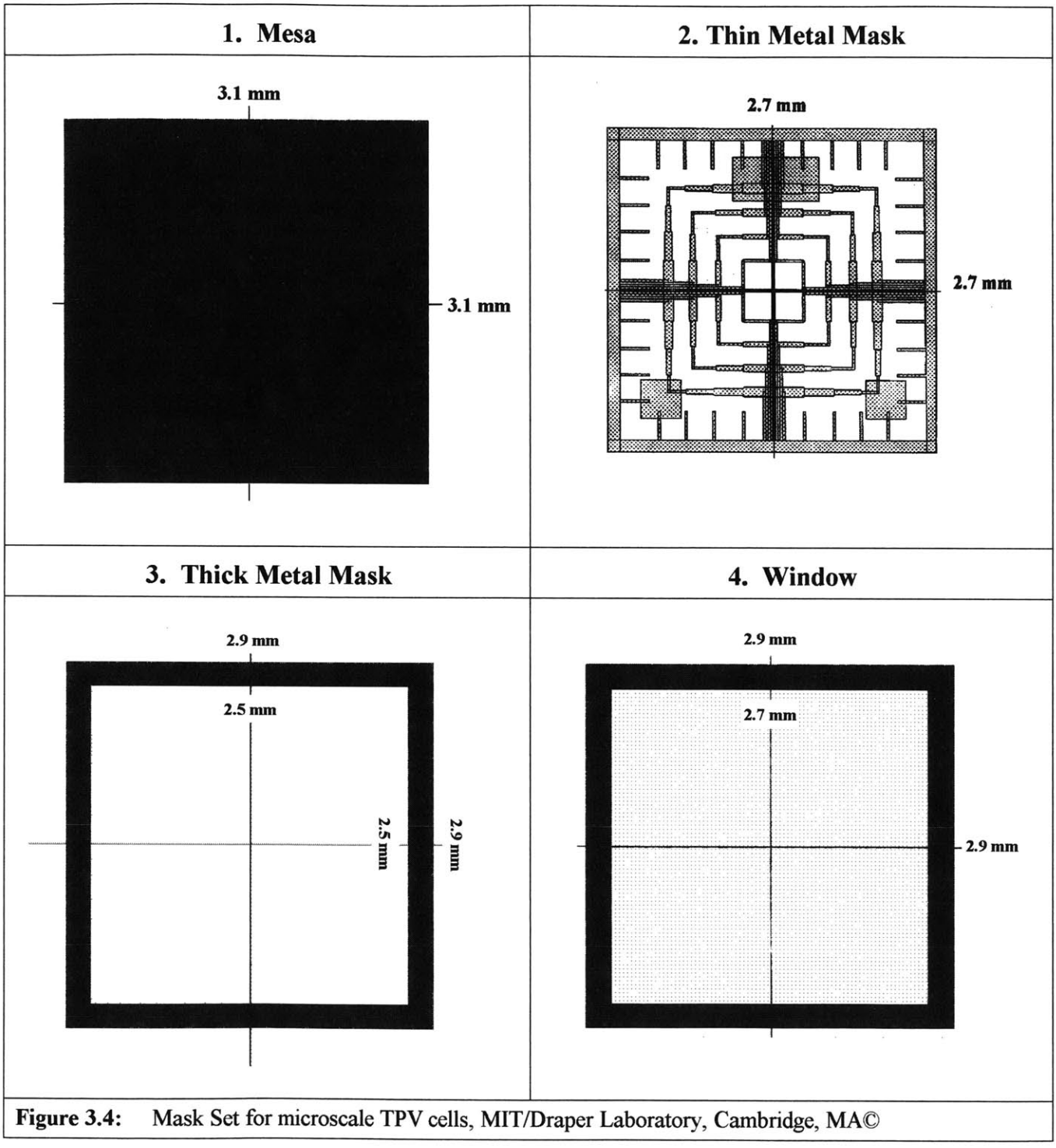


Figure 3.4: Mask Set for microscale TPV cells, MIT/Draper Laboratory, Cambridge, MA©

The set consists of four masks to be used as follows:

Mask #1 is a clear field mask for use with positive resist. After the photolithographic step, the patterned resist was used as an etch mask for junction isolation as shown in Figure 3.1.

Mask #2 is a dark field mask for use with image reversal; the smallest feature size is 20 μm. This mask was used to pattern areas on top of the mesas for deposition of a thin metal layer of approximately 600 Angstroms thick. Mask #2 defines the metal layer that will be brought into close proximity with the emitter.

Mask #3 is a dark field mask for use with image reversal. This mask is used to pattern a perimeter around the thin metal for deposition of a 0.5 μm thick, 0.4 mm wide metal layer. This metal ring has a 0.2 mm overlap with the thin metal to ensure good electrical contact between the two metal layers.

Mask #4 is clear field, for use with positive resist. This mask will be used after a passivating dielectric is deposited on the surface of the wafer, Mask #4 will then be used to for a photolithographic step. The patterned photoresist will be used as an etch mask to open up a window in the passivation layer where the heater chip can be brought close to the InAs TPV cell as shown in Figure 3.1.

A detailed process flow is given at the end of this chapter, and includes the parameters developed in the following sections.

3.4 PROCESSING

Relatively little is published in the open literature about the processing of InAs. Process parameters including etch compositions, etch rates, and photolithography were developed. The photolithographic step required modification of existing process parameters for silicon. Since silicon and InAs have distinctly different optical and transport properties, characteristics like surface reflectivity and thermal conductivity were investigated, analyzed and compared before suitable adjustments could be made to the existing silicon process, to produce a good workable process for the InAs.

While the metal was deposited using standard electron beam evaporation, variations to the metallization step were made in an effort to achieve good adhesion and to minimize surface roughness in the thin metal layer.

3.4.1 ETCHANTS AND ETCH RATES

Most of the references on wet etchants date back to the period 1959 – 1962, with etch rates given in $g/m^2/sec$. Etch rates were calibrated for the most uniform of the

etchants found, while the more complex solutions like HNO_3:HF:CH_3COOH:Br_2 and HNO_3: H_2O_2:$C_4H_6O_6$ remain untested because they proved difficult to handle. A list of wet etchants for InAs is tabulated in Table 3.1.

Table 3.1: Etchants and etch rates

Etchant	Proportion	Etch Rate	Profile
H_3PO_4 : H_2O_2 : H_2O [11]	2:1:8 or 2:1:10	0.016 μm/s	Uniform
H_2SO_4:H_2O_2:H_2O [12]	1:1:20	0.13 μm/s	Non-uniform
HCl:H_2O [13,14]	1:10	-	Non-uniform
HNO_3:HF:CH_3COOH:Br_2 [15,16]	75:15:15:0.06 (at 55 °C) 5:3:3:0.06 (aka CP-4)	-	Not tested
H_2O_2: HF: H_2O	1:1:4	-	Non-uniform
HNO_3: H_2O_2:C_4H_6O6 [17]	1:1:6	-	Not tested

All etchants listed are exothermic when mixed, making the etch rapid, non-uniform and difficult to control. These characteristics are even more pronounced in etchants like Piranha (H_2SO_4:H_2O_2:H_2O) and HCl, which tend to preferentially etch one component of the III-V compound much faster than the other. Because of this property, diluting these etchants to cool them down did not slow down the etch rate to a more controllable range. Figure 3.5 shows the data from a surface profilometry measurement

on an InAs sample after a 5 minute etch in 1:10 HCL:H_2O. In this figure, the horizontal scale is in μm, while the vertical scale is given in kilo-Angstroms. The intent was to etch the area extending from 0 to 600 μm on the horizontal scale, in an effort to define the mesa that extends horizontally to the right of the 600 μm line. The etch is rate fast, approximately 3 μm/minute, and the etch profile is rough, as evidenced by a 4-5 μm depth variation in the area extending to the left of the 600 μm line.

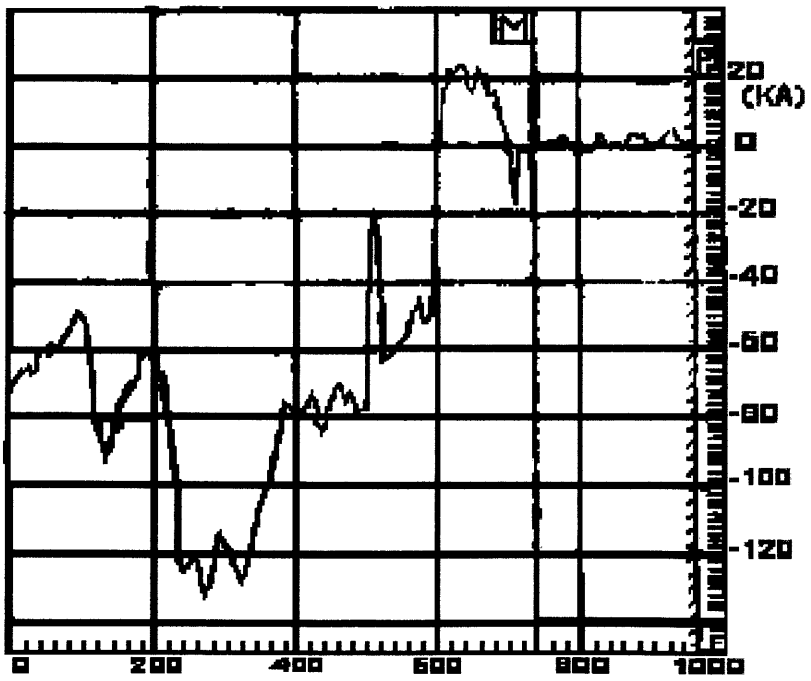


Figure 3.5 InAs etched 5 minutes in 1:10 HCL:H_2O. The horizontal scale is given in μm, while the vertical scale is in kilo-Angstroms. The etch was performed in the area extending 0 to 600 μm on the horizontal scale, while the mesa area extends to the right of the 600 μm line.

The more dilute phosphoric acid etch (2:1:10 H_3PO_4 : H_2O_2 : H_2O) tends to be the most uniform of all the etchants, with the hydrogen peroxide acting as a "smoother" to slow down the etch. Better profiles and slower etch rates were observed when the etchant was allowed to cool for a few minutes before introducing the substrate. The best profiles were obtained when the etch was performed with the etchant submerged in a water bath. The additional cooling effect resulted in even smoother profiles and allowed better control over the etch rate.

Figures 3.6 and 3.7 show etch profiles resulting from two different etches using a concentration ratio of 2:1:10 H_3PO_4 : H_2O_2 : H_2O. For both figures, the horizontal scale is given in μm, while the vertical scale is calibrated in Angstroms. The profile in Figure 3.6 is produced from etch described above, for which the solution was allowed to cool for 6 minutes after mixing. The beaker then was immersed in a water bath and the sample was etched for 95 seconds, for a target etch depth of 1.5 μm. However, this solution was inadvertently mixed with expired hydrogen peroxide, and resulted in a grossly exaggerated etch – at 6.5 μm, the actual etch depth is about four times the target value. The entire mesa is shown in the figure, emphasizing a roughness of 0.5 – 1 μm along the top surface.

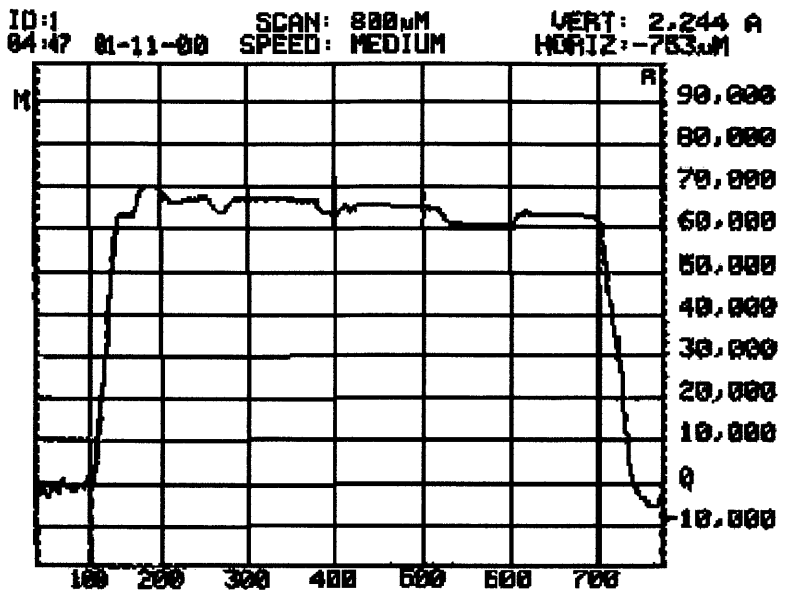


Figure 3.6: InAs mesa etched in 2:1:10 H_3PO_4:H_2O_2:H_2O for 95 seconds. The target etch depth is 1.5 mm, but this is the result when expired H_2O_2 was inadvertently used. The horizontal axis is measured in microns, the vertical axis in Angstroms.

When the junction was etched with a phosphoric acid solution containing active H_2O_2, the results were markedly different. In this case, the desired etch depth was achieved under the same conditions and times mentioned above. The resultant etch profile, shown in Figure 3.7, is smoother and the etch rate is markedly slower. The top of the mesa, extending horizontally along the 16,000 Angstrom line, and to the left of the 260 μm line, shows almost no variation along the surface.

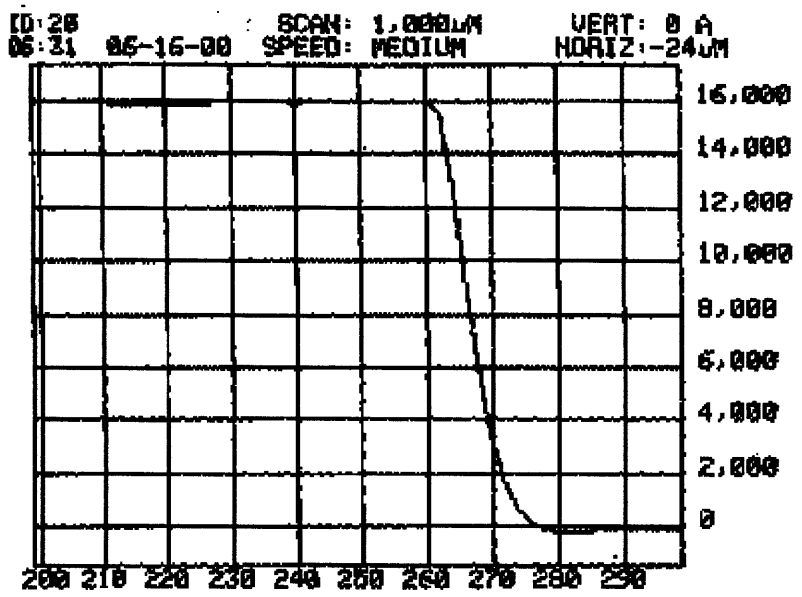


Figure 3.7: InAs mesa etched in Phosphoric Acid solution containing active hydrogen peroxide. The horizontal axis is measured in microns, the vertical axis in Angstroms.

3.4.2 PHOTOLITHOGRAPHY

InAs samples were patterned for metallization and etching at MIT's Technology Research Laboratory (TRL). Because InAs is very brittle, certain modifications were made with regard to the basic handling of the substrate in an effort to eliminate excessive breakage of the samples. Before spin coating on TRL's Solitec Coater, InAs samples were mounted onto 2" silicon carrier wafers. The samples remained mounted throughout subsequent process steps.

3.4.2.1 PHOTORESIST: Exposure and Development

The photolithographic process was first run with different resists -- OCG825-20 positive resist, AZ5214E image reversal and AZ P4620 thick positive resist -- on silicon samples before introducing the process to the InAs samples. Subsequent InAs processing adhered to prescribed times and temperatures.

It is noteworthy that OCG825-20 and AZ5214E on silicon will develop in roughly 90 seconds after exposure; on InAs, however, the same process does not yield a noticeable pattern even after 6 minutes in the developer. This was first thought to be a surface reflectivity problem. UV light acts on the resist as it is transmitted from the source, and once again as it makes a round-trip through the polymer subsequent to reflection from the substrate surface. It was assumed that the InAs surface reflected less light back through the resist than did silicon, and that the problem could be corrected by increasing the exposure time. Increased exposure times yielded a noticeable pattern on the InAs, but only after a minimum of 15 minutes in the developer.

The next step was to obtain a plot of the surface reflectivity as a function of the frequency of the incident radiation. For all materials, the reflectivity R is at unity at low frequencies, then falls off rapidly at the plasma frequency ω_p, and reaches zero at some frequency which we call ω_o. The reflectivity climbs again after ω_o, but only slightly, to

approach a constant value in the high frequency (UV) part of the spectrum. A comparison of the surface reflectivities will serve to clarify whether the need for longer exposure times is related to a difference in surface reflectivity, and what course of action should be taken to rectify the condition.

Using optical properties for these materials – band structure, complex dielectric constant, and carrier mobilities – electron and hole conductivities were calculated, and these values were used to calculate the plasma frequencies of silicon and InAs. Once a value for the plasma frequency is known, we can calculate the frequency ω_o, and a plot of the reflectivity versus frequency can be generated.

Starting with an expression for the real part of the dielectric constant ε_{core} at plasma frequency yields the relation

$$\omega_p^2 = \frac{4\pi\sigma_o}{\varepsilon_{core}\tau} - \frac{1}{\tau^2} \qquad \textbf{Eqn. 3.4.1}$$

where σ_O is the total electron and hole conductivity: $\sigma_O = \sigma_c(0) + \sigma_{lh}(0) + \sigma_{hh}(0)$. τ is the relaxation time, or the mean time between collisions, as the charge carriers scatter off ion cores within the lattice.

Since silicon has an indirect band gap with elliptical pockets,

$$\sigma_{c(0)} = \frac{ne^2\tau}{3}\left(\frac{1}{m_l} + \frac{2}{m_t}\right) \qquad \textbf{Eqn. 3.4.2}$$

m_l and m_t are the longitudinal and transverse electron masses.

For a direct bandgap material such as InAs,

$$\sigma_{c(0)} = \frac{ne^2\tau}{m_c^*} \qquad \textbf{Eqn. 3.4.3}$$

For both materials, the hole conductivities are given as

$$\sigma_{lh(0)} = \frac{n}{1+2\left(\frac{m_{hh}}{m_{lh}}\right)^{3/2}}\frac{e^2\tau}{m_{lh}} \qquad \textbf{Eqn. 3.4.4}$$

$$\sigma_{hh(0)} = \frac{n}{1+\frac{1}{2}\left(\frac{m_{lh}}{m_{hh}}\right)^{3/2}}\frac{e^2\tau}{m_{hh}} \qquad \textbf{Eqn. 3.4.5}$$

For both InAs and silicon, the relaxation time τ is calculated from

$$\tau = \frac{m_c^*\mu_e}{q} \qquad \textbf{Eqn. 3.4.6}$$

Values for the dielectric constant ε_{core} were obtained from standard texts and Equation 3.4.1 was solved using the values obtained from Equations 3.4.1 through 3.4.6.

Next, the frequency ω_o was calculated, noting that the reflectivity R = 0 at $\omega = \omega_o$, with

$$\omega_o = \frac{\omega_p}{\sqrt{1 - \frac{1}{\varepsilon_{core}}}} \qquad \textbf{Eqn. 3.4.7}$$

For frequencies higher than ω_o, we note that

$$R = \left(\frac{1 - \sqrt{\varepsilon_{core}}}{1 + \sqrt{\varepsilon_{core}}} \right)^2 \qquad \text{as } \omega \rightarrow \infty \qquad \textbf{Eqn. 3.4.8}$$

These equations yield

$\omega_p(Si) = 5 \times 10^{12}$ Hz

$\omega_o(Si) = 5.2 \times 10^{12}$ Hz

R(Si) = 0.3 for $\omega \rightarrow \infty$

$\omega_p(InAs) = 2.26 \times 10^{12}$ Hz

$\omega_o(InAs) = 2.34 \times 10^{12}$ Hz

R(InAs) = 0.3 for $\omega \rightarrow \infty$

The results are plotted in Figure 3.8 below.

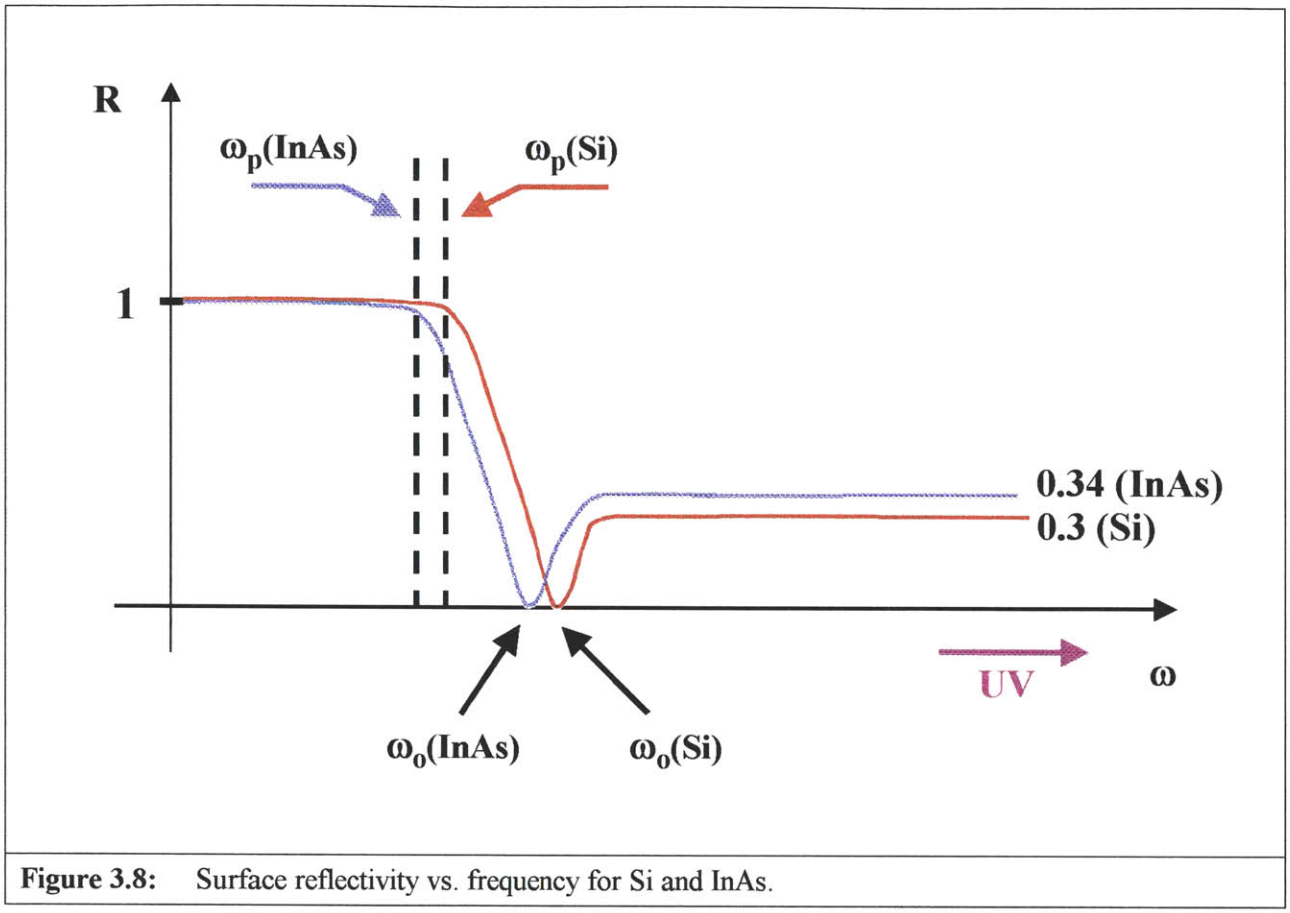


Figure 3.8: Surface reflectivity vs. frequency for Si and InAs.

In the UV regime, the surface reflectivities are roughly the same for both materials, with a slightly higher value for InAs. While this variation is too small to cause such a significant change in the rate of development of the photoresist, the plot predicts that if surface reflectivity was at issue, better results should have been obtained for InAs over silicon.

Prebake temperatures were considered next, and the thermal conductivities of both silicon and InAs were compared.

Electronic conductivity and lattice vibrations both contribute to the thermal conductivity of a given solid:[18]

$$K = K_e + K_{ph}.$$

Material properties determine which of these two terms dominate. The Debye model for the phonon spectrum addresses the theory of thermal conductivity, and the Debye temperature θ_D applies to the theory of lattice vibrations. If a material is heated at a temperature $T >> \theta_D$, its phonon density increases by $N_{ph} \sim T/\theta_D$, and lattice vibrations contribute significantly to the thermal conductivity K. In the limit that $T \geq \theta_D$, phonon density is relatively small, thus, for a material with high electrical conductivity σ_e,

$$\lim_{K_{ph} \to 0} \quad K_e + K_{ph} = K_e = \sigma_e T \left(\frac{\pi^2 k_B^2}{3q^2} \right) \qquad \textbf{Eqn. 3 4.9}$$

this is a statement of Weidemann-Franz law; a good electrical conductor (metal, semimetal and degenerate semiconductor) is a good thermal conductor in the temperature limit $T \geq \theta_D$. Eqns. 3.1 – 3.4 give a total electrical conductivity of 655.94 $\Omega^{-1}m^{-1}$ for InAs compared to 34.96 $\Omega^{-1}m^{-1}$ for silicon. Values for the Debye temperature were obtained for silicon and InAs: θ_D(Si) =645K, θ_D(In) = 129 K and θ_D(As) = 285K. At a 90°C

(363K) prebake temperature, silicon acts as a dielectric, with no thermal conductivity contribution due to phonons and very little due to electrical conductivity. InAs, on the other hand, is a semimetal in the temperature limit $T \geq \theta_D$, and becomes a good thermal conductor at 90 °C. Photoresist on the InAs surface sees prebake temperature, plus a thermal contribution from the substrate. This changes the properties of the resist and alters the exposure and development parameters.

During the prebake step, there are certain time and temperature considerations that affect exposure and development.[19] For a given material exposed to radiation, $R+\alpha+T=1$, where R is the reflectivity, α is the absorption coefficient and T is the transmission coefficient. For a dielectric like photoresist, $R \rightarrow 0$, so that $\alpha + T \simeq 1$. Prebaking drives out the solvent from the resist, allowing UV light to be absorbed in order to break or enhance cross-linking in the polymer. For best exposure and development results, however, there are some important points to consider:

1. High bake temperatures reduce the amount of solvent in the resist and lead to higher α and smaller T. There must be a balance between α and T, so that the transmission depth is at least comparable to the thickness of the resist layer. If T is too low, then exposure will occur in the top layer of the resist only, resulting in poor pattern development.

2. The above statement says that while less solvent in the resist allows higher absorption of UV, a little of the solvent must remain in order to render the resist slightly transparent to the radiation.
3. Shorter bake times and lower bake temperatures increase dissolution, but this must be carefully monitored in order to preserve resolution.

For the three types of photoresist used in the fabrication of the InAs cells, adjustments were made to the standard silicon recipe with regard to bake times and bake temperatures. Best results were obtained for positive resist OCG825-20 (used for thin metal liftoff) and thick positive resist AZP4620 (used for thick metal liftoff) when the prebake time was reduced from 30 minutes to 20 minutes and the prebake temperature was lowered from 90 °C to 85 °C. At these times and temperatures, and subsequent to a 65 second exposure, the develop time dropped markedly, down to 3 minutes from the initial 15 – 20 minutes imposed by the original recipe. With these adjustments, the pattern was well defined and developed through to the substrate surface.

Since image reversal AZ5214E does not use the same recipe, slightly different adjustments were made for this photoresist. The initial hot plate bake temperature was decreased to 85 °C from 90 °C, but the bake time of 30 minutes remained unchanged. Initial exposure was followed by the second flat plate bake conducted at 100 °C, reduced from the standard temperature of 120 °C. After an adjusted flood exposure, the resist

developed in 2½ minutes, compared to a develop time of 20 minutes imposed by the original silicon recipe.

The final recipes for the photolithographic steps, shown in Table 3.2 and Table 3.3, yielded 3-minute develop times for OCG825-20 positive resist and AZ5214E image reversal. Due to the high viscosity of thick positive resist AZP4620, the recipe in Table 3.2 was modified with the exposure time adjusted to 280 seconds; the silicon process for this resist uses comparable exposure times. The thickness of the resist coat was around 6 μm. Before the metal was deposited, the sample was ashed for 10 minutes to remove any residual polymer from the patterned areas.

For all photolithographic processes, a 1 cm x 1 cm InAs sample was mounted on a 2" silicon wafer. The edges of the sample created an uneven surface that lead to very uneven coating when the photoresist was dynamically dispensed. A static dispense was used instead, and these resists were successfully used as etch masks and for metal liftoff.

Table 3.2: InAs Photolithography Process – OCG825-20 Positive Resist

1. Solvent clean
   acetone followed by methanol and 2-propanol
2. Rinse in de-ionized water
3. Dehydration bake 30 minutes @ 90 °C
4. HMDS oven
5. Dispense 1 μm thick resist coat:

   Static dispense 16 seconds
   10 seconds dispense
   6 seconds static

   Spread 12 seconds @ 750 rpm

   Spin 30 seconds @ 2000 rpm
6. Prebake oven 20 minutes @ 85 °C (Silicon: 30 min @ 90 °C)
7. Expose 65 seconds using Karl Suss Model MA-4 Mask Aligner
   (Silicon: 30 seconds)
8. Develop OCG934 1:1 for 3 minutes (Silicon: 90 sec)
9. Hardbake oven 30 minutes @ 90 °C (over baking resist causes tears in the metal lines)
   (Silicon: 30 min @ 120 °C does not over bake the resist)
10. Asher 3 minutes
11. Rinse in de-ionized water

Table 3.3: InAs Photolithography Process – AZ5214E Image Reversal

1. Solvent clean
   acetone followed by methanol and 2-propanol
2. Rinse in de-ionized water
3. Dehydration bake 30 minutes @ 90 °C
4. HMDS oven
5. Dispense 1 μm thick resist coat:
   Static dispense 16 seconds
   10 seconds dispense
   6 seconds static
   Spread 12 seconds @ 750 rpm
   Spin 30 seconds @ 2000 rpm
6. Prebake flat plate for 30 minutes @ 85 °C (Silicon: 30 min @ 90 °C)
7. Expose 50 seconds using Karl Suss Model MA-4 Mask Aligner
   (Silicon: 30 seconds)
8. Flat plate bake 90 seconds @ 100 °C (silicon: 90 seconds 120 °C)
9. Flood exposure 500 seconds (Silicon: 200 seconds)
10. Develop AZ422 $2^1/_2$ minutes (Silicon: 90 seconds)
11. Asher 3 minutes
12. Rinse in de-ionized water

3.4.3 METALLIZATION

The most common metallization schemes used with compound semiconductors include gold as a primary element. As illustrated in Table 3.4, gold has two vital properties that make it suitable for MTPV applications; low resistivity that minimizes power loss, and a high melting point. In this regard, it compares favorably with aluminum and copper as a contact metal.

Table 3.4: Comparison: Au, Cu, Al[20]

	Resistivity (μΩ-cm)	Melting Point (°C)
Cu	1.7	1083
Au	**2.2**	**1064**
Al	2.7	660

For reasons that will be explained in this section, ohmic contacts may be achieved either by depositing a gold alloy, or by depositing a thin, intermediate metal film as an adhesion agent for the gold contact layer. For both these metallization schemes, however, chemical reactions occur at the metal/semiconductor and metal/metal interfaces that affect processing conditions, device lifetime, performance and reliability, and serve to define the optimal operating conditions.

3.4.3.1 Alloyed Contacts

Low resistance ohmic contacts to III-V semiconductors are typically achieved by depositing a metal containing a dopant.[21] When these alloyed contacts are sintered, the dopant diffuses to the substrate, producing a region of high carrier concentration at the metal-semiconductor interface. In these heavily doped regions, the width of the space charge region becomes sufficiently small that carriers can tunnel through the potential barrier (ohmic contact) rather than be limited by thermionic emission over the barrier (diode behavior). The specific contact resistance to *n*-type material may be approximated by[22]

$$R_C \approx A_o \exp\left[\frac{C_2 \phi_b}{\sqrt{N_D}}\right] \qquad \textbf{Eqn. 3.3.10}$$

where

$$C_2 = \frac{4\pi}{h}\sqrt{m_c^* K_{InAs} \varepsilon_o} \qquad \textbf{Eqn. 3.4.11}$$

h is Planck's constant, K_{inAs} is the material's dielectric constant and m_c^* is the electron effective mass, and ϕ_b is the barrier height. Equations 3.4.10 and 3.4.11 show that contact resistance decreases with high doping concentration in the layer beneath the metal film.

There are, however, problems associated with the use of alloyed contacts. While good adhesion is achievable, pinholes may occur in the metal film.[23] These defects may serve as loci of entry for contaminants that cause corrosion in the gold film.[24] In addition, when using gold alloys, ohmic contact is only achievable under optimal conditions.

The diffusion of Au into materials like InAs and InP serves to lower the chemical free energies, providing a driving force for enhanced diffusion of dopants.[25,26] From the ternary phase diagram of Au-InAs in Figure 3.9, and the data tabulated in Table 3.5, we can make several observations. Au selectively binds with In and form several stable compounds at temperatures ranging from 25 – 450 °C. This is due to the high solid solubility of indium in Au, as high as 50 – 51 atomic % for the triclinic intermetallic Au-In alloy.[27] The fact that no stable Au-In phases exist at higher temperatures is a key point in determining the anneal temperatures for Au on indium-based compounds. We will soon see that if the anneal temperature is too low, indium will diffuse into the Au metal contact, leaving vacancies at the metal/semiconductor interface. This phenomena and its consequences are explained by several investigators.

Figure 3.9: Au-InAs Interface [28]

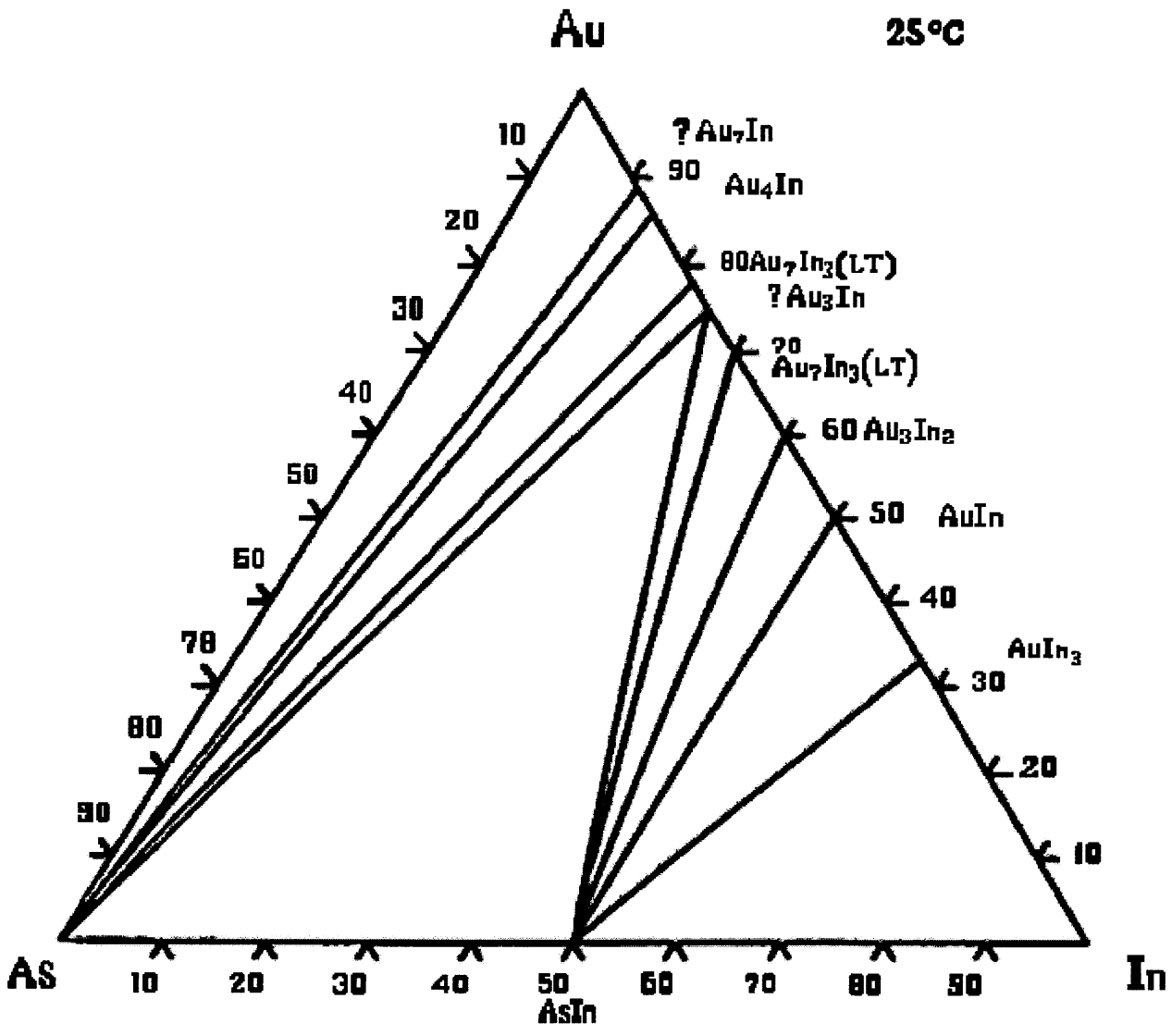


Table 3.5: Au-InAs: stable and unstable phases[29]

Room Temperature Phases			
System	**Phase**	**ΔH^o (kJ/g atom)**	**ΔG^o (kJ/g atom)**
In-Au	$Au_{90}In_{10}$	-5.7	-
	Au_4In	-11.5	-
	$Au_{10}In_3$	-13.3	-
	Au_3In	-14.3	-
	Au_7In_3	-16.8	-
	AuIn	-21.2	-
	$AuIn_2$	-16.8	-
As-Au	No composition		
High Temperature Phases			
System	**Phase**	**Stability range**	**Questionable Stability**
In-Au	Au_9In_4	364 - 482 °C	$Au_{87}In_{13}$
	Au_3In_2	224 - 457 °C	Au_7In
			$Au_{39}In_{11}$

Shen (Refs. 23, 26) found that the evaporation of AuZn onto InP produces a spatially inhomogeneous alloy due to two different evaporation rates of Au and Zn. Zn melts at 419 °C, while gold melts at 1064 °C. This results in the deposition of zinc-rich metal close to the metal/semiconductor interface, while the concentration at the free surface is closer to the desired value. This could mean that the surface concentration of

Au in the metal alloy is much too low to allow the gold to serve as a wetting agent for zinc diffusion into InP. Ideally, sputter deposition should be used instead of evaporation, if uniform stoichiometry throughout the metal layer is to be preserved.

If the anneal temperature is too low, a thorough mixing of AuZn occurs, depleting the Zn at the interface. As shown in Table 3.5, anneal temperatures at or below 450°C will favor the formation of Au-In solid phases. In this temperature range, thermally induced dissociation of the substrate lattice will produce vacancies as indium diffuses into the metal layer. This non-stoichiometry at the metal/semiconductor interface renders the metal contact non-ohmic. Shen found that annealing at temperatures above 460°C resulted in good ohmic contact for Au-Zn on InP. In this case the anneal serves to as a drive in diffusion, transferring the dopants from the gold layer to the semiconductor.

Another source studied the dopant distribution under the alloyed contact and proposed that Eqn.3.4.10 an incomplete representation of the specific contact resistance of an alloyed contact.[30] A study of AuGe contacts to *n*-type GaAs shows that Ge does not penetrate the surface of the semiconductor uniformly. As depicted in Figure 3.10,

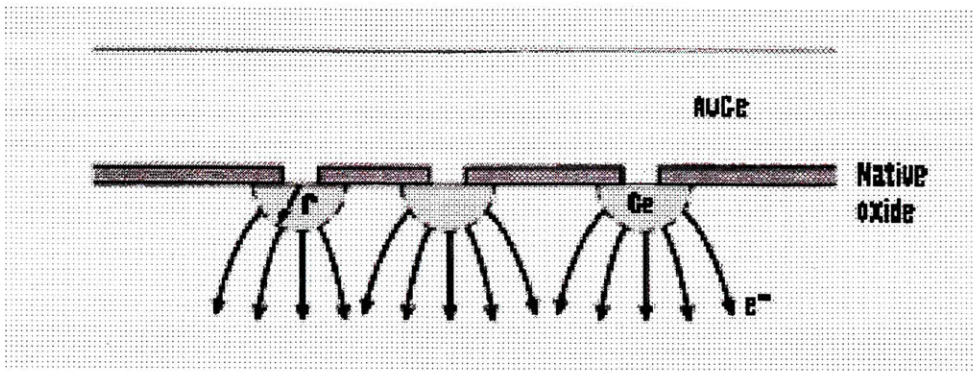


Figure 3.10: Schematic of ohmic contact to n-type GaAs showing the formation of small hemispherical contact regions and subsequent current crowding. (Campbell, Ref. #30)

dopants diffuse in small pockets of hemispherical radius r that have been observed electrically. The specific contact resistance will have two components, and Eqn.3.4.10 becomes

$$R_C \approx A_o \exp\left[\frac{C_2\phi_b}{\sqrt{N_D}}\right] + D^2\frac{\rho}{\pi r} \qquad \textbf{Eqn. 3..4.12}$$

where D is the mean distance between the pockets, ρ is the resistivity, and r is the radius of the hemisphere. It is desirable to have a small separation D between these inclusions, but this is difficult to achieve. An alternative method must be employed to lower the specific contact resistance. Ion implantation is a widely used method for creating highly doped areas beneath the contact metal. Another way obtain a highly doped layer is by

epitaxial growth. For a continuous highly doped layer, D = 0 and r → ∞, the resistance in Eqn. 3.12 is best approximated by Eqn. 3.10, a lowering of the contact resistance.

3.4.3.2 Non-Alloyed Ohmic Contacts –Theoretical considerations

In InAs, the Fermi level is pinned within the conduction band as depicted in Figure 3.11. A metal contact to *n*-InAs produces a bending of the energy bands such that $\phi_b \leq 0$, and ohmic contact is easily achieved. In this case, there is no potential barrier to electrons at the metal/semiconductor interface and low resistance contacts can be made for a wide range of *n*-type doping without the need for alloying to form n^+ surface layers.[31]

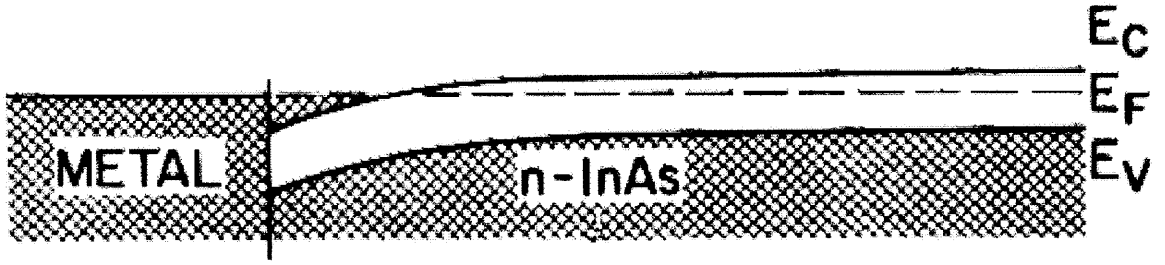


Figure 3.11 Band-bending diagram for metal on *n*-InAs interface. (J.M. Woodall et al).

Gold is a noble metal, and does not adhere well to oxide or oxidized surfaces. One or more metals are normally used at the gold-substrate surface to ensure strong bonding.[32] Low resistance ohmic contacts have been achieved by depositing thin layers of chrome (Cr) or titanium (Ti) onto a highly doped InAs surface before deposition of the Au contact layer. Sputter deposition and evaporation are two techniques used to deposit metal on the InAs surface.

While sputtering produces better film adhesion than does evaporation, bombarding the semiconductor surface with metal atoms may cause surface damage by creating point defects and introducing strain to the semiconductor lattice. As seen in the discussion on alloyed contacts, crystalline order must be maintained under the metal layers if the contacts must exhibit their lowest possible resistivities.

Another point to consider is that sputtered metal layers must be deposited uniformly over the semiconductor surface, patterned and sequentially etched. The situation becomes problematic if the etchant for the bonding metal also etches the semiconductor beneath it.

Evaporation and liftoff provide more favorable means of patterning and defining multiple layers of metal film. When using a straight-wall, positive resist, the poor step coverage of the evaporative process can be used to advantage. As shown in Figure 3.12B, a metal film deposited on top of a patterned photoresist layer will naturally tend to

break at the lower edges of the resist so that when the resist is subsequently dissolved, the metal layer on top of the resist is easily lifted away. Problems arise, however, if the resist is over baked during the photolithographic step. Over baked resist does not dissolve readily, resulting in incomplete liftoff and severe tearing of the metal lines. In more extreme cases, over baking may cause the photoresist to re-flow and the sharp vertical profile is lost.

Depending on the desired metal topology, either thermal or electron beam evaporation may be used. For thermally evaporated films, the metal is evaporated by means of a resistive element, limiting the amount of control one has on the evaporation rate and on the surface roughness of the metal film. Again, we emphasize the goal of close proximity operation, noting that, as illustrated in Figure 3.1, these MTPV cells are designed so that the metal is the topmost layer, with desired emitter/cell spacings as low as 0.2μm. In this case, the premium is on minimizing the surface roughness of the metal.

Electron beam evaporation allows for better control of the evaporation rate, and high vacuum conditions in the high 10^{-8} Torr are achievable. At these low pressures, other particulates are less mobile in the chamber, and the probability of incorporating foreign particles into the metal film is minimized. This allows for better control of the surface roughness of the film.

There are two physical attachments the electron beam system that make it easier to control step coverage in conditions where there are high aspect ratios. This is of special concern when working with the straight-wall geometries that are characteristic of positive photoresists. The aspect ratio is defined as

$$AR = \frac{step\ height}{step\ width} \qquad \textbf{Eqn. 3.4.13}$$

For AR ≥ 1, standard evaporation (stationary liftoff plate) yields extremely poor step coverage, since shadowing can lead to discontinuous film on one side of the contact. In this case, a planetary may be used to rotate the wafers and improve step coverage Profile B in Figure 3.12 is highly desirable for easy liftoff and un-interrupted metal lines and may be obtained using standard evaporation for AR ≤ 0.5.[33]

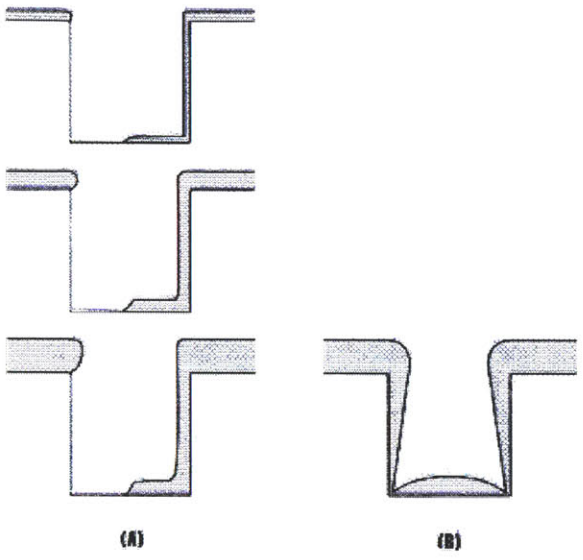


Figure 3.12: (A) Time evolution of the evaporative coating of a feature with aspect ratio of 1.0. (B) Final profile of deposition on rotated and heated substrates. (Campbell, Ref. #33)

As discussed in Section 3.4.2, the resist may be unintentionally hard-baked during the pre-bake step. If the resist is positive and straight-walled, the profile shown in Figure 3.12B can lead to severe tearing of the metal lines. Re-entrant geometry image reversal, schematically represented in Figure 3.13, produces clean metal lines even when un-intentionally hard-baked.

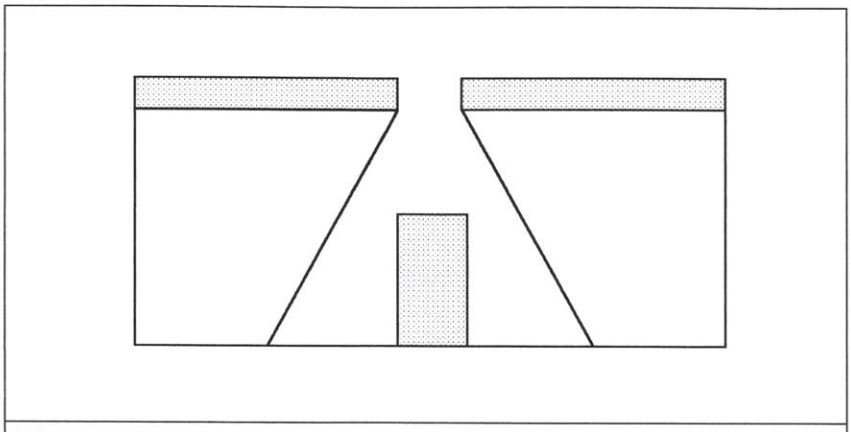


Figure 3.13: Image reversal re-entrant geometry

3.4.3.3 The Metallization Process

During the early stages of process development, the mask set shown in Figure 3.4 was designed for use with a positive resist. The smallest feature size is 20 μm, the width of the metal fingers on Mask #2; thus, the largest value for the aspect ratio is 0.05 when a 1 μm layer of resist is deposited and patterned for metal deposition. This value for the aspect ratio is well within the limits established for good symmetric coverage as described in Figure 312B, and liftoff plate was used for evaporative deposition.

A thin metal layer of Cr/Au was deposited onto the InAs sample using electron beam evaporation, and 300 Angstroms of Cr followed by 300 Angstroms of Au were deposited at a rate of 3 Angstroms/sec. Both the Cr and Au sources were contained in graphite crucibles. The base pressure was 7×10^{-8} Torr, with a background pressure of

around 2 x 10^{-7} Torr during evaporation. Metal liftoff was achieved by soaking the sample in acetone.

Figure 3.14 is a Dektak profile of the thin metal layer deposited in the early stages of process development, showing variations in the range of 100 - 200 Angstroms. This degree of surface roughness is undesirable.

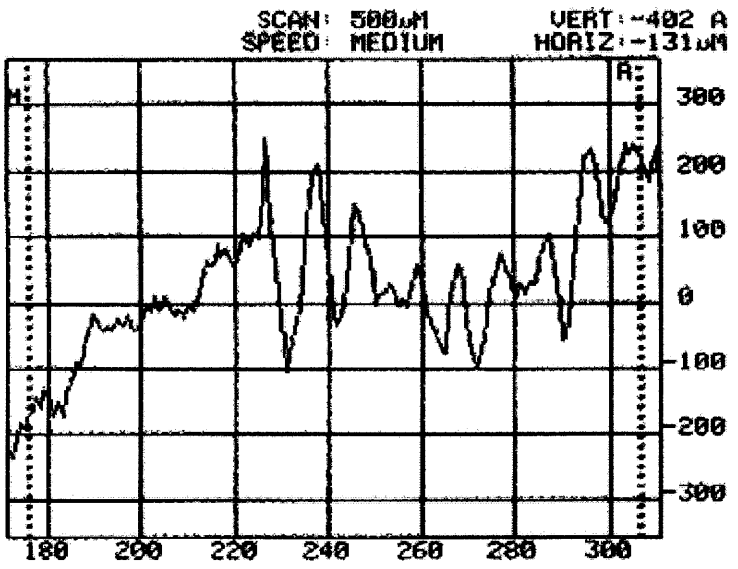
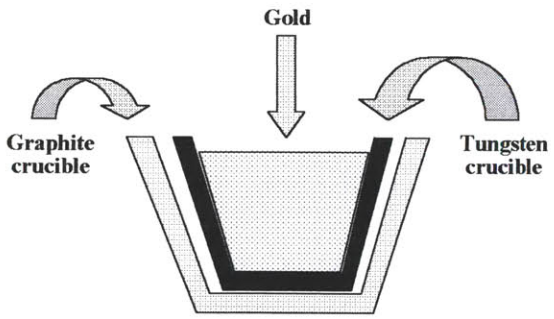


Figure 3.14: Surface roughness, thin metal grid. A first pass using electron beam evaporator. The horizontal axis is given in microns and the vertical axis in Angstroms.

The use of the graphite crucible was targeted as a major contributor to the roughness of the thin metal layer. Care must be taken to focus the electron beam at the

center of the source. During the early stages of the evaporative process, the beam often makes brief contact with the crucible, and graphite particles may be incorporated into the metal film. To alleviate this problem, a tungsten crucible containing the gold was placed inside the graphite crucible. With this setup, the unfocused beam would strike tungsten instead of graphite, reducing the probability of incorporating particulates into the metal film. The setup is illustrated in Figure 3.15, along with a Dektak profile of the metal surface, showing significant decrease in surface roughness, with the highest variation in the surface profile reduced to approximately 20 - 30 Angstroms.



(a)

(b)

Figure 3.15: (a) Schematic of source setup; (b) Surface profile of thin metal layer showing improved surface roughness. The horizontal axis is given in microns, the vertical axis in Angstroms.

Tearing in the thin metal lines precluded further use of positive resist for this metallization step, and in the later stages of process development, image reversal replaced positive resist for the liftoff process.

Following the thin metal liftoff, another photolithographic step was performed using thick, positive resist AZP4620, patterned using Mask #3. Using the same parameters listed above, a thick metal layer was deposited consisting of 300 Angstroms of Cr followed by 5,000 Angstroms of Au. For this part of the process, the background pressure reached an average high of 7×10^{-6} Torr during Au evaporation.

Due to the unavailability of the evaporation equipment at some times, sputter deposition was employed as an alternate means of depositing the thin metal film. During sputter deposition, substrate temperatures may rise as high as 350 C, and for this reason there can be no photoresist coat on the surface during metallization. The two metal layers must be deposited uniformly over the surface of the substrate and then sequentially etched. Since the chromium layer binds directly to the substrate, the etchant for this metal was tested on the InAs surface. A 4-second exposure to the chrome etch was enough to produce a very rough and rapidly etched profile on the semiconductor surface.

It was clear that Cr/Au could not be used as the thin metal layer for this process, and a Ti/Au layer was deposited instead. Titanium could be etched in a dilute solution of

100:1 HF at a rate of 30 Angstroms/sec without any noticeable effect on the underlying InAs layer at short exposure times.

A thin Ti/Au metal layer was uniformly deposited on the surface of the InAs by sputtering 300 Angstroms of Ti, followed by 500 Angstroms of Au. After sputter deposition, the thin metal layer was patterned and etched as follows:

i) Deposit, pattern and develop a 1μm layer of photoresist on top of the gold film; using Mask #2.

ii) etch the gold using an iodine compound of potassium iodide and iodine ($KI + I_2$) with an etch rate of 28 Angstroms/sec;

iii) etch the Ti layer using dilute HF solution as described above;

iv) rinse in de-ionized water.

The sputter deposition and the metal etch were performed on site by the MTPV group at Draper Laboratory, while the photolithographic step was completed at the Technology Research Laboratory (TRL) at Massachusetts Institute of Technology. Initial results were favorable; the metal lines were clean, with no evidence of tearing or peeling in the Ti/Au metal film, and the samples were allowed to sit for a few days until the thick layer could be deposited by electron beam evaporation.

During the early stages of the photolithographic step that preceded the thick metal deposition, degradation became progressively evident in the thin metal layer. It was at

first thought to be a handling problem, but the degradation of the thin metal was uniform throughout the sample. This occurrence was unexpected, since superior adhesion is one of the advantages that sputter deposition offers over the evaporative process. Because gold is a noble metal, the idea that contamination could cause this metal to degrade seemed highly unlikely. Reference to literature citing the occurrence of corrosion in gold, yielded some interesting facts. The presence of halogens, even in trace amounts will cause gold to corrode.[34]

Halogens are the Group 7A elements – fluorine (F), chlorine (Cl), bromine (Br), iodine (I), and astatine (At). It is likely that traces of fluorine and iodine will be present after etching the metal layers in HF and KI + I_2 solutions. With this information in hand, oxidation-reduction (redox) formulas were obtained[35] for each halogen-gold system were used to gauge the likelihood that halogen traces were responsible for the corrosion of the gold layer. The redox system is based on the theory of galvanic cells, for which the total potential of the reacting species is related to ΔG, the free energy difference between the reactants and products. A positive total potential corresponds to a negative value for ΔG, which is the condition for spontaneity.

A comparison of oxidation potentials shows that iodine is a strong oxidizing agent the presence of low humidity, and the room temperature reduction potentials are obtained from the reactions

$2e^- + 2H^+ + IO_4 \rightarrow IO_3^- + H_2O$, with $\mathcal{E} = 1.60V$ (in the presence of humidity)

$I_2 + 2e^- \rightarrow 2I^-$, with $\mathcal{E} = 0.54V$ (no humidity)

The reaction for the oxidation of solid gold to A^{3+} ions is

$Au \rightarrow Au^{3+} + 3e^-$, with $-\mathcal{E} = -1.50V$

The sum of these reactions is given as

$\mathcal{E}_{total} = 1.60V - 1.50V = 0.10V$

for iodine reacting within gold in the presence of humidity, and

$\mathcal{E}_{total} = 0.54V - 1.50V = -0.96V$

for iodine reacting with gold under non-humid conditions.

Under humid conditions, $\mathcal{E}_{total}$ is positive. Therefore, the dissolution of the gold will occur spontaneously under standard conditions, that is, when the device just sits there. In the absence of humidity, however, the negative value for $\mathcal{E}_{total}$ corresponds to a positive free energy, and the dissolution will not take place under standard conditions.

Dissolution is even more spontaneous when fluorine traces are present:

$F_2 + 2e^- \rightarrow 2F^-$, with $\mathcal{E} = 287V$

Of all the elements, fluorine has the highest positive reduction potential, ensuring that room temperature, Au will corrode spontaneously, if even a trace of this halogen is present.

Multiple rinses in de-ionized water will hydrate these halogens to produce acids like HF, HOI, $HOIO_2$, and $HOIO_3$, which may be sluiced away from the surface of the metal. Care was taken to ensure that these elements are flushed from the containers between rinses.

With the process complete, a final batch of MTPV cells were fabricated and characterized. The results of the characterization are given in detail, and under separate cover, by Michael Masaki.

3.5 DISCUSSION

A full process was developed for the fabrication of InAs MTPV cells. Additional steps were taken to ensure that microscale operation would be possible, allowing more energy to be transferred, and ultimately allowing more power to be extracted from the TPV cell.

Process Development

During process development, a suitable etchant was identified for InAs, and the etch rate was calibrated under conditions that were conducive to a well-controlled, uniform etch.

Several photolithographic processes were developed based on adapting an existing silicon process for use on InAs substrates. This was not an easy task, since these two semiconductors possess different optical and transport properties that affect process parameters such as bake temperature, bake times, length of exposure and development time.

The use of alloyed versus non-alloyed contacts on InAs were discussed. It was shown that because of the electronic structure of InAs, ohmic contact could easily be achieve when bifilms of Cr/Au or Ti/Au were deposited on the *n*-InAs surface. With this metallization scheme, electron beam evaporation was identified as the most effective method for metal deposition. Variations were made to the evaporation process in an effort to minimized surface roughness in the thin metal layer during evaporation.

With these processes fully developed, a full process flow is given in Table 3.6.

Table 3.6: Full Process Flow for fabrication of InAs MTPV Cells

Photolithography

1. Solvent clean
   acetone followed by methanol and 2-propanol
2. Rinse in de-ionized water
3. Dehydration bake 30 minutes @ 90 °C
4. HMDS oven
5. Dispense 1 μm thick coat AZ5214E:
   Static dispense 16 seconds
   10 seconds dispense
   6 seconds static
   Spread 12 seconds @ 750 rpm
   Spin 30 seconds @ 2000 rpm
6. Prebake flat plate for 30 minutes @ 85 °C
7. Expose 50 seconds on Karl Suss Model MA-4 Mask Aligner, using Mask #1
8. Flat plate bake 90 seconds @ 100 °C
9. Flood exposure 500 seconds
10. Develop AZ422 $2^1/_2$ minutes
11. Asher 3 minutes
12. Rinse in de-ionized water

Mesa Etch

13. Etch the mesas using 2:1:10 solution of phosphoric acid, H_3PO_4 : H_2O_2 : H_2O. The etch rate approximately 0.016 μm/sec when solution is:
    a) allowed to sit at room temperature for 6 minutes after mixing

b) immersed in a water bath during the etch

14. Rinse thoroughly in de-ionized water

15. Remove photoresist, using solvent clean (Steps 1 and 2).

16. Asher 15 minutes to remove photoresist residue, follow up with de-ionized water rinse.

Photolithography step: Pre-metallization – Thin metal

17. Repeat Steps 3 through 7, this time using Mask # 2 for thin metal deposition.

18. Repeat Steps 8 through 12.

Thin Metal Deposition

19. Deposit 300 Angstroms Cr film at deposition rate of 2 Angstroms/second

20. Deposit 300 Angstroms Au film at deposition rate of 3 Angstroms/second

Metal Liftoff

21. Dissolve photoresist by passive liftoff. Gold adhesion is preserved if the liftoff process does not include the use of ultrasound to accelerate dissolution of the resist. During passive liftoff, the sample may be allowed to sit in acetone for as long as 48 hours until the process is complete.

22. Follow up with rinse in methanol, 2-propanol and de-ionized water

Photolithography step: Pre-metallization – Thick metal

23. Repeat Steps 3 and 4.

24. Dispense 3.5 μm thick coat AZ P4620 (thick positive resist):
    Static dispense 20 seconds
    10 seconds dispense
    10 seconds static
    Spread 12 seconds @ 750 rpm
    Spin 30 seconds @ 2000 rpm

25. Prebake oven 20 minutes @ 85 °C

26. Expose 280 seconds using Karl Suss Model MA-4 Mask Aligner using Mask #3
27. Develop 3 minutes
28. Hardbake oven 30 minutes @ 90 °C
29. Asher 10 minutes
30. Rinse in de-ionized water

Thick Metal Deposition

31. Deposit 300 Angstroms Cr film at deposition rate of 2 Angstroms/second
32. Deposit 5000 Angstroms Au film at deposition rate of 3 Angstroms/second

Metal Liftoff

33. Repeat Steps 21 and 22

The process developed here will be used for the fabrication of more complex MTPV cell geometries and cell structures. To further increase the amount of power that can be extracted from an MTPV cell, InGaAs heterostructures may be employed instead of the simple p-n junctions used in this process. In addition, devices of various sizes may be incorporated in the design in order to investigate the effect of the device size on its performance. Such a mask set was developed and is shown in Figure 3.16.

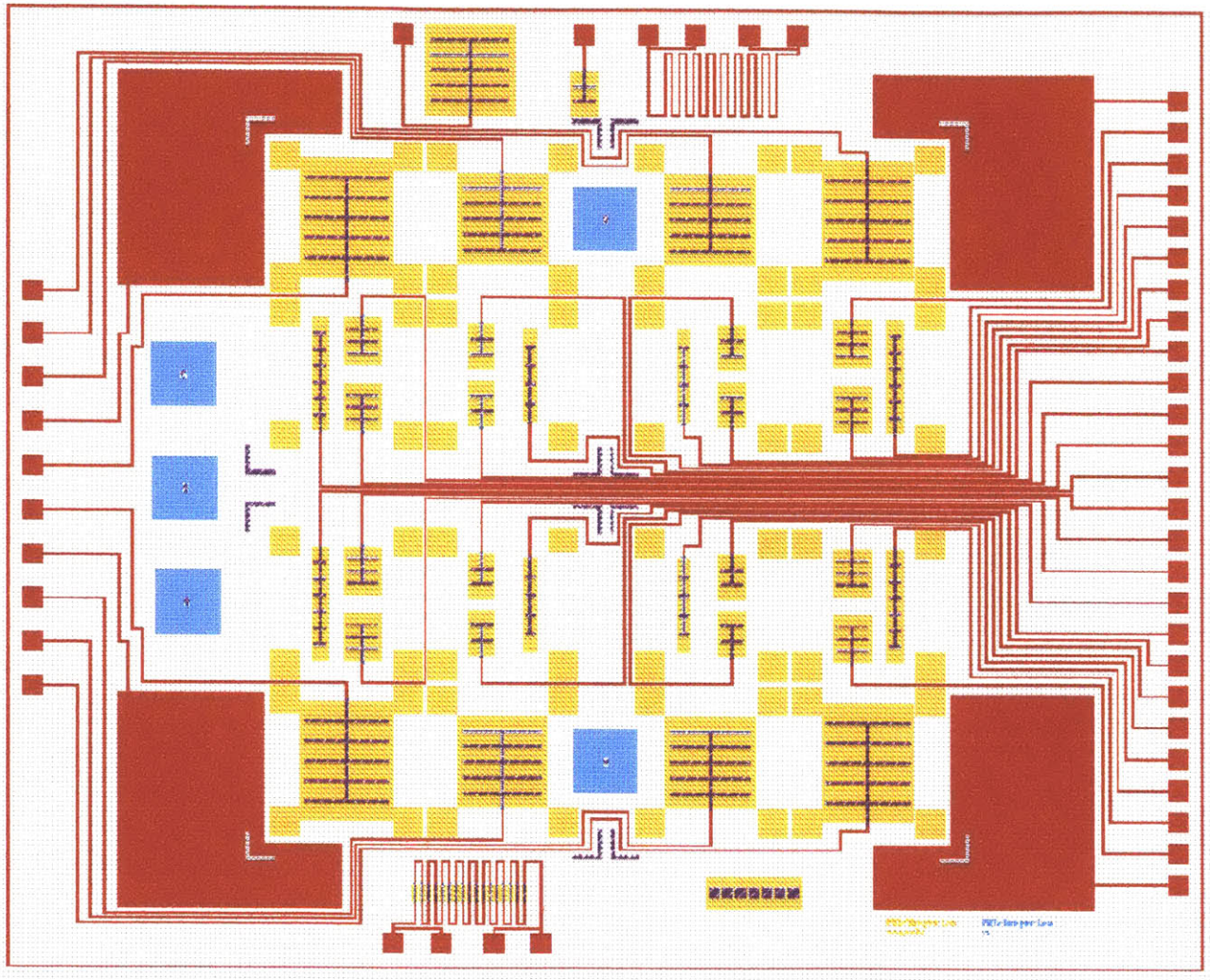


Figure 3.16: Mask Set for future MTPV processing. Cells vary in size and surface area, for easy analysis of how device size affects performance. Massachusetts Institute of Technology, 2000 ©.

CHAPTER 4

PASSIVATION: OXIDATION OF INAS

This chapter discusses the necessity for device passivation, and examines the difficulties faced III-V semiconductor surfaces and offers some solutions to the problem. Section 4.1 discusses the need for surface passivation and examines the possible reasons why current passivation techniques are less than optimal.

Section 4.2 gives an overview UV/ozone treatment of III-V semiconductor surfaces, a newly established technique for surface passivation. The introduction is followed by a detailed discussion of how this technique works, and gives some insight into why other passivation processes might benefit from it. In Section 4.2.2, a model is developed for oxidation of III-V semiconductors at low temperatures with a dry O_2 ambient. Section 4.2.2.1 is dedicated to the characterization of p-type InAs samples

exposed to UV/Ozone treatment, while Section 4.3 summarizes UV/O_3 method and cites areas in the passivation process that warrant further investigation.

4.1 III-V Semiconductor Surface

Atoms residing within the bulk of a semiconductor exhibit four-fold coordination that is conducive to the stability of the crystal. Each constituent atom forms a bond with four nearest neighbors to completely fill its valence shell, thereby achieving its lowest energy configuration.[36]

The periodicity in the bulk of the semiconductor terminates abruptly at the surface, with unsatisfied dangling bonds that make the surface highly reactive. Surface atoms easily form bonds with foreign atoms in an effort to lower their total energy. Elements like carbon, hydrogen and oxygen from the atmosphere will adhere to the semiconductor surface to form hydrocarbons and native oxide. Unlike oxides like SiO_2, III-V native oxides have poor density and may incorporate metallic and organic contaminants.

Empirical evidence confirms that the growth rate of hydrocarbons exceeds native oxide growth on freshly cleaved, oxide-free surfaces. Therefore, a newly exposed III-V surface will not contain a continuous native oxide layer, but consists of localized areas of hydrocarbons interspersed with areas of oxide.[37] This is illustrated in Figure 4.1.

Furthermore, the oxide layer may contain contaminants like sodium and particulates from the environment. Hydrocarbons strongly chemisorb unto the new surface, and do not desorb when the wafer is heated during processing. Instead, they decompose to form carbide fractions on the surface.

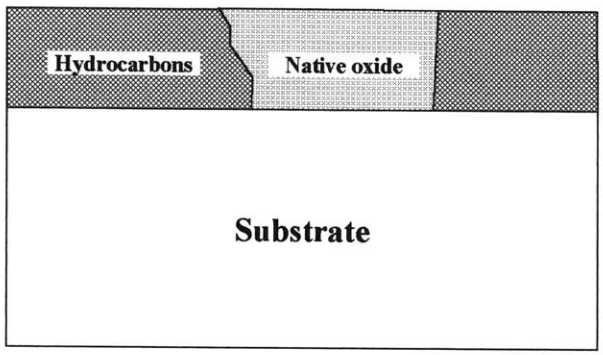


Figure 4.1: A schematic diagram of the newly exposed III-V surface. As proposed by Ingrey, the surface contains patches hydrocarbons and native oxide. Since the oxide also incorporates contaminants, both layers will produce surface trap levels in the energy band gap.

Hydrocarbons and other contaminants create surface trap states in the energy bandgap that act as generation and recombination centers for charge carriers. Since the surface cannot store charge, particle conservation demands that the rate of surface generation minus the rate of surface recombination equals the carrier flow into the surface:[38]

$$G_S - R_S = |F_S| \qquad \text{Eqn. 4.1}$$

The term on the left is the net surface generation rate and is related to the net surface recombination rate U_s, by

$$G_S - R_S = -U_S \qquad \text{Eqn. 4.2}$$

The flux F_s may be expressed as an electron or hole current density

$$F_{es} = -\frac{1}{q} J_{es} \qquad or \qquad F_{hs} = -\frac{1}{q} J_{hs} \qquad \text{Eqn. 4.3}$$

Then the net surface recombination rate may be expressed in terms of an electron or hole current flow towards the surface:

$$U_S = \frac{1}{q}|J_{es}| = \frac{1}{q}|J_{hs}| \qquad \text{Eqn. 4.4}$$

External surface generation occurs when the semiconductor is illuminated. If the length of the device is much longer than the absorption length of the light, then the generation function can be assumed to be confined to a thin layer at the surface to give a surface continuity equation:

$$g_S(ext) - U_S = \frac{1}{q}|J_{es}| = \frac{1}{q}|J_{hs}| \qquad \text{Eqn. 4.5}$$

Since we expect that external carrier generation will exceed net recombination, the terms on the right represent net current flow away from the surface recombination

centers. Under low-level injection conditions, the net surface recombination rate U_s, is linearly proportional to the excess carrier concentration at the surface.

$$U_S = S * n'(s) \qquad \textbf{Eqn. 4.6}$$

Then

$$g_s(ext) - S * n'(s) = \frac{1}{q}|J_{es}| = \frac{1}{q}|J_{hs}| \qquad \textbf{Eqn. 4.7}$$

S is the surface recombination velocity, and may be defined as the perpendicular component of the velocity with which carriers flow into the surface to recombine. S depends on the density of surface traps.

If the surface is well passivated, there are few recombination centers and the carrier flow rate towards the surface is much lower than it would be in the absence of passivation.

Figure 4.2 illustrates why the passivation of III-V surfaces may prove to be problematic. While a buffered oxide etch will remove the patches of native oxide, the most thorough solvent clean will not remove the hydrocarbons. Instead, most solvents contain carbon, hydrogen and oxygen, which serve to accentuate the growth of surface hydrocarbons.

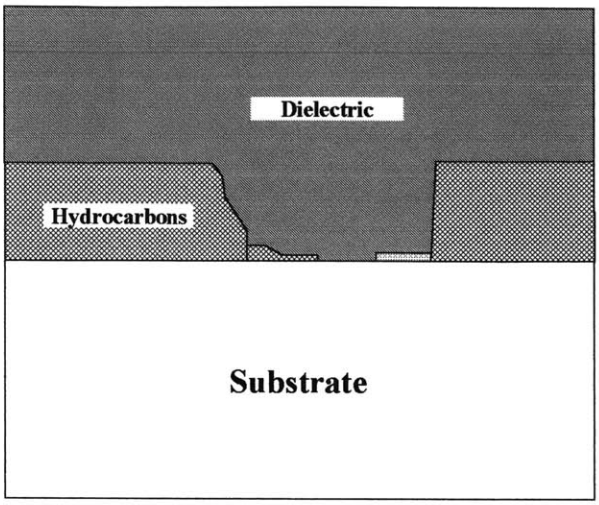


Figure 4.2: Schematic diagram of a III-V surface with a passivating dielectric layer. In a typical process, the surface in Figure 4.1 will have been treated to a thorough solvent clean, and the native oxide removed by a buffered oxide etch.

When a dielectric layer is deposited on this surface, the passivating effect may be less than optimal, since the hydrocarbons have not been eliminated from the surface and the density of surface traps may still be significantly high.

The method employed to deposit the dielectric layer may introduce additional problems, as is the case with wet oxidation, and anodic and plasma grown oxides. During wet oxidation of GaAs and InP surfaces, water molecules adsorb dissociatively at a rate that is three orders of magnitude greater than for dry oxygen. Because of this, H and OH may reside at the oxide/semiconductor interface, to create surface trap levels in the energy band gap. Anodized and plasma formed oxides are non-stoichiometric with

the group V element forming metal bonds at the oxide/semiconductor interface.[39] Thermally grown oxides have been known to be deficient in the group V element, with excess accumulation of this element at the oxide/semiconductor interface. Lowering the growth temperature to around 350 °C has eliminated this problem.[40] However, even these carefully revised and improved methods for oxide deposition will not yield the best results if these layers are deposited on a surface such as the one depicted in Figure 4.2. As an illustration of this, PECVD oxides have also been used for surface passivation, but experimental results discussed in Section 4.2.1 show that this passivation method is less effective if contaminants remain on the semiconductor surface. The process employed to facilitate effective PECVD passivation will now be described in detail.

4.2 UV/Ozone Treatment of III-V Surfaces

A new method for passivating III-V surfaces was proposed by Ingrey in 1992. This method uses already established UV/Ozone surface cleaning and oxidation techniques to remove contaminants from the surface. The entire process essentially removes the two contaminating layers -- hydrocarbons and native oxide – from the surface before the dielectric layer is deposited.[41]

Passivation: Oxidation of InAs

A UV/ozone system operates two characteristic wavelengths: i) radiation at a wavelength 184.9 nm dissociates molecular O_2 to form atomic oxygen. Photons at this wavelength also dissociate hydrocarbons and other organic contaminants like resins and human skin oils. ii) radiation at 253.7 nm wavelength dissociates ozone to create atomic oxygen. Most hydrocarbons will absorb UV radiation at this longer wavelength, and the resultant excitation facilitates reaction with atomic oxygen to form simpler, volatile molecules that desorb from the surface.[42] UV/O_3 will not remove the patches of native oxide, nor any of the contaminants that may be embedded within it. Therefore, deposition of dielectric layers immediately following an initial UV/Ozone clean will lead to a poorly passivated surface.

Samples exposed to UV/ozone treatment may be subjected to slightly elevated temperatures, depending on their proximity to the UV light source. For instance, one investigator found that the temperature in the region within 5 mm of the UV lamp was approximately 70 °C.[43] Devices that are sensitive to high temperature processing conditions may be processed without cause for concern.

Proximity is also an important factor in this process. Ozone must absorb UV to create atomic oxygen, and the intensity of the light falls off with distance from the sample. Therefore, the effect of the UV/O_3 treatment depends on the distance of the sample from the UV source. A sample placed at a distance 5 mm from the UV lamp was

found to be free of hydrocarbons in 90 seconds, while it took 13 minutes to clean a sample placed 8 cm away. For best results, samples for oxidation should be placed within 1 cm of the light source.

Ingrey's proposed method for growing a reproducible, stoichiometric surface oxide is described in Table 4.1. First, the surface must be thoroughly cleaned with a solvent to remove the bulk of inorganic contaminants. After rinsing in de-ionized water, the sample is exposed to UV/O_3 treatment to remove surface hydrocarbons, allowing them to desorb from the surface, to be replaced by a UV/O_3 oxide. The sample now contains two types of oxide, one created by the treatment, and the original native oxide. An oxide etch containing xylene or HF will remove both oxides, with the extra hydrogen forming an H-terminated layer on the bare semiconductor surface.

Passivation: Oxidation of InAs

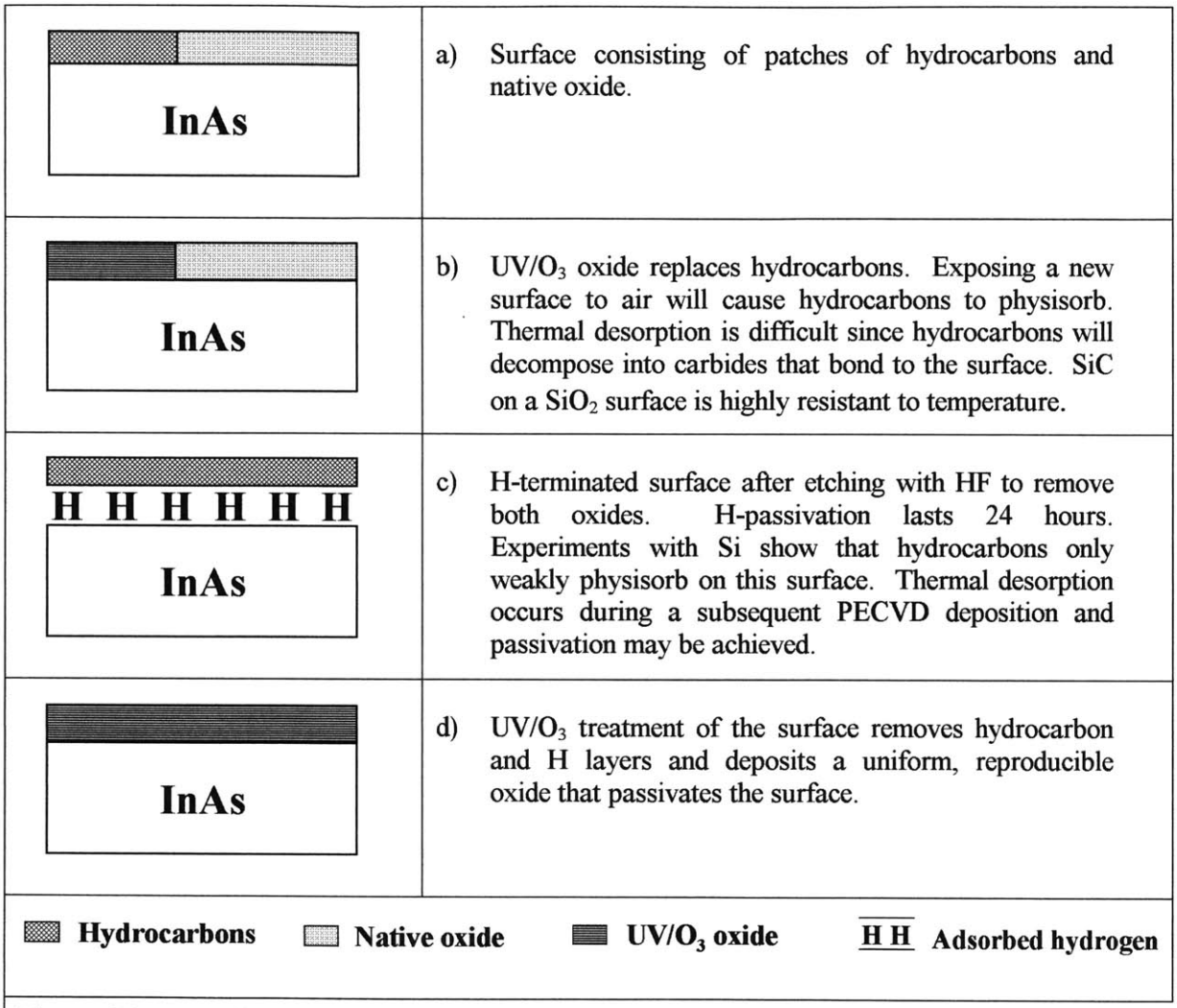


Figure 4.3: UV/Ozone passivation of a III-V semiconductor surface. (Ingrey, *et al* Ref. #41)

Upon exposure to the atmosphere, hydrocarbons weakly physisorb to this H-passivated layer, which may serve to protect the surface from contamination for up to 24 hours. If a PECVD or thermal oxide is deposited at this point, hydrocarbons will desorb

from this surface at process temperatures around 200 C. The hydrogen will bind with oxygen and adsorb from the surface in the form H_2O vapor, allowing the deposition of a passivation layer that is virtually free of contaminants.

As an alternative to PECVD and thermally grown oxide, the sample may once again exposed to UV/O_3 treatment, to deposit a thin, reproducible III-V surface oxide.

Other researchers have successfully used UV/ozone treatment to grow reproducible III-V oxides, overcoming the primary obstacle of surface non-stoichiometry,[44,45] a condition that may either be attributed to the different oxidation rates of the Group III and Group V elements or to the physical chemistry of the growing oxides. These phenomena will be discussed further in Section 4.2.2.

Driad *et al* (Ref. 44) successfully passivated HBTs made from InGaAs/InP using UV/O_3 oxidation techniques. The results were interesting:

1. After exposing the devices to initial UV/ozone treatment to remove hydrocarbons, the devices were tested while the two types of oxide still remained on the surface (as pictured in step b) above). Gummel plots revealed no change in collector current, but showed an improvement in base current gain of almost one order of magnitude at low collector current and a decrease in the ideality factor from 1.5 to 1.36.

2. When a PECVD dielectric layer was deposited immediately after step b), the current gain was drastically affected. This confirms Ingrey's theory on III-V surface morphology. Patches of hydrocarbons and oxide reside on the newly exposed III-V surface. While the UV/ozone treatment removes hydrocarbon contamination from the surface, native oxide containing impurities and contaminants remained on the surface and was capped by the PECVD layer. The PECVD deposition temperature may have caused these contaminants in the native oxide to diffuse to the oxide/semiconductor interface where they formed bonds at the substrate atoms, creating surface trap levels in the bandgap. The passivating effect was lost and the current gain suffered.
3. The current gain was restored when an HF dip was performed to remove the oxides and H-terminate the surface. A subsequent PECVD deposition resulted in successful passivation.
4. It was found that surface stoichiometry is a strong function of UV/O_3 exposure time, with 20 minutes of exposure as the upper bound when samples were placed a distance of 10 mm from the UV lamp.

UV/O_3 treatment appears to be very effective in three key areas: First, when timed correctly, it eliminates any original surface non-stoichiometry. Second, it provides a way to prepare clean surfaces suitable for deposition of a dielectric layer or even for epitaxial

growth. Third, it may be possible to grow UV/O_3 oxides as surface passivation layers. A study of the chemistry and growth kinetics of the oxidation process will help us to better understand the mechanisms governing oxidation of III-V in a dry O_2 ambient. This should help us to predict and control the conditions for maintaining surface stoichiometry. Non-stoiciometric conditions will degrade device performance and reliability. The oxidation of III-V semiconductors will be examined in the next section, but the main goal is to identify ways to grow a high quality oxide on the InAs surface, that will function as a passivating layer.

4.2.1 THE III-V SURFACE OXIDATION

In order for an oxide to grow on any semiconductor surface, atomic oxygen must interact with the atoms that reside at the surface of the semiconductor. For elemental semiconductors like silicon, diffusion is the mechanism behind SiO_2 growth. The growth rate may be parabolic or linear depending on the thickness of the initial surface oxide layer.

The mechanism controlling the growth of III-V oxides is not so easy to determine. Driad *et al* (Ref. 44) and Lu *et al* (Ref. 45), report on oxide composition, oxidation rates and surface stoichiometry for oxides grown on InGaAs (100), GaAs (100) and InP (100)

surfaces. After oxidation, XPS (X-ray Photoelectron Spectroscopy) data revealed that the InGaAs contained an oxide layer composed of In_2O_3, Ga_2O_3, As_2O_3 and As_2O_5. By the same method of analysis, GaAs surface was found to be composed of Ga_2O_3, As_2O_3 and As_2O_5, while the InP surface showed strong evidence of In_2O_3 and a phosphorous oxide. Lu *et al* found that Ga_2O_3 and As_2O_5 both exhibited linear growth rates, while the growth rate of the As_2O_3 oxide was logarithmic. Lu *et al* also found that the As oxides exist in two layers, with As_2O_5 at the surface, and Ga_2O_3 homogeneously distributed throughout the entire oxide layer. A schematic representation of the oxide composition on GaAs is shown in Figure 4.4.

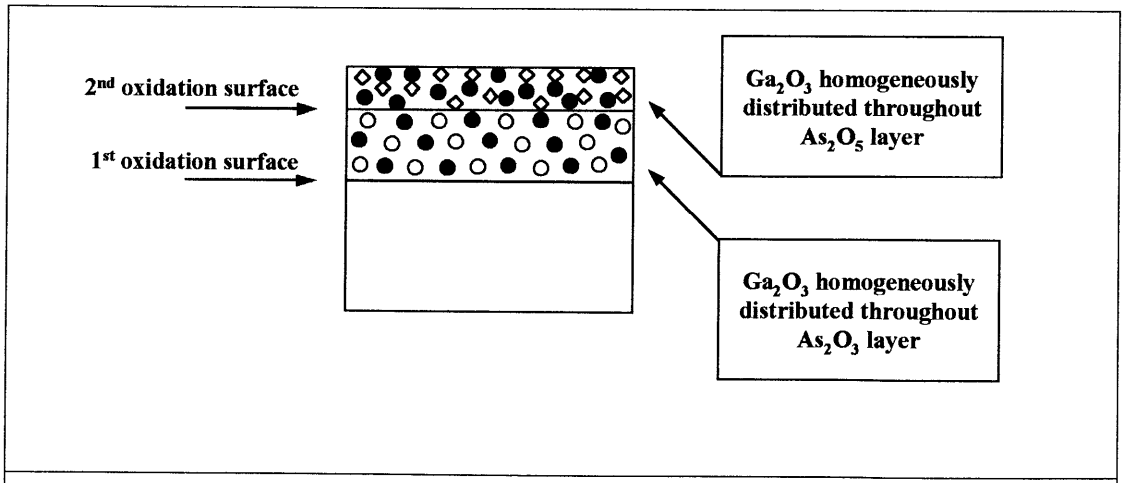


Figure 4.4: Oxidation of the GaAs surface, showing two successive oxidation interfaces.

As mentioned in the previous section, the different oxidation rates of Groups III and V oxides raises the issue of surface stoichiometry. The question to be addressed is:

at what oxide thickness is surface stoichiometry preserved for the different compound semiconductors? Lu *et al* (Ref. #45) reported that good quality GaAs surfaces were obtained for exposure times ranging from 10 to 40 minutes, for which times the Ga/As bulk ratios are very close to unity. This report states that high quality GaAs surfaces are obtainable for roughly 20 minutes of exposure. Driad *et al* (Ref. #44) were more specific in stating that while good GaAs surface stoichiometry is obtained for exposure times of less than 20 minutes, the best surfaces were achieved for 10 minute exposure times. Both groups report oxide thicknesses of less than 30 Angstroms for up to 20 minutes of exposure time. The data in Figure 4.5 shows that for exposure times exceeding 20 minutes, excess arsenic is seen at the GaAs/oxide interface.

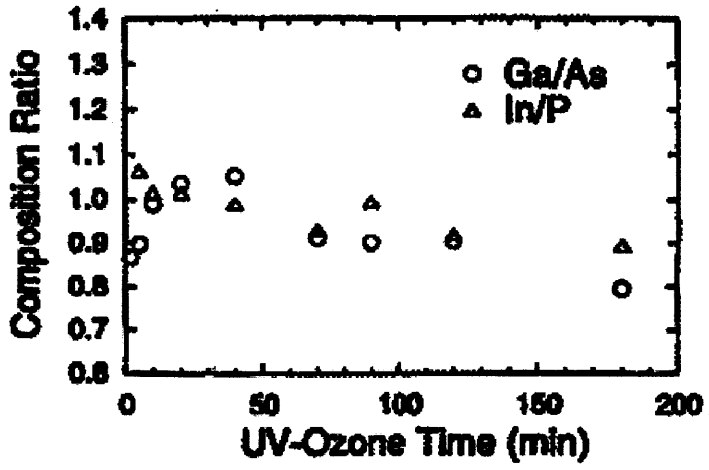


Figure 4.5: Semiconductor composition ratio near the surface as a function of UV exposure time. (Driad *et al*, Ref. #44)

Passivation: Oxidation of InAs

A quick study of Figure 4.5 might help to explain the III-V growth pattern, and help us to understand why arsenic accumulates at the GaAs interface at longer UV/ozone exposure times. From the data in Figure 4.5, we note that at the onset of oxidation, the Ga/As ratio at the semiconductor surface is less than unity and conclude that Ga must the first to oxidize, leaving excess arsenic to accumulate at the oxide/semiconductor surface. At some time greater than t=0 arsenic oxidizes, and does so at a logarithmic rate observed by Lu *et al*, while the Ga oxide continues to grow at a linear rate. The Ga/As ratio increases gradually increases to unity and slightly beyond as the excess surface arsenic is used up at a rate that exceeds that of the Ga. For a short period, excess Ga accumulates at the surface, evidenced in Figure 4.5 a Ga/As ratio that is slightly greater than unity. What happens next is puzzling. The Ga/As ratio suddenly drops below unity, an indication that arsenic is accumulating at the surface, and continues to accumulate as exposure time increases. Lu *et al* (Ref. #45) states that As_2O_3 grows rapidly during the initial oxidation stages and then slows down significantly, at which time, As_2O_5 grows at a linear rate.

These phenomena raise some key questions: Why does As_2O_3 growth come to such an abrupt halt after it is established that initial conditions favor logarithmic growth in this oxide species? Why do two oxidation interfaces exist, as illustrated by Lu *et al*? Why do final conditions favor As_2O_5 growth over As_2O_3 growth? Why does the surface

become non-stoichiometric with excess accumulation of elemental As, and can this condition be controlled? In an attempt to answer these questions, a model was developed in this thesis for III-V oxide growth.

4.2.2 III-V Oxidation Kinetics: Low Temperature UV/Ozone Treatment

A model for III-V oxides UV/Ozone oxidation was developed by the author, in an effort to understand growth kinetics, oxide characteristics, and the associated time constraints for achieving and maintaining surface stoichiometry. A good place to start would be to identify the chemical processes that produce the GaAs oxidation pattern observed by Driad and Lu. When oxygen arrives at the III-V surface, it forms chemical bonds with the Group III and Group V atoms. How the oxidation process develops depends on initial surface conditions and on how these atoms react and bond with the oxygen.

Each element on the periodic table has an associated electronegativity or electron affinity, which is the ability of an atom in a molecule to attract electrons to itself. When two atoms come in close proximity to each other, the difference in their electronegativity determines the polarity of the bond. If this difference is large enough, the more electronegative atom will remove electrons from the other, thereby reducing that atom to an ionic state. An ionic or polar covalent bond may form, due to a combination of

Coulomb attraction and/or sharing of electrons. If atom B is less electronegative than atom A, then the B atom reduces to

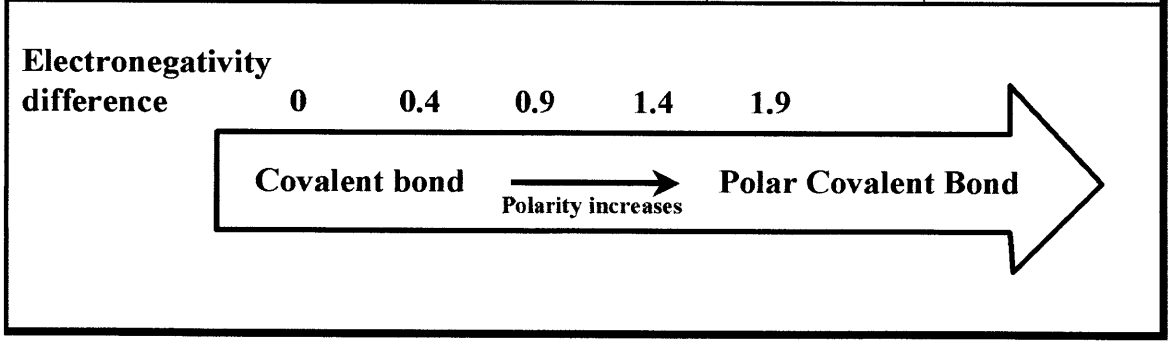
$$B \rightarrow B^{x+} + x \text{ electrons.}$$

From the above equation, we note that the difference in electronegativity is a measure of the oxidation potential of atom B. The value of x is given by the number of electrons in the valence shell of atom B, and x+ is its oxidation state. Atom A acquires only enough electrons to fill its valence shell, with the remainder of the electrons existing as free charge carriers in the A-B material. With both A and B valence shells filled, the ionic bond is the most stable bond, because it represents the lowest energy configuration for the two atoms.

Table 4.1 shows the electronegativities for oxygen and some of the Group III and Group V elements. The electronegativity difference between oxygen and the Group III

Table 4.1: Electronegativity/Oxidation potential[46]

Element	Electronegativity (difference)	Atomic Radius (Angstroms)	Oxidation States	Ionic Radius (Angstroms)
O	3.5	0.73	O^{2-}	1.40
Group III				
Ga	1.6 (1.9)	1.41	Ga^{3+}	0.62
In	1.7 (1.8)	1.66	In^{3+}	0.81
Group V				
P	2.1 (1.4)		P^{5+}	2.12
As	2.0 (1.5)	1.39	As^{5+}	0.47
Sb	1.9 (1.6)		Sb^{5+}	0.62



elements (differences are shown in parentheses) is slightly larger than the electronegativity difference between oxygen and the Group V elements. Thus, the Group III elements exhibit higher oxidation potentials and will tend to oxidize first. As a result, when oxygen is incident upon the III-V surface, the first reaction produces a chemisorbed III-oxide layer at the surface. The numbers in Table 4.1 also suggest that V-atoms will

ionize more slowly, requiring that the resultant V-cations diffuse through the III-oxide to combine with oxygen. The mechanism for III-V oxide growth may be explained by the changes that occur within the energy band structure of the oxygen-semiconductor system.

We expect the initial III-oxide to be very thin, no more than a few atomic layers thick, and that the bandgap of the oxide is sufficiently wide that it may be considered to be perfectly insulating at room temperature. We also expect that the initial chemisorption takes place quickly and uniformly, and produces no electrons:

$$III_2O_3 = III^{3+} + III^{3+} + O^{2-} + O^{2-} + O^{2-} + \text{zero electrons.}$$

With no charges or fields induced in the system, Figure 4.6 may schematically represent the resultant energy band structure for the semiconductor in direct contact with the chemisorbed layer. In the band diagram, E_o is the vacuum level of the semiconductor and qE_o is the energy at which an electron is free to leave the crystal. E_F is the Fermi energy; below this level, no states in the conduction band of an *n*-type semiconductor are occupied. Another important energy is the semiconductor work function, qW_s. As in metals, the work function is the energy required to promote an electron from E_F to the vacuum level. When electrons enter the semiconductor from the vacuum level and fall to the level E_C, they lose an energy $q\chi_s$ known as the electron affinity. Figure 4.6 shows

atomic oxygen incident on the surface of a III-V semiconductor containing a III-oxide layer.

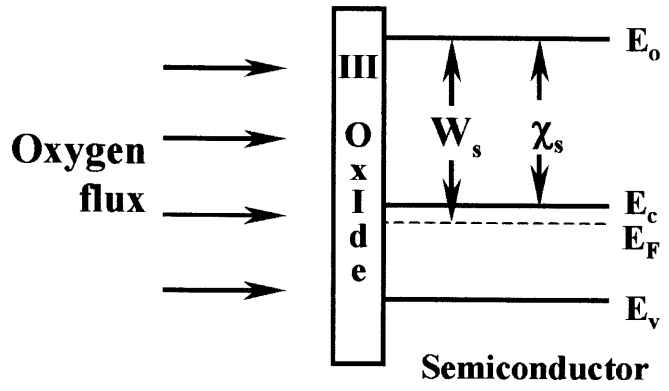


Figure 4.6: Energy band structure of oxide-semiconductor system as initial III-oxide chemisorbs.

While most of the arriving oxygen builds up at the free oxide surface, some of it diffuses through the thin oxide layer to interact with atoms at the oxide/semiconductor interface. Close contact between these two dissimilar materials – atomic oxygen and the III-V compound semiconductor -- will result in the formation of a single electronic system with a uniform Fermi level. The shape of the energy bands is determined by the work functions of the two materials.

Passivation: Oxidation of InAs

Since oxygen has 8 electrons, with 6 of them occupying the outermost valence shell, low Coulomb screening predicts a high work function in this material. On the other hand, a Group III atom such as indium has 49 electrons, with only three occupying the valence shell; arsenic, a Group V atom, has 33 electrons with 5 in the valence shell. Thus, a III-V compound semiconductor like InAs has a high degree of Coulomb screening within its constitutive atoms, and the overall work function is expected to be much lower that that of oxygen. The proposed band line-up for the O-InAs system just after the formation of the initial oxide layer, is shown in Figure 4.7a. E_o represents the alignment of the vacuum levels for both materials, while W_{oxygen} and W_s are the respective work functions for the oxygen and semiconductor. Because of the large difference in work functions, the Fermi level in the oxygen lies below the Fermi level of the semiconductor. Note that oxygen has an electron configuration of

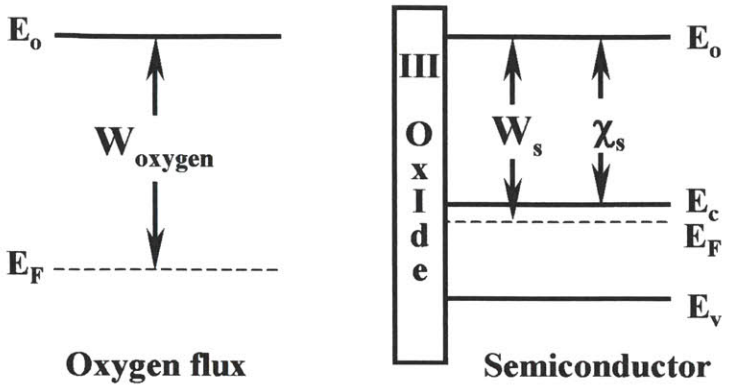
$$1s^2 \boxed{2s^2\ 2p^4}$$

where the boxed electrons represent the population of the partially filled valence shell. The relative positions of the Fermi levels dictates that empty valence states in the oxygen are at lower energy than the valence states of the semiconductor.

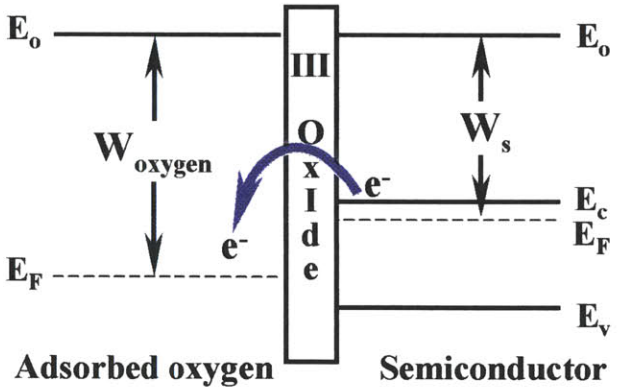
Oxygen arriving at the surface remains separated from the semiconductor by the width of the III-oxide layer. This layer is assumed to be thin enough, however, that charge transfer will occur across the interface, as electrons in the semiconductor are

presented with empty states at lower energy in the oxygen. This charge transfer, illustrated in Figure 4.7b, makes the surface of the semiconductor positively charged, while the oxygen layer at the surface of the oxide becomes negatively charged.

As time goes on and electron flow continues, this ionization process sets up a strong electric field across the oxide, with $E \sim q/r^2$, where r is on the order of a few Angstroms -- the thickness of the existing oxide layer. The electric field gradually builds up across the interface, and in due time, stops further electron migration. Equilibrium is established, as the electric field sets up a built-in potential ϕ_{bi} that subsequently leads to band bending within the semiconductor. This final stage is depicted in Figure 4.8, illustrating that band bending ultimately leads to the formation of a Schottky barrier, ϕ_{bn}. At the oxide-semiconductor surface, electrons must overcome this abrupt barrier in order to get from the semiconductor to the oxygen layer.



(a)



(b)

Figure 4.7: (a) The complete energy band representation of Figure 4.6, as atomic oxygen arrives at the surface. (b) Early stages of electron transfer from semiconductor to oxygen when the two materials are separated by ultrathin III-oxide.

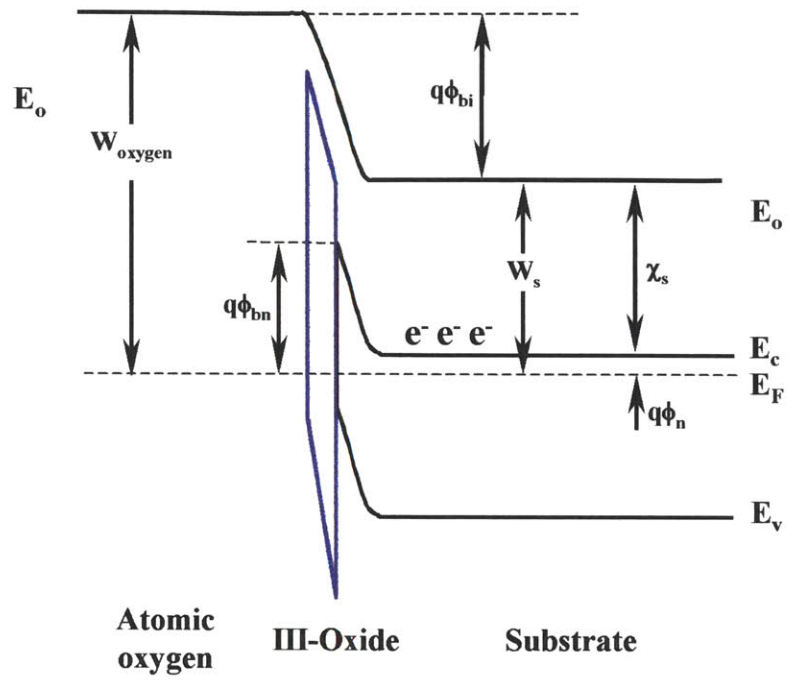


Figure 4.8: Band bending in the semiconductor due to presence of electric field. Charge transfer from semiconductor to oxygen layer continues until electric field gives rise to potential barrier.

Oxide growth proceeds with an intricate combination of both oxygen diffusion and field-aided cation drift through the oxide layer. The Group III atom will react more quickly with any oxygen diffusing through the oxide, but as noted previously, this reaction produces no free electrons. While we acknowledge that Group V atom is slower to ionize, the formation of this cation contributes most to the space charge across the

oxide. The ionization of each Group V atoms yields 5 electrons, and the formation of a charge-neutral V-oxide requires the reaction

$$V_2O_3 = V^{5+} + V^{5+} + O^{2-} + O^{2-} + O^{2-} + 4 \text{ free electrons}$$

We also note from Table 4.1, that with the exception of phosphorus, the ionic radii for the Group V cations are relatively small, while ionic charge is high; therefore, the drift rate for the V-cation will be much higher than that of the III-cation. We must conclude then, that the electric field is sustained during rapid V-oxide growth, and dies abruptly when all the V-cations have combined with O^{2-} anions to form V_2O_3.

Figure 4.9 looks at the growth rate of these oxides in the presence of an electric field. The lengths of the arrows indicate the magnitude of the mobilities of the electrons and cations during charge migration and in the presence of the electric field. These estimates are based on the ionic radii for Group III and Group V elements given in Table 4.1. Appropriate adjustments should be made for phosphide-based compound semiconductors.

Electron diffusion occurs so rapidly that O^{2-} anions form near the surface before oxygen can diffuse through the oxide. Because of their relatively small radii and high positive ionic charge, V^{5+} cations are propelled rapidly towards the surface where they intercept most of the oxygen anions before they can react the III^{3+} cations to form III-oxide. On the other hand, III^{3+} cation drift will proceed at slower rate because of the

larger ionic radii. Some will encounter oxygen anions, but III-oxide formation will be overshadowed by rapid V-oxide growth. When the field dies, however, subsequent oxide growth depends primarily on the diffusion of oxygen through the existing oxide layer.

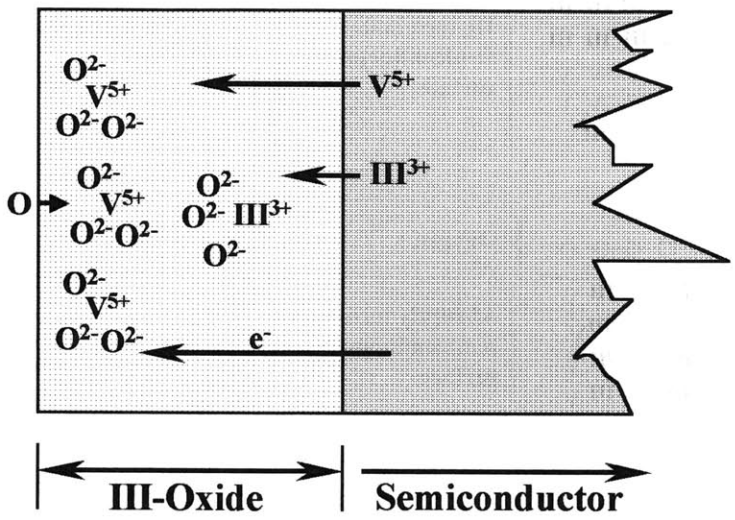


Figure 4.9: III-V oxidation under the influence of the electric field. The lengths of the arrows represent the relative mobilities of electrons and cations as they traverse the oxide. Electron mobility is so high that O^{2-} anions form at the surface before atomic oxygen can diffuse into the oxide. V^{5+} cations exhibit high drift mobility and combine with O^{2-} anions at surface. V-oxide grows exponentially. III^{3+} cations are more sluggish in the presence of the field. III-oxide grows linearly.

Figure 4.10 summarizes III-V oxidation kinetics. Note that because of the different oxidation potentials of the III and V atoms, the end result is expected to be the

same regardless of whether the original semiconductor surface is an abruptly terminated one that mimics the underlying bulk lattice, or whether it is a Group III- or Group V-terminated surface.

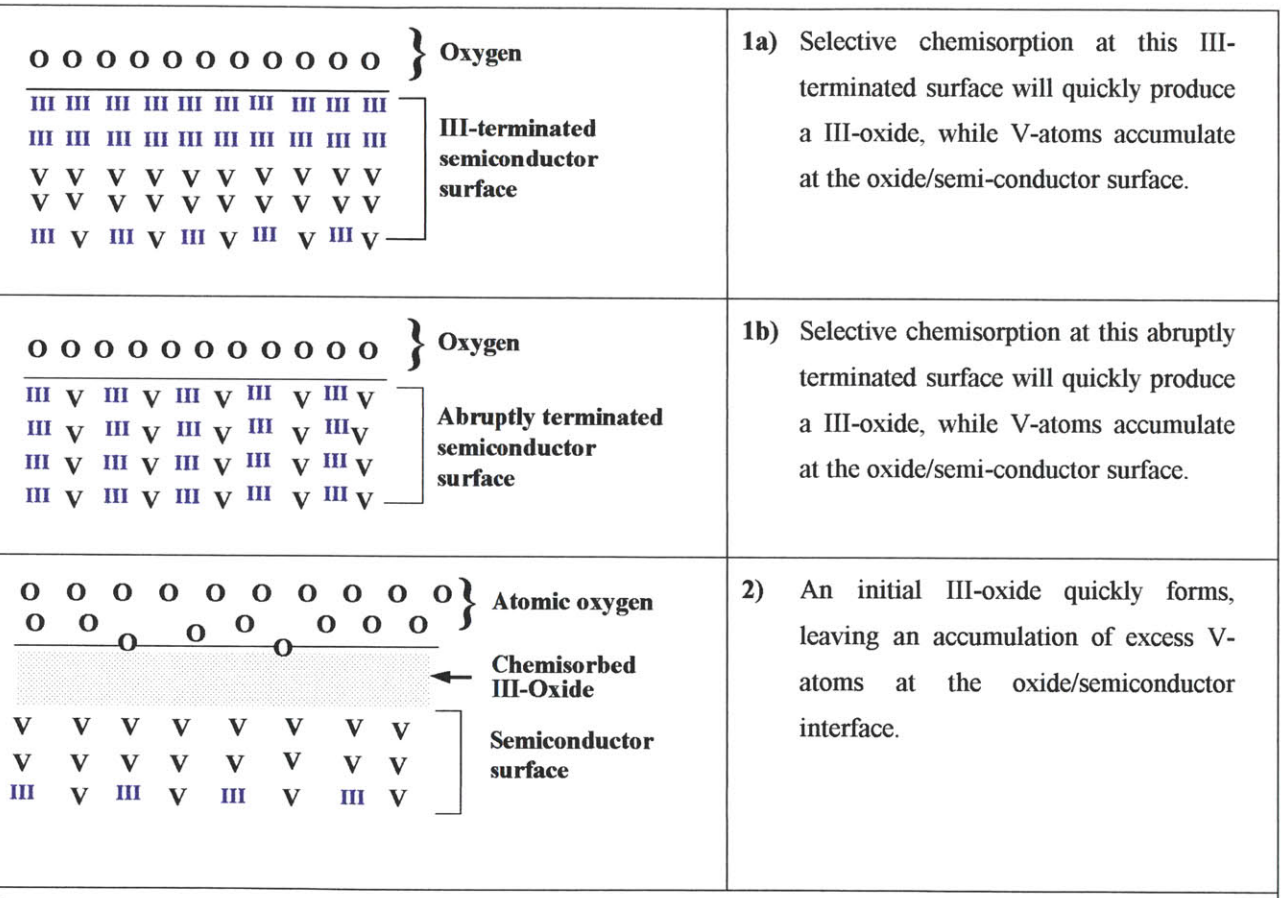
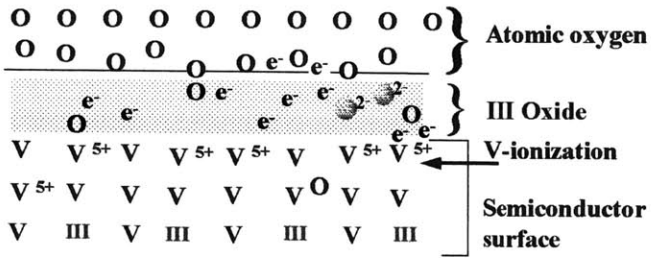
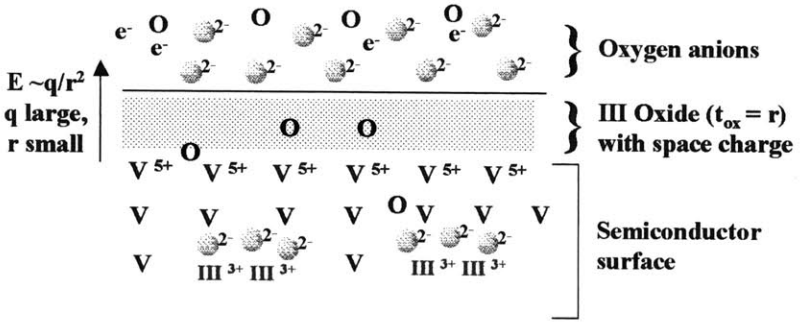


Figure 4.10: Summary of III-V oxidation kinetics

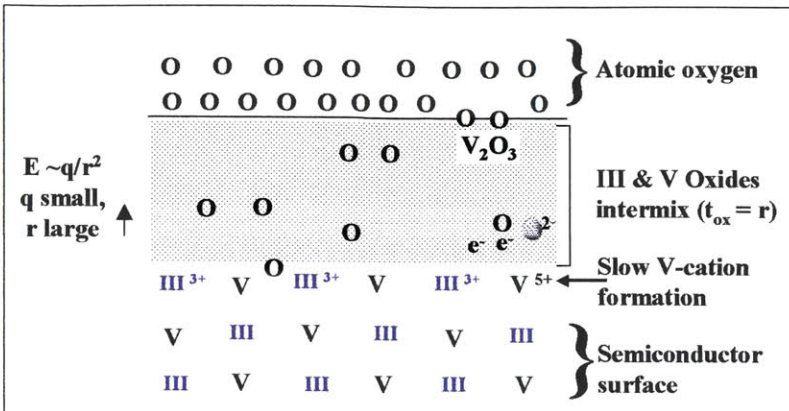


3) Atoms residing at the oxide/semiconductor interface (mostly excess V-atoms) are ionized as electrons in the semiconductor see lower energy states in the oxygen layer across the oxide. These electrons quickly diffuse, creating oxygen anions at the surface. A space charge now exists across the oxide.

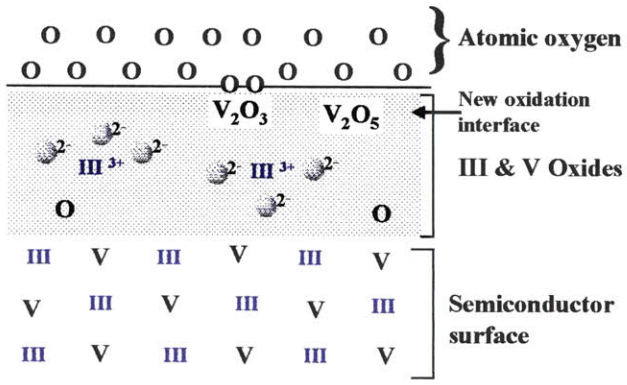


4) An electric field exists across the oxide layer, due to the existence of the oxide space-charge. V-cations drift rapidly, and oxide grows exponentially. Larger III-cations respond more sluggishly to the electric field. III_2O_3 growth rate is linear.

Figure 4.10: Summary of III-V oxidation kinetics, cont'd



5) Eventually, all the excess V-ions and swept out by the field to bond with the surface anions. Exponential growth comes to an abrupt halt as space charge and field dies.. This is characteristic of logarithmic growth.



6) III_2O_3 continues to grow linearly as oxygen diffuses through the oxide. Oxygen at the surface binds to V_2O_3 to form V_2O_5 and a new oxidation interface forms.

At this stage, ionization by oxygen diffusion may cause III-oxide growth to predominate, leaving excess elemental arsenic at the surface. If oxide growth is terminated at this point, a stoichiometric surface results.

Figure 4.10: Summary of III-V oxidation kinetics, cont'd

Stage 1 in the process shows that the untreated surface does not necessarily begin with a III/V ratio that is close to unity. Stage 2 predicts that for very short UV/O_3 exposure times, the III/V ratio will be somewhat less than unity regardless of initial surface conditions. Preferential III-oxidation during this stage results in excess V-atoms

at the semiconductor surface. The surface characteristics at this stage of oxide growth is reported by Driad *et al*, and graphed in Figure 4.5.

Stages 3 and 4 set the mechanism in motion for rapid V-oxide growth. Stage 4 shows that due to the induced electric field, III-oxide will grow linearly because large ionic radii limit cation diffusion. On the other hand, V-oxide will grow exponentially under the influence of the field.

The oxide thickens rapidly during Stage 5. At this stage, the graph in Figure 4.5 climbs, approaching unity as V-oxide growth predominates. As the electric field dies, Stage 6 predicts that further oxide growth must depend on oxygen diffusion through the oxide layer. Oxygen diffusing through the oxide to the substrate surface will continue to oxidize the III-atoms at a quicker rate than it does the V-atoms. Therefore, the III-oxide continues to grow linearly, since growth conditions for this oxide are not affected by the absence of the field. Ionization of the III-atom will again cause a build-up of V-atoms at the oxide/semiconductor interface. This is evidenced in Figure 4.5, as the III/V ratio at the semiconductor surface falls of to values that are less than unity.

A look at the reaction for the interaction of oxygen with V_2O_3 at the surface, no further ionization is required for oxygen to bond with the V-atom in this oxide species.

$$V^{5+} + V^{5+} + O^{2-} + O^{2-} + O^{2+} + O^{2-} + O^{2-} = V_2O_5 + \text{zero electrons}$$

Since the energy expenditure is lower for the formation of these bonds, O_2 will more readily bind with the V-atoms within V-oxide at the free surface than it will with the V-atoms at the semiconductor surface. Therefore, a new oxidation interface will develop as observed by Lu *et al* and graphed in Figure 4.4.

It may be seen from the progress at Stage 6, that halting the oxidation process at some optimal time will lead to a stoichiometric surface, creating the condition for which the energy band diagrams and lattice periodicity is bulk-like all the way to the oxide/semiconductor interface. If one were to characterize the III-V surface after terminating the UV/O_3 exposure at Stage 6, the III/V ratio should be close to unity. If there is a thorough intermixing of the oxides, then a ratio of unity should also be evidenced in this layer. A look at how well Ga_2O_3 and In_2O_3 mix with As_2O_3, will give some insight into the mutual solubility of these mixed oxides.

First, we consider the "like dissolves like" rule associated with the degree of solubility or mixing of a solute in a solvent and apply it to III- and V-oxides -- a polar covalent solid will "dissolve" or mix more thoroughly with another polar covalent solid. Using Figure 4.1, note that the electronegativity difference between As and O is 1.5, so As_2O_3 is polar covalent. The difference between Ga and O is 1.9, making Ga_2O_3 more ionic, while a difference of 1.7 between In and O makes In_2O_3 polar covalent. With respect to polarity, In_2O_3 and As_2O_3 are "like" oxides and relatively more so than are

Ga_2O_3 and As_2O_3 oxides. These differences predict that the oxide mixture on the InAs surface will exhibit better mutual solubility than the oxide mixture on the GaAs surface. Therefore, one would expect the III/V ratio to be near unity for the oxide at the surface of InAs.

Although the previous investigators did not address issues concerning the mixing of the oxides, the foregoing discussion and the model developed in this thesis corroborates the experimental results set forth by Driad and Lu. The model predicts that UV/O_3 oxidation of the InAs surface should follow a similar pattern to that described by these investigators.

Following the Ingrey's technique, oxide layers were grown on three different InAs samples at 10-minute, 15-minute and 20-minute exposure times. The semiconductor surface was then characterized using Angle Resolved X-Ray Photoelectron Spectroscopy.

During this method of characterization, the specimen surface is irradiated with x-rays of known energy, causing electrons to be ejected from the surface. The kinetic energy of these photoelectrons is measured using a hemispherical analyzer; this gives a spectrum with a series of photoelectron peaks. The binding energy values are calculated using the following equation

Binding Energy = X-Ray energy – Electron Kinetic Energy.

The binding energy of the peaks are characteristic of each element and correspond to both the electronic shell and the oxidation state of the atom from which the electron was ejected. Therefore, XPS can be used for both elemental and chemical analysis of the sample surface. The escape depth of the photoelectrons is around 10 atomic layers; therefore, the XPS technique is extremely surface specific.

4.2.2.1 Experimental: UV/Ozone Oxidation of InAs

Three different InAs samples were exposed to UV/O_3 treatment using the Jelight Model 288 UVO Cleaner, and at all times, the samples were positioned at a distance of 20 mm from the UV source. The samples were treated to a thorough solvent clean to remove excess organic contaminants from the surface. All three samples were treated to an initial 10-minute UV/ozone exposure to remove organic contaminants that remained after the solvent clean, and replace them with a UV/O_3 oxide.

Hydrofluoric acid, HF, was added to a buffered oxide etch to produce a 100:1 BOE:HF solution, which was then used to remove the surface oxide layers and H-terminate the semiconductor surface. The samples were each exposed to a final UV/O_3 exposure: Sample 1 for 10 minutes, Sample 2 for 15 minutes and Sample 3 for 20 minutes.

Passivation: Oxidation of InAs

A reference sample was treated to a thorough solvent clean, but was not subjected to UV/O_3 treatment. This sample was used to compare the composition of the untreated InAs surface with those exposed to UV/O_3 oxidation. All surfaces were analyzed by X-Ray Photoelectron Spectroscopy, both at normal incidence, and at 45° glancing incidence.

The spectrum from the surface of the untreated sample shown in Figure 4.11, was taken at a 45° glancing angle. This spectrum may be compared with Figure 4.12, for which the data is also acquired at glancing angle, but taken from the sample treated to 15 minutes of UV/O_3 exposure. The treated sample shows increased surface concentrations of indium, arsenic and oxygen, indicating a marked increase in oxide growth. The carbon signal (occurring at around 300 eV) on the treated sample decreased remarkably, though some carbon is still present and may be accounted for by exposure of the sample to atmosphere subsequent UV/O_3 treatment.

Figure 4.13 shows two species of arsenic oxide on the treated surface. The large peak to the far left of the plot occurs at the binding energy for As in As_2O_3, while the smaller adjacent peak corresponds to As in As_2O_5. The peak at the far right of the plot occurs at the binding energy for As in InAs. Only one indium oxide peak was observed on the exposed samples.

Passivation: Oxidation of InAs

The surface ratio of In/As was measured for the untreated sample at both normal and glancing incidence. In both cases, the untreated sample showed an excess of indium at the surface, with an In/As ratio of 60/40.

The same measurements were made on the treated samples. Sample 1 was exposed for 10 minutes to the UV/ozone radiation, and showed a 55/45 In/As surface ratio. Sample 2 was exposed for 15 minutes, and 48/52 In/As surface ratio was observed. Due to the brittleness of the InAs, Sample 3 broke at loading time and the fragments were too small for XPS analysis.

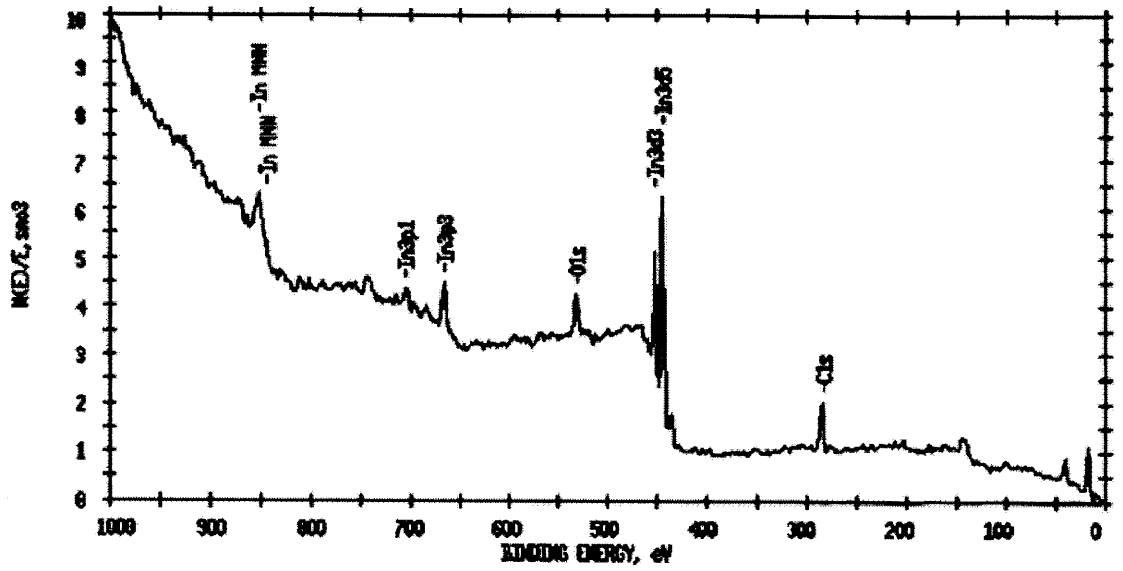


Figure 4.11: Surface spectrum plot, Intensity vs. Binding Energy for unexposed InAs sample.

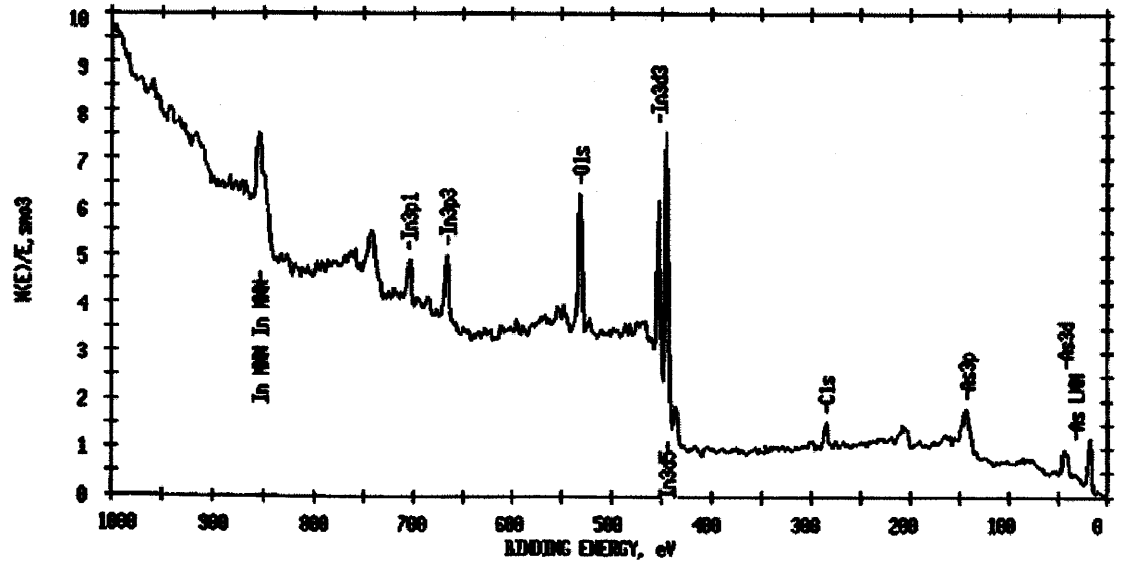


Figure 4.12: Surface spectrum, Intensity vs. Binding Energy for InAs: 15 minute UV/O_3 exposure.

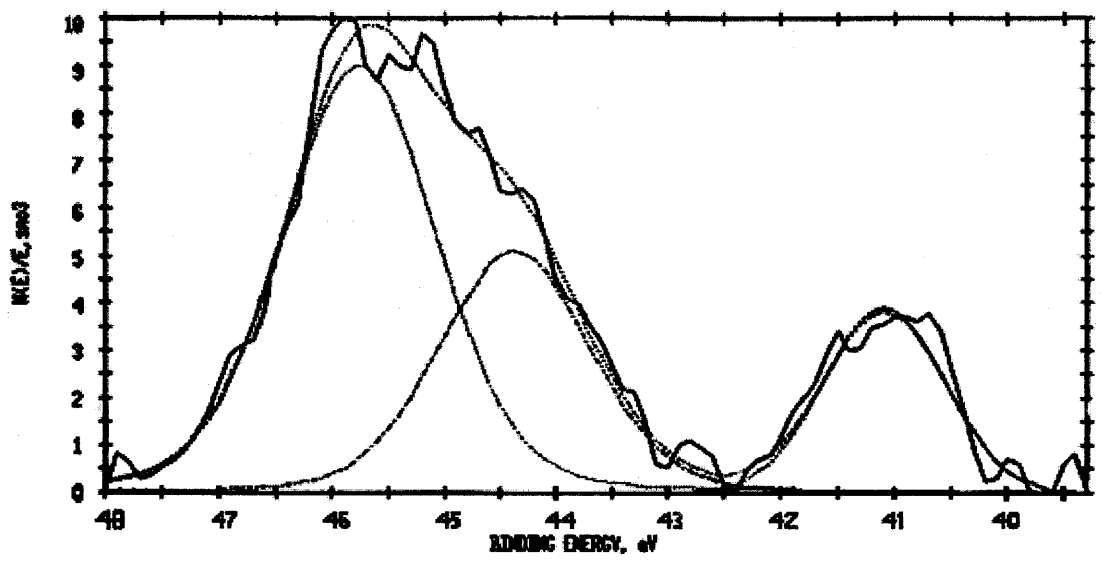


Figure 4.13: Two species of arsenic oxide observed on the UV/O_3 treated surface. The large peak to the far left is the signal for As in As_2O_3, while the smaller adjacent peak is the signal for As in As_2O_5. The peak to the far right is the signal for As in InAs.

4.3 DISCUSSION

The growth of oxides as a means of passivating the III-V surface has so far been problematic. The difficulties associated with the various methods for III-V oxidation were identified in this chapter, and a new method for surface oxidation was explored and

analyzed from the available literature. The method, involving dry oxidation of the III-V surface, with UV/ozone as the source of atomic oxygen, was modeled in this thesis, and its predictions agree well with experimental results. This model may be used to predict the growth patterns for several of the III-V oxides when low temperature UV/ozone oxidation is employed. It explains the growth kinetics of the Group III and Group V oxides and may also be used to determine the mutual solubility of the III- and V-oxides.

UV/ozone oxidation has several benefits which will be outlined below:

1. UV/ozone removes any organic contaminants from the semiconductor surface and replaces the contamination with an oxide layer.
2. A specific sequence of processing steps, obtained from the literature, is designed to remove all traces of native oxide and the contaminants it may contain, and replace it with an oxide grown by UV/ozone treatment.
3. While statements 1) and 2) essentially require that this oxidation method removes the bulk of contaminants from the surface, there is an added benefit to this method of oxidation. Surface stoichiometry is restored in compound semiconductors treated with UV/ozone, making this technique highly attractive for surface preparation prior to epitaxial growth.

One of the benefits of dry oxidation is increased oxide density and low oxide porosity due to low deposition and growth rates. Despite the exponential growth of the

Group V oxides, reports show that 20 minutes of UV/ozone treatment yields an oxide thickness of approximately 26 Angstroms on InGaAs and GaAs. This indicates that the overall growth rate is relatively low, approximately 1.3 Angstroms/minute. However, physical properties must be investigated further in an effort to test the resistance of the oxide to cracking and flaking. The UV/ozone oxide grown on the InAs surface has not been physically tested for these for these characteristics, however, the results confirm that UV/ozone oxide growth is indeed a viable means of restoring InAs surface stoichiometry.

Both the oxide and the semiconductor surface show an In/As ratio that is very close to unity. This shows a high degree of mixing among the In and As oxides, a criterion for overall oxide stability, since the more volatile arsenic oxides are well contained within the more stable indium oxides. This property may also be indicative of the overall oxide density, since the indium oxide grows at a much slower rate and is expected to be more compact than the rapid growing As_2O_3 oxide.

There are certain areas that must be explored in more minute detail. For instance, the model may be used to predict whether a Group V-terminated surface will lead to a thicker oxide layer, but the oxide composition might change, and with it the oxide characteristics. Eventually, III-V oxide properties must be determined and analyzed. It is known that S_iO_2 has a band gap of 9eV, and it is classified as a perfect insulator. Information on the band gaps of these III-V oxides have not been investigated and studies

must be conducted in the future, in an effort to determine the insulating properties of the III-V oxides.

In any event, UV/ozone treatment may be used create a sacrificial oxide in an effort to restore surface stoichiometry. A passivating layer such as PECVD SiN or any other suitable dielectric may be deposited on the restored surface.

Passivation: Oxidation of InAs

CHAPTER 5

HIGH TEMPERATURE EFFECTS

Another point for consideration is the effect, if any, that elevated temperatures might have on the front-side metal contacts to the InAs MTPV cells and to the surface passivation layer. In Section 5.1, high temperature effects on Cr/Au and Ti/Au will be briefly reviewed from the literature and recommendations will be made for future consideration. Section 5.2 will look at the possible temperature effects associated with the use of a oxide layer for the passivation of InAs.

5.1 HIGH TEMPERATURE EFFECTS ON CR/AU FILMS

Since MTPV operation requires that the cell be brought into sub-micron proximity to a heat source for considerably long periods, any adverse temperature effects will influence the operating conditions of these devices. Effects that compromise the integrity

of the metallization layer will undoubtedly undermine device performance, reliability, and lifetime. The following reports from several investigators describe undesirable and potentially detrimental changes that occur in Cr/Au bifilms when exposed to temperatures as low as 280 °C. These reports were analyzed and comparisons were made between the physical chemistry of the described systems and that of the Cr-InAs interface. From this analysis, predictions were made concerning the possible ramifications surrounding exposure of the Cr-InAs surface to a constant source of heat.

5.1.1 Reports of Cr Diffusion in Au at Elevated Temperatures

Researchers have found that at temperatures ranging from 280 – 460 °C, the electrical characteristics of the Cr/Au contact metal changes.

One investigator[47] deposited Cr/Au films on alumina (Al_2O_3) substrates during the fabrication of hybrid microcircuits. A film consisting of 3 μm of Au deposited on 30 nm of Cr, was exposed to a temperature of 300 °C for 2 hours. At the end of the process a 0.8 nm layer of Cr_2O_3 was discovered on the surface of the gold, and the resistance of the gold was found to have increased by 25%.

Munitz *et al*[48] deposited Cr/Au bifilms on a glass substrate. The metal film was then removed and studied at different temperatures. Two different Cr/Au compositions were used; a thin film consisting of 50 nm Au on 30 nm Cr, and a thicker film consisting

of 800 nm Au on 30 nm Cr. Munitz *et al* studied the changes in resistivity when these films were heat treated in air at temperatures ranging from 280 to 460 °C. The resistivity increased at a higher rate during the initial stages of the heat treatment, reached a maximum value, then, at sufficiently high temperatures returned to its original value.

It was also observed, that depending on the temperature and thickness of the film, there is a time limit for which the resistivity reached its maximum value. In the thinner Cr/Au film, the resistivity reached a maximum more quickly than it did in the thicker film. As the temperatures were increased, the maximum resistivity occurred at shorter times in both the 50 nm and the 800 nm Cr/Au films. Both of the groups referenced above independently reported on the presence of Cr_2O_3 in the grain boundaries of the Au film and an accumulation of this oxide on the free surface of the metal.

A model developed by Munitz *et al* showed that Cr diffused through Au film along two independent paths. Diffusion along grain boundaries of the Au film occurred rapidly, while diffusion through the lattice from the Au-Cr interface took place at a slower rate. The combined effect resulted in the covering of the entire free surface of the gold layer with Cr_2O_3 as the chromium is oxidized.

The predictions made by Munitz's model are in direct agreement with empirical observations: initially, the resistance in the metal layer will increase as the Cr diffuses into the gold overlayer, making its way to the free surface where it oxidizes to form

Cr_2O_3. The resistance reaches a maximum when the entire gold layer is saturated with Cr, then drops to its original value when all the Cr diffuses to form a continuous surface oxide layer. As the Cr depletes completely from the metal/semiconductor interface, adhesion breaks down. If one assumes that the grain boundaries run perpendicular to the free surface, then these grain sizes will be smaller for thinner metal layers, causing the resistance to peak earlier in thin metal films.

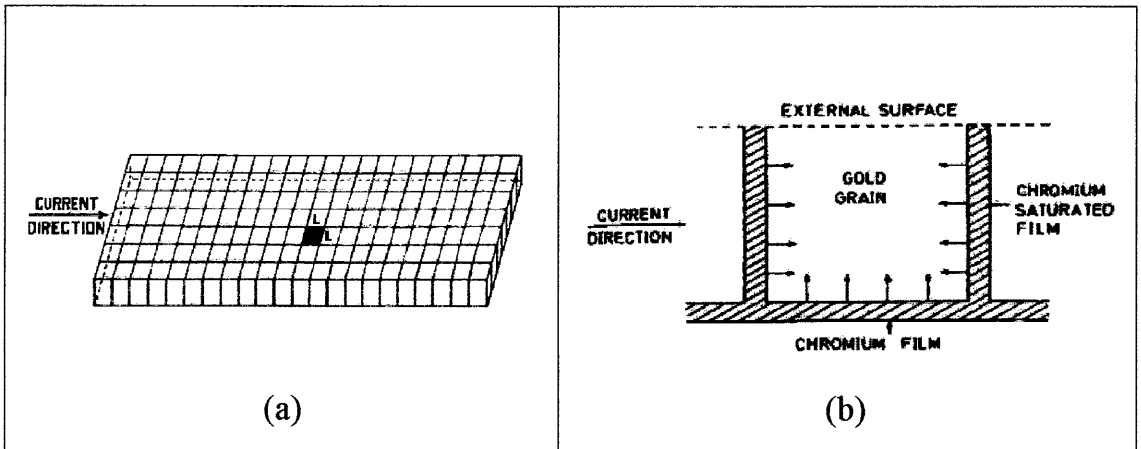


Figure 3.14: (a) A schematic diagram of a gold film containing grains with square cross section. (b) A schematic diagram of a gold grain surrounded by chromium-saturated film. The arrows indicate the direction of diffusion of chromium in the grain. (Munitz *et al*, Ref. #48).

Another source compared the diffusion and oxidation of heat-treated NiCr/Au and Cr/Au films deposited on alumina substrates.[49] Preliminary oxidation studies conducted on both NiCr alloys and chrome films showed that Ni and Cr react differently under different annealing conditions. Cr oxidizes by annealing under vacuum conditions or in

an oxygen-containing ambient. Nickel, on the other hand, will oxidize only in the presence of oxygen.

During sputter deposition of NiCr films, Cr_2O_3 accumulates on the surface and Ni is pushed back, leaving a Ni-rich underlayer. The Cr_2O_3 layer forms a barrier to oxygen, and the quantity of O_2 that reaches the Ni is not enough to produce significant oxidation. The Au layer is deposited on top of this oxidizing film. When the NiCr/Au film was annealed, results depended on the partial pressure of oxygen in the annealing system. Auger spectra revealed that flowing dry O_2 during a two-hour anneal at 560 °C resulted in a 300 Angstrom NiCr oxide layer. However, only a small quantity of Cr_2O_3 was present at the surface when annealing under the same conditions with low partial pressure of oxygen. Thus, at low partial pressures of oxygen, the NiCr/Au metallization system can withstand elevations in temperature without degrading the electrical properties of the Au overlayer or compromising the adhesive properties of the bonding layer.

All sources agree on the effect of temperature on Cr/Au films, but none gave any indication of the existence of a threshold temperature for which this phenomenon occurs. While Munitz *et al* conducted experiments at temperatures ranging from 280 °C to 460 °C, the observations made by Halloway (Ref. #47) are based on the results that occurred at a specific process temperature and duration. The question one might raise here is

whether this temperature range was solely of special interest, and if so, does the out-diffusion of chromium occur at lower than reported temperatures.

The reports from Scatamacchia (Ref. #49) indicate that while Cr will diffuse into and through the gold film at elevated temperatures, it is the sum of the reactions within an ambient-metal-metal-semiconductor system that determines the final outcome. In this vein, we acknowledge that chromium forms an alloy with the InAs surface in its role as an adhesion layer, and that the Cr-InAs bond must first be broken before any out-diffusion can occur. These observations raise a second question: Does the Cr-As bond offer any resistance to Cr diffusion through the Au overlayer?

In effort to answer these questions, a study was made of the solid phases that occur at the Cr/InAs interface

5.1.1.1 The Cr-InAs Interface

A perusal of Figure 5.1 along with the corresponding summary of the solid phases listed in Table 5.1 shows that Cr forms stable arsenides with the InAs surface at temperatures around 25°C. No temperature range is given for which stability is maintained above room temperature, and there is no indication of specific temperatures at which the unstable phases manifest themselves. Similar data was compiled describing the physical chemistry of the Ti-InAs bonds.

High Temperature Effects

A look at Figure 5.2 and Table 5.2 shows that titanium forms stable arsenides at room temperature, but unlike Cr, it also seems to form stable indium alloys. Like the Cr-As alloys, the Ti-In and Ti-As alloys become unstable at elevated temperatures, but again, a temperature range is not given for which stability is maintained above room temperature.

When the data is used in conjunction with known chemical properties, some insight may be gained about the true thermal stability of the Cr-As, Ti-As and Ti-In bonds. The valence shell electron configurations for the various elements involved are given as

As: $4s^2 4p^3$

In: $5s^2 5p^1$

Cr: $3d^5 4s^1$

Ti: $3d^2 4s^2$

Chromium is a transition metal for which the energies of the 4s and 3d orbitals are very similar. Electrons in degenerate orbitals first occupy each orbital in an effort maintain the lowest energy configuration. Therefore, the 4s and 3d orbitals will each contain a lone electron, and the bond between Cr and As consist of low-energy single bonds that are easy to break at temperatures not significantly above room temperature. With the ΔH° values for Cr-As as an indicator, it becomes clear that the Ti-In compounds will

require little thermal energy to stimulate the breaking of these bonds. The Ti-As bonds are somewhat stronger, but these values for enthalpy are still not very high. While these bonds might not break as easily as Cr-As bonds, they might be susceptible to prolonged exposure to temperatures that are not significantly higher than 25 °C.

Figure 5.1: Ternary Phase Diagram: Cr-InAs Interface [50]

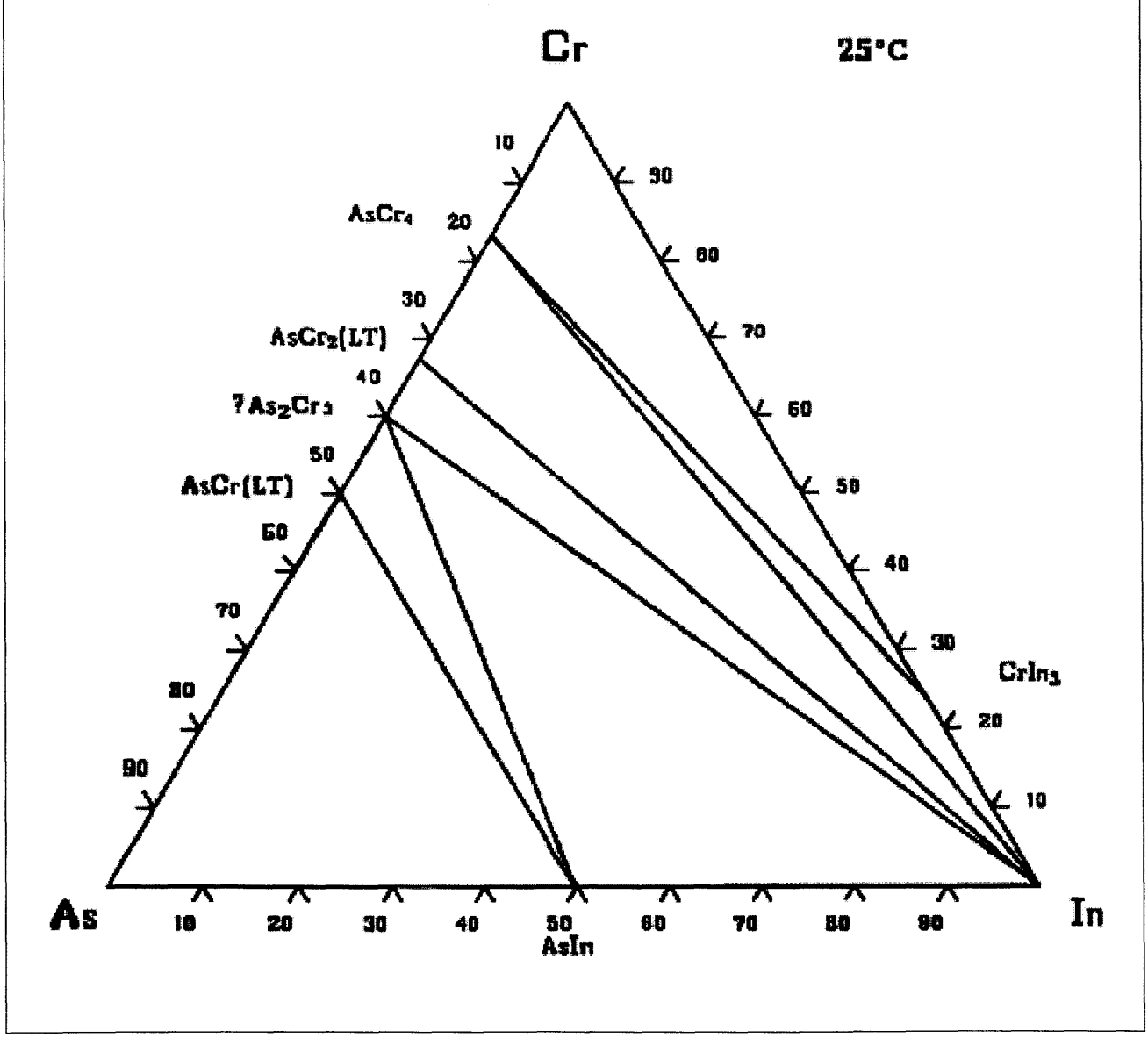


Table 5.1: Cr-InAs: stable and unstable phases[51]

Room Temperature Phases			
System	**Phase**	**ΔH^o (kJ/g atom)**	**ΔG^o (kJ/g atom)**
In-Cr	$CrIn_3$	+7.7	-1.0
As-Cr	Cr_5As	-25.0	
	Cr_2As	-44.8	
	Cr_3As_2	-48.1	
	CrAs	-47.6	
High Temperature Phases			
System	**Phase**	**Stability range**	**Questionable Stability**
As-Cr			Cr_4As
			Cr_5As_3
			Cr_5As_2

Figure 5.2: Ternary Phase Diagram: Ti-InAs Interface [52]

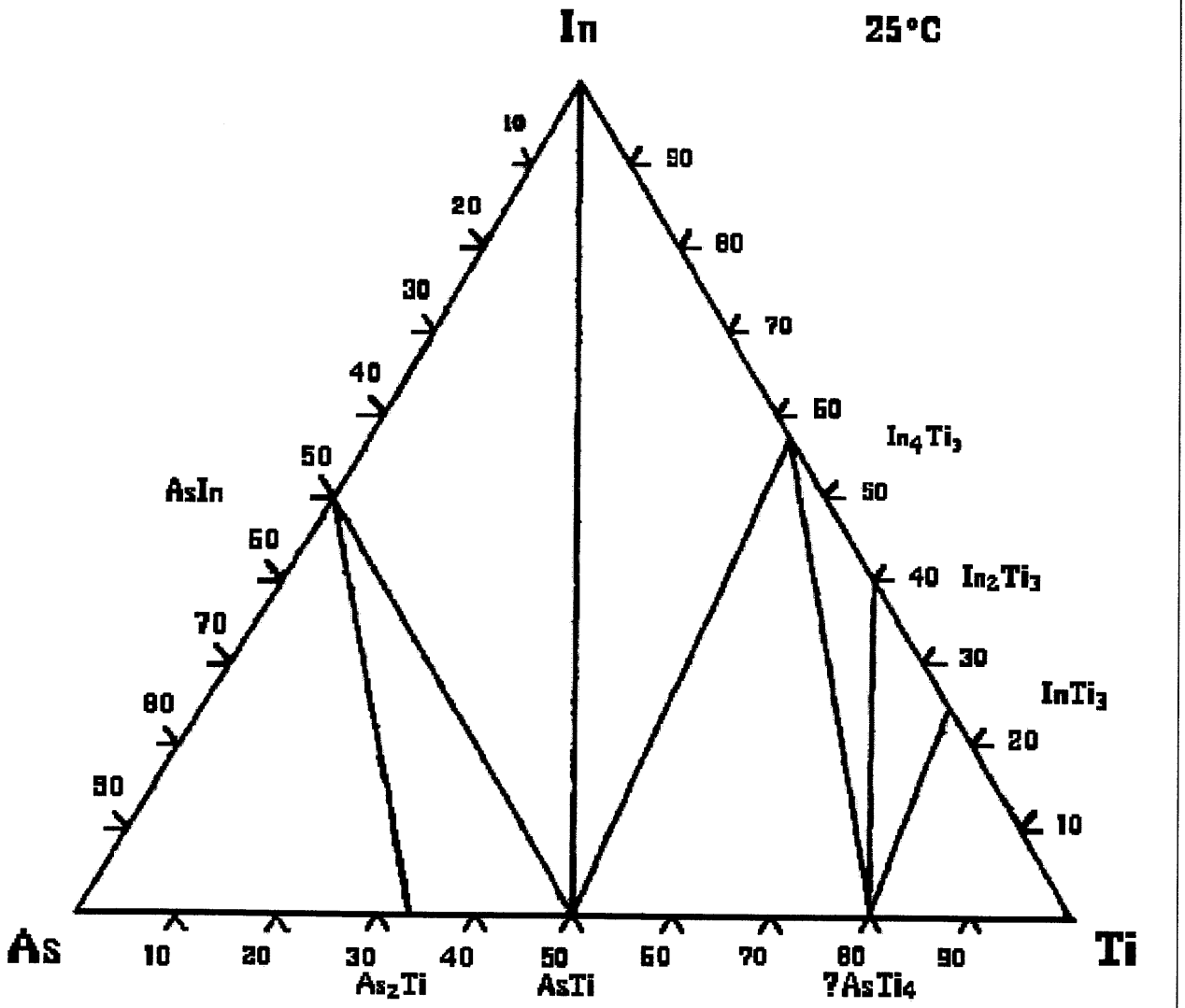


Table 5.2: Ti-InAs: stable and unstable phases [53]

Room Temperature Phases			
System	**Phase**	**ΔH^o (kJ/g atom)**	**ΔG^o (kJ/g atom)**
In-Ti	Ti_3In	-18.5	
	Ti_3In_2	-24.9	
	Ti_3In_4	-23.2	
As-Ti	Ti_4As	-61.6	
	TiAs	-110.3	
	$TiAs_2$	-86.5	
High Temperature Phases			
System	**Phase**	**Stability range**	**Questionable Stability**
In-Ti			$TiIn_3$
As-Ti			Ti_3As
			Ti_5As_3
			Ti_4As_3

5.1.2 SUMMARY AND ANALYSIS OF REPORTS ON CR DIFFUSION IN AU

Having examined the various experimental data related to the effects of high temperature on Cr/Au films, comparisons will now be made between the experimental conditions and the Cr/InAs and Ti/InAs systems described above. A careful study shows

that essentially, all three experiments involving Cr/Au films show the same experimental conditions, and that these conditions closely resemble the Cr-InAs and Ti-InAs interface under high temperature conditions.

First, consider the Au/Cr-InAs system that makes up the surface structure of the InAs MTPV cell. Since a thin native oxide is expected form on the InAs surface prior to metal deposition, Figure 5.3 is the proposed schematic representation of the structural topography. In this scheme, Cr will bond with As at the semiconductor surface, and it will also bond with both As and oxygen in the InAs native oxide layer. When Cr-As bonds become unstable at temperatures significantly above 25 °C, As will diffuse back to the InAs surface and only Cr-O bonds will remain. The structure will resemble Figure 5.4, and will primarily consist of a Au-Cr-O system.

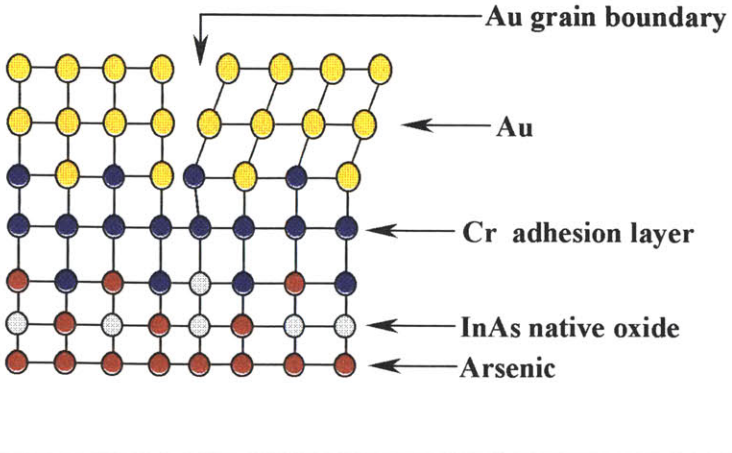


Figure 5.3: Au/Cr-InAs Structure

Halloway (Ref. #47) and Scatamacchia (Ref. #49) both deposited Cr/Au on Al_2O_3, with Cr as the adhesion layer to the substrate. Cr has an electronegativity value of 1.6, compared to 1.5 for Al and 3.5 for Au. Hence, the Cr-Al bond is weakly covalent and is essentially unstable. Thus, in the Cr-Al_2O_3 system, the bond of interest is a Cr-O bond with Au deposited onto the Cr layer as depicted schematically in Figure 5.4.

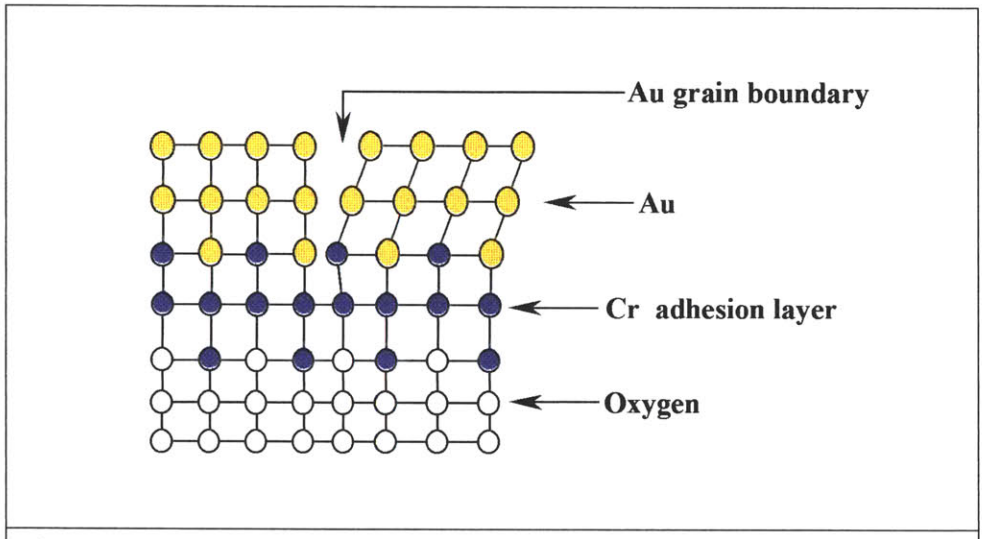


Figure 5.4: Au-Cr-O Structure

Munitz et al deposited Cr/Au films onto glass substrates, then subsequently removed these films and exposed them to oxygen-containing air. The exposed Cr will oxidize rapidly in air, and the situation is the same as described above – a Cr-O bond with Au deposited onto the Cr layer.

High Temperature Effects

In all three experiments, heat treating this Au-Cr-O system leads to the same results until another substance is added.

In the later experiments conducted by Scatamacchia, a NiCr film replaces Cr as the adhesion layer to the alumina substrate. Due to its higher oxidation potential, Cr oxidizes first during deposition in a vacuum to form a surface layer of Cr_2O_3. At atmosphere, oxidation would proceed in similar fashion to that described in Chapter 4 for the oxidation of III-V compounds. In this case, however, the partial pressure of oxygen is too low for further oxidation of Cr, and not enough to activate the ionization of nickel.

The gold layer is deposited on this structure – NiCr with a thin surface Cr_2O_3 oxide scale. Upon contact, NiCr dissociates into Ni and Cr, which diffuse through the Cr_2O_3 barrier to form an alloy with the gold overlayer. We know that this is a simple diffusion rather than an ionization-drift process because from Table 5.3, the Ni-Au and Cr-Au electronegativity differences show that these bonds will be strongly covalent by not very polar. Also note from Table 5.3 we note that due to the relative atomic radii, both Cr and Ni will form substitutional alloys with Au, as a means of establishing a bond between the NiCr layer and the Au overlayer.

As temperature increases and the atoms in the solid vibrate more energetically, substitutional atoms relocated themselves in the lattice by occupying vacant sites. The probability that a vacancy exists increases with increasing temperature and atoms must

gain enough energy (activation energy) to overcome the energy barrier and break free of the bond. Diffusion along grain boundaries will occur at a faster rate than diffusion through the lattice, since there is no energy barrier to overcome. This mode of transport is highly favored, due to the relatively small radii of the diffusing atoms compared to the widths of the grain boundaries.

During annealing, transport of Ni and Cr occurs along the grain boundaries with Ni diffusion occurring at a faster rate due to its smaller atomic size. If the partial pressure of O_2 is low, only a little Cr will oxidize, and the initial Cr_2O_3 forms a protective overlayer against further oxidation. If the partial pressure of O_2 is high, however, the driving force for Ni and Cr oxidation is high and strong oxidation occurs across the Cr_2O_3 surface layer. Eventually, the NiCr bonding layer will be lost and the gold metallization will be compromised.

Table 5.3: Properties of Various Metals and their oxides[54]

Element	Configuration (# electrons)	Electronegativity	Atomic Radius (Angstroms)	Oxidation States	Ionic Radius (Angstroms)
Al	$3s^2 3p^1$ (13)	1.5	1.43	+3	0.51
Au	$6s^1 5d^{10}$ (79)	2.4	1.44	+3	1.37
Cr	$4s^1 3d^5$ (24)	1.6	1.30	+2, +3, +6	0.63
Cu	$4s^1 3d^{10}$ (29)	1.9	1.28	+1, +2	0.72
Ni	$4s^2 3d^8$ (28)	1.9	1.24	+2	0.69
O	$2s^2 2p^4$ (8)	3.5	0.73	-2	1.40
Ti	$4s^2 3d^2$ (81)	1.5	1.47	+2, +3, +4	0.68

Metal Oxides

	ΔH_f° (kJ/mol)	ΔG_f° (kJ/mol)	
Al_2O_3	-1676	-1582	ΔH_f° is a measure of bond strength.
Cr_2O_3	-1128	-1047	
CrO_3	-597	-502	ΔG_f° is a measure of how readily the oxide will form.
Cu_20	-170	-148	
CuO	-156	-128	
NiO	-241	-213	
TiO_2	-945	-890	

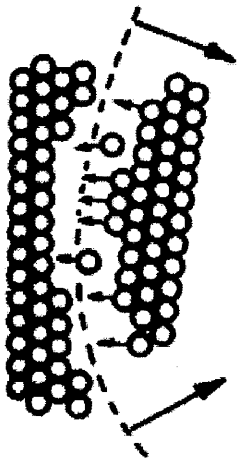
Two main points are made clear in the above analysis: First, all reports indicate that the presence of grain boundaries play an important role in the out-diffusion and loss of the adhesion layer. Second, the results of the NiCr experiment under low partial pressure of O_2 indicate that given the right conditions, selective oxidation may occur when an alloy is used to bond to the semiconductor surface. This selective oxidation inhibits the oxidation of the other constituent of the adhesion layer.

In light of these two points, it might be possible to introduce a new metal that would suppress Cr out-diffusion and oxidation in much the same way that Cr was used to suppress Ni oxidation under low partial pressure of O_2. If at the same time, it is possible to induce grain growth to drastically reduce the density of grain boundaries, then the Cr bonding layer will remain intact and the integrity of the Au metallization will be preserved.

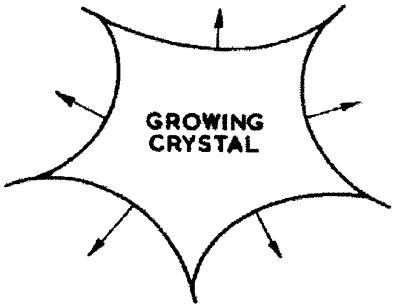
5.1.2.1 Grain Boundary Elimination

With regard to the first point, it is well known that metals re-crystallize at elevated temperatures.[55] The minimum temperature at which re-crystallization occurs is lowest for pure metals—often below room temperature—and is raised significantly if even the smallest amounts or impurities are present. Halloway (Ref. #47) examined the gold films that were annealed at 300 °C to discover gold "nodules" consisting of several grains.

Besides temperature, grain size is also a driving force for re-crystallization, since the high energy associated with the congregation of dislocations at grain boundaries initiate grain growth at temperatures above the re-crystallization threshold.



(a)

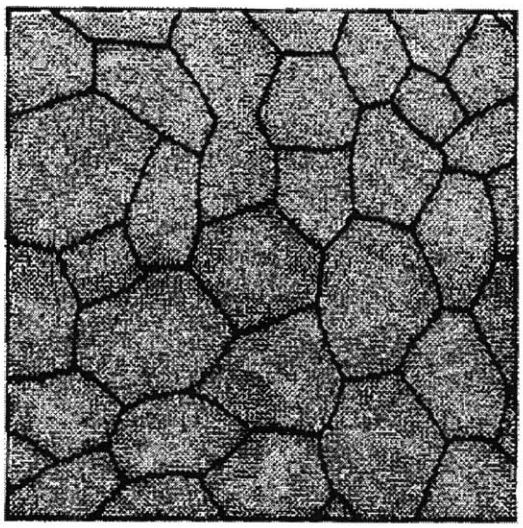


(b)

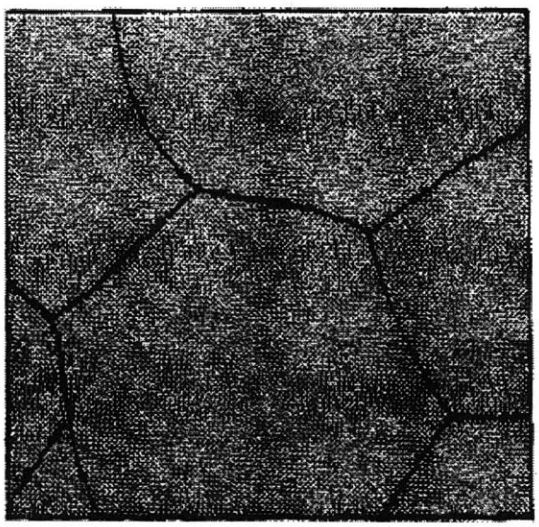
Figure 5.5: (a) Grain growth, through grain boundary migration, decreases the free energy associated with the high density of grain boundaries in the metal. Grain growth proceeds at the expense of its neighbors. (b) Boundary moves towards center of curvature. (Higgins, Ref. #55)

Grains will increase in size by consuming adjacent grains through the migration of their boundaries as shown in Figure 5.5 a). Energy is released as an atom moves across the boundary from the grain with the convex surface to the grain with the concave surface. An atom making such a transition is, on the average, coordinated with a larger number of neighbors at equilibrium inter-atomic spacings. As a result, the boundary moves toward the center of curvature. Since small grains tend to have boundaries with higher degree of convexity and sharp angles than do large grains, they tend to be quickly consumed by the larger grains – the net effect is grain growth as shown in Figure 5.6.

Thus, a finer initial grain accelerates the process of re-crystallization, resulting in the rapid elimination of grain boundaries.[56]



(a)



(b)

Figure 5.6: Excess free energy is stored in the grain boundaries. (a) A metal with a high density of grain boundaries that exhibit high convexity and sharp angles. (b) Resultant grain growth during exposure to elevated temperatures.

Finer size grains may be produced in Au metal films by carefully monitoring the deposition rate. Unlike semiconductors, metal surfaces are atomically rough due to weak covalent bonding among the metal-metal atoms. When the Au film is deposited onto a metal adhesion layer, a low deposition rate allows adatoms to orient themselves with the surface, allowing many small grains to grow.[57] Figure 5.7 shows the atomically rough

metal surface, with arrows indicating the possible location and orientation of crystal grains at low and high deposition rates.

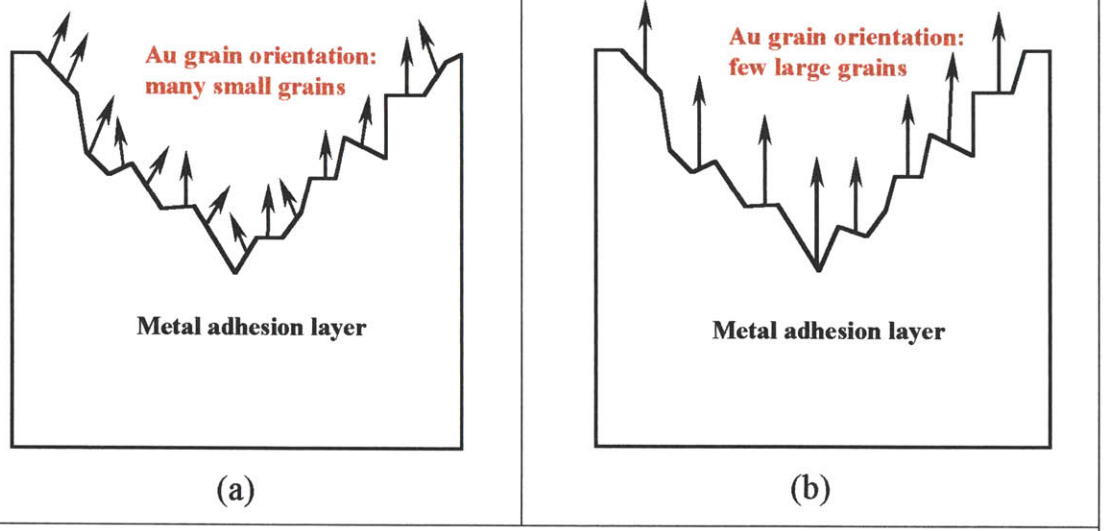


Figure 5.7: Deposition of Au film onto metal adhesion layer at (a) low deposition rate (b) fast deposition rate. The arrows show the possible location and orientation of the crystal grains.

In Halloway's article (Ref. #47), the author mentions a gold deposition rate of 2 – 3 nm/second, a rate that is 10 times faster than the deposition rate used for MTPV. Such a high deposition rate could have produced a coarse-grained metal, and if this is the case, the driving force for grain growth would have been low. At the same time, out-diffusion of Cr into the gold grain boundaries would have slowed grain growth further, allowing all the Cr to diffuse to the surface and oxidize.

For the process described in this thesis, the deposition rate is considerably low, 2 – 3 Angstroms/sec, and is ideal for the generation of small, dense crystal grains. There is no certainty, however, that grain growth will exceed the rate of grain boundary diffusion of the Cr under layer. This brings us to the second point raised by the analysis of the literature.

5.1.2.2 Suppression of Cr Out-diffusion and Oxidation

In similar fashion to the NiCr experiment, a metal that oxidizes more quickly than Cr may be introduced to the Cr adhesion layer. An anneal step may then be performed with this metal functioning as nothing more than a sacrificial oxidant to suppress Cr oxidation until grain growth is complete. Note that any impurities residing within the grain boundary will prohibit the motion of the Au atoms and impede grain growth. Thus, this metal (possibly aluminum) must be present in small enough quantity to diffuse quickly through the Au grain boundary during initial heat exposure to form a surface oxide layer.

The goal is to have initial grain sizes of small enough proportion so that most, if not all, grain boundaries will be eliminated during the anneal. After this process step, the Cr should be well contained beneath a single-crystalline gold layer, so that any subsequent high temperature operation would not result in Cr out-diffusion.

5.2 High Temperature Effects on Oxide Passivation Layer

The high temperature characteristics discussed in Sections 5.1.1 and 5.1.2 indicate that without a workable solution to the Cr out-diffusion problem, surface passivation by UV/O_3 oxidation may be restricted to use with metallization schemes that employ metal alloys rather than Cr/Au or Ti/Au bifilms.

A report on silicon out-diffusion into the gold grain boundaries when annealed at 250 °C[58] demonstrates that this phenomenon is not limited to Cr/Au films and that the possibility of out-diffusion of one or more of the III-V constitutive elements is possible at high enough temperatures. These possibilities must be investigated, and corrective methods must be employed where necessary.

In addition to the above concerns, the oxide itself might undergo dissociation at high enough temperatures, due to the volatility of arsenic, which sublimes at temperatures around 450 °C.

Since these cells will be constantly exposed to a heat source at close proximity, thermal stability of InAs oxides is a primary concern. Mutual solubility of the indium oxide in the III-oxide will determine how well these oxides will mix, as well as how one oxide will modify the characteristics of the other. For instance, any dissociation of As_2O_3 will result in indium or gallium forming bonds with the free oxygen, while the free

arsenic will diffuse to the oxide/semiconductor interface and accumulate there. On the other hand, In_2O_3 and Ga_2O_3 tend to decompose at much higher temperatures. One source reports that In_2O_3 decomposes at temperatures around 2000 °C.[59] If the Group III and Group V oxides are mutually soluble, a thorough intermixing will "screen" V-oxides like Sb_2O_3 and As_2O_3 from high temperature effects, causing dissociation to occur at temperatures that exceed the operating temperature of the MTPV cells.

It was predicted in the previous chapter, that due to the polarity of the oxide bonds, In_2O_3 and As_2O_3 were mutually soluble oxides. This prediction was substantiated by surface characterization, which showed an In/As ratio of unity for the surface oxide composition.

5.3 DISCUSSION

While the MTPV cells will be cryogenically cooled during operation, sub-micron separation between the cell and a heat source operating at temperatures that may exceed 800 °C is expected to cause some degree of front surface heating. The possible effects that prolonged high temperature operation might have on the Au/Cr metallization and surface passivation layers have been examined and analyzed.

It was determined that the mutual solubility between the indium and arsenic oxides is conducive to maintaining overall thermal stability of the InAs surface oxide layer.

On the other hand, reports on the breakdown of Cr/Au films during exposure to temperatures as low as 280 °C raises some concerns surrounding the thermal stability of the top surface metal contact.

The phenomena described in this chapter is not limited to the Cr/Au system; as mentioned previously, similar effects occur when gold is deposited onto Si and SiO_2 substrates and annealed at 250 °C (Ref. #58). The gold deposition rate was low, 1 Angstrom/second, and physical examination revealed that grain growth occurring near the Au/SiO_2 interface prohibited further SiO_2 out-diffusion. SiO_2 accumulation in the grain boundaries near the free surface was also shown to prevent grain growth in that region. Also note that the because of the physical chemistry and kinetics involved, the phenomena surrounding thermally induced out-diffusion of underlying material is not restricted to gold metallization.

Analysis of the reports on the Cr/Au metallization system led to the formulation of a possible solution to the problem of Cr out-diffusion. The proposed solution is based on the results from the Au/SiO_2 system and on the analysis of the Au/NiCr system. In the Au/NiCr system, oxidation appears to proceed in similar fashion to the oxidation of InAs as outlined in Chapter 4, with Cr exhibiting the higher oxidation potential that allows it to

oxidize more readily than the Ni. In this case, however, further oxidation does not take place across the initial chromium oxide layer when conditions do not favor the ionization and oxidation of Ni – Ni oxidation is suppressed.

The proposed solution stresses the importance of a low deposition rate for the gold film in an effort to create a fine-grained gold layer. A subsequent anneal should invariably activate rapid grain growth and produce a single-crystalline gold film. The underlying adhesion layer should contain sacrificial metal that oxidizes more quickly than Cr, in an effort to suppress chromium oxidation during grain growth. High oxidation potential in this sacrificial metal should enable it to diffuse quickly through the Au grain boundaries at a rate that exceeds grain growth, so that only a surface oxide of this material is formed.

In this proposed scheme, the sacrificial metal-oxide will reside at the surface of the gold; grain growth will have proceeded without any interruption from the oxidizing metal, leaving the Cr layer well contained beneath the gold layer with no possibility of out-diffusion. Any subsequent exposure to high temperatures would leave this system intact and well protected from oxidation-corrosion effects.

CHAPTER 6

CONCLUSIONS

Chapter 1 introduced the need for sustainable energy suitable for deep space exploration. To date, Radioisotope Thermoelectric Generators (RTGs) have been a source of sustainable power in areas where solar cells have failed – at distances far removed from the effects of the sun's rays. The RTG has a rigid structure that consists of no moving parts, and a constant supply of energy from a nearby heat source. Together, these two characteristics impart to these devices a robustness and a high degree of reliability that has so far remained unrivaled. However, poor efficiency limits the amount of power that may be extracted from RTGs.

Microscale thermophotovoltaic (MTPV) cells offer the reliability of the RTG, the compactness of the solar cell, and the promise of high power extraction. The MTPV system has one unique feature: sub-micron distance between a thermophotovoltaic (TPV)

cell and its heat source is the catalyst for radiation tunneling effects that greatly increase the amount of energy that may be transferred from source to cell. With this extra energy input, conversion will inevitably lead to power extraction that is predicted to be more than 10 times greater than the output of today's TPV cells.

InAs was chosen for the fabrication of the MTPV cells because of its optical properties; relatively high refractive index, high carrier mobility, low carrier effective mass, and a narrow energy bandgap that is well matched to radiation in the infrared.

A full process was developed for the fabrication of InAs converter cells. A suitable etchant has been identified with good control established over the etch rate. In addition, a full photolithographic process has been developed for the application of three types of photoresists on InAs: OCG825-20 positive resist, AZP4620 thick positive resist and AZ5214E image reversal. These resists were used as etch masks for the junction isolation etch and as a mask for the deposition of the front surface metal contact.

The most common metallization schemes used with III-V compound semiconductors include gold as a primary element. A brief discussion was given, concerning the benefits of using a non-alloyed versus an alloyed gold film as the metal contact to InAs. It was shown that because of the electronic structure of InAs, ohmic contact could easily be achieve when bifilms of Cr/Au or Ti/Au were deposited on the *n*-InAs surface.

The method of deposition was also an issue for discussion. Sputtering requires the deposition of the metal films over the entire substrate surface and systematically etching the metal layers. This restricts the choice of metal for the adhesion layer, since the metal etchant might also etch the underlying substrate, as is the case with Cr.

Another cause for concern is the ongoing effects of the chemicals used to etch the metal layers. Gold etchants contain iodine, and a very dilute HF was used to etch titanium. It has been shown that if even trace amounts of the halogens iodine and fluorine remain on the surface of the metal, severe erosion of the gold metallization layer will occur.

When electron beam evaporation is employed for metal deposition, good adhesion becomes an issue. Metal is deposited over a layer of patterned photoresist and the final metal pattern is achieved through a liftoff process that involves the dissolution of unwanted photoresist. When a straight-walled, positive resist is used, over baking during the post bake step can make resist dissolution difficult and may lead to tearing of the metal lines. In an effort to avoid these conditions, the post bake temperatures and times were reduced as indicated in the process flow in Chapter 3. With regard to surface roughness in the metal layer, best results were obtained when a tungsten crucible was used instead of graphite, and the deposition rate was set at 2-3 Angstroms/second. High

vacuum conditions (around 10^{-8} Torr) ensured the purity of the films, as impurities of the chamber became less mobile and less apt to be incorporated into the metal layer.

Surface passivation was another topic for discussion, and Chapter 4 was dedicated to the study of UV/Ozone oxidation of III-V semiconductor surfaces. A typical UV system uses two characteristic wavelengths; the shorter wavelength dissociates molecular oxygen to create a dry oxygen ambient, while the longer wavelength dissociates ozone to create molecular oxygen and facilitates the dissolution of hydrocarbons from the semiconductor surface. UV systems operate at relative low temperatures, less than 70 °C, and oxidation of a semiconductor surface using this method produces a thin film oxide.

Because of the way in which the III-V surface oxidizes under initial exposure to the atmosphere, care must be taken to remove surface hydrocarbons and native oxide before a passivating layer is deposited. Native oxides may incorporate metallic and organic contaminants. One source described a method for surface preparation using UV/Ozone treatment, while another source used the method successfully on InGaAs/InP HBTs with a marked current gain and a reduction in the device ideality factor. The current gain was lost, however, when a dielectric layer was deposited after UV/Ozone treatment, but without the removal of the native oxide. The passivation was once again

successful when the UV/Ozone treatment was followed by an etch to remove the native oxide before deposition of the passivating layer.

A model was developed in this thesis for low-temperature, dry oxidation of the III-V semiconductor surface. This model for oxide growth follows the energy band theory for two materials with different work functions, and involves the ionization of the III-V constitutive atoms by oxygen atoms accumulation at the semiconductor surface. Oxide growth kinetics proceed with a combination of electric field induced cation drift, oxygen diffusion and oxide interdiffusion.

The model shows that regardless of the initial surface stoichiometry, a stoichiometric surface is obtained when UV oxidation is time controlled. This is verified by experimental results from UV/Ozone exposure of two InAs samples. An initial non-stoichiometry with an In/As surface ratio of 60/40 was corrected by a 10-minute exposure yielding a 55/45 In/As ratio, and was further improved when a 15-minute exposure yielded a 48/52 In/As surface ratio. The passivation effects have not yet been tested on InAs cells, and the electrical properties of the oxides are still unknown.

Theoretically, the model predicts a thorough mixing of the indium and arsenic oxides, a necessary condition for thermal stability, since In_2O_3 decomposes at temperatures greater than 2000 °C while As_2O_3 dissociates at much lower temperatures.

The mixing of the oxides ensures that the arsenic oxide is well contained within the indium oxide to give overall InAs oxide stability at elevated temperatures.

Cr/Au metallization layers do not fare quite so well under exposure to high temperature conditions. Several sources report on the out-diffusion of Cr into the grain boundaries of the gold over-layer when Cr/Au films are annealed at temperatures as low as 280 °C. Further investigation into the literature shows that this phenomenon is not limited to Cr/Au metallization systems; Ni also diffuses through the Au grain boundaries when an anneal is performed at atmosphere. One source also reports of silicon and SiO_2 diffusion through gold grain boundaries after an anneal at 250 °C.

A study of grain growth within metal films was conducted in this thesis, and key points were noted concerning the relationship between grain boundary movement and material out-diffusion. All metals, including copper and gold, undergo grain growth when annealed above the re-crystallization threshold temperature. If the device is exposed to temperatures below the re-crystallization threshold, no grain growth occurs and grain boundaries will remain, providing open channels for material out-diffusion and oxidation. At temperatures above the re-crystallization threshold, grain boundaries will move as grain growth proceeds. However, any impurities residing in the grain boundaries will impede grain growth; grain boundaries will remain open and out-diffusion will occur as observed by the investigators quoted in this thesis. It may be

possible to engineer the entire mechanism for grain growth and out-diffusion so that the former will proceed at a rapid rate, while the latter is suppressed. With the grain boundaries greatly reduced, and the gold assuming a single-crystalline structure, out-diffusion should be curtailed, even when the device is subsequently exposed to high temperatures.

The following method was proposed for the control of Cr out-diffusion in the grain boundaries of gold films:

1. The Cr layer should be deposited as usual, followed by a layer of thin metal; the gold should then be deposited onto this film at a low deposition rate.
2. The thin layer should consist of a metal with a higher oxidation potential than Cr. This will be a sacrificial metal which will be used to suppress Cr oxidation during a thermal anneal that follows directly after the metallization step. Just enough of this metal should be deposited to allow complete diffusion to the surface of the gold layer. A surface oxide of the sacrificial metal will form, isolating the Cr from the oxygen atmosphere.
3. It is expected that: (a) out-diffusion if the sacrificial metal will exceed grain growth so that none of this metal or its oxide is trapped between the gold grains where in can inhibit grain growth; (b) Cr oxidation will be suppressed in such a way that grain growth will exceed subsequent Cr oxidation.

4. When grain growth proceeds, the Cr will be well contained beneath the gold layer with no open channel for out-diffusion.

Experiments must be conducted with the underlying cell structure in mind. The decision must be made as to whether it is feasible to use a short, high-temperature anneal to activate grain growth or whether it is better to use a lower temperature anneal for a longer period of time.

Devices have been fabricated without the benefit of surface passivation, and without the application of the proposed metallization treatment. While the devices exhibited diode behavior, current-voltage characteristics indicate that these devices were very "leaky" and a value of 2 was obtained for the ideality factor. In spite of this, preliminary results from optical characterization reveal a short-circuit current of 0.22 milliamps and an open-circuit voltage of 95.3 millivolts observed at emitter-cell spacings as large as 1 mm and an emitter temperature of 500 °C.

These preliminary results are optimistic, considering the aforementioned current-voltage characteristics and the large device area that allows carriers to recombine before they are able to reach the metal contacts. A mask more complex mask set has been designed, incorporating devices of various sizes in order to investigate the effect of a device size on its performance. The process developed in this thesis will be used for the fabrication of more complex MTPV cell geometries and cell structures. To further

increase the amount of power that can be extracted from a converter cell, heterostructures may be employed instead of simple *p-n* junctions used in this process.

Conclusions

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