

Design of a Bipolar Rail-to-Rail Operational Amplifier

by

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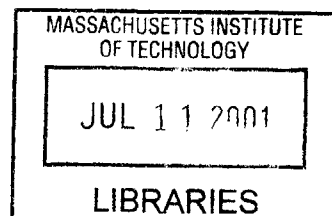
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Abstract

This thesis details the design and simulation of a low-voltage, low-power rail-to-rail input and output high speed operational amplifier. Various input and output structures from the literature are analyzed. Intermediate stage concerns, compensation, current distribution, and power supply, common-mode voltage, and temperature variations are addressed. Considerable time is spent analyzing various Class AB bias-control schemes. The final amplifier settles to 0.1% in 90ns, has an 80 V/ μ s slew rate, and a 200 MHz unity gain bandwidth, while using only 2.3mW from a 2.5 V supply.

Thesis Supervisor: James K. Roberge

Title: Professor of Electrical Engineering

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Fourth, but certainly not last, I would like to thank my parents Al and Elizabeth, for their support and guidance in getting me to MIT, because I certainly would not be here if not for them.

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Introduction

The objective of this thesis is the design and simulation of a rail-to-rail input and output, low-voltage, low-power high speed operational amplifier.

Problem Definition

The most widely used linear integrated circuit is still the operational amplifier. For over thirty years the most widely used part, the operational amplifier (op amp) can be used for literally thousands of circuit functions. Signal amplification, signal filtering, digital logic functions, rectification, multipliers, mixers, non-linear functions, and a myriad other basic building blocks can be most easily implemented using op amps. Although there are hundreds of op amps on the market, each one is tailored to a specific portion of the market, be it low-power, high power, precision, high speed, low distortion, low noise, or any other possible specification imaginable. Even with increasing levels of integration of formerly board-level components into integrated packages, discrete operational amplifier ICs are still widely used in an extremely broad variety of applications. In addition, most large integrated circuits contain one or more op amps, tailored to the specific application needed.

For the last 30 years, voltage supply trends have continuously been towards lower supplies. Years ago the standard system voltage was $\pm 15V$ – currently in systems it is as low as 1.8V, with 5V being a very popular standard. Systems using voltages as low as 2.7V are widespread. The advantages of low power supplies are several – smaller voltages allow the use of lower breakdown voltage processes, which often are considerably faster than processes with higher breakdown voltages. Lower voltage power supplies linearly lower the power consumption of a circuit which uses a constant supply current. Another advantage of lower supply voltage is that power conditioning can become less important. For instance, in a typical battery operated system, voltage regulation is important -- the voltage derating curve for NiCd cells reaches as low as 0.9V for a nominally 1.2V battery. With low-voltage capable circuits, if a circuit is designed to operate at a nominal 3.6V supply but can operate as low as 2.7V, NiCd rechargeable batteries can be used to power it directly, without an additional voltage regulator.

One of the major drawbacks for low supply voltages involves signal-to-noise ratio concerns. For digital logic, lowering the supply voltage often does not directly affect the error rate or noise concerns of the circuit in question. However, for analog circuitry, the quantity most important in many applications is the signal to noise ratio; while the signal size scales with the voltage supply, the noise in many cases remains unchanged. At a single 2.7V supply, losing two V_{BE} drops in output swing and reducing the possible output swing to approximately 1.4V, as is normal with many general-purpose operational amplifiers, reduces the possible signal-to-noise ratio by almost 6dB – an unacceptable loss in many cases. A similar argument applies to non rail-to-rail inputs – losing a V_{CE-SAT} from either rail unnecessarily lowers the input range, limiting the maximum signal-to-noise ratio. This desire to maintain maximum signal-to-noise ratio while scaling the power supplies down to save power demands rail-to-rail inputs and outputs.

In many applications, such as switched capacitor circuits, or in signal filtering applications, the bandwidth of an operational amplifier is of paramount importance. As communications systems reach higher and higher carrier frequencies, the ability to do active filtering, amplification, and other signal functions at high frequencies becomes important. Cable modem systems involve carriers at frequencies upwards of 4 MHz; cell phones have intermediate frequencies in the hundred megahertz region. High speed, high precision A/D converters need their signals buffered properly, sometimes at frequencies in the many tens of megahertz. In short, high speed parts are increasingly important, and low power and low voltage constraints are standard for many of these new applications.

For this thesis, the specifications to be achieved are based on those of a commercially available operational amplifier, Analog Devices' AD8031. The specifications in brief are:

1. Rail-to-rail input and output
2. High speed (unity gain bandwidth > 160 MHz)
3. Low supply current (< 1 mA under all conditions)
4. Low supply voltage (must operate successfully at a single 2.5 V supply)
5. Acceptable operation under capacitive loading upwards of 20pF, as well as at all reasonable resistive loads.

The AD8031 has all of the above specifications, except the bandwidth is only 80 MHz – we will achieve 160 MHz operation with this part. As we shall see, each specification on this list helps constrain the design choices made to architectures which are non-optimal for at least one of the other specifications.

Prior Work

Much work has been done in the field of low-voltage design. Until quite recently, the desired combination of low-voltage, low-power, and high speed were almost a contradiction in terms, due to the difficulty of building high-speed circuits on the processes extant. In 1978, Robert Widlar published a paper in which he was able to get 60 kHz of bandwidth from a circuit which operated at a single 1.1V supply, using only 270 μ A.[13] This was one of the first large circuits which operated at low voltages and low power and also had moderate speed. The necessity of including PNP devices in the signal path due to the low headroom, limited the bandwidth of the circuit to significantly less than 1 MHz, the f_T of the PNP devices.

In the last decades, high speed complimentary bipolar processes have become available, allowing high speed design at low voltage supplies. As in many design problems, an infinite number of solutions are possible, depending on which tradeoffs are made. The state of the art seems to be that most parts are either very low power, with low bandwidth, or are high bandwidth, with high power consumption.[2, 3, 4, 5] Examples of specifications can be found in Table 1.1. These are not intended to be a comprehensive or completely representative group of devices, just to show the variety available.

Part Number	Bandwidth	Power Consumption
AD8031	80 MHz	.8 mA
AD8042	160 MHz	12 mA
OP181 (ADI)	.095 MHz	.004 mA
LT1809	320 MHz	10 mA
LT1632	45 MHz	4.3 mA
LT1812	100MHz	3.6 mA
MAX4321	5 MHz	.725 mA
MAX4122	25 MHz	.650 mA
MAX4040	.06 MHz	.01 mA

Table 1.1: A selection of commercially available rail-to-rail operational amplifiers

As can be seen in Table 1.1, a wide variety of design choices can be made, leading to vastly different end products. The specifications chosen for this amplifier design put it in a somewhat unoccupied market niche – very high speed combined with low power.

Process Discussion

As mentioned previously, the process on which a part is made in a fundamental sense sets the specifications that it is possible to achieve. The design in the current thesis was simulated using device data from a modern complimentary bipolar process.

The process used is a Silicon On Insulator (SOI) process, in which the active devices are grown on a layer of silicon dioxide insulator. This insulation layer allows each device to have its own substrate area, with no shared substrate between devices. The process is trench isolated as well, meaning that neighboring devices are very well electrically and thermally isolated from each other.

Available components include very fast NPN and PNP devices of many sizes and geometries, all of which include buried highly doped collectors for lower collector resistance, and polysilicon emitters for low emitter resistance. Also available are Metal On Metal (MOM) capacitors, which have very good matching and effective-area to fringing-area ratios. Thin film resistors are the primary resistors, and the process includes an option for laser trimming at wafer sort. A Schottky diode is available as well.

The transistor parameters are very good. The minimum device dimension is 1.5 μm , with a minimum 2.6 μm metal layer separation. The collector-to-emitter breakdown voltage is 8V, leading to the possibility of using reasonably large voltage supplies. The f_T of the devices is quite high, with the minimum NPN device f_T reaching a peak of approximately 8 GHz at 100 μA of collector current. The minimum PNP devices reach a peak f_T of 6 GHz at quite large currents – at 100 μA the PNP devices have an f_T of 4 GHz. In this design we will see that the devices are all run at nearer to 10 μA of collector current; at this current, the NPN devices have a 4 GHz f_T , while the PNPs have 2.5 GHz f_T s. DC betas for these devices are typically

in the 100 – 140 range for the NPNs and 60 - 100 for the PNPs. The Early voltage for the NPN devices is typically as high as 90 to 110V, while the PNPs suffer from a much lower Early voltage of only around 16 V.

The parasitic capacitances in these devices are quite small, with the junction capacitances typically around 10 fF in size. Due to the lack of shared substrate, and the fact that the SiO₂ layer beneath the active devices is quite thick, the collector-to-substrate capacitance of these devices is quite low, typically less than 10 fF for a minimum-sized device. Even for quite large devices, the parasitic capacitances are surprisingly small, leading to improved high-frequency operation.

In short, the process used is ideally suited for high-speed design. Unfortunately, at the collector currents necessary for the current design, the devices are not operating at peak f_T , but quite acceptable performance is possible nonetheless.

2. Input Stage

Introduction

The input section of an opamp generally implements several of the fundamental functions of the amplifier. Generally, the input stage has the following characteristics:

1. High gain to differential inputs, and low gain (ideally no gain) to common-mode inputs.
2. The common-mode input voltage can take any value in a wide range without degradation of the small-signal or large signal characteristics of the amplifier.
3. Generally, the overall differential to single-ended conversion is achieved in the input stage if the following stages are single ended.
4. The input-referred offset voltage of the entire amplifier is generally dominated by the offset voltage of the input stage, so this offset should be as small as possible.

Each facet of input stage performance leads to architectural, device sizing, power, complexity, or other tradeoffs. Specific to rail-to-rail amplifiers is the additional constraint that the input common-mode range must include both of the supply rails. The common-mode voltage requirement of rail-to-rail op amps has a major impact on the input stage architecture, as we shall see.

Architecture Discussion

As is typically done, we will decompose the input voltages at the inverting and non-inverting inputs into the common-mode and differential-mode voltages. These voltages are defined (using the voltage definitions of Figure 2.1) as: $V_{\text{differential}} = (V_1 - V_2) / 2$ and $V_{\text{common}} = (V_1 + V_2) / 2$. When discussing the differential and common-mode portions of signals, this decomposition of the signal is assumed.

A commonly used input stage for an op amp is shown in Figure 2.1. This stage provides high differential gain of approximately $\sim g_{m1} \cdot (r_{o4} \parallel r_{o2})$, where g_{m1} is the transconductance of transistor Q1, and r_{o4} and r_{o2} are the output resistances of transistors Q4 and Q2 respectively. The output resistance of the NPN Q2 will hereafter be neglected due to its nearly order of magnitude larger Early voltage. The transconductance for a bipolar transistor is:

$$g_m = q \cdot I_C / k \cdot T \quad [2.1]$$

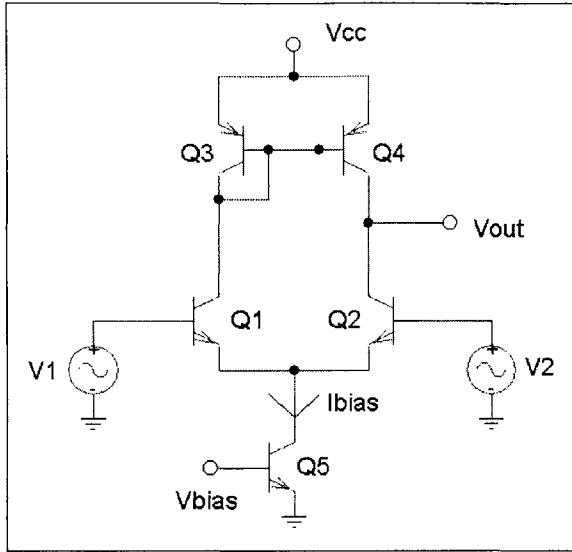


Figure 2.1: Actively Loaded Differential Pair

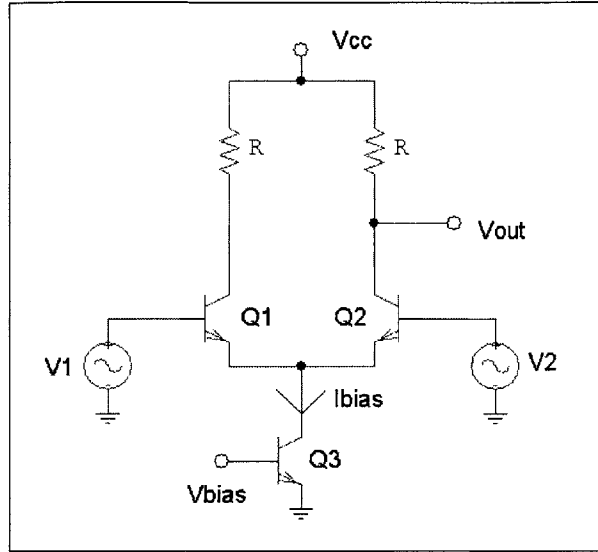


Figure 2.2: Resistively Loaded Differential Pair

where q is the charge on an electron, I_C is the collector current of the device in question, k is Boltzmann's constant, and T is the device temperature in Kelvin. The output resistance for a bipolar transistor is

$$r_o = V_A / I_C \quad [2.2]$$

where I_C is the collector current of the transistor, and V_A is the Early voltage of the device. The circuit of Figure 2.1 has low common-mode gain, and achieves differential to single-ended conversion as well. Its output impedance is high, and the DC value of the output voltage can be nearly any value between V_{CC} and the common-mode value of the input voltage. Typically the DC value of V_{out} is kept approximately a V_{BE} from V_{CC} supply to prevent Q2 from saturating later than Q1 and to avoid the systematic offset due to differing V_{CE} voltages on Q3 and Q4. Nonetheless, the fact that the output voltage can vary easily is still an important advantage of this circuit.

For this discussion and the rest of the thesis, a good definition of the saturation voltage of the bipolar transistor will be needed. The saturation voltage for a BJT is defined as:

$$V_{CE-SAT} = \frac{kT}{q} \ln\left(\frac{1}{\alpha_R}\right) \quad [9] \quad [2.3]$$

where α_R is the reverse common-base current gain. The important parts of this relationship

are that V_{CE-SAT} is proportional to absolute temperature, and that it is inversely proportional to α_R . For a given process, α_R will be fixed; in the process used the quantity $\ln(1/\alpha_R)$ is approximately 2. Equation 2.3 describes the V_{CE-SAT} of an ideal transistor with no ohmic drops – in practice the effective V_{CE-SAT} goes up with I_C :

$$V_{CE-SAT} = \frac{kT}{q} \ln\left(\frac{1}{\alpha_R}\right) + I_C \cdot r_{c-ohmic} \quad [2.4]$$

where $r_{c-ohmic}$ is the combined ohmic drops in the collector-emitter circuit of the device. At room temperature and low enough currents that ohmic drops do not affect the saturation voltage, V_{CE-SAT} is only around 60 mV. At high temperatures this ideal V_{CE-SAT} rises to around 80 mV. We can thus define a value of V_{CE-SAT} which will leave margin for error and for collector current variations at all temperatures. Since most of the devices used in this amplifier are minimum sized but run a significant current, V_{CE-SAT} will be chosen to be 250 mV to allow for ohmic drops.

Despite the fact that circuit of Figure 2.1 has good differential gain, the circuit's common-mode range is insufficient for a rail-to-rail design. As V_{common} approaches the V_{CC} rail, Q1 begins to saturate as its emitter voltage approaches its collector voltage, which is fixed a V_{BE} below V_{CC} . This saturation of Q1 means that this stage cannot be used with V_{common} greater than about $V_{CC} - V_{CE-SAT}$ (assuming $V_{BE-NPN} = V_{BE-PNP}$). When the common-mode voltage is near the ground rail, the collector to emitter voltage across Q5 lowers, until eventually that current source saturates. The saturation of Q5 leads to a dramatic reduction in its output resistance, which causes severe signal degradation and lowered common-mode rejection. These negative effects occur when V_{common} is less than $V_{BE1} + V_{CE-SAT5}$. Thus, the common-mode range of this type of input stage is from $V_{BE1} + V_{CE-SAT5}$ on the lower end to $V_{CC} - V_{CE-SAT}$ on the high end.

A differential pair will operate properly with any common mode voltage so long as the input transistors Q1 and Q2 (in Figure 2.1) are in the forward active region, and the tail current source Q5 is not saturated. A standard resistor-loaded NPN input stage with NPN current source as seen in Figure 2.2 has a common-mode range that can include the top rail. Suppose that the input common-mode voltage is exactly V_{CC} . The input transistors have $V_{BC} =$

output currents using a current mirror stage, we can get full rail-to-rail performance. At each end of the common mode range, only one stage is functioning properly, but over most of the range both stages can be functional. If simply hooked up, the change from one functional stage to two doubles the effective g_m of the stage, which effectively doubles the gain of the opamp. This drastic change in gain leads to substantially suboptimal frequency response, and to poor large signal response.

As discussed previously, in a bipolar transistor the transconductance g_m is proportional to I_C . Thus even in the range where both stages are operational if we are able to keep the sum of the collector currents of the two input stages constant, the composite g_m will be constant. The standard way of achieving this constant collector current is shown in Figure 2.4. As V_{common} approaches $V_{CC} - V_X$, the tail current I from the PNP stage is steered through a mirror to the NPN stage, allowing normal operation as V_{common} approaches and exceeds V_{CC} . The PNP stage is used across most of the voltage range despite its weaker frequency response and lower beta so that the switchover happens as rarely as possible. Since rail-to-rail amplifiers are very often used as followers in single supply systems, and in such applications often have signals with common-mode voltages close to ground, the PNP stage should be active as much as possible. When the switchover occurs several undesirable changes occur, including changes in the magnitude and direction of input bias currents, and a change in the offset voltage.

The last first-order change in g_m that occurs is due to change in temperature. The transconductance $g_m = I_C \cdot q / k \cdot T$ (equation 2.1), and so with constant I_C is inversely proportional to temperature. The solution to this problem is to supply I_C using a so-called PTAT current source, whose current is directly proportional to temperature. This choice for I_C leaves g_m independent temperature, and the architecture already leaves g_m independent of common-mode and supply voltage to first order. For this design an ideal PTAT source was used to bias the entire circuit.

Offset Voltage Concerns

The offset voltage of an operational amplifier is defined as the open-loop input voltage necessary to bring the output voltage of the amplifier to zero volts DC. This offset is usually conceptually divided into the systematic offset and the random offset. Systematic offset arises due to asymmetries in the circuit, whether due to intentional design choices, or due to unavoidable voltage differences. Random offset is offset due strictly to random component variations in an actual circuit. In a properly designed operational amplifier, the offset voltage (both systematic and random) is nearly always dominated by the offset of the input stage. Any offset in stages after the first stage can be compensated for by a very small input voltage due to the large voltage gain of the input stage; the input stage offset is simply reflected to the input.

The systematic offset in the amplifier of Figure 2.4 is primarily due to slight differences in current in the mirror, due to differing V_{CE} voltages on Q5 and Q6. As the supply voltage rises, the mismatch in V_{CE} voltages rises causing a larger current mismatch, causing the offset voltage to rise at larger supplies. To fix this, the mirror in the final circuit is cascoded on both top and bottom, reducing the current mismatch by several orders of magnitude.

The matching between the differential pair transistors and between the load resistors is crucial to circuit operation, but this matching can be improved by making the devices larger and by using common centroid layout. If the absolute mismatch in device dimensions remains constant as the device dimensions grow, the percent mismatch between devices shrinks as the devices grow. Making the load resistors quite physically large in size allows for good matching. The input devices can be made larger as well, but this increases input capacitance and reduces circuit performance as with constant bias current the current density in the devices shrinks as the devices get larger. Since noise performance and f_T are functions of current density and both degrade at lower current densities, making the input devices very large is not a good option. However, common centroid layout can help considerably. By laying out the devices in such a way that any parameter gradient across the wafer equalizes out across the pair of devices, mismatches can be significantly lowered.

3. Output Stage

Introduction

The output stage of a general-purpose operational amplifier has several purposes: to produce an output voltage with as low output resistance as possible, drive large currents, and isolate the previous stages from load characteristics. In the current application a rail-to-rail output voltage and low quiescent power consumption are also called for. As we will see, the rail-to-rail output voltage constraint forces a specific architecture on the design, and the low-power constraint significantly complicates things as well. In addition, for good high frequency behavior neither of the output transistors should ever turn off or saturate, due to the relative slowness of bringing devices from saturation or cutoff back to active functioning. For some architectures it is simple to insure that neither output device leaves the forward active region – as we will see, for the architecture needed to get rail-to-rail output voltages, it is not so simple.

Architectural Discussion

One possible output stage is shown in Figure 3.1 – a simple current-source loaded emitter follower. If the input voltage is limited to swing such that the transistor goes from cutoff to saturation, this output stage can achieve output voltages ranging from V_{CE-SAT} (if the current source is implemented using a transistor) to $V_{CC} - V_{BE}$. This range can be acceptable for many applications, but for a rail-to-rail output, we need to be able to both rails. This stage can source as much current through the NPN output device as required for a given load, but cannot sink more than I current. Lastly, the maximum current the stage can sink is the quiescent current in the stage. If the stage must sink considerable current, the quiescent power consumption will be quite large.

Another possible output stage is the current-source loaded common emitter shown in Figure 3.2. This stage does not immediately seem to be a good choice for an output stage for several reasons. Its output resistance can be quite large, and in fact is on the order of $r_O = V_A / I_C$ for the transistor – often many kilohms. The stage also has gain, which is desirable in the

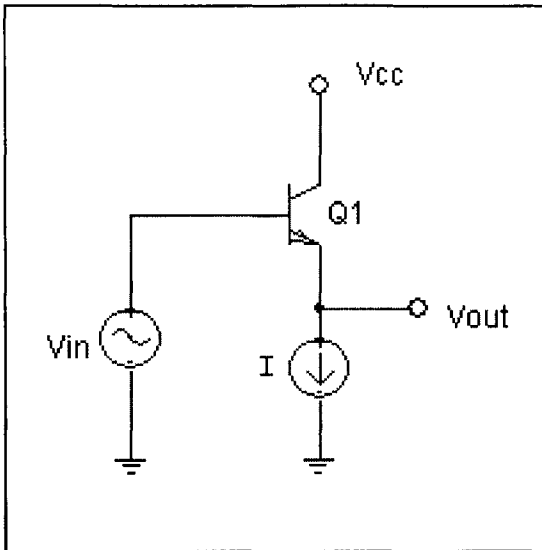


Figure 3.1: Current-source loaded emitter follower

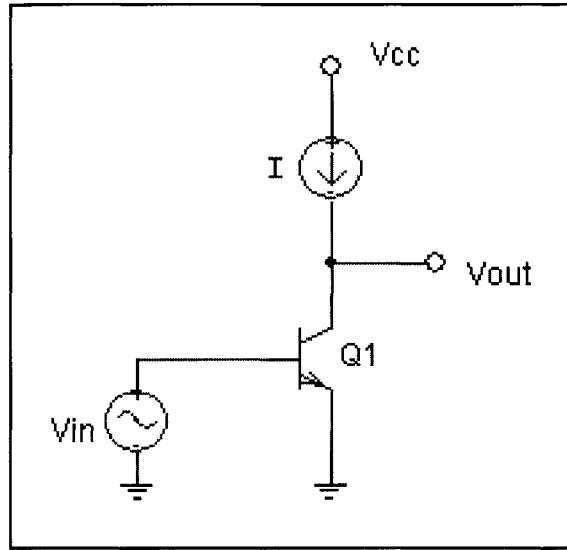
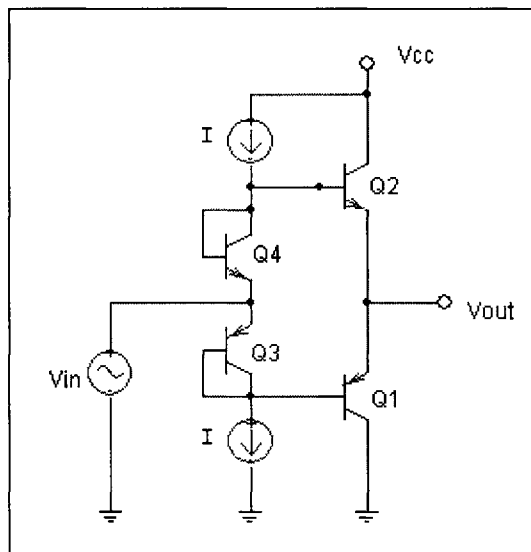


Figure 3.2: Current-source loaded common emitter

amplifier in general, but in an output stage can cause severe bandwidth limitation due to the large size of the output transistor, and thus the large C_{μ} affected by the Miller effect. However, this stage has output voltage swing to recommend it – if the input voltage is again allowed to range such that the device goes from cutoff to saturation, and the current source is implemented with a transistor, the output voltage can go within a V_{CE-SAT} from either rail. At low currents, V_{CE-SAT} can be as low as 100mV, allowing the best rail-to-rail operation possible with bipolar transistors. Again, however, the stage is limited in output current and has poor quiescent power dissipation qualities. The maximum current the stage can source is I , and this is the quiescent current through the stage, meaning that if the stage is to be able to source

Figure 3.3: Complimentary Emitter Follower



considerable current, its quiescent power consumption must be large.

An extremely popular output stage is shown in Figure 3.3. The complementary emitter follower, as this stage is sometimes known, is essentially an NPN emitter follower and a PNP emitter follower operating in parallel. It can be easily seen from the discussion of the simple emitter follower that this stage can both source and sink large currents, with the NPN device sourcing current up to $\beta_{\text{NPN}} \cdot I$ and the PNP device sinking currents up to $\beta_{\text{PNP}} \cdot I$. The same comparison of the circuit of Figure 3.3 with that of Figure 3.1 can lead one to see that the output voltage characteristics of this stage are not rail-to-rail – the output cannot go closer than a V_{BE} from either rail. However, the power consumption of this stage is extremely good – the quiescent current in the output device leg has no relationship with the maximum output current. This lack of coupling between maximum current and quiescent current allows the stage and overall amplifier to draw little quiescent current, and yet still sink and source tens of milliamps when necessary. A last positive feature of this stage is that the output voltage in this stage is controlled by the input voltage directly. It is easy to see that in a DC sense V_{in} and V_{out} must be at approximately the same potential – to go from V_{in} to V_{out} you go down a V_{BE} and back up a V_{BE} , for a net DC difference of approximately zero volts. Thus since the full amplifier will always have overall feedback around it, the output voltage is always well controlled.

Some of the favorable drive characteristics of the common emitter output and of the complimentary emitter follower can be combined in a single stage, shown in Figure 3.4. This output consists of a PNP common emitter connected to an NPN common emitter. If the two transistors are driven by two in-phase voltage sources (V_{common}) that can range such that the devices go from cutoff to saturation, the output voltage can reach within a $V_{\text{CE-SAT}}$ of either rail. Thus, this stage can give the necessary rail-to-rail voltage. In addition, with proper input voltages the stage can source large currents through the PNP device, and sink large currents through the NPN device. As in the complementary emitter follower, the maximum current the stage can source is unrelated to the quiescent current in the output device leg, allowing low quiescent power consumption.

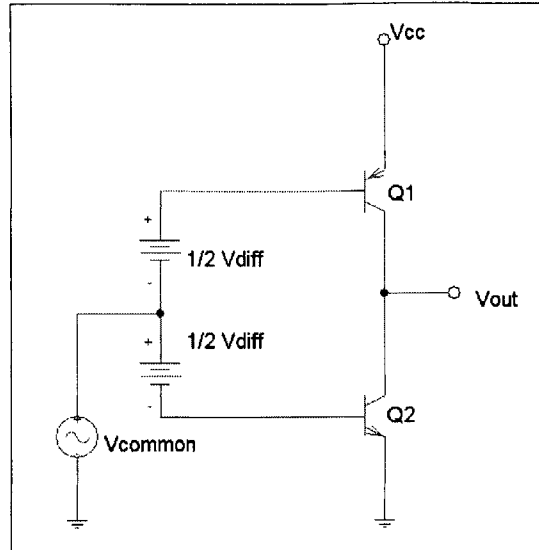


Figure 3.4: Complimentary Common Emitter

However, these benefits are only obtained at the cost of significant complexity. Whereas in the complimentary emitter follower case a single input could be connected to both output devices, in this stage two inputs are needed. In addition, while the output current when loaded is controlled by V_{common} , the in-phase (common-mode) portion of the inputs, the quiescent current must be controlled by a differential signal. Note that V_{common} and V_{diff} are voltages with both DC and AC components – they are indicated differently in Figure 3.4 simply for clarity. The common-mode portion of the two inputs controls the output current – as the two inputs rise, the NPN device sinks more current and the PNP device sources less, causing the output current (and voltage) to go more negative. If common-mode control is the only control applied to the two devices, however, the quiescent current through the two devices is not well controlled. The external feedback around the amplifier may cause the output voltage to be zero, but the actual values of I_{C1} and I_{C2} will be extremely sensitive to the DC voltages applied at the two inputs, V_{diff} . In addition, the values of I_{C1} and I_{C2} are also very temperature and supply voltage sensitive – a constant DC voltage applied at the two input sources will not hold the quiescent current constant. The differential voltage between the two input signals also controls the current in the two output devices, but in such a way that if the V_{diff} voltage rises, both I_{C1} and I_{C2} lower. Thus to completely control the currents in the output devices, there needs to be both a feedback loop around the entire amplifier and an internal feedback loop controlling the quiescent current. This aspect of an output stage is

known as class AB biasing, and will be discussed at length in the next chapter.

Another significant drawback is that the complimentary common emitter stage has a significantly higher output resistance than the emitter follower stages. This output resistance will be effectively reduced by the external negative feedback applied around the amplifier, but will still be large – in most rail-to-rail amplifiers the output resistance is on the order of a kilohms. A large open-loop output resistance is to be avoided because it makes the open-loop gain and other characteristics of the amplifier very load dependant. Ideally, the op amp would have the same open-loop gain (loop gain) when driving a 10Ω load as a $100k\Omega$ load. In practice, for these type of output stages the gain can vary by up to 40dB across expected load conditions. The change in open-loop gain is simply part of the price one has to pay for rail-to-rail performance.

Lastly, this stage has inherent voltage gain, which as mentioned earlier and discussed further in a later section can make compensation much more complicated.

Through this discussion we have seen that the output stage must be a complimentary common emitter stage in order to reach both rails. Many variations on the emitter follower output stage exist with various good properties, but none can achieve the rail-to-rail output voltage the common emitter stage can.

4. Class AB Feedback

Introduction

As seen in the previous section, the preferred architecture for the output stage of a rail-to-rail amplifier is the complimentary common emitter. The requirements for this stage to operate properly are several: first, it needs two in-phase input voltages, one at a V_{BE} from the top rail, and one a V_{BE} from the bottom rail. Second, the quiescent output voltage and current are set by the differential signal applied between the inputs, and this differential signal is not controlled by the external feedback around the amplifier. This quiescent bias situation provides the toughest challenge in the design of this type of output stage.

An additional problem which must be solved is keeping the high-frequency behavior of the circuit well controlled. If either or both of the output transistors ever turns off or saturates, the output becomes severely distorted. The time required to drive a transistor from cutoff or saturation to normal operation is quite long in comparison with the timescale of the hundred megahertz signals this output stage is required to handle. In the saturation region excess charge builds up in the base region in proportion to the saturation base current. In many low-voltage designs, this charge must be removed by a static current source which is of relatively low value, and thus can take tens of nanoseconds to bring the device back to the forward active region. During the time the saturation charge is being removed, the output current does not change at all. When a transistor goes towards cutoff, the opposite situation is true – charge must be added to the base region to return the device to forward operation. As seen in Figures 4.1 – 4.8, in most low-voltage applications, the output devices are driven by a current source with a typically quite small current. If the charge in the output device's base is significantly below that required for forward active operation, it will take some time for that charge to be replaced by the small-valued current source that must refill the base. During the time to refill the base, the collector current rapidly grows, but it may still take some time to reach the correct current; during that time, the output is distorted. Typically this time to bring a transistor from cutoff to forward active operation is significantly less than from saturation to forward active operation, but neither type of delay is acceptable for 100 MHz operation.

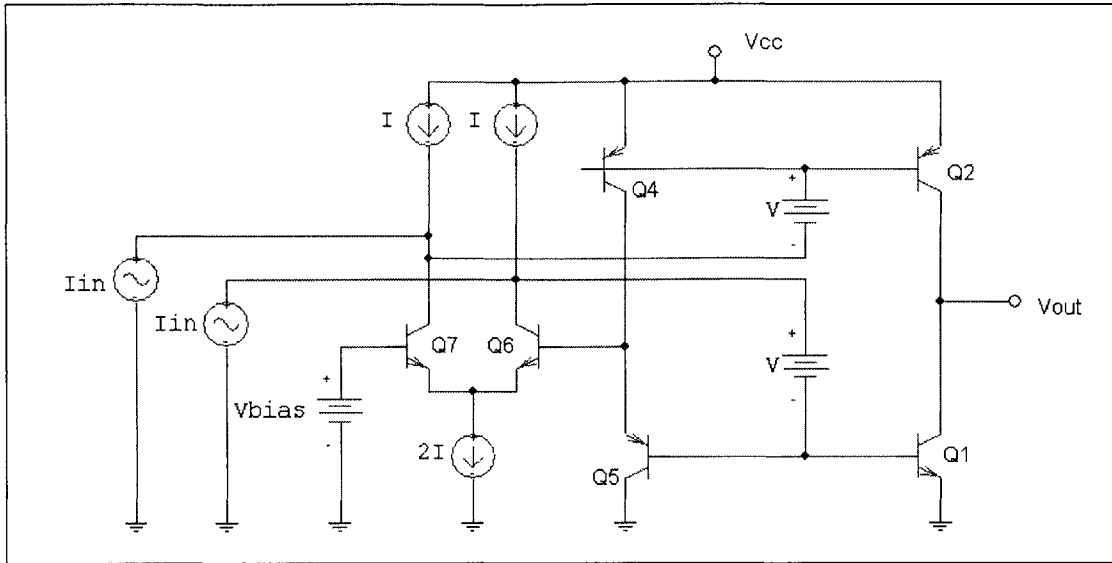
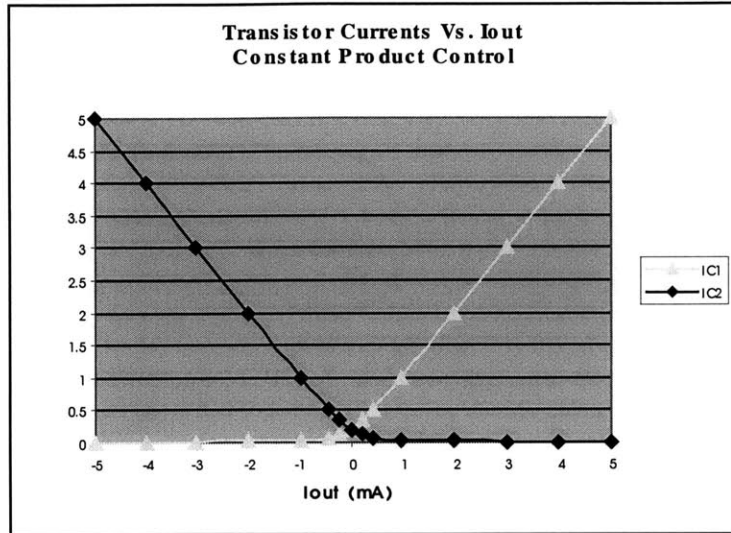


Figure 4.1: Constant Product Class AB feedback loop

All of the previously mentioned problems are typically solved using feedback, usually in the form of Class AB biasing, which keeps both transistors on at all times. Class A is a term for biasing like that of Figures 3.1 and 3.2, where the quiescent current is the maximum possible sinking (or sourcing) current. This type of biasing is by far the simplest type, with no extra circuitry involved, and few extra problems. However, Class A control is out of the question for our current design, as its power dissipation is far too great. Class B is a form of biasing in which both transistors are normally off, leading to very good power characteristics, as there is no quiescent current at all. The input signal can turn the output devices on alternately, depending on whether the output voltage needs to rise or fall. However, this type of biasing suffers from bad high-frequency behavior, due to the output transistors alternately turning off. This type of output stage typically has a “dead-zone” in its open-loop response, due to both devices being off quiescently, and also suffers from the slow turn-on of completely off devices.

Class AB is a form of biasing which has the benefits of Class A and Class B, with few of their drawbacks. The increased usefulness of Class AB biasing has a cost, of course – complexity. While Class A and Class B were simple open-loop biasing schemes, with the output voltage set by the external feedback around the amplifier, Class AB biasing requires control loops

Figure 4.2: I_C vs. I_{out} characteristics of constant product Class AB feedback loop



internal to the amplifier. These internal control loops must be stable, and must operate over the entire useful frequency range of the circuit, under all load conditions. Since the specification for this amplifier is operation at several hundred megahertz with a moderate capacitive load, the internal control loop must be extremely fast, and very stable. This speed and stability requirement is a hallmark of translinear loops – loops of V_{BE} 's. Translinear loops are inherently very stable, and operate up to nearly the f_T of the devices. There is considerable literature about translinear Class AB loops, but for our purposes, they can be sorted into three classes.

Class AB Control Loop Types

The first type of translinear Class AB control constrains the output currents of the two power devices to have a constant product. These types of circuits are also called geometric mean circuits, as they keep the geometric mean of the two output collector currents constant. The geometric mean of two numbers is $(x_i \cdot x_j)^{1/2}$. For example, the circuit in Figure 4.1 will force $I_{C1} * I_{C2}$ to be constant. [10] Please note that the ideal DC voltage sources in the circuit of Figure 4.1 and other circuits this chapter are conceptual aids – in order to simplify the schematics, non-essential devices have been removed. The DC voltage sources are necessary to make the circuit functional in a DC sense without the removed devices. The collector current of Q2 is sensed using transistor Q4. Usually, Q1 and Q2 are large output transistors and are ratioed many times larger than Q4 and Q5; however, for simplicity, we will assume a

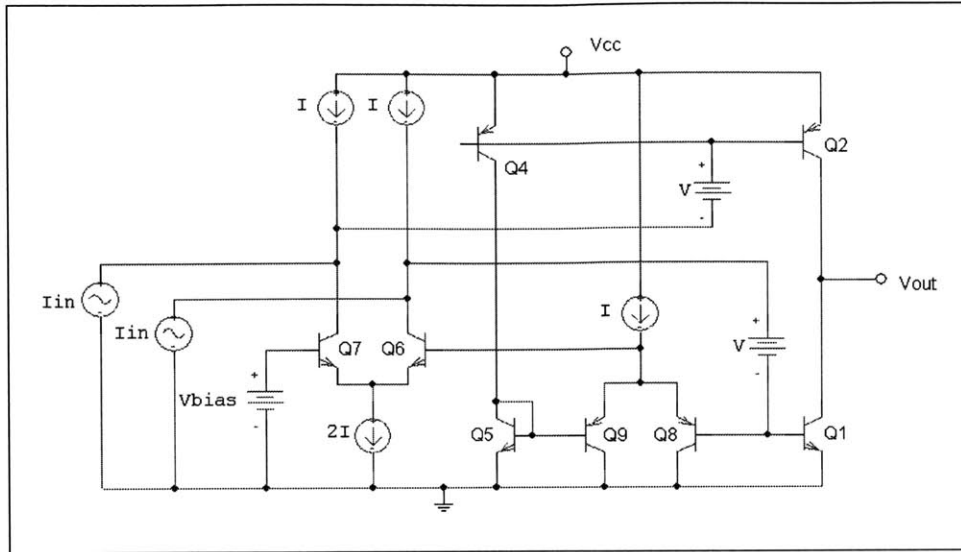
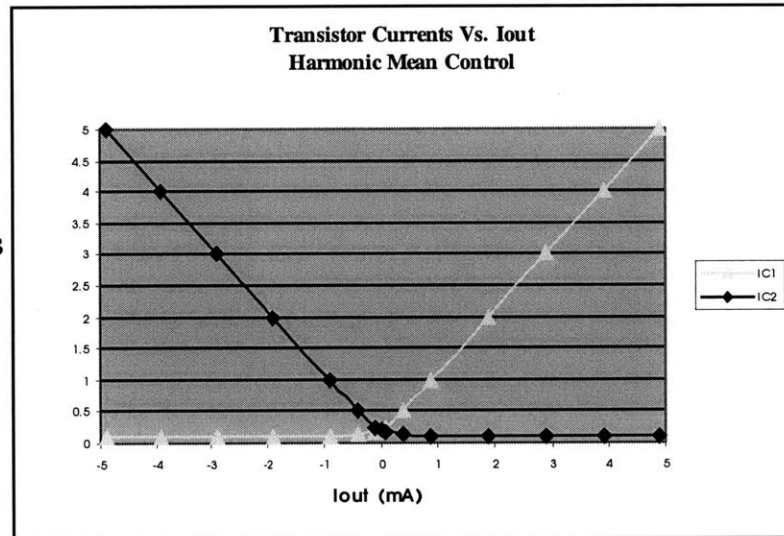


Figure 4.3: Harmonic Mean Class AB Feedback Loop

Figure 4.4: I_C vs. I_{out} characteristics of a harmonic mean Class AB feedback loop



ratio of unity. Since $I_{C5} = I_{C4} = I_{C2}$, and all devices are PNP, it is easily seen that $V_{BE5} = V_{BE2}$. The action of differential pair Q7 and Q6 is such as to keep its inputs equal, thus forcing $V_{BE5} + V_{BE1} = V_{BE2} + V_{BE1}$ to be equal to the constant V_{bias} . For instance, if the current through Q1 or Q2 is too low, $V_{BE2} + V_{BE1}$ will be lower than V_{bias} . The base node of Q6 will thus be lower than the base node of Q7, causing the collector of Q6 to rise, and the collector of Q7 to lower, increasing the collector currents of both Q1 and Q2, and bringing the circuit back to its equilibrium point.

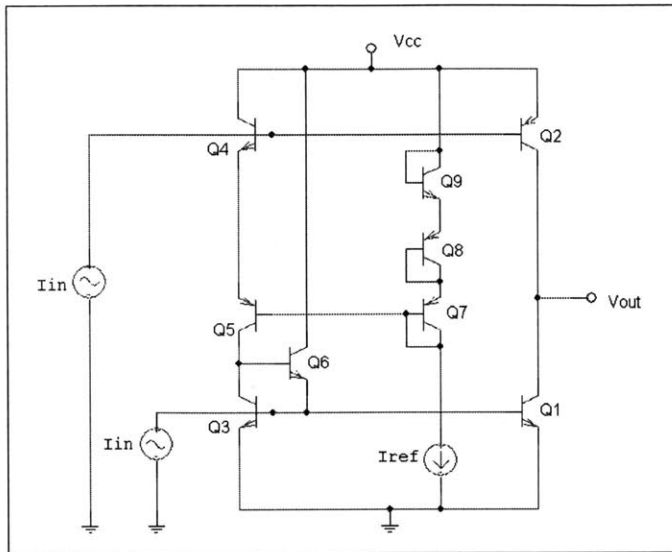


Figure 4.5: Hybrid Class AB Feedback Loop

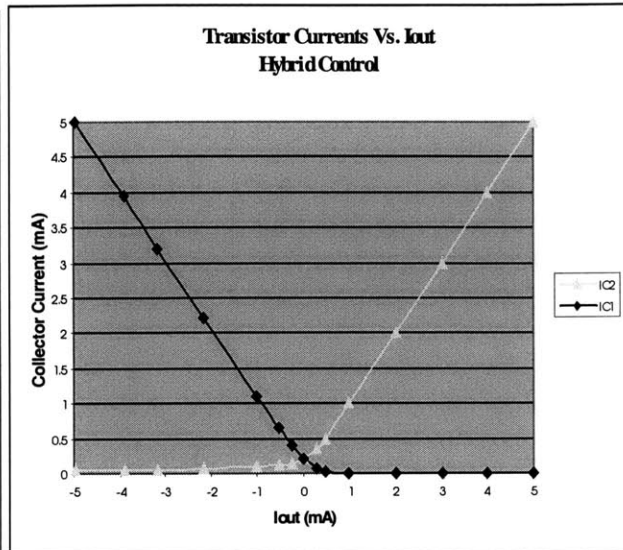


Figure 4.6: IC characteristics of Hybrid AB Feedback Loop

When this constraint of constant $V_{BE2} + V_{BE1}$ is converted into current constraints using the fact that for a bipolar transistor

$$I_C \approx I_S \exp(V_{BE} / V_{th}) \quad [4.1]$$

or:

$$V_{BE} = V_{th} \ln(I_C / I_S) \quad [4.2]$$

where $V_{th} = k \cdot T / q$, one quickly finds that for a constant $V_{BE2} + V_{BE1} = V_{bias}$,

$$V_{bias} = V_{th} \cdot \ln(I_{C1} \cdot I_{C2} / I_{S1} \cdot I_{S2}) \quad [4.3]$$

If V_{bias} is created by a constant current through a PNP diode-connected transistor and an NPN diode-connected device, equation 4.3 reduces to

$$I_{C1} * I_{C2} = \text{Constant} \quad 4.4$$

This constant product means that no matter how large either output current is, the other transistor will carry some current. However, in our current application an extremely large dynamic range is required – we would like the quiescent current through the power devices to be on the order of 200 uA, and the stage needs to be able to easily source 15mA. With constant product feedback, if the stage is sinking 15mA, Q2's collector current is down to only about 2.7uA. Since Q2 is a large power transistor, this low collector current will effectively cut it off. In addition, ohmic drops due to the base resistance, r_b , in the base-emitter circuit of Q1 will raise V_{BE1} , further reducing the current through Q2. A graph showing the ideal possible values of I_{C1} and I_{C2} is shown in Figure 4.2 – as can be seen, at the

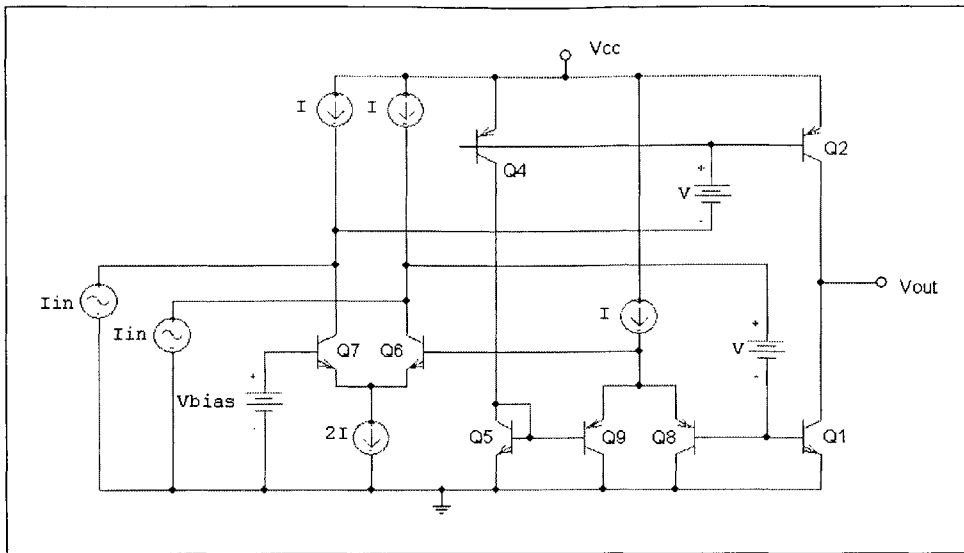


Figure 4.7 (identical to Figure 4.3): Harmonic Mean Class AB Feedback Loop

extremes of current, which are only 1/3 of that required for our purposes, the “off” transistor is actually quite close to off. As mentioned previously, if either output transistor runs at a very low current, it is very slow to respond when it needs to sink/source current. Clearly this topology cannot serve our purposes.

The second type of translinear loop is called a harmonic mean circuit. In this circuit, the harmonic mean of the two output device collector currents is constrained to be constant. The harmonic mean of two numbers is $x_i * x_j / (x_i + x_j)$. The circuit shown in Figure 4.3 causes the collector currents of Q1 and Q2 to have a constant harmonic mean: $I_{C1} * I_{C2} / (I_{C1} + I_{C2}) = \text{constant}$. [4, 10] This control law can be seen using an argument similar to the argument used in the constant product case. As in the previous case, $V_{BE5} = V_{BE2}$. This gives us one equation:

$$V_{BE5} + V_{BE9} = V_{BE8} + V_{BE1} \quad [4.5]$$

Together with Equation 4.2, we can rewrite Equation 4.5 as:

$$V_{th} \cdot \ln(I_{C2}/I_S) + V_{th} \cdot \ln(I_{C9}/I_S) = V_{th} \cdot \ln(I_{C8}/I_S) + V_{th} \cdot \ln(I_{C1}/I_S) \quad [4.6]$$

Since we know that $I_{C8} + I_{C9} = I$, with some algebra involving canceling the V_{th} and I_S terms we can rewrite Equation 4.6 as:

$$I_{C2} \cdot (I - I_{C8}) = I_{C8} \cdot I_{C1} \quad [4.7]$$

The fact that the differential pair Q6 and Q7 works to keep the input voltages to it equal gives

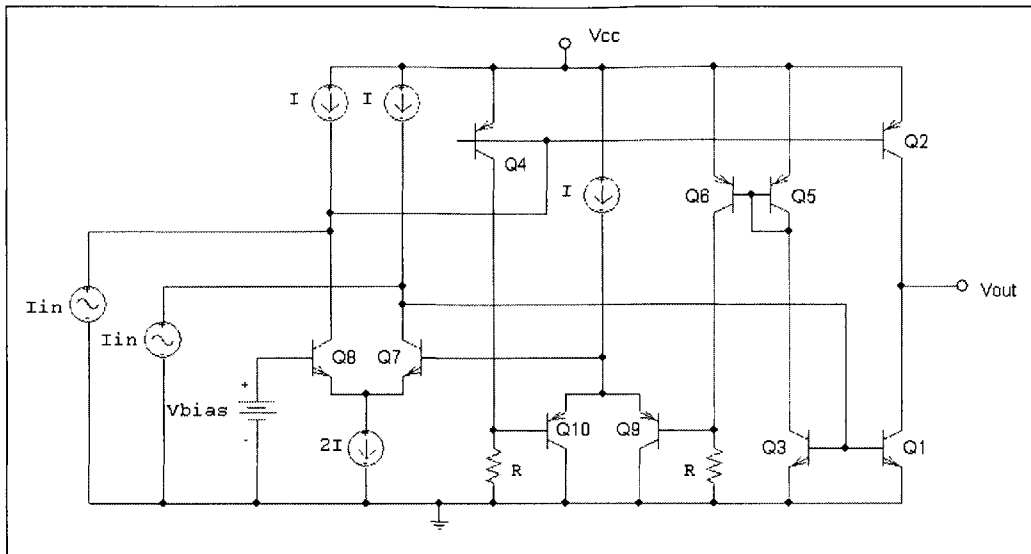


Figure 4.8: Harmonic Mean Class AB Feedback Loop With Resistor Loading

us a second equation:

$$V_{BE1} + V_{BE8} = V_{bias} \quad [4.8]$$

We can rewrite Equation 4.8 using Equation 4.2 and some algebra as:

$$I_{C1} \cdot I_{C8} = I_S \cdot \exp(V_{bias} / V_{th}) \quad [4.9]$$

Combining Equations 4.7 and 4.9 quickly gives:

$$I_{C1} \cdot I_{C2} / (I_{C1} + I_{C2}) = (I_S^2 / I) \cdot \exp(V_{bias} / V_{th}) = \text{Constant} \quad [4.10]$$

If V_{bias} is implemented using a series connected resistor of value $2R$ and a diode-connected PNP device, the exponential dependence of the above constant drops out and becomes a linear dependence upon the current through those devices.

This law is more forgiving of large output currents than the constant product law is. Using the same conditions as the first example, if the quiescent current is $200\mu\text{A}$ and the stage is sourcing 15mA , Q_2 has $I_{C2} = 100.7\mu\text{A}$, which is over 30 times what the constant product scheme would give. As shown in Figure 4.4, this circuit constrains the currents to a different path than the constant product scheme did, and no matter how large the output current is, the opposing transistor has over $100\mu\text{A}$ in it. In fact, it can be shown quite easily by rearranging the control law equation that the minimum current through the “off” device will always be half the quiescent current. This control law allows sourcing and sinking large currents, while

precisely controlling the “off” device current, preserving the amplifier’s stability and speed. There is a small cost – several extra devices, as well as the small current I through devices Q8 and Q9.

The third category of translinear Class AB loops are ones with various combinations or extensions of the first two. These types of loops are used much less often than the geometric or harmonic mean circuits, but can be useful for specific applications. One reason that alternate versions are less often used is that they often result in either asymmetric current driving capabilities, or have problems that are not immediately evident upon inspection of the circuit. The circuit shown in Figure 4.5 could be used in an application such as a single-supply system driving a resistive load, where little current sinking is required.[10] Thus, device Q2 would be a large power transistor, and Q1 would be a smaller device used for low-power sinking of current. The loop in this circuit is the loop of devices Q2, Q4, Q5 and Q7-9. Transistors Q4 and Q5 both have the same I_C as Q1, and Q7-9 all carry I_{ref} . Simple translinear loop equations similar to those in the previous sections indicate that the control law for this circuit causes $I_{C2}^2 \cdot I_{C1}$ to be constant. As shown in Figure 4.6, this keeps the minimum current in Q2 at a higher level than the current in Q1 for the same output sinking or sourcing level.

Since the application for the amplifier described in this thesis is more general, and requires sinking and sourcing at equally high levels, a harmonic mean circuit is the best choice.

Figure 4.7 shows a feedback-type circuit identical to that shown in Figure 4.3. This circuit can operate at low supplies, but not as low as we would like. The fact that the base of Q6 is two V_{BE} ’s above ground proves a problem in our design. Since this design needs to function properly at a 2.7 volt V_{CC} supply, we must be very careful about voltage drops. In the process used, V_{BE} can reach nearly 1 V at -40 degrees C; thus two stacked V_{BE} ’s means that the base of Q6 will be quite close to V_{CC} at low supplies. This high value for the base voltage of Q6 proves to be a huge problem in the final design. To avoid this bias issue, we wish that the bases of Q8 and Q9 were less than a V_{BE} from ground. A second issue with this circuit is that the two feedback loops of transistors Q6,1, and 8 and Q6, 7, 2, 4, 5, and 9 must be active until

very high frequencies for the amplifier to have good high frequency behavior. In the final amplifier, a large capacitor is added to each of the input nodes to frequency compensate the overall amplifier. The Class AB feedback loops have the same Miller capacitors in their loops, causing a very low frequency pole. If the gain around the feedback loop is significantly less than the open-loop gain of the amplifier, the feedback loop will crossover before the main loop. The Class AB feedback loop is only effective in controlling the output currents at frequencies when its loop gain is greater than one. If the Class AB feedback loop crosses over before the main loop, at high frequencies where the amplifier is still active the output device currents will not be well controlled, leading to poor behavior. Since the incremental impedance of Q5 is approximately $1 / g_m$, and the rest of the feedback loop can be modeled as a large transconductance, G_m , the low incremental impedance of Q5 leads to a very low loop gain, and to bad high frequency behavior due to the early loop crossover.

A modified version of Figure 4.7 is shown in Figure 4.8. This version solves several problems in the Figure 4.7 circuit, while keeping the same basic functionality. The diode-connected Q5 is replaced by a resistor, and the sensing of Q1's current is done in a similar way as the sensing of Q2. This circuit is not a pure translinear loop, as the circuit of Figure 4.3 was. Due to the resistors, equation 4.6 is modified to:

$$I_{C2} \cdot R + V_{th} \cdot \ln(I_{C10}/I_S) = I_{C1} \cdot R + V_{th} \cdot \ln(I_{C9}/I_S) \quad [4.11]$$

This transcendental equation cannot be simply solved to give a purely algebraic control law, as Equation 4.6 could be. However, if either I_{C1} or I_{C2} is even 25% greater than the other current, as will be the case much of the time, this difference in currents across resistors R will cause a differential voltage across Q9 and Q10 of 25% of the quiescent voltage drop across R. The quiescent voltage drop across R will be at least 300mV, so the differential voltage created by a 25% collector current difference will be at least 75mV – enough for differential pair Q9 and Q10 to be entirely tipped to one side or the other. If the differential pair is entirely tipped, the voltage at the base of Q7 will be set entirely by the lower of the two resistor voltages, as the higher resistor voltage will be connected to a cut off transistor. If differential pair Q7 and Q8 hold their base voltages equal, and the collector currents differ by enough to fully tip Q9 and Q10, this means that:

$$I_{C2} \text{ (or } I_{C1}) \cdot R + V_{th} \cdot \ln(I/I_S) = \text{Constant} \quad [4.12]$$

This circuit implements a harmonic mean control law, using two separate V_{BE} loops. The twin loops of Q1, 3, 5, and 7 and Q2, 4, 6, and 8 each control the current in one output transistor. When either output is driven hard, the current through the opposing output device is held to a minimum value of 1/2 of the quiescent collector current, as in Figure 4.4. This functionality is easy to see using an example. If the circuit is sinking considerable current, both input current sources are pushing current into the stage. The current from the top current source, going to the PNP output device, cannot go into the PNP device, so it goes to the NPN device through the common-base device Q4. The translinear loop for the PNP device is transistors Q2, 4, 6, and 8. The loop gives the constraint that:

$$V_{th} \cdot \ln(I_{C2}/I_S) + V_{th} \cdot \ln(I_{C4}/I_S) = V_{th} \cdot \ln(I_{C6}/I_S) + V_{th} \cdot \ln(I_{C8}/I_S) \quad [4.13]$$

We can quickly identify that $I_{C6} = I_{C8} = I$, and that Q4 carries $2 \cdot I + I_{in}$. We will choose I such that $2 \cdot I$ is always larger than I_{in} , so that we can approximate I_{C4} under this situation as $2 \cdot I$. Using these identities we quickly get:

$$I_{C2} = \text{Constant} \quad [4.14]$$

The same argument can easily show that this relation is true for I_{C1} under the opposite situation. Under large output current conditions, this circuit functions approximately as a harmonic mean circuit, keeping the “off” device current at a minimum level. As in the circuit of Figure 4.8, the control law is not exactly harmonic mean, but it functions quite like a harmonic mean circuit at moderate current levels.

The figures of merit of the feedforward and feedback harmonic mean circuits are approximately the same, as far as quiescent current use, efficiency, and gain.

Feedback Versus Feedforward

The fundamental difference between the two circuits hinges on the use of feedback versus feedforward. Feedback type circuits are quite often slower than feedforward circuits, due to the fact that the control loop typically involves more active devices. The extra devices add phase shift which limits the bandwidth of the loop, limiting high frequency performance of the overall amplifier. Specifically, the NPN loop in the feedback based harmonic mean circuit involves 6 devices -- several of which are configured as common emitter stages --

while the PNP loop includes 5. Each of these devices adds phase to the loop response, requiring a lower loop bandwidth for stable operation. The feedforward loops only involve four devices each, and since they are simple Gilbert loops, are quite difficult to make unstable. On the other hand, feedforward loops are often less accurate than feedback loops, due to the fact that if any of the assumed parameters are off, the loop function is affected. For instance, in the feedforward circuit, if the matching between the I-valued current sources is poor, the output currents between the two output devices could be poorly matched. At quiescence the output currents are set separately by the two translinear loops; any mismatch between the currents will increase the input-referred offset voltage. In the feedback-based circuit, any mismatches between output stage components are less critical. If the two I-valued current sources in the feedback-based circuit are mismatched, the loop will adjust accordingly, and the only offset voltage difference will be due to second order effects.

For this design, the most critical thing is functionality – as a design intended for mass production, and commercial use, the issues possible with a feedforward design make the choice of a feedback based system simple. The additional fact that through extensive simulation and hand analysis it was found that a feedback system can easily have enough gain and bandwidth to keep high frequency behavior well controlled seals the decision to use feedback rather than feedforward.

The last decision which must be made is whether to drive the output stage with two in-phase inputs or with only a single input. The class AB control is so strong that one input can drive both output devices. [4] In the circuit of Figure 4.8, it is obvious that the bottom input current source can source current which then goes to the output transistor Q1 pulling the output lower. In the other direction, the bottom input current source can pull the base current to Q1 away by sinking current, and since the class AB feedback circuit is so strong, this will cause Q2 to source more current, leading the output voltage to rise. This action of the class AB feedback network is most accurate in the constant-product types of control; in harmonic mean circuits, the single input action is much weaker. For instance, in a constant-product type control circuit, to change the opposing output from 1 mA to 2mA requires a modification in the driven transistor's collector current of 100%. In a harmonic-mean type control circuit, the

same change in output current requires a difference in the driven transistor's current of only 2%. To accurately control such small percentage differences is very difficult, meaning that driving a harmonic-mean circuit with only one input leads to poor Class AB control. An additional problem with driving the output with a single input is that one output must be driven through an extra device. The additional device in the signal path adds additional negative phase shift, which is undesirable in a high speed op amp. The signal path through this amplifier is designed to be as symmetrical with respect to gain and phase as possible, so adding an additional device to one signal path can make a significant difference.

In the end, the decision whether to use two inputs or one input must be made taking into account the difficulty of generating two in-phase inputs. As will be seen in the next section, generating two inputs is relatively easy, so the decision to use two inputs is clear.

5. Other Design Details

As seen in the input and output sections, the decisions about the architectures of the input and output stages are quite involved. The procedure by which those stages were designed were described earlier. In this section, several other assorted parts of the design are discussed.

Intermediate Stage

As seen in the output section, it is desirable to drive the output stage with two in-phase currents. However, all of the input stages we looked at only are capable of outputting one output current. Thus, some circuitry to allow the input stage to give two in-phase outputs which can be at any DC voltage level is required.

One possible way of achieving this goal is shown in Figure 5.1a. [4] From one single-ended input, the stage gives two in-phase outputs. This stage has gain which can be easily controlled by varying the values chosen for the resistors. However, like the resistor-loaded input stage, the output voltages of this stage are set by the DC values of the collector currents in Q2 and Q3. Since one of these outputs will need to be at a V_{BE} from V_{CC} and one at a V_{BE} from ground, this circuit is unsuitable for our application.

The circuit in Figure 5.1b alleviates the DC output voltage problem, but does away with flexibility choosing gain.[4] The desired open loop gain is around 90 dB; it was found that

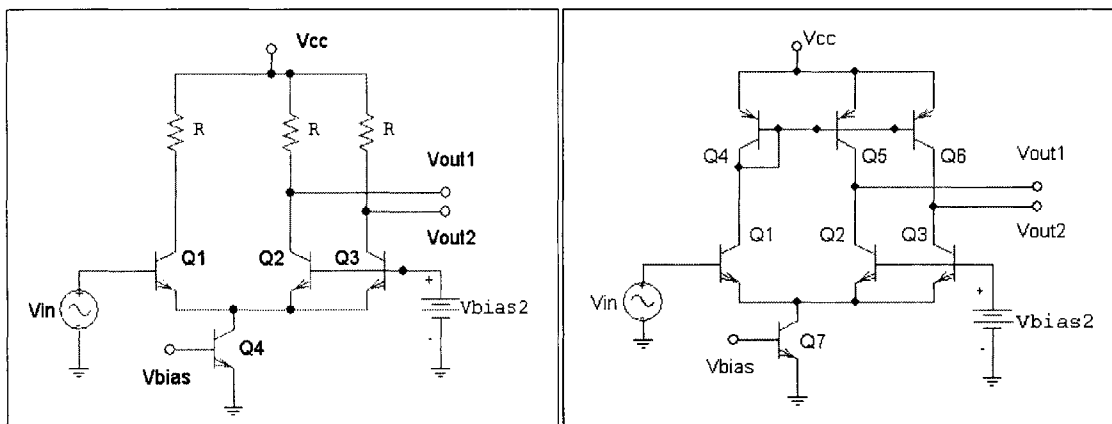


Figure 5.1a: Resistor Loaded Differential Stage Figure 5.1b: Actively Loaded Differential Stage

without an intermediate stage the gain was over 90 dB. The additional gain added by an intermediate stage only complicates the design. To lower gain, the inputs of the intermediate stage differential pairs can be degenerated, seemingly solving the excess gain issue. However, a larger problem is that the stage creates another high-impedance node, complicating compensation. The output node of the input stage consists of two collectors and the input of this stage. Since the input of this stage has a very high impedance when degenerated enough to serve our purposes, that node will have quite high impedance, and have an associated low-frequency pole. In addition, the outputs of this stage lead to the inputs of the output stage, which are also very high impedance. The creation of two low-frequency poles is to be avoided at all costs, as these poles require more complex compensation than simple Miller compensation.

A better option is shown in Figure 5.2a. As seen, it is slightly more complex than a simple differential stage, but its poles are all at quite high frequencies, making the overall amplifier much easier to compensate.

The stage shown in Figure 5.2a is a modification of the mirror part of the final input stage chosen in the input architecture discussion, which is shown for reference in Figure 5.2b. The standard mirror shown in Figure 5.2b has two separate signal paths: one inverting path, and one non-inverting path. The input to the emitter of Q8 sees Q8 as a cascode device to the

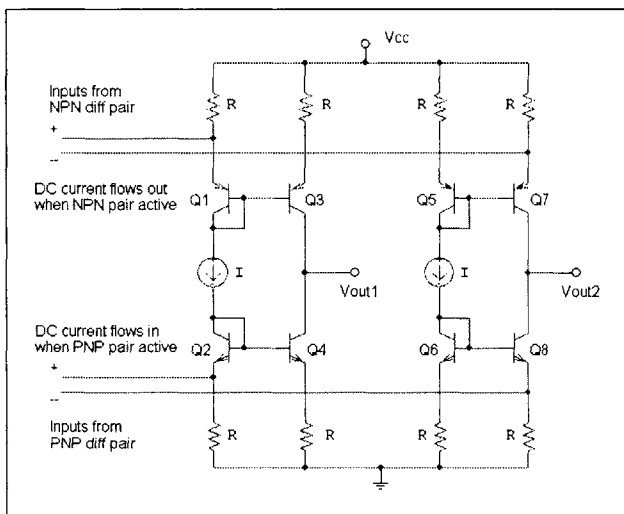


Figure 5.2a: Modified Current Mirror Stage

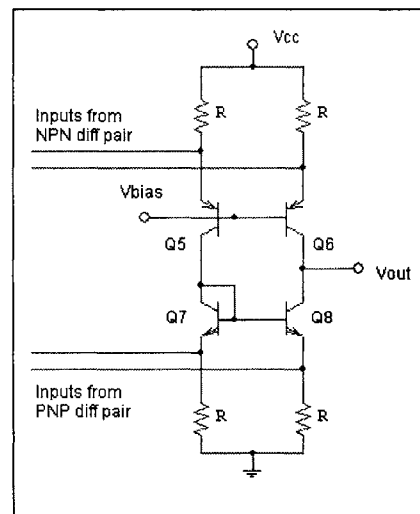
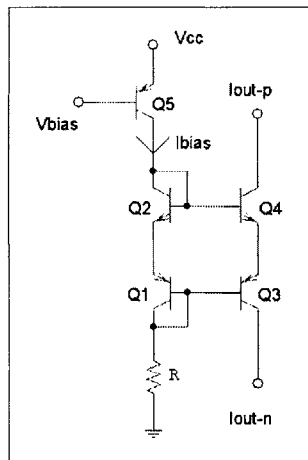


Figure 5.2b: Normal Current Mirror Stage

output, leading to no inversion. The input to the emitter of Q7 sees Q7 as a diode in series with a current source (Q5) and pushes its current through the resistor to ground. When the voltage at the emitter of Q7 rises, so do the base voltages of Q7 and Q8, and Q8 acts as an inverter to this incremental input. Thus the standard current mirror sums the differential input signals from the differential input pair to create a single output. The idea with the modified current mirror is to use these two signal paths separately to get two in-phase outputs. Thus one of each of the differential inputs goes to the inverting side of one mirror, and the other differential input goes to the non-inverting side of a second mirror. This circuit allows two in-phase outputs, and the fact that the output is two collectors allows the DC output voltages to take on a wide range of values. Since all internal nodes of the modified mirror stage are low-impedance nodes, no additional low-frequency poles are added by this stage. Lastly, unlike the previous circuit, no gain is inherent in this stage.

This stage does have two complications, however. First, it requires two floating current sources, which are only referenced to ground or V_{CC} through a V_{BE} which changes nearly 350mV across the temperature range specified. Second, as discussed in the input section, each of the input pairs has tail current only in a certain range of common-mode voltage. When a given input pair is active, each of the outputs of the pair draws $\frac{1}{2}$ of the full input differential pair DC tail current; when deactivated, the pair draws no current. In the normal current mirror of Figure 5.2b, the current draws on the parts of the mirror vary with common-mode voltage, but were symmetrical

Figure 5.3: Floating Current Source

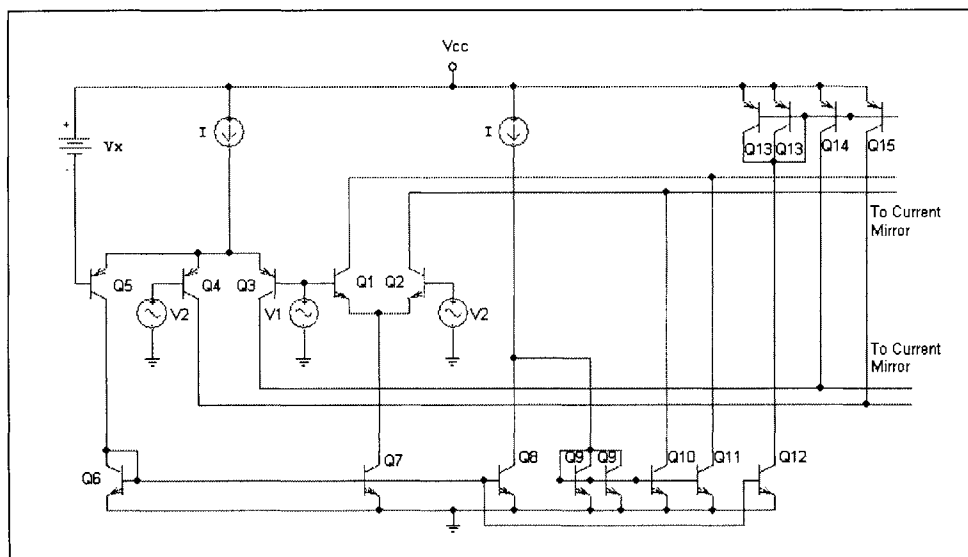


from one side to the other. In the modified circuit of Figure 5.2a, the draws are asymmetrical, and would lead to saturation in the mirror, if not dealt with.

The floating current sources are relatively easy to implement. The design used is shown in Figure 5.3. Although the “floating” source is in fact tied to the ground rail, the part of the current source facing the mirror is connected through two collectors, which allows the voltages on the output side to float as needed. As long as the output voltage range needed is anticipated and taken into account in the DC placement of the emitter of Q1, the circuit functions as a floating current source. The positive output node can swing from V_{CC} to as low as $I_{bias} \cdot R + V_{BE} + V_{CE-SAT}$, while the negative output can swing from ground to $I_{bias} \cdot R + V_{BE} - V_{CE-SAT}$. Two of these circuits are needed.

A slightly more complex problem is that of keeping the mirrors balanced despite the changes in current at the inputs. When the NPN differential pair is active, one-half of the input differential pair current leaves each of the current mirrors on the NPN input lines, while no current enters the mirror on the PNP input lines. When the PNP pair is active, the opposite situation is true. Without some sort of balancing, this leads some of the devices in the mirrors to be saturated at all times, due to the severely unbalanced currents on the sides of the mirror. In the final design, a simple compensation system was used in which the tail current of one of the input pairs is measured, and used to compensate for changes in the currents on the input

Figure 5.4:
Current
Mirror
Balancing
Circuit



lines to the mirror stage. A schematic of this compensation system is shown in Figure 5.4.

The collector current in transistor Q7 is the total tail current of the NPN pair; since the V_{BE} of Q8 is the same, the collector current of Q8 is the same. As discussed in the input stage section, the sum of the tail currents of the two input pairs is kept constant at I by the actions of Q5, 6 and 7. The collector current of Q9 is I minus the NPN collector current, and thus the total tail current of the PNP pair. Thus the current on the line from the collector of Q1 is $\frac{1}{2}$ of the tail current of the NPN pair plus $\frac{1}{2}$ of the tail current of the PNP pair, which since the sum of the two tail currents is I , is always constant at $\frac{1}{2} I$. As can be seen, the compensation current mirrors keep it so that in the absence of a differential input, the total current entering or leaving any of the lines to the current mirror stages remains constant, however the tail current is split between the input pairs. The compensation system does not affect differential currents.

With proper emitter degeneration of all of the various mirrors to reduce variations in currents with V_{CE} , it was found that the maximum deviation of the input line current from the nominal value across the full common-mode, voltage supply and temperature range could be kept to less than five percent.

Current Distribution

One of the most difficult parts of this design was the low supply current allowed. The design was to nominally operate at 800 μA of current from any supply in the range specified. The distribution of current is a difficult part of the design task – how to optimally distribute the current? It is well known that more current nearly always allows more speed and bandwidth. [6] In this design, an approximate methodology was used to distribute current.

The output section of the design requires the most current, for several reasons. First, the output devices and the emitter followers immediately before the output devices are large devices, to allow for sourcing and sinking large currents. As large devices can be approximately viewed as many parallel smaller devices, and f_T is a strong function of I_C , it is easy to see that large devices will require larger currents to achieve similar f_T as the earlier

stages. Second, the g_m of the output devices is important, as it sets the frequency of one of the non-dominant poles. As g_m is proportional to I_C , again we would like as much current in the output devices as possible. Third, the output resistance of the output devices is inversely proportional to the quiescent current through those devices – this output resistance should be as small as possible to avoid loading issues. Lastly, in order to avoid slew-limiting in the output stage itself, the quiescent current in all parts of the output stage should be large enough to drive the output as quickly as the input will allow. Of the 800 μA budget, approximately 350 μA is used in the output section.

The input section of the device also requires quite a bit of current, for several reasons. The slew rate of the amplifier is ideally constrained by the input stage tail current charging the compensation capacitor. Although we will end up degenerating the input differential pair to allow for larger error voltages, the input stage tail current still sets the eventual slew rate. The noise performance of the input stage also is highly dependent on the quiescent current – as current goes up, noise goes down. The input differential pair tail current was chosen at 100 μA , leading to about 100 μA of input stage current use.

The intermediate section of the amplifier, the twin current mirrors, are not nearly as sensitive to current as the rest of the amplifier. As it contains almost no gain, the stage inherently has high bandwidth, and can happily operate on relatively low currents. However, for good balance in the mirror, the currents must be chosen large enough that the small imperfections in the mirror balancing scheme discussed above did not lead to excessive offset voltage variations. In addition, there is a constant DC current into one side of the mirror output and a DC current out of the other side, due to imbalance in the output section and to base currents on the output stage transistors. Since these imbalance currents can add up to a microamp or two, the quiescent current in the mirrors was chosen to be small, but large enough to not be severely affected by these imbalances. Lastly, an unfortunate consequence of the chosen intermediate stage architecture is that a current equal to the input stage differential pair tail current is required simply to keep the mirror balanced, as discussed in the previous section. This brings the total usage in the intermediate section to approximately 350 μA .

The entire device could be expected to keep its bandwidth well if the current of the entire circuit is scaled down. The parasitic capacitors in the circuit are quite small, and the active devices themselves are operating on a low current but still operate well on far less current. The open-loop poles of the system would not move much with slightly lowered current, meaning the compensated bandwidth would likely not change much.

Compensation

As has been previously mentioned, efforts were made in the design of this amplifier to keep the compensation as simple as possible. The number of low frequency poles was kept as small as possible, to allow simple Miller compensation to function properly. However, due to the current constraints, the uncompensated frequency response does contain several poles below the intended unity gain frequency of the compensated amplifier. This type of frequency response is typical for low-power amplifiers, as the current constraints usually do not allow enough current to move poles to high frequencies. [1]

The most commonly used method of op amp frequency compensation is known as Miller compensation. Typically, Miller compensation is used only in cases in which there are two low-frequency poles, and all other poles are significantly above the intended unity gain frequency of the composite amplifier. The effect of Miller compensation is to split the poles – one goes to quite a low frequency, the other goes to a frequency above the intended unity gain frequency of the overall amplifier. [12] If there are more than two poles to split, one pole still goes to a low frequency, but the other two go to the same high frequency. There are two major drawbacks to Miller compensation with more than two low frequency poles. First, the fact that two poles end up coincident at high frequencies adds phase to the amplifier transfer function, even below the frequencies of the poles. In order to keep a constant phase margin, the unity gain frequency of the amplifier must be pushed down by a factor of 2.[5] In addition, the minor loop created by the Miller capacitor encounters stability problems with more than 2 poles in the loop. The minor loop must be stable for it to operate properly and split the poles – with two poles and small amounts of excess phase, the minor loop can be unstable, leading the overall amplifier to be unstable.

Several fixes for this problem have been widely researched and written about. The first and simplest solution is known as nested Miller compensation (NMC). Nested Miller compensation utilizes additional Miller capacitors. Successively larger loops are closed, each only splitting two poles. Thus, if the amplifier has three low frequency poles, the first capacitor moves one pole to high frequencies, while the second capacitor moves the second non-dominant pole to high frequencies. This technique has the advantage that it only involves one additional capacitor; however, it can be shown that for optimal stability each additional loop closed reduces the final unity-gain frequency by a factor of two. This reduction by a factor of two is unacceptable in our current application. [1, 2, 3, 4, 5]

A second popular compensation technique for amplifiers with multiple low frequency poles is known as Multi-path Nested Miller Compensation (MNMC). This form of compensation utilizes the NMC technique of multiple integrating capacitors, but also includes a parallel feedforward stage from the input to the output which takes over at high frequencies. Using MNMC, results have been reported which allow an amplifier with multiple low frequency poles to achieve bandwidths similar to those of amplifiers without the extra poles. However, MNMC requires an additional set of input devices – in our rail-to-rail application this would require two extra sets of input devices with current steering, as well as an extra intermediate stage. The excessive current required to implement the extra devices makes MNMC a poor choice for this application. [1, 2, 3, 4, 5]

If properly designed, simple Miller compensation can be made to be stable with more than two low-frequency poles. However, the results of using simple Miller is that the bandwidth must be more tightly constrained than is desirable and that the gain margin is often low. In the current design, the open loop bandwidth is simulated to be 700 MHz under typical conditions. In a normal Miller compensated op amp, the bandwidth reduction due to compensation is a factor of 2, leading to an estimate of 350 MHz of compensated unity gain frequency if the amplifier had only two low frequency poles.[1] Here, however, the extra poles lead the minor loop to be only marginally stable, and cause the compensated frequency response to have a peak just after the unity gain frequency, leading to a low gain margin. To achieve a 60 degree phase margin and good gain margin the bandwidth must be reduced to less than 120 MHz.

However, given that this amplifier is a low power rail-to-rail design, the open loop specifications are only a 45 degree phase margin and several dB of gain margin. In practice, low phase and gain margin are simply the price one has to pay for high bandwidth, low power, rail-to-rail operation. In the current case, simulations showed that simple Miller compensation could give a unity gain frequency of around 200 MHz with 45 degrees of phase margin and barely acceptable gain margin. The gain margin of the unloaded system was found to be as low as 3dB under worst-case conditions. In an improved design, this low gain margin would need to be increased.

Supply Voltage, Temperature, Common-mode Voltage Variations

Probably the toughest part of the design was making the amplifier work across the specified supply voltage, temperature and common-mode voltage variations. The supply specification was from total supplies of 2.7V to 10V – to ensure a robust design, the amplifier was designed to operate properly from 2.5 to 12V. The temperature range tested was from –40 to 100 degrees Celsius, which is larger than the typical commercial range. The common-mode voltage must be able to run from the negative rail to the positive rail.

The supply voltage variations created two major effects – first, any voltage imbalances in the circuit were greatly exacerbated at high voltage supplies. Second, at low supplies, the circuit voltage clearances became very small, especially at low temperatures. The voltage imbalances were lowered greatly by degenerating all current sources in the amplifier enough that the change in V_{CE} did not create large current imbalances and thereby large input-referred offset voltages. Attempts were made to force one V_{CE} change to offset another V_{CE} change, but often the only solution was to raise output impedances until current changes were tolerable. An example is in the twin mirrors of the intermediate stage. As the supply voltage rises the output voltages V_{OUT1} and V_{OUT2} are pinned at a V_{BE} from V_{CC} and a V_{BE} from ground, respectively. Thus, across the full supply range a ΔV_{CE} on transistors Q4 and Q7 of nearly 10 Volts was seen. This variation causes the two mirrors to tip in opposite directions, and the only method found to overcome this problem was to increase the effective output

resistance of those transistors, through cascoding. At low supplies and low temperatures, V_{BE} becomes nearly 1 V, and the headroom is greatly reduced, such that only $2 V_{BE}$ and $2 V_{CE-SAT}$ can fit between the rails. Due to this low headroom, much effort was put into biasing transistors with minimum V_{CE} voltages, and to prevent stacking of V_{BE} 's. The final design simulates well at -40 degrees Celsius and a single 2.5 V supply.

Temperature variations created two problems: first, the previously discussed lack of headroom at low temperatures and low voltages. Second, at high temperatures shrinking V_{BE} 's led to saturation of transistors unless care was taken to ensure headroom at high temperatures. Several places in the design have a V_{BE} placed across one or more V_{CE} voltages. As temperatures rise, V_{BE} 's lower by approximately $2 \text{ mV}/^\circ\text{C}$; however V_{CE-SAT} , as found previously, is proportional to $V_{th} = k \cdot T / q$, and rises as temperatures rise. At 100°C , V_{BE} is lowered to around .6V, while V_{CE-SAT} has risen to $4/3$ its room-temperature value. In the final design (Figures 6.10a and 6.10b) Schottky diodes D1 and D2 were added in the signal path to act as temperature sensitive voltage sources, to keep the twin intermediate stage current mirrors from saturating as V_{BE} shrank to less than .6V. Again referencing Figure 5.2a, it can be seen that if V_{OUT1} is attached to a node a V_{BE} from ground, that the DC value of this output will shrink towards ground as temperatures rise, and V_{BE} shrinks. If Q3 is cascoded as previously mentioned, V_{OUT1} must be large enough to support $2 V_{CE-SAT}$ voltages and the voltage across resistor R. In the final design it was found impossible to keep this condition true across temperature variations without a small extra voltage added, in the form of a 0.3V Schottky diode drop.

Common-mode variation was primarily dealt with in the intermediate and input stage architecture decisions. An additional problem was that the compound effects of base currents from the cascode devices in the intermediate stage current mirrors were found to add excessively to the input offset voltage. The lost base currents from the top cascode devices were compensated for by subtracting an equal amount of current from the bottom half of the current mirror (devices Q4 and R5 in Figure 6.10a).

Final Schematic

The final schematic for the amplifier is shown in Figure 6.10a and b. It is largely as has been discussed thus far, with a few modifications. The input differential pairs have degeneration resistors, lowering the effective transconductance of the stage, G_m , to:

$$G_m = \frac{g_m}{1 + g_m R_{\text{degeneration}}} \quad [5.1]$$

where $R_{\text{degeneration}}$ is the degeneration resistor added. This degeneration was added for several reasons. First, the DC gain of the amplifier was found to be excessively large – degeneration reduced that gain 6 dB. More importantly, degenerating the input pair raises the slew rate of the amplifier. The slew rate of the amplifier is ideally:

$$\text{Slew Rate} = I_{\text{bias}} / C_{\text{compensation}} \quad [5.2]$$

Where I_{bias} is the bias current of the input differential pair, and $C_{\text{compensation}}$ is the compensation capacitor. However, the unity-gain frequency of the amplifier is typically

$$f_{0\text{db}} = G_m / C_{\text{compensation}} \quad [5.3]$$

If we lower the effective transconductance, G_m , of the input stage we can similarly lower $C_{\text{compensation}}$ and keep the same unity gain frequency. The lowered $C_{\text{compensation}}$ leads to a larger slew rate, which we would often like, at the cost of DC gain.[12] In the case of this design, the DC gain was quite large, and lowering the DC gain a small amount to increase the slew rate of the amplifier is quite justified.

Other modifications included emitter degeneration of nearly every current source in the amplifier, to decrease the effects of voltage supply changes, as previously mentioned. A pair of complimentary emitter followers were added to each signal path in the output stage for load isolation and current gain (Q63 and Q65 in the PNP path, Q74 and Q45 in the NPN path). These devices are sized larger towards the output and run at progressively more current as they approach the output devices.[13]

The entire circuit was biased using one ideal PTAT (proportional to absolute temperature) current source.

6. Simulation Results

Specification Discussion

For a general purpose operational amplifier, there are many specifications that are important. For a rail-to-rail amplifier, several other concerns specific to rail-to-rail designs are also necessary for use of the part. Due to the extremely large number of relevant specifications, in this thesis only the most important will be covered.

All of these specifications are typical values across supply voltage, temperature, and common-mode range, unless otherwise specified.

- Power consumption – quiescent power consumption with no load.
- Output Voltage Swing – the output voltage swing on a rail-to-rail amplifier is of prime importance. Unfortunately, the maximum and minimum output voltages depend on the output load – thus this characteristic is specified at several output load resistances.
- DC Gain – for a rail-to-rail amplifier, the DC gain is a strong function of the load resistance. Thus, a graph of open-loop DC gain versus load resistance is the best way to specify this characteristic.
- Frequency response – generally, an operational amplifier’s frequency response can be described by the -3dB frequency when the amplifier is used as a follower. In addition, a Bode plot of amplifier response can aid designing feedback loops involving the amplifier.
- Input-referred Offset Voltage – this is specified as a maximum offset voltage. The input offset is defined as the voltage necessary to bring the output to the center of the voltage supplies. In rail-to-rail input amplifiers, the offset voltage can change significantly as the input common-mode voltage activates the PNP or NPN input pair. Specified as a maximum across temperature, power supply voltage, and common-mode voltage ranges.
- Common-Mode Range – the range of input common-mode voltages across which the amplifier can be expected to meet all of the other specifications. Also includes a maximum range across which the amplifier operates at all.
- Common-Mode Rejection Ratio (CMRR) – this specification indicates how the common-mode voltage affects the output of the amplifier. Ideally, this value would be infinite, but

in any real circuit the common-mode voltage does affect the output. CMRR is specified as the change in input offset voltage as the common-mode voltage ranges across the full common-mode range.

- Power Supply Rejection Ratio (PSRR) – ideally, the power supply voltage should not affect small-signal circuit operation at all. In reality, variations in power supply voltage can affect the output voltage. PSRR is defined as the change in input offset voltage as the power supply rail is changed. This test was done by increasing the power supplies by 1 volt and measuring the change in input-referred offset voltage.
- Slew Rate – the amplifier cannot change its output voltage arbitrarily fast, due to parasitic and intentional capacitances. This maximum dV_{out}/dt leads to a limitation on the size and frequency of signals that can be amplified by the amplifier without significant distortion. Slew rate is measured here in a closed-loop gain of -1, using a 2V step input, with a 1k Ω load. Note that a closed-loop gain of -1 corresponds to a feedback fraction of $\frac{1}{2}$ -- this lower feedback fraction indicates the amplifier will be relatively more stable than in unity-gain configurations.
- Settling Time – when driving a capacitive load in switched capacitor applications, the settling time of a step input is an important parameter. A representative case is measured: the settling time to 0.1% of a 2V step when the amplifier is configured as an inverter. The load is a 10pF capacitor in parallel with a 1k Ω resistor. The number reported is the slower response of the positive-going and negative-going steps. Again, the feedback fraction is $\frac{1}{2}$, leading to more phase margin than in the unity gain configuration.
- Capacitive Load Stability – nearly all operational amplifiers will go unstable if attached to a large enough capacitive load. The maximum capacitive load at which the amplifier is stable is an important parameter in deciding in what types of applications the circuit can be used. This test is done in a closed-loop unity-gain configuration with a load of a 1k Ω resistor in parallel with the chosen capacitor.
- Short Circuit Current – the maximum current driving capability of an operational amplifier is limited by several things. Thermal and device characteristics are extremely important in an actual design, but are hard to simulate effectively without doing a layout. Another important parameter is the maximum theoretical current the device can output, based on the current gain, driving capability, and series collector resistances. In a rail-to-

rail device, the maximum output current is typically a function of one of the static currents in the output stage. This parameter is measured by simply short-circuiting the output and sweeping the input voltage to determine how much current the part can source/sink.

Simulation Results

Specification	Goal	Simulation Result
Current Consumption	<1mA	< 900 uA
Voltage Swing	Rail-to-rail	w/in 100mV of rails at a 10kΩ load
DC Gain (open loop)	> 80 dB	95 dB
Unity Gain Frequency	> 160 MHz	200 MHz (typical)
Phase Margin	> 40 degrees	45 degrees (at unity gain frequency)
Gain Margin	> 6 dB	~3 dB
Systematic Offset Voltage	< 1.5 mV	< 800 μV (maximum)
Common Mode Range	Rail-to-rail	0.3 V past each rail
CMRR (DC)	> 80 dB	86 dB
PSRR (DC)	> 70 dB	84 dB
Slew Rate	> 30 V / us	80 V / μs
Settling Time to .1%	< 125 ns	90 ns
Maximum Capacitive Load	> 20 pF	> 50 pF
Short Circuit Current		
Sinking	>20mA	48mA
Sourcing	>20mA	31mA

Table 6.1: Simulation Results

Discussion

As can be seen in Table 6.1, nearly all specifications have been exceeded. A short discussion of issues with each follows.

The current consumption of the part is quite acceptable. The current use of the design could likely be further optimized by reducing the large current use of the intermediate stage. As mentioned in the current allocation discussion, the intermediate stage is relatively insensitive to current levels. Its current use of over 1/3 of the supply current seems unjustified. Although not immediately obvious, it seems likely that there is some way to reduce the intermediate stage's current use and improve the other specifications of the amplifier, without increasing supply current use.

The voltage swing of the part again is well within specifications. As shown in Figure 6.1, the swing of the amplifier reaches well within 100mV of each rail under light loads. Even at moderate loads such as a 1kΩ resistor, the swing is still nearly rail-to-rail.

Many rail-to-rail devices have quite low DC gains, due to the problems inherent in achieving both speed and gain, especially in a design required to use a common-emitter output. This part has plenty of DC gain, and in fact begs the question whether some of that DC gain could be traded for more bandwidth. However, the fact that the architecture fundamentally involves only a differential pair, two emitter followers, and a common-emitter output stage indicates that perhaps this process simply makes getting large gains quite easy. Based on the full schematic in Figure 6.10, a simplified formula for the DC gain of this amplifier is:

$$\frac{g_{m-input}}{1 + g_{m-input} \cdot R_{deg}} \cdot \frac{2k\Omega}{2k\Omega + 1/g_{m-intermediate}} \cdot \frac{r_{o-intermediate}}{r_{o-intermediate} + r_{in=output}} \cdot \beta_{NPN} \cdot \beta_{PNP}^2 \cdot R_{load} \quad [6.1]$$

where we have approximated the gain of the overall amplifier as the gain of the PNP signal path, and assumed that R_{load} is significantly less than r_o of the amplifier. The denominator in the g_m term is due to the previously mentioned degeneration of the input pairs. The $g_{m-intermediate}$ term comes from the current divider between the 2kΩ load resistor and the inputs to cascode devices, as previously mentioned. The $r_{o-intermediate}$ term comes from the previously mentioned current divider between the output resistance of the intermediate stage and the input of the output stage. The values of β in the above equation must be evaluated at the correct collector currents – at the used collector currents, β_{NPN} is only around 80, while β_{PNP} is

reduced to only around 50. At a $1\text{k}\Omega$ load, Equation 6.1 evaluates to 95 dB – slightly more than measured, but quite close.

The open-loop unity gain bandwidth of this amplifier exceeds specifications, but is still mildly disappointing. With around 700 MHz of uncompensated bandwidth, one would expect more compensated bandwidth. Using the Nested Miller Compensation technique would normally lead to an estimated compensated UGF that is one-fourth of 700 MHz, or 175 MHz, with good phase margin and gain margin.[1] The worst-case bandwidth for the simple Miller compensation used was around 180 MHz. The compensation used leads to a higher nominal UGF of 200 MHz, but at the cost of worse gain margin and phase margin. The phase margin of the amplifier met specifications, and is in the normal range for high speed rail-to-rail parts. However, the gain margin did not meet specifications. It is nominally acceptable for some applications, but would need to be increased for use in commercial applications. The ability to allocate more current to the output stage would likely alleviate the gain margin issue.

The systematic offset voltage, common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) of the amplifier are well within specifications across all temperature, supply, and common-mode ranges. The common-mode rejection ratio can be significantly less in the small portion of the common-mode range in which the input stage switches which of the input pairs is active, but the device will likely seldom be used exactly in that region.

The slew rate of the device is acceptable. Using the simple formula to calculate slew rate of $\text{Slew Rate} = I_{\text{tail, input stage}} / C_{\text{compensation}}$ leads to an estimate of nearly 185 V / us for slew rate. [12] The observed slew rate is not quite half that, for one main reason -- the nearly 6 dB loss going through the intermediate stage current mirrors. The input impedance of the output stage is extremely high – nearly $10\text{ M}\Omega$. The output resistance of the cascoded intermediate stage is quite high as well, around $12\text{ M}\Omega$, but this divider between the intermediate stage output resistance and the output stage input resistance leads to nearly a factor of two loss in current. One way of reducing this loss is to increase the output resistance of the intermediate stage, but with the PNP devices in the intermediate stage having Early voltages of only around 16 volts,

the improvement is difficult to make. An easy way to increase the slew rate would be to further degenerate the input pairs, lowering the effective g_m of the input stage, which would allow choosing a smaller compensation capacitor. However, the compensation capacitor is already quite small, at 540 fF, and its exact effective value will be moderately affected by the many parasitic capacitances in the circuit. Further reducing the compensation capacitor could lead to a less robust design, as variations in parasitic capacitance could further reduce the gain margin.

The settling time of the amplifier to a step input is well within specifications. However, for an amplifier with 200 MHz of UGB, this settling time is moderately slow. If given a step input small enough to avoid slew-rate limiting, a well damped 200 MHz amplifier would be expected to settle to .1% in approximately 7 amplifier time constants. Since this test is done in an inverting connection, where the amplifier has a feedback fraction of $\frac{1}{2}$, means the effective time constant of the amplifier will be $\tau = \frac{1}{2} \cdot (2\pi f_{0dB})^{-1}$, or that the amplifier should settle in less than 14 ns.[7] The fact that the amplifier took 70 – 90ns to settle is an indication of the effect that slew-rate limiting and small phase margin has on settling time. With an 80V/ μ s slew rate, it should take only around 25 ns to slew 2V -- as seen in Figure 6.8, the rest of the time is spent in small-signal settling. Increasing the slew rate or phase margin would lower the overall settling time, but as previously discussed, the slew rate is near the practical maximum for this architecture, and it is quite difficult to increase the phase margin.

The maximum capacitive load the circuit can drive is a somewhat fuzzy specification. In practice, not only stability matters, but settling time, peak overshoot, and other specifications are important. In simulation, the circuit was strictly stable at capacitive loads exceeding 50 pF, however relative stability suffered significantly at loads exceeding 35 pF, exhibited in the increasing peak overshoot and ring time.

As hinted at in the specification definition, short-circuit current at high levels is often more a function of layout and thermal considerations than of circuit performance. However, this circuit does have plenty of current gain – if properly laid out and with short-circuit over-current protection it could be expected to exceed specifications on short-circuit current. The

calculation for short circuit current, again referring to Figure 6.10, the full schematic of the amplifier is $I_{Short-Circuit} = I_{source} \cdot \beta_{NPN}^2$. I_{source} in this case is the current from static current sources Q9 and Q66, or 10 μA and 20 μA , respectively. For the PNP side, β_{PNP} would replace β_{NPN} in the previous equation. Using the previously mentioned β values at the appropriate current levels, we quickly estimate that the circuit should be able to source 50mA, and sink 64mA. The simulated values for both of these parameters are about a factor of two below these calculations, due to lowered β at very high collector currents.

Several representative figures are included in this chapter. Figure 6.1 is a plot of the output swing of the amplifier as a function of load resistance. As the necessary sinking and sourcing currents lower, the saturation voltage asymptotically approaches V_{CE-SAT} for the device. Figure 6.2 is a plot of the DC gain of the amplifier as function of load resistance – once the output load resistor surpasses the intrinsic output resistance of the amplifier, or about 150k Ω , the gain stops rising, as the effective load is primarily determined by the output resistance of the amplifier.

Figure 6.3 is an open loop bode plot of the full amplifier, without any compensation applied. Figure 6.4 is an open loop bode plot with the compensation capacitor (c_m) of 540 fF included, with a 1k Ω load. Figure 6.5 is an open loop bode plot with a 10k Ω load – note the troublesome peak in the frequency response after the unity gain frequency. Figure 6.6 is a bode plot of the system in a simple unity-gain configuration. Note the lack of visible peaking in the frequency response.

Figure 6.7 is a plot of the circuit in unity-gain configuration, following a 1V peak-to-peak sine wave. Note the fact that neither output device current ever goes to zero, due to the Class AB control scheme. Figure 6.8 is the response of the amplifier connected as an inverter to a 2 volt step – due to the slew-rate limiting for most of the response, only slight peaking is visible. Figure 6.9 is the response of the same configuration to a 100 mV step. Here more peaking is visible, due to the lowered slew period. The extra peaking here is due to the relatively low phase margin of the system – only 45 degrees. Both of these configurations benefit from the previously mentioned feedback fraction of only $\frac{1}{2}$ in the inverter configuration leading to more phase margin than in the unity-gain follower configuration.

Simulation Conclusions

The amplifier simulates well. In transient analysis including large and small signal steps, the step response is well controlled. The slew rate allows operation up to large signal magnitudes at low frequencies, and moderate amplitudes at high frequencies. The settling time is quite good, and the high frequency behavior is well controlled. With the exception of gain margin, all specifications have been met.

The unity gain bandwidth of 200 MHz, gain of 95 dB and power consumption of less than 2.3 mW at a 2.5V supply place this simulated design among the fastest commercially available amplifiers.

Representative Figures

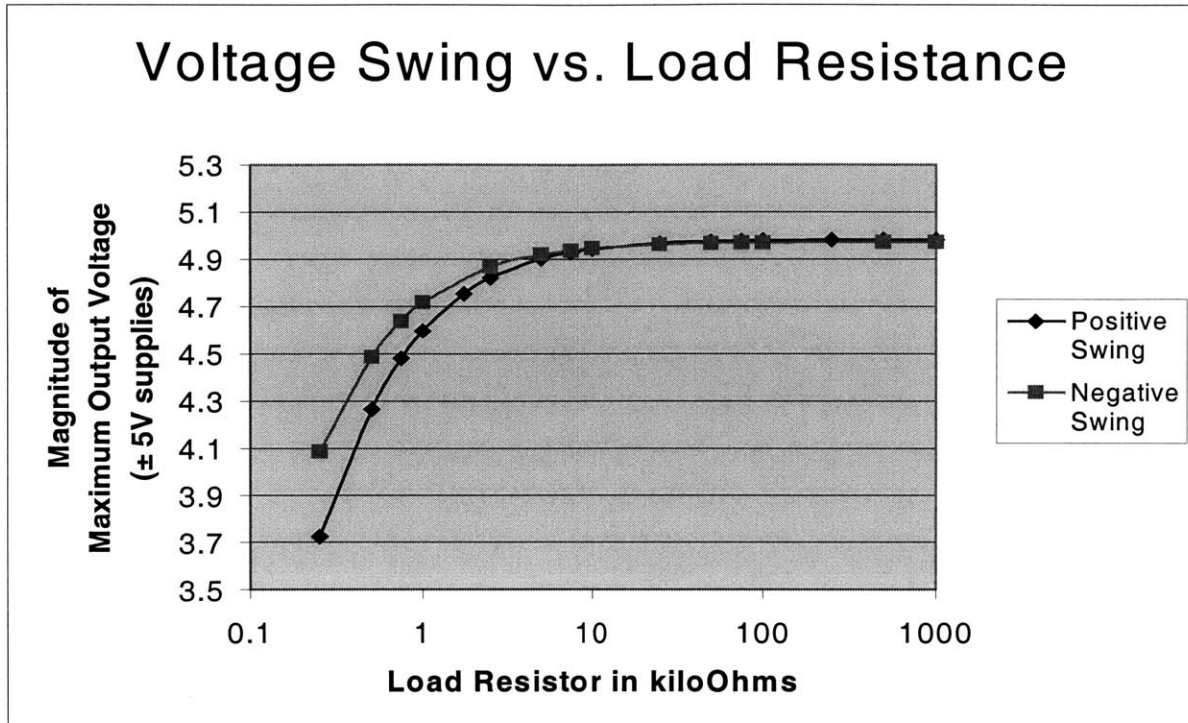


Figure 6.1: Gain Versus Load Resistor

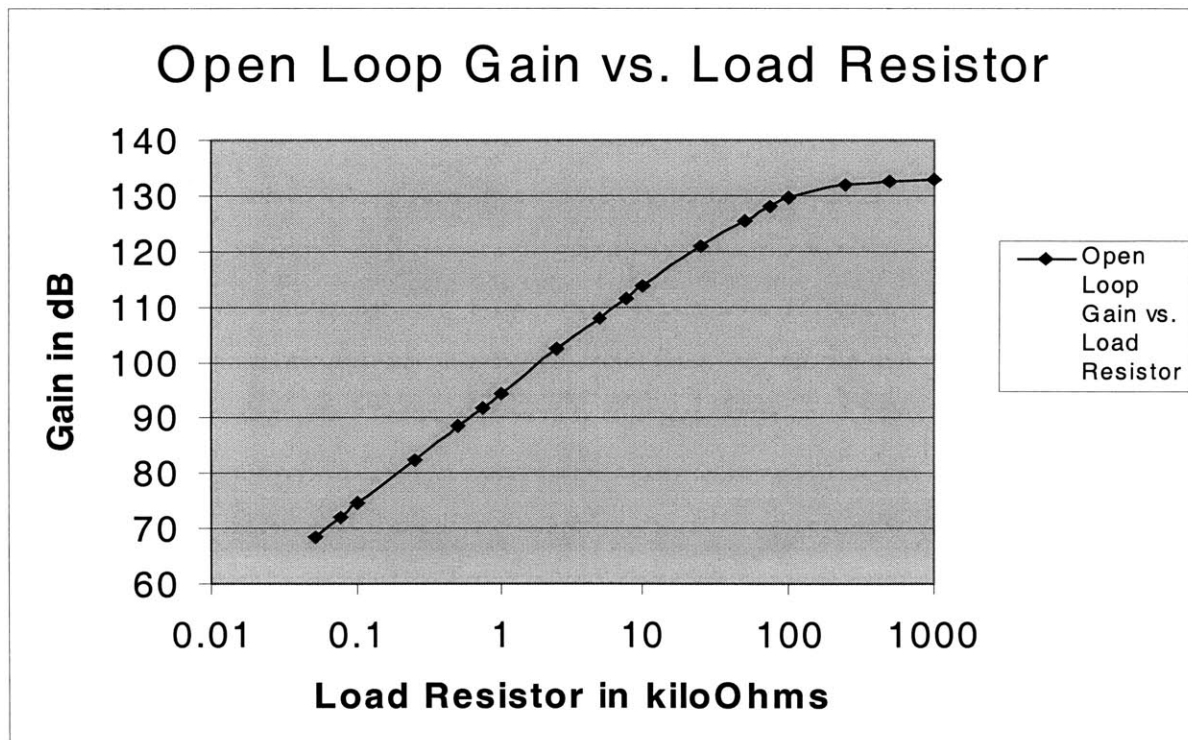


Figure 6.2: Open Loop Gain versus Load Resistor

Open Loop Bode Plot
loadr = 1k

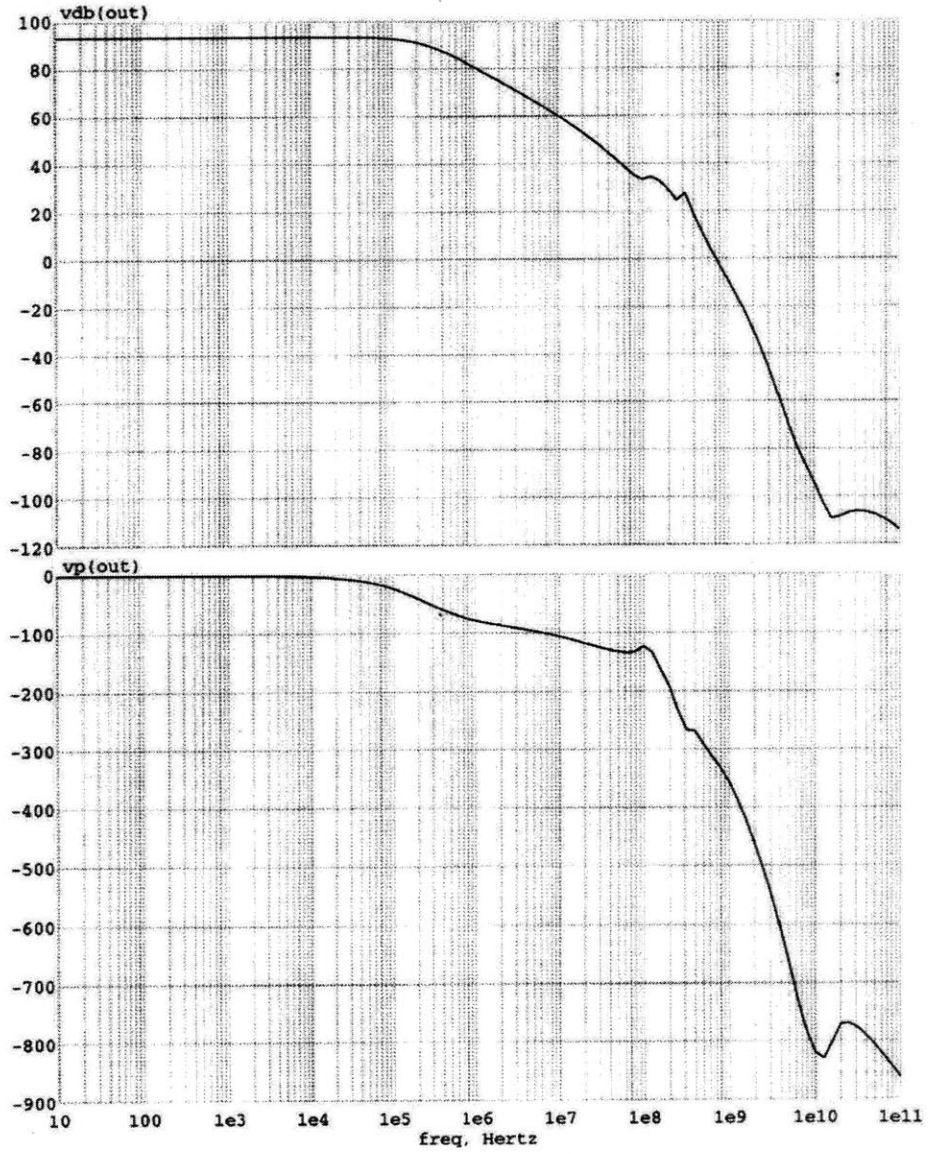


Figure 6.3: Open Loop Bode Plot – no compensation capacitor; 1kΩ load

Open Loop Bode Plot - cm = .54p
loadr = 1k

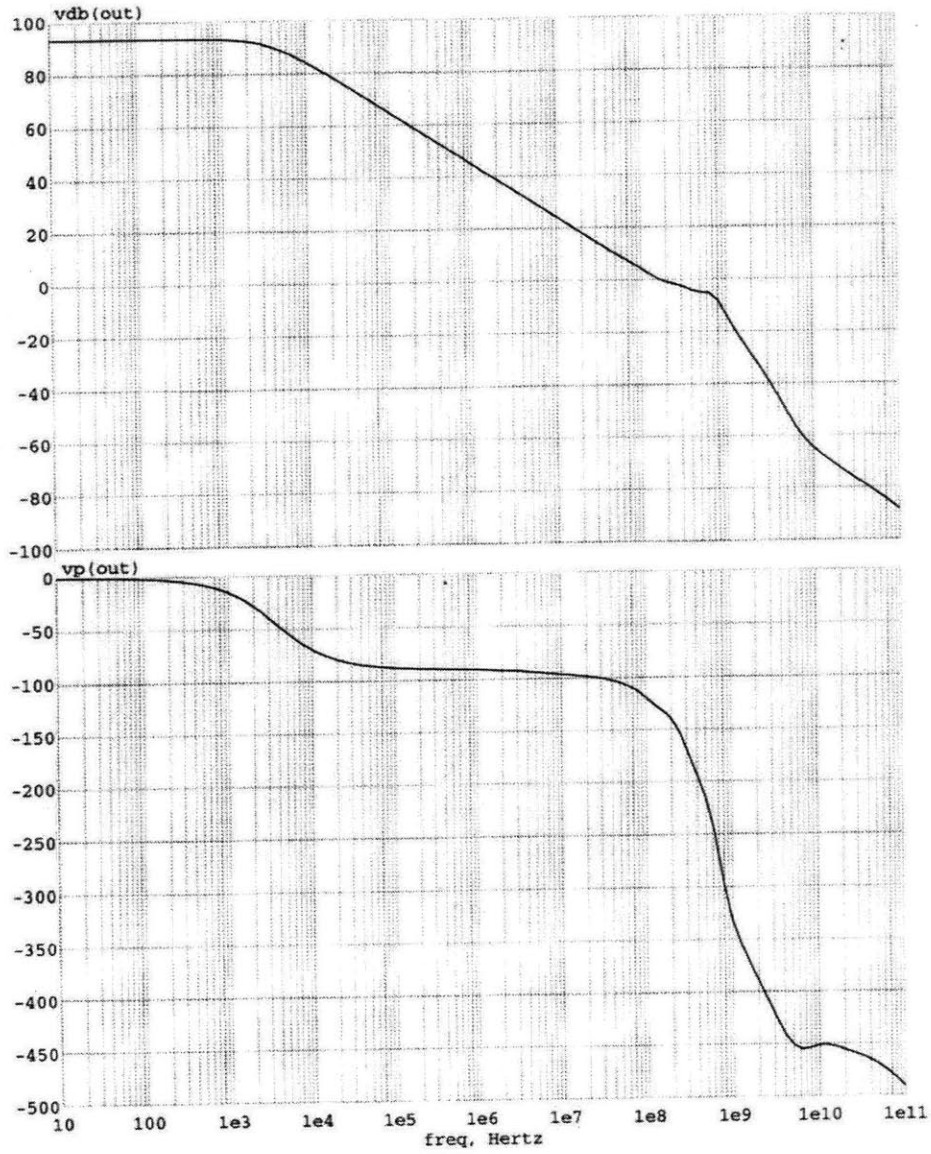


Figure 6.4: Open Loop Bode Plot – compensated; 1kΩ load

USER: rsoenne

Mon Apr 23 12:26:30 2001

Open Loop Bode Plot - cm = .54p
loadr = 10k

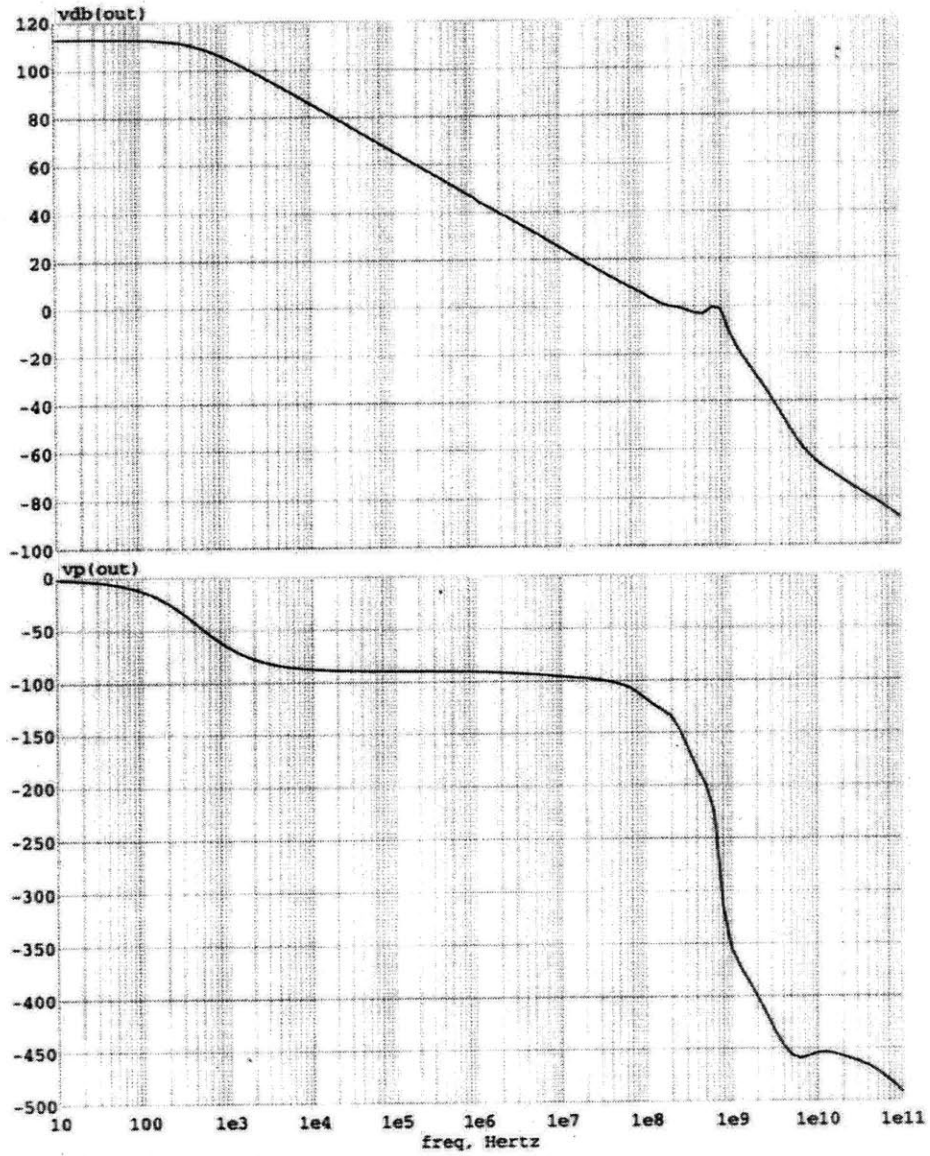


Figure 6.5: Open Loop Bode Plot – compensated; 10kΩ load

Unity Gain Response
loadr = 1k; loadc = 0p

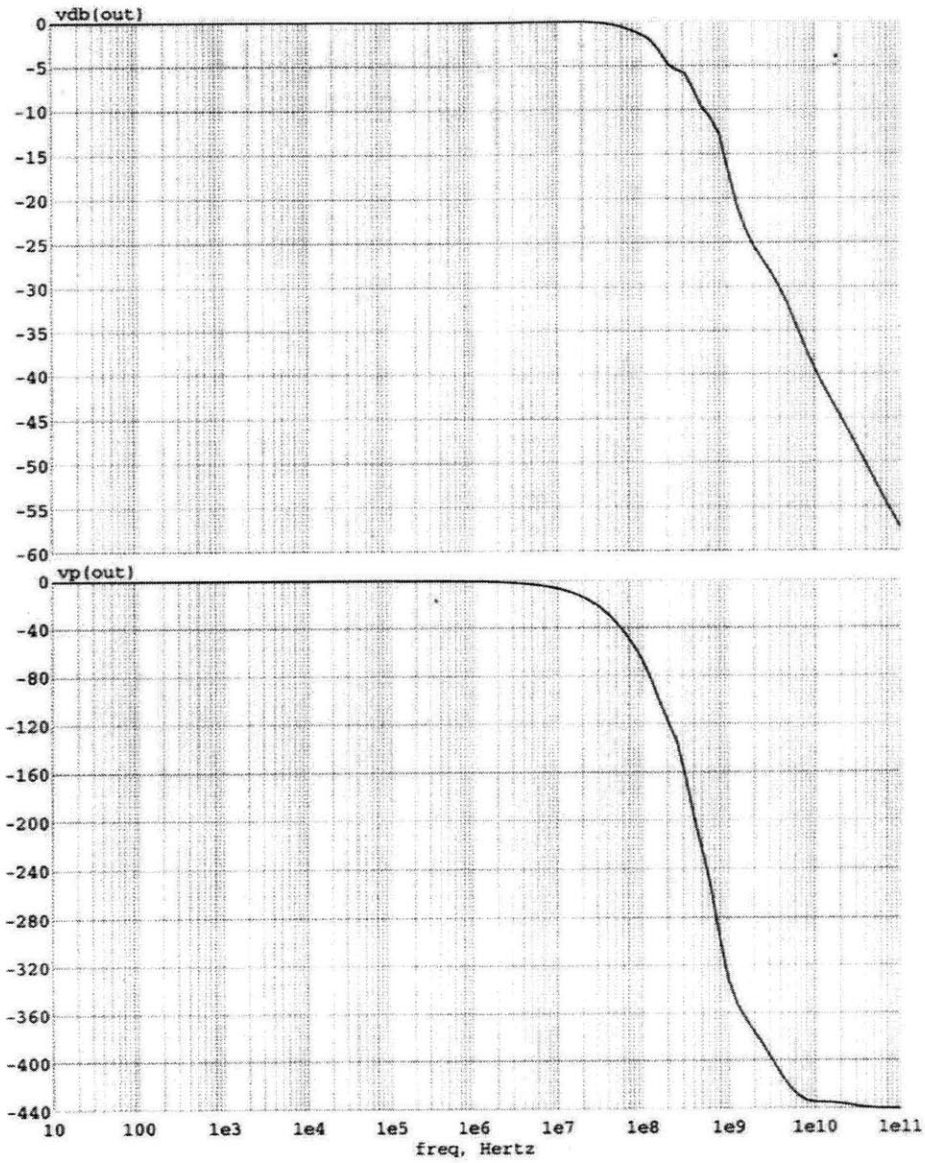


Figure 6.6: Unity Gain Bode Plot -- compensated; 1kΩ load

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Unity Gain Response -- 1 MHz 1V p-p sine wave
loadr = 1k; loadc = 0p

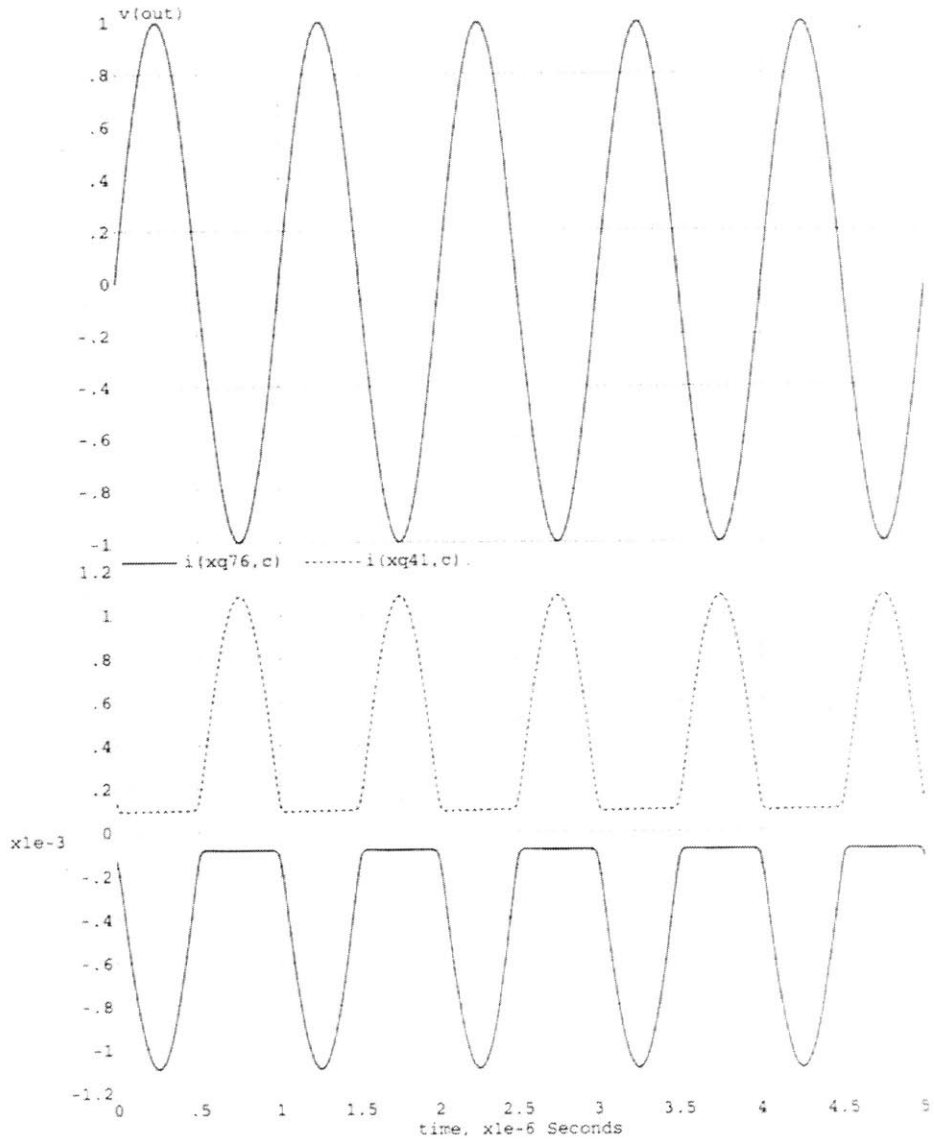


Figure 6.7: Waveforms of a 1 MHz signal; amplifier connected in unity gain mode

USER: rsoenne

Mon Apr 23 16:09:58 2001

Inverter 2 Volt Step Response
loadr = 1k; loadc = 10p

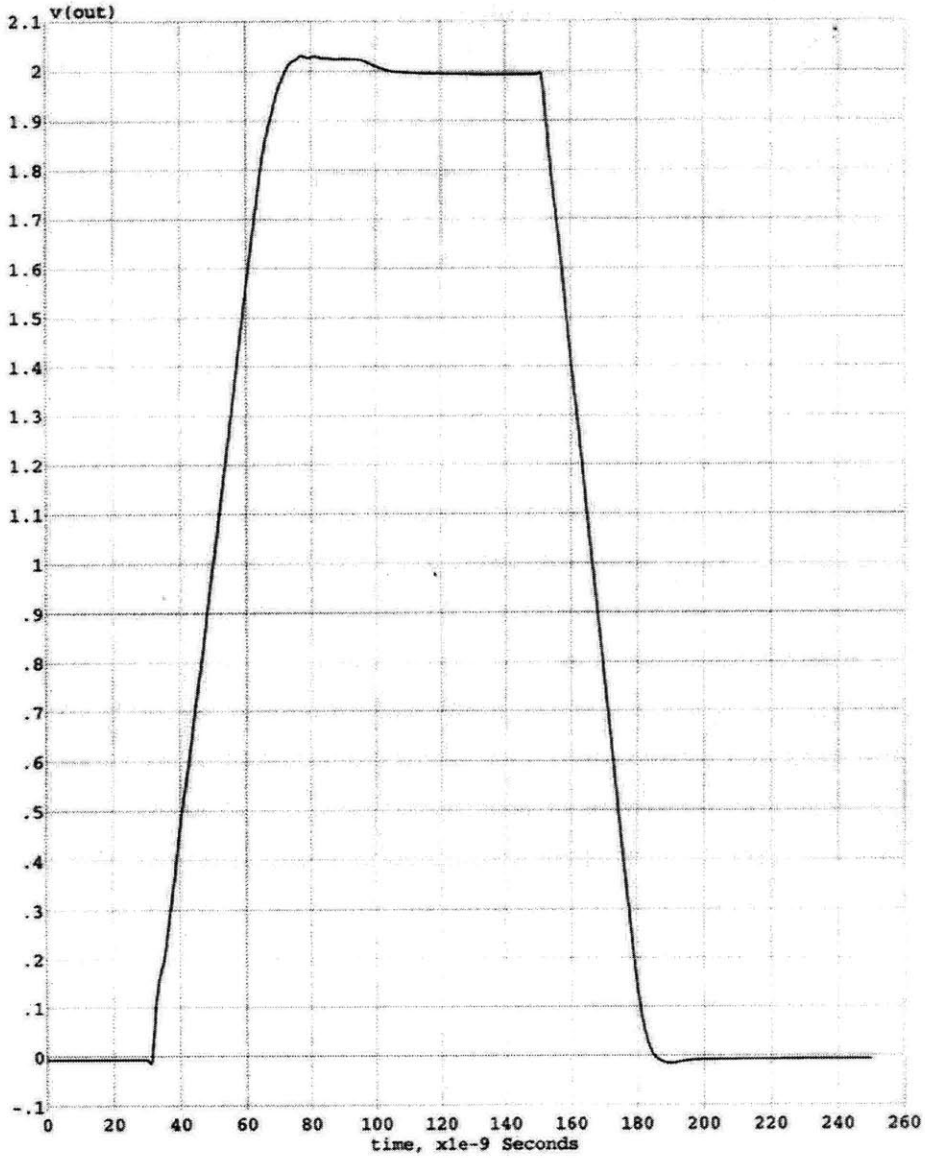


Figure 6.8: A 2 volt step response; 10 pF load

Inverter Step Response
loadr = 1k; loadc = 10p

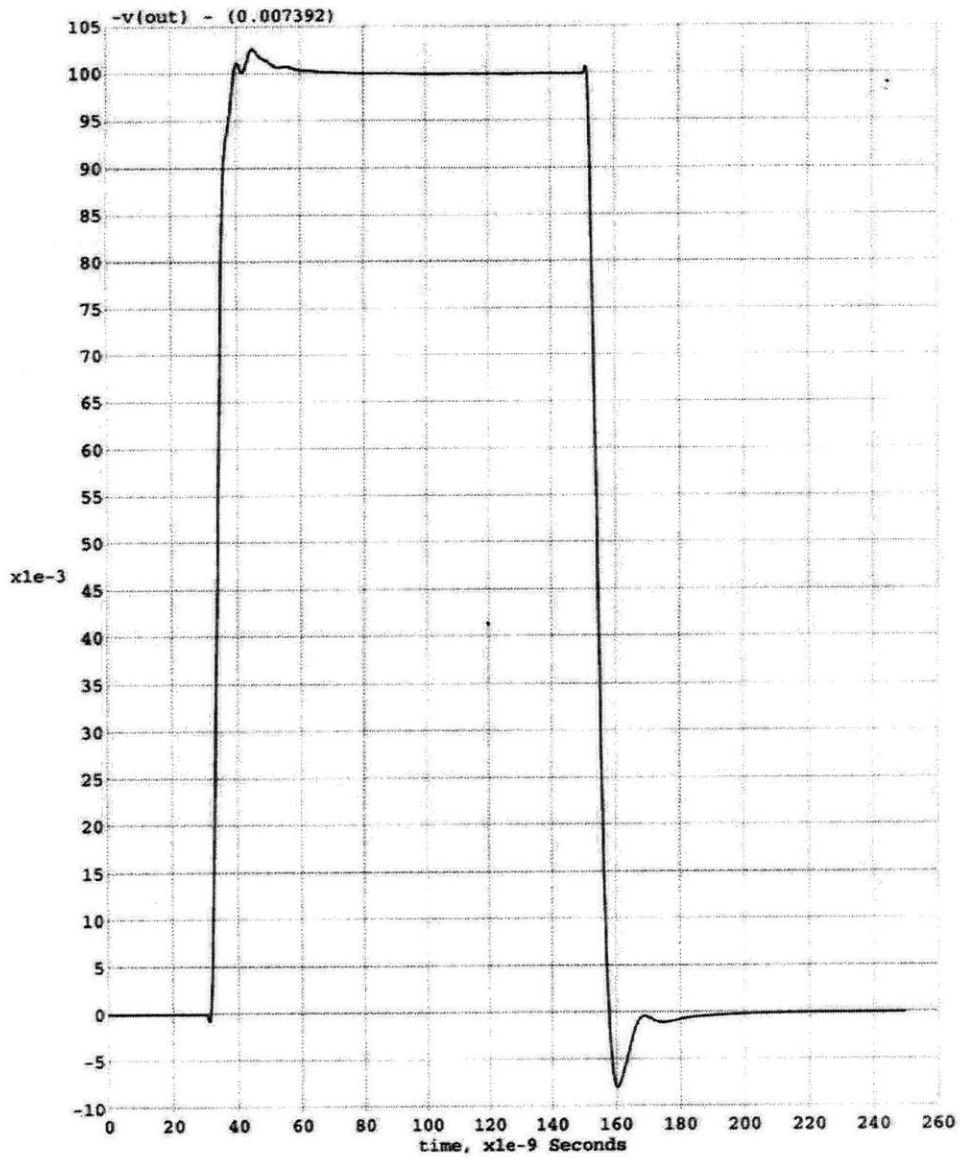
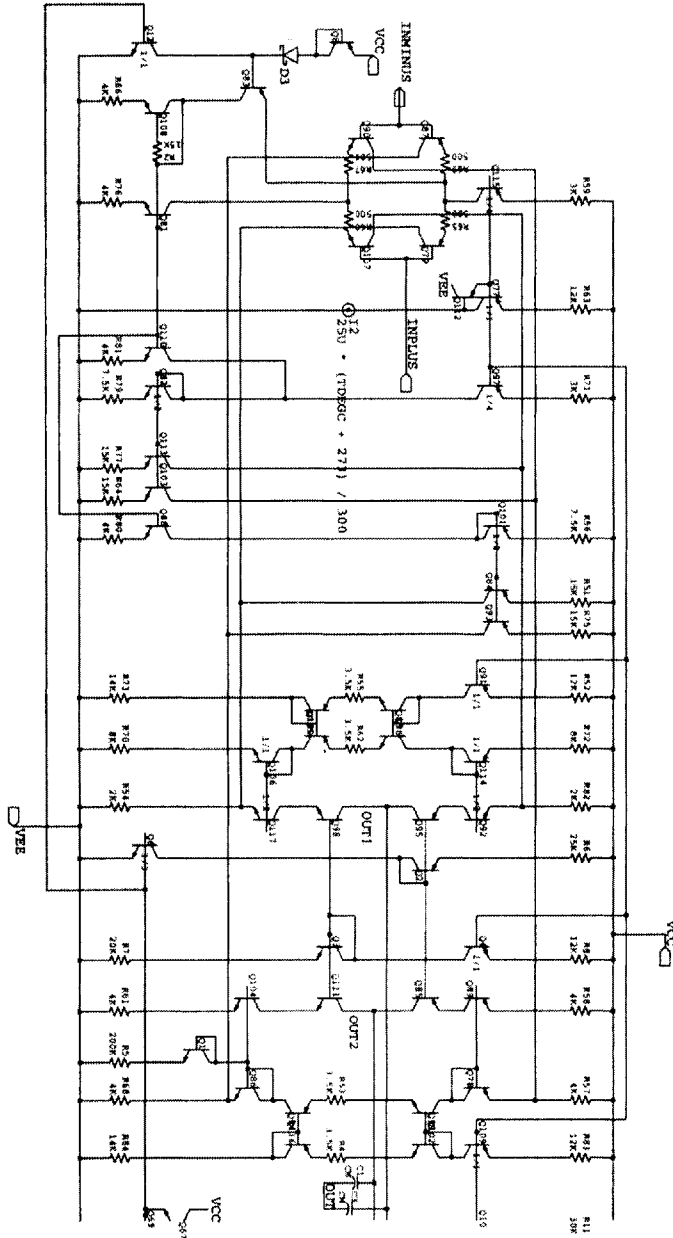


Figure 6.9: A 100 millivolt step response; 10 pF load



User: rsosenne Plotted: Mon Apr 23 17:32:45 2001

Figure 6.10a: The left half of the full schematic of the final design

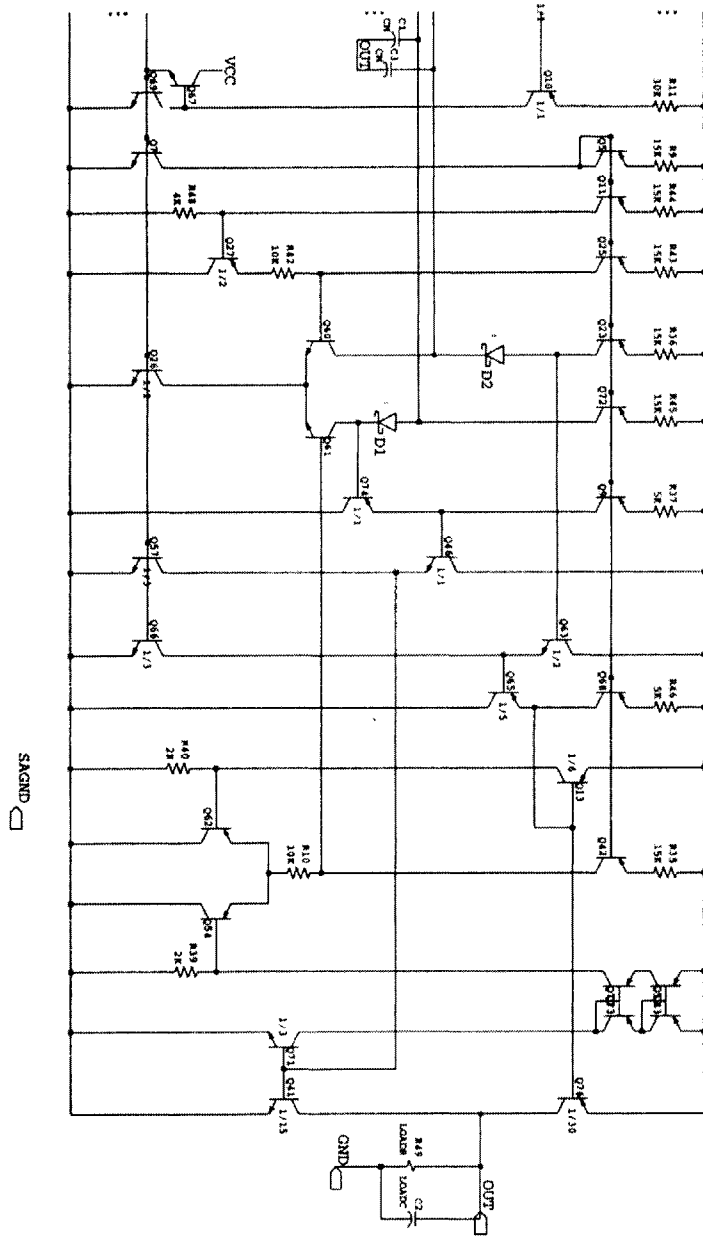


Figure 6.10b: The right half of the full schematic of the final design

Conclusion

A high-speed, low-power, low-voltage rail-to-rail operational amplifier has been designed and simulated. While the input and output stages are somewhat constrained by the rail-to-rail specifications, the intermediate stage, current distribution, and Class AB control architecture decisions are underconstrained, and involved a significant amount of work to decide what architectures to use.

In simulation, the amplifier is truly rail-to-rail, and operates at supply voltages from 2.5V to 10V, across a -40 to 100 degree Celsius temperature range. In all, the amplifier typically has 200 MHz of unity gain bandwidth, while dissipating only 2.3 mW at a 2.5 V supply. The amplifier is stable at a 50 pF capacitive load, and can source and sink over 20 mA.

The designed amplifier is suitable for use as a high-speed operational amplifier in low-voltage low-power situations such as handheld or battery operated equipment. Further work will hopefully include laying out this circuit and testing functionality.

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