Oversampled Pipeline A/D Converters with Mismatch Shaping

by

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Abstract

This thesis introduces a technique to improve the linearity of pipeline analog to digital converters (ADC). Through a combination of oversampling and mismatch shaping, the distortion introduced by component mismatch is modulated out of the input signal frequency band, where it can be removed by subsequent digital filters, significantly improving the linearity.

Mismatch shaping can be realized in traditional 1-bit-per-stage pipeline ADCs, but suffers from some fundamental limitations, which limit its effectiveness at pushing the distortion out of band. These limitations can be alleviated by using a 1 bit/stage commutative feedback capacitor switching (CFCS) pipeline design, due to the properties of the CFCS ADC's transfer characteristic, which has reduced differential nonlinearity (DNL) and an even integral nonlinearity (INL). The CFCS converter offers the foundation for the implementation of many different algorithms for mismatch shaping, some with very simple circuit realizations. It is possible to generalize some of these ideas to multi-bit-per-stage pipelines, but with reduced effectiveness.

A test-chip was fabricated in a 0.35μm CMOS process to demonstrate mismatch shaping in a 1-bit-per-stage CFCS pipeline ADC. The experimental results obtained from this chip indicate that the Spurious Free Dynamic Range (SFDR) improves by 8.5dB to 76dB when mismatch shaping is used at an oversampling ratio of 4 and a sampling rate of 61MHz. The Signal to Noise and Distortion Ratio (SNDR) improves by 3dB and the maximum Integral Nonlinearity (INL) decreases from 1.8LSB to 0.6LSB at the 12-bit level.

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I would like to thank my nephews and nieces Sarah, Khadeejah, Aziz, Ahmed and Umar for being so wonderful. Thank you Maryam and Sumayyah for your continuous love, and thanks also to Anas.

'My Lord! bestow on them (my parents) thy Mercy even as they cherished me in childhood." (The Quran: The Night Journey)

"All praise is due to God, the Lord of the Worlds. The Beneficent, the Merciful." (The Quran: The Opening)

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Chapter 1

Introduction

The accurate digitization of wide-band signals is needed in a great variety of applications. These include wireless base-stations, digital subscriber lines, and high speed networks. The signal bandwidths in these applications are relentlessly increasing with new product generations, placing tough demands on the analog front-ends. For example, the need to filter these wide-band signal prior to digitization to avoid aliasing of out-of-band signals, requires the use of wide-band filters with narrow transition bands. These filters invariably have high orders and are difficult to design in practice. Although it is possible to oversample the input signal to relax the filtering requirements by expanding the transition band, this does demand higher sampling frequencies in the Analog to Digital Converter (ADC). The wide bandwidth of the input signal limits the practically achievable oversampling ratio in current technology to between 4 and 8.

This work investigates the use of pipeline ADCs under these low oversampling conditions. In particular, it develops mismatch shaping algorithms for pipeline converters [1, 2]. Mismatch shaping, a technique which was developed for delta-sigma converters [3], pushes the distortion introduced by component mismatch out of the signal band, thereby improving the signal-to-noise ratio (SNR). The technique has its origins in an approach called dynamic element matching which was developed to improve the linearity of digital to analog converters [4]. It was later used to help improve the stability of delta-sigma converters by allowing

for the use of multi-bit quantizers [5]. Dynamic element matching, in its modern form, randomizes the distortion introduced by component mismatch and spreads it evenly over the entire Nyquist band. Mismatch shaping, on the other hand, does not merely attempt to whiten the distortion, but it tries to minimize the distortion energy in the signal band.

1.1 High Performance ADCs at Low Oversampling Ratios

In recent years, a number of different architectures have been used in low oversampling applications where both high speed and high resolution are needed. These architectures include delta-sigma modulators, pipeline converters, and folding and interpolating converters. All of these architectures can be implemented in CMOS, however, folding and interpolating ADCs are better suited for Bipolar or BiCMOS processes where transistors with good matching properties are available [6, 7]. CMOS implementations suffer from the poor matching properties of the MOS transistors, which are an order of magnitude worse that the matching properties of capacitors and resistors, limiting the converters to about 8bits. Averaging resistors can be used to improve the resolution [8], but analog calibration is unavoidable if high resolution is needed [9]. The improvement in the resolution in [9] is achieved using an analog calibration scheme, which adjusts the zero crossing of all the folding amplifiers.

Delta-sigma modulators are very popular ADCs in applications where high oversampling ratios are possible [10]. At high oversampling ratios delta-sigma ADCs have many advantages compared with conventional ADCs. These advantages include:

- Shaping of quantization noise thereby reducing in-band quantization noise.
- Ease of anti-aliasing due to inherent oversampling.
- Tolerance to component mismatches.

In delta-sigma converters employing a single loop and 1-bit feedback [10], the converter is inherently linear, and hence does not require good component matching.

Delta-sigma converters with 1-bit feedback generally require a large oversampling ratio in order to achieve a high signal-to-noise ratio. The reason for this is, first, the quantization noise of the resulting converter is directly proportional to the quantization noise of the D/A converter in the feedback path. The 1-bit D/A converter in the feedback introduces large quantization noise. Second, the order of the loop has a diminishing effect on the signal-to-noise ratio for the loop to remain stable at high order [11]. The cascaded or MASH structure [12, 13] was developed to circumvent the instability of high-order delta-sigma converters, and thus increases the signal-to-noise ratio at a given oversampling ratio. Unfortunately, the MASH architecture is much less tolerant to component mismatches even when 1-bit feedback is used, as it requires the replication of the analog filtering in the digital domain. Any mismatch between the analog and digital filters results in quantization noise leakage, which degrades the signal-to-noise ratio. Moreover, since the MASH is built using first and second order loops to attain unconditional stability, it is prone to limit-cycle tones which are unavoidable in low order loops with 1-bit feedback. This makes MASH unsuitable for applications where a low oversampling ratio is desired.

Another method for increasing the signal-to-noise ratio of delta-sigma converters is to increase the number of bits in the feedback D/A converter. An unfortunate consequence of multi-bit feedback is that the D/A converter must now be accurate to the final resolution of the delta-sigma converter. For example, in a delta-sigma converter with a target SNDR of 98dB (16 bits), the D/A converter in the feedback path must be accurate to 16 bits, even if the D/A converter has a resolution of only 2-bits. A number of techniques have been developed to overcome the accuracy problems in the multi-bit feedback A/D converters. They include self-calibration [14], dynamic component matching [15] [5], and mismatch shaping [3].

There have also been attempts at reducing the quantization noise over the entire Nyquist-band, resulting in delta-sigma converters which do not require oversampling. This is accomplished either through parallel architectures which operate on different frequency sub-bands [16], or pipeline architectures which unravel the delta-sigma loop [17]. Both ap-

proaches rely on significantly increasing the analog hardware. Parallel architectures also suffer from path mismatches which need to be calibrated [18]. At high sampling speeds it is anticipated that the path mismatch will be dominated by time-varying dynamic errors and clock skew between the paths [19] which cannot be calibrated.

Pipeline converters have been traditionally applied to Nyquist-rate sampling. Although pipeline A/D converters are relatively simple and power efficient, component mismatch limit their accuracy to about 10 bits. Numerous techniques which include self-calibration [20] [21] [22] [23], error-averaging [24], ratio-independent [25], and reference refreshing [26] methods have been devised to remove errors due to component mismatch. A technique applicable only to cyclic A/D converter has also been devised [27]. Except for self-calibration techniques, all these techniques take up extra cycles of the valuable conversion time, reducing the throughput of the converter significantly, and the added complexity often increases the power consumption considerably. Self-calibration techniques, on the other hand, remove component mismatch without increasing the conversion time. Depending on the particular self-calibration technique used, power consumption can be comparable to standard pipeline converters or can be substantially increased. The drawback of self-calibration is the additional complexity and the necessity of the calibration period during which the converter is inoperable. The missing samples during this period can be generated using nonlinear interpolation [23], but this results in lower accuracy. Alternatively, redundant hardware can be used to avoid missing samples [28], but this inevitably increases power consumption and complexity. In practice, factory calibration has been preferred. However, to maintain calibration stability, the ADC errors must be completely dominated by capacitor errors over the entire life of the device [29]. A recently reported pipeline converter using commutative feedback capacitors does not require self-calibration, neither increases conversion time nor adds more power consumption [30] [31]. Although this technique offers superior differential linearity, the integral linearity still depends on capacitor matching. Therefore, this technique is suitable for applications in which the integral linearity is less important than differential linearity.

In comparing delta-sigma converters and pipeline converters for wide-band signals, for example 50-100 MHz IF for spread-spectrum receivers, we recognize a few important attributes. Due to the wide bandwidth of the input signal and limited circuit speed, delta-sigma converters can afford only low oversampling ratios, which makes high-resolution conversion difficult. The low oversampling ratio generally nullifies the primary advantage of delta-sigma converters; the tolerance to component mismatches. As for quantization noise in pipeline converters, the quantization noise can be made smaller by adding more stages at the end of the pipeline. Since the last stages of the pipeline do not contribute much thermal noise, they can be made extremely small and low power. Therefore, the quantization noise itself can be made arbitrarily small with negligible increase of area and power. Certainly, doing so will not improve the accuracy or thermal noise. However, it is no different in delta-sigma converters with low oversampling ratios.

Based on the above observation, we can conclude that delta-sigma converters do not possess any fundamental advantage over pipeline converters for wide-band applications that necessitate low oversampling ratios. At these low oversampling ratios the benefits of delta-sigma modulation disappear. Two delta-sigma designs have been reported at oversampling ratios of 4 to 8 [32] [33]. In [32] a 12-bit pipeline A/D converter is employed in the back-end of a 2nd order delta-sigma converter with 5-bit truncated feedback. Dynamic element matching is used to linearize the feedback DAC. This converter reportedly achieved 89dB SNR with the oversampling ratio of 8, and a 82dB SNR at an oversampling ratio of 4. The design of [33] is based on a 2-1-1 cascaded delta-sigma modulator. 4-bit quantizers are employed in every stage and use a variant of data weighted averaging to enhance the linearity. 90dB SNR is reported at an oversampling ratio of 8.

Although the design of these delta-sigma converters is complex, the complexity can perhaps be reduced if lower SNR figures are desired by simply reducing the number of bits in the DAC. However, the number of bits cannot be reduced to 1, where no dynamic element matching would be needed, because quantizer overload would become unavoidable resulting in significant integral nonlinearity [5].

We believe that a more efficient approach would be to oversample a pipeline converter, and shape the mismatch distortion out of band, where it will be removed by a subsequent digital filter. Since no attempt is made to shape the quantization noise, there are none of the concerns associated with delta-sigma converters with a low oversampling ratio.

In addition to simplicity, a pipeline design offers some interesting advantages from a system design perspective. First, a pipeline design can be easily reconfigured to perform Nyquist conversion in addition to the oversampled conversion it performs at improved SNDR. It will be shown in the next chapter that oversampled bandpass operation can also be realized at improved resolution. All of this is accomplished with the same hardware. Delta-sigma converters cannot achieve this without significant complications. Second, pipeline converters offer a very simple way to save power under operating conditions where the full resolution is not needed, through the powering down of unneeded stages [34]. In a 1-bit-per-stage implementation, the granularity of this power-resolution control is very fine, allowing for great flexibility in system optimization. Finally, since the pipeline converter is fundamentally a memoryless system, it can be easily multiplexed. This allows for the same ADC to digitize multiple input channels, while oversampling and mismatch shaping each one of them.

1.2 Thesis Organization

Chapter 2 introduces many different mismatch shaping algorithms for pipeline ADCs. It presents the circuit implementation and simulation results. It also presents theoretical analysis which predicts the behavior and provides insights into techniques to improve the performance. Chapter 3 describes the design of a test-chip which was built as a vehicle to test the different mismatch shaping algorithms. The experimental results from this test-chip are presented in chapter 4. This chapter also probes these results to highlight the advantages and practical limitations of the different mismatch shaping techniques. Chapter 5 concludes this work and outlines possible directions for further research.

Chapter 2

Mismatch Shaping in Pipeline A/D Converters

Mismatch shaping improves the linearity of oversampled converters by pushing the distortion introduced by component mismatch out of the input signal frequency band. This chapter will explore different techniques to implement mismatch shaping in pipeline converters. It will show how mismatch shaping can be realized in traditional 1-bit-per-stage pipeline ADCs. This implementation does suffer from some fundamental limitations, which limit its effectiveness at pushing the distortion out of band. These limitations can be alleviated by using a 1-bit/stage commutative feedback capacitor switching (CFCS) pipeline design, due to the properties of the CFCS ADC's transfer characteristic, which has reduced differential nonlinearity (DNL) and an even integral nonlinearity (INL). The CFCS converter offers the foundation for the implementation of many different algorithms for mismatch shaping, some with very simple circuit realizations. It is possible to generalize some of these ideas to multi-bit-per-stage pipelines, but with reduced effectiveness. It will also be shown how the distortion spectrum can be shaped in a bandpass converter.

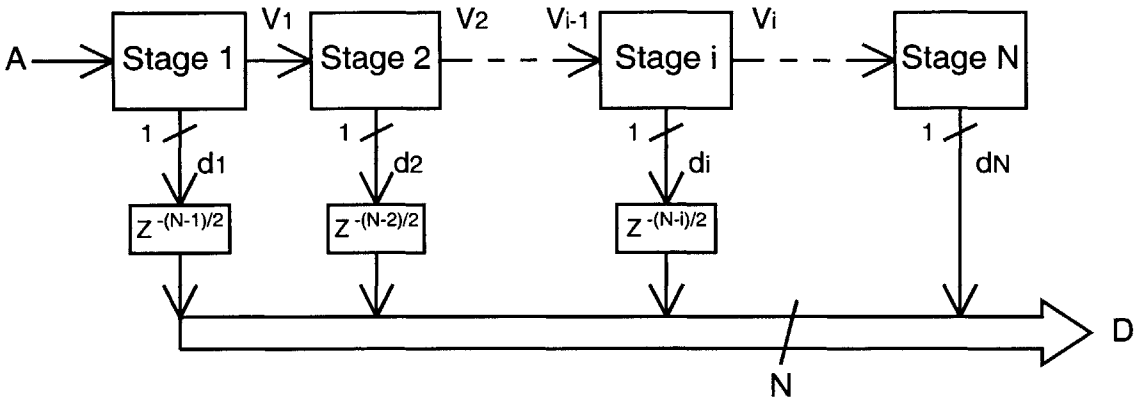


Figure 2-1: 1-Bit/stage Pipeline A/D Converter.

2.1 Mismatch Shaping in Traditional 1-bit/stage Pipeline Converters

A 1-bit-per-stage pipeline converter with a resolution of N bits is composed of a cascade of N stages, as shown in fig. 2-1. Each stage contributes a single bit to the digital output by implementing a simple algorithm. The implementation of the i-th stage is shown in fig. 2-2. The capacitors C_1 and C_2 are nominally identical. Each converter operates in two phases; a sampling phase and a multiplying phase. During the sampling phase shown in fig. 2-2(a), both C_1 and C_2 sample the input voltage to the stage $V_{i-1}[n]$. At the same time, the comparator determines whether the input voltage $V_{i-1}[n]$ is greater than or less than 0V.

If $V_{i-1}[n] > 0$, then the stage decision bit $d_i[n] = 1$, otherwise $d_i[n] = 0$. During the second phase which is the amplifying phase, C_1 is connected to the output of the operational amplifier, and C_2 is connected to either the reference voltage V_{REF} or $-V_{REF}$ depending on the bit value $d_i[n]$. If $d_i[n] = 1$, C_2 is connected to V_{REF}, resulting in an output voltage

$$V_i[n] = 2V_{i-1}[n] - V_{REF} \tag{2.1}$$

Otherwise, C_2 is connected to $-V_{REF}$, giving an output voltage

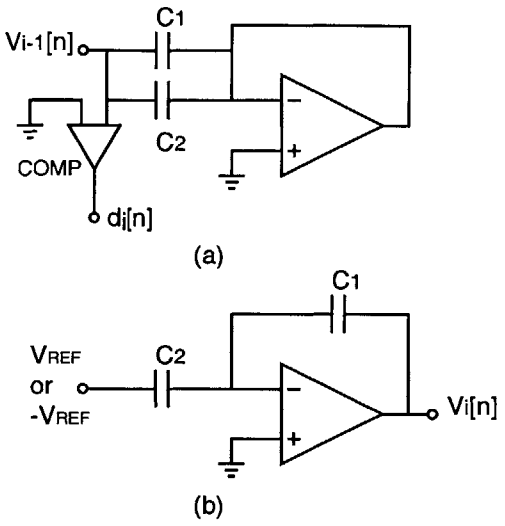


Figure 2-2: The i-th stage of a 1-Bit/stage Pipeline A/D Converter.

$$V_i[n] = 2V_{i-1}[n] + V_{REF} \tag{2.2}$$

In other words,

$$V_i[n] = 2V_{i-1}[n] + (-1)^{d_i[n]}V_{REF} \tag{2.3}$$

N similar stages can be cascaded to construct an N-bit pipeline A/D converter. After each stage samples and holds (S&H) its input V_{i-1}, it then generates a 1-bit coarse estimate d_i of the input V_{i-1} using a 1-bit ADC. This estimate d_i is converted into an analog signal using a DAC and subtracted from the stage input, to generate an output which represents the deviation of the estimate from the stage input. The subtracter also does a multiply by 2 to make the possible values for the stage input and output cover the same range.

Since each stage samples and holds its input, the digital outputs of the pipeline stages due to an input sample $A[n]$, get misaligned in time. The delay elements in the bottom of fig. 2-1 realign the bits to construct the digital output $D[n]$.

In practice, a number of sources introduce errors in the conversion [35, 22]. They include the charge injection from the sampling switch, the comparator offset, and the mismatch between C_1 and C_2. We assume here the open-loop gain of the operational amplifier is sufficiently large. By employing the standard digital error correction, the comparator offset can be easily compensated [36]. The effect of charge injection can be substantially reduced by a fully-differential configuration. The residual charge injection causes only a benign input referred offset of the converter with digital error correction. The effect of capacitor mismatch, however, is much more difficult to remove. If we define

$$C = \frac{C_1 + C_2}{2} \tag{2.4}$$

and

$$\Delta = \frac{C_1 - C_2}{C} \tag{2.5}$$

then

$$C_1 = C(1 + \frac{\Delta}{2}) \tag{2.6}$$

and

$$C_2 = C(1 - \frac{\Delta}{2}) \tag{2.7}$$

The resulting output voltage $V_i[n]$ can be shown to be:

$$V_i[n] = 2(1 + \frac{\Delta}{2})V_{i-1}[n] + (-1)^{d_i[n]}(1 - \Delta)V_{REF} \tag{2.8}$$

In order to consider the effect of the capacitor mismatch on the converter characteristic, assume that only the first stage of the pipeline has the capacitor mismatch Δ, and all subsequent stages have perfect matching. From equation 2.8 we can relate the first stage output $V_1[n]$ to the ADC input $A[n]$:

$$V_1[n] = 2(1 + \frac{\Delta}{2})A[n] + (-1)^{d_1[n]}(1 - \Delta)V_{REF} \tag{2.9}$$

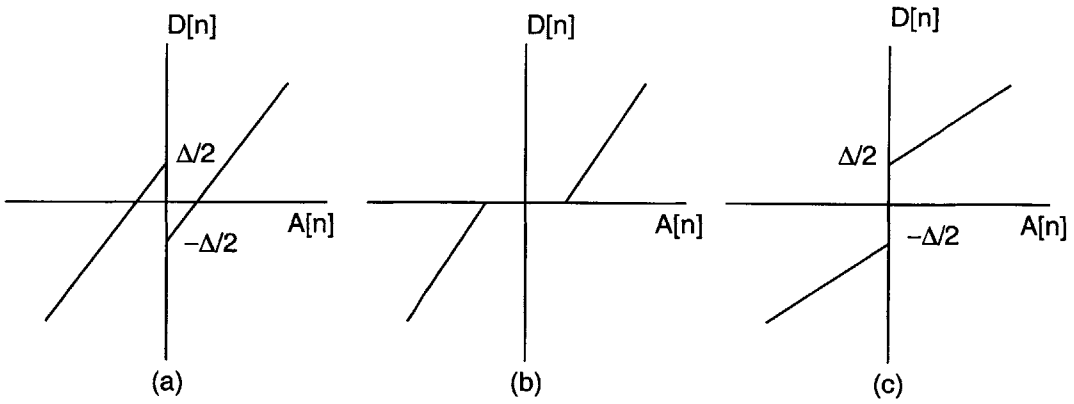


Figure 2-3: Effects of the First Stage Capacitor Mismatch. a) $\Delta > 0$, b) $\Delta < 0$ and c) $\Delta > 0$ and no digital error correction results in a wide code.

The input referred converter characteristic can be found by subtracting $(-1)^{d_1[n]}V_{REF}$ from the first stage output and dividing the result by 2. This compensates for the effect of the first stage and if digital error correction is employed in the subsequent stages, it gives the converter transfer characteristic:

$$D[n] = \begin{cases} A[n](1+\frac{\Delta}{2}) - V_{REF}\frac{\Delta}{2} & \text{if } A[n] > 0 \\ A[n](1+\frac{\Delta}{2}) + V_{REF}\frac{\Delta}{2} & \text{otherwise} \end{cases}$$

where $A[n]$ and $D[n]$ are the converter input and output respectively. The resulting converter characteristic is indicated in fig. 2-3 for $V_{REF} = 1$. The non-monotonicity near the center of the characteristic in fig. 2-3(a) for $\Delta > 0$ arises if digital error correction is employed in the subsequent stages. Otherwise, a 'wide code' will result as shown in fig. 2-3(b). When $\Delta < 0$ then missing codes result as shown in fig. 2-3(c).

2.1.1 Rudimentary Mismatch Shaping

As rudimentary mismatch shaping, one can exchange the roles of C_1 and C_2 at the sampling rate. In other words, for one sample of the input, C_1 and C_2 are operated as shown in fig. 2-

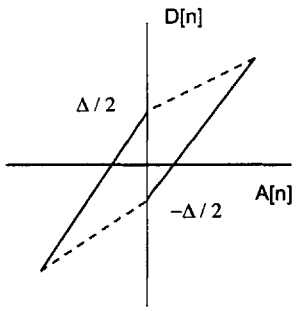


Figure 2-4: Mismatch shaping applied to a 1-bit-per-stage pipeline ADC results in the alternating between the two transfer characteristics.

2. For the next sample, C_2 is employed as the feedback capacitor while C_1 is connected to V_{REF} or $-V_{REF}$. The converter characteristic will alternate at the sampling frequency between that in fig. 2-3(a) and fig. 2-3(c), as shown in fig. 2-4, if digital error correction is employed. We see that although the amplitude of the error introduced into each sample is the same as before, the polarity of the error now alternates. The error introduced to the input manifests itself as distortion, and mismatch shaping has simply multiplied the distortion by $(-1)^n$, and hence modulated it to half the sampling frequency. If the analog input is DC, the error is indeed at half the sampling rate and can be removed completely by a digital low pass filter. Since the mismatch shaping is to be applied to oversampled converters, the input does not change very rapidly from one sample to another, and we can reason that most of the distortion will be pushed out to high frequencies. However, a close examination of the converter characteristic reveals the problem with such a method. Suppose the input is changing slowly near 0, and the first sample was just below 0 and the next just above 0. In both cases, if the role of C_1 and C_2 are swapped between the two samples, both samples will have $+\Delta$ as their error which add up rather than cancel each other. Although this error happens at the particular point of the converter input and will be averaged out over many samples, the reduction of the error by averaging will be small if the oversampling ratio is small.

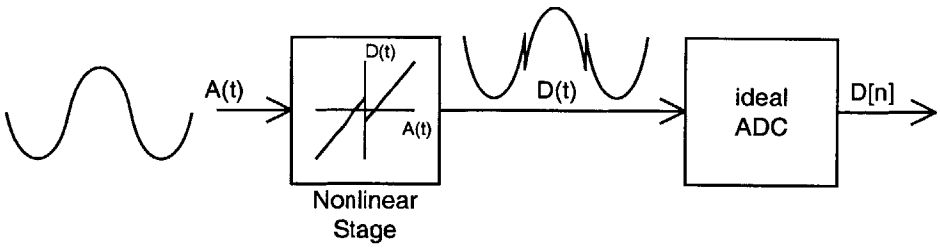


Figure 2-5: Converter model used for distortion analysis.

2.1.2 Performance Analysis

To get a quantitative estimate of the performance of this mismatch shaping technique, let us assume that the input to the ADC is a single tone $A(t) = A\,cos(\omega_o t)$. Furthermore let us assume that the capacitors mismatch only in the first pipeline stage, resulting in the transfer characteristics of fig. 2-4. To calculate the distortion spectrum that will result when no mismatch shaping is applied, we can assume that the input first goes through a continuous time nonlinear stage which models the ADC nonlinearity, followed by an ideal ADC as shown in fig. 2-5. The output of the nonlinearity $D(t)$, which is sketched in fig. 2-5, can be decomposed into the sum of a sinusoid and a square wave with a peak to peak amplitude of Δ, as illustrated in fig. 2-6. A Fourier series expansion of the square wave reveals that it has frequency components at odd multiples of the input frequency, each with an amplitude equal to $A_i = \frac{2\Delta}{\pi i}$, where i is an odd integer representing the harmonic number. The spectrum of $D(t)$ therefore contains distortion components which fall as $\frac{1}{i}$ as shown in fig. 2-7. When $D(t)$ is digitized by the ideal ADC, the distortion components in $D(t)$, which are at frequencies above half the sampling frequency, fold back into the frequency band from 0 to half the sampling frequency. This is illustrated in fig. 2-8(a), which shows the simulated output spectrum for a 15-bit converter with 0.1% mismatch in the first stage and a full scale input. The dominant harmonics in this spectrum fall as $\frac{1}{i}$.

When mismatch shaping is applied the distortion is modulated to half the sampling frequency as shown in fig. 2-8. Since the oversampling ratio is low and the dominant distortion components only fall of as $\frac{1}{i}$, strong distortion components alias back into the

Figure 2-6: The converter nonlinearity output decomposition.

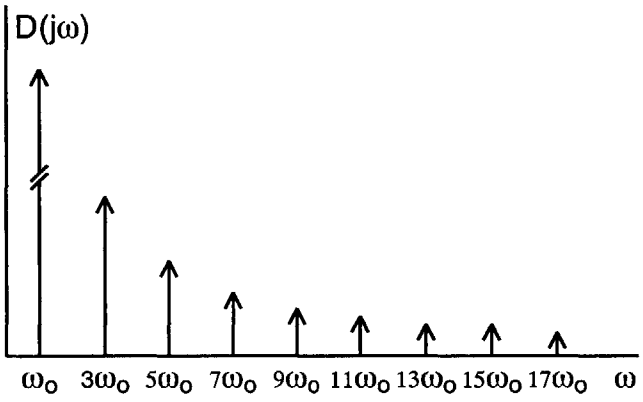
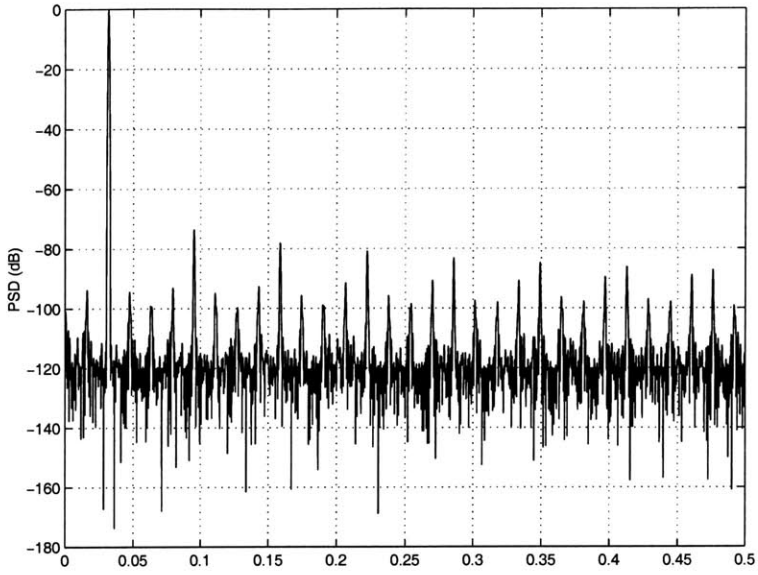


Figure 2-7: The spectrum of $D(t)$.

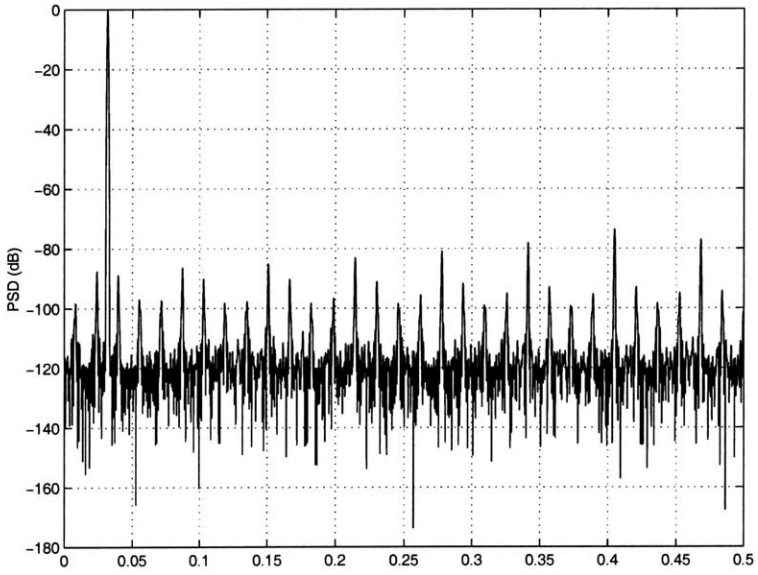
signal band. For example, at an oversampling ratio of 4 the worst case scenario is when the input is a single input tone at the edge of the signal band. This results in the 5th harmonic falling in the signal band and the improvement in the spurious free dynamic range (SFDR) due to mismatch shaping is only 4.4dB. At an oversampling ratio of 8, the worst case results in the 9th harmonic falling in-band which leads to a 9.5dB improvement in SFDR.

2.2 Mismatch Shaping Using the CFCS Pipeline ADC

To improve the performance of the mismatch shaping technique described in the last section it is desirable to use an ADC which will introduce distortion components that fall faster than $\frac{1}{i}$. To help towards that goal, one can try to eliminate jump discontinuities in the transfer characteristic of the converter to make it smooth. A possible converter characteristic is shown in fig. 2-9. The converter characteristic is swapped between the solid line and the dotted line at the sampling rate as before. In this case, if the input is changing slowly near 0, the errors in two successive samples just below and above 0 now cancel each other. The



(a)



(b)

Figure 2-8: The simulated power spectral density of the output of a traditional 1-bit/stage 15bit pipeline ADC with 0.1% mismatch in the first stage a) without mismatch shaping b) with mismatch shaping.

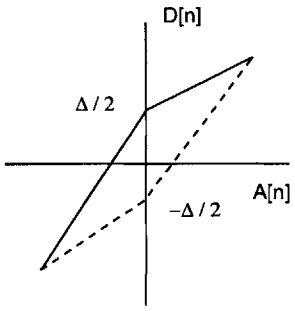


Figure 2-9: Candidate smooth converter characteristic with no DNL errors.

converter characteristic in fig. 2-11 can be obtained by the commutative feedback capacitor scheme (CFCS) in [30, 37]. CFCS is implemented by slightly altering the basic operation of the standard converter shown in fig. 2-2. Instead of designating C_1 as the feedback capacitor, either C_1 or C_2 is selected as the feedback capacitor while the other capacitor is connected to V_{REF} or $-V_{REF}$ depending on the bit value $d[n]$. The sampling phase shown in fig. 2-10(a) is unchanged. For $d[n] = 1$, the operation is the same as in fig. 2-2, with C_1 being selected as the feedback capacitor. For $d[n] = 0$, however, C_2 is selected as the feedback capacitor as shown in fig. 2-10(c). It is shown in [30] that this operation gives the characteristic in fig. 2-11 despite capacitor mismatches. The dotted characteristic in fig. 2-11 with the errors in the opposite direction can be obtained by reversing the roles of C_1 and C_2; For $d[n] = 1$, C_2 is selected as the feedback capacitor, and for $d[n] = 0$, C_1 is selected as the feedback capacitor. Alternating between these two characteristics at the sampling rate pushes the mismatch error to high frequencies. This will be studied further later in this section.

2.2.1 Properties of the Transfer Characteristic of a 1-bit/Stage CFCS ADC

In addition to the reduced differential nonlinearity (DNL) [30, 37], the 1-bit-per-stage CFCS ADC has a transfer characteristic with a nonlinear portion which is even. That is the integral nonlinearity (INL) is even. To demonstrate this property we will analyze

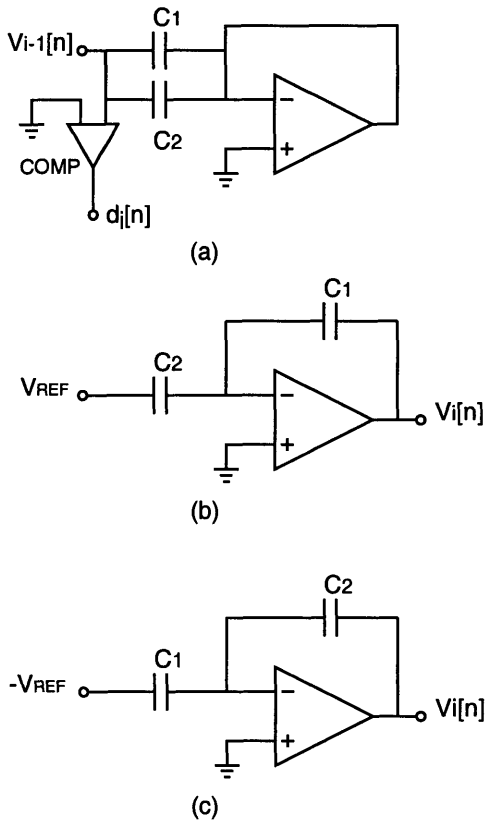


Figure 2-10: Commutative Feedback Capacitor Scheme (CFCS).

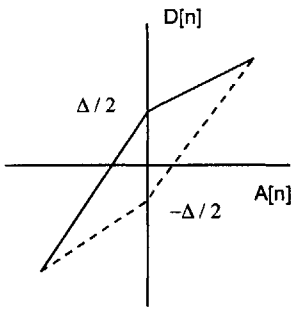


Figure 2-11: CFCS converter transfer characteristic with Δ mismatch only in the first stage.

the circuit in fig. 2-10. During the sampling phase the bottom plate of the nominally equal capacitors C_1 and C_2 sample the input, while the opamp is placed in a unity gain configuration, as shown in fig. 2-10(a). In the next phase, if the input is greater than zero then C_1 is connected as a feedback capacitor and C_2 is connected to V_{REF}, as shown in fig. 2-10(b). The output of the stage in this case is:

$$V_i[n] = \frac{C_1 + C_2}{C_1} V_{i-1}[n] - \frac{C_2}{C_1} V_{REF} \tag{2.10}$$

On the other hand, if the input is less than zero then C_2 is connected as a feedback capacitor and C_1 is connected to $-V_{REF}$ as shown in fig. 2-10(c), and the output of the stage is:

$$V_i[n] = \frac{C_1 + C_2}{C_2} V_{i-1}[n] + \frac{C_1}{C_2} V_{REF} \tag{2.11}$$

If we assume capacitor mismatch only in the first stage of the pipeline as follows:

$$C = \frac{C_1 + C_2}{2} \tag{2.12}$$

and

$$\Delta = \frac{C_1 - C_2}{C} \tag{2.13}$$

then

$$C_1 = C(1 + \frac{\Delta}{2}) \tag{2.14}$$

and

$$C_2 = C(1 - \frac{\Delta}{2}) \tag{2.15}$$

the transfer characteristic of the converter will be as shown in fig. 2-11 and will equal:

$$D[n] \approx \begin{cases} A[n](1 - \frac{\Delta}{2}) + V_{REF}\frac{\Delta}{2} & \text{if } A[n] > 0 \\ A[n](1 + \frac{\Delta}{2}) + V_{REF}\frac{\Delta}{2} & \text{otherwise} \end{cases}$$

Separating the linear and nonlinear parts gives:

$$D[n] \approx A[n] + V_{REF}\frac{\Delta}{2} - |A[n]|\frac{\Delta}{2} \tag{2.16}$$

The nonlinear part is the absolute value function and is an even function.

When the first two stages of the pipeline suffer from capacitor mismatch, each linear segment of fig. 2-11 will be replaced by a segment with the overall shape of fig. 2-11, resulting in the transfer characteristic shown in fig. 2-12, where the nonlinearity is exaggerated for illustration purposes. The effect of mismatch in the remain stages of the pipeline can be found by repeating this process for each linear segment. Due to the even symmetry of this replacement process, the nonlinear portion of the converter transfer characteristic maintains an even symmetry, even with capacitor mismatch in all the ADC stages. The dashed line in fig. 2-12 can be achieved by reversing the role of C_1 and C_2 in the second pipeline stage. If the role of C_1 and C_2 are also reversed in the first pipeline stage then 2 additional transfer characteristics are realizable as shown if fig. 2-13, bring the number of achievable characteristics to 4. If the role of the capacitors in the 3rd pipeline stage is also allowed to be reversed then the number of realizable characteristics will be 8. This ability to influence the transfer characteristic will be exploited later on in this chapter in implementing different mismatch shaping techniques.

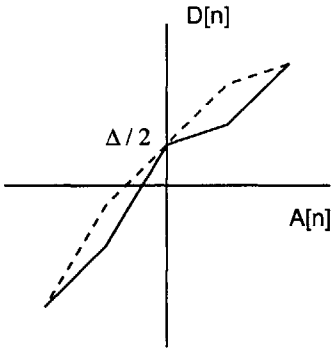


Figure 2-12: The effect of capacitor mismatch in the first two stages of a pipeline on the input-output characteristic of a CFCS converter.

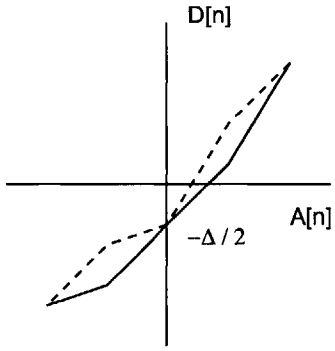


Figure 2-13: Reversing the role of C_1 and C_2 in the first two pipeline stages allows for the realization of 4 different transfer characteristics.

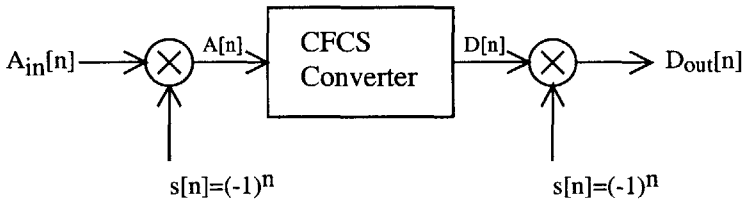


Figure 2-14: Simple implementation of mismatch shaping using a 1-bit-per-stage CFCS ADC.

2.2.2 A Simple Implementation of Mismatch Shaping Using a CFCS ADC

A simple implementation of mismatch shaping using a CFCS ADC is shown in fig. 2-14. If the input to the CFCS is multiplied by -1 at alternating sampling phases, and its digital output is also multiplied by -1 during those phases as shown in fig. 2-14, then the converter characteristics simply alternates between the characteristics in fig. 2-11, at a rate equal to the sampling frequency, and mismatch shaping is realized. To understand this, let us analyze the implementation in fig. 2-14. The CFCS converter characteristic can be expressed as:

$$D[n] = A[n] + N_w[n] + N_{1/f}[n] + g(A[n]) \tag{2.17}$$

Where $A[n]$ and $D[n]$ are the input and output of the CFCS ADC. $N_w[n]$ is the ADC white noise, which includes quantization and thermal noise. $N_{1/f}$ is the converter $1/f$ noise. The function $g(.)$ models the nonlinearity of the ADC, which is a result of the capacitor mismatch in the stages of the pipeline. The CFCS ensures that $g(.)$ does not contain any large discontinuities which would result in a differential nonlinearity. In addition, it ensures that $g(.)$ is an even function. This feature is utilized in realizing mismatch shaping in the following manner:

- The input of the ADC $A_{in}[n]$ is multiplied by a sequence $s[n] = (-1)^n$, resulting in $A[n] = A_{in}[n]s[n]$.
- $A[n]$ is digitized by the CFCS core resulting in:

  $$D[n] = s[n]A_{in}[n] + N_w[n] + N_{1/f}[n] + g(A_{in}[n]) \tag{2.18}$$

  This result can be obtained by noting that $g(x_{in}s[n]) = g(x_{in})$, because $g(.)$ is an even order function.
- Finally, the output of the CFCS core is multiplied by the same sequence $s[n]$ giving:

  $$D_{out}[n] = A_{in}[n] + s[n]N_w[n] + s[n]N_{1/f}[n] + s[n]g(A_{in}[n]) \tag{2.19}$$

The first term in $D_{out}[n]$ is the desired signal $A_{in}[n]$. The second term, $s[n]N_w[n]$, is the quantization and thermal noise modulated to half the sampling frequency (π), an operation that does not change its white nature. The third term, $s[n]N_{1/f}[n]$, is the $1/f$ noise modulated to half the sampling frequency, and hence mismatch shaping removes the $1/f$ noise from the band of interest. The final term is the distortion components modulated to half the sampling frequency π.

From the above analysis it is evident that a CFCS core with its even INL is essential for this scheme to work. If a converter with odd INL is used then $g(x_{in}s[n]) = s[n]g(x_{in})$ and the converter output will be:

$$D_{out}[n] = A_{in}[n] + s[n]N_w[n] + s[n]N_{1/f}[n] + g(A_{in}[n]) \tag{2.20}$$

The distortion is $g(A_{in}[n])$ and is the same as the distortion when no mismatch shaping is applied. The input passes through the same characteristic during all sampling phases and the error is not pushed to higher frequencies.

In a fully differential implementation multiplying the input with -1 can be realized by swapping the polarity of the input applied to the CFCS stage, an operation which has a very simple circuit realization. The multiplication in the digital domain can also be realized very simply. Moreover, the implementation of the 1-bit-per-stage CFCS pipeline converter only requires a very slight modification of the standard pipeline stage comparator's logic, to give the even nonlinearity. It can be concluded therefore, that the circuit implementation of this technique only entails little added complexity. Although a digital low-pass filter is needed to remove the out-of-band distortion, this filter would serve the dual purpose of augmenting the function of the weak analog anti-aliasing filter.

2.2.3 Performance Analysis

We can analyze the distortion in the output of the CFCS converter using the model of fig. 2-15, in an approach similar to the one used in the last section. With a sinusoidal input $A(t) = Acos(\omega t)$ and no mismatch shaping the output of the nonlinearity, $D(t)$ can be

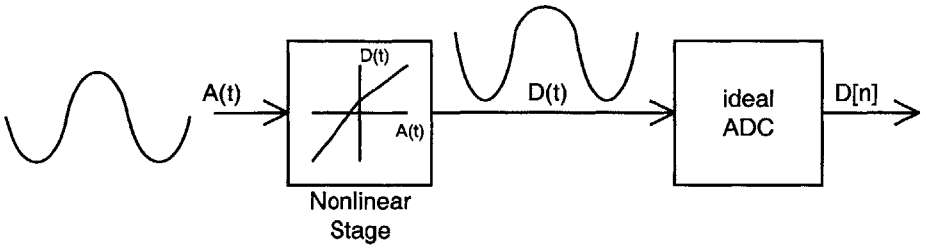
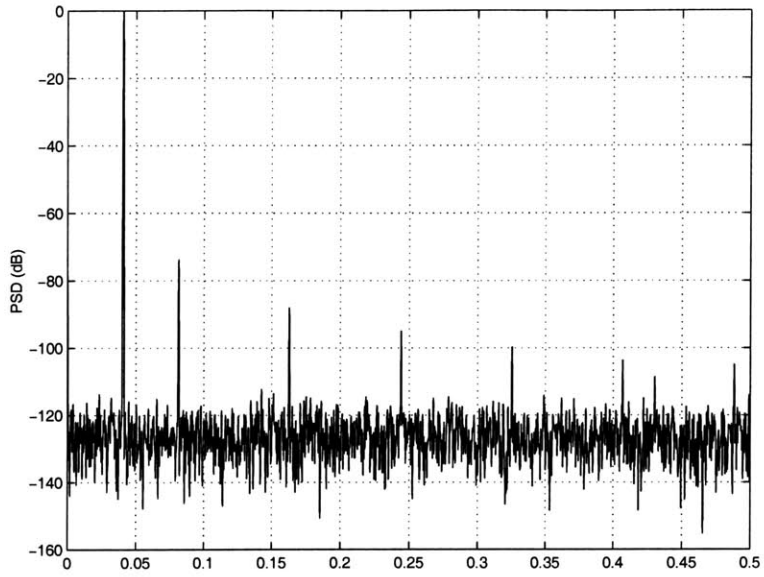


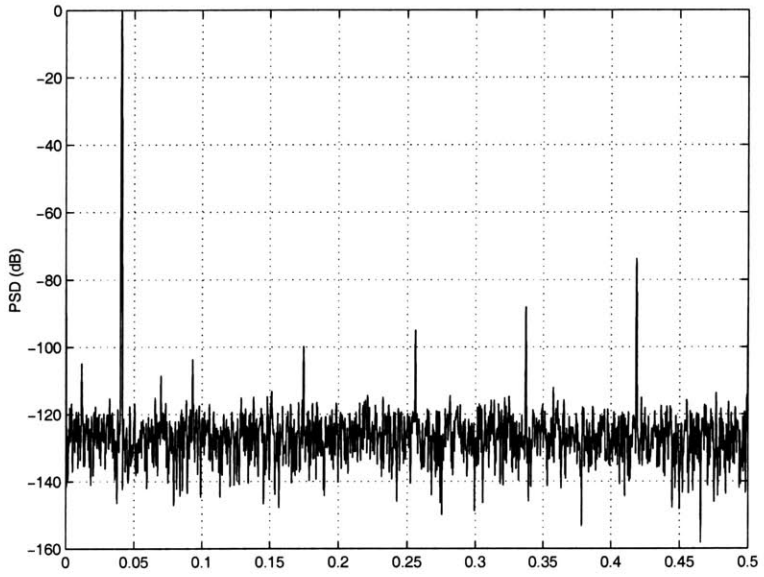
Figure 2-15: Converter model used for distortion analysis.

Figure 2-16: The converter nonlinearity output decomposition.

decomposed into a sinusoidal signal plus a full wave rectified sinusoidal with a peak value of Δ as shown in fig. 2-16. A Fourier series expansion of the full wave rectified sinusoid reveals that it contains even order distortion components with an amplitude $A_i = \frac{2\Delta A}{\pi(i^2-1)}$ where i is an even integer representing the harmonic number, and A is the amplitude of the input. The ideal ADC causes frequency folding as plotted in fig. 2-17(a) for a 15-bit CFCS ADC with 0.1% mismatch in the first stage and a full scale input. The dominant distortion components fall as $\frac{1}{i^2}$. When mismatch shaping is applied the distortion gets modulated to half the sampling frequency and since the harmonics fall as $\frac{1}{i^2}$, significant improvement in SFDR can be expected as can be seen in fig. 2-17(b). For example, at an oversampling ratio of 4, under the worst case scenario the 4th harmonic will alias in-band when mismatch shaping is used, yet this represents a 14dB improvement in SFDR over a non-mismatch shaped CFCS ADC. Moreover, this represents a 9.5dB improvement over a non-CFCS mismatch shaped pipeline converter operating at the same oversampling ratio.



(a)



(b)

Figure 2-17: The power spectral density of the output of a 15bit CFCS ADC with 0.1% mismatch in the first stage and a 1-bit/stage architecture a) without mismatch shaping b) with mismatch shaping.

2.2.4 Choice of Sequences for $s[n]$

To gain a further insight on how to improve the performance of the ADC, let us revisit equation 2.19:

$$D_{out}[n] = A_{in}[n] + s[n]N_w[n] + s[n]N_{1/f}[n] + s[n]g(A_{in}[n]) \tag{2.21}$$

Modulating the distortion components $g(A_{in}[n])$ to half the sampling frequency using $s[n] = (-1)^n$ does not eliminate discrete harmonic tones in the signal band, but it does reduce their amplitude, as was shown in the last subsection and as illustrated by fig. 2-17. To randomize the in-band harmonics, a random swapping sequence can be used instead of $s[n] = (-1)^n$. The power spectral density (PSD) of this sequence must satisfy a few requirements, in order to effectively eliminate tones and to simultaneously achieve mismatch shaping. Since the swapping sequence is multiplied by the distortion components due to the ADC nonlinearity $g(x_{in}[n])$, as shown in equation 2.19, in the frequency domain the spectrum of the swapping sequence $S_{ss}(e^{j\omega})$ is convolved with the spectrum of the distortion $S_{gg}(e^{j\omega})$. For the result of the convolution $(S_{ss}(e^{j\omega}) * S_{gg}(e^{j\omega}))$ to be spectrally shaped with most of its energy concentrated at half the sampling frequency and with a randomized in-band noise floor, it is desired for $S_{ss}(e^{j\omega})$ to have a single PSD lobe at half the sampling frequency. In addition, the PSD lobe of $S_{ss}(e^{j\omega})$ should be wide enough to spread the in-band distortion tones as shown in fig. 2-18(a), but not too broad, to prevent a rise in the in-band noise floor as shown in fig. 2-18(b). Ideally we would want a rectangular PSD with all the sequence energy in a band around half the sampling frequency, and with no energy at all outside that band. Such a sequence is unfortunately unrealizable practically.

A candidate sequence with many of the desired PSD properties is:

$$s[n] = (-1)^{n+B[n]} \tag{2.22}$$

where $B[n]$ is a discrete-time Bernoulli counting process; a process that increments with every Bernoulli success event [38]. We can write $B[n] = \sum_{i=0}^{n} b_i$, where b_i is an independent

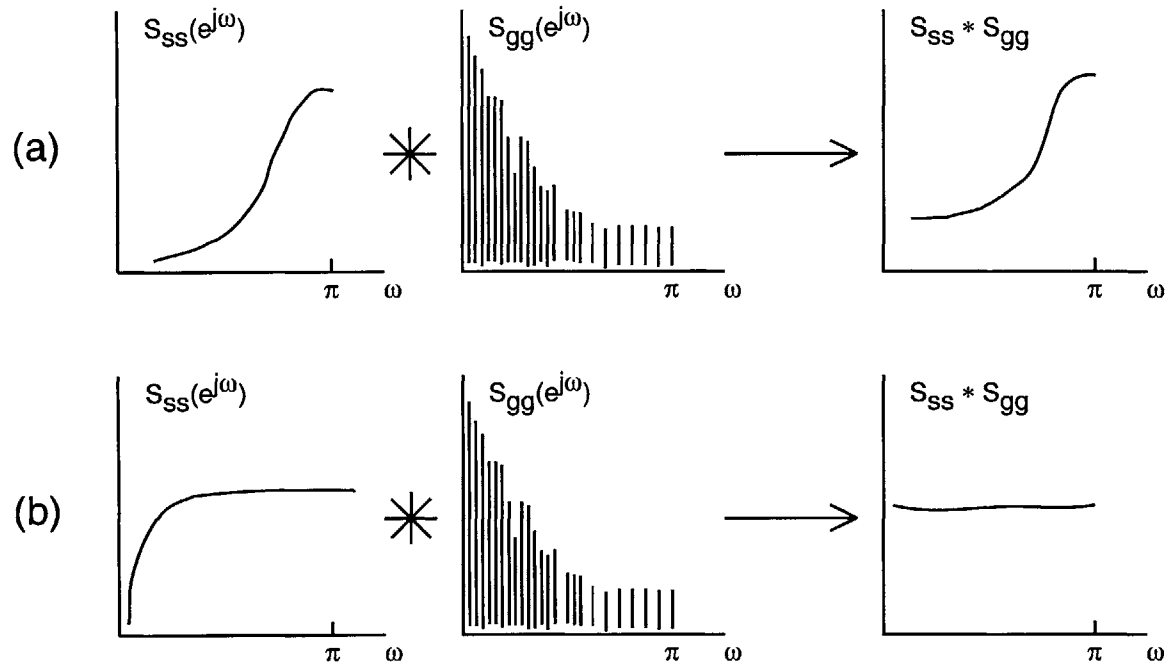


Figure 2-18: The PSD of the swapping sequence needs to have most of its energy concentrated at half the sampling frequency to effectively whiten the in-band tones and realize mismatch shaping.

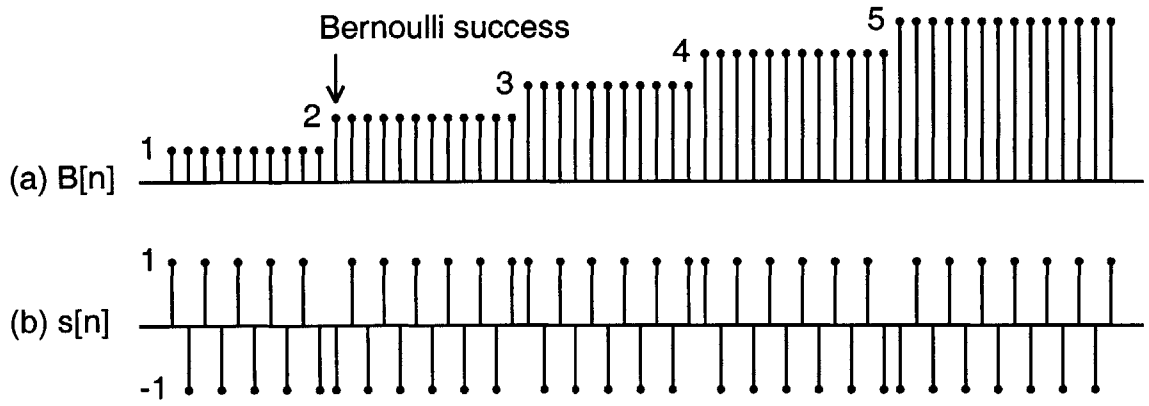


Figure 2-19: (a) A Bernoulli counting process increments at every Bernoulli success event (b) The swapping sequence has phase jumps at every Bernoulli counting process increment.

Bernoulli trial which equals 1 with probability α and zero with probability $1-\alpha$. In the time domain $s[n]$, shown in fig. 2-19(b), looks like a phase modulated alternating sequence, with 180^o phase jumps occurring at every Bernoulli success, shown in fig. 2-19(a). The autocorrelation function of the stochastic process $s[n]$ is:

$$\begin{aligned} R_{ss}[n,k] &= E\left[s[n]s[k]\right] \\ &= E\left[(-1)^{n+B[n]}(-1)^{k+B[k]}\right] \end{aligned} \tag{2.23}$$

Noting that $(-1)^{n+k} = (-1)^{|n-k|}$ and $(-1)^{B[n]+B[k]} = (-1)^{|B[n]-B[k]|}$, therefore:

$$\begin{aligned} R_{ss}[n,k] &= (-1)^{|n-k|}E\left[(-1)^{|B[n]-B[k]|}\right] \\ &= (-1)^{|n-k|}\left\{\Pr\left[|B[n]-B[k]| \text{ is even}\right] - \Pr\left[|B[n]-B[k]| \text{ is odd}\right]\right\} \end{aligned} \tag{2.24}$$

Now:

$$\Pr\left[|B[n]-B[k]| \text{ is even}\right] = \sum_{i \text{ odd}}^{|n-k|} \binom{|n-k|}{i} \alpha^i (1-\alpha)^{|n-k|-i} \tag{2.25}$$

and:

$$\Pr\left[|B[n]-B[k]| \text{ is odd}\right] = \sum_{j \text{ even}}^{|n-k|} \binom{|n-k|}{j} \alpha^j (1-\alpha)^{|n-k|-j} \tag{2.26}$$

which allows us to write:

$$R_{ss}[n,k] = (-1)^{|n-k|} \sum_{l}^{|n-k|} \binom{|n-k|}{l} \alpha^l (1-\alpha)^{|n-k|-l} \tag{2.27}$$

using the Binomial theorem [39]:

$$R_{ss}[n,k] = (-1)^{|n-k|}(1-2\alpha)^{|n-k|} \tag{2.28}$$

Since $R_{ss}[n,k]$ is a function of $|n-k|$, the stochastic process $s[n]$ is wide-sense stationary,

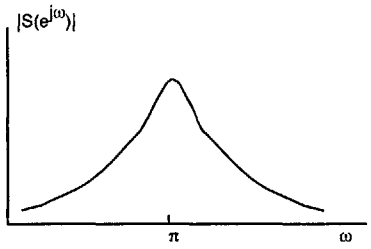


Figure 2-20: PSD of swapping sequence.

which allows us to write:

$$R_{ss}[m] = (-1)^{|m|}(1-2\alpha)^{|m|} \tag{2.29}$$

The power spectral density is the Fourier transform of the autocorrelation function and is:

$$\begin{aligned} S_{ss}(e^{-j\omega}) &= \sum_{m=-\infty}^{\infty} R_{ss}[m]e^{-j\omega n} \\ &= \frac{1}{1-(2\alpha-1)e^{-j\omega}} - \frac{1}{1-(2\alpha-1)^{-1}e^{-j\omega}} \\ &= \frac{\frac{(2\alpha-1)^2-1}{2\alpha-1}e^{-j\omega}}{[1-(2\alpha-1)e^{-j\omega}][1-(2\alpha-1)^{-1}e^{-j\omega}]} \end{aligned} \tag{2.30}$$

The PSD of this stochastic process decays as we move away from half the sampling frequency as illustrated in fig. 2-20 for $\alpha \in (0, 0.5)$. The rate of decay can be increased by reducing α which helps in reducing the energy of $s[n]$ at low frequencies, but results in a narrower PSD bandwidth. Conversely, attempting to increase the bandwidth of the PSD lob results in an increase of the energy at low frequencies. The value of α needs to be optimized to simultaneously satisfy these conflicting requirements.

The main shortcoming of using a noise shaped sequence is that it may degrade the ADC's signal to noise ratio. This degradation in performance can be understood by noting that one component of the ADC noise floor results from convolving the spectrum of the distortion with the spectrum of the swapping sequence. If the core ADC in fig. 2-14 produces

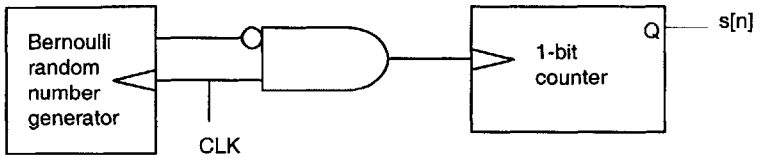


Figure 2-21: Generating the swapping sequence using a Bernoulli counting process.

strong distortion components even if they are primarily low order distortion components, the convolution will inevitably results in a rise in the total in-band noise floor. Simulation results will demonstrate this later in the section.

2.2.5 Generating the Noise Shaped Sequence $s[n]$

In the last section a Bernoulli counting process was used to generate the sequence $s[n]$. A hardware implementation of this idea is shown in fig. 2-21. The pseudo-random number generator produces an output which is 1 with probability α and 0 with probability $(1 - \alpha)$. This output is used to disable or enable the incrementing of a 1-bit counter. If the pseudo-random number generator output is 0, the counter is incremented, otherwise it isn't incremented causing a 180^o phase jump.

It is possible to generate the desired power spectral density using other methods. One possible implementation is shown in fig. 2-22. A white Gaussian number generator produces N_g, which is a sequence with independent samples of unit variance and a autocorrelation function $R_{N_g N_g}[m] = \delta[m]$. N_g is used to produce a spectrally shaped sequence $N_H[n]$ with PSD $|H(e^{j\omega})|^2$ using a filter with transfer function $H(e^{j\omega})$. The output of the filter goes through a hard limiter which quantizes the output value to ± 1, to obtain a 1-bit sequence $s[n]$. The autocorrelation function of the limiter output $R_{ss}[m]$ is related to $R_{N_H N_H}[m]$, the autocorrelation function of N_H, through [38]:

$$R_{ss}[m] = \frac{2}{\pi} \arcsin(R_{N_H N_H}[m]) \tag{2.31}$$

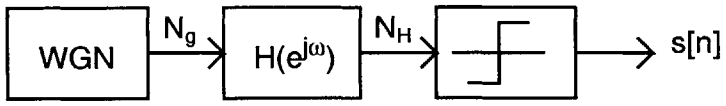


Figure 2-22: Generating the swapping sequence using a white Gaussian noise generator.

$R_{ss}[m]$ can be approximated using a Taylor series expansion as:

$$R_{ss}[m] = \frac{2}{\pi}(R_{N_H N_H}[m] + \frac{1}{6}R^3_{N_H N_H}[m] + \frac{3}{80}R^5_{N_H N_H}[m] + \cdots \tag{2.32}$$

The higher order terms in the Taylor series expansion cause spectral broadening, since multiplication in the time domain is a convolution in the frequency domain. The quantized sequence $s[n]$ will therefore have a broader spectrum than $N_H[n]$. Moreover, $s[n]$ will contain low frequency energy even if $N_H[n]$ does not (except in the limit case of $S_{ss}(e^{j\omega}) = \delta(\omega - \pi)$).

The white Gaussian number generator can be eliminated in this implementation by relying on the shaping of quantization noise in a delta sigma modulator with a multi-bit quantizer as shown in fig. 2-23. It is necessary to use a hard limiter after the delta sigma loop to quantize the output to ± 1. Attempting to use a 1-bit quantizer within the loop raises stability problems, by making the loop design equivalent to the a delta sigma loop with an oversampling ratio close to 1. To understand this consider fig. 2-24(a) which shows the distribution of poles and zeros for the quantization noise transfer function $H(e^{j\omega})$ in a traditional oversampling delta sigma modulator. The zeros are distributed in a band concentrated around low frequencies, while the poles are placed just outside that band, resulting in an immediate rise in the quantization noise, as shown in fig 2-24(b). This is however not desirable for the spectrum of $s[n]$, which must have most of its energy at half the sampling frequency, or equivalently, the oversampling ratio for the modulator must be very close to 1. Fig. 2-24(c) shows the pole-zero plot which would result in the desired spectrum of fig. 2-24(d). The transfer function from the quantization noise to the output in fig. 2-23 can be written as:

$$H(z^{-1}) = \frac{1}{1 - G(e^{j\omega})}$$

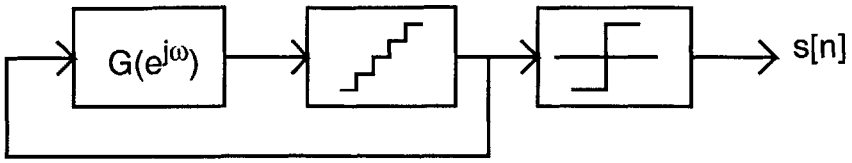


Figure 2-23: Generating the swapping sequence using a multi-bit Delta Sigma modulator.

$$= \frac{(1-a_1z^{-1})(1-a_2z^{-1})\cdots(1-a_kz^{-1})}{(1-b_1z^{-1})(1-b_2z^{-1})\cdots(1-b_kz^{-1})} \tag{2.33}$$

where a_1 through a_k are the transfer function zeros and b_1 through b_k are the poles. $G(e^{j\omega})$ is the loop filter in fig. 2-23. The transfer function $H(e^{j\omega})$ satisfies the condition $\lim_{z\to\infty} H(z^{-1}) = 1$, which is needed to make the first sample value of the quantization noise impulse response $h[0] = 1$ [40]. To insure the stability of a delta sigma loop, a common rule of thumb is that the out-of-band gain should be around 1.5, or $H(-1) \approx 1.5$ [11, 41]. For the pole-zero distribution of fig. 2-24(a) this condition can be met. However, for the pole-zero distribution of fig. 2-24(c) this condition will not be met since:

$$H(-1) = \frac{(1+a_1)(1+a_2)\cdots(1+a_k)}{(1+b_1)(1+b_2)\cdots(1+b_k)} \gg 1.5 \tag{2.34}$$

No stable loop design was found when a 1-bit quantizer was used. With a multi-bit quantizer, the loop designs were stabilized albeit with difficulty, sometimes with the help of dither.

The stability concerns in the design of the delta sigma loops can be mitigated by noting that the condition $h[0] = 1$ is placed because the output of the loop is the output of the multi-bit quantizer. If we take another point to be the loop output as shown in fig. 2-25, then the loop design becomes considerably easier. If we desire the loop to have a quantization noise transfer function $H(z^{-1}) = \frac{N(z^{-1})}{D(z^{-1})}$, this can be achieved easily by choosing:

$$H_1(z^{-1}) = \frac{D(z^{-1}) - 1}{N(z^{-1})} \tag{2.35}$$

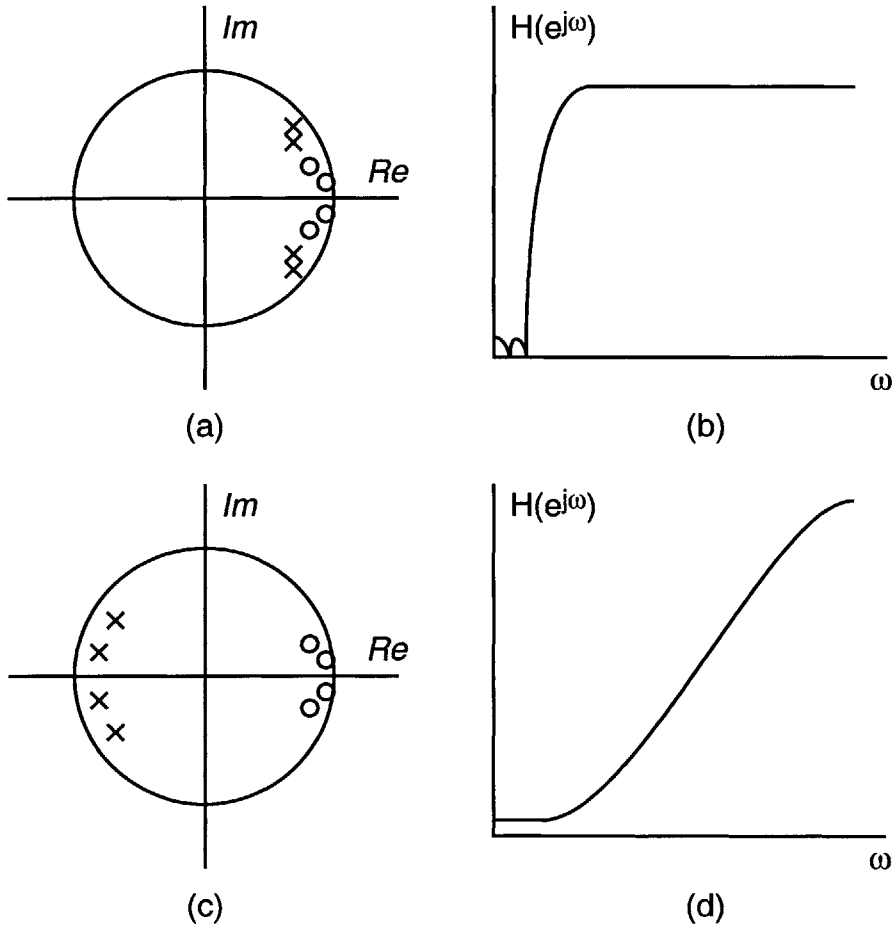


Figure 2-24: The quantization noise transfer function of a delta sigma converter (a) pole zero plot for high oversampling ratio converter (b) frequency response for high oversampling ratio converter (c) pole zero plot for low oversampling converter (d) frequency response for high oversampling ratio converter.

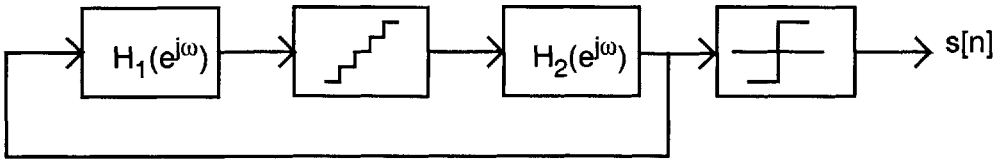


Figure 2-25: Generating the swapping sequence using a modified multi-bit Delta Sigma modulator.

and

$$H_2(z^{-1}) = N(z^{-1}) \tag{2.36}$$

$\frac{N(z^{-1})}{D(z^{-1})}$ can be synthesized using a filter design software package. Although $\frac{1}{N(z^{-1})}$ needs to be stable, this is not a difficult condition to meet. All that needs to be done is to make the quantization noise transfer function minimum phase.

2.2.6 Simulation Results

To demonstrate the previous mismatch shaping algorithms a MATLAB program was written to model the behavior of a 1-bit-per-stage CFCS pipeline converter. The model contains 15 pipeline stages. The first stage produces 1-bit, while the remaining stages produce 2-bits-per-stage to allow for digital error correction. The program can model the effect of capacitor mismatch, finite opamp gain and comparator offset.

To compare the performance of a mismatch shaped converter with a non-mismatch shaped converter, the ADC input must be selected carefully. If the comparison is done with a very low frequency input, then the mismatch shaped converter will have all of its distortion out of band, whereas the the distortion will all be in band for a non-mismatch shaped converter. On the other hand, if the input is placed at the edge of the signal band, then more lower order harmonics will fall in-band for a mismatch shaped converter as compared to a non-mismatch shaped converter. This would suggest that a fair comparison between the two cases can be made if the input contains two tones; one at a low frequency and the other at the edge of the signal band.

Fig. 2-26 shows the converter output spectrum when no mismatch shaping is applied

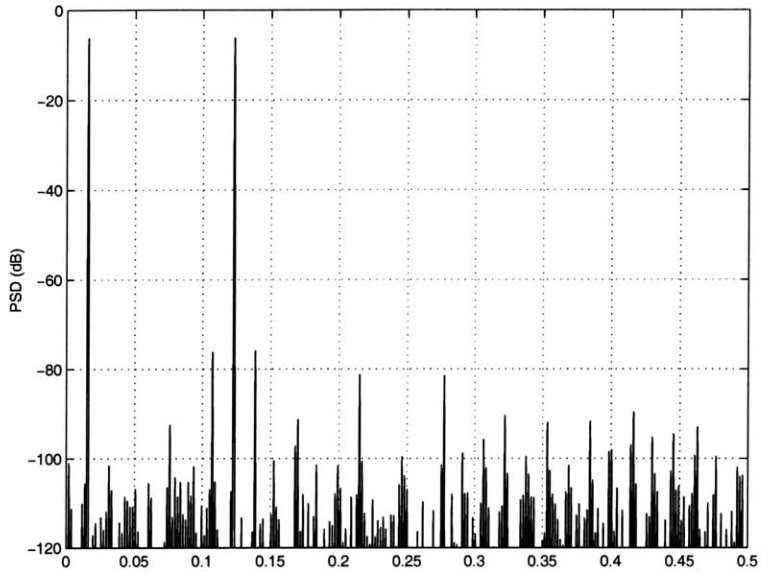
Algorithm	OSR=4 SNDR(dB)	OSR=4 SFDR(dB)	OSR=8 SNDR(dB)	OSR=8 SFDR(dB)
CFCS	72.8	70	72.8	70
$s[n] = (-1)^n$	80.8	84	91.1	94
$s[n]$ in fig. 2-29	79.6	97	86	103
3 swapping sequences	81	98	89.3	98

Table 2.1: Summary of simulated performance.

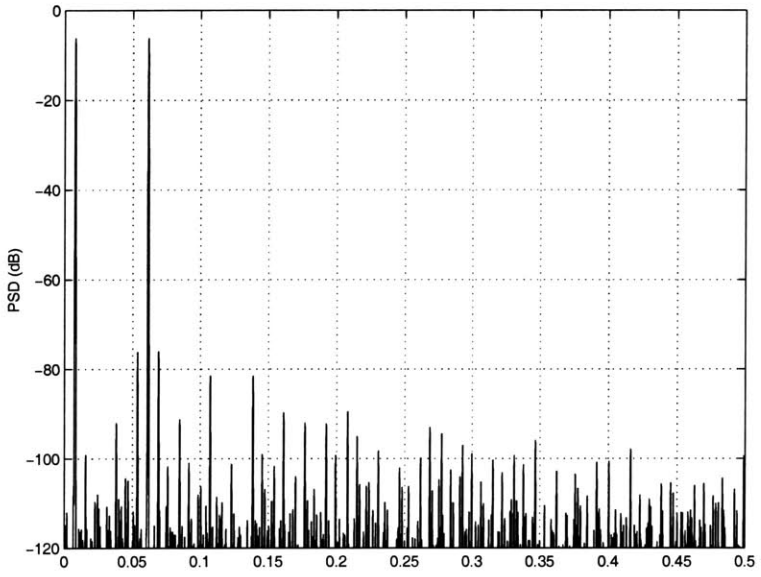
for an oversampling ratio of 4 and 8. Strong distortion components fall in-band limiting the SNDR to 72.8dB and the SFDR to 70dB for an oversampling ration (OSR) of 4. For an OSR=8 no improvement in performance is achieved and the SNDR=72.8dB and SFDR=70dB. When mismatch shaping is applied using a sequence $s[n] = (-1)^n$ the spectrums shown in fig. 2-27 result, and the distortion is modulated to half the sampling frequency, improving the SNDR to 80.8dB and the SFDR to 84dB for OSR=4. A SNDR=91.1dB and a SFDR=94dB are obtained by increasing the OSR to 8. When $s[n]$ is a noise shaped sequence with a PSD shown in fig. 2-29, then the output spectrum of fig. 2-28 results. The in-band distortion components are whitened and SFDR improves to 97dB and 103dB for oversampling ratios of 4 and 8 respectively. The overall noise floor does rise in this case as anticipated resulting in a SNDR of 79.6dB for OSR=4, and an SNDR of 86dB for OSR=8. All these results were obtained with 0.1% capacitor mismatch in all the pipeline stages. Moreover, the polarity of the mismatch error in each stage was selected to give the worst case performance. The results are summarized in table 2.1.

2.2.7 Impact of Non-idealities

The techniques presented in this section hinge on the even nature of the INL characteristic of the 1-bit/stage CFCS converter, which is the result of capacitor mismatch. Practically, the INL will also contain a small amount of odd terms due to effects such as finite opamp gain, input dependent charge injection and incomplete settling. The distortion introduced

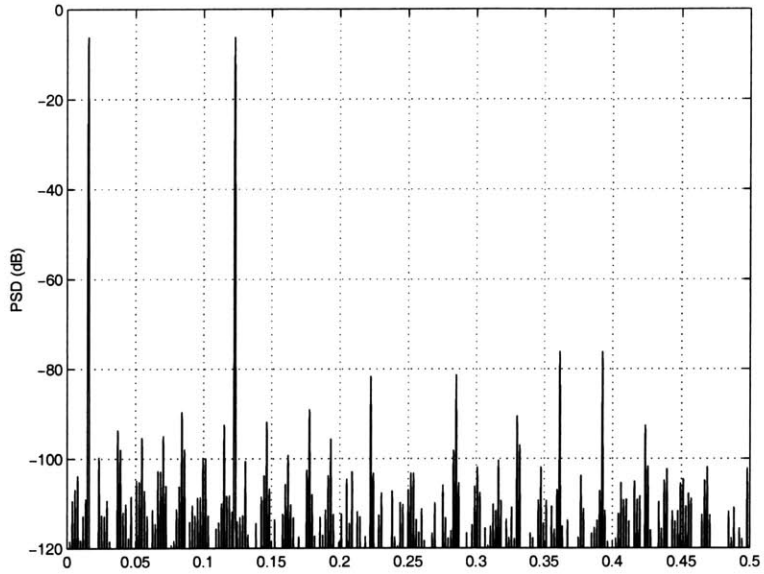


(a)

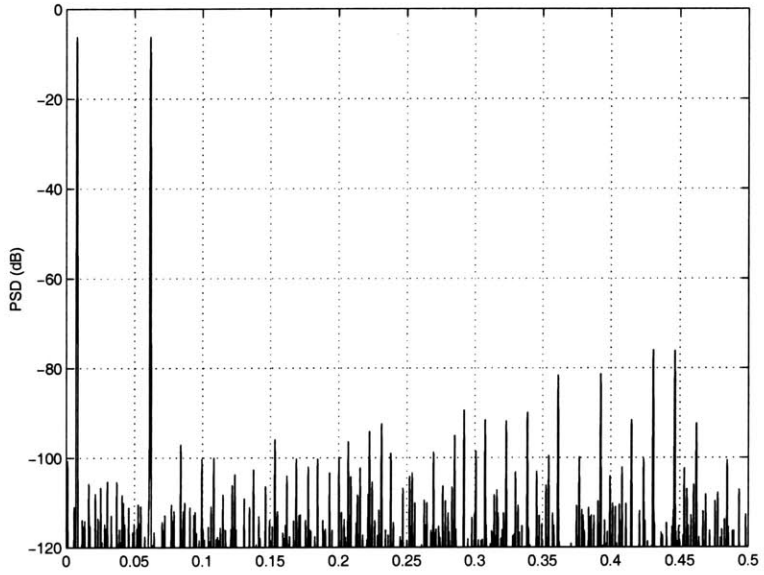


(b)

Figure 2-26: The PSD of the output of a 15bit CFCS ADC with 0.1% mismatch in all pipeline stages without mismatch shaping a) OSR=4 b) OSR=8.

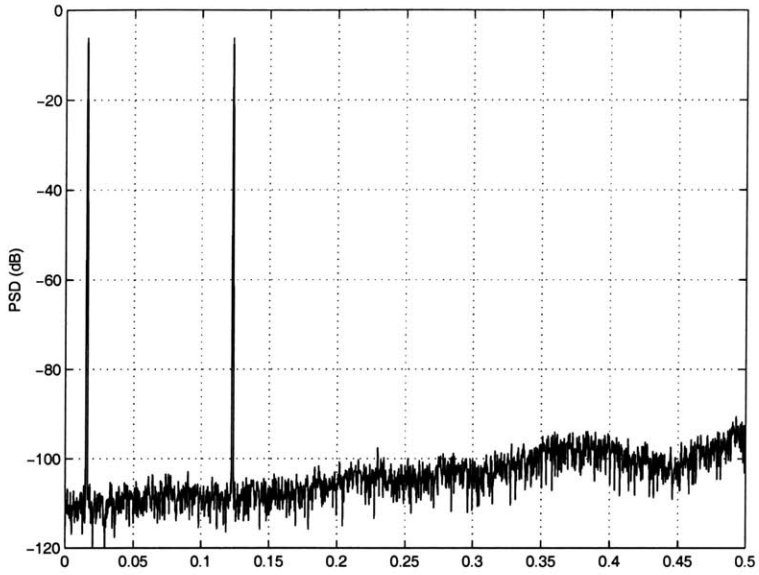


(a)

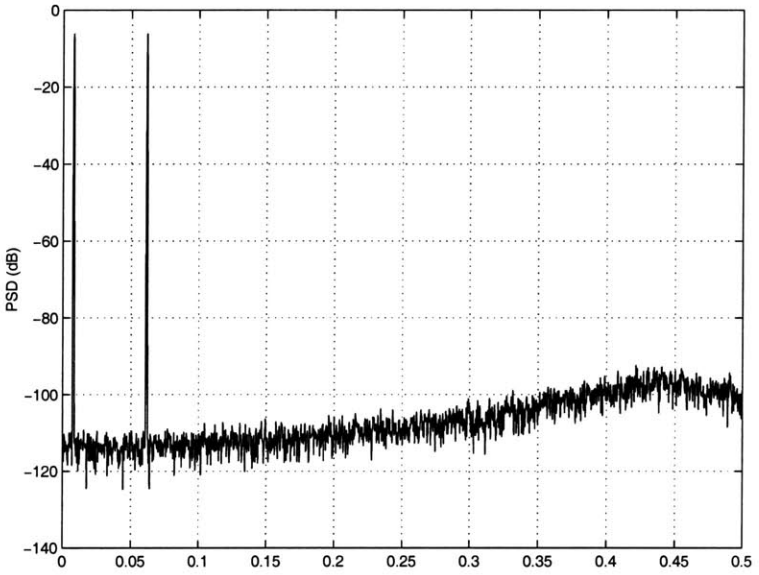


(b)

Figure 2-27: The PSD of the output of a 15bit CFCS ADC with 0.1% mismatch in all pipeline stages with mismatch shaping using $s[n] = (-1)^n$ a) OSR=4 b) OSR=8.



(a)



(b)

Figure 2-28: The PSD of the output of a 15bit CFCS ADC with 0.1% mismatch in all pipeline stages with mismatch shaping and $s[n]$ is a noise shaped sequence in fig. 2-29 a) OSR=4 b) OSR=8.

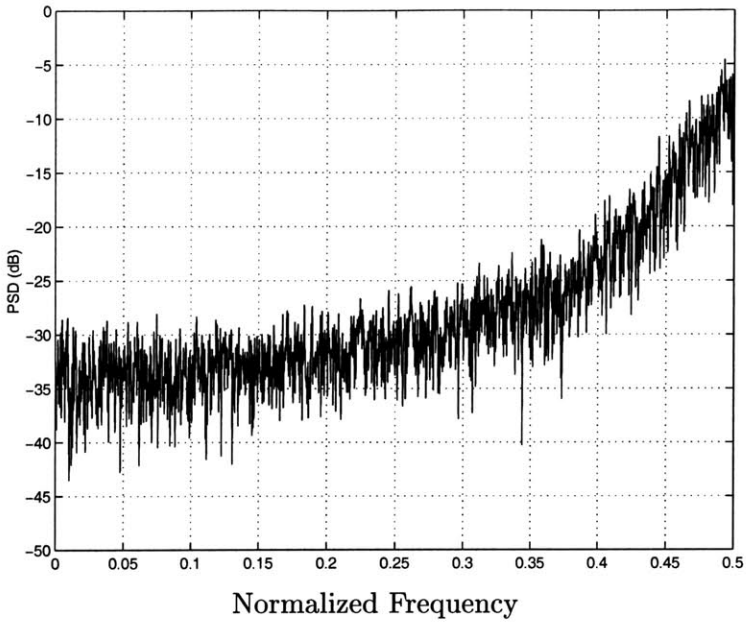
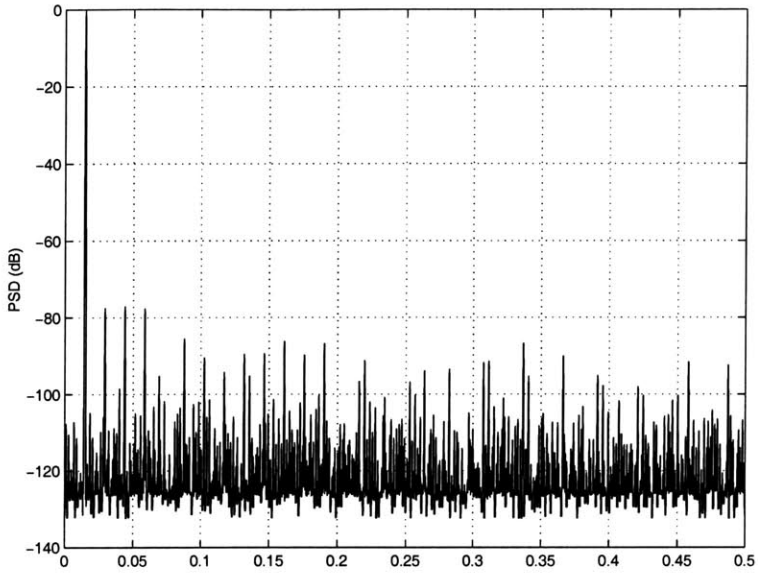


Figure 2-29: The PSD of the noise shaped sequence $s[n]$ used to obtain the results in fig. 2-28.

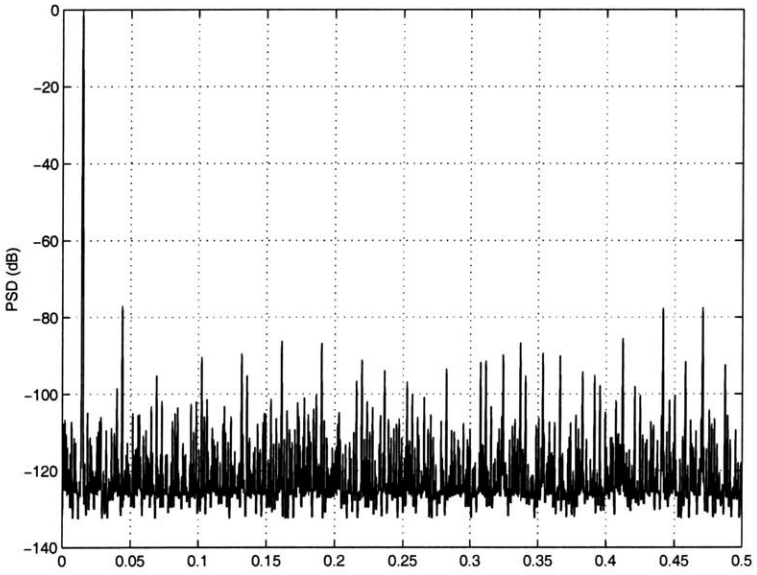
due to these mechanisms will not be pushed out-of-band using mismatch shaping and will impact the linearity of the converter. However, the impact of these non-idealities can be minimized through careful circuit design to the extent that is required by the application at hand.

Fig. 2-30(a) shows the output spectrum of a CFCS converter where the first pipeline stage opamp has a gain of 6.5K. The finite opamp gain introduces odd harmonics because the nonlinearity it introduces is odd. When mismatch shaping is applied as shown in fig. 2-30(b), only the even order distortion components are modulated to half the sampling frequency. The odd harmonics are unaffected. In this particular case the SFDR does not improve at all, and the SNDR improves modestly from 72.1dB to 76.4dB.

The transfer characteristic of a CFCS ADC in the absence of capacitor mismatch, but with the first pipeline stage opamp having a gain of G, can be found using the same analysis method used earlier in the chapter to be:



(a)



(b)

Figure 2-30: The PSD of the output of a 15bit CFCS ADC with 0.1% mismatch in all pipeline stages and with an opamp gain of 6.5K in the first pipeline stage a) no mismatch shaping applied b) with mismatch shaping.

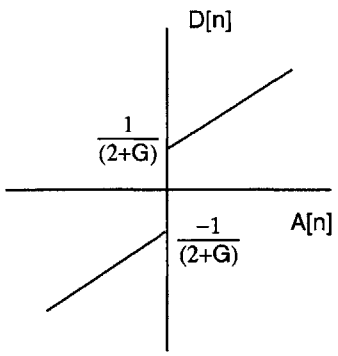


Figure 2-31: The transfer characteristics of a CFCS converter with no capacitor mismatch but with the first pipeline stage opamp having a gain of G.

$$D[n] = \begin{cases} A[n]\frac{1}{1+\frac{2}{G}} + \frac{V_{REF}}{2+G} & \text{if } A[n] > 0 \\ A[n]\frac{1}{1+\frac{2}{G}} + \frac{V_{REF}}{2+G} & \text{otherwise} \end{cases}$$

Fig. 2-31 plots this transfer characteristic for $V_{REF} = 1$. As the gain of the opamp is increased the nonlinearity introduced into the transfer characteristic will be reduced and its impact on the performance of a mismatch shaped converter will be reduced as plotted in fig. 2-32. The improvement does saturate at high gain values because the SNDR becomes dominated by the tones due to capacitor mismatch which alias back into the signal band.

The effect of comparator offset on the transfer characteristic is different than opamp gain. In the absence of capacitor mismatch, comparator offset has no impact because of digital error correction. With capacitor mismatch in the first pipeline stage the transfer characteristic can be rewritten with threshold between the two line segments of the transfer characteristic set to V_{os}:

$$D[n] \approx \begin{cases} A[n](1 - \frac{\Delta}{2}) + V_{REF}\frac{\Delta}{2} & \text{if } A[n] > V_{os} \\ A[n](1 + \frac{\Delta}{2}) + V_{REF}\frac{\Delta}{2} & \text{otherwise} \end{cases}$$

This transfer characteristic is plotted in fig. 2-33(a), and the nonlinear portion of the transfer

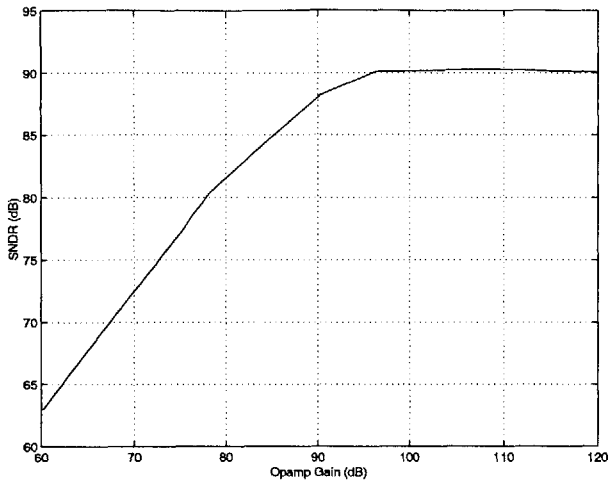


Figure 2-32: SNDR vs. opamp gain for a mismatch shaped CFCS ADC with 0.1% capacitor mismatch and finite opamp gain in all pipeline stages.

characteristic $g(A[n])$ is plotted in fig. 2-33(b). $g(A[n])$ can be decomposed into an even function:

$$g_e(A[n]) = \frac{1}{2}(g(A[n]) + g(-A[n])) \tag{2.37}$$

plotted in fig 2-33(c), and an odd function:

$$g_o(A[n]) = \frac{1}{2}(g(A[n]) - g(-A[n])) \tag{2.38}$$

plotted in fig 2-33(d), such that $g = g_e + g_o$. $g_o(.)$ will introduce odd harmonics which will not be removed by mismatch shaping. The impact of the offset will however not be significant if the offset is not very large, since $g_o(.)$ will remain small. Simulations indicate that an offset as large 5% of the reference voltage V_{REF} can be tolerated without degrading the effectiveness of mismatch shaping. This does assume that the pipeline stage opamp does not saturate when its output exceeds the reference voltage V_{REF} because of the comparator offset. Digital error correction will not function properly if the opamp saturates and this will result in missing and wide codes.

In the simulation results presented up to this point the input to the converter is a band

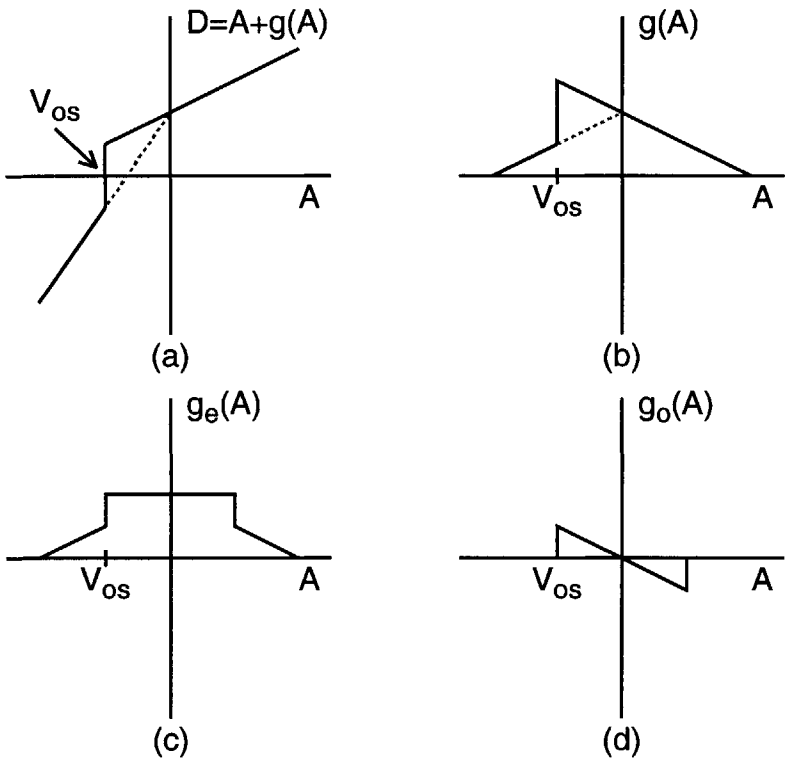


Figure 2-33: (a) The effect of V_{os} comparator offset on the CFCS ADC transfer characteristic in the presence of capacitor mismatch in the first stage. (b) g the non-linear portion of the transfer characteristic (c) g_e the even portion of g d) g_o the odd portion of g.

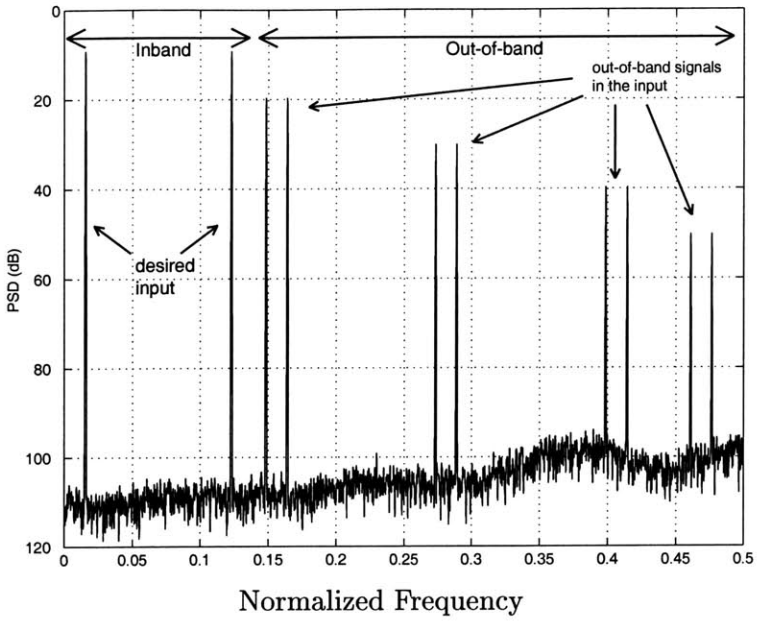


Figure 2-34: The presence of out-of-band signals does not degrade the performance of a mismatch shaped converter if an anti-aliasing filter is used.

limited signal. In a practical scenario the input is likely to contain out-of-band signals. The effectiveness of mismatch shaping is impacted by the bandwidth of the input signal. As the bandwidth of the input increases so does the bandwidth of the distortion and a greater amount of energy will alias back into the signal band with mismatch shaping, reducing the effectiveness of the technique. Typically, the bandwidth of the input is limited using an anti-aliasing filter. In an oversampling converter the anti-aliasing filter will have a wide transition band to ease the complexity of the filter. Fig 2-34 shows the output spectrum in the presence of out-of-band signals which have amplitudes that diminish as the frequency increases to mimic the impact of a weak anti-aliasing filter. The SNDR is 77.2dB and the SFDR is 95dB, compared to a SNDR of 79.6dB and SFDR of 97dB, when no out-of-band signals are present as in fig. 2-28(a). The 2.4dB degradation in performance is not due to a rise in the in-band distortion energy, but rather due to a 3dB reduction in the amplitude of the in-band signal to maintain the total input to within the ADC full scale.

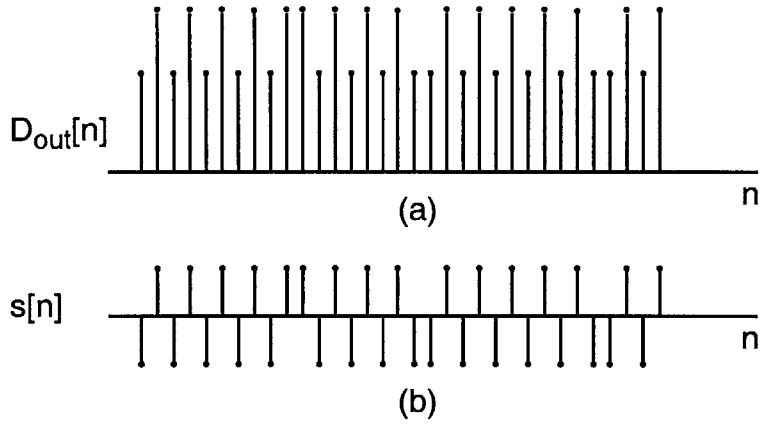


Figure 2-35: (a) The output of a mismatch shaped ADC D_{out} when the input is DC. (b) The mismatch shaping swapping sequence $s[n]$.

2.3 Additional Mismatch Shaping Techniques for CFCS ADCs

In the last section a noise shaped swapping sequence was used to eliminate the discrete tones which alias into the signal band due to mismatch shaping. This however introduced the possibility of a rise in the in-band noise floor. Fig. 2-35(a) shows a time domain view of this by plotting D_{out} the output of the ADC in fig. 2-14, when a DC input is applied. Because the noise shaped swapping sequence $s[n]$ in fig. 2-35(b) is used, the output D_{out} does not simply alternate between two values, but it also exhibits phase modulation. A running average of this output will not be constant; it will rise when two consecutive output samples are high, and will fall when two consecutive samples are low. This time domain view offers an alternate explanation of the rise in the in-band noise floor. It also suggests that eliminating the phase modulation of the output would solve the problem, if we can find an alternate way to randomize the output.

In section 2.2.1 it was shown that by exchanging the role of the pipeline stage capacitors, the transfer characteristics of CFCS converter can be changed. Fig. 2-12 and fig. 2-13 show four different transfer characteristics which can be realized if the role of the capacitors are exchanged for the first two stages. This offers an additional degrees of freedom in the design which can be exploited by making the capacitor that is connected in feedback dependent

d_i	s_i	Feedback capacitor
0	-1	C_1
0	1	C_2
1	-1	C_2
1	1	C_1

Table 2.2: Feedback capacitor selection is controlled by the stage decision bit d_i and stage swapping sequence s_i.

not only on the decision bit of the pipeline stage d_i, but also on a swapping sequence s_i, as summarized in table 2.2. When the first two stages have capacitor mismatch, if the swapping sequence s_1 and s_2 are used for the first and second stages respectively, then the four transfer characteristics in fig. 2-36 can be realized. The figure illustrates how the transfer characteristic can be altered using s_1 and s_2.

To understand the effect of using different swapping sequences for each pipeline stage, let us consider the simple case of a DC input V_{dc}, to a CFCS converter with mismatch only in the first two stages. Changing the swapping sequence s_1 and s_2 makes it possible for the output to take on four values, V_1 through V_4, as illustrated in fig. 2-36. The output of the ADC is shown in fig. 2-37(a) when the same noise shaped sequence is used for the first two stages, or $s_1 = s_2$, as shown in fig. 2-37(b). The ADC output in fig. 2-37(a) takes on only two values because only two of the four possible combinations of s_1 and s_2 are exercised. Here we have ignore the effect of the half sample delay between the pipeline stages to simplify the illustrations. Taking the half sample delay into account only requires us to make $s_1[n] = s_2[n + \frac{1}{2}]$, but this does not alter D_{out}. The ADC output is exactly the same output as in fig. 2-35(a), and the performance is no different.

The ADC output in fig. 2-38(a) results when two independent random sequences are used. The use of the two sequences in fig. 2-38 (b) and (c), allows us to exercise all the four combinations of $s1$ and $s2$, and the output D_{out} takes on four distinct values. Amplitude modulation can be observed in D_{out}, in addition to the phase modulation, which can also be

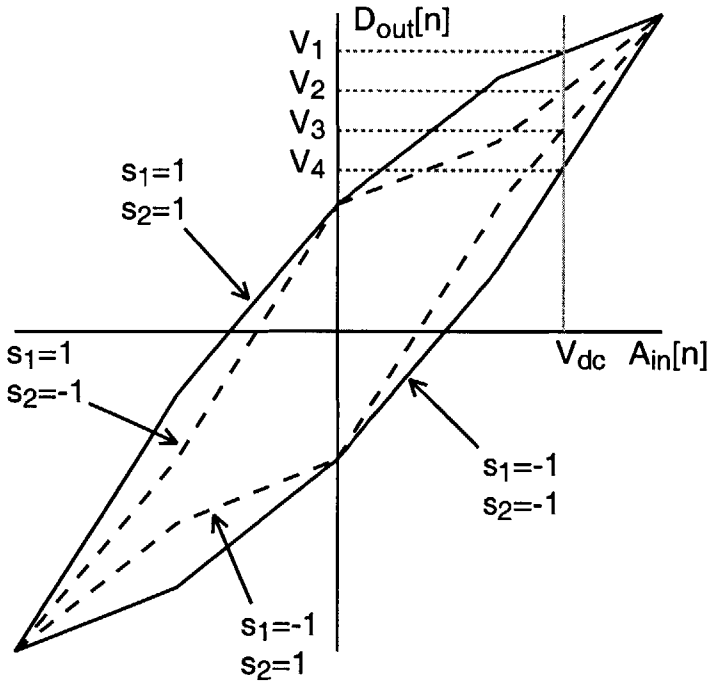


Figure 2-36: The effect of the swapping sequences s_1 and s_2 on the transfer characteristic of a CFCS converter.

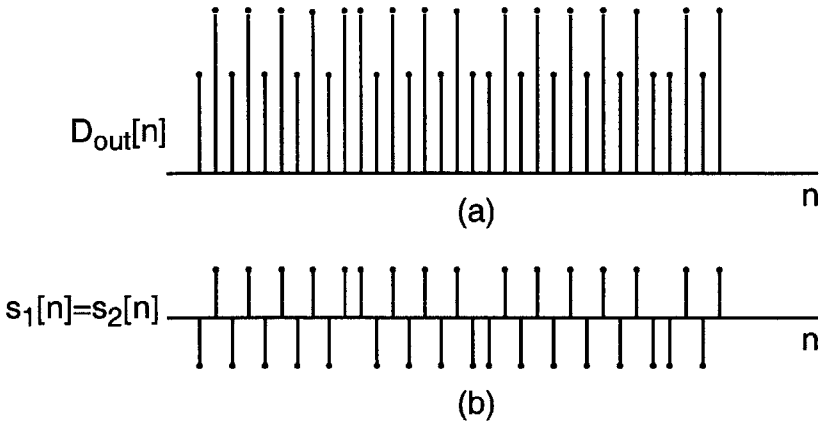


Figure 2-37: (a) The output of a mismatch shaped ADC D_{out} when the input is DC and two mismatch shaping sequences are used. (b) The first and second stage stage swapping sequence.

seen in fig. 2-37(a). The phase modulation whitens the in-band noise floor, but introduces errors at each phase transition. A more effective approach would be to eliminate these phase transitions, while relying on the amplitude modulation to whiten the in-band distortion. This can be realized by using the nonrandom sequence $s[n] = (-1)^n$ for the first stage, and a noise shaped sequence for the remaining stages. Fig. 2-39(a) illustrates the effect of this technique on the output of the ADC with a DC input, with the use of the swapping sequences in fig. 2-39(b) and (c). This method results in an improvement in the SNDR.

A simple implementation of this approach is shown in fig. 2-40, where the first stage is swapped by the sequence $s_1[n] = (-1)^n$, and the remaining stages are swapped simultaneously using the sequence $s_2[n]$. The implementation of the analog and digital multipliers is again simple.

It is possible to use multiple swapping sequences, although no notable performance improvement results when more than 3 sequences are used. For the case of using 3 sequences, 8 different transfer characteristics are possible. With a DC input this translates into 8 possible output values, as shown in fig. 2-41(a). The additional levels make it possible to have better shaping of the distortion, by improving the amplitude modulation. Phase modulation of the output must be avoided here too. The selection rational for the first

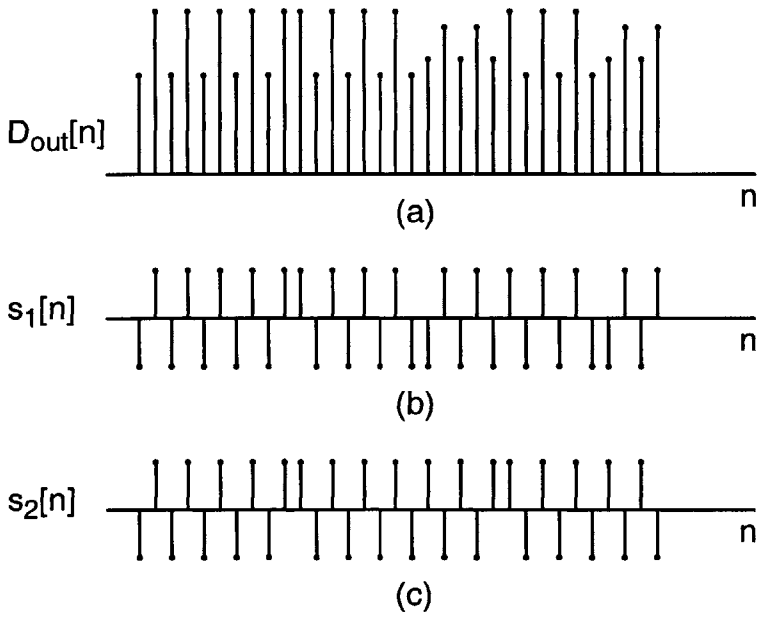


Figure 2-38: (a) The output of a mismatch shaped ADC D_{out} when the input is DC and two independent randomized mismatch shaping sequences are used. (b) The first stage swapping sequence $s_1[n]$. (c) The second stage swapping sequence $s_2[n]$.

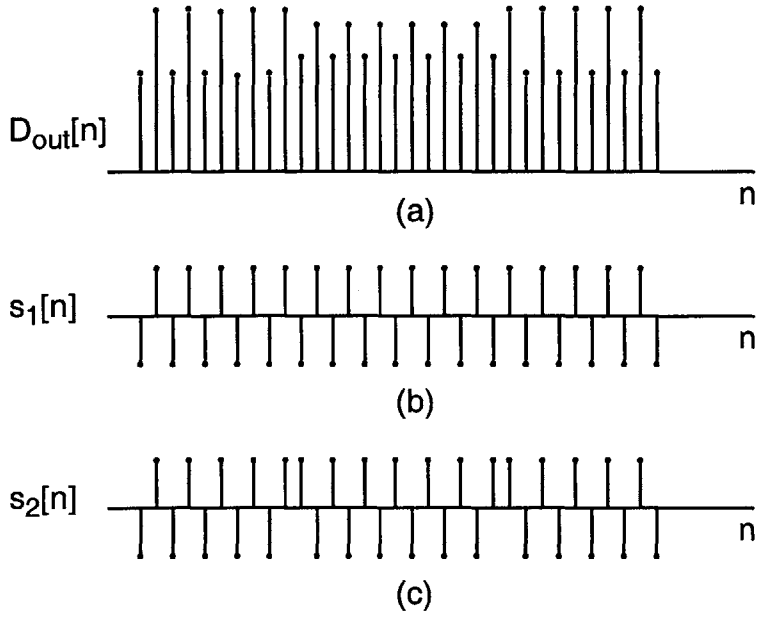


Figure 2-39: (a) The output of a mismatch shaped ADC D_{out} when the input is DC and two independent mismatch shaping sequences are used. (b) The first stage swapping sequence $s_1[n] = (-1)^n$. (c) The second stage swapping sequence $s_2[n]$.

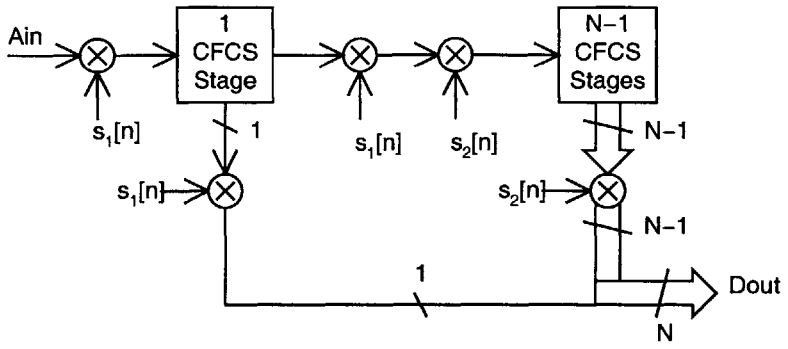


Figure 2-40: Implementation of the two swapping sequence idea.

stage is the same as before, and is the sequence $s_1[n] = (-1)^n$ shown in fig. 2-41(b). The sequences for the remaining stages will be noise shaped sequences, with the second stage sequence, $s_2[n]$ in fig. 2-41(c), having fewer phase transitions compared to the sequence for the back-end, $s_3[n]$, as shown in fig. 2-41(d). The PSD of $s_2[n]$ is shown in fig. 2-42 has a narrower bandwidth compared to the PSD of $s_3[n]$, shown in fig. 2-29. For a DC input case, $s_3[n]$ will result in a fast amplitude modulation on the output due to capacitor mismatch in the back-end and will therefore not be very large in amplitude, reducing the energy aliased into the signal band. This is illustrated in fig. 2-41(a). Fig. 2-43 shows the simulated output spectrum with 0.1% capacitor mismatch in all the pipeline stages. The SNDR in this case is 81dB and the SFDR is 98dB for OSR=4. This demonstrates a 9dB improvement in SNDR and a 28dB improvement and SFDR compared to a CFCS converter. Moreover, it demonstrates a 2dB improvement in SNDR compared to the results in fig. 2-28(a). At an oversampling ratio of 8 the SNDR is 89.3dB and the SFDR is 98dB. These results are included in the last row of table 2.1.

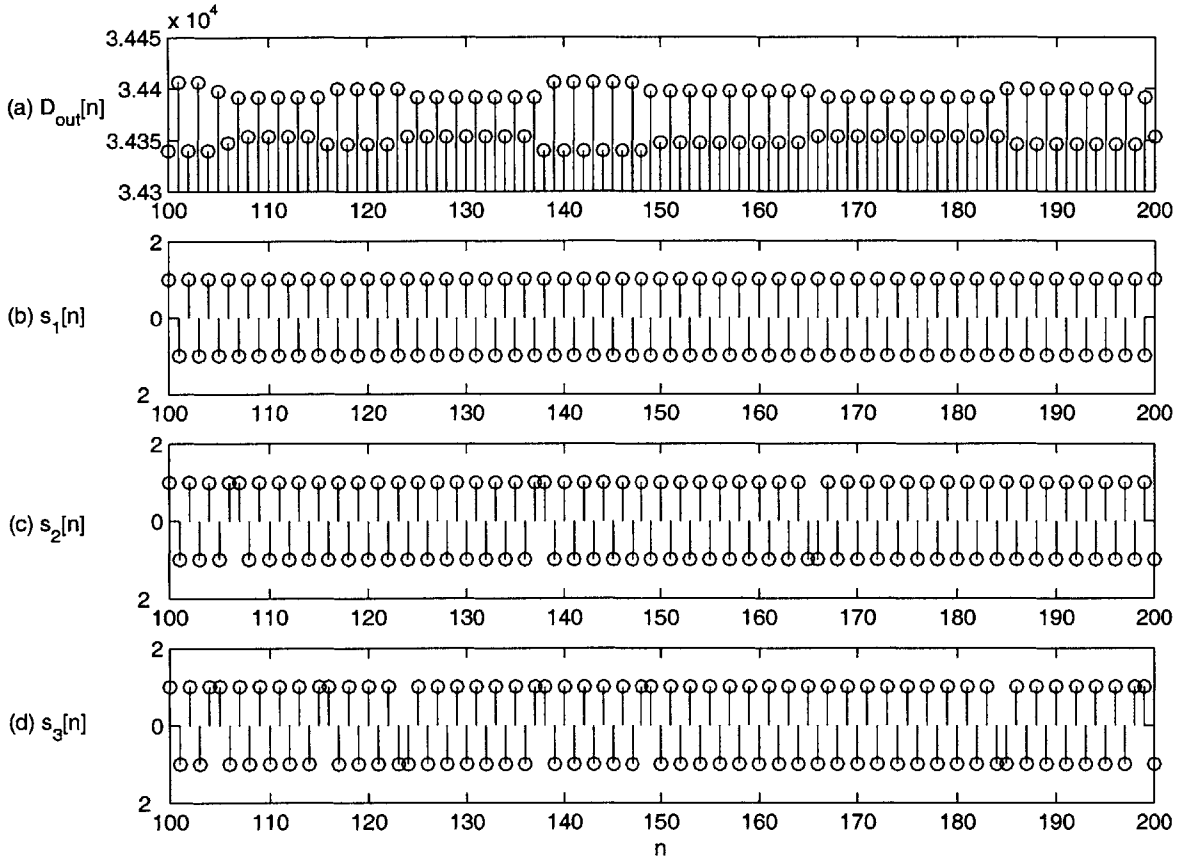


Figure 2-41: (a) ADC output when 3 mismatch shaping sequences s_1, s_2 and s_3 are used. (b) s_1 (c) s_2 (d) s_3.

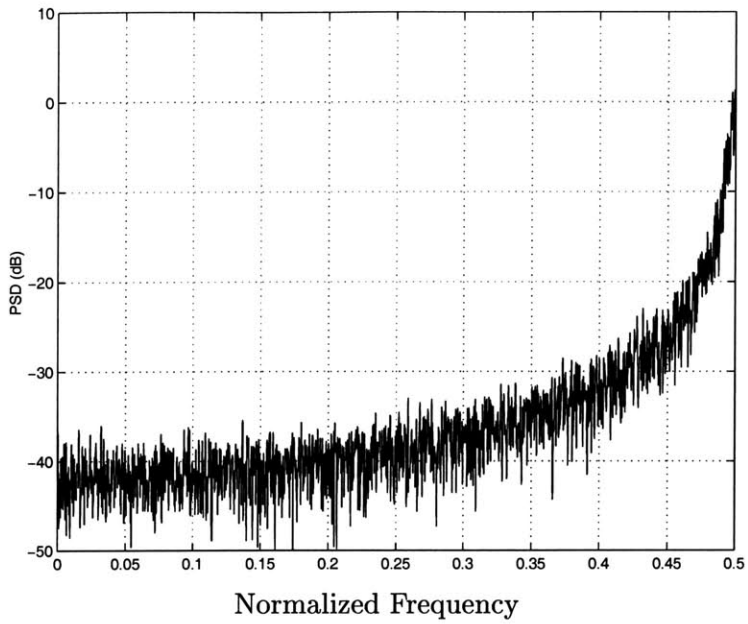
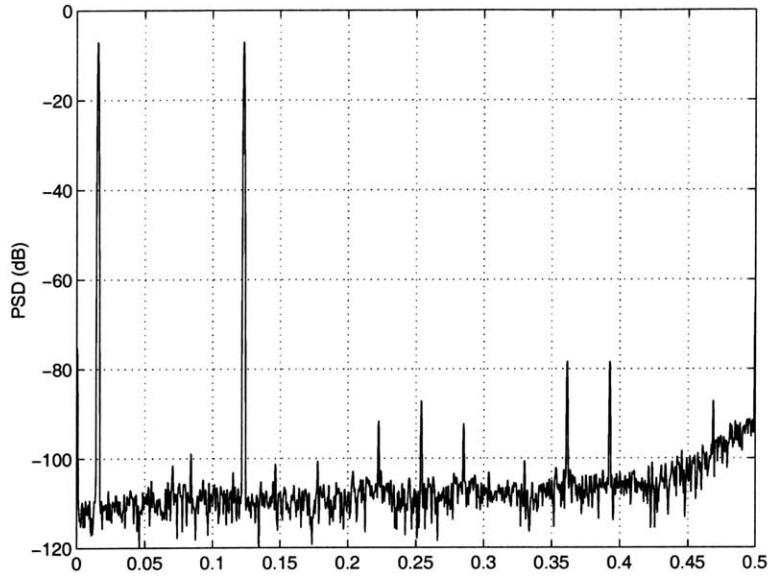


Figure 2-42: The PSD of sw_2, the mismatch shaping sequence used for the second pipeline stage.

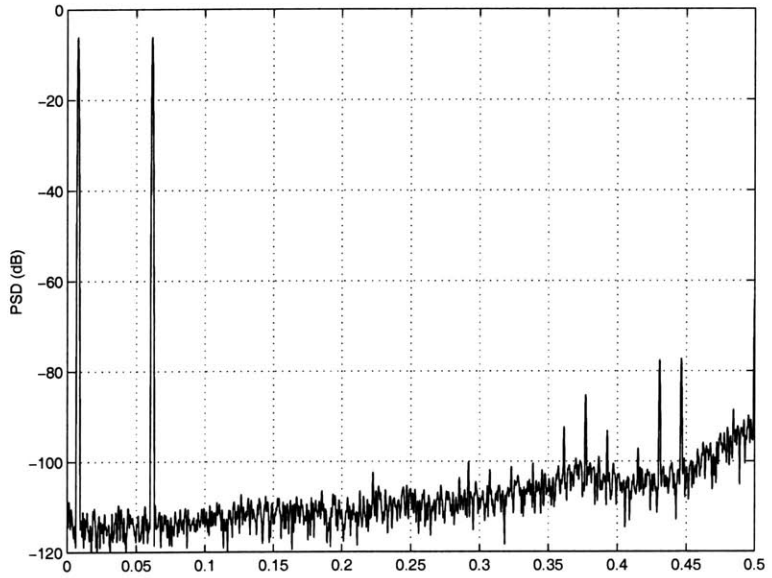
2.4 Extension of Mismatch Shaping to Multi-bit/stage Pipeline ADCs

The extension of the mismatch shaping to multi-bit/stage pipeline converters is quite straightforward. The CFCS is employed here again because it smoothes out the converter transfer characteristic and renders the mismatch shaping more effective. Any one of the methods including dynamic element matching (DEM) based on random selection [5], individual level averaging [15], and data-weighted averaging (DWA) [3] can be used. It appears the DWA is most effective for low oversampling ratio applications. Consider the 2-bit first stage of a pipeline converter with CFCS shown in fig. 2-44. For the simplicity of discussion, the input range of the converter is 0 to V_{REF}, instead of $-V_{REF}$ to V_{REF} in the 1-bit/stage example.

In the normal operation of CFCS, C_1, C_2, C_3, or C_4 is selected as the feedback capacitor if the data is (00), (01), (10), or (11), respectively. In order to accommodate DWA in



(a)



(b)

Figure 2-43: Simulated ADC output with 3 swapping sequences used for mismatch shaping a) OSR=4 b) OSR=8.

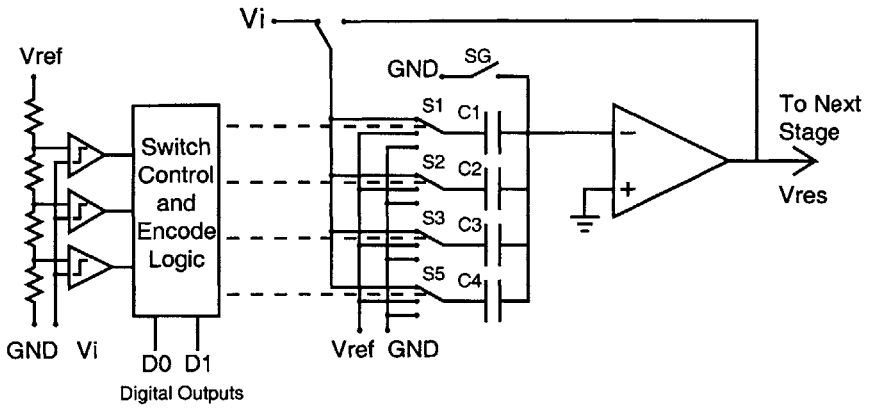


Figure 2-44: 2-Bit/Stage Converter with CFCS and Mismatch Shaping.

conjunction with CFCS, we rotate the roles of C_1 through C_4, such that they are exercised uniformly. For example, if the current data is (10), C_1 and C_2 are connected to V_{REF} (exercised) and C_3 acts as the feedback during the amplification phase. On the next sample, C_3, C_4, C_1, and C_2 assume the role of C_1, C_2, C_3, and C_4, respectively. As a consequence, if the next data is (11), C_3, C_4, C_1 are connected to V_{REF}, and C_2 becomes the feedback capacitor. Now that C_1 through C_4, and then C_1 have been exercised, C_2 assumes the role of C_1, etc., and the process continues. The result of this is shaping of integral nonlinearity of the converter out to high frequencies. Subsequent digital low-pass filtering removes the high frequency error.

This mismatch shaping approach is not as effective as the 1-bit-per-stage implementation. If the input is DC and is in the (01) range it will take 4 samples to exercise all the levels, compared to 2 samples for a 1-bit-per-stage implementation. This results in larger low frequency energy content and lower SNDR compared to a 1-bit-per-stage implementation.

2.5 Distortion in CFCS Pipeline Converters with Bandpass Inputs

Direct-conversion architectures promise to reduce the complexity of the wireless receiver front-ends [42]. They do however suffer from DC offset problems due to VCO leakage into the receive signal path. The use of low IF frequencies is an approach that can be used to mitigate the DC offset problem, while retaining the advantages of direct-conversion. Bandpass ADCs can be applied in these architectures, and in multi-standard radios in which superheterodyne receivers are desired.

It is possible to develop bandpass mismatch shaping techniques based on the ones discussed in this chapter to shape the mismatch energy out of the passband of bandpass converters. However if we simply digitize a bandpass signal using a 1-bit/stage CFCS converter, with a sampling frequency equal to four times the input frequency, then all the distortion will fall out of band. In the discussion that follows this property of CFCS converters will be demonstrated by analyzing the nature of the distortion introduced by it.

Distortion in any converter output is the result of the nonlinearity in its transfer characteristic. To simplify the following distortion analysis, let us use the ADC model shown in fig. 2-45. The first block in the figure is continuous-time, and models the converter nonlinearity. The second block is assumed to be an ideal converter. The first blocks transfer characteristic can be decomposed into a linear and a nonlinear part. The output for a given input is the addition of the contribution of these two parts, that is:

$$D(t) = A(t) + g(A(t)) \tag{2.39}$$

A graphical method is employed in fig. 2-46 to find the output of the first block due to the sinusoidal excitation in fig. 2-46(a), when the nonlinear part of the characteristic is an even function $g_e(.)$, in addition to the case when the nonlinearity is an odd function $g_o(.)$. The even and odd nonlinearities are shown in fig. 2-46(b) and (d) respectively, and the distortion components produced by them are shown in fig. 2-46(c) and (e) respectively, assuming an

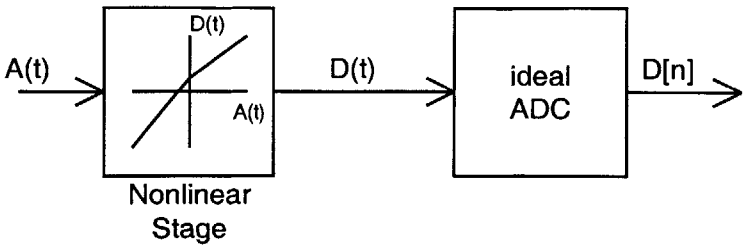


Figure 2-45: The converter model used for distortion analysis.

input with a period of T. When the nonlinear characteristic is odd, the distortion has a period equal to the period T of the input. However, when the nonlinear characteristic is even, as was shown to be the case for a 1-bit/stage CFCS converter, then the distortion component has a period of $\frac{T}{2}$. A Fourier series expansion of this signal reveals that it contains frequency components at multiples of $\frac{2}{T}$, which correspond to even multiples of the input frequency $\frac{1}{T}$. This means that a CFCS converter will have only even order harmonic distortion with no odd order harmonics. The output of the nonlinear stage is sampled by the ideal ADC. If the sampling frequency is four times the input frequency, that is $\frac{4}{T}$, then the distortion components in $D[n]$ will be at DC and half the sampling frequency. For this reason, the intermodulation distortion due to co-channel and near-channel interferers will fall completely out of band, when the input channel frequency is a quarter of the sampling frequency.

To demonstrate the distortion properties, a 15-bit, 1-bit per-stage, CFCS converter was simulated in Matlab. Fig. 2-47 and fig. 2-48 show the output power spectral density, with 0.1% mismatch in the first three stages of the converter, and an oversampling ratio (OSR) of 8 and 16 respectively. The output of the converter contains two input tones, each 6dB below full scale. The distortion and intermodulation products fall out of band, concentrated near half the sampling frequency and zero, and with no distortion visible near the band of interest in fig. 2-48, which implies a very large third intercept point(IP3). The SNDR calculated from the simulation output is 90dB and 97dB respectively. Similar results were obtained even in the presence of a 5% offset in the input. Fig. 2-49 shows the output spectrum of a conventional 1-bit-per-stage pipeline ADC. Since the transfer characteristic

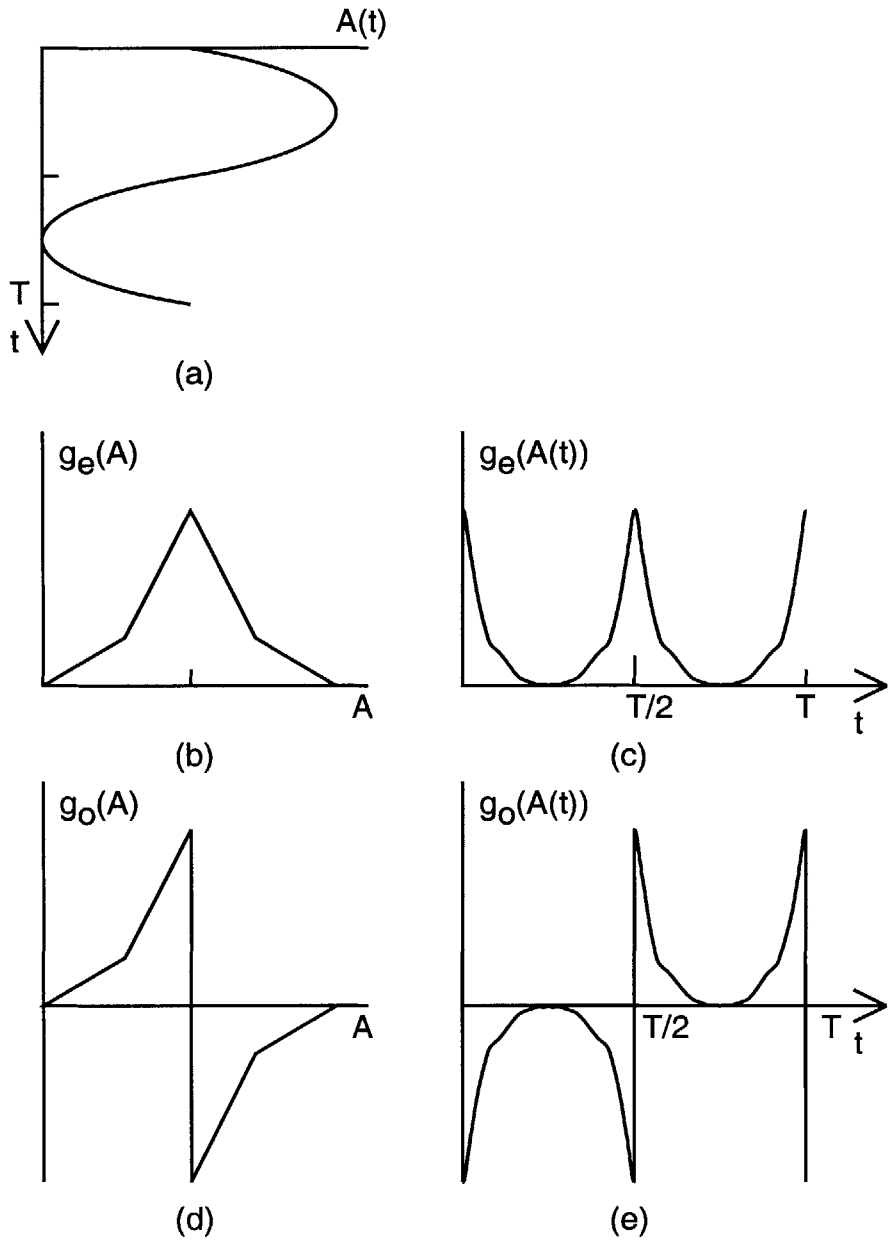


Figure 2-46: (a) Input to the ADC (b) Even nonlinearity (c) distortion due to even nonlinearity (d) Odd nonlinearity (e) distortion component due to odd nonlinearity.

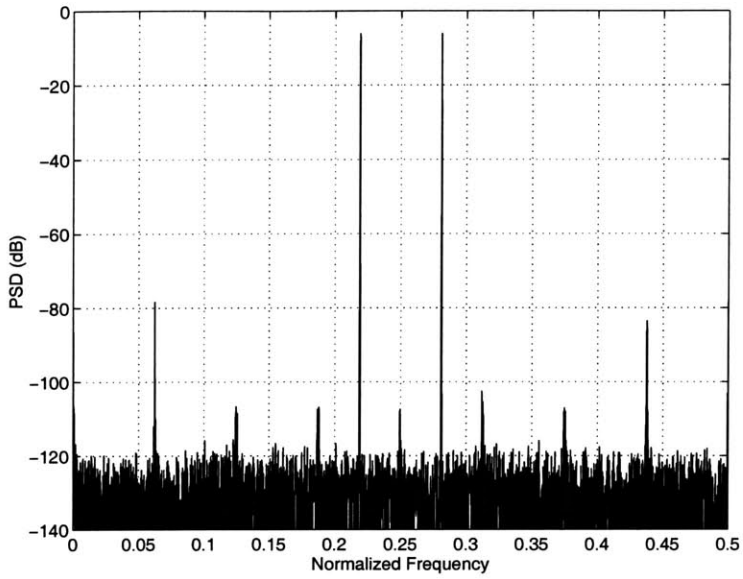


Figure 2-47: Power spectral density of converter output when OSR=8.

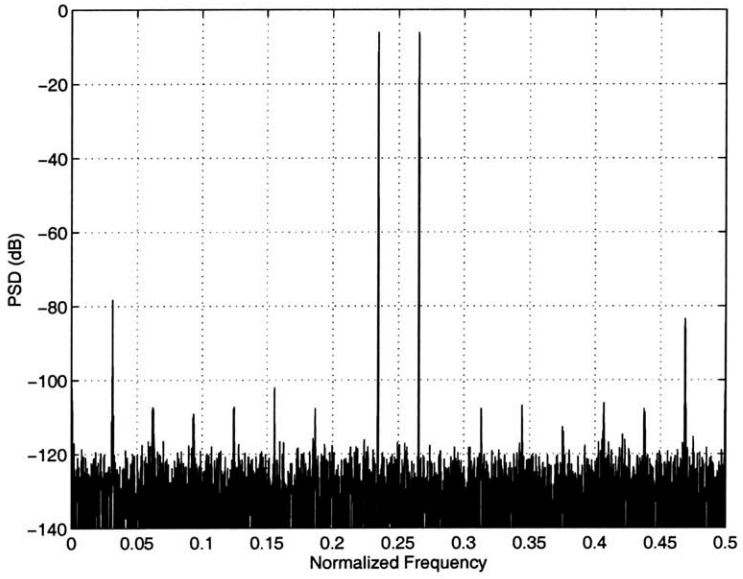


Figure 2-48: Power spectral density of converter output when OSR=16.

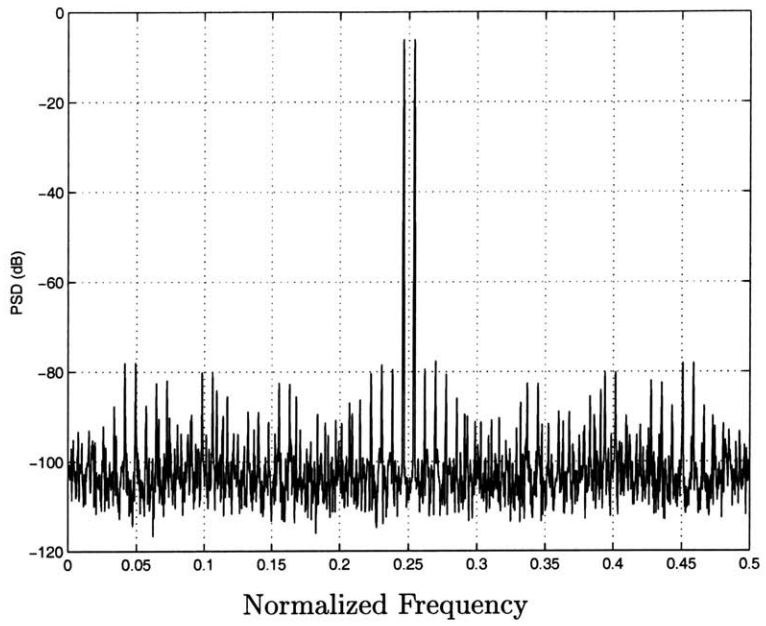


Figure 2-49: The output spectrum of a conventional 1-bit-per-stage pipeline ADC with 0.1% component matching.

of such an ADC has an odd INL, the dominant distortion and intermodulation products are odd-order. With a two tone input the worst case scenario is when the tones are close to each other in frequency. The dominant distortion components fall in-band and limit the SNDR to 66dB and the SFDR to 72dB, at an oversampling ratio of 8 and 0.1% component matching. Increasing the oversampling ratio does not improve the performance since the distortion components will continue to fall in-band.

The performance of the CFCS converter is tolerant to the presence of out-of-band signals. In fig. 2-50 an out-of-band signal is place at half the input frequency, such that it's second harmonic falls in-band. In addition, this out-of-band signal is 40dB below full scale, a worst case value, since a typical attenuation figure for a IF bandpass filter is around 40dB. From fig. 2-50 it can be seen that no tones are visible in-band, and there is no rise in the quantization noise floor.

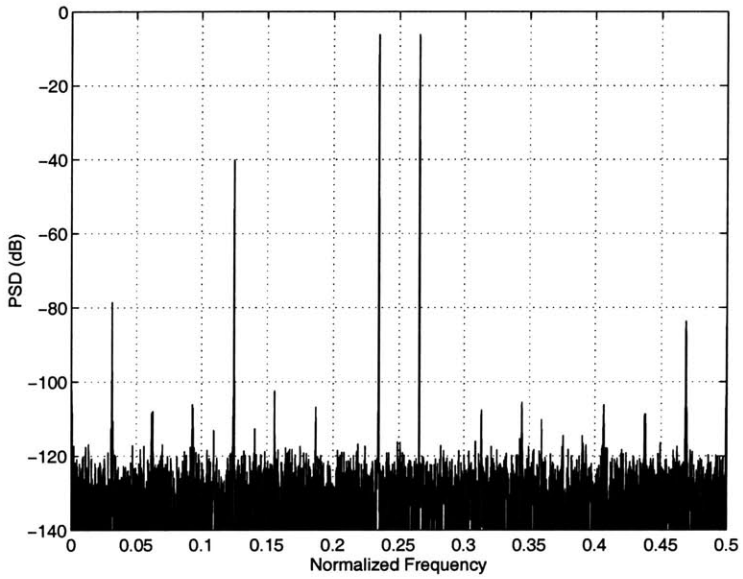


Figure 2-50: Out-of-band signals have no effect on the performance of the ADC.

Chapter 3

Test Chip Architecture and Design

In the previous chapter it was shown that mismatch shaping coupled with oversampling can be used to significantly improve the accuracy of pipeline converters. The 1-bit/stage CFCS converter played a central role in the realization of mismatch shaping algorithms. This chapter will describe the design of a test chip which was fabricated in a 0.35μm CMOS process to demonstrate mismatch shaping. The test chip has at its core a 1-bit/stage CFCS converter. The chapter will begin by discussing the target specifications of the converter and the motivation behind selecting these goals. The overall architecture of the ADC will be presented. Each of the ADC's building blocks will then be described in greater detail. The chapter will end with a brief discussion of the approach adopted to verify the performance of the ADC in simulation.

3.1 ADC Target Specifications

The SNDR performance of an oversampling pipeline ADC with mismatch shaping is dependent on many factors including capacitor mismatch, noise and circuit nonidealities. Fig. 3-1 demonstrates some of these dependencies by plotting the ADC SNDR as a function of capacitor mismatch for a mismatch shaped converter and for a CFCS converter with no mismatch shaping. The SNDR here does not include the effect of thermal noise, and is

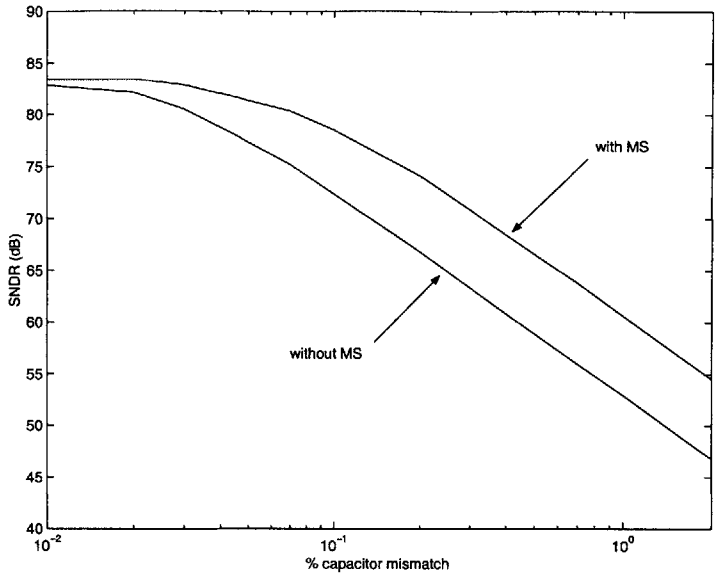


Figure 3-1: ADC SNDR (at OSR=4) vs. capacitor matching with and without mismatch shaping. The ADC opamps have a gain of 2^{14}.

dominated by distortion, with the effect of quantization noise being negligible. The figure demonstrates that mismatch shaping improves the performance under most conditions compared to a CFCS ADC. The performance also improves as capacitor matching improves, simply because the energy of the distortion is directly proportional to capacitor mismatch. The SNDR does not continue to improve as capacitor matching improves, because the performance of the converter becomes limited by factors other than capacitor matching. In this particular simulation the limiting factor is the finite opamp gain which was set to 2^{14}(about 16400). Other possible performance limiting factors may include signal dependent charge injection, comparator offset and dynamic error, such as incomplete settling and comparator hysteresis, all of which introduce distortion. The performance could also be limited by white noise sources such as the $\frac{kT}{C}$ thermal noise or quantization noise. The dominant limit can be identified by comparing the SNR and the THD of the converter. If the SNR is much smaller than the THD, then the converter is limited by the white noise sources. This is a desirable condition in a properly designed converter because the SNDR is no longer a function of parameters which vary with the fabrication process, leading to a robust design.

More importantly, in many signal processing and control applications it is important not to have the dominant ADC error source to be correlated with the ADC input, as is the case with distortion[1].

In fig. 3-1 the SNDR, at a capacitor mismatch of 0.1%, is 72.4dB and 78.5dB, for a CFCS ADC and a mismatch shaped CFCS ADC respectively. This SNDR figure is dominated by distortion, with thermal noise effects not included in the simulation. If we want to make the converter SNDR dominated by thermal noise and not distortion, then we will have to set the thermal noise floor around 66dB and 72dB for a CFCS and mismatch shaped converter respectively. If we were to set the thermal noise floor for a CFCS converter to 72dB then the total noise floor will be around 69dB and will have a strong distortion component in it. Applying mismatch shaping to this CFCS converter will increase the SNDR to 72dB and reduce the impact of distortion.

In choosing the target SNDR specifications of a converter one needs to keep these considerations in mind. Assuming the process being used offers capacitors which match between 0.1% to 0.2%, a SNDR target of 70dB is selected based on fig. 3-1. A 70dB SNDR sets the effective resolution of the converter to near 12bit.

The input range of the ADC is set to $2V_{pp}$, and is selected based on the requirements for NMOS switches in a 3.3V 0.35μm process, without relying on clock boosting [32]. The sampling rate was set at a reasonably aggressive figure for the process with minimum power consumption. Table 3.1 summarizes the target specifications of the converter. These figures will be revisited later in this chapter.

[1]For example, in problems which involve waveform detection in the presence of noise, the optimal detector which minimizes the mean squared error, requires the additive noise to be white. Whitening filters are often used to help satisfy this requirement. However, distortion produced by the ADC is a result of a nonlinear process that is not generally known apiori, and it is not possible to use a linear filter to whiten the distortion. Hence, in such a case it would be necessary for the ADC distortion to be much smaller than the other additive noise sources in order for the results of linear detection theory to be used.

SNDR (dB)	70
Resolution (bits)	12
Differential input range (V_{pp})	2
Supply voltage (V)	3.3
Clock speed (MHz)	110
Power consumption	minimize

Table 3.1: ADC target specifications.

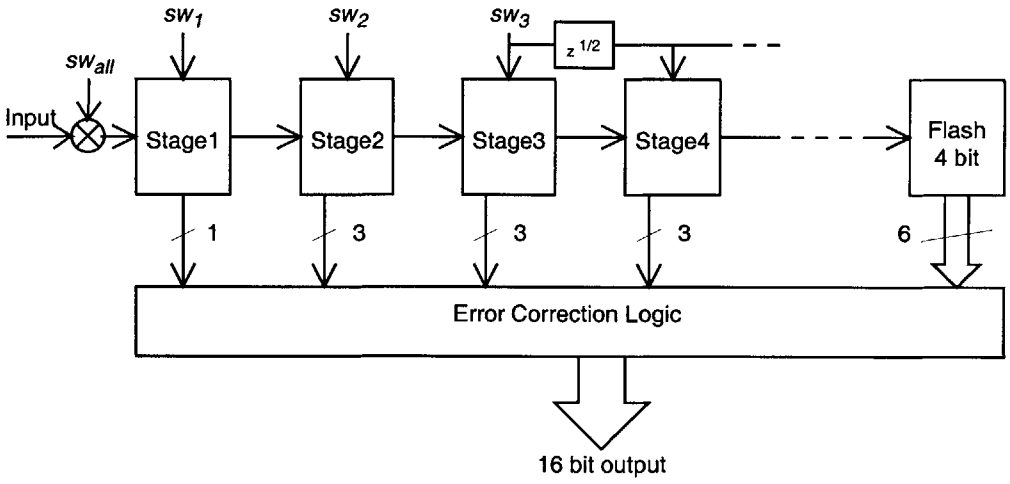


Figure 3-2: ADC block diagram.

3.2 ADC Architecture

This section will present an overview of the ADC architecture, with more details in the sections that follow. Figure 3-2 shows the ADC block diagram. The ADC is composed of 11 CFCS pipeline stages, a back-end flash ADC, digital error correction logic and a front-end multiplier for mismatch shaping using the sequence sw_{all}. A back-end multiplier is also needed but is implemented off-chip in software. The ADC can in addition utilize the swapping sequences sw_1 and sw_2, which are applied to the first and second stages respectively. The sequence sw_3 is applied to stages 3 through 7.

Although the ADC has a resolution of 12 bits, it produces a 15-bit output. This reduces

the quantization noise to a level much below the $\frac{KT}{C}$ thermal noise floor. If the quantization noise were made equal to the thermal noise, as is usually done, then the total ADC noise floor would be 3dB's above the thermal noise. Reducing the quantization noise by using a low power flash in the ADC back-end, allows us to increase the thermal noise budget by reducing the values of the capacitors used and hence saving power.

The first stage produces a single bit, whereas stages 2 through 11 produce 3 bits each, to allow for digital error correction [36]. As the analog input signal propagates through the pipeline stages it is possible in the presence of capacitor mismatch, comparator offsets or charge injection, for the signal to exceed the allowable internal range of the ADC: V_{ref} to $-V_{ref}$. This will result in saturating the remaining stages of the pipeline if no error correction is used. Error correction simply pulls the signal back into the allowable range in the analog domain, and corrects for this level shift digitally. Fig. 3-3 plots the residue diagram for stage 2, which is identical to the residue diagram for the remaining pipeline stages. The residue diagram is simply the transfer characteristic of the stage. When the input to the stage is below $-V_{ref}$ then the stage adds V_{ref} to its analog output and to compensate for that it subtracts $\frac{1}{2}$ from the stages digital output. This error correction implementation results in a 3-bit output for the stage, representing 4 possibilities, which are $-\frac{1}{2}$, 0, 1 and $1\frac{1}{2}$, and are encoded as 000, 001, 011 and 100 respectively.

The final stage in the pipeline is a 4-bit flash ADC, which also outputs 2 additional bits to be used for digital error correction. The 37 bits generated by the pipeline stages are fed into buffers which align the bits, which were misaligned by the half sample delay due to each pipeline stage. The output of these buffers is then fed into an adder that performs the error correction. The final output is 16 bits, and contains 15 bits of information. The output is reduced to 15 bits off-chip by simply subtracting the offset in the 16bits.

3.3 Design of the CFCS Pipeline Stages

The design of the CFCS pipeline stages is based on the principle explained in the previous chapter. For the test chip a fully differential implementation was selected. This section will

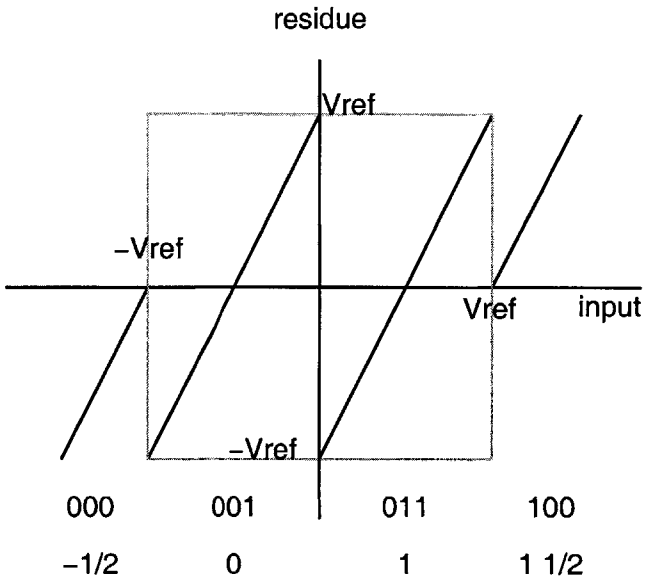


Figure 3-3: Residue diagram for the pipeline stages following the first stage.

show in detail the operation of the stage by demonstrating how the stage capacitors are connected in the network around the opamp. This is accomplished using switches controlled by the clocks, the stage decision bit and the swapping sequence.

The fully differential implementation of the first stage is shown in figure 3-4. During the sampling phase ϕ_1 the polarity of the input can be reversed depending on the value of sw_{all}, using cross coupled switches. When sw_{all} is one the input is connected directly to the sampling capacitors and when it is zero the input polarity is reversed. This realizes the front-end multiplier operation simultaneously with the first stage sampling. At the end of the sampling phase the comparator is enabled and its output goes through combinational logic circuits that decided the configuration of the network that surrounds the opamp during the second phase ϕ_2. This is accomplished through the use of the 6 control signals shown in figure 3-4. These control signals are generated using the following logic equations:

- $a = \phi_2 \cdot d \cdot \overline{sw_1}$
- $ab = \phi_2 \cdot \overline{d} \cdot sw_1$

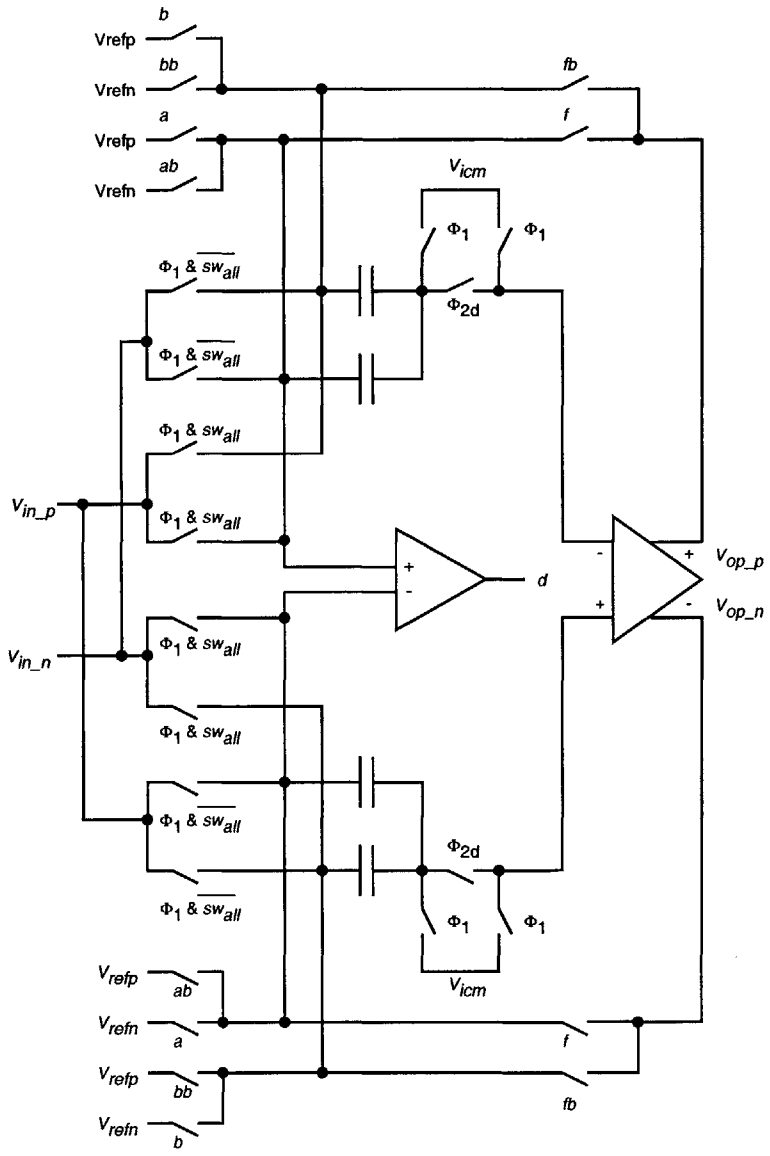


Figure 3-4: Circuit diagram of the first pipeline stage.

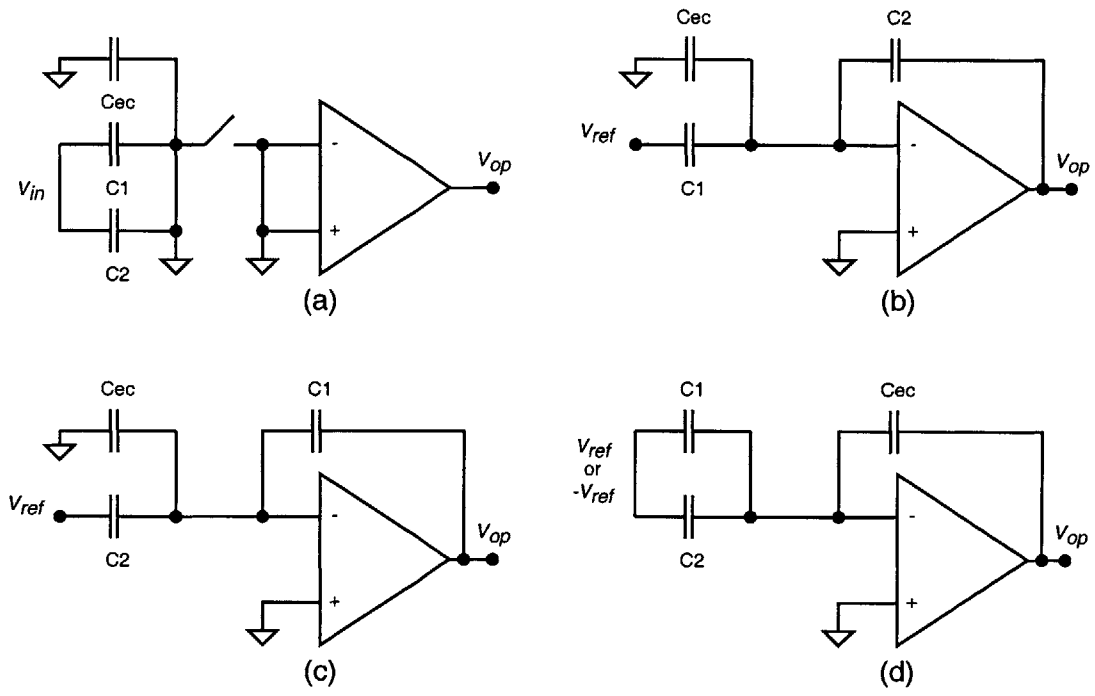


Figure 3-5: Operation of the 2nd stage a) sampling phase b)1 if $V_{ref} > V_{in} > 0$ c) if $-V_{ref} < V_{in} < 0$ d) if the input is out of range that is $V_{in} > V_{ref}$ or $V_{in} < -V_{ref}$.

- $b = \phi_2 \cdot d \cdot sw_1$
- $bb = \phi_2 \cdot \overline{d} \cdot \overline{sw_1}$
- $f = \phi_2 \cdot (\overline{d} \cdot \overline{sw_1} + d \cdot sw_1)$
- $fb = \phi_2 \cdot (d \cdot \overline{sw_1} + \overline{d} \cdot sw_1)$

where d is the comparator decision bit and sw_1 is the swapping sequence for the first stage. The above equations show that the capacitor connected in feedback is not only a function of the decision bit as required for CFCS operation, but is also a function of the swapping sequence sw_1, as summarized in table 2.2.

The pipeline stages following the first stage implement digital error correction and have the residue plot shown in fig. 3-3. A simplified circuit realization of this residue diagram is shown in fig. 3-5, with sampling phase is shown in fig. 3-5(a). To detect over ranging 2

additional comparators are needed to compare the input to V_{ref} and $-V_{ref}$. This implementation also requires one additional capacitors Cec. If the input to the stage is in the allowed range then the operation of the stage is shown in fig. 3-5(b) and (c) for the multiplying phase. This is identical to the CFCS operation described in the previous chapter, with the exception of the presence of Cec, which performs no function in these phases. If the input is out of range then Cec is connected in feedback as shown in fig 3-5(d). The stage output V_{op} can be written as a function of the input V_{in} as:

$$V_{op} = \begin{cases} \frac{C_1+C_2}{C_{ec}} V_{in} - \frac{C_1+C_2}{C_{ec}} V_{ref} & \text{if } V_{in} > V_{ref} \\ \frac{C_1+C_2}{C_2} V_{in} - \frac{C_1}{C_2} V_{ref} & \text{if } V_{ref} \geq V_{in} > 0 \\ \frac{C_1+C_2}{C_1} V_{in} + \frac{C_2}{C_1} V_{ref} & \text{if } 0 \geq V_{in} > -V_{ref} \\ \frac{C_1+C_2}{C_{ec}} V_{in} + \frac{C_1+C_2}{C_{ec}} V_{ref} & \text{if } V_{in} \leq -V_{ref} \end{cases}$$

We note that as the input transitions from below V_{ref} to above it, the stage output decreases by exactly V_{ref}, even in the presence of capacitor mismatch. This is very important because the digital error correction logic will compensate for this level shift exactly and no DNL errors will result. If C_{ec} is not used as the feedback capacitor when $V_{in} > V_{ref}$, then the voltage drop will not be V_{ref} in the presence of capacitor mismatch. The compensation in the digital domain will not be exact and large DNL errors will result. A similar effect results if C_{ec} is not used as the feedback capacitor when $V_{in} < -V_{ref}$. Therefore, selecting Cec as the feedback capacitor under over-ranging conditions, is necessary to avoid large DNL errors.

With the residue digram of fig. 3-3, the digital output of the stage contains 3 bits, because of the need to represent $-\frac{1}{2}$, 0, 1 and $1\frac{1}{2}$. It is possible to have a 2-bit representation of the output if the residue plot in fig. 3-6 is implemented. Although this simplifies the digital output, it requires the use of an additional capacitor. This results in the opamp operating at a feedback factor of 1/4 instead of 1/3. To accommodate for the lower feedback factor requires a larger gain in the opamp to maintain a fixed steady settling error. Settling time requirements are harder to meet under these conditions for a high speed converter and this

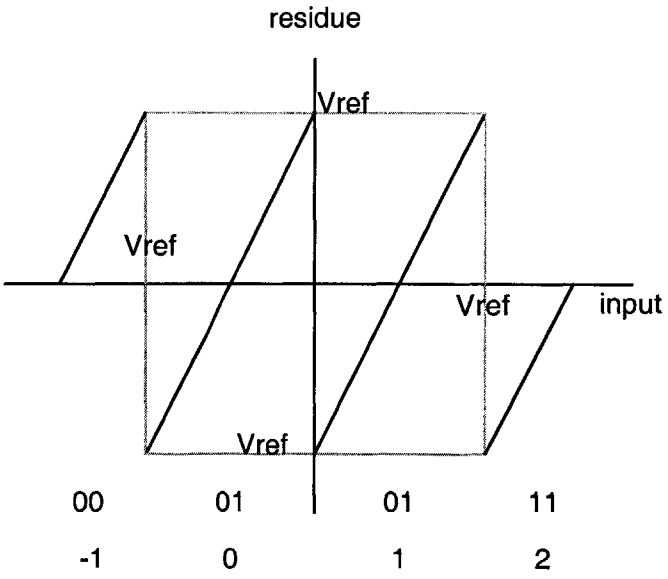


Figure 3-6: An alternate residue plot for the 2nd pipeline stage with simpler encoding for the digital output.

approach was avoided.

Fig. 3-7 shows a detailed circuit diagram of the implementation of the 2nd stage. Although the differential half of the circuit is shown for simplicity, the diagram does show all the needed control signals. There are 9 control signals which realize the logic equations:

- $a = \phi_2(d \cdot \overline{sw_2} + H)$
- $ab = \phi_2(\overline{d} \cdot sw_1 + L)$
- $b = \phi_2(d \cdot sw_1 + H)$
- $bb = \phi_2(\overline{d} \cdot \overline{sw_1} + L)$
- $f = \phi_2 \cdot (\overline{d} \cdot \overline{sw_1} + d \cdot sw_1)(\overline{HL})$
- $fb = \phi_2 \cdot (d \cdot \overline{sw_1} + \overline{d} \cdot sw_1)(\overline{HL})$
- $over\_H = H \cdot \phi_1$
- $over\_L = L \cdot \phi_1$

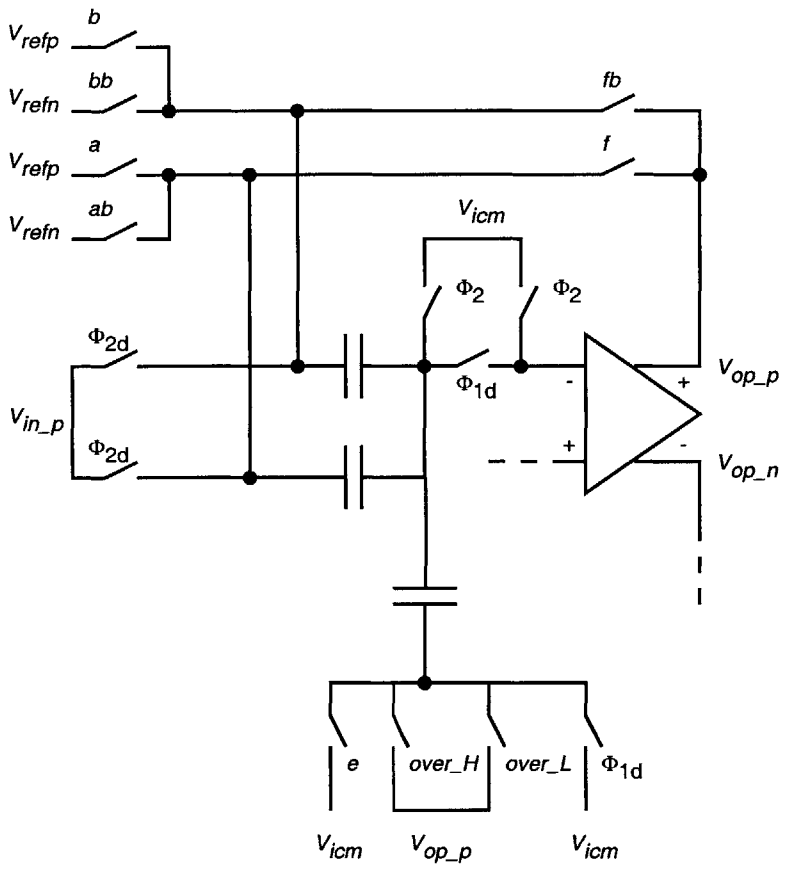


Figure 3-7: Simplified circuit diagram of the 2nd pipeline stage.

- $e = \overline{H + L} \cdot \phi_1$

where H is high when the stage input is larger than the allowed range, and L is high when the stage input is lower than the allowed range, as detected by the extra comparators.

Bottom plate sampling is performed [43, 44], with the input switches turned off at a delayed time to reduce input dependent charge injection. Also, during the sampling period the opamp is disconnected from the sampling network, this speeds up the sampling operation [29] as the switches and capacitor determine the speed and the slower opamp dynamics are removed. Disconnecting the opamp helps reduce the input common mode disturbance to the opamp input, which would otherwise result due to the large common mode charge injected by the bottom plate (input) switches. Finally, the opamp is not placed in unity

gain feedback during sampling, which simplifies the opamp design since it no longer needs to be unity gain stable. Although open loop sampling does not cancel the opamp offset, the performance of the converter is unaffected. The opamp offset does result in an offset in the residue curve of the pipeline stage, but does not change the residue curve shape. Since digital error correction is employed, the offset does not result in saturation effects, and it can simply be referred to the ADC input as an overall offset. Mismatch shaping will modulate the ADC offset to half the sampling frequency, where it can be removed digitally without impacting the converter performance.

3.3.1 The Switches

The switches play a very important role in determining the achievable performance of the converter. The switches must have low enough parasitic capacitance and ON resistance in order not to effect the speed of the pipeline stage. Large switch parasitic capacitance connected to a two stage opamp output will reduce the opamp's non-dominant pole frequency. This will reduce the phase margin and can result in ringing in the opamp transient response degrading the settling time. At the opamp input, large parasitic capacitance will reduce the feedback factor and hence increase the settling time and noise. Switch resistance in the opamp sampling network creates a RC network with the sampling capacitors. High ON resistance and parasitic capacitance will serve only to increase the time constant of the RC network and will slow it down.

Switch resistance also combines with circuit capacitors to introduce pole-zero pairs in the closed loop response of the opamp. A switch with resistance R in series with the stage capacitor results in a total impedance:

$$Z = R + \frac{1}{sC} = \frac{sCR + 1}{sC} \tag{3.1}$$

When the opamp is in feedback, the stage gain is:

$$Gain = \frac{Z_i + Z_f}{Z_i} = \frac{sC(R_i + R_f) + 2}{sCR_i + 1} \tag{3.2}$$

where Z_i is the impedance of the input capacitor and the switch resistance in series with it R_i. Z_i is the impedance of the series combination of the feedback capacitor and the switch resistor R_i in series with it. The switch resistance introduces a pole zero pair in the stage gain. Large switch resistance will reduce the pole-zero pair frequency to a point where it begins to impact the transient response [45].

The top plate switches of the sampling capacitors need to be small enough to minimize the signal dependent charge injection. Ideally, the charge in the top plate switch splits equally between the transistor source and drain when it is turned off, if bottom plate sampling is implemented. However, variations in the bottom plate switch resistance and non-linear parasitic capacitance caused by the input impacts the splitting of the charge, adding a signal dependent component to the sampling capacitor charge. Nonlinear variations in the switch resistance and parasitic capacitance cause the charge injection to be nonlinear, introducing distortion. This distortion can be reduced by reducing the size of the top plate switch.

Finally, the first stage input switches sample a continuous time signal and must be linear to avoid distorting the input. The voltage dependence of the MOS transistor channel resistance, source and drain depletion capacitance and the gate capacitance introduce nonlinearity which pre-distorts the ADC input prior to sampling. To minimize distortion, 35μm NMOS bottom plate switches are used. Simulations indicate that a 70dB SDR is achievable when a 50MHz signal is sampled at a 200MHz clock frequency.

A PMOS transistor switch placed in parallel with a NMOS switch can help linearize the ON resistance of the switch. However, this is only possible when the NMOS and PMOS transistors have the same ON resistance in deep strong inversion. The ON resistance R_{on} is:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_t)} \tag{3.3}$$

where μ is the carrier mobility, C_{ox} is the oxide capacitance, W the transistor width, L the transistor length, V_{gs} the gate to source voltage and V_t the threshold voltage. The reduced hole mobility and the lower $(V_{sg} - V_t)$ for PMOS transistors, mandate a PMOS width equal

to 4 times the NMOS transistor's width, to achieve the same ON resistance. These large PMOS transistors (140μm) introduce significant parasitic capacitance which degrades the opamp step response. In addition, the charge injection and clock feed-through due to these transistors, significantly perturbs the operating point of the opamp. At the ADC input the use of complementary switches was found to introduce far more distortion compared to NMOS switches. This is due to the effect of the nonlinear parasitic capacitance of the switch, which dominates over the effects of the nonlinear switch ON resistance.

To maintain a low ON resistance the NMOS switches must be in deep strong inversion. With a clock high value equal to the supply voltage V_{dd}, the maximum signal voltage must be lower than $V_{dd} - V_t$, with the body effect taken into account. In the absence of clock boosting the use of NMOS switches does reduce the allowable signal swing to about 1V (single ended). Low Vt devices were investigated in an attempt to increase the swing [33]. It was found that these devices do not offer any advantage, because their ON resistance was larger than the high Vt transistors, if we keep the switch parasitic capacitance constant. The higher ON resistance is due to the longer minimum gate length of these devices, which is perhaps imposed by hot carrier degradation concerns [46]. No attempt was made to use these devices with lengths lower than this limit, because the operating supply voltage is very close to the maximum allowed, where hot carrier effects are most pronounce.

3.3.2 References

The ADC references are generated off-chip using bandgap references (AD589) which are buffered using low noise amplifiers (SSM2135) and decoupled with low inductance 0612 ceramic capacitors immediately next to the ADC chip pins. A 15Ω on-chip resistor is needed in series with the bondwire as shown in fig. 3-8. This helps reduce the on-chip reference ringing caused by the LC tank of the bondwire inductance and sampling capacitor being perturbed by the current impulses during the multiply phase of operation. The on-chip resistance simply reduces the quality factor of the LC network and hence eliminates the ringing. The on-chip metal interconnects provided the needed resistance. Transient

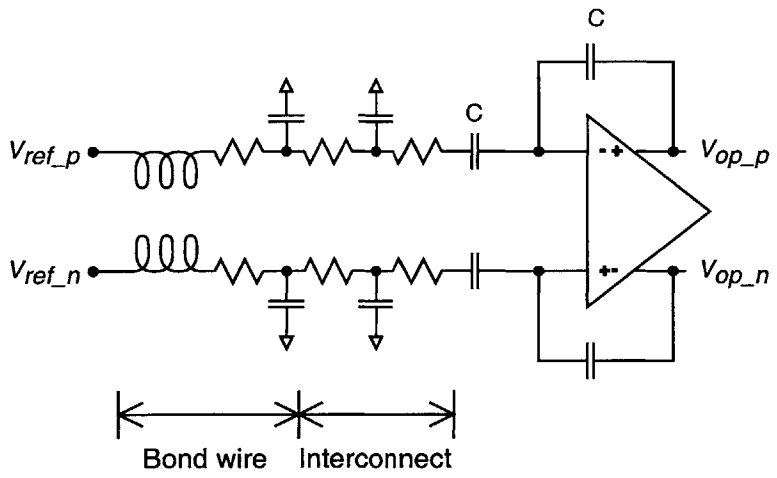


Figure 3-8: The resistance of the on-chip interconnects reduce the ringing in the references due to the bond wire inductance.

simulations using the model for a 100-pin TQFP package and the on-chip interconnects were carried out to verify that the references settle sufficiently fast. No on-chip reference voltage decoupling capacitance was used, because it was found to introduce a slow settling component due to the increase in the LC networks time constant. Slow settling components on the references must be avoided because they can cause input dependent modulation of the references and result in distortion [29]. Only when an impractically large on-chip capacitance was used, did the decoupling help provide a steady reference voltage.

3.3.3 Capacitor Sizing

The mean squared thermal noise sampled on each of the capacitors of the first pipeline stage at the end of the sampling phase is simply $\frac{KT}{C}$ [44], where K is Boltzmann's constant and T is the absolute temperature. When the pipeline stage opamp is placed in feedback in the multiply phase, this noise will appear in the output of the stage as $\frac{4KT}{C}$. The stage output will also contain noise due to the switches connected in the multiply phase and due to the opamp, both of which will be sampled by the next pipeline stage. The switch noise, which is referred to as the direct switch noise, is small and can be neglected [24]. The sampled

opamp noise will have a mean square value $\frac{1}{\beta}\frac{8KT}{3C_c}$, if the opamp is operated at a feedback factor of β and when a frequency compensation capacitor C_c is used [43]. The total mean squared noise voltage at the output of the first pipeline stage at the end of the multiply phase can therefore be written as:

$$\overline{v_n^2} = 4\frac{KT}{C} + \frac{1}{\beta}\frac{8KT}{3C_c} \tag{3.4}$$

If we neglect the parasitic capacitance at the input of the opamp then the feedback factor will be $\beta = 0.5$. Moreover, if assume that the compensation capacitor $C_c = 3C$, then we can write:

$$\overline{v_n^2} = \frac{52}{9}\frac{KT}{C} \tag{3.5}$$

If the pipeline stage capacitors are scaled by $\frac{1}{2}$, which results in an optimal design from a power consumption perspective [47], then the input referred root mean squared noise is:

$$\begin{aligned} \overline{v_{in}} &= \sqrt{\frac{52}{9}\frac{KT}{C}(\frac{1}{4} + \frac{2}{16} + \frac{4}{32} + \cdots} \\ &= \sqrt{\frac{26}{9}\frac{KT}{C}} \end{aligned} \tag{3.6}$$

For 12-bit performance with a 2V signal swing and an oversampling ratio of 4, the input referred noise must be smaller than $\frac{2}{2^{12}}\frac{2}{\sqrt{2}}\mathrm{V}_{rms}$, or $690\mu\mathrm{V}_{rms}$. To meet this requirement, 250fF capacitors are used in the first stage of the pipeline. This value gives a $\frac{KT}{C}$ thermal noise floor low enough to achieve a 70dB SNR at an oversampling ratio of 4. The calculation ignores the effect of the quantization noise floor, because it is much lower than the thermal noise floor due to the 15bit raw output of the converter.

3.4 Opamp Design

3.4.1 Opamp Topology

The 110Ms/s target sampling frequency of this design corresponds to a clock period of 9ns. Since this period needs to be divided into two non-overlapping phases, and within each of these phases an opamp needs to settle, one is left with about 4ns for opamp settling. Taking into account process variation, an opamp settling time of about 2ns is required under nominal conditions. Since the opamp is operating at a feedback factor around 0.5, for a settling time of 2ns to 12bit resolution, we need a settling time constant of τ =0.2ns or an opamp unity gain frequency of:

$$f_u = \frac{1}{2\pi\tau\beta} = \frac{2}{2\pi * 0.2ns} = 1.6 \text{ GHz} \tag{3.7}$$

In order to maintain the opamp non-dominant poles at a high enough frequency, the transit frequency f_t of the devices in the signal path need to be at least an order of magnitude greater that the unity gain frequency. f_t's in that frequency range can be obtained in the 0.35μm process, but only for NMOS transistor operated at a high gate drive (0.4V above V_t). In addition, transistors that are not in the signal path need to have f_t's about 3 times greater than the f_u, to ensure that the non-dominant poles due to the active loads are at a high enough a frequency where they don't perturb the settling time. This can be achieved from PMOS transistors when V_{gs} is at least 0.5V above V_t.

From the discussion above it can be concluded that the only NMOS devices should be used in the signal path [48]. Also, it can be concluded that a single stage design is not a possible candidate at a supply voltage of 3.3V, simply because the opamp will have a very small output swing. A single stage telescopic amplifier, for example, has a single ended swing:

$$\text{swing} = 3.3 - 3V_{d,sat,n} - 2V_{d,sat,p} - 5V_{margin} \tag{3.8}$$

where $V_{d,sat,n}$ and $V_{d,sat,p}$ are the drain to source voltages which cause pinch off, for NMOS

and PMOS transistors respectively. V_{margin} is the margin allowed in drain to source voltage above $V_{d,sat}$. If $V_{d,sat,n}$=0.4V, $V_{d,sat,p}$=0.5V and V_{margin}=0.2V then the opamp output swing will be only 0.1V.

The two stage design shown in figure 3-9 was chosen for the opamp. A telescopic amplifier with regulated cascode gain enhancement is used for the first stage. The second stage has a tail transistor in order to accommodate the large common-mode voltage at the output of the first stage. This tail transistor could be removed, but that would require operating the 2nd stage input transistors at a very large V_{gs} equal to:

$$V_{gs} = 3V_{d,sat,n} + 3V_{margin} \tag{3.9}$$

If $V_{d,sat,n}$=0.4V and V_{margin}=0.2V then V_{gs}=1.8V. This large V_{gs} will reduce the second stage input transistors g_m to I_D ratio, and will result in a significantly larger current in the 2nd stage. Another possible way to eliminate this tail transistor is to use an active wide-band level-shift stage between the 1st and 2nd stages, but this was found to degraded the step response of the opamp because of the additional high frequency poles introduced by this stage. Yet another way to remove the tail transistor is to use a capacitive level shift. In order for this level shift stage not to reduce the effective transconductance of the second stage, a very large level-shift capacitor (few pF) is needed to minimize the effect of capacitive voltage devision between the level shift capacitor and the input capacitance of the opamp 2nd stage. This is the primary reason this approach was not adopted.

Two methods were used to reduce the impact of the second stage on the step response of the opamp. First, the second stage was scaled up in order to reduce the effect of the opamp load capacitance on the primary non-dominant pole. This resulted in a second stage current of 20mA as opposed to 4mA consumed by the opamp first stage (these figures are for the opamp in the first pipeline stage). Second, the PMOS load transistors of the second stage, Mp13 and Mp14, were operated at a very large V_{sg} of 1.7V. This helps reduce the size of these transistors and their parasitic capacitance. Although the large V_{sg} results in a V_{dsat} of about 0.9V, it has no impact on the pipeline stage voltage swing, which is set by

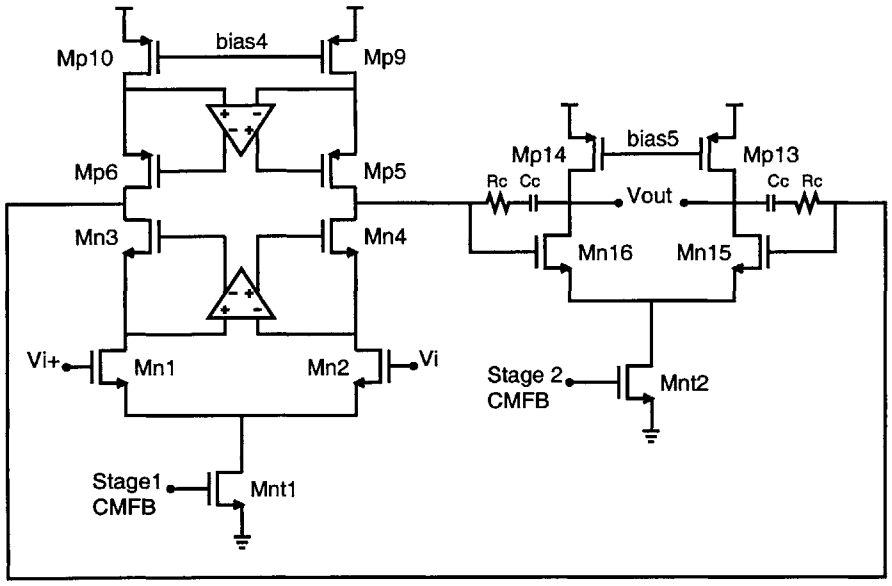


Figure 3-9: Simplified circuit diagram of the opamp.

the requirements of the NMOS switches.

Operating the transistors deep into strong inversion results in low transistor intrinsic gain, and hence low opamp gain. To compensate for this, gain enhancement was used [49, 50], and an opamp gain of 96dB was easily obtained. This value, which is much larger than what is needed for 12-bit operation. It allows for testing of the ADC at oversampling ratios higher than 4, where resolutions higher than 12-bits would be expected, without the performance being impaired by distortion. For example, if the ADC is tested at an oversampling ratio of 16 the expected resolution would be 13bits, and the opamp gain would still be large enough, and the steady state settling error would be small enough to obtain the desired results. The gain enhancement amplifiers have a folded cascode topology used in [51].

3.4.2 Common Mode Feedback Circuit

The common mode levels in the opamp are regulated using two independent loops; one for each stage. This approach was chosen over having a single loop around the opamp. A

single common-mode-feedback (CMFB) loop is ill conditioned due to the presence of the tail transistor in the second stage, which greatly reduces the common mode gain of the second stage. This implies that a large common-mode change at the first stage output is needed in order to achieve the desired control over the second stage output. As mentioned before, the first stage has a small output swing, making the single loop CMFB unworkable.

The maximum signal swing at the output of the first opamp stage, is on the order of 100mV. This allows for the use of the continuous time CMFB circuit in fig. 3-10, while maintaining sufficient linearity. The gates of transistors Mn_cmfb1 and Mn_cmfb2 are connected to the output of the first opamp stage. The drain terminals of these transistors are tied together. Since these transistors are operated in the triode region, the sum of their drain currents is proportional to the common-mode voltage of the first stage [52]. This common-mode current controls the first stage tail transistor, and hence regulates the output common mode of the first stage. The CMFB loop contains three inverting stages, two of which have a low gain and a high bandwidth. The transistors of the 1st opamp stage compose the 3rd stage in the CMFB loop, and are in the right hand side of fig. 3-10. The loop only contains a single high impedance node, located at the output of the 3rd stage, which sets the dominant pole. The loops non-dominant poles are at a very high frequency because the diode connected transistor Mpcmfb3 is biased with a Vsg=2V, and as a consequence the loop does not require frequency compensation. The low transconductance of Mpcmfb3 due to the large Vsg does not effect the loop gain.

The 2nd stage CMFB is the traditional switch capacitor design (figure 3-11) [44]. The only modification is the use of a source follower (transistors Mn158 and Mn159) to drive the input of the common-mode amplifier (the gate of Mt2). Without this source follower, the large gate capacitance of Mt2 coupled with the small CMFB capacitors results in a feedback factor of 0.1, which will reduce the loop gain to only 4. The low gain results in poor control over the output common mode, and simulations indicate that in steady state the common-mode output will be a few 100mV away from the desired value.

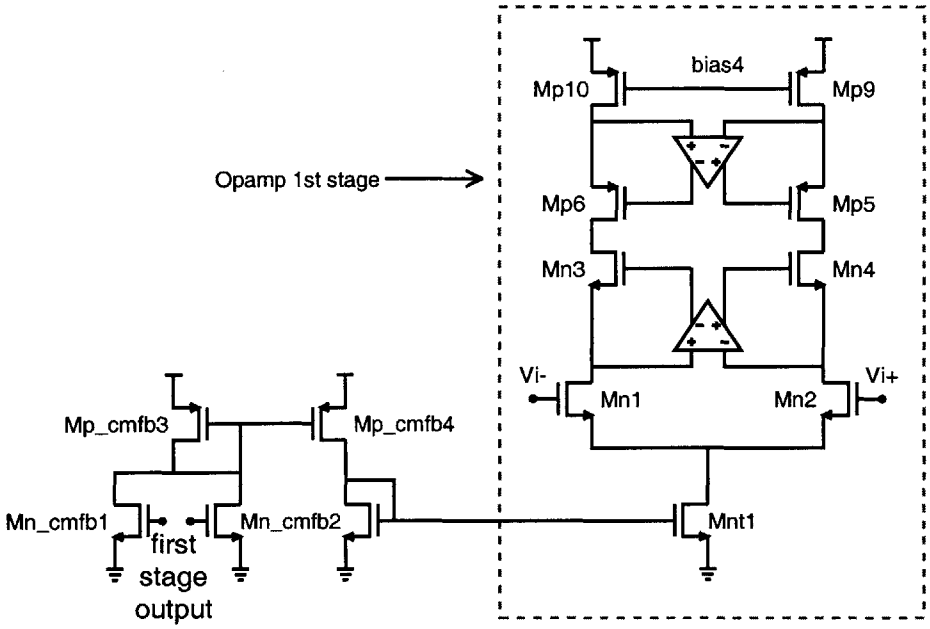


Figure 3-10: Simplified diagram of the CMFB circuit for the opamp's first stage.

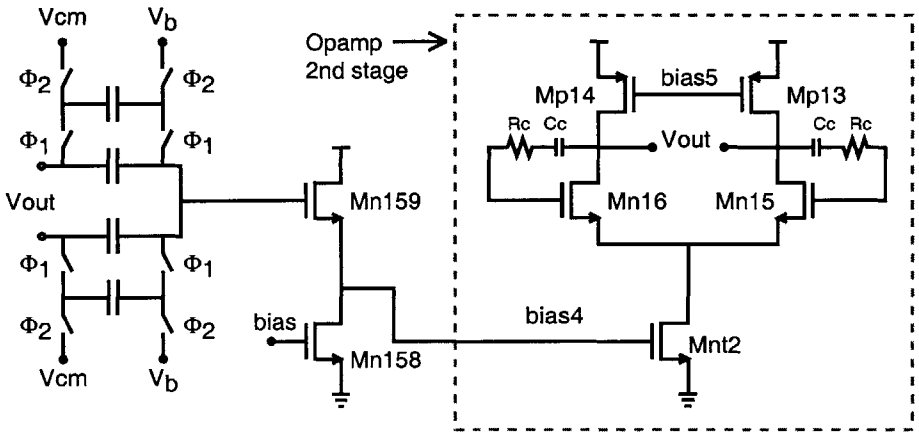


Figure 3-11: Simplified circuit diagram of the opamp's-2nd-stage CMFB.

Pipeline stage	Settling time (ns)	Settling accuracy (bits)	Gain	Power (mW)
1	1.85	12	65K	141
2	1.9	11	65K	77
3	1.9	10	62K	45
4	2.0	9	8K	28

Table 3.2: Summary of pipeline stages opamps performance.

3.4.3 Opamps in Latter Pipeline Stages

The opamps are scaled down by a factor of two in stages 2, 3 and 4 to save power. This scaling does not degrade the operating speed since the capacitors are also scaled. Continuing to scale beyond the forth stage would result in extremely small capacitors and was therefore avoided. In these remaining stages the same opamp as stage 4 is used. The only part of the opamp that is not scaled at all is the bias circuit, because it consumes relatively low power. All of these opamps operate at a feedback factor of $\frac{1}{3}$ as oppose to $\frac{1}{2}$ for the first stage. If we consider the open loop system of the opamp and the feedback network, reducing the feedback factor from $\frac{1}{2}$ to $\frac{1}{3}$ reduces the unity gain frequency of this system by $\frac{2}{3}$. To maintain the same unity gain frequency, the frequency of the dominant pole was increased by $\frac{3}{2}$, by reducing the compensation capacitor by $\frac{2}{3}$. This does not change the location of the nondominant poles and hence the same stability margins are maintained. In the ADC back-end, the requirements on opamp gain are more relaxed. The NMOS cascode gain enhancement amplifier was therefore removed in the 4th stage opamp.

3.4.4 Summary of Simulated Opamp Performance

Table 3.2 summarizes the simulated performance of the different opamps in the pipeline stages. Table 3.3 summarizes the performance of the first stage opamp in the presences of transistor mismatch.

Settling time (ns)	1.8
Offset voltage (mV)	3.1
DC Gain	53K
f_u (GHz)	1.6
Phase margin	49^o
CMRR (at DC)	72dB
CMRR (at f_u)	72dB
PSRR+ (at DC)	90dB
PSRR+ (at f_u)	72dB
PSRR- (at DC)	86dB
PSRR- (at f_u)	69dB

Table 3.3: Summary of the first pipeline stages opamp performance when device mismatch is included.

3.5 Comparator and Control Logic

Figure 3-12 shows the design of the first stage comparator. It is composed of a pre-amp with a gain of 4 followed by a latch [53]. The design is not a sampling comparator, as the input to the latch is continuous time. This results in the comparator having a dynamic offset and hysteresis [54]. To understand this consider the case where the ADC input is a 50MHz sine wave. Simulations indicate that the pre-amp delays the sine wave by 100ps. This delay results in a difference of about 20mV between the latch input and the value on the sampling capacitors, if the input is going through a zero crossing, as shown in fig. 3-13. This difference between the signal at the latch input and the signal sampled on the capacitor will result in a comparator decision error. Although the pre-amp delay is a function of the input frequency, the difference between the latch and sampling capacitor signals is also a function of the input amplitude. Moreover, the polarity of the difference is related to sign of the derivative of the input. So if the input is increasing the difference will be negative and if the input is decreasing the difference will be positive. All these dependencies will result in a dynamic offset and hysteresis in the comparator decision. Comparator errors will result in the opamp output going out of the ADC reference range. For a comparator dynamic offset

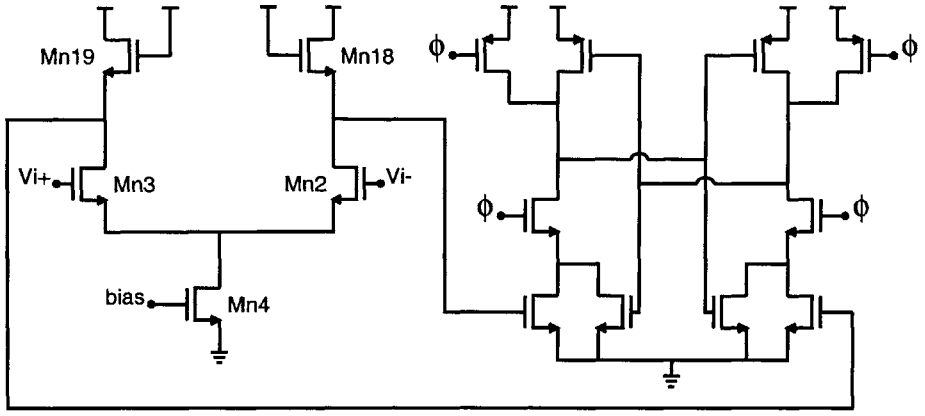


Figure 3-12: Simplified circuit diagram of the first pipeline stage comparator.

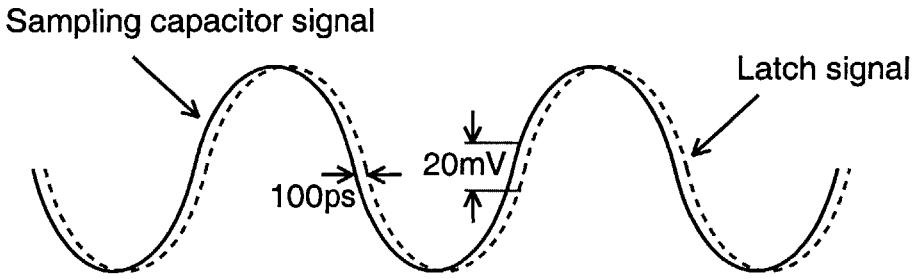


Figure 3-13: The preamp delay causes a difference between the signal at the sampling capacitors and the signal a the latch input.

of 20mV magnitude the opamp must settle fast enough. The comparator decision error will be taken care of by the digital error correction logic. This error mechanism imposes the limit on the maximum input frequency for this design. At low input frequencies the comparator decision errors are dominated by errors due to the static latch offset, caused by mismatch in the active devices and parasitic capacitances including layout capacitances. The estimated latch offset is about 30mV, which when referred to the comparator input becomes 7mV.

The logic circuits that follow the comparator implement the control signal logic equations using a modified form of domino logic shown in figure 3-14 [55]. The modification moves the late arriving clock ϕ to the nearest point to the output in order to speed the computation. The NMOS transistor connected to ϕ is usually placed at the bottom of the NMOS stack,

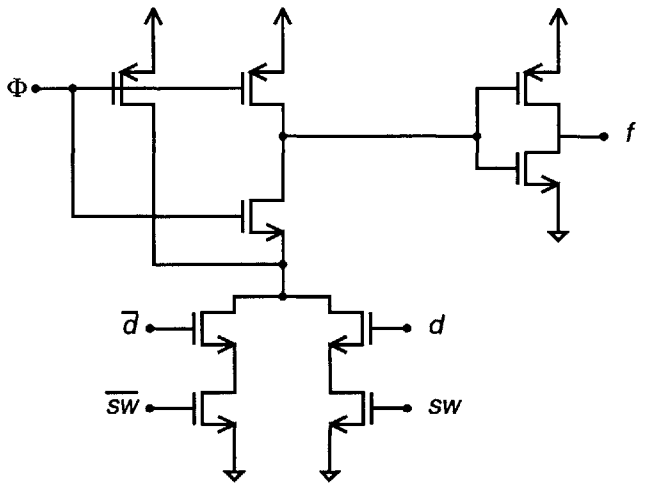


Figure 3-14: Modified domino logic used in the comparators.

but such a configuration was found to be slower. A small PMOS device is used to avoid charge sharing problems, at the expense of the possibility of a small static current.

3.6 Back-End Flash ADC

The flash ADC in the back-end generates 4 bits, plus overrange signals for digital error correction. The number of bits in the flash were selected with two considerations in mind: power and input capacitance. As the number of bits in the flash increase so does its input capacitance. Increasing the number of bits also allows for reducing the number of CFCS pipeline stages. This initially reduces the total power consumption, but since the number of comparators increases exponentially in the flash, a point is reached where the flash power dominates and the power consumption begins to increase. Table 3.4 demonstrates this result by tabulating the power-saved and input capacitance as a function of the number of bits in the flash.

Figure 3-15 shows the block diagram of the flash, which uses 15 comparator to generate a thermometer code. In addition two comparators are used to detect over-ranging. The references for all the comparators are generated using a resistor string. The thermometer code output of the comparators can be easily converted into a binary representation by

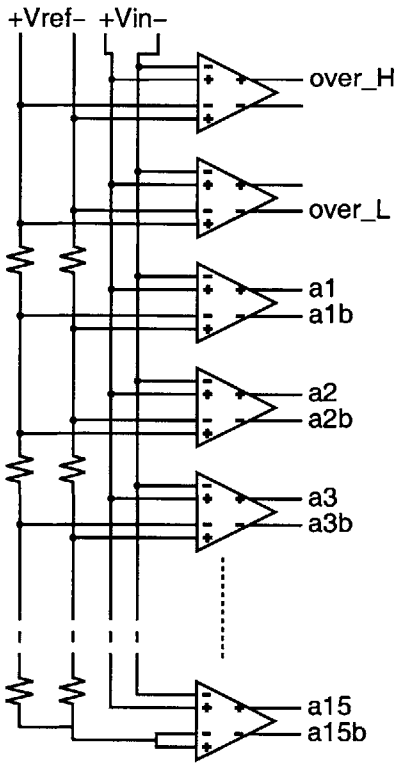


Figure 3-15: Simplified circuit diagram of the flash.

noting that the problem at hand is the same as parity generation, which can be implemented using XOR gates. The logic equations are as follows:

$$
\begin{aligned}
D3 &= a_{15} \\
D2 &= a_7 \oplus a_{15} \oplus a_8 \\
D1 &= a_3 \oplus a_7 \oplus a_{11} \oplus a_{15} \oplus a_{12} \oplus a_8 \oplus a_4 \\
D0 &= a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7 \oplus a_8 \oplus a_9 \oplus a_{10} \oplus a_{11} \oplus a_{12} \oplus a_{13} \oplus a_{14} \oplus a_{15}
\end{aligned}
$$

The XOR gates are implemented using differential cascade voltage switch logic (DCVSL) because of its simplicity, as shown in figure 3-16 [55]. The inputs to the XOR gate are only connected to NMOS transistors which reduces the input capacitance. Since the PMOS load capacitance is much smaller compared to static CMOS gate, the DCVSL XOR gate is faster.

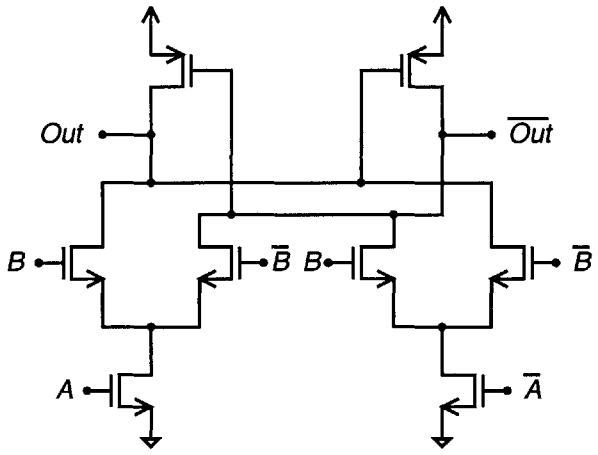


Figure 3-16: DCVSL XOR gate.

Flash bits	Power saved (mW)	Input capacitance (fF)
6	78	109
5	90	55
4	82	29
3	60	15
2	31	8
1	0	5

Table 3.4: The effect of the number of bits in the flash on the power saved and the input capacitance of the flash.

This logic family does require the complements of the inputs, but these are generated by the fully differential comparators.

3.7 Error Correction Logic

The error correction logic simply performs a binary weighted addition of the pipeline stages digital outputs. The operation is best explain through an example. Consider the case when the outputs of the pipeline stages are as follows:

Stage1 output	1													
Stage2 output	0	1	1											
Stage3 output	.	0	1	1										
Stage4 output	.	.	0	1	1									
Stage5 output	.	.	.	0	0	1								
Stage6 output	.	.	.	.	0	0	1							
Stage7 output	.	.	.	.	.	0	0	1						
Stage8 output	.	.	.	.	.	.	0	0	1					
Stage9 output	.	.	.	.	.	.	.	0	0	1				
Stage10 output	.	.	.	.	.	.	.	.	0	1	1			
Stage11 output	.	.	.	.	.	.	.	.	.	0	1	1		
Stage12 MSB's	.	.	.	.	.	.	.	.	.	.	0	1	1	
Stage12 LSB's	.	.	.	.	.	.	.	.	.	.	.	.	1	1 1
ADC output	10	0	1	1	0	0	0	0	0	1	1	1	0	1 1

The ADC output is the addition of the pipeline stages' outputs as aligned above. The alignment weights the stage outputs in a binary fashion, which is a natural consequence of the gain of 2 used in the pipeline stages. The result is a 16-bit number, but contains only 15 bits of information, since there is a fixed offset in the ADC output. To understand this consider the case when the ADC input is $-V_{ref}$. All the ADC stages will detect a zero which is represented as 001. Clearly the output of the ADC will not be zero, rather it will be 001111111111100(recall that the stage output is 000 only when the stage under-ranges). When the ADC input is V_{ref}, all stages will detect a 1, which is represented as 011, and the ADC output will be 1001111111111011. The difference between the digital output for V_{ref} and $-V_{ref}$ is 111111111111111, and contains 15-bits of information.

Since three numbers are added by the error correction logic 2 adders are needed. The addition must be completed within one clock cycle of 9ns. To verify that the adders meets the timing requirement, the adders were tested with the following worst case input:

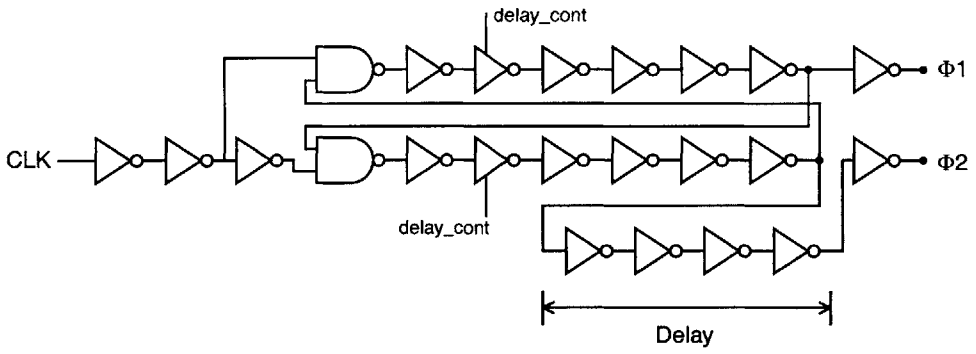


Figure 3-17: Clock generator.

Stage1 output	0													
Stage2 output	0	1	0											
Stage3 output	.	1	1	0										
Stage4 output	.	.	1	1	0									
Stage5 output	.	.	.	1	1	0								
Stage6 output	.	.	.	.	1	1	0							
Stage7 output	.	.	.	.	.	1	1	0						
Stage8 output	.	.	.	.	.	.	1	1	0					
Stage9 output	.	.	.	.	.	.	.	1	1	0				
Stage10 output	.	.	.	.	.	.	.	.	1	1	0			
Stage11 output	.	.	.	.	.	.	.	.	.	1	1	0		
Stage12 MSB's	.	.	.	.	.	.	.	.	.	.	1	1	1	
Stage12 LSB's	.	.	.	.	.	.	.	.	.	.	.	.	1	0 0
ADC output	1	0	1	1	1	1	1	1	1	1	1	1	0	0 0

which corresponds to adding the following numbers:

0	0	0	0	0	0	0	0	0	0	0	0	1		
0	1	1	1	1	1	1	1	1	1	1	1	1		these two numbers causes a carry to ripple
0	0	1	1	1	1	1	1	1	1	1	.	.	+	this number causes a carry delete to ripple
1	0	1	1	1	1	1	1	1	1	1	0	0		

Simulation results indicate that this addition is completed in 3.3ns.

3.8 Clock Generation and Distribution

A two phase clocking methodology was adopted in this design. The clock phases are generated using the conventional two phase clock generator shown in figure 3-17 [56], which has the output waveforms shown in figure 3-18. The non-overlapping period between the falling

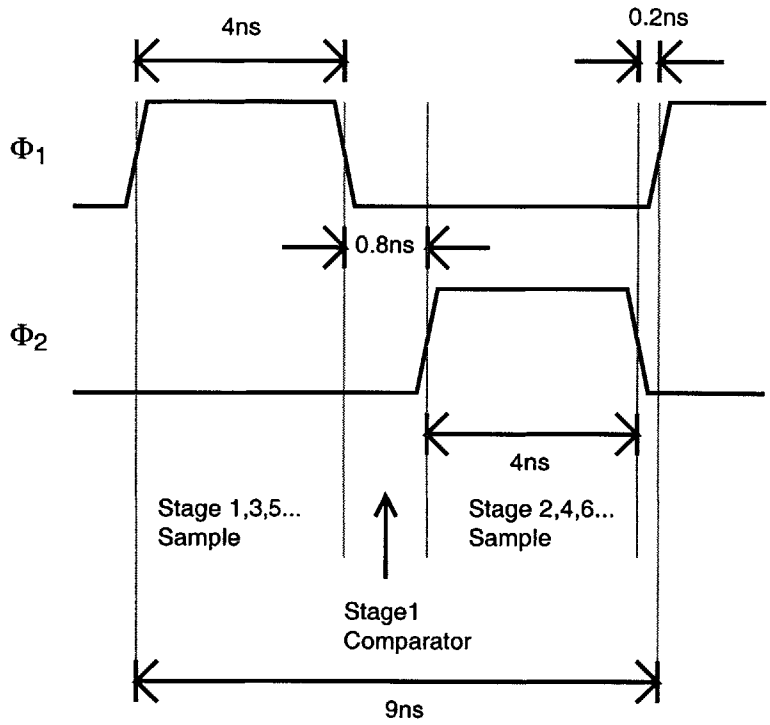


Figure 3-18: Clock phases generated by the clock generator.

edge of Φ1 and the rising edge of Φ2 is longer than the non-overlapping period between Φ2 and Φ1. The reason behind this choice is related to the first stage comparator which is enabled on the falling edge of Φ1 and has to reach a final value before the beginning of Φ2. Nominally the time allocated for this comparison is 0.8ns, and can be increased using the input delay_cont which decreases the current in a current starved inverter. This can be used to increase the time allocated for the comparator.

In the first iteration of the clock generator design, all the phases derived from Φ1 and Φ2 were generated at a single location and then distributed all over the chip with no buffering of the clocks at the pipeline stages. The main short coming of this approach was that it required the clock generator output to drive capacitive loads ranging in value from a few 100fF to a few pF, using interconnects as long a 3mm which were periodically loaded as shown in fig. 3-19. The interconnect resistance degraded the rise time of the clock phases for the heavily loaded lines, creating severe skew problems. For example, it was found that

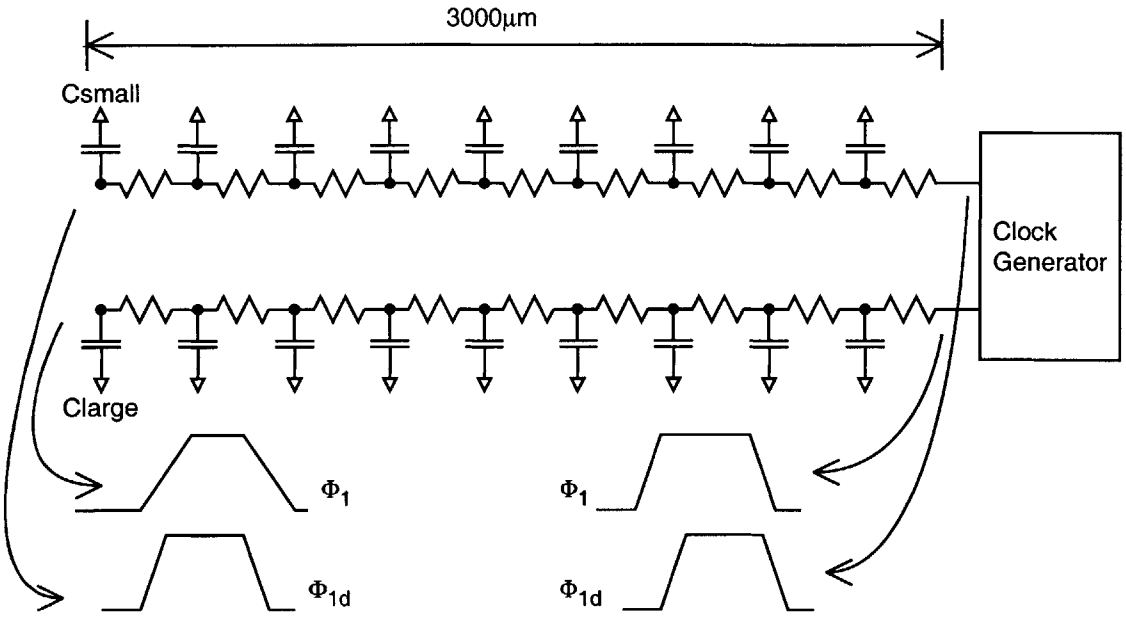


Figure 3-19: Clock skew is caused by the interconnect resistance.

after passing through the interconnect, $\Phi 1d$ was no longer a delayed version of $\Phi 1$, but actually arrived before it, as can be seen in the waveforms in the left hand side of fig. 3-19.

To overcome the clock skew problem, the generation of the phases was moved to the pipeline stages, with every two stages sharing a common phase generator. Only $\Phi 1$ and $\Phi 2$ are distributed all over the chip, and they drive only a small load capacitance composed of the inputs to the phase generators. Using this approach assures that no clock skew problems arise.

One last point to mention is that the phase generators produce the clock phase that enables the comparators. In the stages that follow the first stage, this comparison is done 1ns into the sampling phase, and it can be delayed using a current starved inverter.

3.9 Output Pad Drivers

The outputs of the error correction logic circuit cannot directly drive the package and the off-chip impedance. To help accomplish this, pad drivers are used. These drivers, shown in

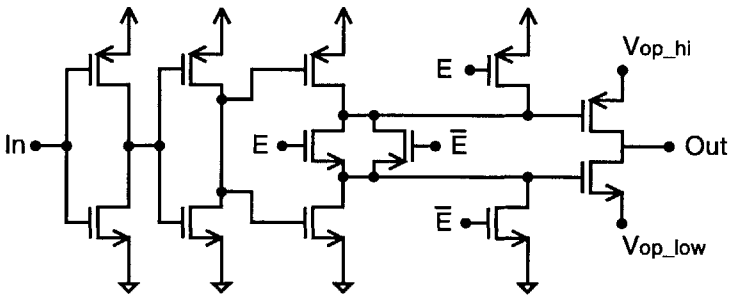


Figure 3-20: Low output swing pad driver.

fig. 3-20, are composed of a string of inverters, which are scaled up progressively, such that the final inverter has a current drive large enough to drive the load impedance. When the enable input E is low, the driver output is in tri-state. To allow for the reduction of the swing of the output signal down to 0.3V, the last inverter is connected to a different supply (V_{op_hi}) and ground (V_{op_low}). Reducing the output swing reduces the charge that needs to be transfered to the load capacitance when the output transitions, greatly reducing the power consumption of the drivers. Reducing the amount of charge that the output transistors must deliver also reduces the charge these transistors inject into the substrate because of impact ionization in the transistor channel. This help reduce substrate noise which could impact the sensitive analog circuits.

The pad drivers were simulated with the model for a 100pin TQFP package, and an off-chip load capacitance of 20pF. An off-chip series termination resistor is need in order to minimize the ringing on the load capacitance when long circuit-board transmission lines are used.

3.10 Mismatch Shaping Sequences

To allow for the testing of different mismatch shaping algorithms and to allow for maximum flexibility during testing, the swapping sequences are not generated on-chip, but rather are loaded on to the test-chip during full speed testing from an off-chip SRAM. New swapping sequences can be easily generated in software and then loaded into the SRAM, without

the need to modify the hardware. The test-chip has four inputs for the mismatch shaping sequences, which are sw_{all}, sw_1, sw_2 and sw_3. These correspond to the sequences in the test-chip block diagram in fig. 3-2. These four sequences allow for the test-chip to be operated in three main modes, which encompass all the algorithms described in the previous chapter. These modes are:

1. CFCS mode: here all the mismatch shaping sequences will be set to one (or zero).
2. ADC swapping: here only the sw_{all} input will be used and sw_1, sw_2 and sw_3 will be set to one.
3. Individual stage swapping: here sw_{all} will be set to one and sw_1, sw_2 and sw_3 can be used for the mismatch shaping. sw_1, sw_2 and sw_3 are applied to pipeline stages 1,2 and 3 respectively. Furthermore, sw_3 is buffered and delayed on-chip and applied to stages 4, 5, 6 and 7. This is done in a manner that insures that as a sample propagates through the pipeline it will go through stages using the same value for the swapping sequence.

3.11 ADC Simulation

Simulating the entire ADC posed a considerable challenge. The objective is to run simulations that demonstrate the proper operation of the converter. This entails using parasitic capacitors and resistors extracted from the layout. It also requires using proper models for the chip package and for the circuits external to the chip. The netlist to be simulated is huge. Moreover, the simulations must be done at high tolerance levels, which are needed to verify the 12-bit operation. The high tolerance levels result in small transient simulation time steps. Running such a simulation, unfortunately, requires an infeasible amount of computing time and storage space. A Sun Ultra60 workstation with over 1GB of swap space was only able to simulate a portion of the ADC for about 60ns. The portion simulated included the pipeline stages, the clock generator and the digital error correction logic. A simulation was run using a DC input of -15/16. The simulation output was 0010001111111100,

which agrees with the expected output. The simulation was repeated with another DC input (878.90625mV), resulting in an output of 1001100000101100, which is slightly different from the expected value of 1001100000111011. The error (1111) is most likely due to the tolerance settings of the simulation, which caused an error in the output of the flash. Resimulating at a higher tolerance was not feasible because of storage limitations.

To reach some degree of confidence in the simulations, the ADC netlist was split into overlapping sets. Each of these sets was verified individually. Since the sets overlap the possibility of interface problems between the sets is eliminated. In addition, since each of the individual netlist sets simulate properly, this approach suggests that if a complete netlist simulation were run, it would provide the desired results.

3.12 ADC Layout

The test-chip layout is shown in fig. 3-21. Considerable care was taken to minimize the noise coupling between the noisy digital nodes and the sensitive analog nodes. This coupling can occur through the chip package, the substrate and through the interconnects. To reduce the effect of coupling through the package, the digital inputs and outputs were place at the opposite end of the chip from the sensitive analog signals. This also helps reduce the interference at the test-board level since a natural isolation exists between the analog and digital portions. Physical isolation was also used inside the test-chip to reduce the noise coupled through the substrate and to separate the noisy signals such as the pipeline stage outputs from the analog signals such as the ADC references. This can be seen in the layout of the pipeline stage in fig. 3-22. Analog and digital supplies were also isolated. Nevertheless, the digital supplies need to be quiet because any noise on them would impact the clock generators and can result in clock jitter. To reduce this possibility, a 10nF on-chip decoupling capacitor is used. This capacitor is composed of an array of 12μm by 12μm unit NMOS capacitors operated in inversion. The large gate length of these capacitors results in a low quality factor which helps prevent any ringing on the supplies because of the LC network formed with the bondwires.

The most critical aspect of the layout is the layout of the analog circuits. Great care was taken in maintaining a symmetrical layout. Asymmetry in the layout can have a devastating effect on the performance of the converter. For example, the comparator latch is extremely sensitive to mismatch in its capacitive load. Any mismatch in capacitance between the two half circuits of the fully differential latch, will translate into an offset voltage. An asymmetrical layout can cause offset voltages on the order of a few hundred millivolts.

The opamp layout is also very important. The opamp's differential inputs were completely shielded to avoid stray coupling from other nodes. Asymmetrical coupling to the opamp's differential inputs from the control signals can cause differential nonlinearity errors, which would otherwise not appear in a CFCS converter. For example, if the control signal "a" in fig. 3-4 couples asymmetrically to the opamp input, then the opamp will have an offset which depends on "a". Since "a" depends on the stage decision bit "d", the offset will also depend on "d". Such an offset in the first pipeline stage will cause a DNL error in the middle of the transfer characteristic of the converter. Another reason the opamp inputs must be shielded is to eliminate any stray capacitive coupling between the opamp output and its input. A stray capacitance between these two nodes is a fixed capacitor around the opamp, and will result in a stage gain error causing differential nonlinearity. This error will not be removed by mismatch shaping and may render the technique useless. Shielding the opamp inputs helps avoid these problems, but it does increase the capacitance at these inputs resulting in smaller feedback factors and lower clock speeds. This shield was added in a second version of the test-chip layout and reduced the clock speed from the initial design of 110MHz to about 85MHz.

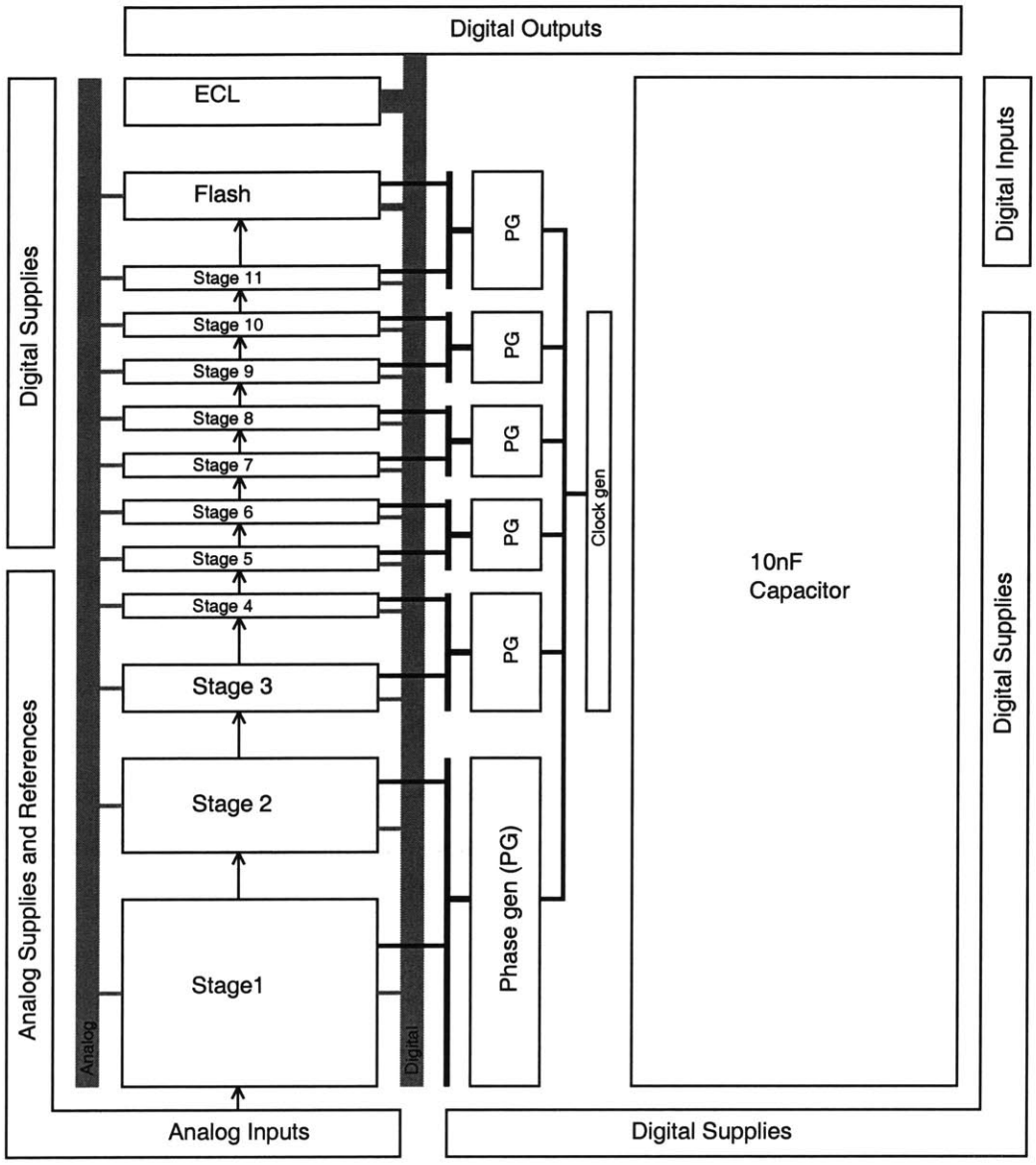


Figure 3-21: Chip layout.

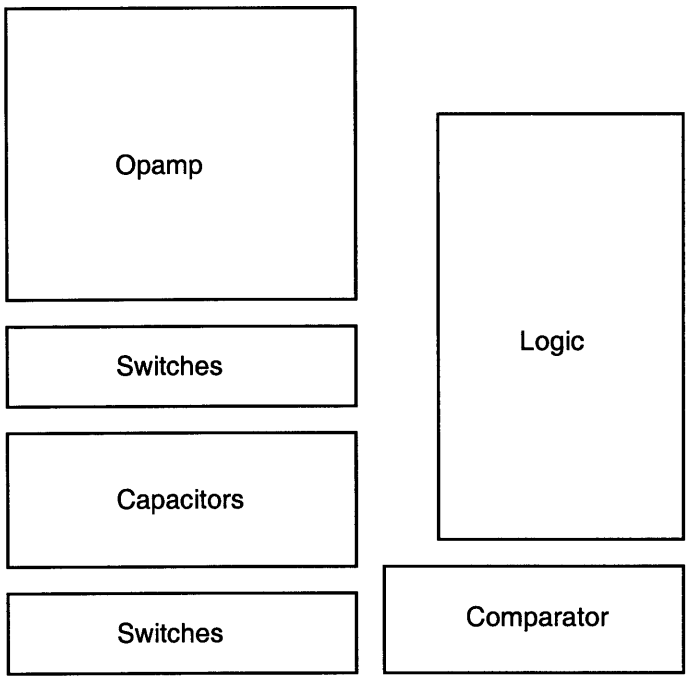


Figure 3-22: Pipeline stage layout.

Chapter 4

Experimental Setup and Results

The test chip described in the last chapter was fabricated in TSMC's 0.35μm CMOS process. Fig. 4-1 shows the microphotograph of the chip. Here the experimental results obtained from this chip are presented. The chapter presents an overview of the laboratory setup used in obtaining the results. This is followed by results obtained from the test chip which demonstrate the mismatch shaping techniques presented in chapter 2.

4.1 Experimental Setup

A simplified block diagram of the test setup is shown in fig. 4-2. At the center of the experimental setup is the ADC test board, which contains the test-chip. The analog signal source and clock source provide inputs to the test board. The experimental setup is controlled by a PC through a digital I/O card. The PC is also used to acquire the ADC data from the test board.

The analog signal source provides a sinusoidal input to the ADC. When observing the ADC output spectrum, the noise and distortion in the input source is indistinguishable from the noise and distortion introduced by the ADC. Therefore, the analog source must have noise and distortion significantly below that of the ADC. To achieve this goal, a low phase noise synthesized signal generator (AT8662A) is used. This signal generator has strong

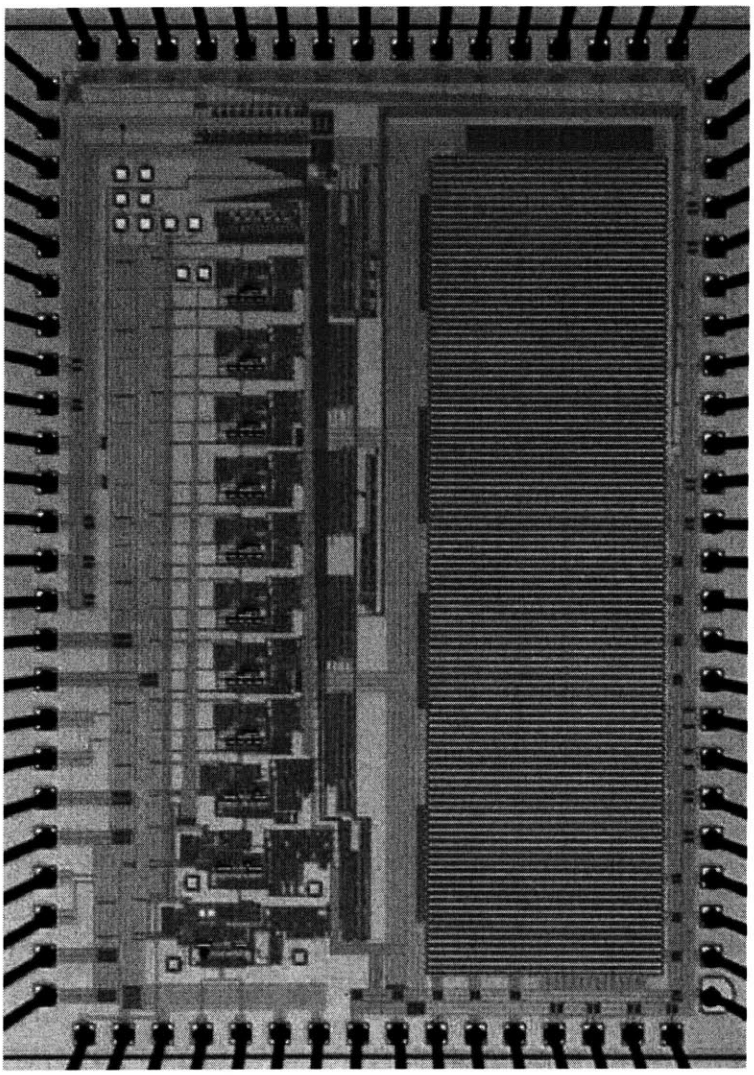


Figure 4-1: Test chip micro-photograph.

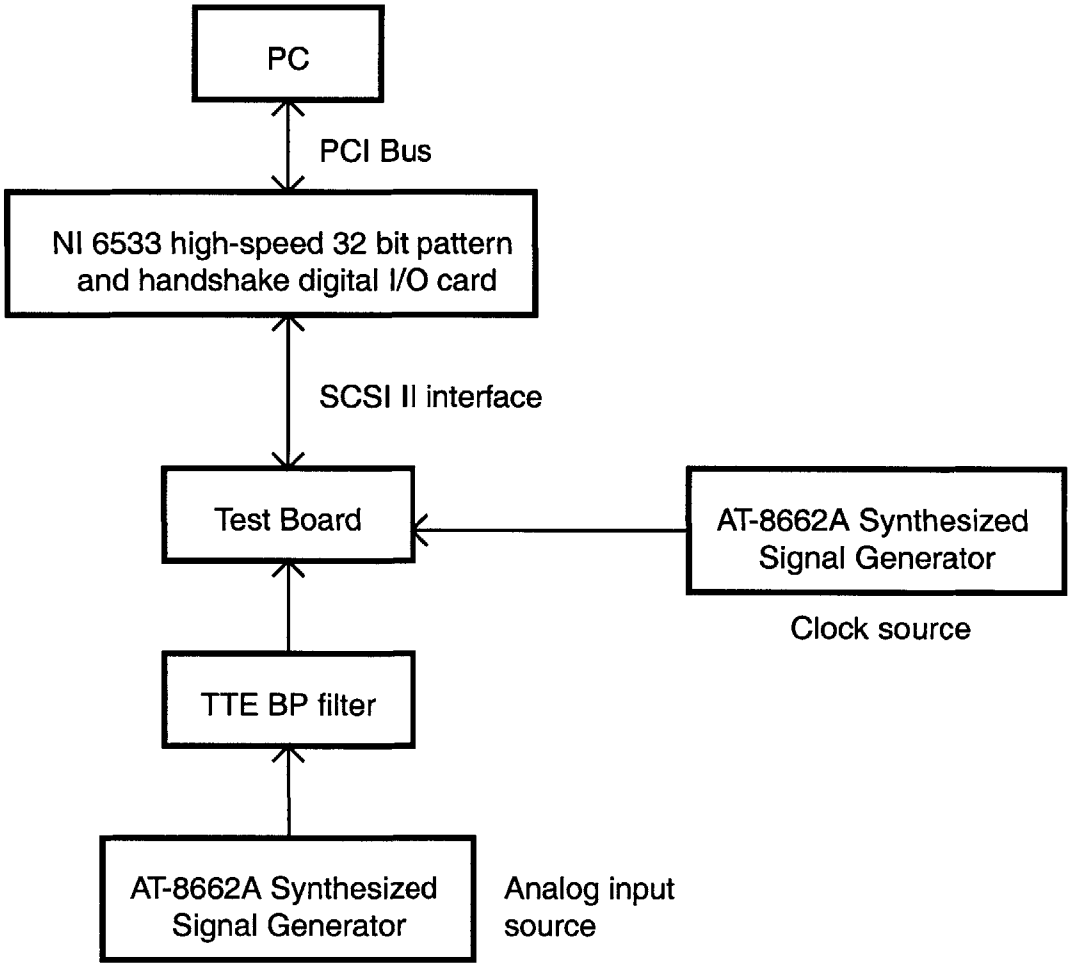


Figure 4-2: ADC test system.

harmonic distortion which are suppressed using a TTE narrow-band bandpass filter. Even with such a high spectral purity input source, it is possible for the input to be corrupted by noise which is electromagnetically coupled into the input path. To avoid this the input path consists of shielded coaxial transmission lines and circuit board micro-stripline transmission lines.

Low jitter in the clock source is also of utmost importance [57, 58, 59]. If the input source varies with time, then the clock jitter makes the value of the sampled input deviate from the ideal. This introduces errors into the sampling process and causes distortion. If the input is a sinusoid with an amplitude A and frequency ω then for a errors less than one LSB at the n-bit level the clock jitter must satisfy [58]:

$$\text{Jitter} < \frac{2^{1-n}}{A\omega} \tag{4.1}$$

If the input source has a 2V amplitude and a 40MHz frequency, and the resolution is 12-bits, then the jitter must be less than 1ps. A synthesized signal generator (AT8662A) was found to meet these jitter requirements.

The test board block diagram is shown in fig. 4-3. This 6-layer PCB contains the ADC test-chip. It also contains analog references, which provide the ADC bias current and the ADC references. These are generated using bandgap references(AD589), which are buffered using low-noise amplifiers(SSM2135). These references are low noise, low impedance and are able to drive their loads without drooping or instability [57, 58, 59].

The data acquired from the ADC is stored in a 512KB SRAM, while another SRAM stores the swapping sequence (*sw* SRAM). The address for the SRAM's is provided by an ECL counter. The board also contains Low Voltage Differential Signaling (LVDS) receivers (Rx) to convert the low swing signals into 3.3V CMOS digital signals. The low swing signals include the ADC outputs, the clock source and ECL counter output.

To obtain a fully differential input for the ADC from the single-ended source, a transformer with a 1:2 turns ratio is used. The transformer provides voltage amplification to the input. This allows for the input source to be operated at lower signal levels, where lower

distortion figures are possible. A 200Ω termination resistor is connected to the secondary side of this transformer, and provides a 50Ω termination when the resistance is referred to the primary side.

The clock is distributed across the test board using 50Ω micro-stripline transmission lines. The effect of reflections was minimized by using series termination resistors [60]. Series termination resistors were also used on all the high speed digital lines. To maintain proper timing across the test board the impact of the delays introduced by the transmission lines is taken into consideration. Delay element are introduced into the clock path to guarantee proper timing. These delay elements are simply transmission lines with lengths set to values that give the needed delay [60]. Transmission line delay elements offer precise control over the delay value. Active discrete delay elements, such as buffers, are unable to provide the short delays needed, which are in the order of 1ns. Moreover, they suffer from poor control over the delay value because of variations in the fabrication process, which result in the maximum possible delay being about 5 times larger than then minimum expected value.

To acquire data from the test chip experimental setup goes through the following test sequence. Initially, the *sw* SRAM is placed in the write mode and is loaded with the swapping sequences. Then the *sw* SRAM is placed in the read mode and the data SRAM in the write mode, to prepare for data acquisition. Data acquisition occurs a full speed driven by the clock source. During this phase the swapping sequence is loaded into the ADC from the *sw* SRAM and the ADC output data is loaded into the data SRAM. The acquisition ends when the 512Ksample data SRAM is full. Finally, the ADC data which is stored in the data SRAM, is read into the PC where it is analyzed. This entire sequence is controlled using the NI6533 I/O card which is driven from LABVIEW 5.0.

4.2 Experimental Results

In the following the measured output spectrum of the ADC will be presented under various mismatch shaping conditions. All these measurements are performed at a sampling rate f_s

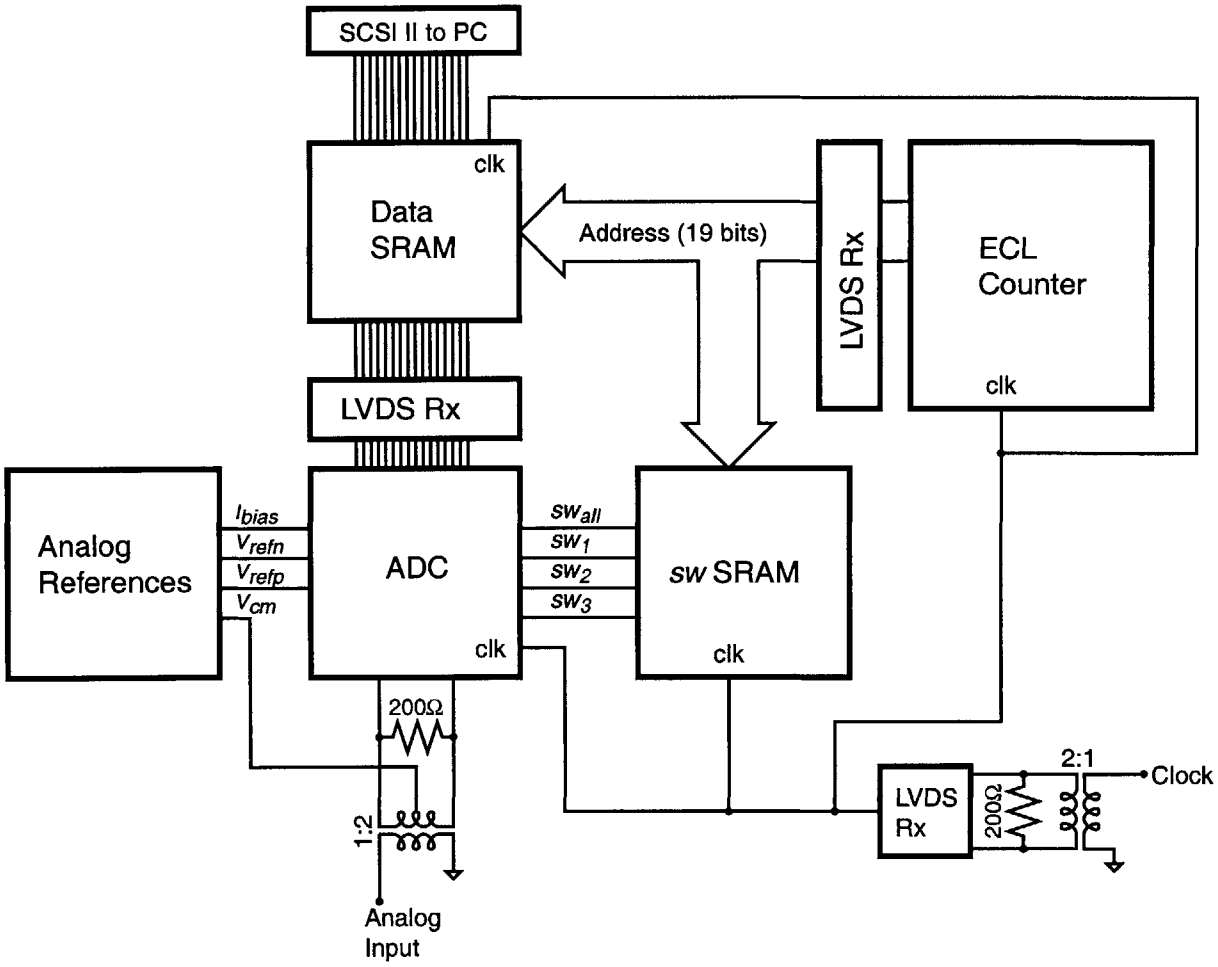


Figure 4-3: Test board block diagram.

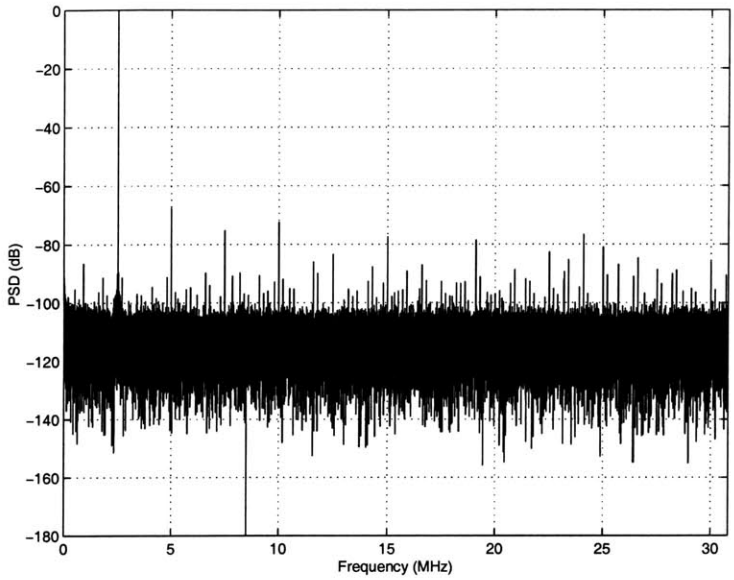


Figure 4-4: CFCS ADC: SNDR=64.1dB, SFDR=67.5dB, f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

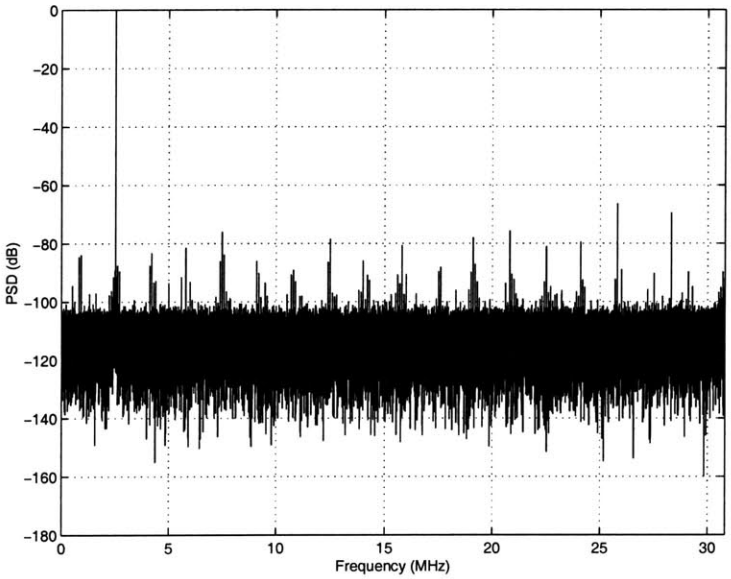


Figure 4-5: Mismatch shaped CFCS ADC using $sw_{all} = (-1)^n$: SNDR=67.4dB, SFDR=76dB, f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

of 61.6MHz and using a single-tone input frequency f_{in} of 2.5MHz. The two tone test used to obtain the simulation results was not used, because of the practical difficulties associated with generating the tones with the desired spectral purity. A 2.5MHz input was found to be a good compromise, since it is at a relatively high frequency, yet the dominant 2nd and third harmonics are in the signal band. The ADC reference was reduced by 3dB, to avoid what appears to be an opamp saturation problem due to an over-ranging comparator with large offset. This reduces the expected SNR by 3dB to 67dB.

A CFCS ADC with no mismatch shaping has the measured output spectrum shown in fig. 4-4. The measured SNDR is 64.1dB and SFDR is 67.5dB at an OSR=4. On the other hand, a mismatch shaped CFCS ADC using the swapping sequence $sw_{all} = (-1)^n$, has an output spectrum shown in fig. 4-5. The measured SNDR is 67.4dB and SFDR is 76dB at an OSR=4. This demonstrates an SNDR improvement of 3.3dB and an SFDR improvement of 8.5dB. As expected the 2nd and 4th harmonics have been modulated to half the sampling frequency, and the SNDR becomes thermal noise dominated. The dominant inband harmonic is now the third harmonic, which is caused mainly by signal dependent charge injection in the sampling circuits, and is unaffected by mismatch shaping as expected.

When mismatch shaping is applied using the swapping sequence sw_{all} with a spectrum shown in fig. 2-29, the ADC output spectrum shown in fig. 4-6 is observed. The measured SNDR=60.3dB at an OSR=4. The SNDR degrades by 3.8dB as compared to a CFCS ADC. The coloring of the in-band noise floor is inconsistent with the theory. At f_s=51MHz the noise floor rises in the entire signal band as shown in fig. 4-7. Reducing the input frequency to 475KHz does not change the noise floor as can be seen in fig. 4-8. Only at sampling frequencies below 25MHz do the results agree with the theory. Fig. 4-9 and fig. 4-10 respectively show the output spectrum at f_s=25.7MHz for the ADC without mismatch shaping and with mismatch shaping using a noise shaped sequence. The degradation at high sampling rates is not likely to be due to high order distortion components, because changing the input frequency does not effect the noise floor. Moreover, it is unlikely that the dynamic errors in the comparator cause this problem since it would be a function of the

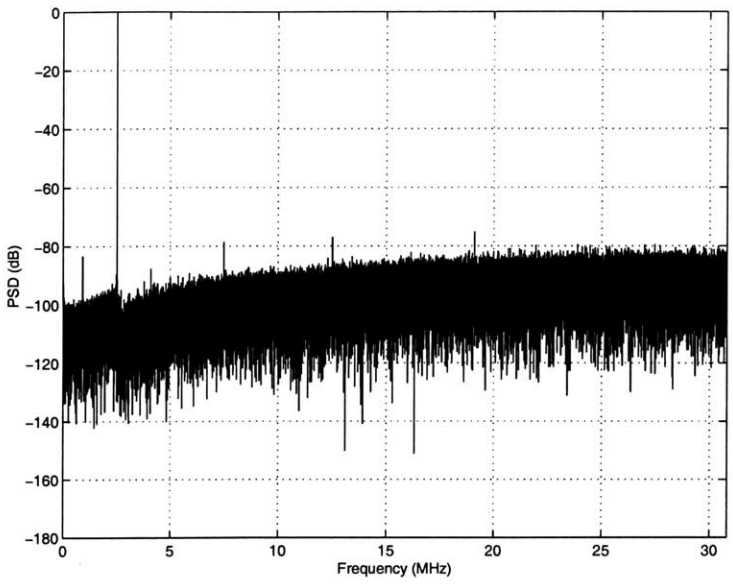


Figure 4-6: Mismatch shaped CFCS ADC using sw_{all} shown in fig. 2-29: SNDR=60.3dB, SFDR=78.5dB, f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

input frequency. The coloring of the noise floor is most likely due to the coupling of digital noise into the analog signal path on the test chip.

To verify this hypothesis, the digital output spectrum in fig. 4-8 was first passed through a notch filter to remove the input. This resulted in the spectrum shown in fig. 4-11. The output of the notch filter is multiplied with the swapping sequence to produced the PSD in fig. 4-12. The process of removing the input and multiplying by the swapping sequence has allowed us to expose the even order distortion components introduced by the ADC. The odd order distortion components, on the other hand, have been convolved with the spectrum of the swapping sequence. The first observation that can be made is that the even order distortion components are not particularly high. This confirms that the coloring of the noise floor is not due to the convolution of the even order distortion components with the spectrum of the swapping sequence. The second observation that can be made here is that the colored noise floor in fig. 4-12, does not correspond with what would be obtained by convolving the odd order distortion components in fig. 4-11 with the swapping sequence. From this it can be concluded that the coloring of the noise floor is definitely

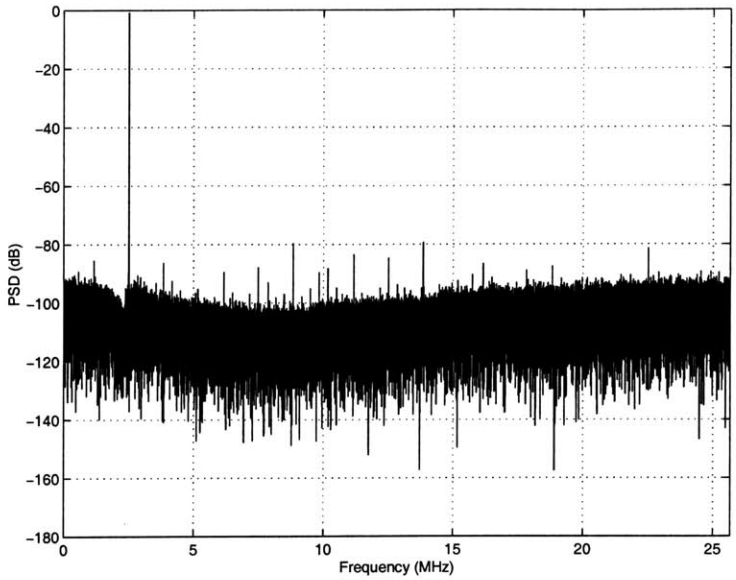


Figure 4-7: Mismatch shaping of CFCS ADC using sw_{all} shown in fig. 2-29: SNDR=62.1dB, SFDR=85dB, f_s=51.3MHz, f_{in}=2.5MHz and OSR=4.

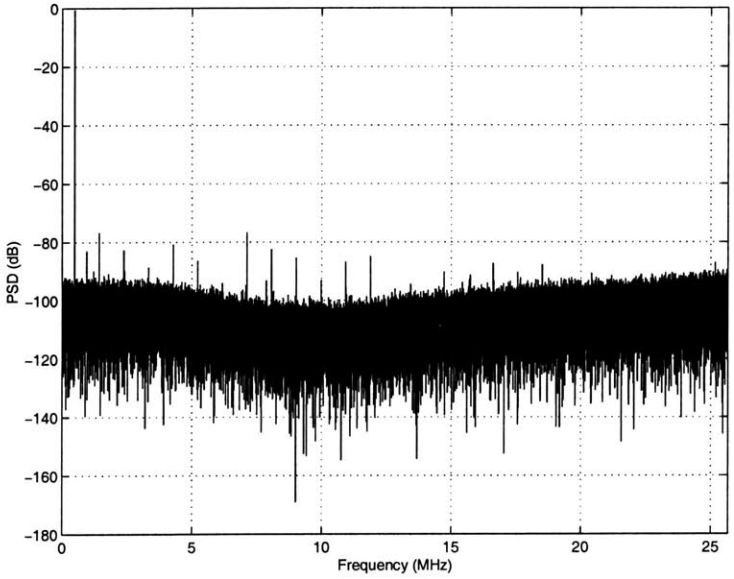


Figure 4-8: Mismatch shaping of CFCS ADC using sw_{all} shown in fig. 2-29: SNDR=60.6dB, SFDR=76.8dB, f_s=51.3MHz, f_{in}=0.475MHz and OSR=4.

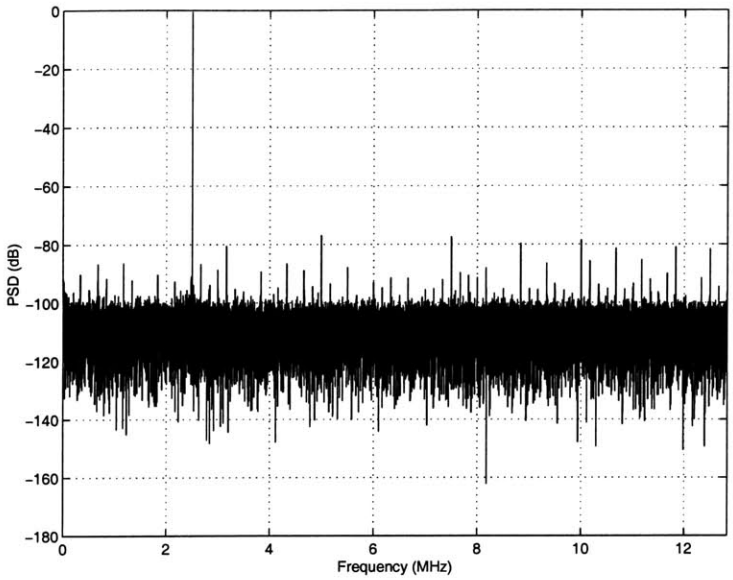


Figure 4-9: CFCS ADC: SNDR=67dB, SFDR=80dB, f_s=25.7MHz, f_{in}=2.5MHz and OSR=4.

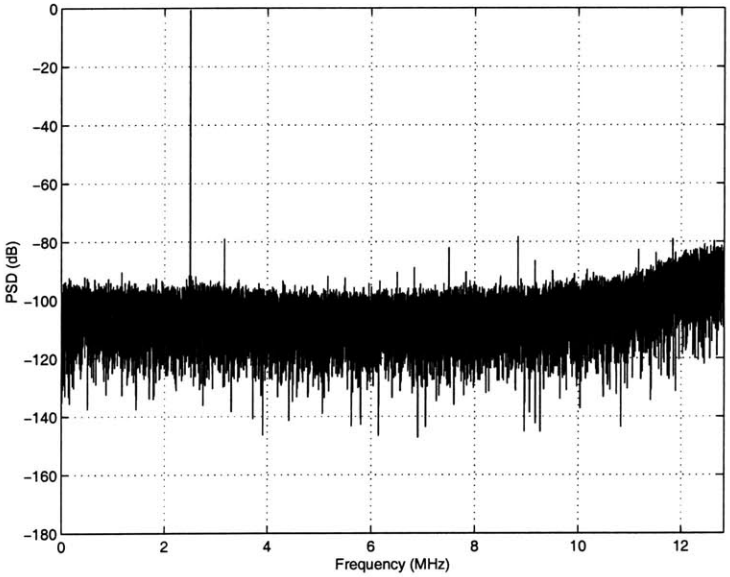


Figure 4-10: Mismatch shaping of CFCS ADC using sw_{all} shown in fig. 2-29: SNDR=64.5dB, SFDR=78.5dB, f_s=25.7MHz, f_{in}=2.5MHz and OSR=4.

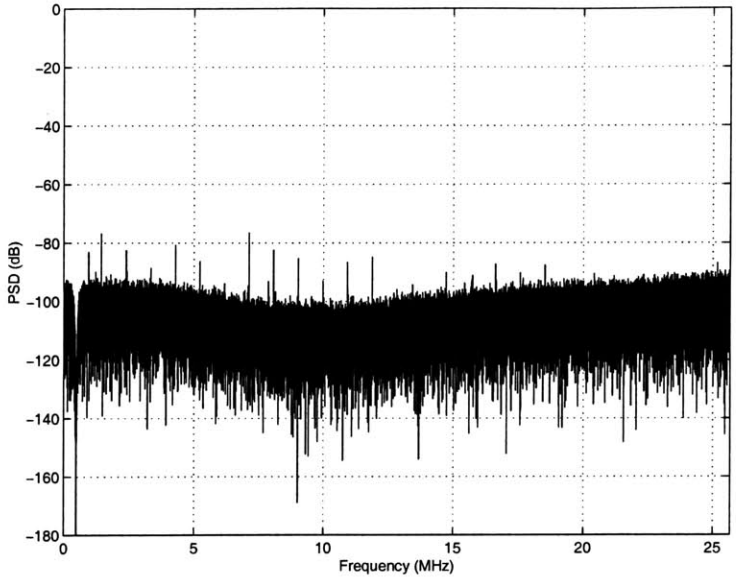


Figure 4-11: The input signal in fig. 4-8 has been removed using a notch filter.

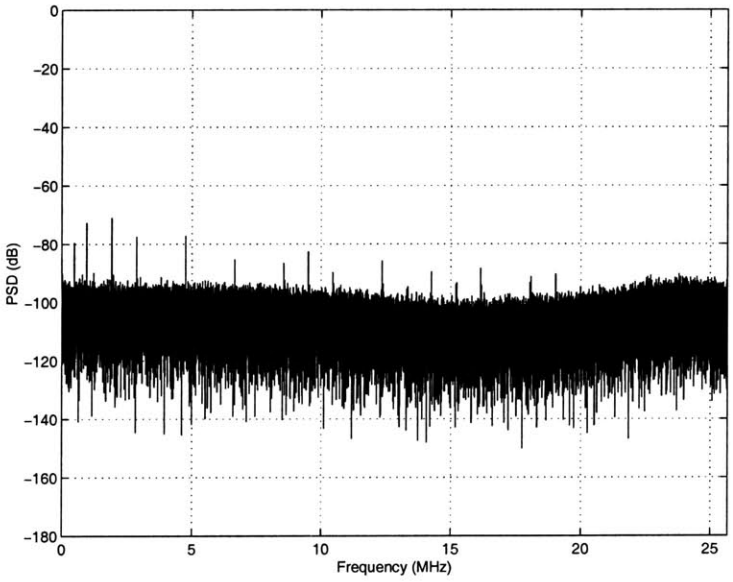


Figure 4-12: The spectrum in fig. 4-11 is convolved with the spectrum of the swapping sequence in fig. 2-29.

not due to distortion. Since the spectral purity of the input source is known, the only remaining possibility is that the observed noise floor in fig. 4-8 is due to noise coupling on-chip. Reducing the amplitude of the input signal was found to reduce the amplitude of the distortion, which leads us to suspect that the on-chip digital logic that processes the ADC output is impacting the analog signal, since a larger input amplitude will result in more digital activity. The data from the CFCS ADC is re-multiplied by the swapping sequence off-chip and the on-chip logic operates on the raw output of the CFCS ADC. The raw output will be noised shaped and therefore it is reasonable to expect that the noise coupled to the analog signal path to be noise shaped and not harmonically related to the input.

Mismatch shaping applied to individual pipeline stages with the swapping sequence $sw_1 = sw_2 = sw_3 = (-1)^n$, results in the output spectrum shown in fig. 4-13. The measured SNDR is 66.5dB and SFDR is 75.7dB at an OSR=4. This demonstrates an SNDR improvement of 2.3dB and an SFDR improvement of 8.2dB, compared to a CFCS ADC. The even harmonics are not completely modulated to half the sampling frequency. Theoretically we should get results which are identical to when $sw_{all} = (-1)^n$, but the measured results are slightly worse. This can be explained if the even order distortion is not completely due to capacitor mismatch. The even order distortion may also be caused by sources such as slight asymmetries in the fully differential circuits. When the sequence $sw_{all} = (-1)^n$ is used the source of the even order distortion is not important and the technique modulates all of this distortion to half the sampling frequency. On the other hand, when mismatch shaping is applied to individual stages, only capacitor errors get shaped.

Mismatch shaping applied to individual stages results in the spectrum shown in fig. 4-14, when the swapping sequence $sw_1 = (-1)^n$, sw_2 and sw_3 have spectra shown in fig. 2-42 and fig. 2-29 respectively. The measured SNDR is 66.6dB and SFDR is 75.6dB at an OSR=4. The SNDR improves by 2.4dB and the SFDR improves by 8.1dB, compared to a CFCS ADC. This technique also does not completely modulate the even order distortion, and the

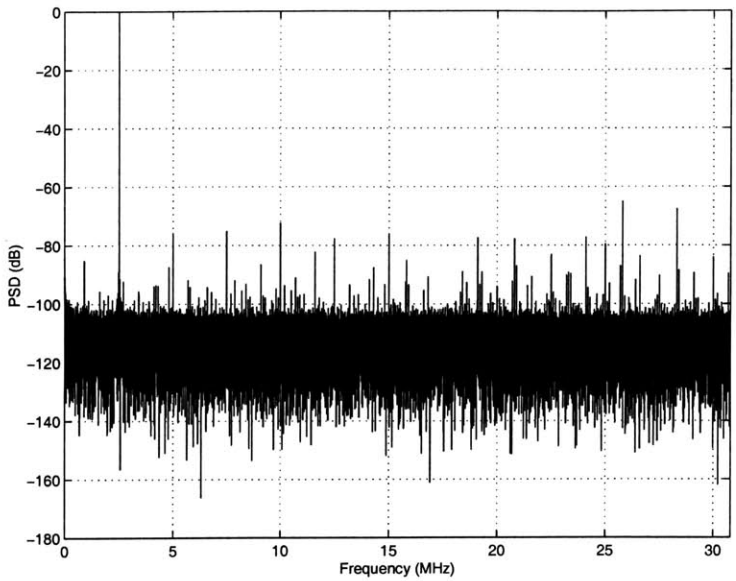


Figure 4-13: Mismatch shaping applied to individual pipeline stages with sequence $(-1)^n$: SNDR=66.5dB, SFDR=75.7dB, f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

residual distortion can be explained by the same mechanism of the last paragraph.

All the previous results are summarized in table 4.1. The estimates of the ADC output power spectral density were computed using the Welch procedure with the data windowed using a Kaiser window with β=21 [61].

Fig. 4-15 and 4-16 show the INL of the converter without and with mismatch shaping respectively. Fig. 4-17 and 4-18 show the DNL without and with mismatch shaping. The INL and DNL plots are obtained using the procedure in [62] from the measured data after it has been filter digitally to remove the out-of-band signals. The mismatch shaping is applied using the sequence $sw_{all} = (-1)^n$.

Fig. 4-19 plots the SNDR and SFDR as a function of the sampling rate for a mismatch shaped converter. The converter has a SNDR of at least 67dBs up to a sampling rate of 61MHz. Beyond this frequency the performance becomes effected by distortion due to incomplete opamp settling and the SNDR degrades.

Fig. 4-20 plots the SNDR as a function of the oversampling ratio. The SNDR improves by 3dBs for every doubling of the OSR, as would be expected from a thermal noise limited

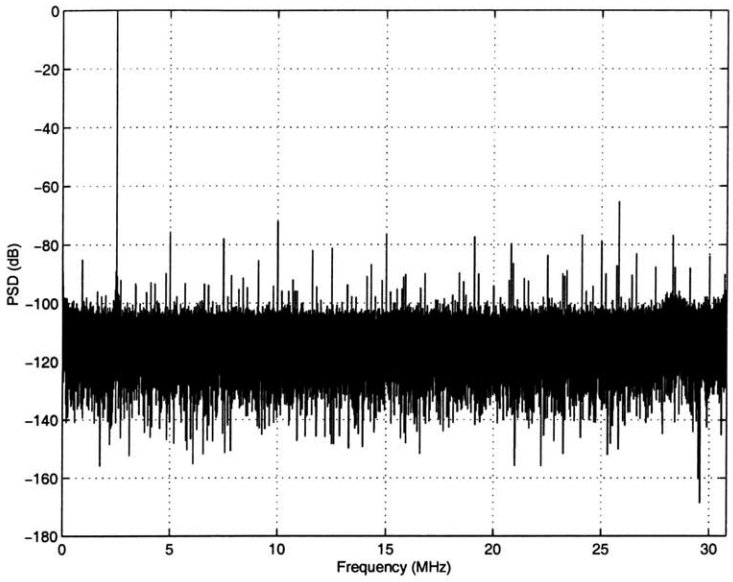


Figure 4-14: Mismatch shaping applied to individual stages with $sw_1 = (-1)^n\ sw_2$ shown in fig. 2-42 and sw_3 shown in fig. 2-29: SNDR=66.6dB SFDR=75.6dB, f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

converter. The SNDR does not exceed 80dB though, as the converter performance becomes dominated by the inband distortion.

As discussed in section 2.5, a oversampled CFCS ADC with a bandpass input placed at one fourth the sampling rate will have most of its distortion out of band. The output spectrum of a CFCS converter with a 36MHz(-2dB full scale) bandpass input is shown in fig. 4-21, when f_s=49MHz. The dominant distortion components fall out of band and the measured SNDR is 61.5dB and the SFDR 75dB. The choice of f_s was limited by the bandpass filter available to filter the ADC input. The rise in the noise floor around the carrier is caused by noise in the input source which is not completely suppressed by the bandpass filter. There is an overall 3.5dB degradation in SNDR which can be attributed partially due to this rise in the noise floor around the carrier. Another source is the overall rise in the noise floor which is perhaps caused by dynamic error in the front end comparator.

Table 4.2 summarizes the measured performance of the ADC

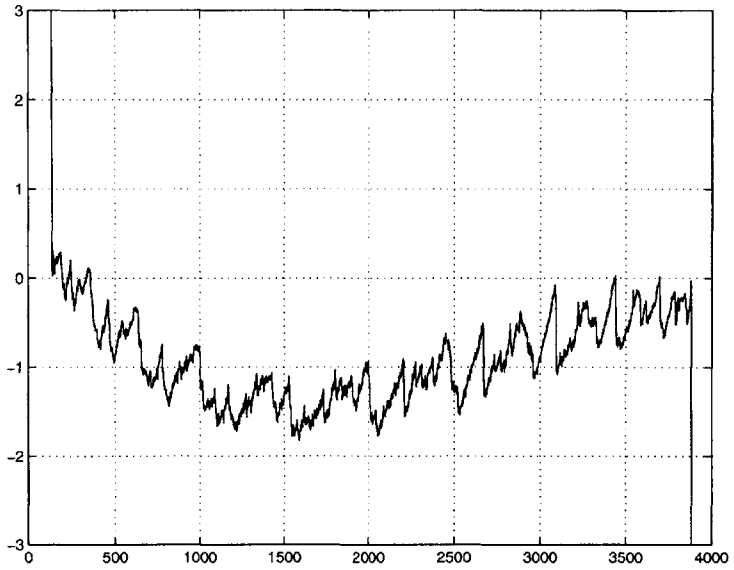


Figure 4-15: CFCS INL plot: f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

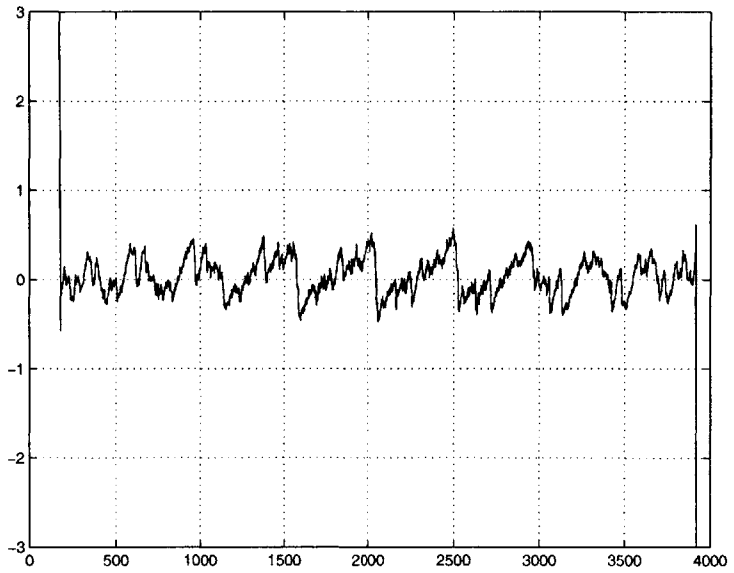


Figure 4-16: INL of mismatch shaped CFCS with $sw_{all} = (-1)^n$, f_s=61.6MHz $f_{in} = 2.5MHz$ and OSR=4.

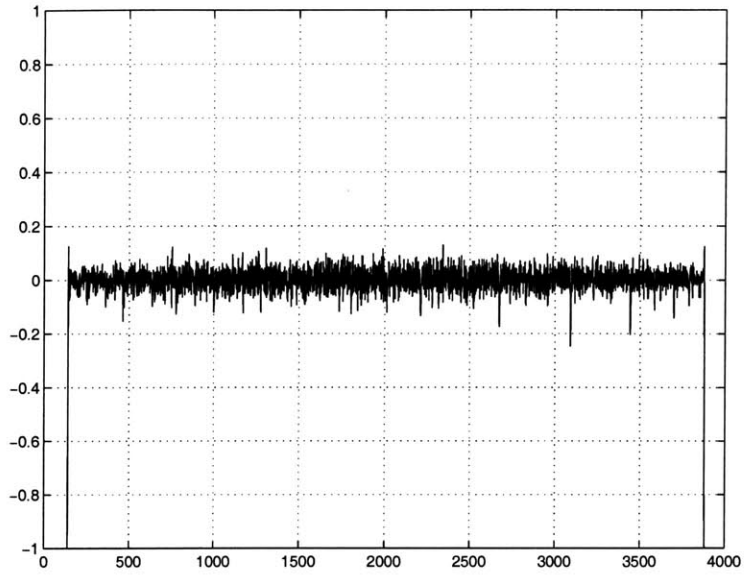


Figure 4-17: CFCS DNL plot: f_s=61.6MHz, f_{in}=2.5MHz and OSR=4.

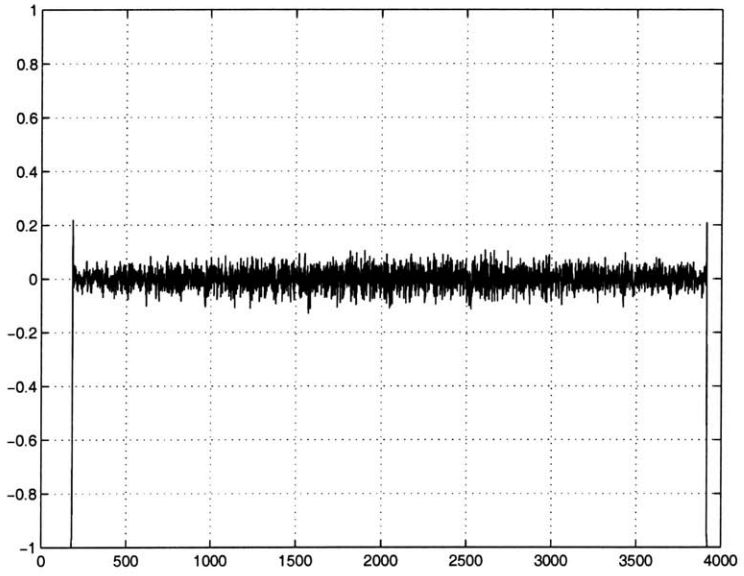


Figure 4-18: DNL of mismatch shaped CFCS with $sw_{all} = (-1)^n$, f_s=61.6MHz f_{in}=2.5MHz and OSR=4.

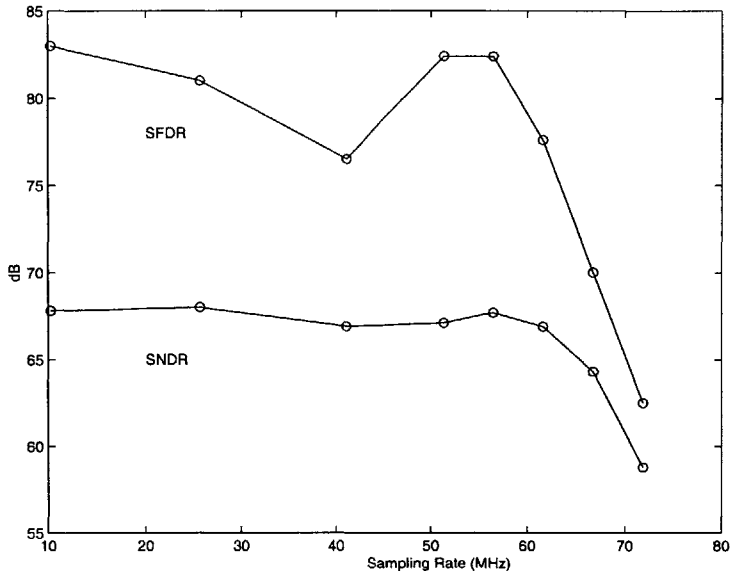


Figure 4-19: The SNDR and SFDR of a mismatch shaped converter vs. sampling frequency (f_{in}=0.475MHz).

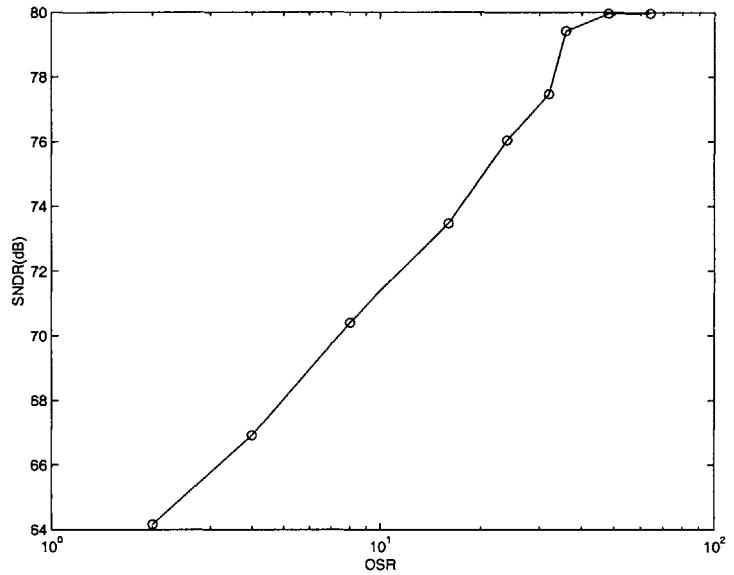


Figure 4-20: The SNDR of a mismatch shaped converter vs. the over sampling ratio (f_s=61.6MHz and f_{in}=0.475MHz).

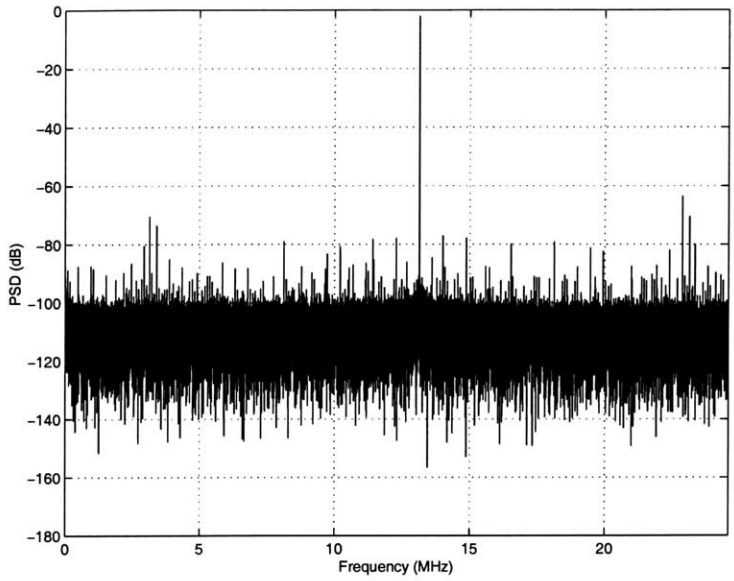


Figure 4-21: CFCS ADC: SNDR=61.5dB, f_s=49.1MHz, f_{in}=36MHz at -2dB full scale and OSR=4.

Algorithm	SNDR(dB) (dB)	SFDR(dB) (dB)
CFCS	64.1	67.5
$sw_{all} = (-1)^n$	67.4	76
sw_{all} with the PSD in fig. 2-29	60.3	78.5
$sw_1 = sw_2 = sw_3 = (-1)^n$	66.5	75.7
$sw_1 = (-1)^n$ sw_2 with the PSD in fig. 2-42 sw_3 with the PSD in fig. 2-29	66.6	75.6

Table 4.1: Summary of the measured performance of different mismatch shaping algorithms.

Process	0.35μm CMOS
Supply Voltage	3.4V
Differential Input Range	1.4Vpp
Resolution (OSR=4)	12bits
Sampling Rate	61Msample/s
SNDR (w/o MS and OSR=4)	64.1dB
SNDR (with MS and OSR=4)	67.5dB
SFDR (w/o MS and OSR=4)	67.4dB
SFDR (with MS and OSR=4)	76dB
INL (w/o MS)	+0.3/-1.8 LSB
INL (with MS)	+0.6/-0.4 LSB
DNL (w/o MS)	+0.12/-0.25 LSB
DNL (with MS)	+0.12/-0.12 LSB
Analog Power Dissipation	435 mW
Digital Power Dissipation	165 mW

Table 4.2: Summary of the measured performance.

4.3 Conclusions

The experimental results raise two important issues which will be discussed here. The main limit on the achievable improvement in SFDR performance is due to circuit nonidealities which introduce odd distortion components which do not get shaped. The most important odd order distortion effect in this design is signal dependent charge injection. The tones which alias into the signal band when mismatch shaping is applied are smaller in amplitude than the inband odd order distortion. The use of noise shaped mismatch shaping sequences therefore does not improve the SFDR, and does not offer an advantage, since it degrades the converter SNDR because of the larger energy aliased into the signal band.

This test chip also demonstrates another important practical consideration. Mismatch shaping is more effectively realized by chopping (using sw_{all}) as opposed to being realized through controlling the feedback capacitor (using sw_1, sw_2 and sw_3). Chopping shapes the even order distortion regardless of its source. Controlling the feedback capacitor on the other hand only shapes the distortion due to capacitor mismatch. This leads to the

conclusion that implementing mismatch shaping on individual stages will also be more effective if chopping is performed on each stage.

Chapter 5

Conclusion

5.1 Thesis Summary

This thesis presented mismatch shaping techniques to improve the linearity of oversampled pipeline data converters. The techniques do not rely on calibration, which estimates the converter nonlinearity and compensates for it. Rather they improve the linearity by modulating the distortion energy out of the signal band. This is accomplished without any knowledge of the specifics of the converter nonlinearity, except for the overall structure of the nonlinearity which is constrained to be an even function. The 1-bit-per-stage CFCS pipeline converter offers the basic building block with the desired nonlinearity structure, and is used to implement mismatch shaping using simple circuit realizations. In the simplest implementation the entire CFCS converter is chopped, modulating the distortion to half the sampling frequency. Experimental results show that the converter SFDR can be improved by 9dBs, making the SNDR figure dominated by the converter thermal noise. Other mismatch shaping techniques are based on the chopping the individual stages in the pipeline. This allows for greater degrees of freedom which can be exploited by using different randomized mismatch shaping sequences to obtain significant improvements in performance.

The simplicity of the implementation of a mismatch shaped converter based on the

1-bit-per-stage CFCS pipeline allows for rapid design of the converter circuits, compared to multi-bit-per-stage pipelines or delta sigma converters with dynamic element matching. Moreover, the desired specifications can be meet without the need for calibration.

5.2 Future Work

The concept of exploiting the even structure of the nonlinearity is a general one. An area for further research is to extend this approach to different types of data converters, through the engineering of their transfer characteristics. It may also be possible to extend this idea to other sample-data systems. If the even transfer characteristic can be engineered then mismatch shaping can help significantly improve the linearity.

Another area for further investigation is the generation of the swapping sequences. The techniques presented in this thesis attempt to approximate the ideally desired spectral properties, but fall short of the optimal in a number of ways. Sequences which better approximate the ideal spectrum would be very useful in improving the performance of mismatch shaping.

Yet another area for further investigation is the use of different sequences for different pipeline stages. The approach presented in this thesis is based on an intuitive time domain analysis. A more detailed investigation of the interaction of the distortion introduced by the different stages might reveal powerful data-dependent techniques to improve the performance.

Finally, the major part of this work revolved around 1-bit-per-stage implementations of the pipeline stages. Multi-bit-per-stage pipeline designs while more complex, do possess some advantages. If better mismatch shaping techniques can be developed for multi-bit-per-stage designs they would be very practical.

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