

MIT Open Access Articles

Stacked Switched Capacitor Energy Buffer Architecture

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

Citation: Chen, Minjie, Khurram K. Afridi, and David J. Perreault. "Stacked Switched Capacitor Energy Buffer Architecture." IEEE Trans. Power Electron. 28, no. 11 (n.d.): 5183–5195.

As Published: <http://dx.doi.org/10.1109/TPEL.2013.2245682>

Publisher: Institute of Electrical and Electronics Engineers (IEEE)

Persistent URL: <http://hdl.handle.net/1721.1/86995>

Version: Author's final manuscript: final author's manuscript post peer review, without publisher's formatting or copy editing

Terms of use: Creative Commons Attribution-Noncommercial-Share Alike



Stacked Switched Capacitor Energy Buffer Architecture

Minjie Chen, *Student Member, IEEE*, Khurram K. Afridi, *Member, IEEE*, and David J. Perreault, *Fellow, IEEE*

Abstract—Electrolytic capacitors are often used for energy buffering applications, including buffering between single-phase ac and dc. While these capacitors have high energy density compared to film and ceramic capacitors, their life is limited. This paper presents a stacked switched capacitor (SSC) energy buffer architecture and some of its topological embodiments, which when used with longer life film capacitors overcome this limitation while achieving effective energy densities comparable to electrolytic capacitors. The architectural approach is introduced along with design and control techniques. A prototype SSC energy buffer using film capacitors, designed for a 320 V dc bus and able to support a 135 W load, has been built and tested with a power factor correction circuit. It is shown that the SSC energy buffer can successfully replace limited-life electrolytic capacitors with much longer life film capacitors, while maintaining volume and efficiency at a comparable level.

Index Terms—Switched capacitor circuits, Buffer circuits, Energy storage, AC-DC power conversion, DC-AC power conversion.

I. INTRODUCTION

POWER conversion systems that interface between dc and single-phase ac need energy storage to provide buffering between the constant power desired for a dc source or load and the continuously-varying power desired for a single-phase ac system, as illustrated in Fig. 1. Applications for such buffering include power supplies, solar photovoltaic inverters, electric vehicle chargers and grid-connected light emitting diode (LED) drivers. Assuming unity power factor, the power from or to the single-phase ac system, $P_{ac}(t)$, varies sinusoidally at twice-line frequency (120 Hz in the US) between zero and twice its average value, P_{avg} , with average ac system power equaling the dc system power, P_{dc} :

$$P_{ac}(t) = P_{dc}(1 - \cos(2\omega_{line}t)). \quad (1)$$

Here ω_{line} is the line's angular frequency ($2\pi \times 60$ rad/s for the US). The difference in instantaneous power between source and load must be absorbed or delivered by the energy buffer:

$$P_b(t) = P_{dc} - P_{ac}(t) = P_{dc}\cos(2\omega_{line}t). \quad (2)$$

The peak energy that needs to be buffered, E_b , is the total energy delivered to (or extracted from) the buffer during a half-line cycle and is given by:

$$E_b = \frac{P_{dc}}{\omega_{line}}. \quad (3)$$

The authors are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: minjie@mit.edu; afridi@mit.edu; djperrea@mit.edu).

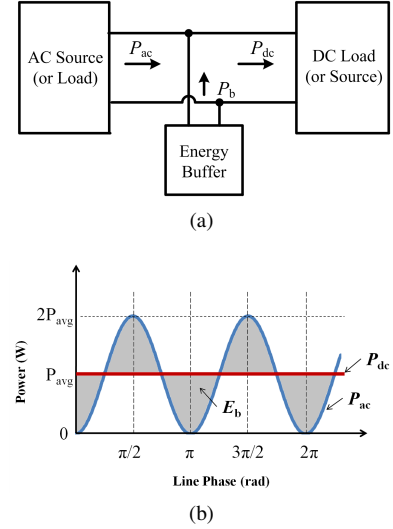


Fig. 1. Mismatch in instantaneous power between single-phase ac, P_{ac} , and constant power dc, P_{dc} , results in the need for an energy buffer, as shown in (a), to absorb and supply the energy, E_b , indicated by the shaded area in (b).

Since the peak buffered energy depends only on the dc system power and the line frequency, the volume of the energy buffer cannot be reduced simply by increasing the switching frequency of a power electronic converter interfacing the single-phase ac and dc systems.

Today, electrolytic capacitors are generally used to provide high-density energy storage for buffering. However, it is widely appreciated that despite providing the best available energy density, electrolytic capacitors represent a significant constraint on system lifetime, especially in high temperature environment. On the other hand, film capacitors have much longer lifetime, but considerably lower peak energy density. Hence, the development of energy buffering architectures that eliminate electrolytic capacitors while maintaining high energy storage density and high efficiency is important for future grid interface systems that require both small size and long life.

While electrolytic capacitors provide much higher peak energy density than film capacitors (by an order of magnitude), electrolytic capacitors can only be operated over a narrow charge/discharge range (corresponding to a small voltage ripple) at 120 Hz for thermal and efficiency reasons. These considerations directly limit the energy buffering capability of electrolytic capacitors at 120 Hz. Thus, while peak energy densities of up to 0.8 J/cm^3 can typically be achieved with commercially available electrolytic capacitors at the voltage and power levels we consider, the allowable energy swing at 120 Hz yields practical energy densities that are significantly

lower [1]. Film capacitors typically have peak energy densities of only about 0.1 J/cm^3 . Therefore, if electrolytic capacitors are simply replaced by film capacitors (with similar voltage swing constraints), the passive volume would roughly increase by an order of magnitude, which is usually unacceptable. However, film capacitors have considerably lower series resistance compared to electrolytic capacitors, which allows them to be efficiently charged and discharged over a much wider energy range. Using a large fraction of the capacitor's stored energy necessitates large voltage swings, which is also unacceptable in most applications. Therefore, if electrolytic capacitors are to be replaced by film capacitors while maintaining high energy density, this wide variation in capacitor voltage must somehow be curtailed.

This paper presents a new switched capacitor based energy buffer architecture that restricts the apparent voltage ripple while utilizing a large fraction of the energy in the capacitors. It successfully replaces electrolytic capacitors with film capacitors to achieve longer lifetimes while maintaining small volume. When used with other energy-storage types, such as ultracapacitors, the proposed approach is also applicable to energy buffering applications at high powers and long time-scales. This work represents an expansion on our earlier conference paper [2], and includes a more detailed explanation of the new energy buffer architecture, additional experimental results and estimates of loss breakdown. The remainder of this paper is organized as follows: Section II describes the past work on film-capacitor-based energy buffers and switched-capacitor-based energy storage architectures. Section III details the fundamental principles of the proposed stacked switched capacitor (SSC) energy buffer architecture. A specific topological implementation of this architecture and its extensions are described in section IV. This section also provides design guidelines for selecting an appropriate topology for a particular application. Section V describes the design and implementation of a prototype SSC energy buffer. The experimental results from this prototype are discussed and compared with simulation in section VI. Finally, section VII summarizes the conclusions of the paper and identifies directions for future work.

II. PAST WORK

In past efforts, bi-directional dc-dc converters have been employed to effectively utilize film capacitors while maintaining a desired narrow-range bus voltage [3], [4]. While this approach is flexible in terms of its use, it unfortunately leads to low buffering efficiency if high power density is to be maintained, due to losses in the dc-dc converter. Other systems have incorporated the required energy buffering as part of the operation of the grid interface power stage [5]–[8]. This can offset a portion of the buffering loss associated with introduction of a complete additional power conversion stage, but still introduces high-frequency loss and is quite restrictive in terms of operation and application.

An alternative approach relies on switched capacitor circuits. Many switched capacitor circuits have been developed for energy conversion applications [9]–[13]. However,

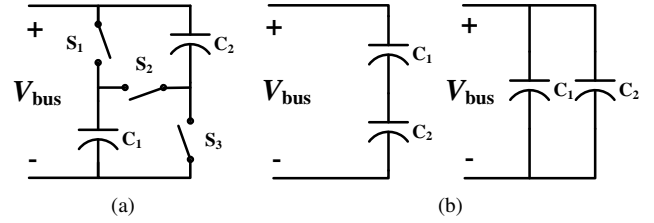


Fig. 2. (a) A simple parallel-series switched capacitor circuit, and (b) its two configurations under alternate switch states. This circuit can constrain bus voltage to within 33.3% of nominal value while providing energy buffering capability of 93.75% of total peak energy-storage capability of the capacitors.

switched capacitor circuits have not been extensively explored for energy buffering applications. Switched capacitor circuits that reconfigure capacitors between parallel and series combinations have been used to improve the energy utilization of ultra-capacitors [14]–[16]. A simple version of this parallel-series switched capacitor circuit is shown in Fig. 2. While this circuit has a high **energy buffering ratio**¹ of 93.75%, it suffers from a large **voltage ripple ratio**² of 33.3%. More complex parallel-series switched capacitor circuits which achieve better voltage ripple ratio have also been developed [16]. However, they suffer from high circuit complexity when high energy utilization and small voltage ripple are required. For example, the circuit with the best performance in [16] (the 8-6-5-4-3 parallel-series switched capacitor circuit) has energy buffering ratio of 92.09% and a voltage ripple ratio of 14.3%. However, it needs 41 switches and 120 capacitors. This makes it overly complicated for practical use.

III. STACKED SWITCHED CAPACITOR (SSC) ENERGY BUFFER ARCHITECTURE

Figure 3 shows the general architecture of the proposed stacked switched capacitor (SSC) energy buffer. It is composed of two series-connected blocks of switches and capacitors. The capacitors are of a type that can be efficiently charged and discharged over a wide voltage range (e.g., film capacitors). The switches enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to the buffer port (V_{bus}). The SSC energy buffer works on the principle that its individual buffer capacitors absorb and deliver energy without tightly constraining their individual terminal voltages, while a narrow-range voltage is maintained at the buffer port through appropriate reconfiguration of the switches. Hence, even though the buffer port voltage varies only over a small range, the capacitors charge and discharge over a wide range to buffer substantial energy. This enables high effective

¹**Energy buffering ratio** (Γ_b) is defined as the ratio of the energy that can be injected and extracted from an energy buffer in one cycle to the total energy capacity of the buffer, i.e., $\Gamma_b = \frac{E_{max} - E_{min}}{E_{rated}}$, where E_{max} and E_{min} are the maximum and minimum values of energy stored in the energy buffer during normal operation, and E_{rated} is the total energy capacity of the energy buffer.

²**Voltage ripple ratio** (R_v) is defined as the ratio of the peak voltage ripple amplitude to the nominal (or average) value of the voltage, i.e., $R_v = \frac{V_{max} - V_{min}}{2V_{nom}}$, where V_{max} , V_{min} and V_{nom} are the maximum, minimum and nominal values of the voltage, respectively [17].

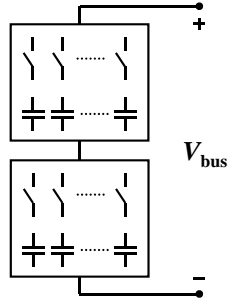


Fig. 3. General architecture of the stacked switched capacitor (SSC) energy buffer.

energy density through maximum utilization of the capacitor energy storage capability.

Efficiency of the SSC energy buffer can be extremely high because the switching network need operate at only very low (line-scale) switching frequencies, and the system can take advantage of soft charging of the energy storage capacitors to reduce loss [18]. Moreover, the proposed buffer architecture exhibits losses that scale with the amount of energy that must be buffered, such that high efficiency can be achieved across the full operating range.

IV. SSC ENERGY BUFFER TOPOLOGIES

There are multiple embodiments of the proposed stacked switched capacitor (SSC) energy buffer [1]. In this paper we present one embodiment, the 2-6 bipolar SSC energy buffer, and its extensions in the form of the generalized n - m bipolar SSC energy buffer.

A. 2-6 Bipolar SSC Energy Buffer

Figure 4 shows an example embodiment of the stacked switched capacitor energy buffer: the 2-6 bipolar SSC energy buffer. This topology has two backbone capacitors, C_{11} and C_{12} ; six supporting capacitors, C_{21} , C_{22} , C_{23} , C_{24} , C_{25} , and C_{26} ; and twelve switches, S_{11} , S_{12} , S_{21} , S_{22} , S_{23} , S_{24} , S_{25} , S_{26} , S_{h1} , S_{h2} , S_{h3} , and S_{h4} . This circuit can keep the bus voltage ripple within 10% of nominal value when designed and operated in the manner described below.

The eight capacitors are chosen to have identical capacitance, but different voltage ratings. The two backbone capacitors, C_{11} and C_{12} , have voltage rating of $1.6V_{nom}$, where V_{nom} is the nominal value of the bus voltage (V_{bus}). The voltage ratings of the six supporting capacitors are as follows: $0.6V_{nom}$ for C_{21} , $0.5V_{nom}$ for C_{22} , $0.4V_{nom}$ for C_{23} , $0.3V_{nom}$ for C_{24} , $0.2V_{nom}$ for C_{25} and $0.1V_{nom}$ for C_{26} . A precharge circuit (not shown in Fig. 4, but discussed in section V-B) ensures that the following initial voltages are placed on the eight capacitors: $0.4V_{nom}$ on C_{11} , $0.4V_{nom}$ on C_{12} , $0.5V_{nom}$ on C_{21} , $0.4V_{nom}$ on C_{22} , $0.3V_{nom}$ on C_{23} , $0.2V_{nom}$ on C_{24} , $0.1V_{nom}$ on C_{25} , and $0V$ on C_{26} .

Figure 5 shows the switch states, the capacitor voltages and the resulting bus voltage for the 2-6 bipolar SSC energy buffer over a complete charge and discharge cycle. When the energy buffer starts charging up from its minimum state of

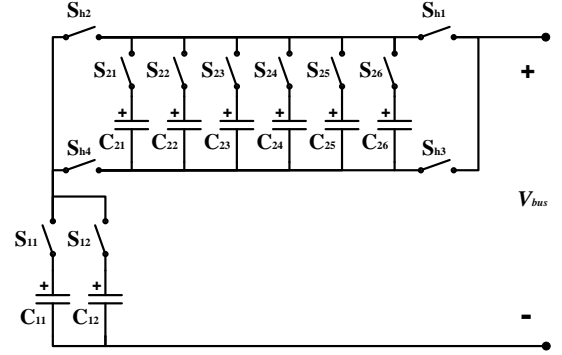


Fig. 4. An example embodiment of the SSC energy buffer architecture: the 2-6 bipolar SSC energy buffer. This circuit has two backbone capacitors C_{11} and C_{12} and six supporting capacitors C_{21} to C_{26} and twelve switches. Precharge and control circuits are not shown.

charge, S_{h1} , S_{h4} , S_{21} and S_{11} are turned on with all the other switches turned off. In this state, C_{11} and C_{21} are connected in series and charged until the bus voltage rises from $0.9V_{nom}$ to $1.1V_{nom}$. At this instant the voltage of C_{21} (V_{21}) reaches $0.6V_{nom}$ and the voltage of C_{11} (V_{11}) reaches $0.5V_{nom}$. Then S_{21} is turned off and S_{22} is turned on; and the bus voltage drops back down to $0.9V_{nom}$. Then as the charging continues, the voltage of C_{22} rises to $0.5V_{nom}$ and the voltage of C_{11} reaches $0.6V_{nom}$ and the bus voltage again reaches $1.1V_{nom}$. Next S_{22} is turned off, S_{23} is turned on and C_{23} is charged. This process is repeated until C_{26} is charged. At this stage all the supporting capacitors are at their maximum voltage; the voltages of the backbone capacitors are: V_{nom} on C_{11} and $0.4V_{nom}$ on C_{12} ; and the bus voltage is $1.1V_{nom}$. Next S_{h1} and S_{h4} are turned off, and S_{h3} and S_{h2} are turned on. This connects C_{26} , and the other supporting capacitors, in reverse orientation with C_{11} and the bus voltage again drops to $0.9V_{nom}$. Now C_{11} can continue to charge up through the now reverse-connected supporting capacitors through a process similar to the one described above, except that the supporting capacitors are discharged in reverse order, i.e., first through C_{26} , then through C_{25} , and so on until finally through C_{21} . At this stage C_{11} is fully charged to $1.6V_{nom}$ and charging of C_{12} must begin. For this the h-bridge switches are again toggled (i.e., S_{h3} and S_{h2} are turned off, and S_{h1} and S_{h4} are turned on), S_{11} is turned off and S_{12} is turned on. The charging process for C_{12} is identical to the charging process for C_{11} , as shown in Fig. 5. During the discharge period, the capacitors C_{11} and C_{12} are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge period are a mirror of those in the charging period.

Throughout the charging and discharging period of this energy buffer, the bus voltage stays within the range $0.9V_{nom}$ – $1.1V_{nom}$. Hence, the 2-6 bipolar SSC energy buffer operating in this manner has a bus voltage ripple ratio (R_v) of 10%. Furthermore, it has an energy buffering ratio (Γ_b) of 79.6%.

To help elucidate the operation of the SSC energy buffer, the waveforms in Fig. 5 are drawn assuming that the charge/discharge current is a square-wave (instead of sinusoidal) at twice-line-frequency. The bus voltage at the termi-

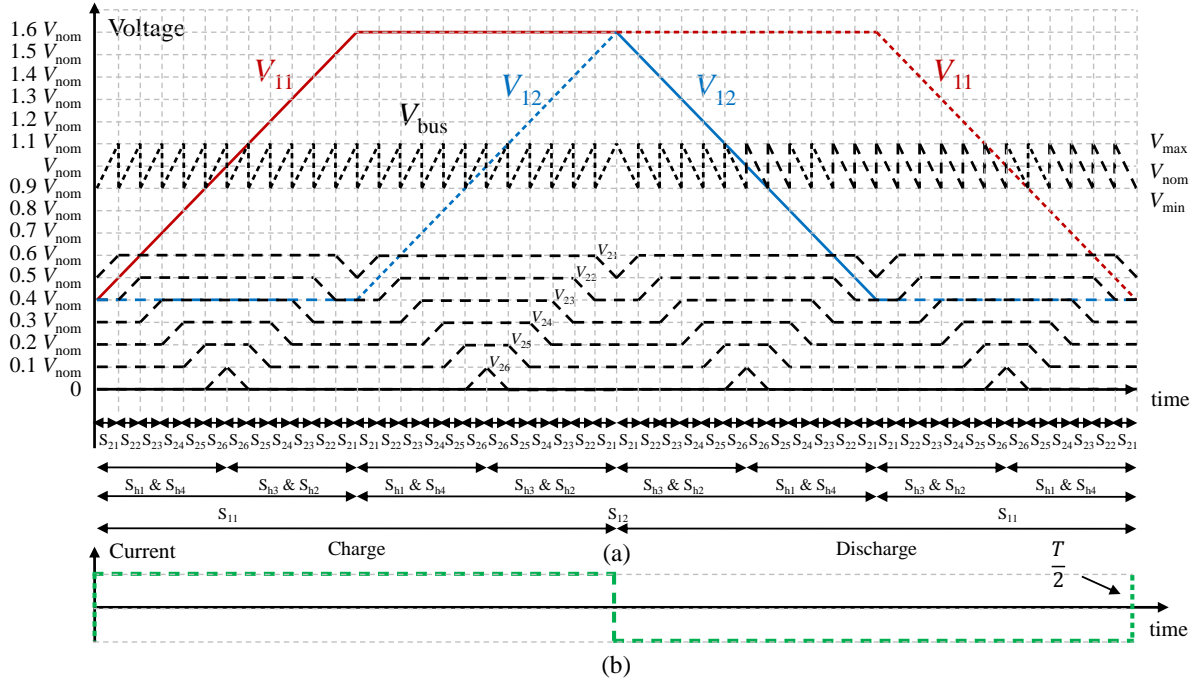


Fig. 5. Waveforms for the 2-6 bipolar SSC energy buffer of Fig. 4 over a charge and discharge cycle with a square-wave terminal current: (a) Switch states, individual capacitor voltages, and resulting bus voltage, and (b) terminal current waveform. In a twice-line-frequency energy buffering application, this complete charge/discharge cycle would take place in a half-line-cycle (i.e., $\frac{T}{2} = \frac{1}{120\text{Hz}} = 8.33$ milliseconds in the US power grid).

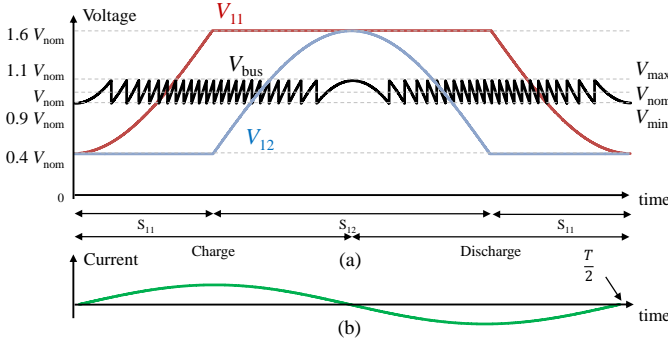


Fig. 6. Waveforms for the 2-6 bipolar SSC energy buffer of Fig. 4 over a charge and discharge cycle with a sinusoidal terminal current: (a) Backbone capacitor voltages and bus voltage, and (b) terminal current waveform. In a twice-line-frequency energy buffering application, this complete charge/discharge cycle would take place in a half-line-cycle (i.e., $\frac{T}{2} = \frac{1}{120\text{Hz}} = 8.33$ milliseconds in the US power grid).

nals of the energy buffer and the backbone capacitor voltages with a sinusoidal charge/discharge current are shown in Fig. 6. In summary, this SSC energy buffer achieves high energy buffering density (corresponding to the high energy buffering ratio) by allowing the voltages of the backbone capacitors (C_{11} and C_{12}), which store most of the energy, to swing over a wide range as they are charged and discharged at twice-line-frequency. To compensate for this large voltage swing, supporting capacitors (C_{21} , C_{22} , C_{23} , C_{24} , C_{25} , and C_{26}) with appropriate voltage levels are connected in series with the backbone capacitors. This makes the voltage variation in the bus voltage (V_{bus}) much smaller than the voltage variation across the backbone capacitors (V_{11} and V_{12}). The h-bridge

allows the supporting capacitors to be connected in series with the backbone capacitors in reverse polarity as well. This permits the backbone capacitors to be charged to voltages higher than the bus voltage and enhances the energy storage capability of the buffer structure since the energy stored in a capacitor is proportional to the square of the voltage.

Since, the backbone capacitors store most of the energy, the inclusion of the supporting capacitors does not degrade the energy buffering density of the overall buffer. High energy buffering density reduces the passive volume requirement for a given bus voltage ripple. That is, for a given allowed bus voltage ripple ratio, the passive volume of the SSC energy buffer will be significantly smaller than that of a single-capacitor energy buffer. Alternatively, for the same passive volume as a single capacitor, an SSC energy buffer can be designed with smaller voltage ripple.

B. n - m Bipolar SSC Energy Buffer

The capacitors that buffer most of the energy in the circuit of Fig. 4 are the backbone capacitors C_{11} and C_{12} . Therefore, by adding additional backbone capacitors in parallel with C_{11} and C_{12} the energy buffer could potentially achieve better buffering performance. The number of supporting capacitors can also be changed. To evaluate the impact of the number of backbone and supporting capacitors on the performance of the energy buffer, the topology of Fig. 4 is extended by incorporating n backbone capacitors and m supporting capacitors, as shown in Fig. 7. The energy buffering ratio for this n - m bipolar SSC energy buffer (with n backbone capacitors of equal value C_1 and m supportive capacitors of equal value C_2) is given by:

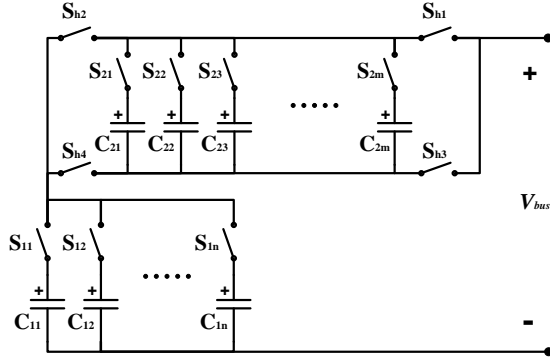


Fig. 7. The n - m bipolar SSC energy buffer. The circuit has n backbone capacitors, m supporting capacitors and $(n+m+4)$ switches.

$$\Gamma_b = \frac{nC_1((1 + 2mR_v \frac{C_2}{C_1+C_2})^2 - (1 - 2mR_v \frac{C_2}{C_1+C_2})^2)}{nC_1(1 + 2mR_v \frac{C_2}{C_1+C_2})^2 + C_2(1 + 2^2 + \dots + m^2)R_v^2}. \quad (4)$$

Figure 8 shows the variation in energy buffering ratio, Γ_b , (with C_1 equal to C_2) as a function of the number of backbone capacitors n and the number of supporting capacitors m for three different values of voltage ripple ratio R_v . These plots indicate that there is an optimal number of supporting capacitors that should be used for a given number of backbone capacitors in order to maximize the energy buffering ratio. Note that this optimal number of supporting capacitors depends on the value of allowed voltage ripple ratio.

The plots of Fig. 8 can be used to select the optimal number of backbone and supporting capacitors to maximize the energy buffering ratio for a given bus voltage ripple ratio. If a larger voltage ripple ratio is allowed, a high energy buffering ratio can be achieved with fewer backbone and supporting capacitors. For a fixed number of backbone capacitors, a lower voltage ripple ratio requires a larger number of supporting capacitors if maximum energy buffering is to be achieved. However, increasing the number of supporting capacitors also increases the complexity of the circuit and the switching frequency of the switches associated with the supporting capacitors (S_{21} - S_{2m}).

For a ripple ratio (R_v) of 10% with 2 backbone capacitors, the optimal number of supporting capacitors is 6 (see Fig. 8(b), providing an energy buffering ratio of 79.6%); hence our choice of the 2-6 bipolar SSC energy buffer discussed earlier to meet the 10% voltage ripple requirement. Note that for an R_v of 10%, with 8 backbone and 8 supporting capacitors, an energy buffering ratio of 91.6% can be achieved. Hence, the SSC energy buffer achieves performance similar to the 8-6-5-4-3 parallel-series switched capacitor circuit of [16] with only 16 capacitors and 20 switches instead of 120 capacitors and 41 switches.

The bipolar implementations presented here are one class of embodiments of the SSC energy buffer architecture. Another class of embodiments are the unipolar SSC energy buffers [1]. The unipolar SSC energy buffers do not have the h-bridge switches and only have one backbone capacitor. However, a unipolar design with 10% voltage ripple ratio achieves a lower

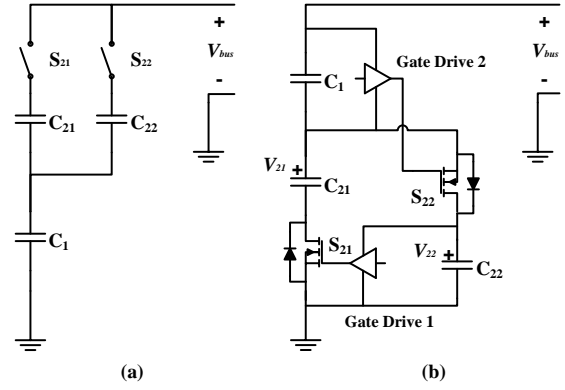


Fig. 9. (a) The 1-2 unipolar SSC energy buffer. The circuit has 1 backbone capacitor, 2 supporting capacitors and 2 switches. The energy buffer can be implemented very simply as shown in (b). In this implementation, the positions of the supporting and backbone networks are inverted for convenience. All gate drives are self-powered by the buffer capacitors (via step-down regulation circuitry integrated within the gate drive). Note: V_{22} is always kept larger than V_{21} using a precharge and control strategy similar to the one described in Section IV.

energy buffering ratio than the 2-6 bipolar design although it has fewer switches. A simple unipolar SSC energy buffer — the 1-2 unipolar SSC energy buffer — is shown in Fig. 9(a). This energy buffer has only 3 capacitors and 2 switches. It also allows the use of a simple gate drive implementation as shown in Fig. 9(b). However, with 10% voltage ripple ratio its energy buffering ratio is 38.1%, which is lower than the 79.6% of the 2-6 bipolar energy buffer. Hence, the SSC energy buffer architecture allows tradeoffs to be made between complexity and effective energy density by appropriate choice of topology [1], [19].

V. PROTOTYPE DESIGN

To validate the proposed concept we have designed and built a prototype of the 2-6 bipolar SSC energy buffer, similar to the one described in Section IV-A and shown in Fig. 4. The prototype is designed as the energy buffer for a power factor correction (PFC) front-end of a two-stage single-phase ac-to-dc power converter as shown in Fig. 10. The SSC energy buffer replaces the electrolytic capacitor normally connected at the output of the PFC. To simplify our implementation, a load resistor is used in place of the second-stage dc-dc converter. The SSC energy buffer is designed to meet a 10% bus voltage ripple ratio requirement on a 320 V dc bus with a maximum load of 135 W.

The PFC used for this prototype is an evaluation board from STMicroelectronics that uses their transition-mode PFC controller (L6562A). This controller operates the boost PFC at the boundary between continuous and discontinuous conduction mode by adjusting the switching frequency. The evaluation board has a 330 μ F electrolytic capacitor at the output of the PFC, and according to the PFC datasheet can maintain a voltage ripple ratio of 2.5%, while supplying a 400 W load at a bus voltage of 400 V. We have experimentally verified that a 40 μ F electrolytic capacitor is sufficient to support 135 W of output power with 10% voltage ripple ratio. The total

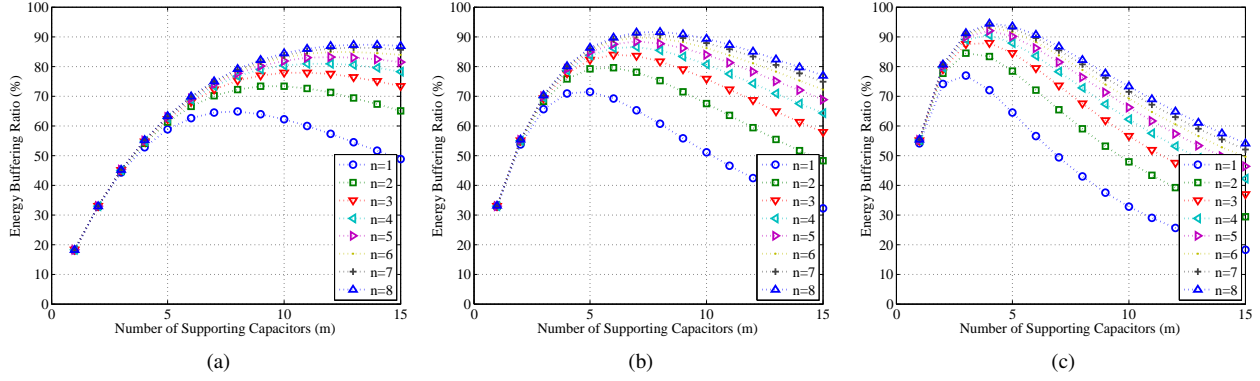


Fig. 8. Energy buffering ratio (Γ_b) as a function of the number of backbone capacitors n and number of supporting capacitors m for different values of voltage ripple ratio: (a) $R_v = 5\%$, (b) $R_v = 10\%$ and (c) $R_v = 20\%$.

volume of the electrolytic capacitor used for this verification is approximately 9 cm^3 .

The energy buffer that replaces this electrolytic capacitor consists of three functional blocks: the energy buffer power circuit, the precharge circuit and the control unit, as shown in Fig. 10. In addition, the energy buffer needs to provide a feedback signal to the PFC for its proper operation as shown in Fig. 10. The design of each of these four elements is discussed below.

A. SSC Energy Buffer Power Circuit

According to Fig. 8(b), to achieve a voltage ripple ratio of 10% with a two-backbone-capacitor ($n = 2$) bipolar SSC energy buffer, the optimal number of supporting capacitors is six, (i.e., $m = 6$). Hence in the prototype, the electrolytic capacitor is replaced by a 2-6 bipolar SSC energy buffer. The schematic of the energy buffer power circuit, including switch and gate drive implementation, is shown in Fig. 11. To meet the 10% voltage ripple requirement at the 320 V bus voltage and the 135 W output power level, the eight capacitors of the SSC energy buffer (C_{11} , C_{12} , C_{21} , C_{22} , C_{23} , C_{24} , C_{25} and C_{26}) have to be about $2.2 \mu\text{F}$ each. The required voltage ratings of these film capacitors are different and range from 32 V to 512 V as shown in Table I and discussed in section IV. However, for simplicity and to provide adequate safety margin, 700 V film capacitors are used as the two backbone capacitors (C_{11} and C_{12}) and 250 V capacitors are used as the six supporting capacitors. The forward & reverse voltage blocking and current carrying capability of all the switches are listed in Table II. Each switch has to carry a peak current of about 0.5 A. Only switches S_{22} , S_{23} , S_{24} and S_{25} of Fig. 4 must have bi-directional voltage blocking capability. However, for simplicity switches S_{11} , S_{12} , S_{21} , S_{22} , S_{23} , S_{24} , S_{25} and S_{26} are all implemented with bi-directional voltage-blocking capability using two power MOSFETs in anti-series with sources tied together as shown in Fig. 11. All the switches are silicon power MOSFETs (STMicroelectronics STP12NK Series). The switches' source voltages are floating during operation. As a result, all the gate drivers for these switches need to be isolated. They are implemented with Analog Device ADuM5230 isolated gate driver to provide

TABLE I
REQUIRED CAPACITANCE, VOLTAGE AND CURRENT RATING OF THE CAPACITORS IN THE SSC ENERGY BUFFER (THE NORMALIZED VOLTAGE RATING IS NORMALIZED TO THE NOMINAL BUS VOLTAGE ($V_{\text{bus}}=320 \text{ V}$), AND THE NORMALIZED CURRENT RATING IS NORMALIZED TO THE AVERAGE OUTPUT CURRENT ($I_{\text{avg}}=0.420 \text{ A}$)). NOTE THAT THE SINGLE CAPACITOR THAT THIS BUFFER REPLACES IS A $40 \mu\text{F}$ ELECTROLYTIC CAPACITOR RATED AT 450 V.

Capacitor	Capacitance	Voltage rating	Normalized voltage rating (V/V_{bus})	Current rating	Normalized current rating (I/I_{avg})
C_{11}	$2.2 \mu\text{F}$	512 V	1.6	0.420 A	1.000
C_{12}	$2.2 \mu\text{F}$	512 V	1.6	0.420 A	1.000
C_{21}	$2.2 \mu\text{F}$	192 V	0.6	0.420 A	1.000
C_{22}	$2.2 \mu\text{F}$	160 V	0.5	0.418 A	0.996
C_{23}	$2.2 \mu\text{F}$	128 V	0.4	0.414 A	0.986
C_{24}	$2.2 \mu\text{F}$	96 V	0.3	0.406 A	0.968
C_{25}	$2.2 \mu\text{F}$	64 V	0.2	0.396 A	0.943
C_{26}	$2.2 \mu\text{F}$	32 V	0.1	0.382 A	0.909

TABLE II
REQUIRED FORWARD & REVERSE VOLTAGE BLOCKING AND CURRENT CARRYING CAPABILITY OF THE POWER SWITCHES (NORMALIZED TO NOMINAL BUS VOLTAGE ($V_{\text{bus}}=320 \text{ V}$), AND AVERAGE OUTPUT CURRENT ($I_{\text{avg}}=0.420 \text{ A}$)).

Switch	Forward blocking voltage	Normalized forward blocking voltage (V/V_{bus})	Reverse blocking voltage	Normalized reverse blocking voltage (V/V_{bus})	Peak current	Normalized peak current (I/I_{avg})
S_{11}	0 V	0	384 V	1.2	0.420 A	1.000
S_{12}	384 V	1.2	0 V	0	0.420 A	1.000
S_{21}	0 V	0	192 V	0.6	0.420 A	1.000
S_{22}	64 V	0.2	160 V	0.5	0.418 A	0.996
S_{23}	96 V	0.3	128 V	0.4	0.414 A	0.986
S_{24}	128 V	0.4	96 V	0.3	0.406 A	0.968
S_{25}	160 V	0.5	64 V	0.2	0.396 A	0.943
S_{26}	192 V	0.6	0 V	0	0.382 A	0.909
S_{h1}	0 V	0	192 V	0.6	0.420 A	1.000
S_{h2}	192 V	0.6	0 V	0	0.420 A	1.000
S_{h3}	192 V	0.6	0 V	0	0.420 A	1.000
S_{h4}	0 V	0	192 V	0.6	0.420 A	1.000

independent and isolated high-side and low-side outputs. In order to increase the drive current, a Fairchild FAN3111 gate driver is placed between the ADuM5230 and the power MOSFET.

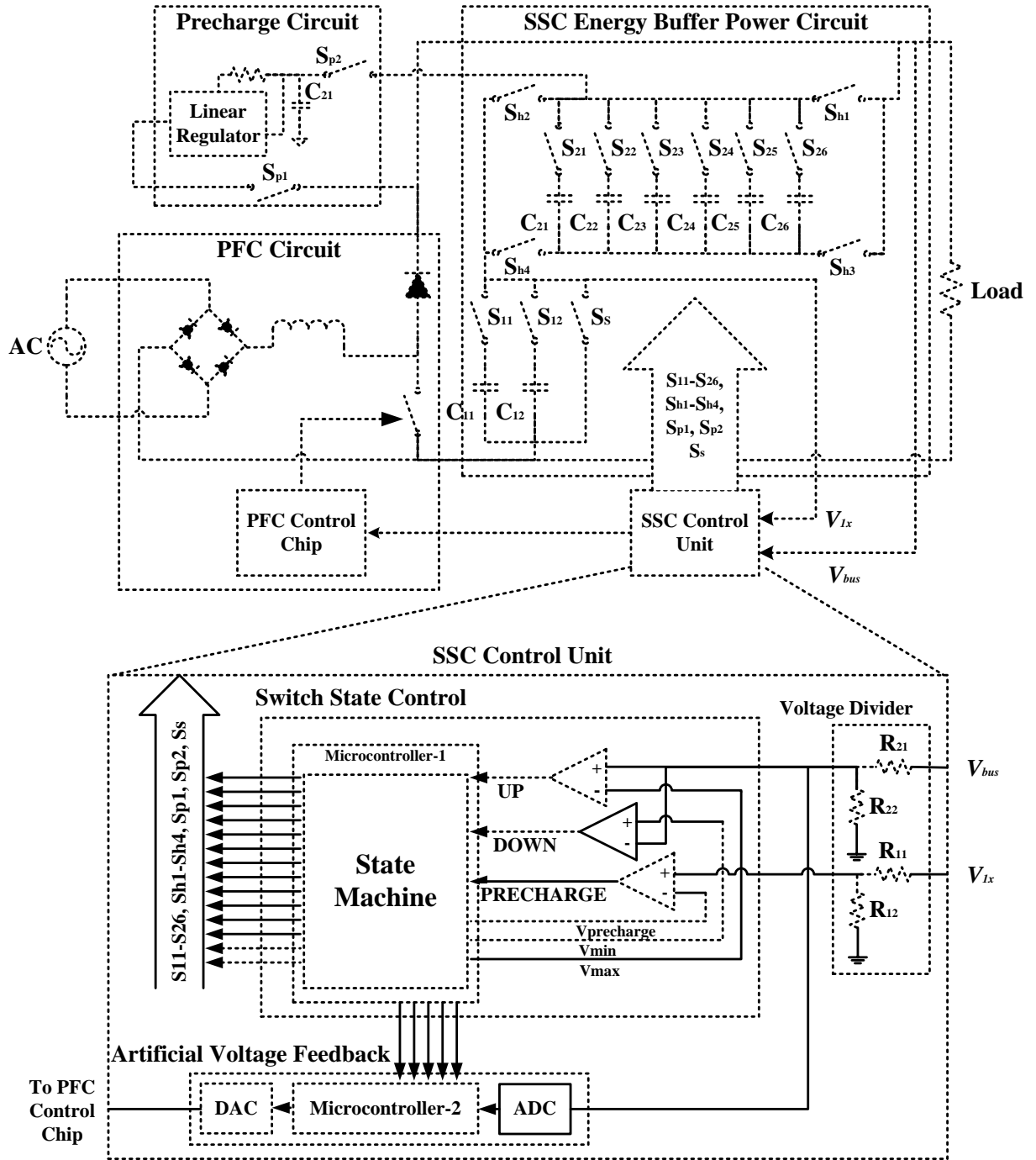


Fig. 10. Schematic of the prototype system consisting of a power factor correction (PFC) ac-dc converter, a dc load and the prototyped SSC energy buffer. The prototyped SSC energy buffer consists of: the SSC energy buffer power circuit, the precharge circuit, and the control unit.

B. Precharge Circuit

An important part of the SSC energy buffer is the precharge circuit. When the system starts, the precharge circuit draws power from the PFC to charge the individual capacitors of the energy buffer to the desired initial voltage levels. The precharge circuit designed here uses a Supertex LR8 linear regulator (with a maximum output current of 20 mA) operated as a current source, as shown in Fig. 10. The linear regulator can be disconnected from the energy buffer power circuit by two isolating switches S_{p1} and S_{p2} .

C. Control Unit

The precharge circuit and the SSC energy buffer power circuit are both controlled by an ATMEL ATmega2560 microcontroller as shown in Fig. 10. During precharge, the microcontroller turns the switches on or off appropriately to connect the current source to the capacitor that needs to be charged. The states (on or off) of the switches for charging a particular capacitor during the precharge period are shown in Table III. First S_{p1} , S_{p2} , S_{21} , S_{h4} and S_s are turned on, and all the other switches are turned off to charge C_{21} .

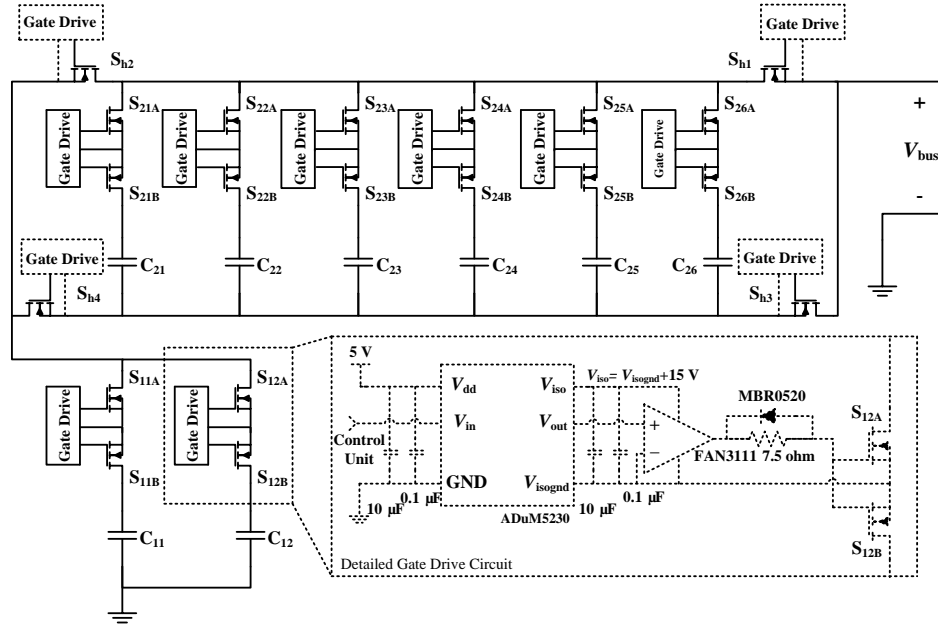


Fig. 11. Schematic of the energy buffer power circuit. ADuM5230 is an isolated gate drive which contains an integrated dc-to-dc converter. It powers and drives the FAN3111 (a low-side gate drive with a larger output current) which in turn drives the power MOSFETs. S_{h1} , S_{h2} , S_{h3} , S_{h4} , S_{11A} , S_{11B} , S_{12A} and S_{12B} are 800 V power MOSFETs (STP12NK80Z). S_{21A} , S_{21B} , S_{22A} , S_{22B} , S_{23A} , S_{23B} , S_{24A} , S_{24B} , S_{25A} , S_{25B} , S_{26A} and S_{26B} are 400 V power MOSFETs (STP12NK40Z).

TABLE III
STATE OF THE SWITCHES DURING PRECHARGE OF EACH OF THE EIGHT CAPACITORS (BLANK CELL INDICATES THAT THE SWITCH IS OFF).

	C_{11}	C_{12}	C_{21}	C_{22}	C_{23}	C_{24}	C_{25}	C_{26}
S_{11}	on							
S_{12}		on						
S_{21}			on					
S_{22}				on				
S_{23}					on			
S_{24}						on		
S_{25}							on	
S_{26}								on
S_{h1}								
S_{h2}	on	on						
S_{h3}								
S_{h4}			on	on	on	on	on	on
S_{p1}	on	on	on	on	on	on	on	on
S_{p2}	on	on	on	on	on	on	on	on
S_s			on	on	on	on	on	on

The microcontroller senses the voltage of C_{21} (through the voltage divider formed by R_{21} and R_{22}) and compares it with the specified precharge voltage ($0.5V_{nom}=160$ V). Once the voltage of C_{21} reaches 160V, S_{21} is turned off and S_{22} is turned on to charge C_{22} to its specified precharge level. Similarly, C_{23} , C_{24} , C_{25} and C_{26} are charged one at a time to their designed initial level. Once C_{26} is charged, S_{26} , S_{h4} and S_s are turned off, and S_{h2} and S_{11} are turned on to charge C_{11} . Now the microcontroller senses the voltage of C_{11} (through the voltage divider formed by R_{11} and R_{12}) and compares it with the specified precharge voltage ($0.4V_{nom}=128$ V). Once the voltage of C_{11} is larger than 128 V, S_{11} is turned off and S_{12} is turned on to charge C_{12} . Once all the capacitors are precharged, the precharge circuit is disconnected from the SSC energy buffer by switches S_{p1} and S_{p2} , and the energy buffer

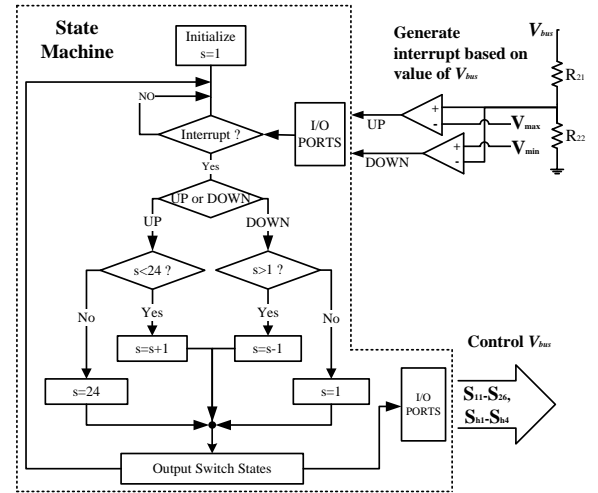


Fig. 12. Flow chart showing the logic of the state machine during the normal operation of the 2-6 bipolar SSC energy buffer. The state machine controls the on/off state of the power switches. The interrupts (\overline{UP} and \overline{DOWN}) which cause the switch states to change are generated when the bus voltage (V_{bus}) reaches a specified upper (V_{max}) or lower threshold (V_{min}), as shown here and in Fig. 10.

enters normal operation.

The normal operation of the energy buffer is also controlled by a state machine implemented in the ATMEL ATmega2560 microcontroller. The state machine controls the state (on or off) of the twelve switches in the SSC energy buffer power circuit. The state machine has a total of 24 states, with each state corresponding to a unique and valid combination of the states of the twelve switches, as shown in Table IV.

The flow chart of the normal operating mode control logic of the state machine is shown in Fig. 12. In this flow

chart, s denotes the current state of the state machine. The energy buffer starts normal operation in state 1 (i.e., $s=1$), which corresponds to minimum energy stored in the buffer, and starts to charge up. Once the bus voltage reaches the maximum allowed voltage, $1.1V_{\text{nom}}$ (352 V), the $\widehat{\text{UP}}$ interrupt is triggered and the state is incremented by one (i.e., $s=s+1$). The microcontroller turns the appropriate power switches on or off to match the configuration for the new state. This drops the bus voltage back to $0.9V_{\text{nom}}$ (288 V), and the charging of the energy buffer continues until it again reaches the upper voltage limit. This process is repeated as long as the energy buffer is being charged and it has not reached state 24. Once the energy buffer has reached state 24, the state machine stays in state 24 even if it receives additional $\widehat{\text{UP}}$ interrupts. This helps protect the energy buffer to a certain extent in case load power exceeds its design specifications. During this overload condition the energy buffer looks like a $1.1 \mu\text{F}$ capacitor to the external system. The energy buffer will return to normal operation once the load power returns to the design range.

During discharge of the energy buffer, the $\widehat{\text{DOWN}}$ interrupt is triggered when the bus voltage reaches the minimum allowed voltage, $0.9V_{\text{nom}}$ (288 V). This decrements the state by one (i.e., $s=s-1$). The microcontroller turns the appropriate power switches on and off to match the configuration for the new state and the bus voltage increases to $1.1V_{\text{nom}}$ (352 V). This process is repeated each time the bus voltage reaches the lower voltage limit until it has reached state 1. As in the case of charging, to protect the energy buffer, the state machine stays in state 1 even if it receives additional $\widehat{\text{DOWN}}$ interrupts.

Hence during normal operation at maximum power, the state machine will iterate through states 1 through 24 in a sequential manner, first going from 1 to 24 as it charges, and then returning from 24 to 1 as it discharges, and this process is repeated as long as the energy buffer is in normal operation.

D. Artificial Voltage Feedback

In a conventional system with an electrolytic capacitor at the output of the PFC for energy buffering, the PFC uses the bus voltage (i.e., the voltage across the buffering capacitor) to control its output current. The bus voltage is scaled down by a resistive divider and fed back to the PFC control chip. Since the bus voltage is a good measure of the energy stored in the capacitor, this feedback mechanism ensures that the average output power from the PFC matches the power drawn by the dc load and the system stays stable. However, when the electrolytic capacitor is replaced with the SSC energy buffer, the bus voltage may no longer be a true representation of the energy stored in the energy buffer.

In the precharge mode, the SSC energy buffer behaves simply like two capacitors connected in series. Hence, during this period the bus voltage reflects the energy stored in the two capacitors and the voltage that needs to be fed back is simply a scaled version of the bus voltage. However, once the SSC energy buffer enters normal operating mode, the bus voltage does not represent the energy stored in the buffer. Hence, an artificial signal must be generated (and fed back to the PFC control chip, as shown in Fig. 10.) that represents the energy

stored in the energy buffer and mimics the bus voltage of the electrolytic capacitor. In our prototype this signal is generated by a second ATMEL ATmega2560 microcontroller.

The energy stored in the SSC energy buffer increases monotonically as it goes from state 1 to state 24 and then decreases monotonically as it returns to state 1. The energy that gets stored in the energy buffer as it goes from state 1 to state 24 is given by:

$$\Delta E(t) = \sum_{i=1}^N \frac{1}{2} C_i (V_i(t)^2 - V_{i0}^2), \quad (5)$$

where N is the total number of capacitors in the energy buffer (eight in the 2-6 bipolar SSC case), C_i is the capacitance of capacitor i , $V_i(t)$ is the voltage of capacitor i at time t , and V_{i0} is the initial voltage of capacitor i after it is precharged. In our prototype all eight capacitors have the same capacitance (i.e., $C_i = 2.2 \mu\text{F}$ for all i). The effective energy in the energy buffer as a function of time is given by³:

$$E_{\text{b(eq)}}(t) = \frac{1}{2} C_{\text{eq}} V_{\text{min}}^2 + \Delta E(t), \quad (6)$$

where V_{min} is the minimum value of the bus voltage, and C_{eq} is an equivalent capacitance for this energy buffer valid while it is in normal operating mode, and is given by:

$$C_{\text{eq}} = \frac{2 \int_{t_1}^{t_2} p(t) dt}{V_{t_2}^2 - V_{t_1}^2}. \quad (7)$$

Here $p(t)$ is the power flowing into the energy buffer, and V_{t_1} and V_{t_2} are the voltages at the beginning (time t_1) and the end (time t_2) of the charging period, respectively. For our prototype, C_{eq} is equal to $26.4 \mu\text{F}$. The effective energy in the energy buffer can also be expressed as:

$$E_{\text{eq}}(t) = \frac{1}{2} C_{\text{eq}} V_{\text{fb}}^2(t), \quad (8)$$

where $V_{\text{fb}}(t)$ is the apparent voltage that needs to be fed back to the PFC. $E_{\text{eq}}(t)$ needs to be equal to $E_{\text{b(eq)}}(t)$, hence V_{fb} is given by:

$$V_{\text{fb}}(t) = \sqrt{\frac{C_{\text{eq}} V_{\text{min}}^2 + 2\Delta E(t)}{C_{\text{eq}}}}. \quad (9)$$

This feedback signal reflects the apparent energy stored in the energy buffer.

While the expression given by Eq. 9 for the normal operating mode feedback signal can be implemented, it is simpler to implement an approximation to this expression which works just as well within the resolution of our 8-bit DAC. The approximate feedback signal is derived assuming that the feedback voltage signal is linear between two switching instances and the current flowing into or out of the energy buffer is constant (i.e., current has a square profile). This approximate feedback voltage is given by:

³Note that $E_{\text{b(eq)}}$ as given by Eq. 6 is not the actual energy in the energy buffer but rather the apparent energy.

TABLE IV
STATES OF THE TWELVE SWITCHES CORRESPONDING TO EACH OF THE 24 STATES OF THE STATE MACHINE (BLANK CELL INDICATES THAT THE SWITCH IS OFF).

States	S ₂₁	S ₂₂	S ₂₃	S ₂₄	S ₂₅	S ₂₆	S ₁₁	S ₁₂	S _{h1}	S _{h2}	S _{h3}	S _{h4}
1	on						on		on			on
2		on					on		on			on
3			on				on		on			on
4				on			on		on			on
5					on		on		on			on
6						on	on		on			on
7						on	on			on	on	
8					on		on			on	on	
9				on			on			on	on	
10			on				on			on	on	
11		on					on			on	on	
12	on						on			on	on	
13	on							on	on			on
14		on						on	on			on
15			on					on	on			on
16				on				on	on			on
17					on			on	on			on
18						on		on	on			on
19						on		on		on	on	
20					on			on		on	on	
21				on				on		on	on	
22			on					on		on	on	
23		on						on		on	on	
24	on							on		on	on	

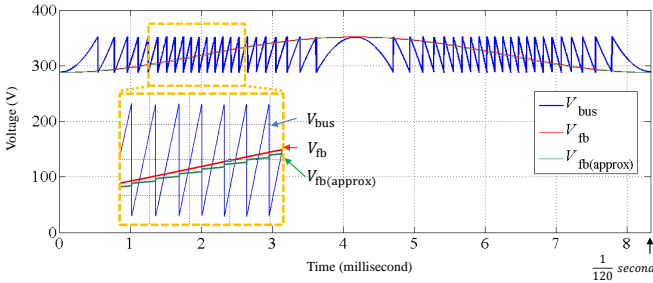


Fig. 13. Comparisons between the accurate (V_{fb}) and approximate ($V_{fb(approx)}$) artificial feedback voltages for a sinusoidal energy buffer terminal current. The $V_{fb(approx)}$ is fed back to the PFC in the prototype. This feedback mechanism ensures that the average output power from the PFC matches the power drawn by the dc load and the system stays stable.

$$V_{fb(approx)}(t) = V_{min} + (V_{max} - V_{min}) \frac{i}{24} + (V_{bus}(t) - V_{min}) \frac{C_b}{2C_{eq}}. \quad (10)$$

Figure 13 shows that this approximate feedback signal matches the more accurate one quite well even when the terminal current of the energy buffer is sinusoidal. It has been experimentally demonstrated that the slower outer control loop of the PFC works well with this approximate feedback signal.

VI. EXPERIMENTAL RESULTS

The prototype 2-6 bipolar SSC energy buffer has been successfully tested with the PFC and a load resistor up to

power levels of 135 W. The measured waveforms from the energy buffer operated at 100 W are shown in Fig. 14. As the energy flows into and out of the energy buffer at 120 Hz, the backbone capacitors charge and discharge over a wide voltage range. However, this voltage variation is compensated for by the supporting capacitors and the bus voltage remains within the 300 V and 370 V range. Hence, it meets the voltage ripple ratio design requirement of 10%.

A PLECS⁴ model for this energy buffer has also been built and simulated. In the simulation the terminal current of the energy buffer is assumed to be sinusoidal. Comparing Fig. 14 and Fig. 15, there is a reasonably close match between the experimental and simulated waveforms. The main difference is due to the fact that in the simulation the terminal current of the energy buffer is assumed to be perfectly sinusoidal, while in the case of the experimental setup that is not exactly the case. Figure 14(b) shows the state of the state machine. As can be seen, the state machine goes down to state 4 and up to state 24. The state machine does not go into states 1, 2 and 3 in its normal operating mode as the load power is not large enough to discharge it down to its minimum stored energy level. The circuit behaves as designed, and validates the concept of the stacked switched capacitor energy buffer. Fig. 16 compares how the bus voltage ripple changes when the SSC energy buffer is used instead of a single capacitor with the same energy capacity as the SSC energy buffer. Clearly the SSC energy buffer reduces the bus voltage ripple considerably compared to the single-capacitor energy buffer.

⁴PLECS is a simulation tool for power electronic circuits.

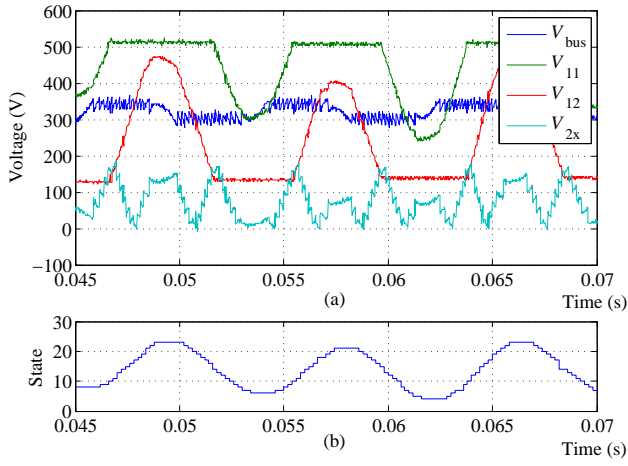


Fig. 14. Measured waveforms of (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (V_{2x}), and (b) corresponding state (1-24) of the state machine.

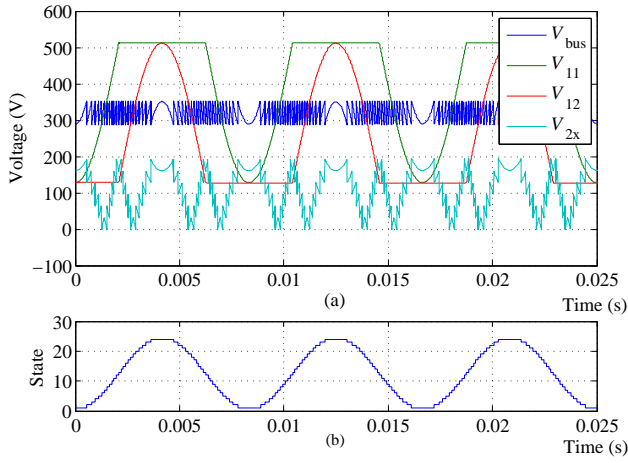


Fig. 15. Simulated waveforms of (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (V_{2x}), and (b) corresponding state (1-24) of the state machine.

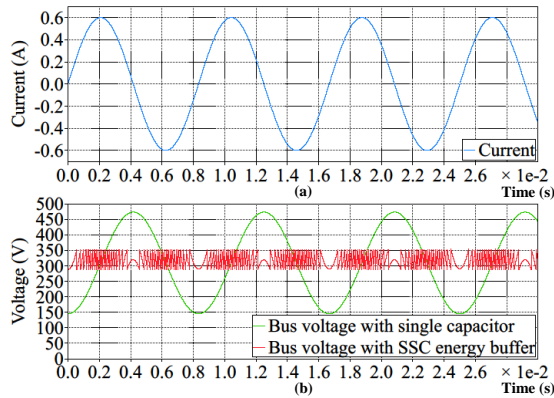


Fig. 16. Bus voltage ripple comparison between a single-capacitor and the SSC energy buffer with the same rated energy storage capability.

The control technique implemented in the SSC energy buffer directly handles transient conditions also. A change in load or supply simply alters the rate at which the state machine traverses its states, and makes it go through a wider or narrower range of states. Figure 17 shows the waveforms of the SSC energy buffer during startup with a 100 W load. The SSC energy buffer starts normal operation at $t = 0.009$ s. Before this, the power factor correction (PFC) circuit functions as a full-wave rectifier and limits the peak output voltage to 170 V. Also before start of normal operation, the backbone and supporting capacitors of the SSC energy buffer, except for C_{11} and C_{21} , are precharged to pre-specified voltage levels by the precharge circuit and the state of state machine is 1. During this time, C_{11} and C_{21} are connected in series across the bus to provide enough capacitance for the PFC to start operation. Once the SSC energy buffer starts normal operation, the state of the state-machine starts to increase and the PFC begins to charge the SSC energy buffer until the bus voltage reaches the designed threshold. In our prototype, it takes 3 cycles for the bus voltage to settle down within its designed 10% ripple range, and it takes 6 cycles for the states of the state-machine to reach periodic steady-state.

Figure 18 shows the waveforms of the SSC energy buffer during a load transient. At $t = 0.027$ s, the load changes from 50 W to 100 W. The SSC energy buffer now has to traverse across a wider range of states to buffer the additional power. However, due to its slower dynamics, the PFC cannot increase its output power very rapidly. Therefore, initially additional energy is extracted from the SSC energy buffer to maintain the bus voltage ripple within the designed range. Hence, the state of the state-machine goes down lower than would be needed in the steady-state. The SSC energy buffer reaches a new steady-state equilibrium in about two cycles, which is the time needed for the PFC to adjust its output to match the load. With the increased load the backbone capacitors (C_{11} and C_{12}) are charged and discharged across a wider voltage range, as can be seen from Fig. 18.

The round trip efficiency of the prototype 2-6 bipolar SSC energy buffer was measured for the 20 W to 127.6 W load power range. The measured efficiency, with and without the control and gate drive losses, is shown in Fig. 19 along with the measured efficiency of the electrolytic-capacitor-only and the film-capacitor-only solutions. Without including the control and gate drive losses, the efficiency of the SSC energy buffer stays above 95.2% throughout this power range. The peak measured efficiency is 97.0% at 127.6 W. If control and gate drive losses are included, the efficiency has a significant drop at low power levels.

The loss mechanisms in this prototype were determined using experimental measurements and data from component datasheets. The results are shown in Table V. Clearly the gate drivers are the largest contributor to losses in this prototype. In this prototype, the control and gate drive circuits were not designed for high efficiency. The control and gate drive losses can be minimized by appropriately designing these parts of the energy buffer, and would result in significant improvement in the overall efficiency of the system.

The prototype energy buffer successfully replaces the func-

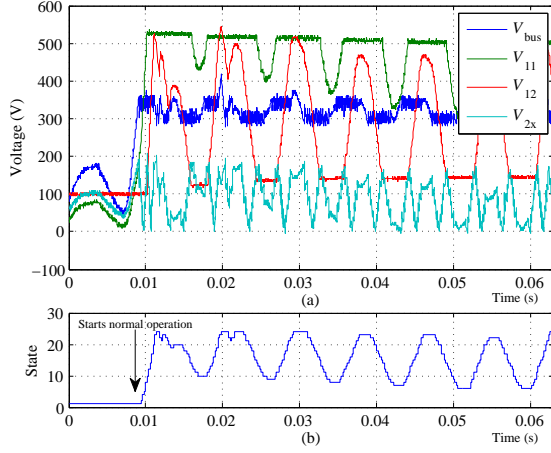


Fig. 17. Measured waveforms of the SSC energy buffer during startup: (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (V_{2x}), and (b) corresponding state (1-24) of the state machine. The SSC energy buffer starts normal operation at $t = 0.009$ s. It takes 3 cycles for the bus voltage (V_{bus}) to settle down within its designed ripple range, and it takes 6 cycles for the states of the state-machine to achieve periodic steady-state.

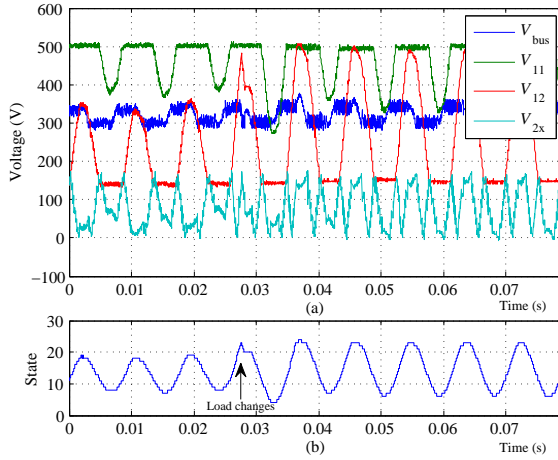


Fig. 18. Measured waveforms of the SSC energy buffer during a load transient: (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (V_{2x}), and (b) corresponding state (1-24) of the state machine. The load steps from 50 W to 100 W at $t = 0.027$ s. The state machine traverses through higher and lower states within the first cycle and the system settles down to a new equilibrium in two cycles.

TABLE V
ESTIMATED BREAK DOWN OF LOSSES

Component	Losses	Percentage
Gate Drivers (Adum5230)	3.0 W	44.77%
Voltage Dividers, Comparators, D/A and A/D Converters	1.0 W	14.93%
Microcontrollers (ATMEL ATmega2560)	0.2 W	2.98%
Conduction and Parasitic Loss	2.5 W	37.32%
Total	6.7 W	100%

tion of the electrolytic capacitor at the output of the PFC. Its passive volume of 20 cm^3 , which is much smaller than the

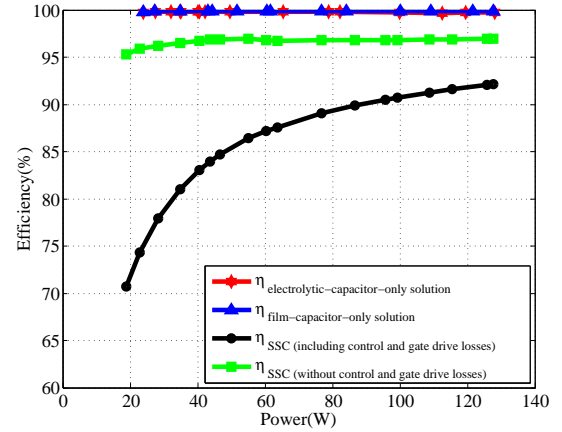


Fig. 19. Measured round-trip efficiency of the prototype 2-6 bipolar SSC energy buffer as a function of power drawn by the load, along with the round-trip efficiency of the electrolytic-capacitor-only and the film-capacitor-only solutions.

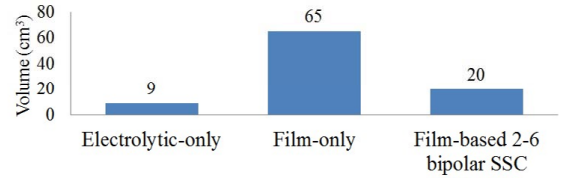
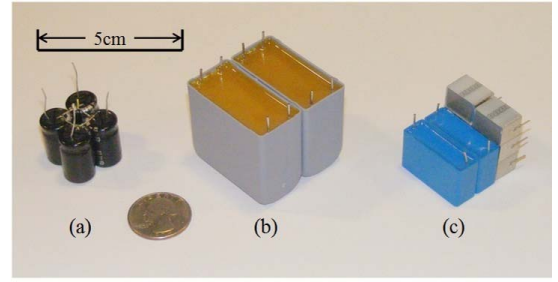


Fig. 20. Relative size of passive energy storage components in different energy buffer architectures: (a) electrolytic-capacitor-only (9 cm^3) (b) film-capacitor-only (65 cm^3) and (c) film-capacitor-based SSC (20 cm^3) energy buffer.

65 cm^3 needed for a film-capacitor-only solution, is only about twice the size of the 9 cm^3 electrolytic capacitor it replaces, as shown in Fig. 20. The total volume of the switches is 8 cm^3 , which is considerably less than the SSC energy buffer's passive volume, even though no attempt was made to minimize the size of the switches in the prototype. The switches, the precharge circuit and the control circuit can be made quite small with appropriate packaging and integration.

Hence, the film-capacitor-based SSC energy buffer achieves energy buffering density comparable to those of the electrolytic capacitors while providing much longer life.

VII. CONCLUSIONS

This paper introduces a stacked switched capacitor (SSC) architecture for dc-link energy buffering applications, including buffering between single-phase ac and dc. This architecture utilizes the energy storage capability of capacitors more effectively than previous designs, while maintaining the bus voltage within a narrow range. This enables the energy buffer

to achieve higher effective energy density and reduce the volume of the capacitors. A prototype 2-6 bipolar SSC energy buffer using film capacitors designed for a 320 V bus with 10% voltage ripple and able to support a 135 W load has been built and tested. It is shown that the SSC energy buffer can successfully replace limited-life electrolytic capacitors with much longer life film capacitors, while maintaining volume and efficiency at a comparable level.

ACKNOWLEDGMENT

The authors would like to thank James Page of Princeton, NJ, summer intern at MIT, for his help with collecting and analyzing film and ceramic capacitor data.

REFERENCES

- [1] M. Chen, *Stacked Switched Capacitor Energy Buffer Architecture*, SM Thesis, Dept. of EECS, Massachusetts Institute of Technology, Cambridge, MA, Dec. 2011.
- [2] M. Chen, K. K. Afridi and D. J. Perreault, "Stacked Switched Capacitor Energy Buffer Architecture," *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, Orlando, FL, Feb. 2012.
- [3] A. C. Kyritsis, E. C. Tatakis, "A Novel Parallel Active Filter for Current Pulsation Smoothing on Single Stage Grid-Connected AC-PV Modules," *Proceedings of the 11th European Conference on Power Electronics and Applications (EPE)*, Aalborg, Denmark, Sep. 2007.
- [4] A. C. Kyritsis, N. P. Papanikolaou and E. C. Tatakis, "Enhanced Current Pulsation Smoothing Parallel Active Filter for Single Stage Grid Connected AC-PV Modules," *Proceedings of the International Power Electronics and Motion Control Conference (EPE-PEMC)*, pp. 1287-1292, Poznan, Poland, Sep. 2008.
- [5] T. Shimizu, K. Wada and N. Nakamura, "Flyback-Type Single-Phase Utility-Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1264-1272, Sep. 2006.
- [6] S. B. Kjaer and F. Blaabjerg, "Design Optimization of a Single-Phase Inverter for Photovoltaic Applications," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 1183-1190, Acapulco, Mexico, Jun. 2003.
- [7] P. T. Krein and R. S. Balog, "Cost-Effective Hundred-Year Life for Single-Phase Inverters and Rectifiers in Solar and LED Lighting Applications Based on Minimum Capacitance Requirements and a Ripple Power Port," *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, pp. 620-625, Washington, DC, Feb. 2009.
- [8] B. J. Pierquet and D. J. Perreault, "Single-Phase Photovoltaic Inverter Topology with Series-Connected Power Buffer," *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2010.
- [9] P. Lin and L. Chua, "Topological Generation and Analysis of Voltage Multiplier Circuits," *IEEE Transactions on Circuits and Systems*, vol. 24, no. 10, pp. 517-530, Oct. 1977.
- [10] S. V. Cheong, S. H. Chung and A. Ioinovici, "Development of Power Electronics Converters based on Switched-Capacitor Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1907-1910, May. 1992.
- [11] C. K. Tse, S. C. Wong and M. H. L. Chow, "The Simplest Lossless Switched-Capacitor AC/DC Converter," *Proceedings of the 25th Annual IEEE Power Electronics Specialists Conference (PESC)*, pp. 1212-1217, Jun. 1994.
- [12] M. S. Makowski and D. Maksimovic, "Performance Limits of Switched-Capacitor DC-DC Converters," *Proceedings of the 26th Annual IEEE Power Electronics Specialists Conference (PESC)*, pp. 1215-1221, Jun. 1995.
- [13] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *IEEE Transactions on Power Electronics*, pp. 841-851, Mar. 2008.
- [14] A. Rufer and P. Barrade, "A Supercapacitor-Based Energy Storage System for Elevators with Soft Commutated Interface," *IEEE Transactions on Industry Applications*, vol. 38, issue 5, pp. 1151-1159, Oct. 2002.
- [15] S. Sugimoto, S. Ogawa, H. Katsukawa, H. Mizutani and M. Okamura, "A Study of Series-Parallel Changeover Circuit of a Capacitor Bank for an Energy Storage System Utilizing Electric Double-layer Capacitors," *Electrical Engineering in Japan*, vol. 145, pp. 33-42, 2003.
- [16] X. Fang, N. Kutkut, J. Shen and I. Batarseh, "Ultracapacitor Shift Topologies with High Energy Utilization and Low Voltage Ripple," *International Telecommunications Energy Conference (INTELEC)*, Orlando, FL, Jun. 2010.
- [17] J. G. Kassakian, M. F. Schlecht and G. C. Verghese, *Principles of Power Electronics*, pp. 126, Addison-Wesley, New York, 1991.
- [18] R. C. N. Pilawa-Podgurski, D. Giuliano and D. J. Perreault, "Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 4008-4015, Rhodes, Greece, Jun. 2008.
- [19] K. K. Afridi, M. Chen, and D. J. Perreault, "Enhanced Bipolar Stacked Switched Capacitor Energy Buffers," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4209 - 4216, Raleigh, NC, Sep. 2012.



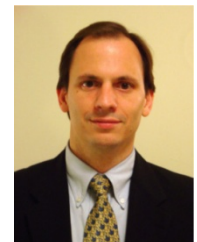
Tsinghua University and the E.E Landsman Fellowship from MIT.

Minjie Chen (S'10) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China in 2009, and the S.M. degree from the Massachusetts Institute of Technology (MIT) in 2012, where he is currently working towards the Ph.D degree. His research interests include analysis and design of high-frequency, high-energy-density power electronics, focusing on resonant converters, soft switching techniques, active energy-buffering techniques and high-frequency-link dc-ac inverters. He received the outstanding student scholarship from



School of Science and Engineering (SSE) as Project Director, and was appointed Associate Professor and the Werner-von-Siemens Chair for Power Electronics in 2008. Since 2009 he is at MIT as a Visiting Associate Professor in the Department of Electrical Engineering and Computer Science. His research interests are in power electronics and its applications in smart electric grids. Dr. Afridi received the Carnation Merit Award from Caltech and the BMW Scientific Award from BMW AG.

Khurram K. Afridi (S'93–M'98) received the B.S. degree in electrical engineering from the California Institute of Technology (Caltech) in 1989 and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT) in 1992 and 1998, respectively. Between degrees he worked for JPL, Lutron, Philips, and Schlumberger. In 1997, he joined the founding team of Techlogix as Chief Technology Officer and became Chief Operating Officer in 2000. From 2004 to 2008 he also led the development of LUMS



IEEE prize papers. His research interests include design, manufacturing, and control techniques for power electronics, and their use in a wide range of applications. Dr. Perreault received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society, an Office of Naval Research Young Investigator Award, and the Society of Automotive Engineers Ralph R. Teetor Educational Award.

David J. Perreault (S'91–M'97–SM'06) received the B.S. degree from Boston University, Boston, MA, in 1989, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 1991 and 1997, respectively. In 1997, he joined the Laboratory for Electromagnetic and Electronic Systems, MIT as a Postdoctoral Associate, and became a Research Scientist in 1999. In 2001, he joined the Department of Electrical Engineering and Computer Science, MIT, where he is currently a Professor. He has coauthored four