Investigation of Noise Sources in Scaled CMOS Field–Effect Transistors

by

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

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Abstract

This thesis is a study of noise in CMOS field effect transistors, and the effects of scaling on high frequency low noise circuit design. A graphical derivation of the intrinsic noise sources in a square-law MOSFET transistor that includes the drain noise current, the gate noise current, and their correlation is presented. In this derivation, the channel is modeled as a series connection of differential conductances that generate thermal noise. However, it is well established that as CMOS transistors are scaled, carrier transport in the channel becomes velocity saturated. This effect changes the channel noise generation mechanisms because the channel is no longer ohmic in nature. Based on the noise analysis of velocity saturated MESFET transistors[1],[2], it is expected that the correlation between the drain noise current and the induced gate noise current increases. The increase in correlation should result in a lower noise figure for amplifiers designed with these devices than would be predicted without accounting for the increased correlation. To test this hypothesis, transistors are fabricated in an advanced 0.15 μm, 1.5 V CMOS process courtesy of Texas Instruments. Measurements of the DC performance curves, gate tunneling current, transconductance, output resistance, and unity current gain frequency(f_T) are presented for a subset of the devices. A measurement setup for obtaining the noise parameters of the devices is presented and discussed. Future directions in the areas of modeling and circuit design are indicated.

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Chapter 1

Introduction

1.1 Noise

Noise is probably one of the most overused terms in electrical engineering. In general, noise is used to describe any unwanted signal. In its strictest definition, noise should be reserved to describe only those signals that are random. If the signal can be predicted or triggered on a scope, then it is not noise[3]. The two noise processes that are of interest here are thermal noise and shot noise. Thermal noise, also know as Nyquist noise or Johnson noise, originates from random electron motion in a conductor. The available power (P_n) from a thermal noise source is equal to $kT\,\Delta f$, where k is Boltzmann's constant,[1] T is the temperature of the conductor in Kelvin, and Δf is the bandwidth of interest.[2] Shot noise results from a direct current that is the result of a random process. Commonly, the random process is electrons crossing an energy barrier. The current then has an average value of I_{DC}, and a variance of $\overline{i^2} = 2q\,I_{DC}\,\Delta f$. As an order of magnitude calibration, the available thermal noise power in a 100 MHz bandwidth is 0.4 pW, and the shot noise power of a 100 μA current delivered to 50 Ω load in the same 100 MHz bandwidth is 0.16 pW.

[1] $k = 1.38 \times 10^{-23}$ J/K

[2] A useful reference is $P_n/\Delta f = kT \approx 4 \times 10^{-21}$ W/Hz at room temperature($T = 290$ K)

1.2 Motivation

Although the power[3] of these noise sources is low, they impose a physical limit on the minimum detectable signal of a circuit or system. Of specific interest in this work is the minimum detectable signal of a receiver. Because of the prospect of low cost and high integration of scaled CMOS, much effort is being focused on its use for radio–frequency(RF) communication circuits. Low noise amplifiers(LNA) are essential building blocks for the design of communication devices. MOS transistors have been typically considered to be the noisiest transistor technology, but with the scaling of channel length, MOS transistors have f_T s[4] in the tens of giga-Hertz. High f_T results in gain out to higher frequencies, and a lower noise figure at those frequencies. The focus of this thesis is the intrinsic noise mechanisms of CMOS transistors, and their relation to low noise circuit design. Both NMOS and PMOS devices are examined experimentally, but it is expected that PMOS devices are inferior to NMOS devices because of their lower transconductance. The question to be answered is how to design the best LNA with a scaled CMOS technology.

1.3 Organization

The organization of this thesis is as follows: Chapter 2 presents a graphical view of the classic long channel noise derivation, hypothesizes a simple short channel theory based on Pucel et. al.[2], and briefly discusses other modern noise theories for MOSFETs. Chapter 3 discusses the measurement techniques used to determine the noise parameters of the intrinsic device from on wafer measurements. Chapter 4 presents the measurement results, and Chapter 5 draws conclusions from the measured data and suggests future direction in the application of the results.

[3]Equivalently, voltage and current can be used if an impedance is defined.

[4]f_T is the transistor unity current gain frequency

Chapter 2

Noise in MOSFETs

2.1 Long Channel Noise Theory

The classic long channel noise theory for intrinsic FET transistors proposed by van der Ziel[4],[5] defines two noise sources that are present at the device terminals. The first is the drain noise current which originates from the conductance of the channel, and the second is the induced gate noise current which originates from the charge fluctuations in the channel when the drain current fluctuates. This description implies that the two would be completely correlated, but this is not the case. To be sure, they are dependent on each other, but due to the active nature of the channel, the two are only partially correlated.[1] Together, these sources give a complete description of the device noise suitable for a two-port Y-Parameter model (Figure 2-1).

While the mathematical derivation of the drain noise current and the induced gate noise current is covered elsewhere ([6], [7], [8] [9]), a graphical approach to the derivation is presented here that originates from a graph of channel potential given in [7] and [9]. First, the derivation of the drain noise current, induced gate noise current, and correlation is presented for $V_{DS} = 0\,\mathrm{V}$. Then, the derivation is re-examined as V_{DS} approaches V_{Dsat}, and the results for saturation are presented.

[1] Correlation is a measure of linear dependence.

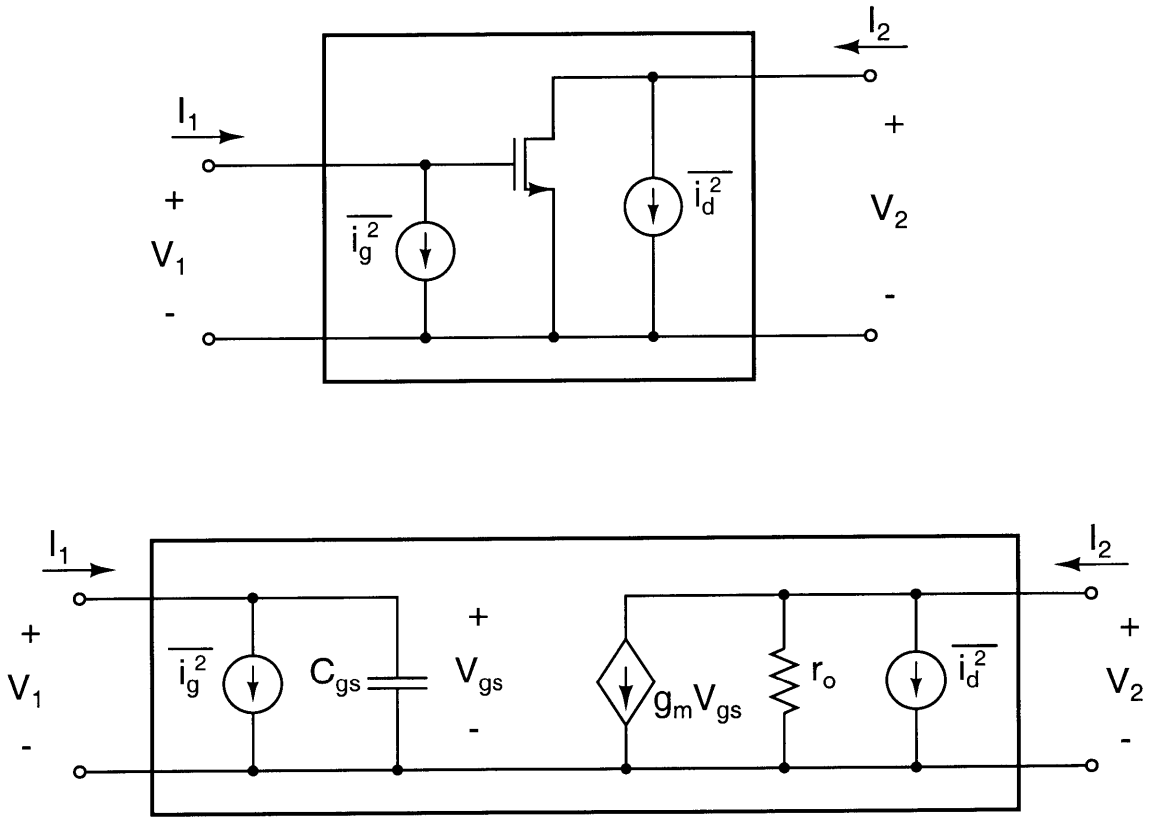

Figure 2-1: Intrinsic Noise Model

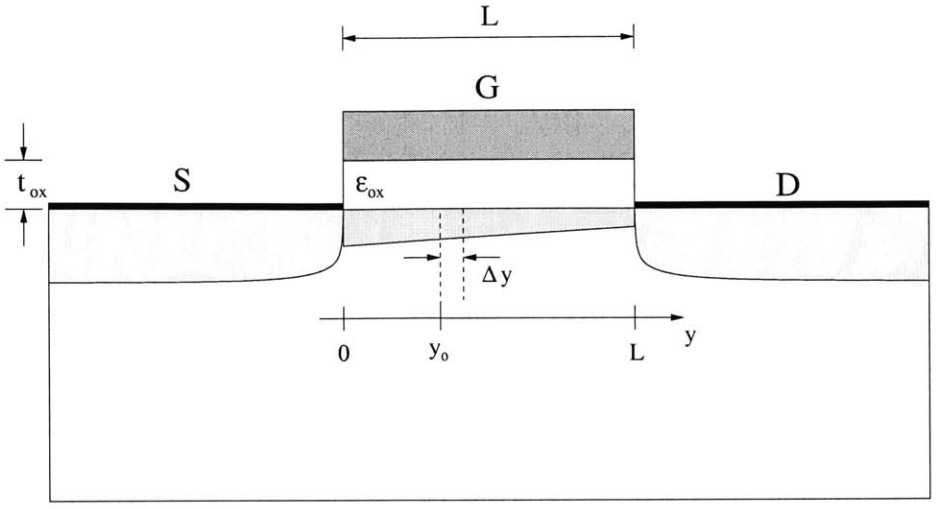

Figure 2-2: Differential MOSFET Model

The starting point for the derivation is the classic long channel MOSFET model given in Figure 2-2. This is the model commonly use to derive the drain current I_D as a function of V_{GS} and V_{DS} in the triode[2] region. The familiar differential equation defining the drain current is

$$I_D = WQ_c(y)\mu\frac{dV}{dy} \tag{2.1}$$

Rearranging terms gives something more suitable for the noise derivation.

$$I_D = \frac{g_d(y)}{dy}\,dV \tag{2.2}$$

where

$$g_d(y) = W\mu C_{ox}\left(V_{GS} - V(y) - V_T\right) \qquad (\mathrm{S}\cdot\mathrm{cm}) \tag{2.3}$$

The channel can be thought of as a series connection of differential conductances or resistances. Because a resistance has thermal noise $\overline{v^2} = 4kTR\,\Delta f$, the small signal change in the drain current(Δi_d) can be determined using the model in Figure 2-3

[2]Also called the linear region.

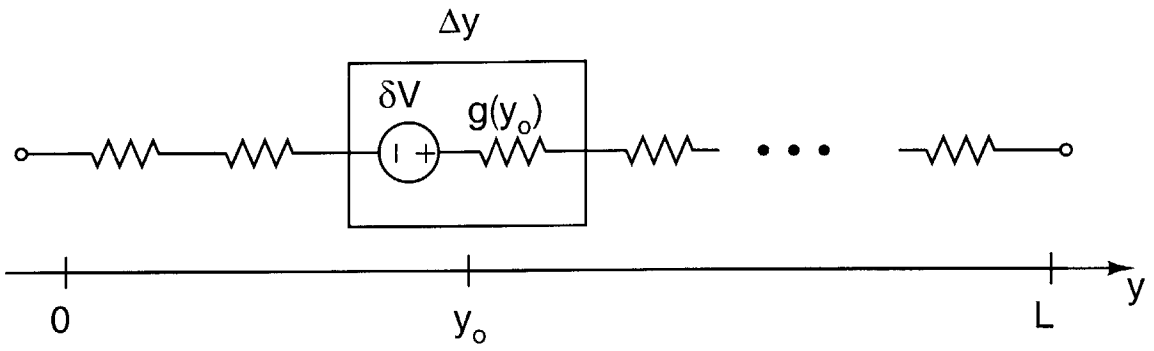

Figure 2-3: Differential Conductance MOSFET Model

where

$$\overline{\delta V^2} = 4kT\frac{dy}{g_d(y_o)}\Delta f \tag{2.4}$$

To determine the conductance value of each differential channel piece, the potential distribution in the channel must be known. Starting with the simplest case where $V_{DS} = 0\,\mathrm{V}$, the channel potential is simply

$$V_o(y) = 0 \tag{2.5}$$

The top graph in Figure 2-4 is a sketch of change in channel potential for noise voltages at three different positions (y_{o1}, y_{o2}, y_{o3}) where

$$\Delta V = V(y) - V_o, \tag{2.6}$$

$V(y)$ is the disturbed channel potential, and V_o is the nominal channel potential. Notice that the mean value of the disturbance is zero, and the magnitude of the discontinuity at y_o is δV. For $V_{DS} = 0$, the magnitude of the disturbances is constant as a function of channel position because the channel charge and the differential conductance are independent of position.

$$Q_c(y) = C_{ox}(V_{GS} - V_T) = Q_c \tag{2.7}$$

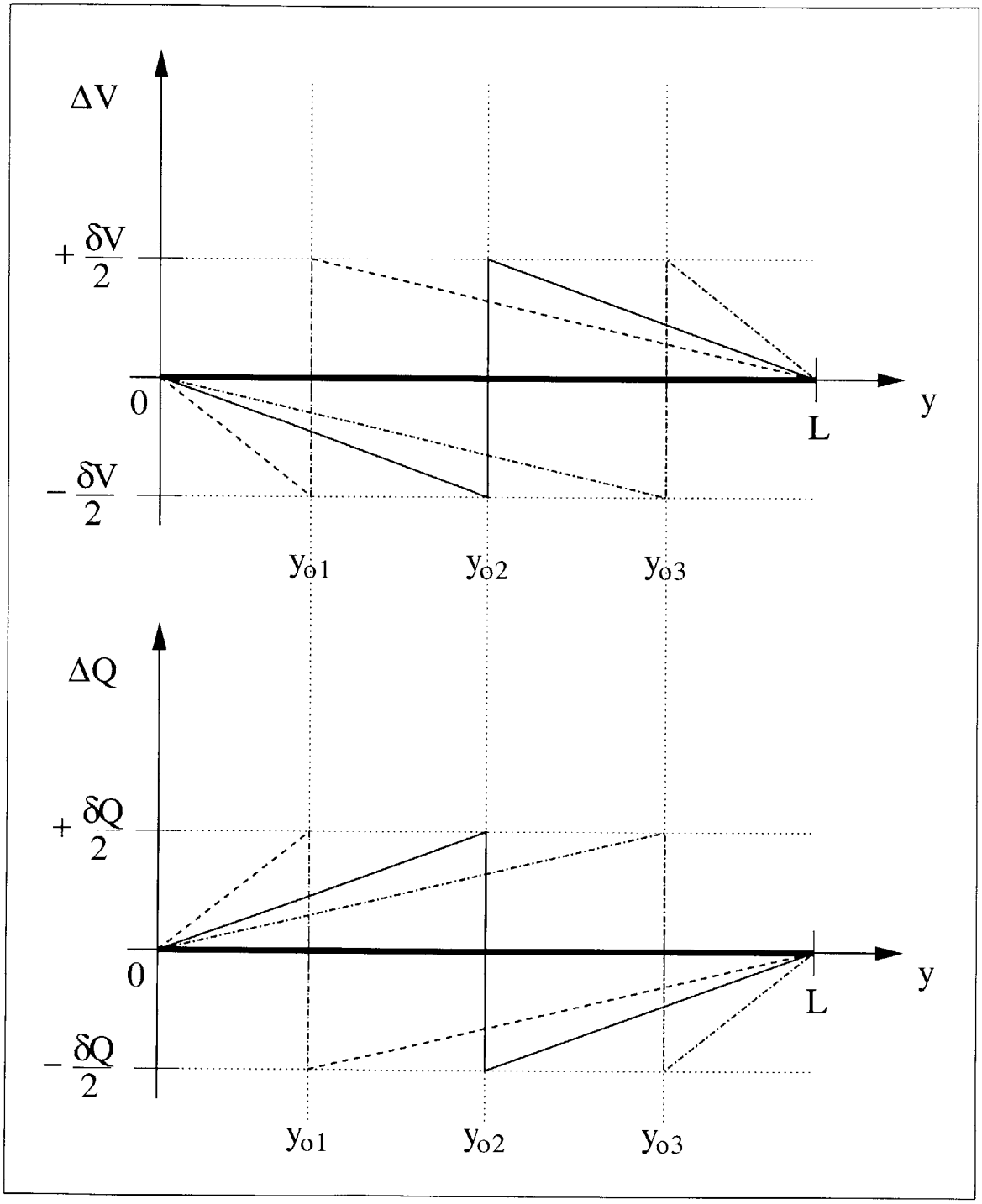

Figure 2-4: Change in Channel Charge and Potential Distributions ($V_{DS} = 0V$)

$$g_d(y) = W\mu Q_c = g_d \tag{2.8}$$

The change in drain current due to a voltage disturbance at y_o is therefore also independent of position

$$\Delta i_d = -\delta V \frac{g_d(y_o)}{L}, \tag{2.9}$$

where $g_d(y_o)/L$ is the effective conductance seen by the noise voltage δV. The mean square change in drain current is $\overline{\Delta i_d^2}$, and the total drain current noise is the integral of the mean square changes over the channel length.

$$\overline{i_d^2} = \int_0^L \overline{\Delta i_d^2}\, dy \tag{2.10}$$

In the present case, $\overline{\Delta i_d^2}$ is independent of channel position. Therefore,

$$\overline{i_d^2} = 4kT\frac{g_d}{L^2}\Delta f \int_0^L dy = 4kT g_{do}\Delta f \tag{2.11}$$

where

$$g_{do} \equiv \left.\frac{dI_D}{dV_{DS}}\right|_{V_{DS}=0} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T) \tag{2.12}$$

With no drain to source voltage, the transistor is a simple conductance of g_{do} that has thermal noise.

The induced gate current is the time rate of change of charge on the gate, which is equal in magnitude to the time rate of change of channel charge.

$$i_g(t) = \frac{dq}{dt} \tag{2.13a}$$

$$i_g(\omega) = j\omega q \tag{2.13b}$$

As mentioned above, the nominal channel charge is constant when $V_{DS} = 0$. The bottom graph in Figure 2-4 shows the change in channel charge as a function of position

$$\Delta Q = Q_c(y) - Q_o \tag{2.14}$$

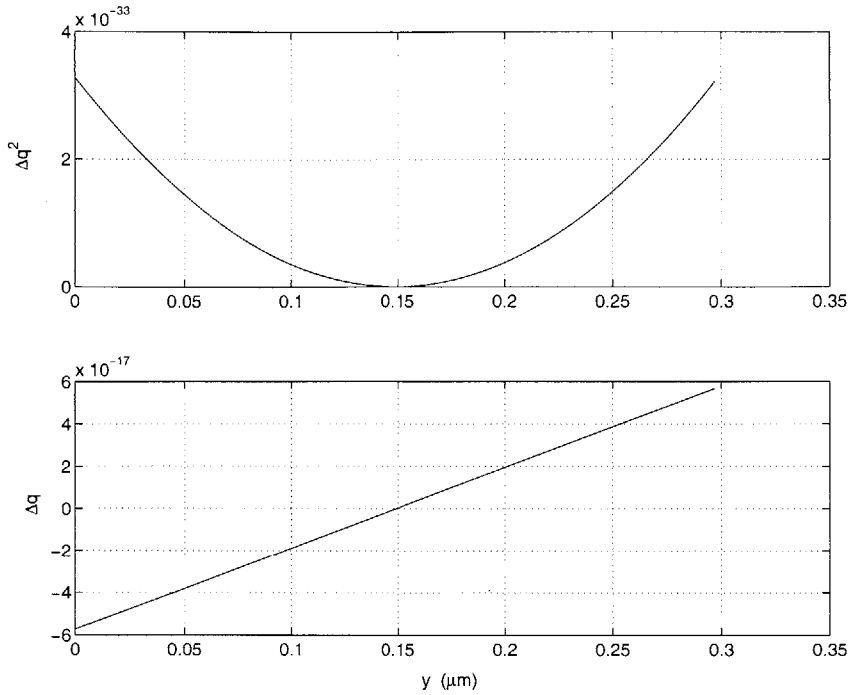

Figure 2-5: Net Change in Channel Charge versus y ($V_{DS} = 0V$)

for the same three noise voltages at y_{o1}, y_{o2}, and y_{o3}, but the net change in channel charge (Δq) is what determines the charge on the gate.

$$\Delta q = \int_0^L \Delta Q \, dy \tag{2.15}$$

Figure 2-5 shows both the net change in channel charge as a function of position(Δq) and the mean square net change in charge($\overline{\Delta q}$). The mean square induced gate charge is

$$\overline{q^2} = \int_0^L \overline{\Delta q^2} \, dy \tag{2.16}$$

or graphically, the area under the curve of $\overline{\Delta q^2}$ versus y. Because the gate current is the time rate of change of the gate charge, and a Fourier spectral analysis is being performed

$$\overline{i_g^2} = \omega^2 \overline{q^2} \tag{2.17}$$

It can be shown that[8] for $V_{DS} = 0$ and $I_D = 0$

$$\Delta q = WC_{ox}\left(y - \frac{L}{2}\right)\delta V \tag{2.18}$$

Substituting this expression back into Equations (2.16) and (2.17) results in

$$\overline{i_g^2} = 4kT\left(\frac{1}{12}\right)\left(\frac{\omega^2(WLC_{ox})^2}{g_{do}}\right)\Delta f \tag{2.19}$$

which according to[8] is consistent with the thermal noise generated from the real part of the gate admittance.

In order to determine the correlation between the gate and drain noise currents, the cross-correlation of Δq and Δi_d must be determined.

$$c_\Delta = \frac{\overline{\Delta q\,\Delta i_d}}{\sqrt{\overline{\Delta q^2}\cdot\overline{\Delta i_d^2}}} \tag{2.20}$$

Because both Δi_d and Δq are proportional to δV(Equations (2.9) and (2.18)), they are fully correlated ($|c_\Delta| = 1$). Returning to Figure 2-5, the change in channel charge is zero at $L/2$, and the change in charge is of equal magnitude but opposite signs for points located symmetrically about $L/2$. In reference to Figure 2-4,

$$\Delta q(y_{o1}) = -Q_1 \tag{2.21a}$$

$$\Delta q(y_{o2}) = 0 \tag{2.21b}$$

$$\Delta q(y_{o1}) = +Q_1 \tag{2.21c}$$

if $y_{o2} = L/2$. The change in drain current (Δi_d) is always the same sign. Therefore, as shown in Figure 2-6, the correlation between Δq and Δi_d is

$$c_\Delta = \begin{cases} +1 & y < L/2 \\ -1 & y > L/2 \end{cases} \tag{2.22}$$

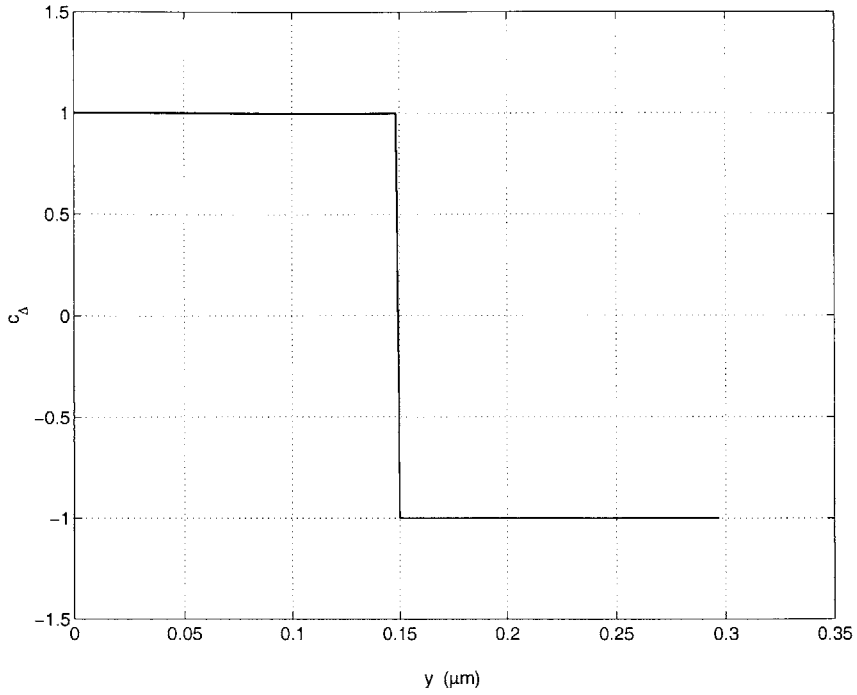

Figure 2-6: Correlation of Δi_d and Δq versus y ($V_{DS} = 0V$)

To calculate the correlation between q and i_d,

$$c = \frac{\overline{q\, i_d}}{\sqrt{\overline{q^2} \cdot \overline{i_d^2}}} \tag{2.23}$$

where

$$\overline{q\, i_d} = \int_0^L \overline{\Delta q \Delta i_d}\, dy \tag{2.24}$$

must be evaluated. Because Δi_d is constant, it is easy to see from Figure 2-5 that $\overline{q\, i_d} = 0$ for $V_{DS} = 0$. It then follows that the correlation between i_g and i_d is actually zero. This happens because the drain current fluctuations are independent of position and the magnitude of the net induced charge is symmetric about $L/2$ and opposite in sign. When these conditions change, the correlation will no longer be zero.

While the above discussion is useful in outlining the calculation of the noise generated in the device, field effect transistors are operated in the saturation region for

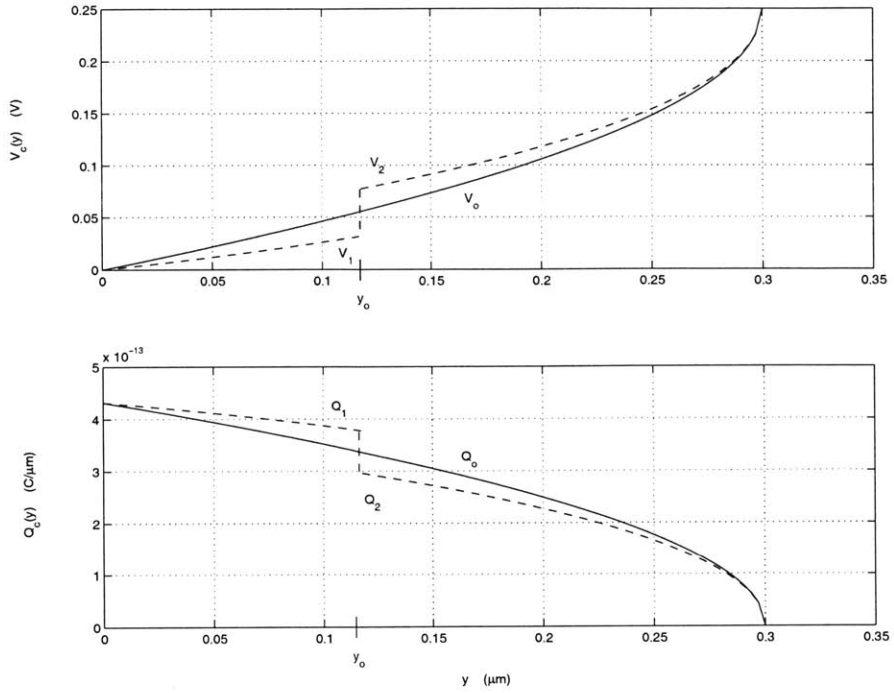

Figure 2-7: Channel Charge and Potential Distributions

amplifier applications. Therefore, the above analysis must be generalized to obtain results for the saturated condition.

The channel potential and charge at the edge of saturation are shown in Figure 2-7. The magnitude of the disturbance has been exaggerated to illustrate the shape of the potential. Figure 2-8 shows the changes only in channel potential and channel charge at the edge of saturation. Notice that the disturbances near the drain are no longer small and triangular in shape. This happens because the resistance of the channel increases dramatically near the pinch off point.

Figure 2-9 shows the mean square change in drain current versus y as V_{DS} is swept from 0 to V_{Dsat}. Again, the area under each curve is the mean square drain current noise at the associated value of V_{DS}. The flat line across the top of the graph is for $V_{DS} = 0$, and the area under the curves decreases following the arrow of increasing V_{DS} until at V_{Dsat} the drain current noise is that of $(2/3)g_{do}$.

Figure 2-10 shows the mean square net change in channel charge versus y as V_{DS}

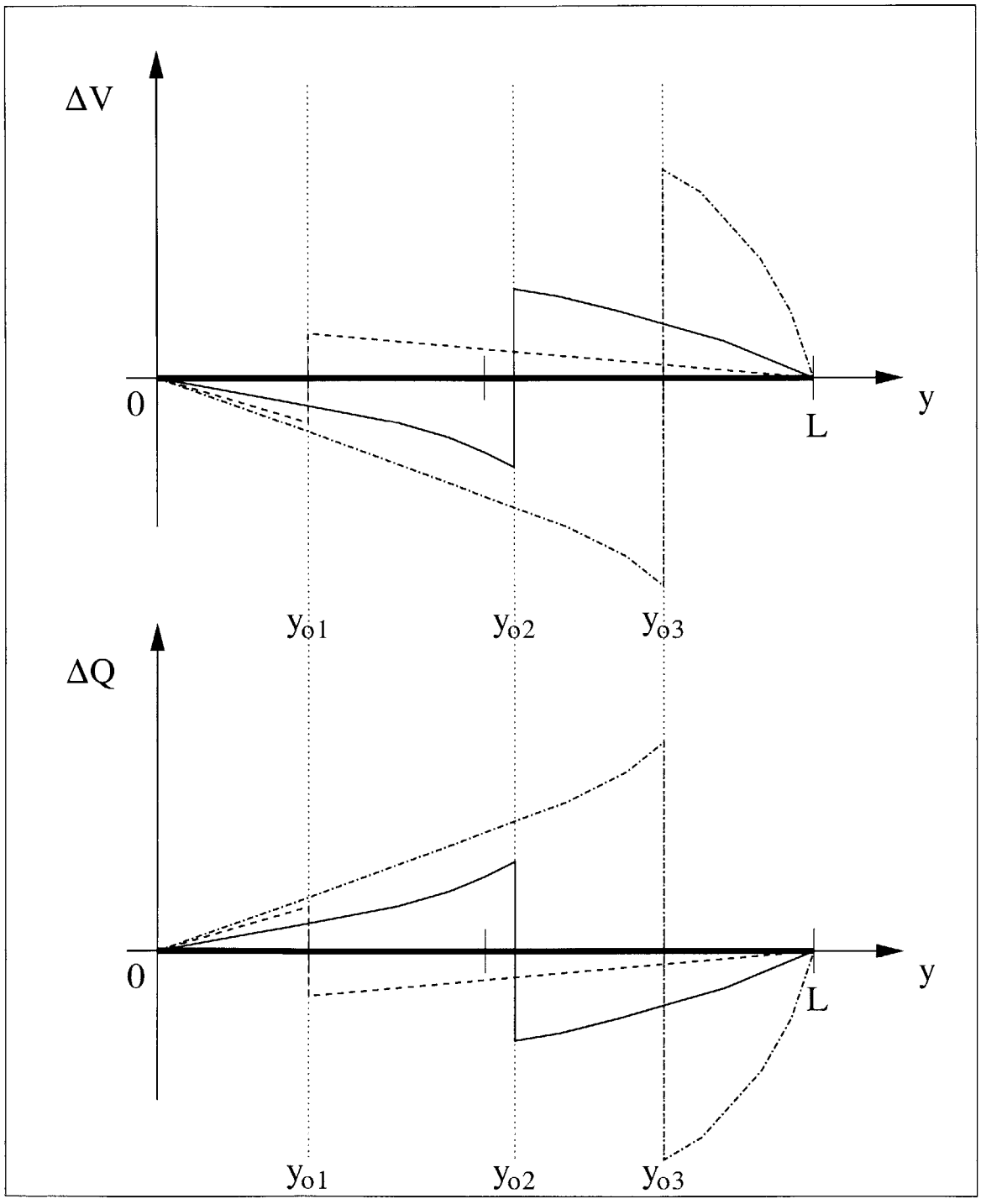

Figure 2-8: Change in Channel Charge and Potential Distributions ($V_{DS} = V_{Dsat}$)

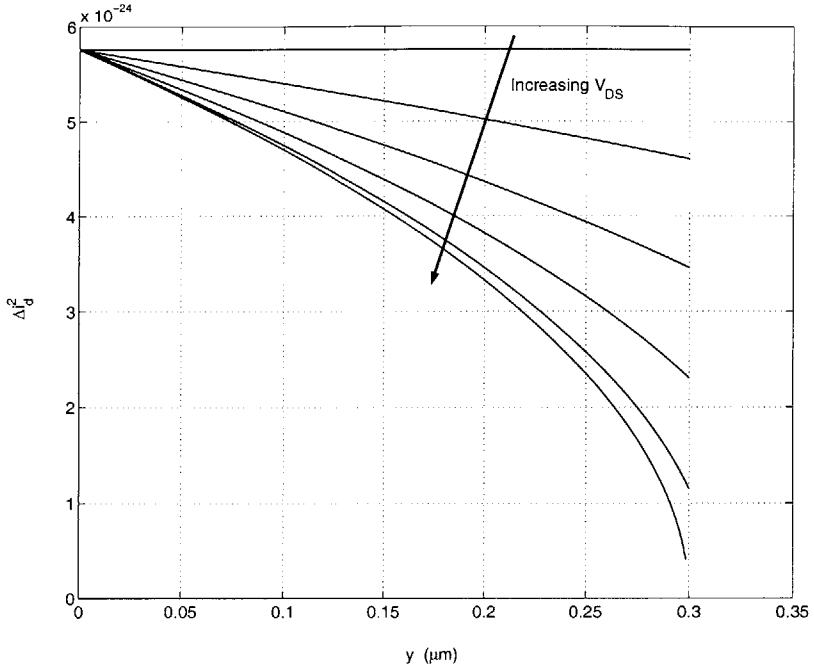

Figure 2-9: Mean Square Change in Drain Current versus y (V_{DS} sweep)

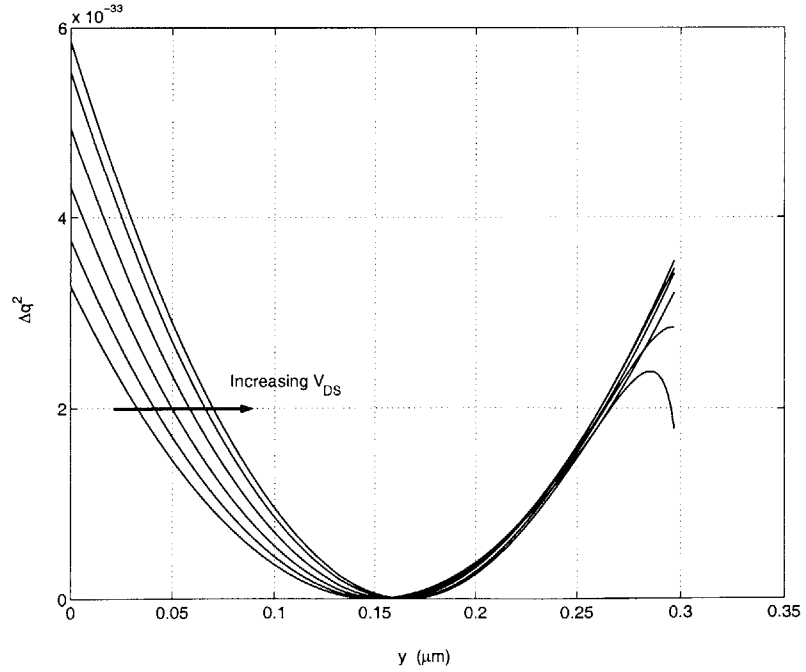

Figure 2-10: Mean Square Net Change in Channel Charge versus y (V_{DS} sweep)

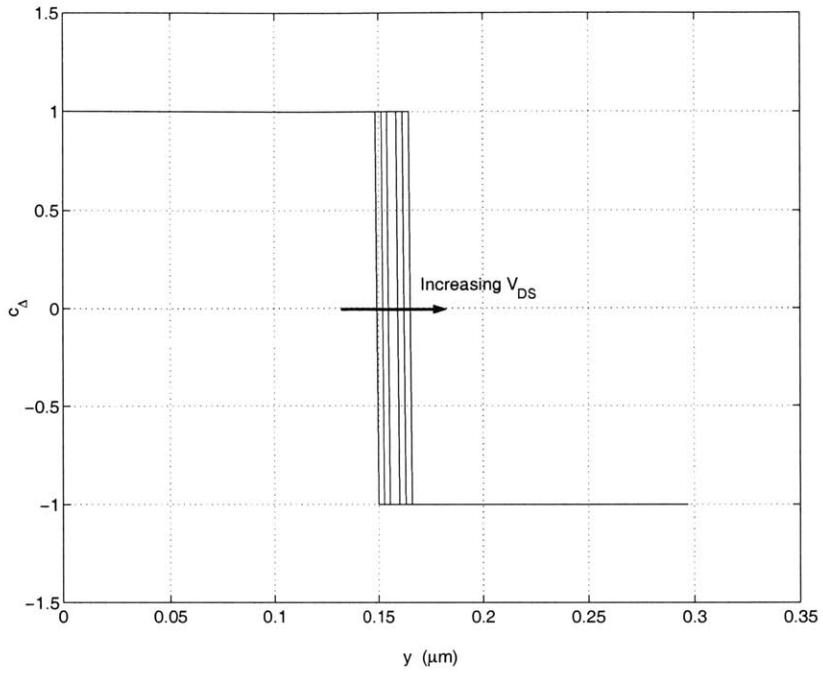

Figure 2-11: Correlation of Δi_d and Δq versus y (V_{DS} sweep)

is swept from 0 to V_{Dsat}. In this case, the area under the curve is proportional to the gate noise current. The area under the curve closer to the drain does not change much as V_{DS} increases, and the area under the curve on the source side only increases a little. As V_{DS} increases, the position in the channel where there is zero net change in charge($\Delta q = 0$) moves toward the drain. At saturation, the gate current noise corresponds to

$$\overline{i_g^2} = 4kT\left(\frac{4}{3}g_{gs}\right)\Delta f \tag{2.25}$$

where g_{gs} is the real part of the gate admittance at saturation.

$$g_{gs} = \frac{\omega^2 C_{gs}^2}{5g_{do}} \tag{2.26}$$

Figure 2-11 shows the correlation between the net change in channel charge and change in drain current for a disturbance at y_o as V_{DS} is swept from 0 to V_{Dsat}. Notice that as V_{DS} increases, the position in the channel where the correlation changes

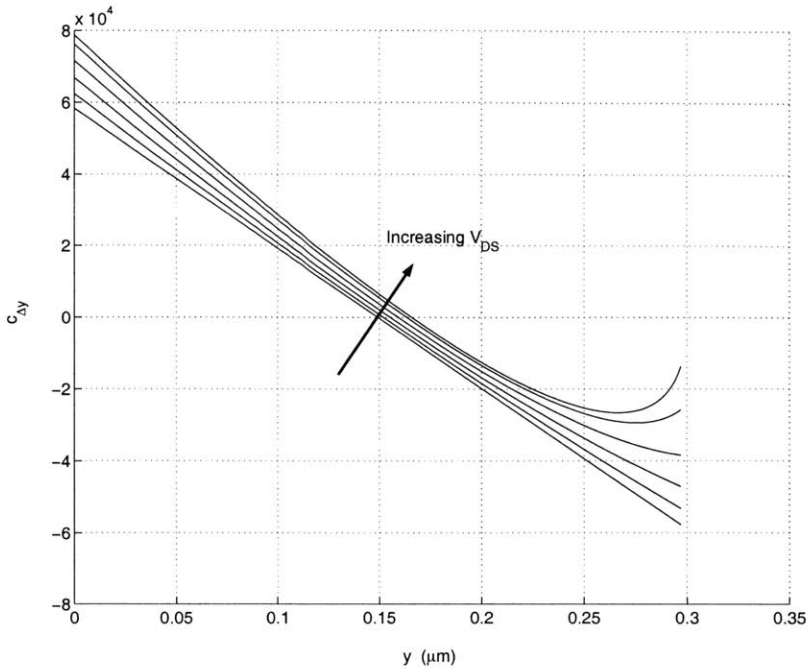

Figure 2-12: Correlation of Δi_d and Δq versus y (V_{DS} sweep)

sign moves toward the drain. Based on the relative movement of this position, it is reasonable that the correlation between i_g and i_d at saturation is greater than zero but still small.

$$c_{\Delta y} = \frac{\overline{\Delta q \, \Delta i_d}}{\sqrt{\overline{q^2} \cdot \overline{i_d^2}}} \tag{2.27}$$

This allows the visualization of the correlation as V_{DS} approaches V_{Dsat}. The area under the curve in Figure 2-12 is the correlation between q and i_d.

If all the integrations and modeling indicated above are followed through rigor-

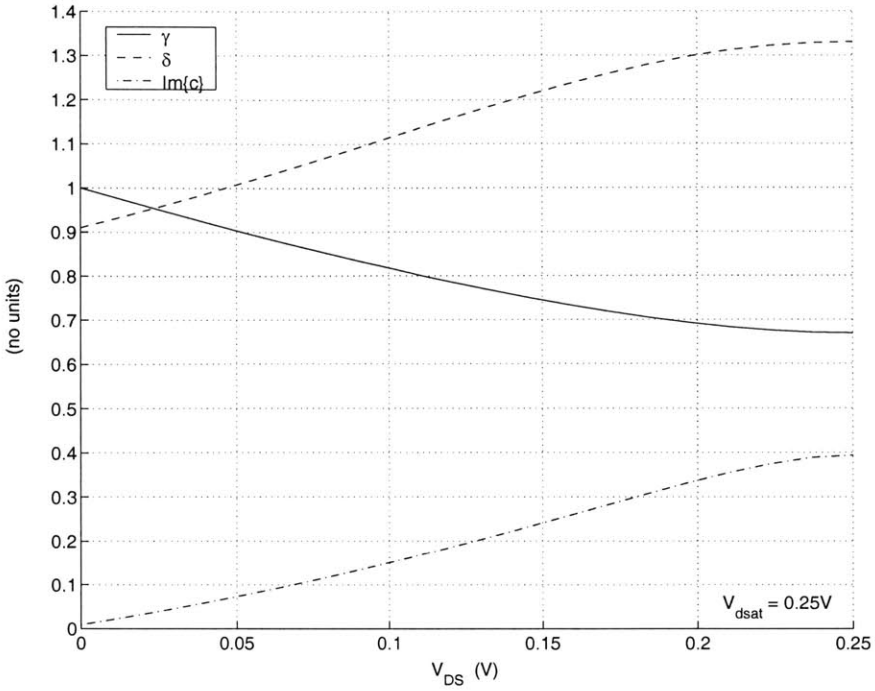

Figure 2-13: γ, δ, and c versus V_{DS}

ously, the results are

$$\overline{i_d^2} = 4kT\gamma g_{do}\,\Delta f \tag{2.28}$$

$$\overline{i_g^2} = 4kT\delta g_{gs}\,\Delta f \tag{2.29}$$

$$c = \frac{\overline{i_g \cdot i_d^*}}{\sqrt{\overline{i_g^2} \cdot \overline{i_d^2}}} \tag{2.30}$$

where in saturation

$$c = j0.395$$

$$\delta = 4/3$$

$$g_{gs} = \frac{\omega^2 C_{gs}^2}{5g_{do}}$$

and

$$\gamma = 2/3$$

$$g_{do} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0}$$

Figure 2-13 is a plot of the constants γ, δ, and c versus V_{DS}.

2.2 Short Channel Theory

In short channel length transistors, a significant portion of the channel is velocity saturated. This effects the way the noise in the channel is modeled. The model presented here is based on the description from Pucel et. al. [2] with the additional assumption that the channel is completely velocity saturated. A more general and complete way to analyze the problem is to divide the channel into two regions, one where the gradual channel approximation holds and the other velocity saturated. Because the goal here is to present a simple physical picture to motivate the proposed theory, the limit of 100% velocity saturation is considered. Therefore, the results obtained are a limiting case, and the actual performance should be between this solution and the long channel theory.

With the channel velocity saturated, the picture of the noise mechanism is much different from the long channel conductance noise theory. The more general theory of diffusion noise must be used.

$$\overline{i_n^2} = \frac{4\,q^2 D n A\,\Delta f}{\Delta x} \tag{2.31}$$

where D is the diffusion constant, n is the carrier density, A is the cross-sectional area. Diffusion noise simplifies to Johnson noise if the Einstein relation[3] holds, but it applies even if the diffusion coefficient is a function of the electric field. A simplified

[3] $D/\mu = kT/q$

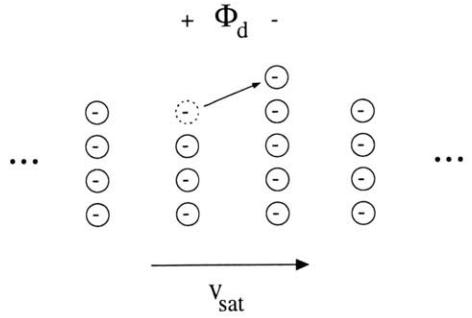

Figure 2-14: Velocity Saturation Noise Model

picture of the channel in velocity saturation is given in Figure 2-14. In saturation, the current is proportional to the charge in the channel.

$$I_D = WQ_I v_{sat} \tag{2.32}$$

Therefore, for a constant drain current, the charge in each differential section Δx of the channel must be constant. This is represented in the figure as a continuous sequence of four charges moving along the channel at velocity v_{sat}. Each carrier still has a roughly spherical velocity distribution around its nominal point. The dotted carrier moving to the group of charges in front of it (solid carrier) represents a random change in carrier velocity. This creates a dipole of charge in the channel with a potential distribution $\Phi_d(x)$. It can be shown[1] that this process results in a mean square drain noise voltage. The sum of the noise voltages from each Δx along the channel gives the open circuit mean square drain voltage. The short circuit mean square drain current noise is calculated using Ohm's law and the output conductance $g_{ds} = 1/r_o$.

The gate noise current is still the result of charge fluctuations in the channel. The generation of dipoles is a charge neutral process that does not directly induce charge on the gate. However, the dipole generation does cause an increase in the drain current, and therefore a compensating increase in channel charge. This increase in channel charge couples to the gate just as in the long channel case. The difference

in this case is that because the whole channel "breaths," the gate current noise is fully correlated with the drain current noise($c = 1$). Since the entire channel is not expected to be in velocity saturation, the value of c should be between one and the long channel value ($0.395 \leq c < 1$).

Recently, more work has been done on the modification of the drain current noise for short channel MOSFETs than on the analysis of both the gate and drain noise currents. Analysis of the short channel drain noise current in Wang et. al.[10], Knoblinger et. al.[11], and Triantis et. al.[12] use the more general form for the drain current

$$I_D = WQ_c(y)v(y), \tag{2.33}$$

and incorporate mobility degradation and velocity saturation. Wang et. al. uses the following model[13]

$$v(y) = \begin{cases} \dfrac{\mu_{\text{eff}} E(y)}{1 + \dfrac{E(y)}{E_c}} & E(y) < E_c \\ v_{sat} & E(y) \geq E_c \end{cases} \tag{2.34}$$

where

$$E_c = \frac{2v_{sat}}{\mu_{\text{eff}}} \tag{2.35}$$

The models in Knoblinger et. al.[11] and Triantis et. al.[12] also include an increased effective temperature to account for excess thermal noise due to hot carrier effects.

$$T_e = T_o \left[1 + \delta \left(\frac{E(y)}{E_c} \right)^2 \right] \tag{2.36}$$

where delta is a fitting parameter. The drain current noise can then be expressed as[14],[15],[16]

$$\overline{i_d^2} = 4kT_e \frac{\mu Q_N}{L^2} \Delta f \tag{2.37}$$

where

$$Q_N = \int_0^L WQ_c(y)\, dy \tag{2.38}$$

is the total inversion layer charge.

Analysis of both the gate and drain noise currents is essential for a complete picture of MOSFET noise behavior and low noise design. One study by Triantis et. al.[17], revisits the analysis of Pucel et. al.[2], and derives the results using MOSFET device equations. Another approach taken by Goo et. al.[18],[19] is to perform an impedance field simulation, where the impedance field is determined using a two-dimensional dc device simulator.[4] They compare the results of using both a drift-diffusion and hydrodynamic carrier transport model. Their results show that the hydrodynamic model predicts an increase in the gate and drain noise currents at shorter channel lengths, and the drift-diffusion model does not. Both models predict an increase in their correlation.

The best way to test the validity of these theories is to measure the drain noise current, the gate noise current, and their correlation for progressively shorter channel lengths. Recently, Knoblinger[20] reported measured results of the drain noise, gate noise, and correlation for 0.18 μm NMOS transistors. His results show increased drain noise current over the long channel value, and a substantially larger amount of gate noise current (30x). The correlation reported is about $j0.55$ which is also larger than the long channel value.

[4]MEDICI

Chapter 3

Measurements

3.1 Test structures

In order to measure the high frequency performance of transistors on chip, special coplanar waveguide probes and probing structures must be used. A rough sketch of the probing structure used for the test chip is given in Figure 3-1. This structure allows the use of both ground-signal-ground(GSG) and ground-signal(GS) probes from Cascade in a minimum chip area.[1] The thick rectangle that surrounds the probe pads is an n^+-diffusion ground plane. This structure minimizes the substrate losses at the expense of increased pad capacitance. Short and open structures are constructed using these probe pads which can be used to remove the effects of the pads.

A summary of the transistor structures included on the TI 0.15 μm test run are given in Table 3.1 and a die photograph[2] in Figure 3-2. Devices with an (N) are NMOS devices and those with a (P) are PMOS devices. The format of the entries is (Number of Fingers) x Width/Length, where width and length are given in microns(μm). For example, 20 x 10/0.15 is a device made of 20 transistors of width to length ratio of 10/0.15, which together make a $W/L = 200/0.15$ device. Cell-1

[1] Layout suggestion from Kamal Behaissa at TI

[2] Courtesy of Andrew Chen

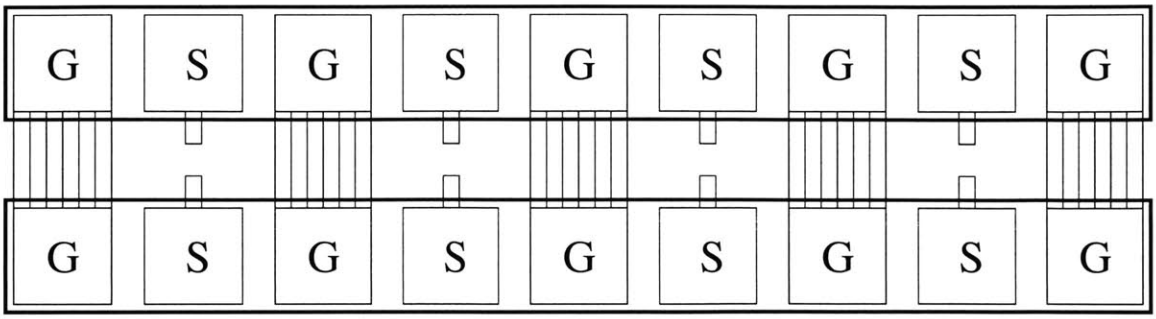

Figure 3-1: RF Probe Pad Structure

is a set of reference structures. It contains open, short and thru standards plus a long gate length device (200/1.0). Cell-2 is a set of three NMOS transistors of width 200 μm and three different gate lengths. The fourth device is a PMOS device with a 200 μm width and a 0.15 μm length. Cell-3 is same as Cell-2 except the device widths are 98 μm.

Only two widths were chosen because to the first order, noise performance is independent of device width. This is true if the effects of extrinsic parasitics as a function of width are negligible. Three different lengths were chosen because noise performance scales with the f_T of the device and therefore scales with length.

3.2 S–Parameters

S-parameters are used to characterize the devices at high frequencies. This is done because it is difficult if not impossible to have perfect open and short standards to measure either the Y or Z parameters directly. Another problem is the tendency of amplifiers to oscillate with their input or output terminals shorted at high frequencies because a physical short circuit presents a finite inductance and resistance at the input or output terminal.

S-parameters are defined with reference to a characteristic impedance Z_o usually the characteristic impedance of the transmission line attached to the ports of the

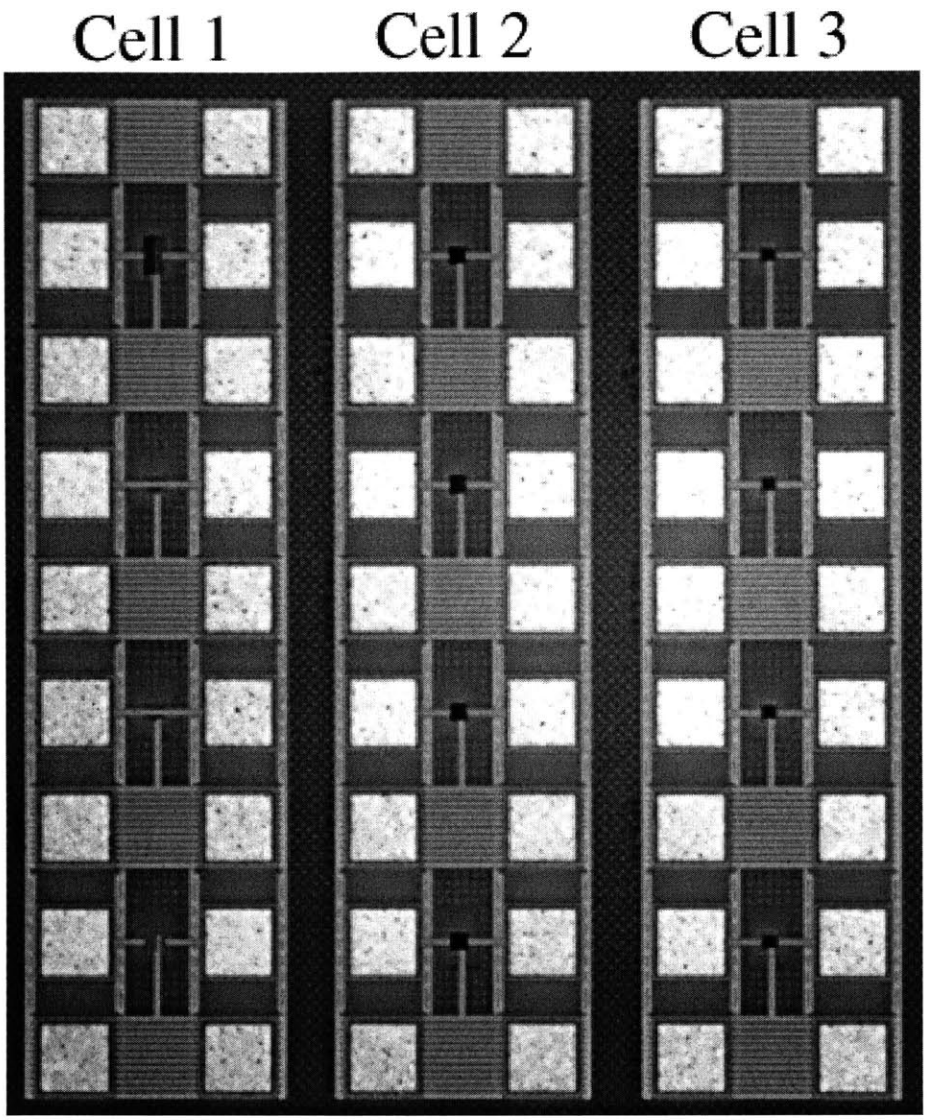

Figure 3-2: Die Photograph of RF Structures

	Cell-1	Cell-2	Cell-3
Device-1	Open	(N) 20 x 10/0.15	(N) 14 x 7.0/0.15
Device-2	Short	(N) 20 x 10/0.20	(N) 14 x 7.0/0.20
Device-3	Thru	(N) 20 x 10/0.275	(N) 14 x 7.0/0.275
Device-4	(N) 20 x 10/1.0	(P) 20 x 10/0.15	(P) 14 x 7.0/0.15

Table 3.1: Table of Device Geometries

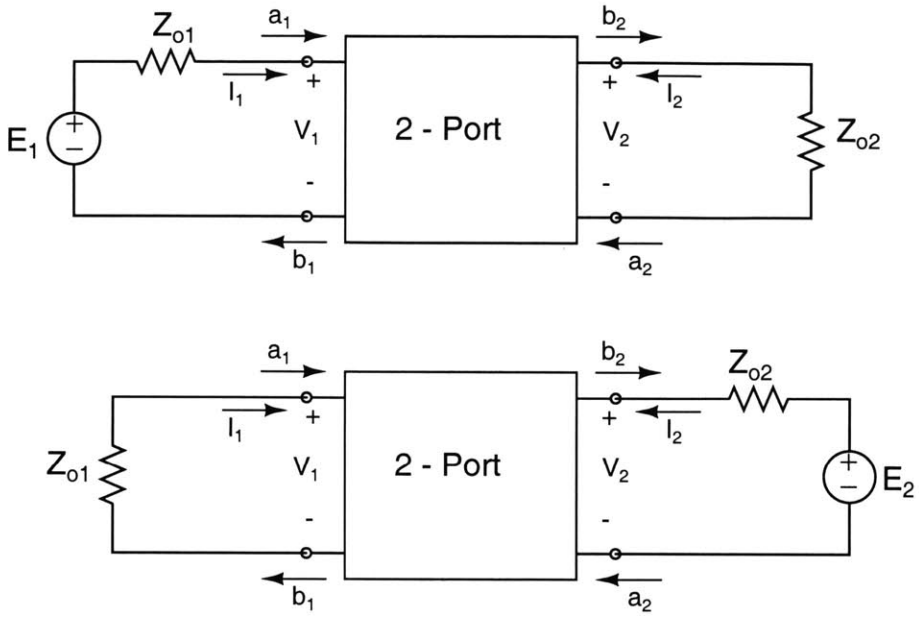

Figure 3-3: S-parameter Test Circuit

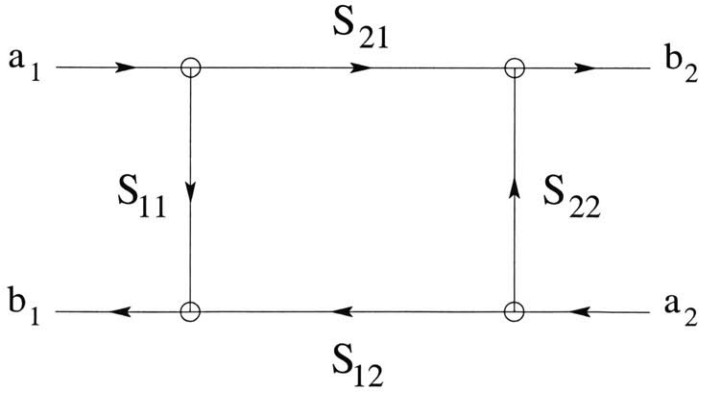

Figure 3-4: S-parameters Signal Flow Graph

device.[3] Instead of using the input and output voltage and current to define the port signals, the quantities

$$a_1 = \frac{V_1^+}{\sqrt{Z_{o1}}} = \frac{1}{2\sqrt{Z_{o1}}}(V_1 + Z_{o1}I_1) \tag{3.1}$$

$$b_1 = \frac{V_1^-}{\sqrt{Z_{o1}}} = \frac{1}{2\sqrt{Z_{o1}}}(V_1 - Z_{o1}I_1) \tag{3.2}$$

$$a_2 = \frac{V_2^+}{\sqrt{Z_{o2}}} = \frac{1}{2\sqrt{Z_{o2}}}(V_2 + Z_{o2}I_2) \tag{3.3}$$

$$b_2 = \frac{V_2^-}{\sqrt{Z_{o2}}} = \frac{1}{2\sqrt{Z_{o2}}}(V_2 - Z_{o2}I_2) \tag{3.4}$$

are used. The quantity a_i represents the square-root of the incident power at port i, and the quantity b_i represents the square-root of the reflected power at port i (Figure 3-3). The S-parameters are then defined as

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{Z_{T1} - Z_{o1}}{Z_{T1} + Z_{o1}} \tag{3.5}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \sqrt{\frac{Z_{o2}}{Z_{o1}}}\frac{V_1}{E_2/2} \tag{3.6}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \sqrt{\frac{Z_{o1}}{Z_{o2}}}\frac{V_2}{E_1/2} \tag{3.7}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = \frac{Z_{T2} - Z_{o2}}{Z_{T2} + Z_{o2}} \tag{3.8}$$

where Z_{T1} and Z_{T2} are in input and output impedances with the output or input ports terminated in Z_{o2} or Z_{o1} respectively. In general, the S-parameters should be thought of as the square root of power ratios, and they may be expressed as functions of the terminal voltages and currents. Figure 3-3 shows the two-port test circuits to determine the S-parameters, and Figure 3-4 is a signal flow graph representation of

[3] The ubiquitous 50 Ω.

the S-parameters that is useful in the analysis of interconnected S-parameter blocks. For an excellent and more detailed description of S-parameters, their uses, and how to convert them to and from other two-port representations see Gonzalez[21].

3.3 Noise Parameters

The IRE, predecessor of the IEEE, published a formal definition for noise figure in 1952[22] and the following reworded definition in 1957[23],[24]. Noise Factor (Noise Figure) of a Two-Port Transducer at a specified input frequency (is) the ratio of

1. the total noise power per unit bandwidth at a corresponding output frequency available at the output port, to

2. that portion of 1. engendered at the input frequency by the input termination at the Standard Noise Temperature (290 K).

Standards for noise measurements of linear two-ports were defined in 1959[25], [26]. The noise of any two-port device can be represented using the devices two-port parameters and two correlated external noise generators (Figure 3-5). One common approach is to use the $ABCD$ chain matrix representation because it refers all the device noise sources to the input. This is the familiar input referred noise and noiseless device model. The benefit of this representation is that the input signal and noise levels are easily compared.

An equivalent representation of the device noise performance is possible using Noise Factor.[4]

$$F = F_{min} + \frac{R_n}{\mathfrak{Re}\{Y_s\}}|Y_s - Y_{opt}|^2 \tag{3.9}$$

[4]I have adopted the somewhat standard convention of calling F (ratio) Noise Factor and NF (dB) Noise Figure.

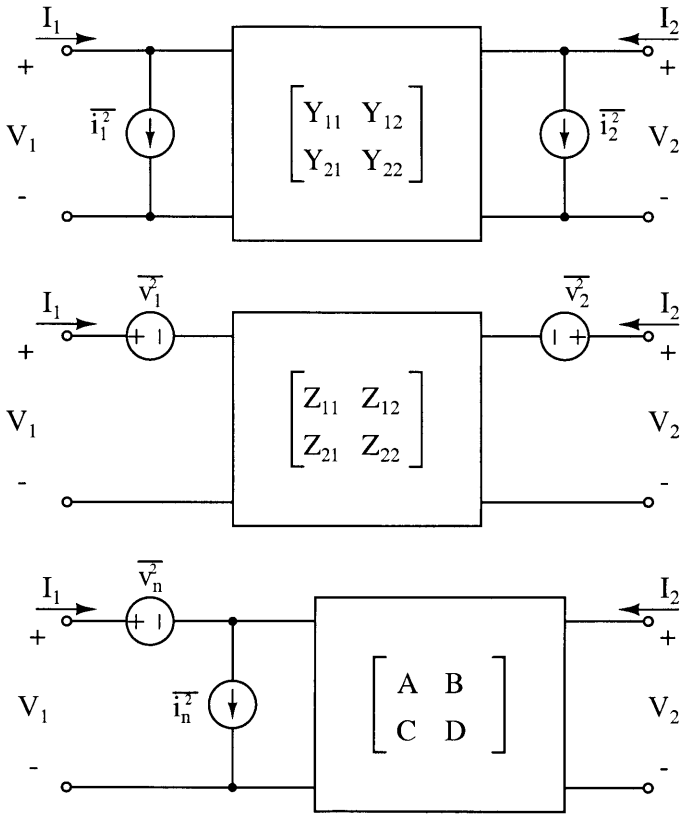

Figure 3-5: Two-Port Noise Circuits

where the four noise parameters are F_{min}, R_n, $G_{opt} = \mathfrak{Re}\{Y_{opt}\}$, and $B_{opt} = \mathfrak{Im}\{Y_{opt}\}$. In terms of the chain matrix representation

$$F_{min} = 1 + 2\left(\frac{\overline{v_n\, i_n^*} + \overline{v_n^2}\, Y_{opt}^*}{4kT\Delta f}\right) \tag{3.10a}$$

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f} \tag{3.10b}$$

$$G_{opt} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}} - (B_{opt})^2} \tag{3.10c}$$

$$B_{opt} = -B_c \tag{3.10d}$$

where

$$Y_c = \frac{\overline{v_n^*\, i_n}}{\overline{v_n^2}} = G_c + jB_c \tag{3.11}$$

Sometimes at lower frequencies, the correlation between v_n and i_n is somewhat cavalierly ignored ($\overline{v_n\, i_n^*} = 0$), under the assumption that i_n is negligibly small. This leads to the familiar expressions

$$F_{min} = 1 + 2\sqrt{\left(\frac{\overline{v_n^2}}{4kT\Delta f}\right)\left(\frac{\overline{i_n^2}}{4kT\Delta f}\right)} = 1 + 2\sqrt{R_n G_u} \tag{3.12a}$$

$$G_{opt} = \sqrt{\frac{\overline{i_n^2}}{\overline{v_n^2}}} = \sqrt{\frac{G_u}{R_n}} \tag{3.12b}$$

$$B_{opt} = 0 \tag{3.12c}$$

where G_u is the equivalent noise conductance at the input that is uncorrelated with v_n. However, the assumption that v_n and i_n are uncorrelated is never true. For

example, the input referred noise sources for an intrinsic MOSFET are

$$v_n = -\frac{i_d}{g_m} \tag{3.13}$$

$$i_n = -\frac{j\omega C_{gs}}{g_m} i_d + i_g \tag{3.14}$$

Clearly, the correlation between v_n and i_n is not zero, even if induced gate noise is ignored. However, if the correlation between i_d and i_g is ignored,[5] Y_{opt} can be shown to be approximately

$$Y_{opt} \approx \omega C_{gs} \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}} - j\omega C_{gs} \tag{3.15}$$

At lower frequencies, only G_{opt} is of practical concern because amplifiers are usually designed for broad–band gain, and the inductor required to implement B_{opt} for a narrow–band amplifier would be too large.[6] A very large source resistance is needed to achieve the optimum noise match because G_{opt} very small at lower frequencies. This means that v_n dominates the noise performance of the amplifier, which is consistent with conventional analog design methods.

The general expressions that are true at all frequencies are obtained by rewriting the intrinsic MOSFET noise model from Chapter 2 in the chain matrix representation and substituting the result into the expressions for the four noise parameters(Equations (3.10)). Contrary to the common custom of ignoring the polarity of the noise generators, the direction of the noise generators does matter when consid-

[5]Admittedly, this is a questionable assumption in general, but it does not alter the conclusion of this example.

[6]For $f = 1\,\text{MHz}$, $C_{gs} = 250\,\text{fF}$, $Z_{opt} = 1/Y_{opt}$ is approximately the series combination of $290\,\text{k}\Omega$ and 70 mH. If the gate and drain noise correlation is included, these values increase to $410\,\text{k}\Omega$ and 80 mH.

ering the correlation between noise sources.

$$F_{min} = 1 + 2R_n \left(G_{opt} + G_c\right) \tag{3.16}$$

$$G_c = \mathfrak{Re}\left\{ Y_{11} \left(1 - c\frac{Y_{21}}{Y_{11}} \sqrt{\frac{\overline{i_g^2}}{\overline{i_d^2}}} \right) \right\} \tag{3.17}$$

$$R_n = \frac{\gamma g_{do}}{|Y_{21}|^2} \tag{3.18}$$

$$G_{opt} = \sqrt{\frac{\overline{i_g^2}\left(1 - |c|^2\right)}{\overline{i_d^2}/|Y_{21}|^2} + G_c^2} \tag{3.19}$$

$$B_{opt} = -\mathfrak{Im}\left\{ Y_{11} \left(1 - c\frac{Y_{21}}{Y_{11}} \sqrt{\frac{\overline{i_g^2}}{\overline{i_d^2}}} \right) \right\} \tag{3.20}$$

which in the long channel case simplify to

$$F_{min} \approx 1 + 2\frac{\omega}{\omega_T}\sqrt{\frac{\gamma\delta}{5}\left(1 - |c|^2\right)} \approx 1 + \frac{4}{5}\left(\frac{\omega}{\omega_T}\right) \tag{3.21}$$

$$G_c \approx \mathfrak{Re}\left\{Y_{11}\right\} \approx 0 \tag{3.22}$$

$$R_n \approx \frac{\gamma g_{do}}{g_m^2} = \frac{2}{3g_m} \tag{3.23}$$

$$G_{opt} \approx \omega C_{gs}\left(\frac{g_m}{g_{do}}\right)\sqrt{\frac{\delta}{5\gamma}\left(1 - |c|^2\right)} \approx \frac{3}{5}\,\omega C_{gs} \tag{3.24}$$

$$B_{opt} \approx -\omega C_{gs}\left(1 - c\frac{g_m}{g_{do}}\sqrt{\frac{\delta}{5\gamma}}\right) \approx -\frac{3}{4}\,\omega C_{gs} \tag{3.25}$$

Interestingly, the Q of Y_{opt} is equal to

$$Q_{opt} = \frac{|B_{opt}|}{G_{opt}} \approx 1.3 \tag{3.26}$$

independent of frequency, device size, and operating point. Therefore, measured data for Y_{opt} traces out an arc of constant Q on the Smith Chart as a function of increasing

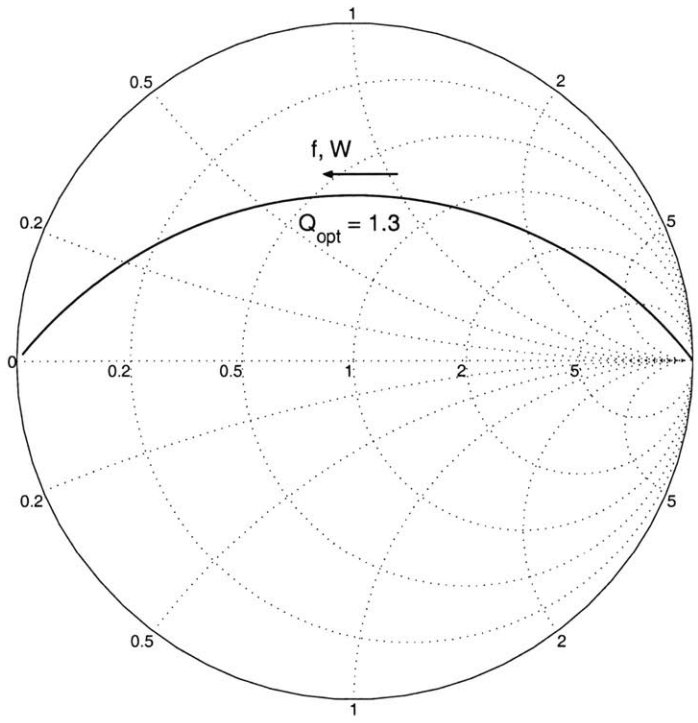

Figure 3-6: Ideal Y_{opt} versus f and W

device width and measurement frequency (Figure 3-6).

3.4 Noise Parameter Measurement Methods

The traditional method of measuring the four noise parameters is to use a source admittance tuner to present the device with a minimum of four different source admittances, and the resulting overdetermined system of equations is solved using least squares fitting. The paper by Pucel et. al.[27] gives a comprehensive explanation of this technique. This method has also been the basis for the development of automated noise measurements systems (eg. ATN Noise Measurement System). One drawback of this technique is the amount of separate measurements that are required and the number of post-processing steps, both of which increase the uncertainty of the final results.

Unfortunately, tuner based methods even when fully automated are time consuming. The procedure described above must be done for each frequency of interest. This has led people to look for more rapid ways of determining the noise parameters. One approach popular with MESFETs is the hybrid representation proposed by Pospieszalski[28]. He suggests that a FET can be modeled with an output current noise source and an input noise voltage which are uncorrelated. This means that the problem of finding the four noise parameters simplifies to finding only two frequency independent constants T_g and T_d. Unfortunately, the assumption that the input noise voltage $\overline{v_{gs}^2}$ and the output noise current $\overline{i_o^2}$ are uncorrelated is not valid for MOSFETs[29].

Another approach that does not require a source tuner was proposed by Dambrine et. al.([30],[31]) that utilizes the fact that the $50\,\Omega$ noise factor (F_{50}) is proportional to ω^2. This method uses only measured F_{50} versus frequency data and device Y-parameters. Unfortunately, losses in the on-wafer probe pads are neglected, which is a significant limitation for this technique especially when making measurements on silicon wafers.

At lower frequencies, direct measurement of the noise power can be done. Unfortunately, at lower frequencies, the measurement of $\overline{i_g^2}$ is very difficult because its magnitude is small. This eliminates this approach for complete noise characterization. It is possible to measure the drain current noise with this technique, making this technique useful as a check that the drain current noise extracted using noise figure measurements is correct. For a MOSFET, ignoring parasitics, the output noise measured with the gate short circuited is the drain current noise $\overline{i_d^2}$. To find the input referred equivalent noise resistance, van der Ziel[32] suggests making two measurements (Figure 3-7).

$$M_1 = \overline{i_o^2} = g_m^2 \cdot 4kT\,R_n\,\Delta f \tag{3.27}$$

$$M_2 = \overline{i_o^2} = g_m^2 \cdot 4kT\,(R_n + R)\,\Delta f \tag{3.28}$$

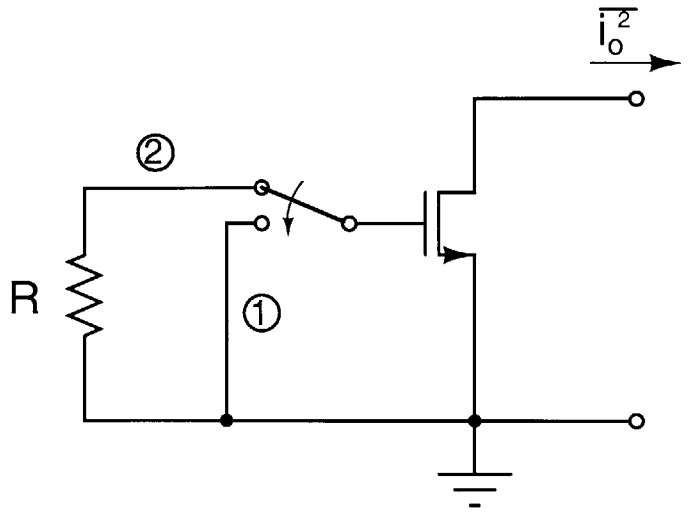

Figure 3-7: R_n Measurement Circuit

The noise resistance is then

$$R_n = \left(\frac{M_1}{M_2 - M_1}\right) R \tag{3.29}$$

where R should be on the same order as R_n. The effects of the parasitic resistances can be removed and what remains is the drain current noise.

The source tuner approach was adopted for this thesis because it requires very few assumptions to be made about the device that is being measured, and it allows for the complete characterization of the devices noise sources. The procedure used in the data acquisition and analysis is outlined in the following section.

3.5 Measurement and Post-processing

3.5.1 S-parameters

The test and measurement software IC-Cap is used to perform semi-automated measurements of the device. The gate–to–source and drain–to source voltages are controlled with an HP4145A Semiconductor Parameter Analyzer. Cascade Microtech

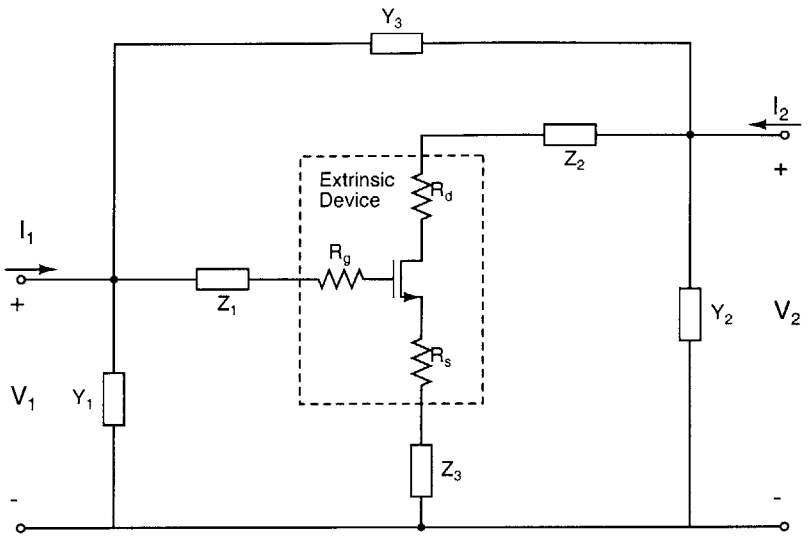

Figure 3-8: Pad/Package De-embedding Circuit

coplanar probes are used to make the on–wafer measurements, and the S–parameters are measured as a function of frequency (0.2–6 GHz) with the HP8753C Vector Network Analyzer(VNA) and 85047A Test Set. The reference planes for the S–Parameter measurements are defined using a short-open-load-thru(SOLT[7]) two–port calibration and an impedance standard substrate. Therefore, the measured S–parameters represent the two–port parameters of the transistor and the probe pad structure. To obtain the two–port parameters of the transistor only, the measured data must be de-embedded with a two step procedure[33]. The series and shunt components of the pads are subtracted from the measured data using the measurements from the on-wafer Open and Short structures(Figure 3-8).

Conversions between the S–parameters and any other set of two–port parameters(Y, Z, H, ABCD) can be found in any standard microwave design text[21]. From the measurement of the on-wafer open, the shunt admittances(Y_1, Y_2, Y_3) can be determined. The Y–Parameters of the total structure minus the shunt admittances

[7]Sometimes also referred to as LOST.

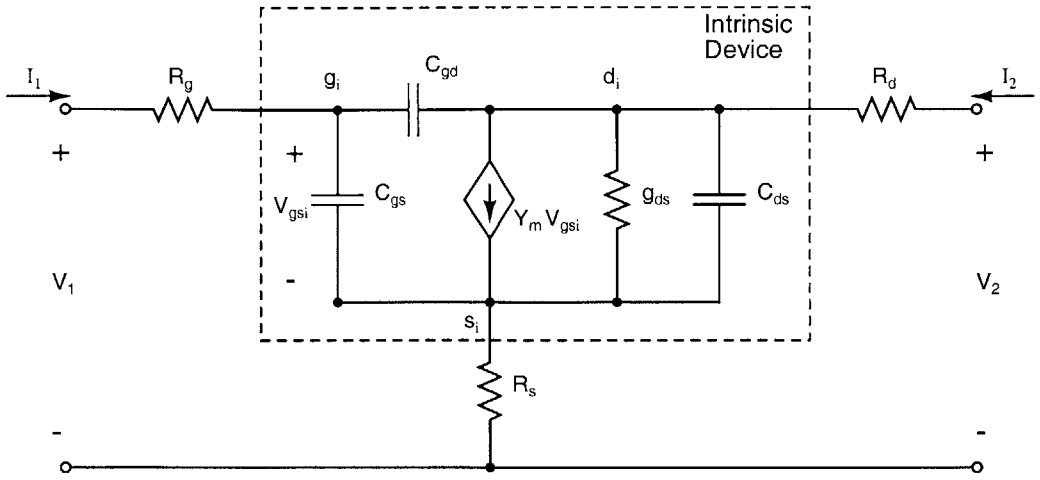

Figure 3-9: MOSFET Small Signal Model

is

$$\mathbf{Y_x} = \mathbf{Y_{pd}} - \mathbf{Y_{open}} \tag{3.30}$$

The series impedances (Z_1, Z_2, Z_3) are obtained from the measurements of the on-wafer short. First, the open parasitics must be removed from the short-circuited pad data

$$\mathbf{Y_y} = \mathbf{Y_{short}} - \mathbf{Y_{open}} \tag{3.31}$$

and then the series impedances are removed

$$\mathbf{Z_{ext}} = \mathbf{Z_x} - \mathbf{Z_y} \tag{3.32}$$

where $\mathbf{Z_x}$ is the Z-parameter version of $\mathbf{Y_x}$, and $\mathbf{Z_{ext}}$ are the Z-parameters of the extrinsic device under test.

From the two–port parameters of the extrinsic transistor as a function of frequency, a small–signal model for the MOSFET can be developed using the procedure outlined by Raskin et. al. [34]. The simplified circuit model is shown in Figure 3-9. One feature to note in this model is the drain–to–source capacitance. This element is not a physical parameter, but is used to model the effect of the output resistance falling off at higher

frequencies. The drain to bulk capacitance in series with the bulk resistance are the physical cause of the decreasing output impedance. If the frequency the device is measured at is low enough such that the drain–to–bulk impedance is much larger than the bulk resistance, the effect can be modeled as shown. This procedure allows the extraction of the series resistances and inductances of the transistor which are needed below to remove the thermal noise of the extrinsic resistances. However, caution should be used, and the results obtained with this technique should be compared with estimates from the layout.

Noting that the series parasitics($\mathbf{Z}_\sigma$) and the intrinsic device($\mathbf{Y_{int}}$) can be modeled as the addition of the Z-parameters[8] of the intrinsic device

$$\mathbf{Z_{ext}} = \mathbf{Y_{ext}}^{-1} = \mathbf{Z}_\sigma + \mathbf{Y_{int}}^{-1} \tag{3.33}$$

where $\mathbf{Y_{ext}}$ are the measured Y-parameters after pad de-embedding.

$$\mathbf{Z}_\sigma = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \tag{3.34}$$

$$\mathbf{Y_{int}} = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ Y_m - j\omega C_{gd} & g_{ds} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \tag{3.35}$$

Raskin et. al. then showed that by plotting the measured data parametrically, a linear regression could be used to extract the series elements. For the series resistances R_s, R_g, and R_d, the data sets $(\mathfrak{Re}\{Z_{12ext}\}, \mathfrak{Re}\{Z_{21ext}\})$, $(\mathfrak{Re}\{Z_{11ext}\}, \mathfrak{Re}\{Z_{21ext}\})$, and $(\mathfrak{Re}\{Z_{22ext}\}, \mathfrak{Re}\{Z_{12ext}\})$ are used respectively.

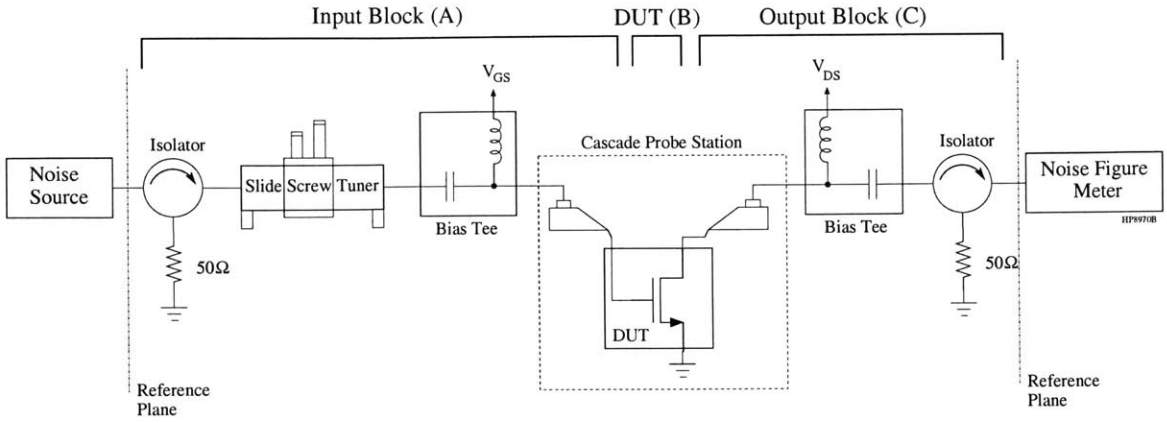

Figure 3-10: Noise Figure Measurement Setup

3.5.2 Noise

The measurement and de-embedding steps for the noise figure characterization method are itemized below. The measurement setup is given in Figure 3-10. The Agilent 8970B with the 8971C NF test set and a 346B 15 dB ENR noise source were used to make the measurements in an RF shielding chamber. The noise figure meter is calibrated at the reference planes shown by attaching the noise source directly to the noise figure meter. The device is part of a test wafer that is contacted using the Cascade probes mentioned above for the S-parameter measurements. Bias-Tees are used to supply the gate and drain voltages with an Agilent 4156C Semiconductor Parameter Analyzer. A Maury 8045P slide-screw tuner is used to determine the source admittance presented to the transistor. The isolators at the input and output of the measurement system ensure that the insertion gain of the system that is measured by the 8970 is the available gain that is used to calculate the corrected noise figure. These devices also minimize the uncertainty of the system noise figure measurements[35].

[8]The inverse operation noted here is not really a true matrix inverse, but the conversion of Y-parameters to Z-parameters or vice versa.

Noise Measurement Steps

1. **Measure S-parameters[9] of input isolator and tuner at various admittances.**

   This step is critical to the ability of the measurement system to determine the four noise parameters. The factors involved in selecting the number of source admittances, the magnitude of the reflection coefficient of the source admittance(Γ_S), and the general distribution of the admittances on the Smith Chart are discussed in a paper by Davidson et. al.[36]. To minimize the RMS error in the linear regression of the four noise parameters, the maximum source reflection coefficient should be maximized, no fewer than five source admittances should be used, and these admittances should be evenly distributed around the Smith Chart.

   Because an efficient method was required to obtain the admittance settings over a wide frequency range, the following method was adopted. First, the maximum reflection coefficient magnitude that the tuner could present over the desired frequency range was determined. Second, the minimum reflection coefficient magnitude was determined. Third, two additional reflection coefficient magnitudes were selected between the maximum and minimum values. Finally, a frequency in the band was selected, and five evenly spaced reflection coefficient angles where chosen. A sketch of the tuner coverage on the Smith Chart is given in Figure 3-11. This spacing produces sixteen well spaced source admittances at the frequency the angles were chosen. Unfortunately, the individual spokes of admittances do not all rotate at the same rate as a function of frequency. It is possible that at a different frequency some points overlap, and the effective number of points is reduced. Figure 3-12 illustrate this with plots of the source admittance locations for 2.5 GHz and 4.0 GHz.

2. **Measure S-parameters of bias-Tees/cables/probes.**

[9] All S-parameter data is linear interpolate in magnitude and phase as a function of frequency.

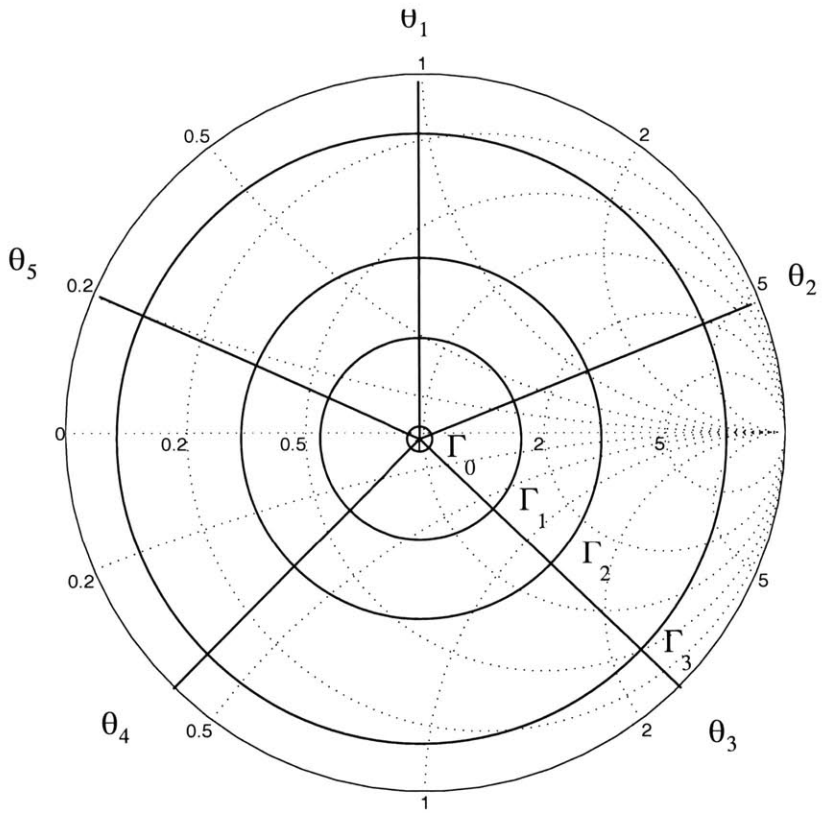

Figure 3-11: Example Tuner Coverage

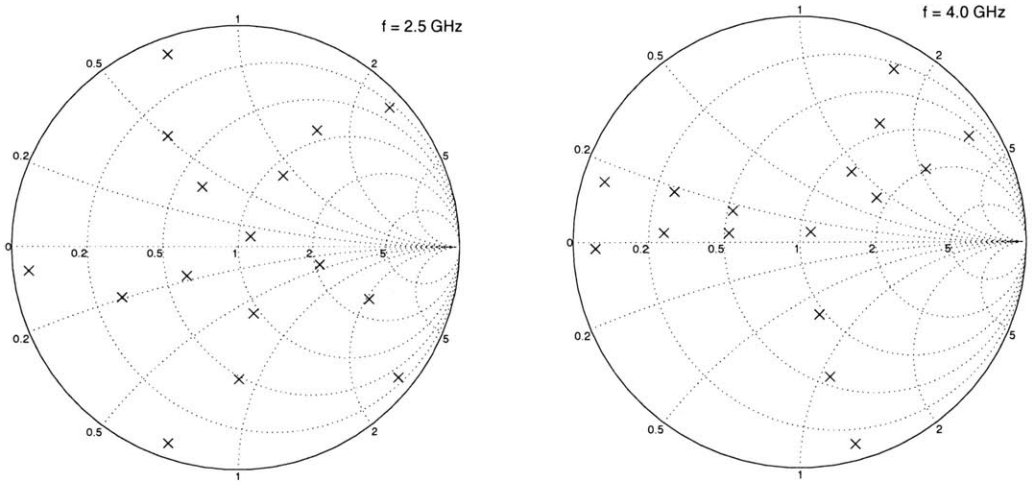

Figure 3-12: Source Admittance Points at 2.5 GHz and 4.0 GHz

In order to determine the source impedance actually seen looking toward the source from the probe tips, all the components from the tuner to the probe tip must be characterized with S-parameters. Also, any noise contribution of these components at the input and output of the on-wafer device must also be removed. Unfortunately, it is not possible to directly make a full two-port characterization of these blocks using the network analyzer because one port is a wafer probe and the other is a 3.5 mm connector. The S-parameters can be obtained using three separate measurements and the following procedure.

(a) Calibrate the network analyzer to a 3.5 mm connector reference plane.

(b) Connect the 3.5 mm input of the bias-Tees/cables/probe to the calibrated network analyzer port.

(c) Measure S_{11} for three known loads with the probes. A Cascade impedance standard substrate(ISS) 50 Ω load, short, and open probe tips were used.

Assuming that terminations are ideal and all the measured devices are passive and reciprocal($S_{12} = S_{21}$),[10] the following expressions can be derived using the signal flow graph in Figure 3-13.

$$S_{11} = \Gamma_{50} \tag{3.36a}$$

$$S_{21} = \sqrt{\frac{2(\Gamma_{short} - S_{11})(\Gamma_{open} - S_{11})}{\Gamma_{short} - \Gamma_{open}}} \tag{3.36b}$$

$$S_{12} = \sqrt{\frac{2(\Gamma_{short} - S_{11})(\Gamma_{open} - S_{11})}{\Gamma_{short} - \Gamma_{open}}} \tag{3.36c}$$

$$S_{22} = -\frac{S_{21}S_{12} + (\Gamma_{short} - S_{11})}{\Gamma_{short} - S_{11}} \tag{3.36d}$$

where Γ_{50}, Γ_{short}, and Γ_{open} are Γ_{in} for a 50 Ω load, a short, and an open, respectively.

[10] This excludes the isolators, but these can be measured separately.

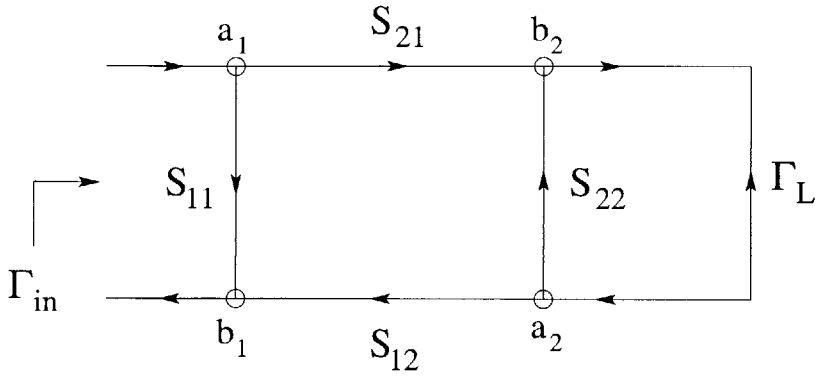

Figure 3-13: S-parameters from Short–Open–Load Measurements

3. **Measure the output isolator S-parameters using a standard two-port network analyzer measurement.**

4. **Mathematically cascade isolator/tuner and the output isolator with the bias-Tee/cables/probe S-parameters obtained above.**

   The expressions for the cascaded S-parameters can be quickly derived from the signal-flow graph in Figure 3-14 using Mason's Gain formula[21],[37],[38],[39],[40].

$$S_{11} = S_{11_m} + \frac{S_{21_m} S_{11_n} S_{12_m}}{1 - S_{22_m} S_{11_n}} \tag{3.37a}$$

$$S_{12} = \frac{S_{12_n} S_{12_m}}{1 - S_{22_m} S_{11_n}} \tag{3.37b}$$

$$S_{21} = \frac{S_{21_m} S_{21_n}}{1 - S_{22_m} S_{11_n}} \tag{3.37c}$$

$$S_{22} = S_{22_n} + \frac{S_{12_n} S_{22_m} S_{21_n}}{1 - S_{22_m} S_{11_n}} \tag{3.37d}$$

   The results are the S-parameters for blocks **A** and **C** in Figure 3-10.

5. **Measure the S-parameters of the on-wafer short/open standards to obtain the pad parasitics.**

   These measurements are made using the Cascade microwave probes calibrated

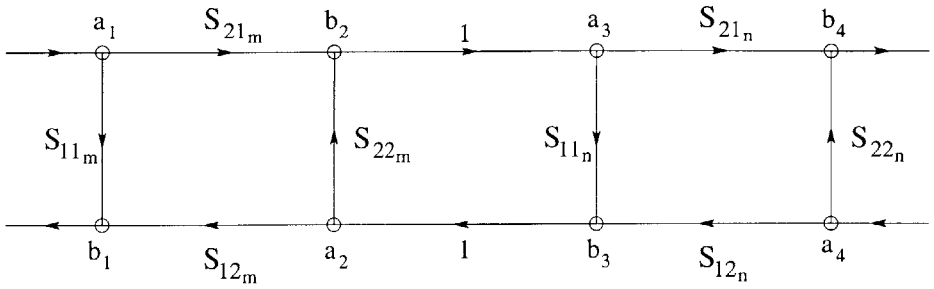

Figure 3-14: S-parameter Cascade

with the impedance standard substrate.

6. **Measure S-parameters of block** B = Device + Pads.

   This information along with the S_{22} of block **A** is used to check the stability of the different source impedances, and verify that the transistor is stable when terminated with a 50 Ω load. This is done using source and load stability circles on the Smith Chart. Source stability circles show the regions of source admittances on the Smith Chart that present a negative resistance at the output of the device ($|\Gamma_{out}| > 1$). In Figure 3-15, all impedances inside the solid circle (low resistance, moderate inductance) cause a negative resistance to be seen looking into the output of the device. This must be verified for each source admittance presented to the device. Load stability circles show the regions of load admittances on the Smith Chart that present a negative resistance looking into the input of the device ($|\Gamma_{in}| > 1$). The area inside the dashed circle in Figure 3-15 (low resistance, low to moderate inductance), cause a negative resistance to be seen looking into the input of the device. In this case, as long as the circle does not enclose the center of the Smith Chart (50 Ω), the device is stable. For further discussion on stability circles consult Gonzalez[21].

7. **Measure 50 Ω noise figure of system at each tuner setting.**

   First, calibrate the noise figure meter to the reference planes shown in Figure 3-10, and then measure the noise figure over a range of frequencies for a set of

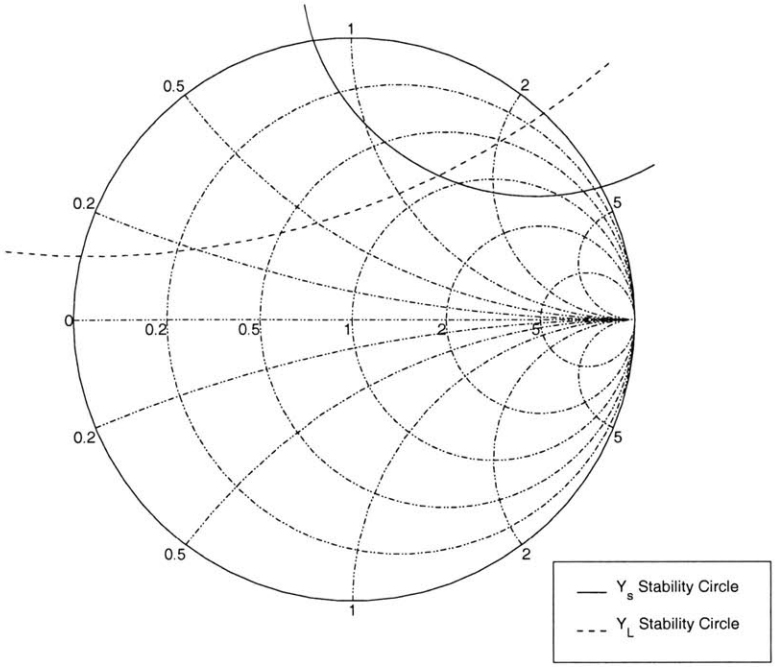

Figure 3-15: Source and Load Stability Circles

source admittances. The measured noise figure is for everything between the calibrated reference planes. The ambient temperature must be set in the noise figure meter to perform a correction for the ENR.[11] The uncertainty of the noise figure measurements may be estimated using the procedure outlined in the Agilent application note AN57-2[35].

8. **Calculate the Noise Figure of the on-wafer device (B).**

To de-embed the tuner, isolators, cables, probes, and bias-Tees, the S-parameters measured above are used to determine the available gain(G_a) of the input and output blocks, **A** and **C** respectively. Because these blocks are passive, the noise factor at $T_o = 290\,\mathrm{K}$ is equal to the loss or the inverse of available gain($1/G_a$).

[11] Special Function 6.0 for the 8970

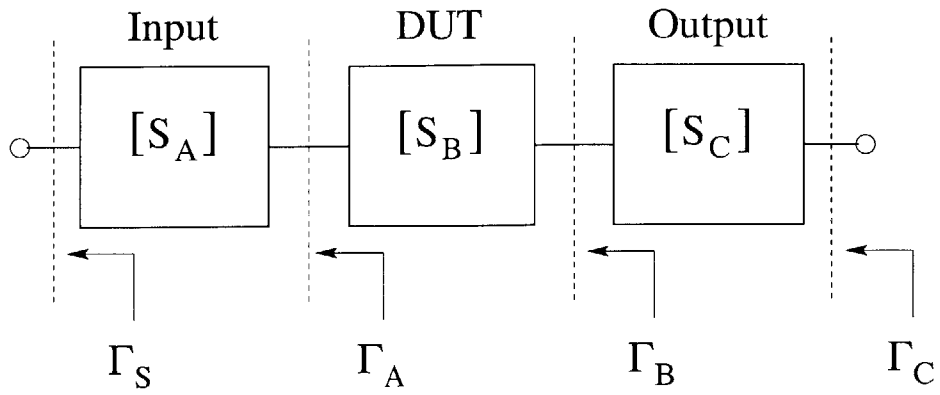

Figure 3-16: De-embedding Input and Output Blocks

Using the same procedure and notation as[27],

$$\Gamma_S = 0.07 \tag{3.38a}$$

$$\Gamma_A = S_{22_A} + \frac{(S_{12_A} S_{21_A} \Gamma_S)}{1 - \Gamma_S S_{11_A}} \tag{3.38b}$$

$$\Gamma_B = S_{22_B} + \frac{S_{12_B} S_{21_B} \Gamma_A}{1 - \Gamma_A S_{11_B}} \tag{3.38c}$$

$$\Gamma_C = S_{22_C} + \frac{S_{12_C} S_{21_C} \Gamma_B}{1 - \Gamma_B S_{11_C}} \tag{3.38d}$$

$$G_{a_A} = \frac{|S_{21_A}|^2 (1 - |\Gamma_S|^2)(1 - |\Gamma_A|^2)}{|(1 - \Gamma_S S_{11_A})(1 - \Gamma_A^* S_{22_A}) - \Gamma_S \Gamma_A^* S_{12_A} S_{21_A}|^2} \tag{3.39a}$$

$$G_{a_B} = \frac{|S_{21_B}|^2 (1 - |\Gamma_A|^2)(1 - |\Gamma_B|^2)}{|(1 - \Gamma_A S_{11_B})(1 - \Gamma_B^* S_{22_B}) - \Gamma_A \Gamma_B^* S_{12_B} S_{21_B}|^2} \tag{3.39b}$$

$$G_{a_C} = \frac{|S_{21_C}|^2 (1 - |\Gamma_B|^2)(1 - |\Gamma_C|^2)}{|(1 - \Gamma_B S_{11_C})(1 - \Gamma_C^* S_{22_C}) - \Gamma_B \Gamma_C^* S_{12_C} S_{21_C}|^2} \tag{3.39c}$$

where Γ_S is the reflection coefficient of the noise source.

Using these results, the noise factor of the input and output blocks are

$$F_A = \left(\frac{1}{G_{a_A}} - 1\right)\frac{T}{T_o} + 1 \tag{3.40a}$$

$$F_C = \left(\frac{1}{G_{a_C}} - 1\right)\frac{T}{T_o} + 1 \tag{3.40b}$$

where T is the ambient temperature at which the measurement was performed, and T_o is the IEEE standard reference temperature of 290 K. If the noise factor measured at the reference planes is F_m, then

$$F_B = G_{a_A}\left(F_m - F_A - \frac{F_C - 1}{G_{a_A} G_{a_B}}\right) + 1 \tag{3.41}$$

9. **Calculate the four noise parameters of the on-wafer device (B).**

To calculate the four noise parameters of block **B**, Equation (3.9) is rearranged as proposed in [41].

$$\mathfrak{Re}\{Y_{s,i}\} F_i = |Y_{s,i}|^2 x_1 - 2\,\mathfrak{Im}\{Y_{s,i}\} x_2 + x_3 + \mathfrak{Re}\{Y_{s,i}\} x_4 \tag{3.42}$$

where i is for each tuner point. The four unknowns are

$$x_1 = R_n \tag{3.43a}$$

$$x_2 = B_{opt} R_n \tag{3.43b}$$

$$x_3 = |Y_{opt}|^2 R_n \tag{3.43c}$$

$$x_4 = F_{min} - 2G_{opt} R_n \tag{3.43d}$$

where $Y_{opt} = G_{opt} + jB_{opt}$. The resulting overdetermined system of equations is solved using least squares fitting.[12] Equations (3.43) can be inverted to deter-

[12]The Matlab \ operator was used.

mine the four noise parameters.

$$R_n = x_1 \tag{3.44a}$$

$$B_{opt} = \frac{x_2}{x_1} \tag{3.44b}$$

$$G_{opt} = \sqrt{\frac{x_3}{x_1} - \left(\frac{x_2}{x_1}\right)^2} \tag{3.44c}$$

$$F_{min} = x_4 + 2\sqrt{x_1 x_3 - x_2^2} \tag{3.44d}$$

10. **De-embed pads to transform the four noise parameters of block B to the extrinsic MOSFET four noise parameters.**

    The open and short on-wafer standards are used to perform the transformation using a procedure parallel to the one described in Section 3.5.1 for de-embedding the S-parameter measurements. Correlation matrices[42] are used to represent the noise contributions of the different two-ports that are being added or subtracted in the de-embedding procedure. The correlation matrix of a passive two-port in admittance form is $2kT\Re\mathfrak{e}\{\mathbf{Y}\}$. An outline of the steps involved in the de-embedding is given in Figure 3-17. The blocks labeled A2B are two-port conversions from A-parameters to B-parameters. The three results of this de-embedding procedure are the S-parameters, the MOSFET noise parameters, and the four noise parameters. The details of the matrix manipulations are in Appendix A.

11. **Remove series parasitics of the transistor.**

    Up to this point no assumptions have been made about the device being measured. In fact, it has not even been assumed that it is a MOSFET under investigation. The series parasitics obtained either from measurement or layout are removed by subtracting the Z-parameters of the extrinsic device and the series parasitics resulting in the intrinsic device Z-parameters. At this point, a

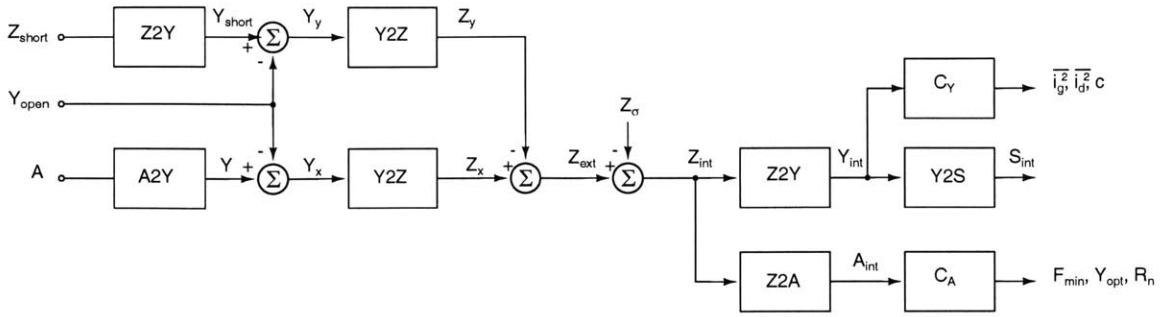

Figure 3-17: Block Diagram of Pad De-embedding Procedure

simple small signal model may be determined from the intrinsic Y-parameters

$$C_{gs} = \frac{\mathfrak{Im}\{Y_{11}\} + \mathfrak{Im}\{Y_{12}\}}{\omega} \tag{3.45a}$$

$$C_{gd} = -\frac{\mathfrak{Im}\{Y_{12}\}}{\omega} \tag{3.45b}$$

$$C_{ds} = \frac{\mathfrak{Im}\{Y_{22}\} + \mathfrak{Im}\{Y_{12}\}}{\omega} \tag{3.45c}$$

$$g_m = |Y_{21} - Y_{12}| \tag{3.45d}$$

$$\phi = \angle(Y_{21} - Y_{12}) \tag{3.45e}$$

$$r_o = \frac{1}{\mathfrak{Re}\{Y_{22} + Y_{12}\}} \tag{3.45f}$$

12. **Calculate $\overline{i_g^2}$, $\overline{i_d^2}$, and c from $\mathbf{C_{Y_{int}}}$.**

From the definition of the correlation matrices

$$\overline{s_i s_j^*} = 2\Delta f \, C_{s_i, s_j^*} \qquad i, j = \{1, 2\} \tag{3.46}$$

Therefore,

$$\overline{i_d^2} = 2\Delta f\, C_{Y_{i_2,i_2^*}} \tag{3.47a}$$

$$\overline{i_g^2} = 2\Delta f\, C_{Y_{i_1,i_1^*}} \tag{3.47b}$$

$$c_{int} = \frac{C_{Y_{i_1,i_2^*}}}{\sqrt{C_{Y_{i_1,i_1^*}} C_{Y_{i_2,i_2^*}}}} \tag{3.47c}$$

13. **Determine the associated available gain from the device at noise match.**

With Y_{opt} as the source resistance, the available gain is

$$G_{ass} = \frac{1 - |\Gamma_{opt}|^2}{|1 - S_{11_{int}}\Gamma_{opt}|^2} |S_{21_{int}}|^2 \frac{1}{1 - |\Gamma_{out}|^2} \tag{3.48}$$

where Γ_{opt} is the reflection coefficient of Y_{opt} in a $50\,\Omega$ system, and

$$\Gamma_{out} = S_{22_{int}} + \frac{S_{12_{int}} S_{21_{int}} \Gamma_{opt}}{1 - S_{11_{int}}\Gamma_{opt}} \tag{3.49}$$

This value can then be compared to the maximum available gain(MAG).

$$\text{MAG} = \begin{cases} \dfrac{|S_{21_{int}}|}{|S_{12_{int}}|}\left(K - \sqrt{K^2 - 1}\right), & \text{if } K > 1 \text{ and } B_1 > 0 \\ \dfrac{|S_{21_{int}}|}{|S_{12_{int}}|}, & \text{if } K \leq 1 \text{ or } B_1 \leq 0 \end{cases} \tag{3.50}$$

where K and B_1 are the stability factors and are defined as

$$K = \frac{1 - |S_{11_{int}}|^2 - |S_{22_{int}}|^2 + |\Delta|^2}{2|S_{12_{int}} S_{21_{int}}|} \tag{3.51a}$$

$$B_1 = 1 + |S_{11_{int}}|^2 - |S_{22_{int}}|^2 - |\Delta|^2 \tag{3.51b}$$

$$\Delta = S_{11_{int}} S_{22_{int}} - S_{12_{int}} S_{21_{int}} \tag{3.51c}$$

This completes the measurement and de-embedding of the transistors. With the noise characterization obtain from these measurements, comments on the intrinsic noise sources and their correlation can be made.

Chapter 4

Results

4.1 DC Characterization

An equivalent circuit diagram of the DC measurement setup is shown in Figure 4-1. The resistors R_1, R_2, and R_3 represent cable and probe contact resistances in the measurement setup. Because of these resistances, it is impossible to control the internal gate-to-source(V_{GS_i}) and drain-to-source(V_{DS_i}) voltages. All the measurements are made with these series resistances at each terminal. DC performance curves are measured with one terminal voltage held constant while the other terminal voltage is swept. If the effects of the series resistances are mathematically removed from the measurements, the internal voltages V_{GS_i} and V_{DS_i} are dependent on the drain current. For this reason, all the DC performance curves given in this chapter include the effects of the cable and probe contact resistances.[1] These resistances should not significantly alter the device performance data, but they do cause a small inherent difference between the measured results the internal transistor performance.

[1]The losses associated with the cables and probes must be removed for the high frequency and noise measurements.

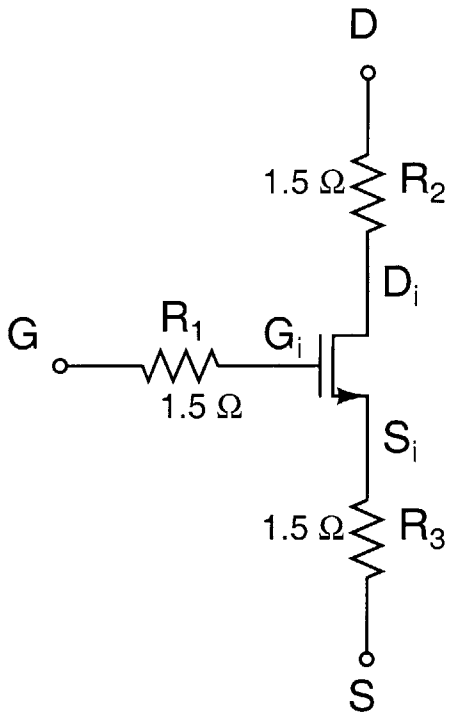

Figure 4-1: DC Characterization Equivalent Circuit

4.1.1 Standard Performance Curves

The I_D–V_{DS} curves for the 98 µm wide devices are given in Figures 4-2 to 4-4. Immediately apparent from the graphs is the significant decrease in output resistance as device length approaches the minimum for the technology. Figure 4-5 shows $\log(I_D)$–V_{GS} curves for the 98 µm devices at $V_{DS} = 1.0\,\mathrm{V}$. The off current(I_{off}), sub-threshold slope(S), and

$$n = \frac{S}{2.3\,kT/q} \tag{4.1}$$

for the three device lengths are listed in Table 4.1.

4.1.2 Analog Design Curves

Based on the framework for analog design characterization presented in Sodini et. al.[43], log-log graphs of g_m/W versus I_D/W and r_o versus I_{Do}/W are presented in Figures 4-

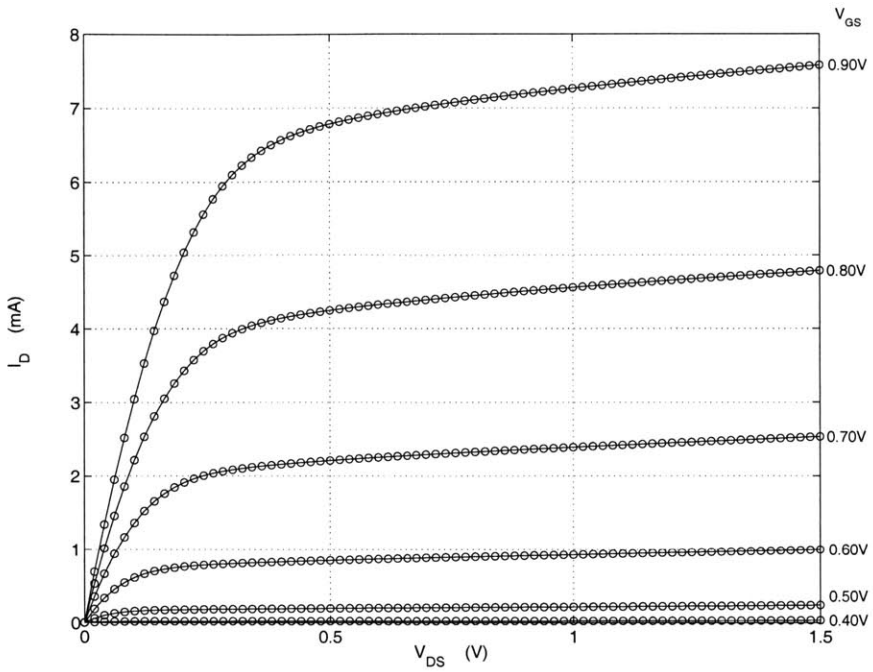

Figure 4-2: I_D versus V_{DS} and V_{GS} ($W/L = 98\,\mu\text{m}/0.275\,\mu\text{m}$)

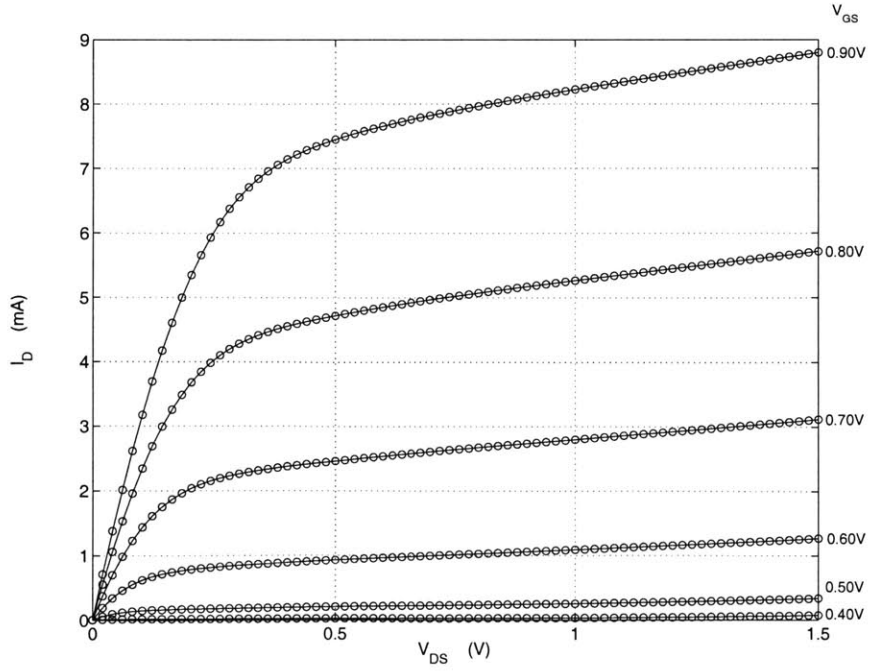

Figure 4-3: I_D versus V_{DS} and V_{GS} ($W/L = 98\,\mu\text{m}/0.20\,\mu\text{m}$)

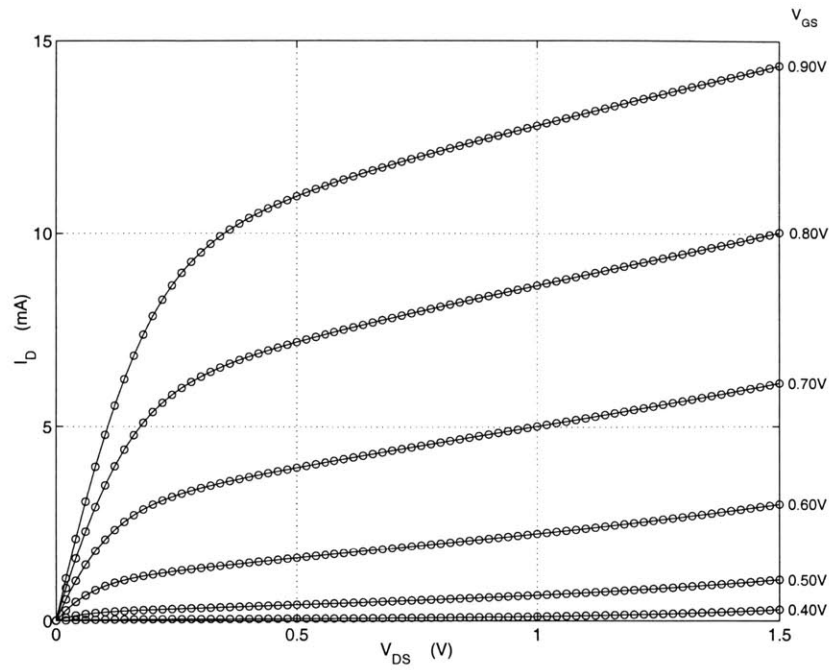

Figure 4-4: I_D versus V_{DS} and V_{GS} ($W/L = 98\,\mu\text{m}/0.15\,\mu\text{m}$)

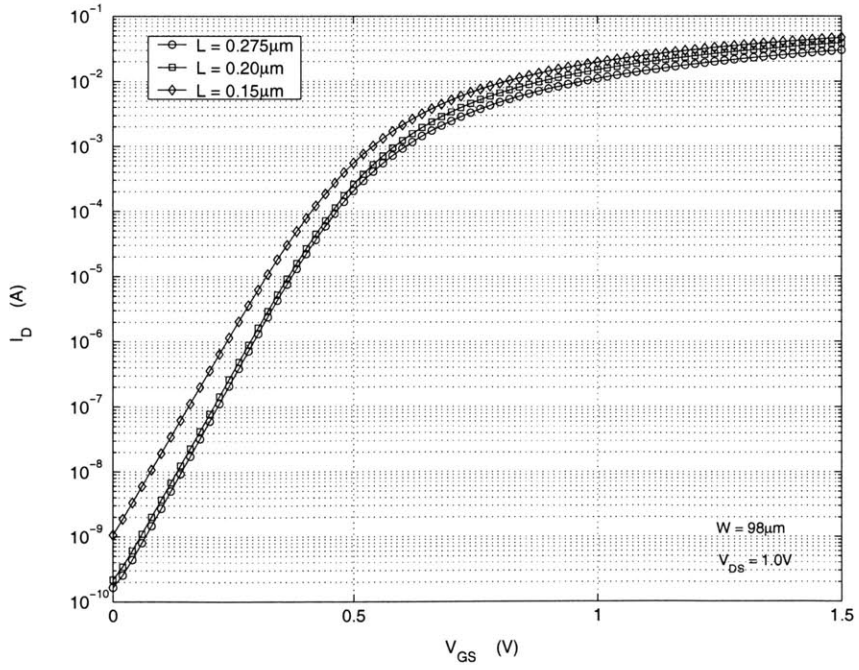

Figure 4-5: $\log(I_D)$ versus V_{GS} ($W = 98\,\mu\text{m}$, $V_{DS} = 1.0\,\text{V}$)

L (μm)	I_{off} (nA)	S (mV/dec)	n
0.275	0.165	82.7	1.38
0.200	0.218	83.0	1.39
0.150	1.061	90.5	1.51

Table 4.1: Sub-threshold Data ($W = 98\ \mu\text{m}$, $V_{DS} = 1.0\ \text{V}$)

9 and 4-7. A brief discussion of the results follows.

Output Resistance

If the output resistance is modeled as channel length modulation

$$I_D = I_{Do}\left(\frac{L}{L - l_p}\right) \tag{4.2}$$

where l_p is the pinch-off point, L is the channel length, and I_{Do} is the drain current at the edge of saturation. If it can also be assumed that the pinch-off point is not very different from the channel length ($l_p/L \ll 1$), Equation (4.2) can be approximated as

$$I_D \approx I_{Do}\left(1 + \frac{l_p}{L}\right), \tag{4.3}$$

then the small signal output conductance($g_o = 1/r_o$) is

$$g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{I_{Do}}{L}\frac{\partial l_p}{\partial V_{DS}} \tag{4.4}$$

This result states that the output resistance should be proportional to $1/I_{Do}$ and L. According to the simplest MOSFET output resistance theories[16], the ratio l_p/L can be approximated with an Early voltage like term.

$$I_D = I_{Do}\left(1 + \frac{V_{DS} - V_{Dsat}}{V_A}\right) \tag{4.5}$$

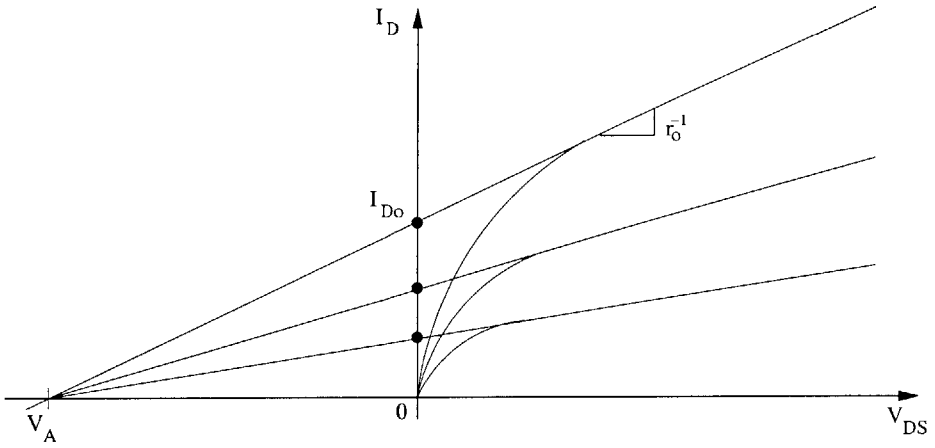

Figure 4-6: MOSFET Early Voltage Model

where V_A is similar to the Early voltage in a bipolar transistor. Often, the variable $\lambda = 1/V_A$ is used in Equation (4.5) for MOSFET analysis. According to this expression, the current I_{Do} is the expression for the drain current at the edge of saturation

$$I_D\Big|_{V_{Dsat}} = I_{Do} \tag{4.6}$$

If V_A is large compared to V_{Dsat}, then Equation (4.5) can be approximated as

$$I_D = I_{Do}\left(1 + \frac{V_{DS}}{V_A}\right) \tag{4.7}$$

For this expression, the extrapolated lines from the I_D versus V_{DS} intersect the V_{DS} axis at $-V_A$ for all V_{GS}, and the reference current I_{Do} is the drain current extrapolated to $V_{DS} = 0$ (Figure 4-6). Therefore,

$$g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{I_{Do}}{V_A} \tag{4.8}$$

This result states that the output resistance is proportional to $1/I_{Do}$, and the Early voltage is proportional to L.

From Figure 4-7 the output resistance of both the 0.275 μm and 0.20 μm devices

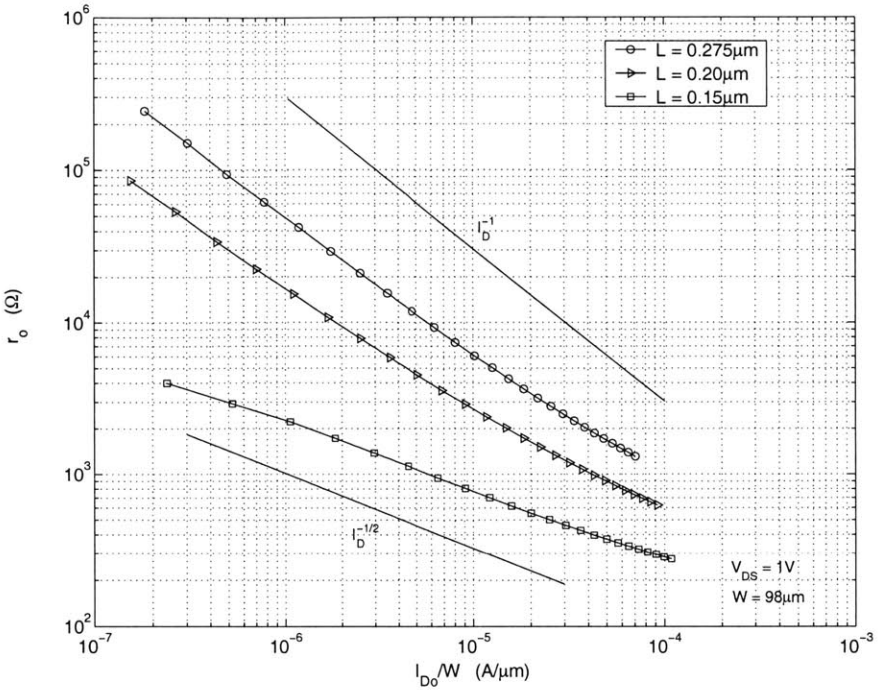

Figure 4-7: r_o versus I_D/W ($W = 98\,\mu\text{m}$)

is approximately proportional to $1/I_D$. The small deviation in output resistance from the $1/I_{Do}$ behavior at high currents is possibly due to the series resistances in the measurement setup. Assuming a simple low frequency small-signal model, it can be shown that the output resistance is

$$R_{out} = R_2 + R_3 + r_o(1 + g_m R_3) \approx r_o(1 + g_m R_3) \tag{4.9}$$

which is approximately r_o for low g_m and increases as g_m increases.[2] Further study is required to explain the apparent $1/\sqrt{I_D}$ behavior of the 0.15 µm device. Figure 4-8 shows that the Early voltage increases as the gate-to-source voltage increases or equivalently as the drain current increases, which is inconsistent with the channel length modulation model described above.

These discrepancies indicate that either the approximations used in deriving the

[2]For $g_m = 60\,\text{mS}$ and $R_3 = 1.5\,\Omega$, R_{out} is roughly 10 % larger than r_o.

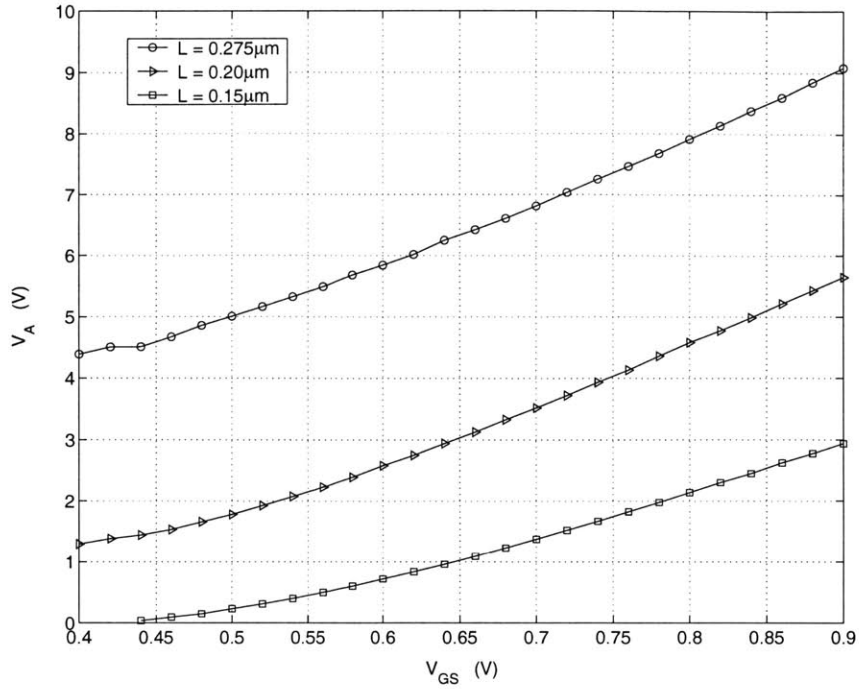

Figure 4-8: V_A versus V_{GS} ($W = 98\,\mu m$)

output resistance model need to be reexamined, or the mechanism causing the increase in drain current for an increase in drain-to-source voltage is not channel length modulation. If channel length modulation is still the cause of the output resistance, the assumption that the pinch-off point is a small fraction of the channel length might not be valid. Another possibility is that this one-dimensional model is an over simplification of a two-dimensional problem. However, at short channel lengths, channel length modulation might not be the dominant cause for the increasing drain current with increasing drain-to-source voltage. Other possible causes are Drain Induced Barrier Lowering(DIBL) and impact ionization[16],[44],[45].

If the drain-to-source voltage influences the depletion region underneath a significant portion of the gate, an increase in the drain-to-source voltage causes a decrease in the threshold voltage. This effect is known as Drain Induced Barrier Lowering(DIBL). A decrease in threshold voltage causes an increase in the drain current, resulting in an output resistance due to DIBL.

Impact ionization occurs if the lateral electric field in the channel is high enough such that the electrons in the channel have enough energy to generate additional electron-hole pairs when they impact with the silicon lattice atoms. The additional electrons contribute to the drain-to-source current, and the holes result in a drain-to-bulk current. Both of these currents contribute to the drain terminal current. The drain-to-bulk current also causes a voltage drop in the finite resistance of the bulk, resulting in a source-to-bulk voltage that decreases the threshold voltage. This decrease in threshold voltage causes a further increase in the drain current. If the electric fields are high enough, avalanche breakdown can occur.

Another factor that could influence the output resistance is the pocket implant used in short gate length technologies to control DIBL. As discussed in Chatterjee et. al.[46] and Buss[47], the pocket implant decreases the Early voltage and the rate at which the Early voltage increases with gate length.

Because only three different device lengths were measured, it is not clear that V_A is proportional to the channel length. Figures 4-7 and 4-8 do confirm that increasing channel length does increase V_A.

Transconductance

The graph of g_m/W versus I_D/W in Figure 4-9 shows three different regions of device operation.[3] At low currents, the device is operating in sub-threshold and transconductance is proportional to drain current (4.10a). For a small range of moderate drain currents, transconductance follows a square-law dependence (4.10b). At high current levels, the transconductance becomes independent of drain current as velocity

[3]Appendix B gives justification for plotting g_m and I_D instead of the values corrected for finite output resistance.

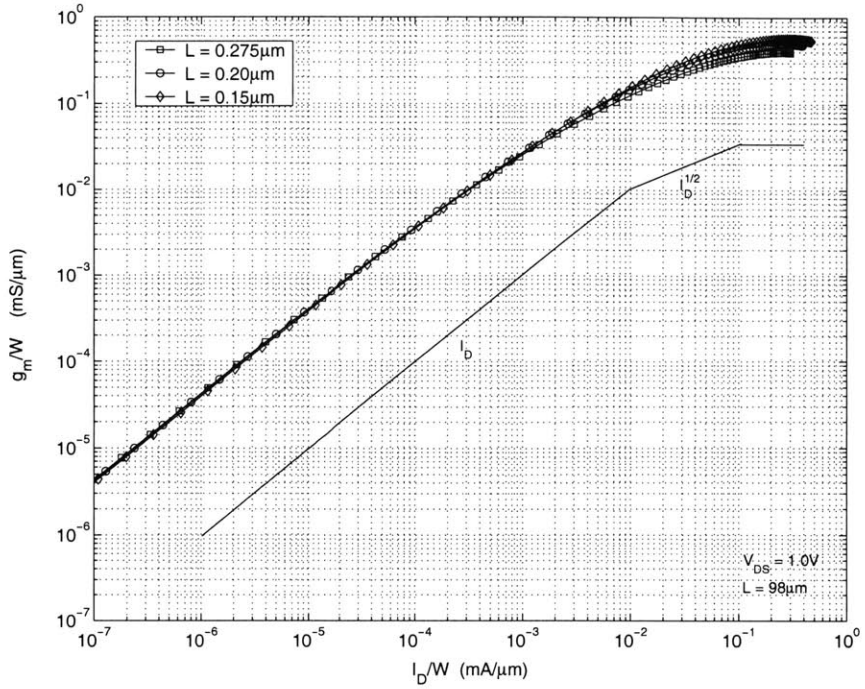

Figure 4-9: g_m/W versus I_D/W ($W = 98\,\mu\text{m}$)

saturation limits the transconductance (4.10c). Mathematically,

$$g_m = \frac{q\,I_D}{n\,kT} \qquad \text{(sub-threshold)} \tag{4.10a}$$

$$g_m = \sqrt{2\frac{W}{L}\mu\,C_{ox}I_D} \qquad \text{(square-law)} \tag{4.10b}$$

$$g_m = KWC_{ox}v_{\text{sat}} \qquad \text{(velocity saturation)} \tag{4.10c}$$

4.1.3 Gate Current

According to Lee et. al.[48] and Lo et. al.[49], the direct tunneling gate current for an oxide thickness of 2.5 nm is about $1 \times 10^{-3}\,\text{A/cm}^2$ at $V_{GS} = 1.5\,\text{V}$. This value matches with the measured gate current density at $V_{GS} = 1.5\,\text{V}$ in Figure 4-10. At lower V_{GS}, the reverse bias leakage of the protection diode dominates the gate

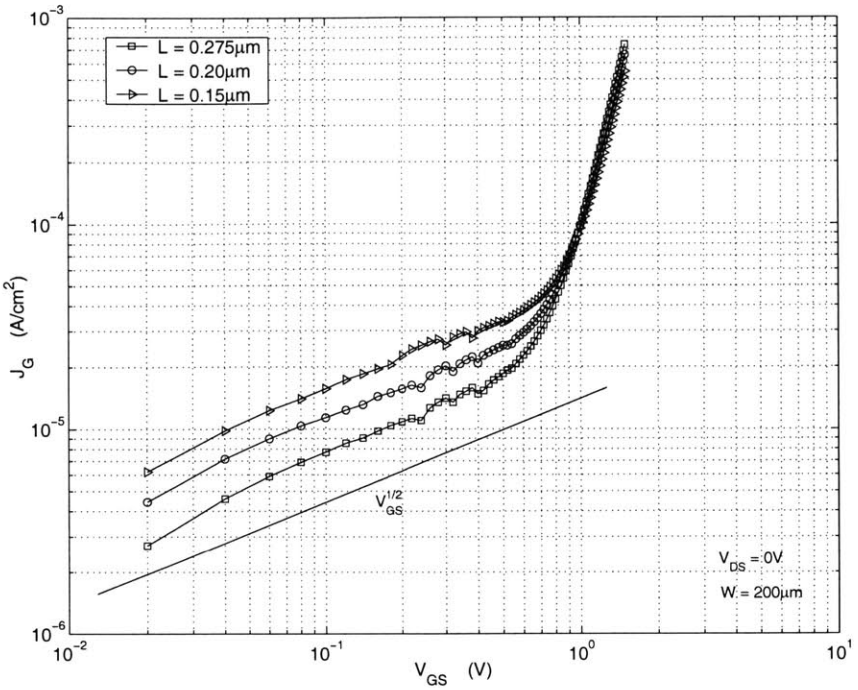

Figure 4-10: Gate Tunneling Current Density versus V_{GS}

current.[4] The reverse bias current increases as the square-root of voltage because the diode depletion width increases as the square-root of reverse bias voltage[50]. The slope of current density versus gate-to-source voltage is 1/2 (log-log) verifying that it is reverse bias diode leakage current.

The gate current versus gate-to-source voltage is plotted in Figure 4-11. Assuming gate tunneling current generates a shot noise in the gate circuit, the maximum gate tunneling shot noise current is

$$\overline{i_G^2} = 2qI_G \approx 2q(100\,\text{pA}) = 3.2 \times 10^{-29}\,\text{A}^2/\text{Hz} \tag{4.11}$$

This value must be compared to the induced gate noise current at the frequency of operation to determine its relative importance to low noise design.

[4]This diode was required in the layout to meet the process antenna design rule.

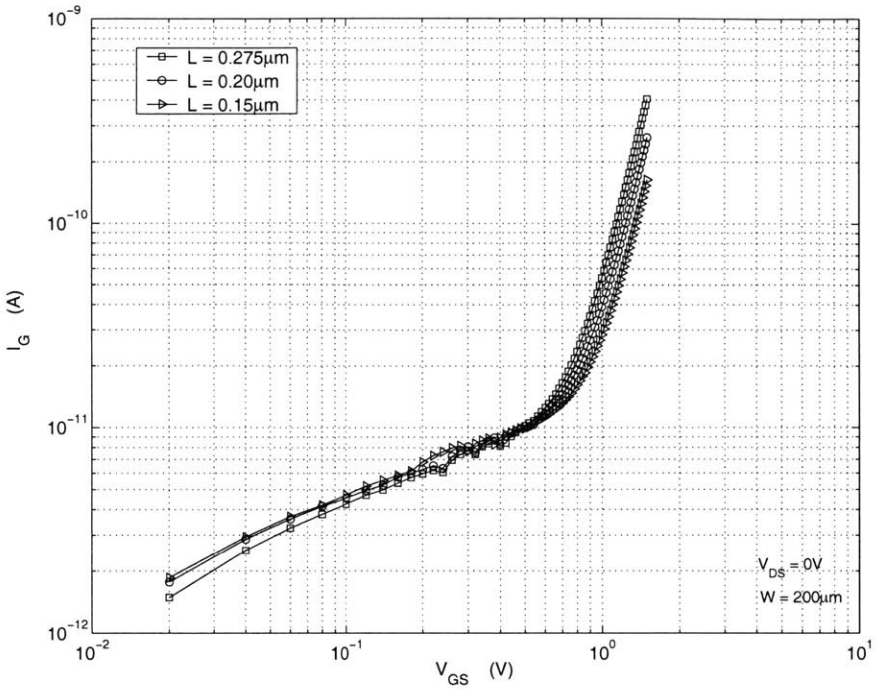

Figure 4-11: Gate Tunneling Current versus V_{GS}

4.1.4 Transconductance versus Zero-Bias Drain Conductance

Often when the device is operating in the saturation region, the zero-bias drain conductance

$$g_{do} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0} \tag{4.12}$$

in the drain noise current expression($4kT\gamma g_{do}\,\Delta f$), is replaced with the device transconductance

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}\geq V_{Dsat}} \tag{4.13}$$

Using a first order expression for drain current,[5] it can be easily shown that

$$g_{do} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T) = g_m \tag{4.14}$$

[5]Also known as the square-law model.

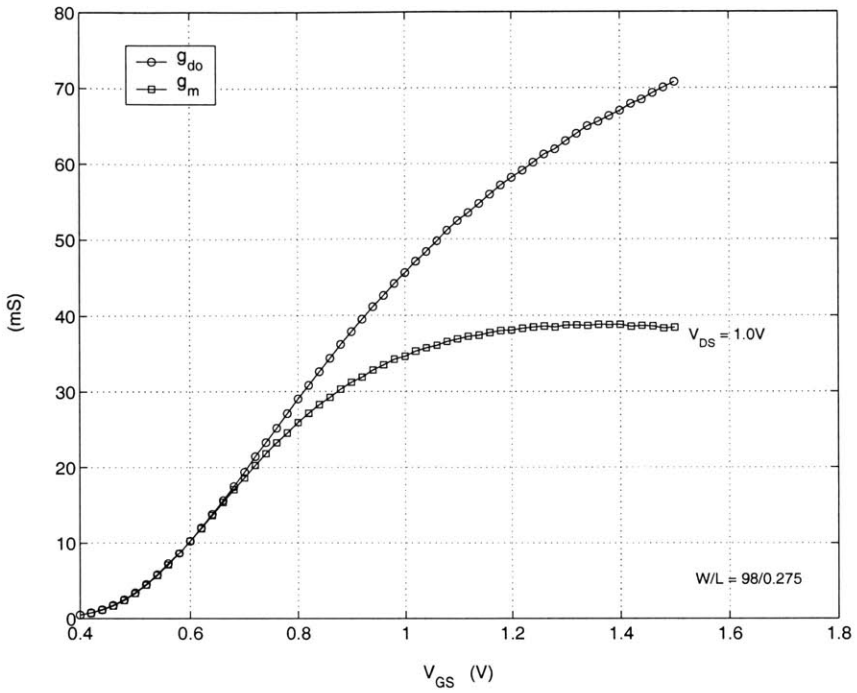

Figure 4-12: g_m and g_{do} versus V_{GS} ($W/L = 98\,\mu m/0.275\,\mu m$)

However, with the addition of velocity saturation effects and mobility degradation, these two parameters are not necessarily equal. Figure 4-12 is a plot of both g_m and g_{do} for a $98\,\mu m/0.275\,\mu m$ device. Notice that at high V_{GS} when velocity saturation effects limit transconductance, a large difference between g_m and g_{do} exists, but at lower gate voltages they are approximately equal. For gate overdrives[6] of 100-200 mV, the approximation is quite reasonable.

4.2 S-parameters

4.2.1 Pad Characterization

Figure 4-13 shows an approximate circuit model for the on-wafer probe pads. This model was determined using measured data from the open and short reference struc-

[6] V_T is between 0.4 and 0.5 V.

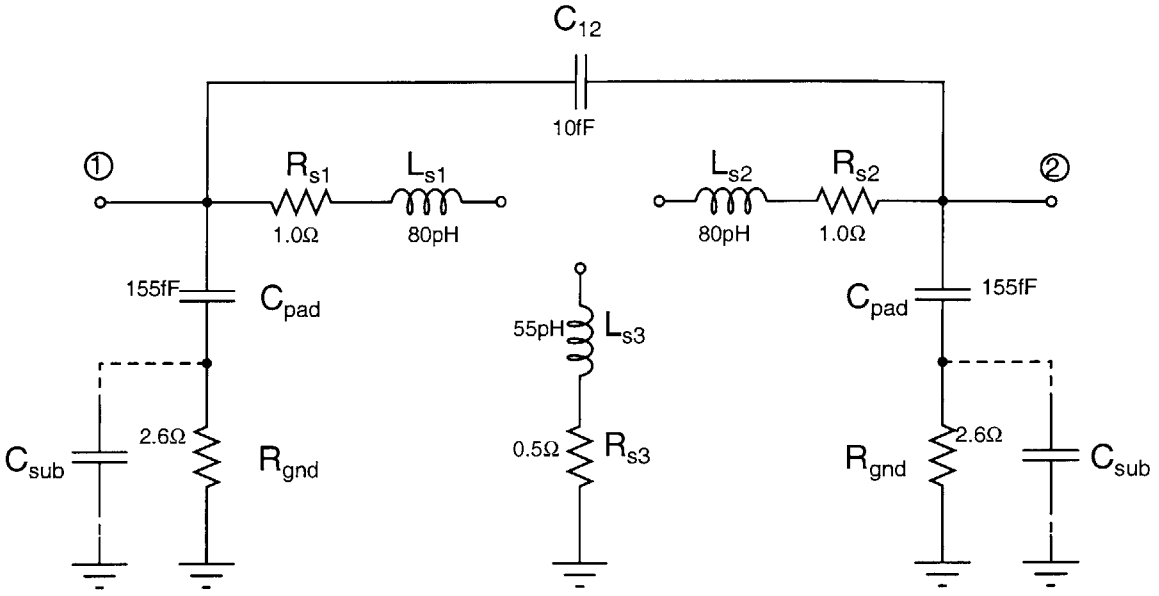

Figure 4-13: RF Pad Circuit Model

tures. Important things to notice from this model are that the n^+ ground plane under the pads does a good job of minimizing the shunt pad losses, and the series parasitics are also small. Small losses and parasitics in the pad structure should improve the accuracy of the on-wafer measurements because the situation of subtracting two measurements of roughly the same value to determine the device performance is avoided.

4.2.2 Unity Current Gain Frequency versus I_d/W

Figure 4-14 shows the unity current gain frequency(f_T) as a function of drain current per unit width for the 98 μm devices. Neglecting the drain-to-gate overlap capacitance(C_{gd}), the unity current gain frequency may be approximated as

$$f_T \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}} \tag{4.15}$$

Figure 4-15 plots $f_T \times L$ versus I_D/W. This graph removes the length dependence from f_T due to C_{gs} showing that the dependence of f_T on I_D/W is identical to that of g_m. Notice that at lower currents, the device is operating in sub-threshold where transconductance per unit drain current is independent of device length. Therefore, all the curves in Figure 4-15 overlap at lower I_D/W, and progress through a square-law region and finally reach a maximum from velocity saturation.

Figure 4-16 shows the dependence of f_T when the drain-to-source voltage is varied. The slight increase in f_T at $V_{DS} = 1.5\,\mathrm{V}$ compared to $V_{DS} = 1.0\,\mathrm{V}$ is probably due to DIBL. The decrease in V_T at higher V_{DS} causes a small increase in transconductance and therefore, f_T. For the $V_{DS} = 0.5\,\mathrm{V}$ curve, f_T falls off at higher currents because the device is entering the triode region and g_m is decreasing.

4.2.3 Series Parasitic Extraction

Essential to the accuracy of the calculation of the intrinsic noise sources is the precise extraction of the series parasitic impedances. Resistive components add noise to the extrinsic device that would corrupt extracted values for $\overline{i_g^2}$, $\overline{i_d^2}$, and their correlation.

The approach initially attempted for series parasitic extraction was the one proposed by Raskin et. al.[34] and described in Chapter 3. The extraction technique was verified using simulation of a test circuit identical to that assumed in Raskin et. al.[34]. When this technique was applied to measured data(Figures 4-18–4-20), resistances extracted were significantly larger than those estimated from layout and process parameters (Table 4.2). From a DC measurement at $V_{DS} = 0\,\mathrm{V}$ and $V_{GS} = 1.5\,\mathrm{V}$, the sum of the source and drain resistances is approximately $6.0\,\Omega$, which matches with the layout estimates.

This indicates that the devices being measured cannot be modeled as the extraction theory proposes. Another indication that the model is inadequate is the frequency dependence of the extracted values for r_o and C_{ds}. As shown in the next section, a drain-to-bulk capacitance C_{db}, substrate resistance R_b, and substrate capacitance C_{si} need to be included in the device modeling to obtain frequency independent modeling

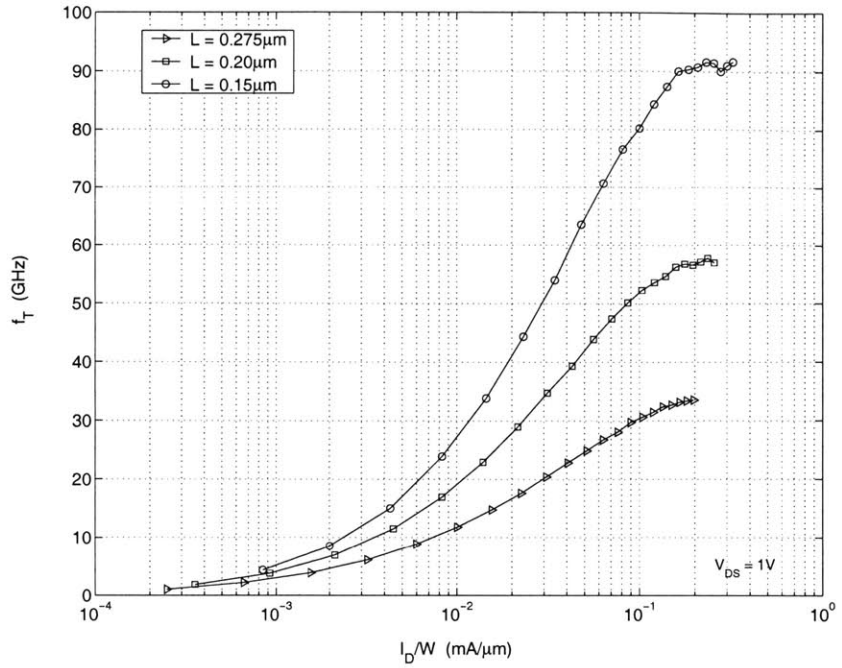

Figure 4-14: f_T versus I_D/W ($W = 98\,\mu\text{m}$, $V_{DS} = 1.0\,\text{V}$)

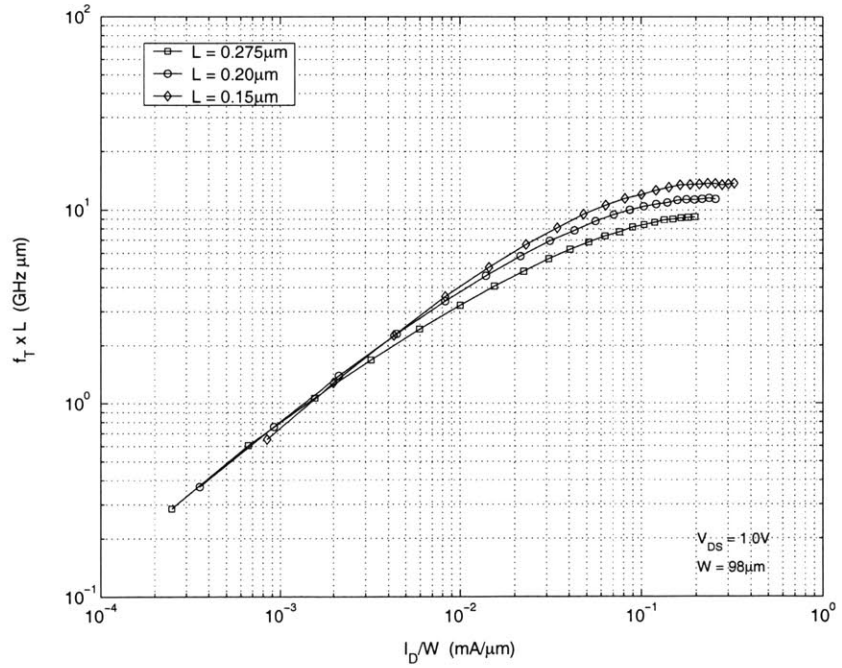

Figure 4-15: $f_T \times L$ versus I_D/W ($W = 98\,\mu\text{m}$, $V_{DS} = 1.0\,\text{V}$)

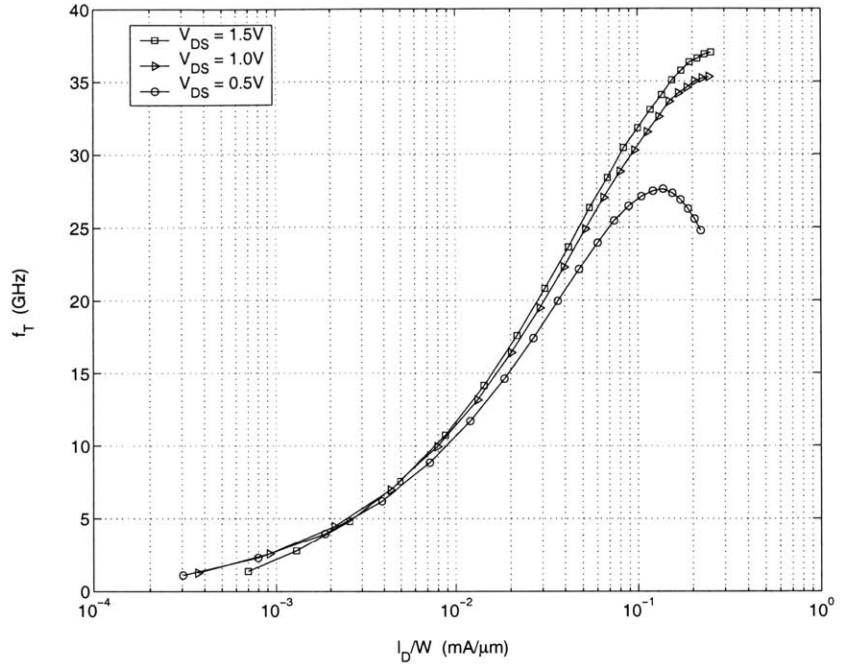

Figure 4-16: f_T versus I_D/W for different V_{DS} ($W/L = 200\,\mu\text{m}/0.275\,\mu\text{m}$)

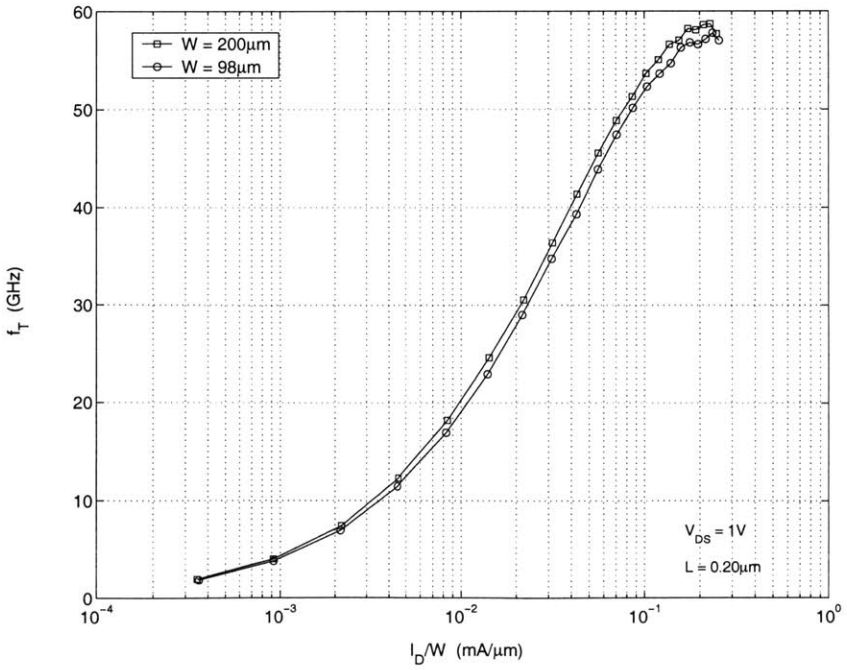

Figure 4-17: f_T versus I_D/W at different W ($V_{DS} = 1.0\,\text{V}$)

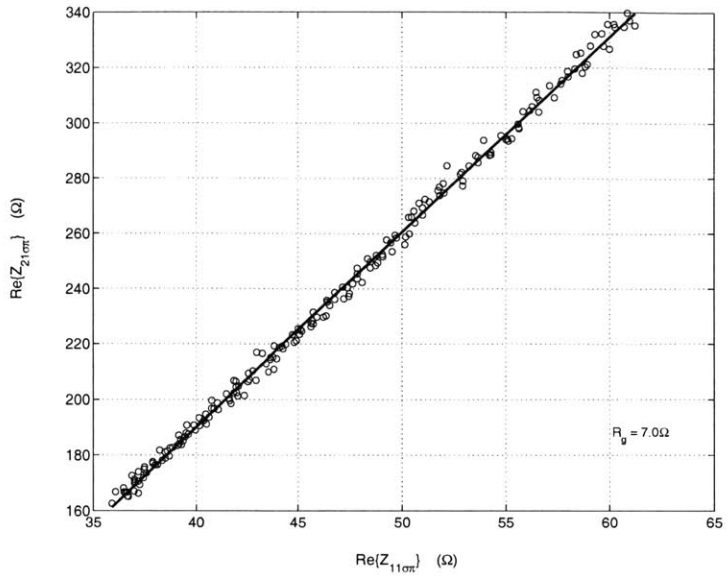

Figure 4-18: Series Parasitic Extraction (R_g) ($W/L = 200\,\mu\text{m}/0.275\,\mu\text{m}$, $2\,\text{GHz} \leq f \leq 6\,\text{GHz}$)

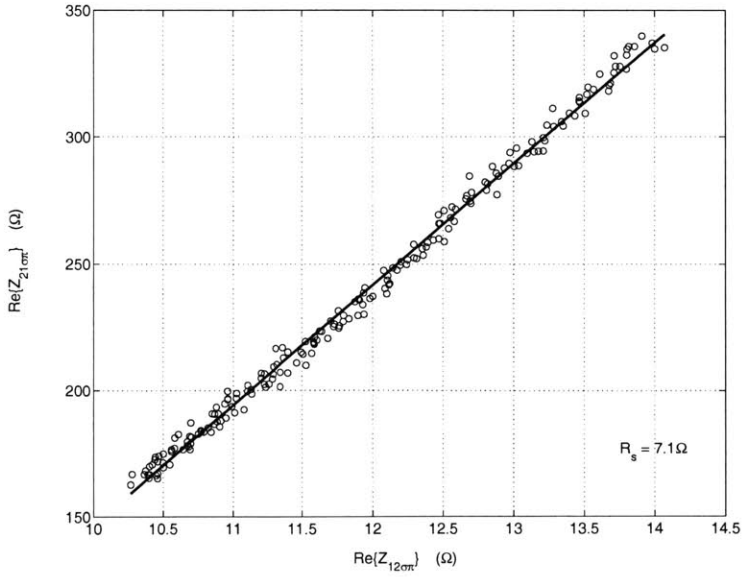

Figure 4-19: Series Parasitic Extraction (R_s) ($W/L = 200\,\mu\text{m}/0.275\,\mu\text{m}$, $2\,\text{GHz} \leq f \leq 6\,\text{GHz}$)

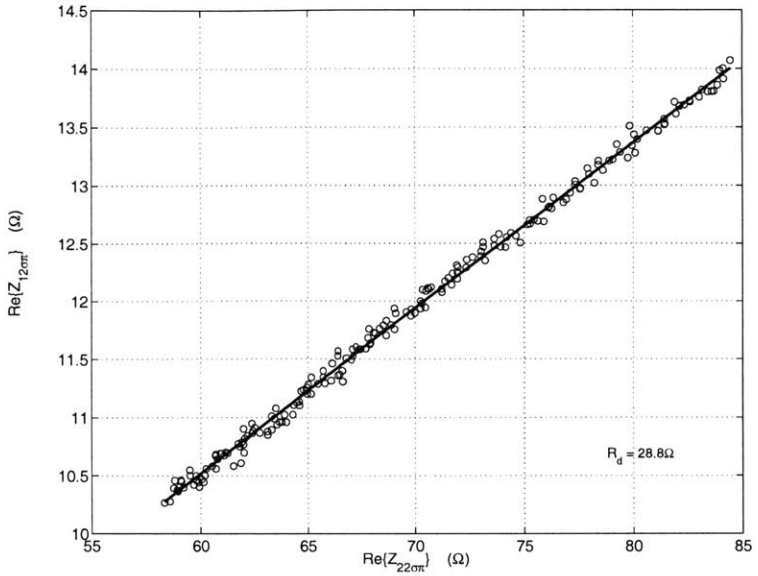

Figure 4-20: Series Parasitic Extraction (R_d) ($W/L = 200\,\mu\text{m}/0.275\,\mu\text{m}$, , $2\,\text{GHz} \leq f \leq 6\,\text{GHz}$)

	R_g (Ω)	R_s (Ω)	R_d (Ω)
Raskin[34]	7.0	7.1	29
Layout	9.0	2.5	2.7

Table 4.2: Extracted Series Parasitics ($W/L = 200\,\mu\text{m}/0.275\,\mu\text{m}$)

parameters.

4.2.4 Output Admittance Modeling

To illustrate that modeling of the output impedance requires a drain-to-bulk capacitance, substrate resistance and substrate capacitance, the model in Figure 4-21 is fit to output admittance data from a $200\,\mu\text{m}/0.275\,\mu\text{m}$ device, where

$$Y_{out} = Y_{22} + Y_{12} \tag{4.16}$$

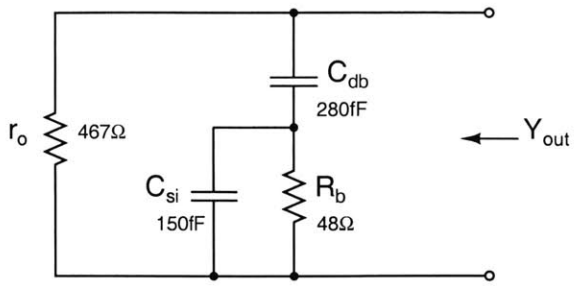

Figure 4-21: Approximate Output Admittance Model

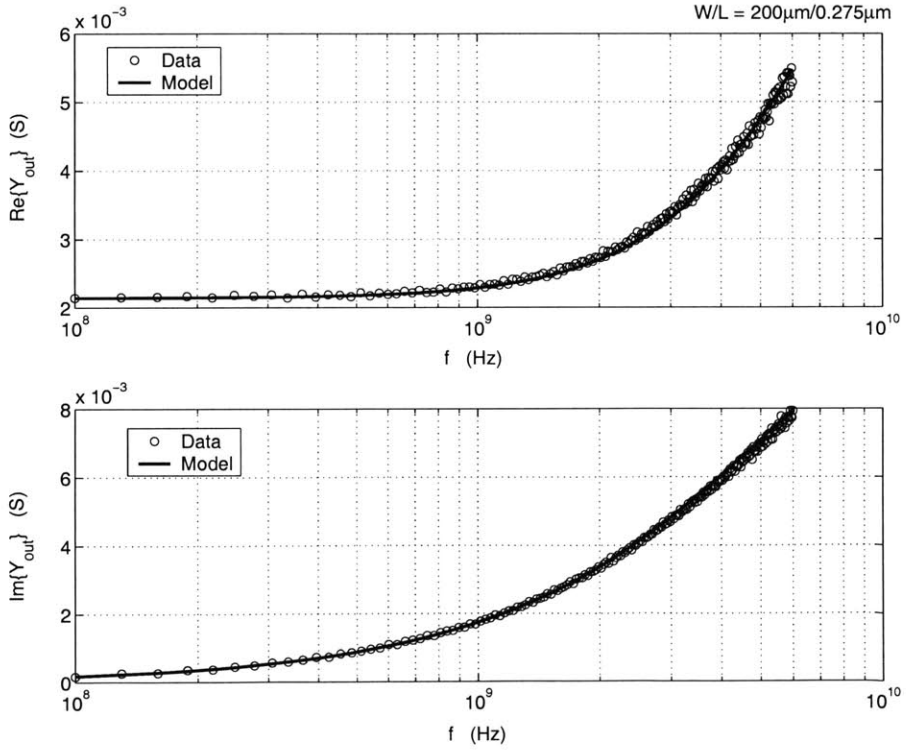

Figure 4-22: Output Admittance ($V_{DS} = 1.0\,\mathrm{V}$, $I_D = 20.5\,\mathrm{mA}$)

It is assumed that R_g is known precisely and its effect has been removed from the Y-parameters used to calculate Y_{out}. For this example, the layout estimate for R_g of $9.0\,\Omega$ was used.

At low frequencies,

$$Z_{out} \approx r_o(1 + g_m R_s) \tag{4.17}$$

which may be approximately r_o if $g_m R_s \ll 1$. For reasonable gain($|S_{21}| = 14\,\text{dB}$) in a $50\,\Omega$ system, g_m needs to be on the order of

$$g_m = \frac{|S_{21}|}{2Z_o} = 50\,\text{mS} \tag{4.18}$$

If R_s is $2\,\Omega$, neglecting R_s causes a $10\,\%$ error in Z_{out}. This assumption is not always justified, but for this analysis, R_s will be ignored. From the plot of Z_{out} at low frequencies, r_o is determined to be $467\,\Omega$.

The complete expression for Y_{out} from the model valid over all frequencies is

$$Y_{out} = g_o + Z_{db}^{-1} \tag{4.19}$$

where

$$Z_{db} = Z_{si} + \frac{1}{j\omega C_{db}} \tag{4.20}$$

and

$$Z_{si} = \frac{R_b}{1 + j\omega C_{si} R_b} \tag{4.21}$$

at moderate frequencies, values for R_b and C_{db} are obtained from plots of the real and imaginary parts of Z_{db}.

$$Z_{db} = R_b + \frac{1}{j\omega C_{db}} \tag{4.22}$$

If C_{si} is excluded from the model, R_b and C_{db} have a slight frequency dependence at the upper end of the frequency range. The capacitance C_{si} was added to the model

and its value determined from

$$Y_{si} = Z_{si}^{-1} = \frac{1}{R_b} + j\omega C_{si} \tag{4.23}$$

One final important assumption in this analysis are that R_d, which is in series with Z_{out}, has a negligible effect on the output admittance. Assuming a value of 2.7 Ω for R_d from the layout estimations, the effect on the output admittance is small for this example. Figure 4-22 shows the output admittance versus frequency along with the results from the circuit model in Figure 4-21.

4.3 Noise Characterization

4.3.1 Test Setup

The combined input isolator and tuner has been characterized across the corresponding isolator frequency ranges (2-4 GHz and 4-6 GHz). Figure 4-23 shows the S-parameters for the 2-4 GHz range tuner/isolator combination. The curve labels (2.25, 0.50, 0.00) correspond to the probe depth on the tuner, where 0.00 corresponds to the maximum depth. The tuner/isolator is clearly not reciprocal ($|S_{12}| \neq |S_{21}|$) because of the isolator. Also, notice that the isolator maintains a good input match even when the tuner is set for a high reflection coefficient at port 2. Another interesting property illustrated in Figure 4-23 is that the insertion loss of the tuner increases as the magnitude of the reflection coefficient it presents at port 2 increases.

An example of the results of the S-parameter calculation for the input and output cables and probes is presented in Figure 4-24. These results are consistent with those expected. The return loss at the input of the cables and probe tips (S_{11} and S_{22}) are both fairly high corresponding to a good 50 Ω impedance match. The insertion loss is also reasonable based on values from the cable and probe data sheets.

Figure 4-25 shows S-parameters for the 2-4 GHz output isolator. The return loss($|S_{11}|, |S_{22}|$) of the input and output ports is better than 20 dB over the frequency

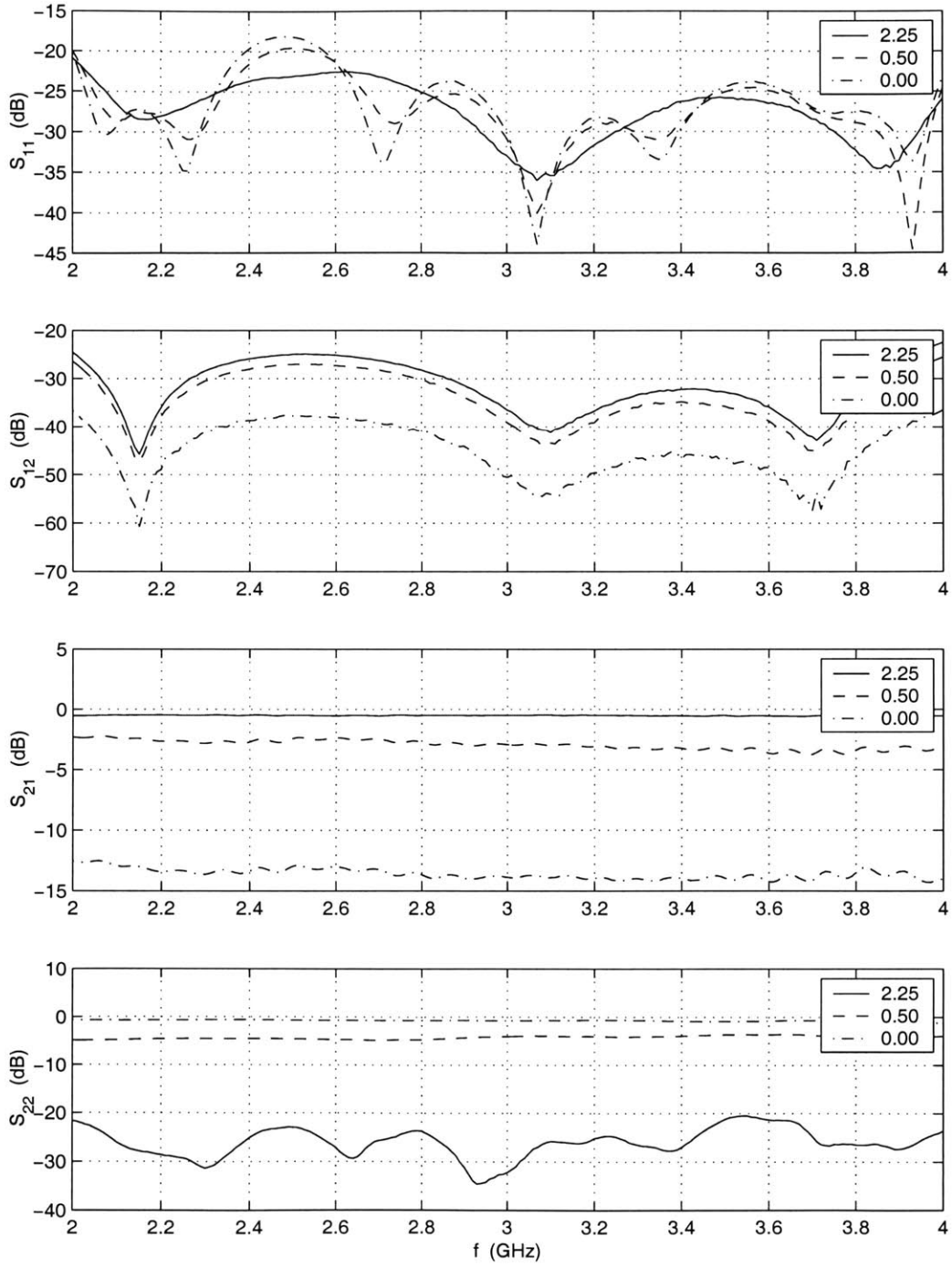

Figure 4-23: Tuner/Isolator S-parameters (2–4 GHz)

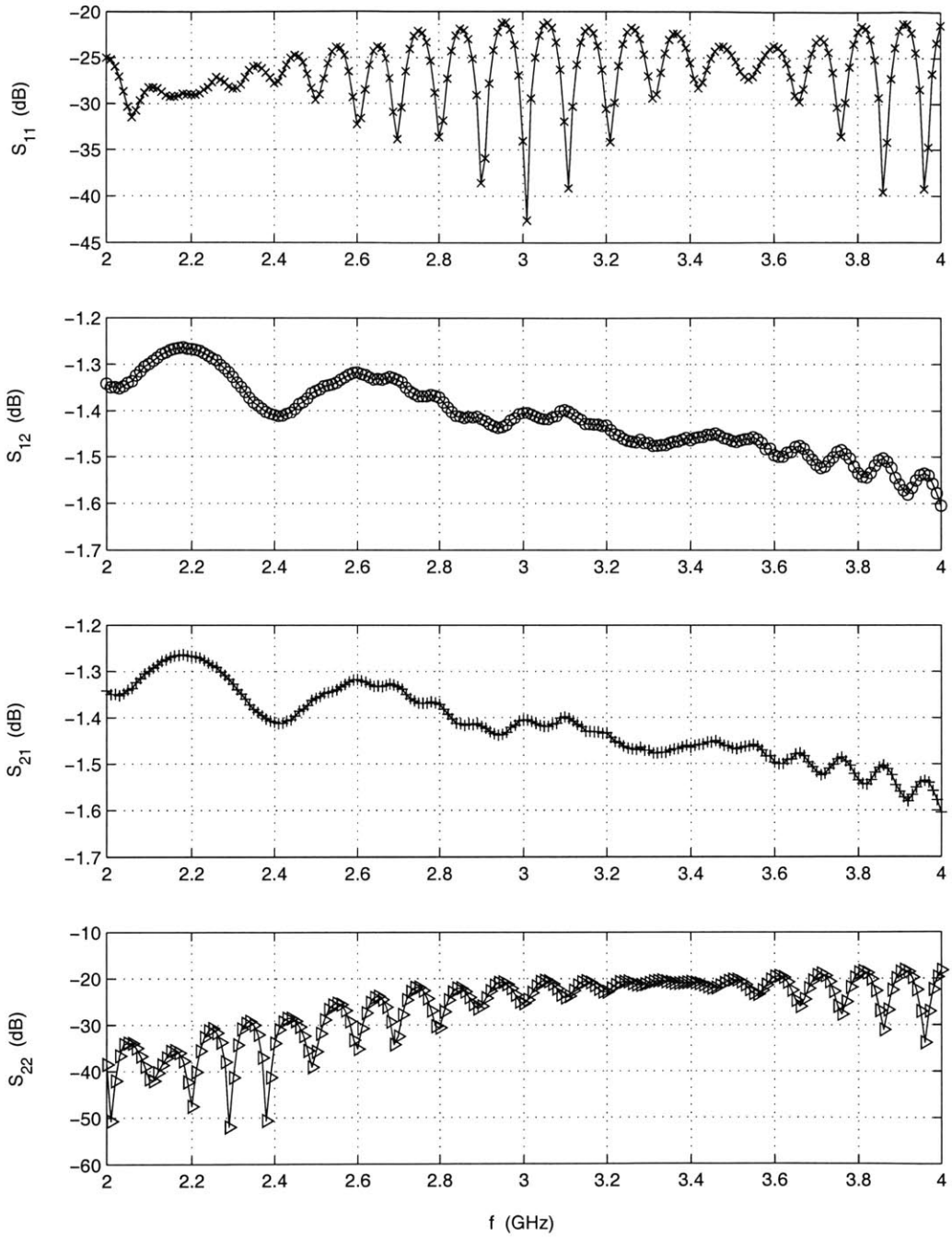

Figure 4-24: Bias-Tee/Cable/Probe S-parameters (2–4 GHz)

range, and reverse isolation($|S_{12}|$) is also better than 20 dB. The insertion loss($|S_{21}|$) is less than 0.25 dB over the frequency band.

4.3.2 Extracted Noise Figure Data

The noise de-embedding system has been verified using input data from simulation. The measurement setup was simulated using Agilent's EESOF simulator (libra). The use of simulation to generate data required for de-embedding scripts provided a situation where results were known *a priori* and conditions could be easily modified to be ideal. The following is a brief discussion of problems encountered to date.

While trying to simulate the noise figure of a simple Tee network attenuator(Figure 4-26),[7] it was noticed that the noise figure was not exactly equal to loss in the circuit. This turned out to be due to the default simulation temperature being 27 °C and not 16.85 °C, which corresponds to the standard noise temperature of $T_o = 290$ K[51],[52].[8] An often used rule of thumb in noise analysis is that the noise figure in decibels of an attenuator is equal to the amount of attenuation in decibels. This can be understood as follows. Noise figure is the measure of the degradation in the signal-to-noise through a device. For example, in a 6 dB attenuator, the signal power is decreased by 6 dB, but the noise power available from the output of the attenuator at $T = T_o = 290$ K is still $kT_o\,\Delta f$. Therefore, the signal-to-noise ratio is degraded by 6 dB, which is the noise factor. At temperatures other than 290 K, the noise power available at the output is higher, and the noise figure of the device is also higher. The difference in

[7] The resistor values R_1, R_2, and R_3 are determined from the amount of attenuation (A) and the input and output impedance requirements. For the case where $Z_{in1} = Z_{in2} = Z_o$, the attenuation is the magnitude of S_{21}, and the design equations are

$$R_1 = R_2 = Z_o\left(\frac{1-A}{1+A}\right)$$

$$R_3 = Z_o\left(\frac{2A}{1-A^2}\right)$$

[8] Quoting Dr. Friis, "...it makes little difference whether the noise figure be defined for a temperature of 290 degrees Kelvin or 300 degrees Kelvin. I chose the value 290 degrees merely because it makes the value of kT a little easier to handle in computations"

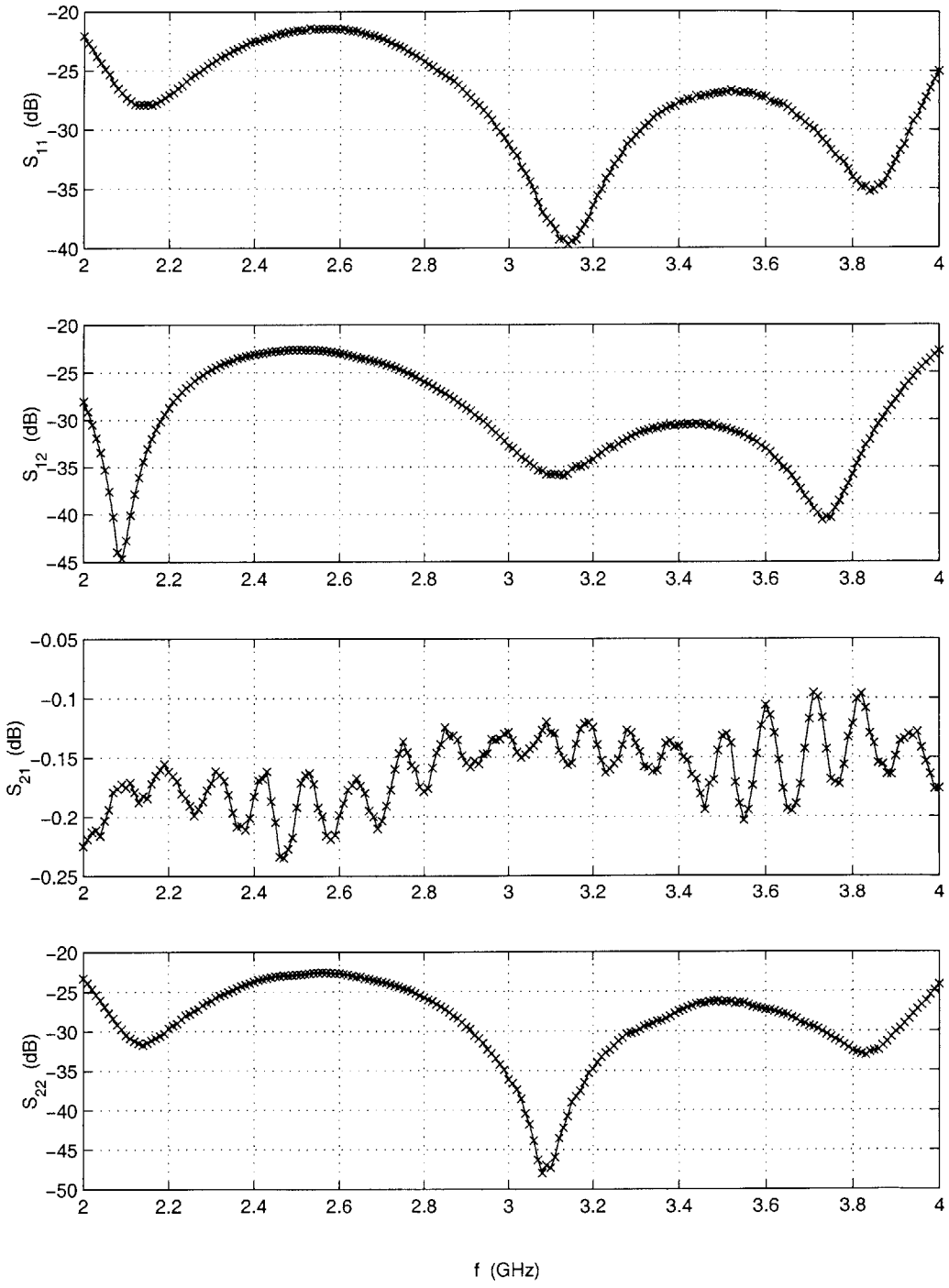

Figure 4-25: Output Isolator S-parameters (2–4 GHz)

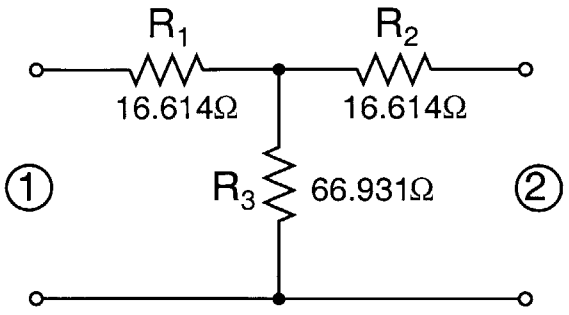

Figure 4-26: Tee-Network Attenuator

temperature can be corrected for using the following general expression for the noise factor of a passive device

$$F = \left(\frac{1}{G_A} - 1\right)\frac{T}{T_o} + 1 \tag{4.24}$$

where G_A is the available power gain of the device. For example, if the physical temperature of the attenuator is 300 K $\approx$ 27 °C, then the noise figure is 6.1315 dB rounding to four decimal places.[9]

Another important place that the reference temperature T_o appears is in the on-wafer probe structure de-embedding. To correctly account for the ambient temperature of the pads, the four noise parameters of the device with pads must be converted to a correlation matrix using T_o because the noise parameters are always defined with reference to T_o.

$$\mathbf{C_{A_{dut}}} = 2kT_o \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n|Y_{opt}|^2 \end{bmatrix} \tag{4.25}$$

The noise of the resistive parasitics in the pads must be calculated using the ambient temperature.

$$\mathbf{C_{Y_{open}}} = 2kT\mathfrak{Re}\{\mathbf{Y_{open}}\} \tag{4.26}$$

[9]Remember that a 6 dB attenuator is actually 6.0206 dB, which corresponds to a one-quarter attenuation in power.

Finally, the four noise parameters of the intrinsic device are determined with reference to T_o

$$R_n = \frac{\mathbf{C_{A_{11int}}}}{2kT_o} \tag{4.27a}$$

$$|Y_{opt}|^2 = \frac{\mathbf{C_{A_{22int}}}}{2kT_oR_n} \tag{4.27b}$$

$$B_{opt} = \frac{\mathbf{C_{A_{21int}}} - \mathbf{C_{A_{12int}}}}{-j4kT_oR_n} \tag{4.27c}$$

$$G_{opt} = \sqrt{|Y_{opt}|^2 - B_{opt}^2} \tag{4.27d}$$

$$F_{min} = 1 + 2\left(\frac{\mathbf{C_{A_{21int}}}}{2kT_o} + R_nY_{opt}\right) \tag{4.27e}$$

See Appendix A for the full de-embedding procedure.

Care must also be used in the implementation of short-open-load calculations for determining the cable and probe S-parameters. The calculation of $S_{21} = S_{12}$ requires a square-root operation. If the data used has a phase that varies from ($-\pi$ to $+\pi$), after the square-root is taken the phase varies from ($-\pi/2$ to $+\pi/2$).

$$(Ae^{j\phi})^{1/2} = \sqrt{A}e^{j\phi/2} \tag{4.28}$$

This does not yield the desired results if the resulting S_{21} is interpreted as a continuous function of frequency for interpolation purposes. The solution to this problem is perform the square-root operation as indicated in Equation 4.28, where the square-root is taken of the magnitude, and the phase of the result is one-half of the continuous phase. In Matlab, the `unwrap` function has been used to obtain the continuous phase of the variables.

At this time, no device noise figure data has been successfully extracted from measurements.

Chapter 5

Conclusions and Further Work

A graphical derivation of the intrinsic noise sources in a square-law MOSFET transistor that includes drain noise, gate noise and their correlation is presented. The insights gained in the process point to further work in modifying the theory for scaled devices where velocity saturation and mobility degradation are significant. Modeling of the device when the carriers are velocity saturated is also discussed. More work needs to be done in this area once measured data is available to compare with candidate theories.

The fundamentals of high frequency noise analysis using the noise figure approach were discussed, and some comparisons were made to the assumptions typically used in analog circuit design. Further study is required to determine the impact of the complete noise theory on broadband analog design.

Initial characterization data of 0.15 μm devices show the expected behavior for scaled CMOS transistors. One exception that requires further investigation is the apparent departure from the $1/I_D$ behavior of the output resistance for minimum length device. The deviation of g_{do} from g_m in saturation is also presented for a velocity saturation limited device.

Further study is required on the measurement and extraction of device noise sources. Presently, the methods outlined in this thesis correctly extract noise parameters from simulated data generated with idealized models. Successful application

to measured data has not been achieved. One possible cause is the series parasitic extraction procedure currently used. As discussed in Sections 4.2.3 and 4.2.4, the procedure used does not correctly account for effects of the drain-to-bulk capacitance and substrate resistance. A new approach needs to be adopted to obtain better estimates for the extrinsic parasitics which are critical to the ultimate accuracy of the noise de-embedding.

Another problem that has been encountered in the de-embedding of the test setup blocks A and C, is that the resulting noise figure is very small ($\sim 0.4\,\mathrm{dB}$), and when the pads and extrinsic component noise is removed the resulting noise figure is less than $0\,\mathrm{dB}$. This obviously impossible result points to an error in either the post-processing or the data itself.

After the successful acquisition of device noise data, the results need to be compared to proposed models for short channel MOSFET noise performance. Based on these comparisons, general trends in the noise behavior of scaled CMOS suitable for application to low noise design should be summarized. Finally, these results should be applied to a low noise design for verification and illustration of their applicability.

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Appendix A

De-embedding with Correlation Matrices

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{A.1}$$

$$\mathbf{S} \longrightarrow \mathbf{Y} \tag{A.2}$$

$$\mathbf{S_{open}} = \begin{bmatrix} S_{11o} & S_{12o} \\ S_{21o} & S_{22o} \end{bmatrix} \tag{A.3}$$

$$\mathbf{S_{open}} \longrightarrow \mathbf{Y_{open}} \tag{A.4}$$

$$\mathbf{C_{Y_{open}}} = 2kT\mathfrak{Re}\left\{\mathbf{Y_{open}}\right\} \tag{A.5}$$

$$\mathbf{S_{short}} = \begin{bmatrix} S_{11s} & S_{12s} \\ S_{21s} & S_{22s} \end{bmatrix} \tag{A.6}$$

$$\mathbf{S_{short}} \longrightarrow \mathbf{Y_{short}} \tag{A.7}$$

$$\mathbf{C_{Y_{short}}} = 2kT\mathfrak{Re}\{\mathbf{Y_{short}}\} \tag{A.8}$$

$$\mathbf{C_{A_{dut}}} = 2kT_o \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{rmin}-1}{2} - R_n Y_{opt} & R_n|Y_{opt}|^2 \end{bmatrix} \tag{A.9}$$

$$\mathbf{T_{AY}} = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix} \tag{A.10}$$

$$\mathbf{C_{Y_{dut}}} = \mathbf{T_{AY}} \times \mathbf{C_{A_{dut}}} \times \mathbf{T_{AY}}^{\dagger} \tag{A.11}$$

where $\mathbf{A}^{\dagger}$ is the conjugate transpose of matrix $\mathbf{A}$.

$$\mathbf{Y_x} = \mathbf{Y} - \mathbf{Y_{open}} \tag{A.12a}$$

$$\mathbf{C_{Y_x}} = \mathbf{C_{Y_{dut}}} - \mathbf{C_{Y_{open}}} \tag{A.12b}$$

$$\mathbf{Z_x} = \begin{bmatrix} \frac{Y_{22x}}{|\mathbf{Y_x}|} & \frac{-Y_{12x}}{|\mathbf{Y_x}|} \\ \frac{-Y_{21x}}{|\mathbf{Y_x}|} & \frac{Y_{11x}}{|\mathbf{Y_x}|} \end{bmatrix} \tag{A.13}$$

$$\mathbf{T_{YZ}} = \begin{bmatrix} Z_{11x} & Z_{12x} \\ Z_{21x} & Z_{22x} \end{bmatrix} \tag{A.14}$$

$$\mathbf{C_{Z_x}} = \mathbf{T_{YZ}} \times \mathbf{C_{Y_x}} \times \mathbf{T_{YZ}}^{\dagger} \tag{A.15}$$

$$\mathbf{Y_{short}} = \begin{bmatrix} \frac{Z_{22short}}{|\mathbf{Z_{short}}|} & \frac{-Z_{12short}}{|\mathbf{Z_{short}}|} \\ \frac{-Z_{21short}}{|\mathbf{Z_{short}}|} & \frac{Z_{11short}}{|\mathbf{Z_{short}}|} \end{bmatrix} \tag{A.16}$$

$$\mathbf{T_{ZY}} = \begin{bmatrix} Y_{11short} & Y_{12short} \\ Y_{21short} & Y_{22short} \end{bmatrix} \tag{A.17}$$

$$\mathbf{C_{Y_{short}}} = \mathbf{T_{ZY}} \times \mathbf{C_{Z_{short}}} \times \mathbf{T_{ZY}}^{\dagger} \tag{A.18}$$

$$\mathbf{Y_y} = \mathbf{Y_{short}} - \mathbf{Y_{open}} \tag{A.19a}$$

$$\mathbf{C_{Y_y}} = \mathbf{C_{Y_{short}}} - \mathbf{C_{Y_{open}}} \tag{A.19b}$$

$$\mathbf{Z_y} = \begin{bmatrix} \frac{Y_{22y}}{|\mathbf{Y_y}|} & \frac{-Y_{12y}}{|\mathbf{Y_y}|} \\ \frac{-Y_{21y}}{|\mathbf{Y_y}|} & \frac{Y_{11y}}{|\mathbf{Y_y}|} \end{bmatrix} \tag{A.20}$$

$$\mathbf{T_{YZ}} = \begin{bmatrix} Z_{11y} & Z_{12y} \\ Z_{21y} & Z_{22y} \end{bmatrix} \tag{A.21}$$

$$\mathbf{C_{Z_y}} = \mathbf{T_{YZ}} \times \mathbf{C_{Y_y}} \times \mathbf{T_{YZ}}^{\dagger} \tag{A.22}$$

$$\mathbf{Z_{ext}} = \mathbf{Z_x} - \mathbf{Z_y} \tag{A.23a}$$

$$\mathbf{C_{Z_{ext}}} = \mathbf{C_{Z_x}} - \mathbf{C_{Z_y}} \tag{A.23b}$$

$$\mathbf{Z}_\sigma = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \tag{A.24}$$

$$\mathbf{C_{Z_\sigma}} = 2kT\mathfrak{Re}\left\{\mathbf{Z}_\sigma\right\} \tag{A.25}$$

$$\mathbf{Z_{int}} = \mathbf{Z_{ext}} - \mathbf{Z}_{\sigma} \tag{A.26a}$$

$$\mathbf{C_{Z_{int}}} = \mathbf{C_{Z_{ext}}} - \mathbf{C_{Z_{\sigma}}} \tag{A.26b}$$

$$\mathbf{Y_{int}} = \begin{bmatrix} \dfrac{Z_{22int}}{|\mathbf{Z_{int}}|} & \dfrac{-Z_{12int}}{|\mathbf{Z_{int}}|} \\ \dfrac{-Z_{21int}}{|\mathbf{Z_{int}}|} & \dfrac{Z_{11int}}{|\mathbf{Z_{int}}|} \end{bmatrix} \tag{A.27}$$

$$\mathbf{T_{ZY}} = \begin{bmatrix} Y_{11int} & Y_{12int} \\ Y_{21int} & Y_{22int} \end{bmatrix} \tag{A.28}$$

$$\mathbf{C_{Y_{int}}} = \mathbf{T_{ZY}} \times \mathbf{C_{Z_{int}}} \times \mathbf{T_{ZY}}^{\dagger} \tag{A.29}$$

$$\mathbf{Z_{int}} \longrightarrow \mathbf{A_{int}} \tag{A.30}$$

$$\mathbf{T_{ZA}} = \begin{bmatrix} 1 & -\mathbf{A_{11int}} \\ 0 & -\mathbf{A_{21int}} \end{bmatrix} \tag{A.31}$$

$$\mathbf{C_{A_{int}}} = \mathbf{T_{ZA}} \times \mathbf{C_{Z_{int}}} \times \mathbf{T_{ZA}}^{\dagger} \tag{A.32}$$

$$R_n = \frac{\mathbf{C_{A_{11int}}}}{2kT_o} \tag{A.33a}$$

$$|Y_{opt}|^2 = \frac{\mathbf{C_{A_{22int}}}}{2kT_oR_n} \tag{A.33b}$$

$$B_{opt} = \frac{\mathbf{C_{A_{21int}}} - \mathbf{C_{A_{12int}}}}{-j4kT_oR_n} \tag{A.33c}$$

$$G_{opt} = \sqrt{|Y_{opt}|^2 - B_{opt}^2} \tag{A.33d}$$

$$F_{min} = 1 + 2\left(\frac{\mathbf{C_{A_{21int}}}}{2kT_o} + R_nY_{opt}\right) \tag{A.33e}$$

$$NF_{min} = 10\log_{10}(F_{min}) \tag{A.34}$$

$$\Gamma_{opt} = \frac{1 - \dfrac{Y_{opt}}{Y_o}}{1 + \dfrac{Y_{opt}}{Y_o}} \tag{A.35}$$

$$\overline{i_d^2} = 2\,\mathbf{C_{Y_{22int}}} \tag{A.36a}$$

$$\overline{i_g^2} = 2\,\mathbf{C_{Y_{11int}}} \tag{A.36b}$$

$$c_{int} = \frac{\mathbf{C_{Y_{12int}}}}{\sqrt{\mathbf{C_{Y_{11int}}} \cdot \mathbf{C_{Y_{22int}}}}} \tag{A.36c}$$

$$\overline{v_n^2} = 2\,\mathbf{C_{A_{11int}}} \tag{A.37a}$$

$$\overline{i_n^2} = 2\,\mathbf{C_{A_{22int}}} \tag{A.37b}$$

$$\overline{v_n i_n^*} = 2\,\mathbf{C_{A_{12int}}} \tag{A.37c}$$

$$c_A = \frac{\mathbf{C_{A_{12int}}}}{\sqrt{\mathbf{C_{A_{11int}}} \cdot \mathbf{C_{A_{22int}}}}} \tag{A.37d}$$

Appendix B

Transconductance versus Drain Current

This appendix gives mathematical justification of the claim that the slope information of a graph of $\log(g_m)$ versus $\log(I_D)$ is identical to that of a graph of $\log(g_{mo})$ versus $\log(I_{Do})$.

If

$$I_D = I_{Do}\left(1 + \frac{V_{DS}}{V_A}\right) \tag{B.1}$$

then to the extent that

$$\frac{\partial V_A}{\partial V_{GS}} = 0 \tag{B.2}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{B.3a}$$

$$= \frac{\partial I_{Do}}{\partial V_{GS}}\left(1 + \frac{V_{DS}}{V_A}\right) \tag{B.3b}$$

$$= g_{mo}\left(1 + \frac{V_{DS}}{V_A}\right) \tag{B.3c}$$

Therefore,

$$I_D = I_{Do}\, A \tag{B.4}$$

$$g_m = g_{mo}\, A \tag{B.5}$$

where

$$A = 1 + \frac{V_{DS}}{V_A} \tag{B.6}$$

However, it is $\log(g_m)$ and $\log(I_D)$ that are of interest

$$\log I_D = \log I_{Do} + \log A \tag{B.7}$$

$$\log g_m = \log g_{mo} + \log A \tag{B.8}$$

In order to show that the slope information is identical, some functional dependence between g_{mo} and I_{Do} must be assumed. Because the slope of a curve at a point can be used to estimate the curve in the region of that point,[1] the curve on log-log graph paper can be estimated with its slope or on linear graph paper its exponent.

$$g_{mo} = I_{Do}^n \tag{B.9}$$

$$\log g_{mo} = n \log I_{Do} \tag{B.10}$$

Substituting this expression for $\log(g_{mo})$ into (B.8), results in

$$\log g_m = n \log I_{Do} + \log A \tag{B.11}$$

Solving (B.7) for $\log(I_{Do})$, and substituting into (B.11)

$$\log g_m = n \log I_D + (\log A - n \log A) \tag{B.12}$$

[1] In other words, a first order Taylor expansion.

which shows that the plot of $\log(g_m)$ versus $\log(I_D)$ preserves the slope information of $\log(g_{mo})$ versus $\log(I_{Do})$.

Unfortunately, the assumption (B.2) that V_A is independent of V_{GS} is not true (Figure 4-8). As mentioned in Chapter 4, further investigation of the dependence of V_A on V_{GS} is required.