Investigation of Mechanisms and Influencing Processing Factors on Mobility Enhancement in Strained Si *n*-MOSFETs

by

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ABSTRACT

As CMOS technology scales, strained Si technology has received more attention for its enhanced performance due to higher carrier mobility. Two different aspects of mobility enhancement in strained Si *n*-MOSFETs are explored in this work. The first study investigates the impact of strain on the various mobility limiting mechanisms. We report temperature dependent measurements and modeling of the effective electron mobility in surface channel, strained Si *n*-MOSFETs. Mobility measurements were taken from 30 K to 300 K. A three-term model was used to fit the data and extract the various mobility terms. Surface-roughness limited mobility of strained Si *n*-MOSFETs is shown to be enhanced by the introduction of strain and have the same effective field dependence as that of unstrained Si *n*-MOSFETs. The results suggest that surface-specific mechanisms may be involved in the strain-induced electron mobility enhancement, which persists to high vertical effective field. The second part of this work investigates influencing processing factors on electron mobility enhancement, particularly the impact of ion implantation damage and thermal budget. Long channel MOSFETs were fabricated on both CZ Si wafers and strained Si/relaxed $Si_{0.8}Ge_{0.2}$ heterostructures. Si and Ge were implanted into the channel in six different doses ranging from 4×10^{12} to 1×10^{15} atoms/cm^2. Three different rapid thermal anneals (RTA) were used. It is shown that the mobility enhancement factor is degraded by ion implantation and RTA. For each RTA condition, there is a threshold implantation dose, above which the strained Si mobility starts to degrade significantly. The threshold dose is smaller for devices with higher thermal budget. The degradation is larger for devices with higher implantation doses or larger thermal budget. Two mechanisms are involved in the mobility degradation introduced by ion implantation and thermal processing: strain relaxation due to misfit dislocations and residual ion implantation damage in the strained Si channel.

Thesis Supervisor: Judy L. Hoyt

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CHAPTER 1 Introduction

Semiconductor devices have been the basis for the electronics industry for a few decades. Among various semiconductor devices, silicon complementary metal oxide semiconductor field effect transistor (Si CMOSFET) is the most important. Behind the advancement of many electronic products, such as computer, cell phone etc, is the continued scaling and the performance improvement of Si CMOS. However, physical limitations and processing difficulties are making scaling more difficult as Si CMOS is scaled to the deep submicron regime. Many efforts have been made to overcome short channel effects and extract more performance from scaled CMOS, such as using high-k gate dielectric materials, double-gate design, vertical structure, silicon-on-insulator (SOI). Another option to enhance the performance of CMOS is to use strained Si technology. Tensile strain in the Si channel has been shown to enhance electron and hole mobility by 1.8X [1, 2].

1.1 Strained Si technology

1.1.1 Epitaxial structure and mobility enhancement

Several structures exist for strained Si MOSFETs, such as buried-channel MOSFETs, surface strained MOSFETs and SiGe-on-insulator (SGOI). All of them are based on the epitaxial (epi) growth of $Si_{1-x}Ge_x$ and strained Si. A relaxed

$Si_{1-x}Ge_x$ layer is used as the virtual substrate of the strained Si channel. The lattice constant of pure Ge is larger than that of Si by 4%. Thus, the $Si_{1-x}Ge_x$ virtual substrate has a larger lattice constant than the equilibrium lattice constant of Si. When a thin Si layer is epitaxially grown on a relaxed $Si_{1-x}Ge_x$ layer, the lattice of Si accommodates the larger lattice of the $Si_{1-x}Ge_x$ below. Therefore, tensile stain is introduced into the Si channel. Figure 1-1 shows the epitaxial heterostructure of strained Si on a relaxed $Si_{1-x}Ge_x$ substrate.

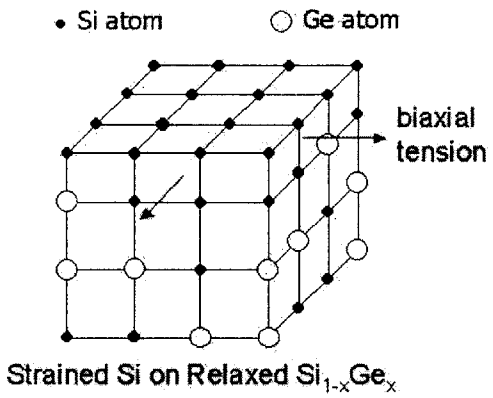


Figure 1-1 The epitaxial heterostructure of strained Si on a relaxed $Si_{1-x}Ge_x$ substrate.

Figure 1-2 shows the structure of a long channel surface strained Si *n*-MOSFET. A relaxed $Si_{0.8}Ge_{0.2}$ layer was epitaxially grown on a graded relaxed $Si_{1-x}Ge_x$ buffer layer in a UHCVD reactor. The strained Si layer was epitaxially grown on the relaxed $Si_{0.8}Ge_{0.2}$ layer. The graded $Si_{1-x}Ge_x$ buffer layer was formed by increasing the Ge content from 0% to 20% over a thickness of 2 μm. The graded buffer layer is used to reduce the threading dislocation density level in the relaxed $Si_{0.8}Ge_{0.2}$ cap and the strained Si channel. Utilizing the graded buffer technology, the threading

dislocation density in the relaxed $Si_{0.8}Ge_{0.2}$ cap can be reduced to 10^5 cm^{-2}, which is sufficient for the operation of Si MOSFET [3]. Without the buffer layer, the relaxed $Si_{10.8}Ge_{0.2}$ cap would have a very high threading dislocation density on the order of 10^9~10^{10} cm^{-2}.

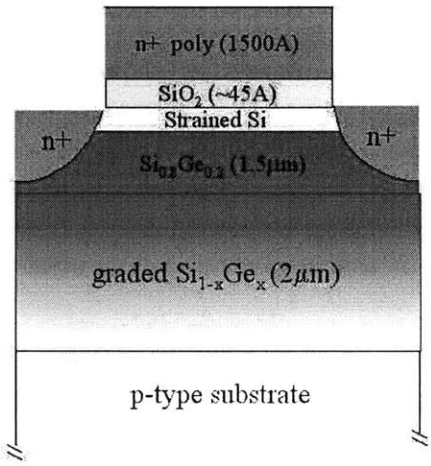


Figure 1-2 The structure of a long channel surface strained Si *n*-MOSFET.

The main advantage of strained Si MOSFETs is the enhancement in the carrier mobility and thus the current drive over unstrained Si MOSFETs. J. Welser first reported the 1.8X electron mobility enhancement in strained Si *n*-MOSFETs [1]. K. Rim *et al.* reported a 1.8X enhancement in hole mobility in strained Si *p*-MOSFETs on $Si_{0.71}Ge_{0.29}$ substrates over those on $Si_{0.90}Ge_{0.10}$ substrates [2]. A 75% enhancement in electron mobility over the universal mobility of unstrained Si *n*-MOSFETs and an increased transconductance were seen in deep submicron in strained Si *n*-MOSFETs [4]. Several research groups have obtained similar enhancement factors for electron mobility. Figure 1-3 shows the electron mobility of a strained Si MOSFET fabricated by K. Rim *et al* and the universal mobility of an

unstrained Si MOSFET by Takagi *et al.* at room temperature and 77 K [4,5]. Electron mobility is enhanced over the temperature range of 77 K to 300 K.

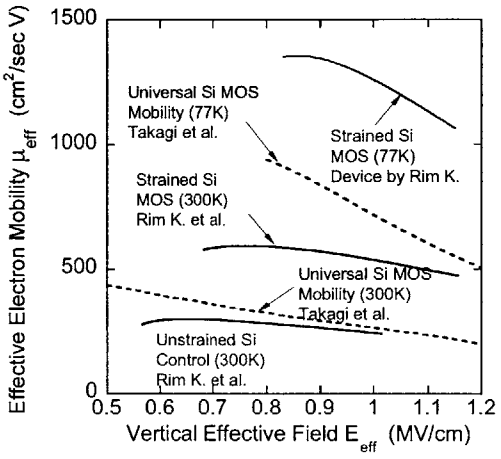


Figure 1-3 Effective electron mobility of unstrained Si MOSFETs in ref [5] (dashed lines) and strained Si MOSFETs in ref [4] (solid lines) at 300 K and 77 K.

Figure 1-4 and 1-5 show the mobility enhancement factors vs. Ge fraction for electrons and holes measured by different research groups [6]. At room temperature and for this E_{eff} range, the MOS electron mobility is dominated by phonon scattering. Peak electron mobility enhancements measured in uniformly doped devices saturate near a mobility enhancement factor of 1.8 for strained Si with a substrate Ge content above 20%. This agrees with calculations of the impact of strain on the phonon-limited MOS electron mobility [7]. While strained Si *n*-MOSFETs display electron mobility enhancements over a wide E_{eff} range, the hole mobility in *p*-MOSFETs with strained Si surface channels is improved primarily at low E_{eff} (< 1 MV/cm). The enhancement ratio *r* approaches 1 at E_{eff} ~ 1 MV/cm for *p*-MOSFETs with substrate Ge fractions below 30%.

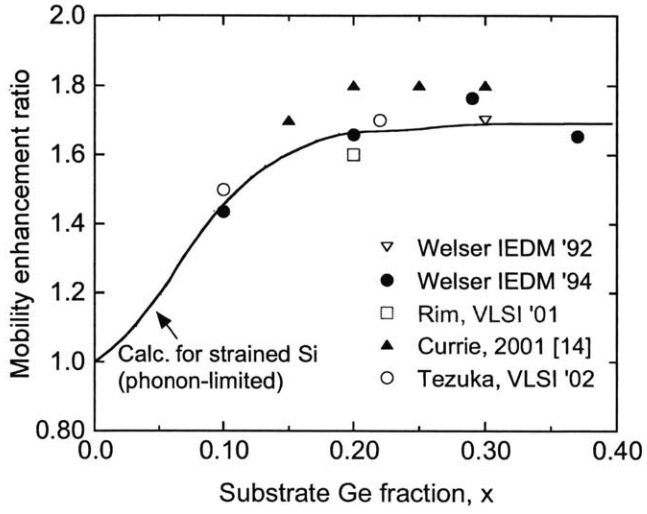


Figure 1-4 Measured (symbols) effective mobility enhancement ratios compared to calculations for the phonon-limited MOS mobility (solid line) for strained Si *n*-MOSFETs. From [6].

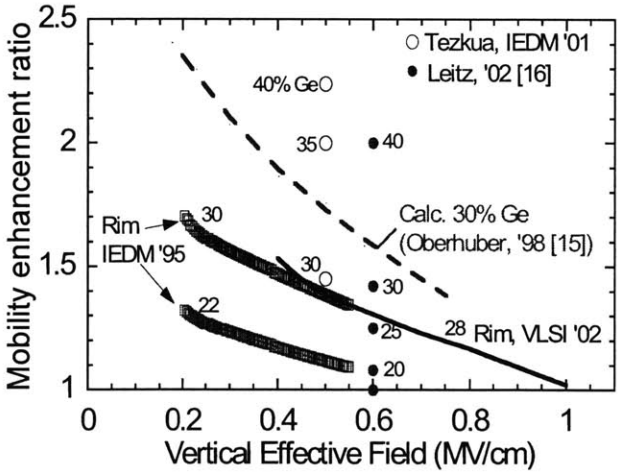


Figure 1-5 Comparison of hole mobility enhancement ratios in strained Si *p*-MOSFETs as a function of vertical effective field, E_{eff}. Unlike electron mobility, hole mobility enhancement is reduced for higher E_{eff}. From [6].

Theoretical study shows that biaxial tensile strain in the Si layers grown on relaxed $Si_{1-x}Ge_x$ splits the 6-fold degeneracy in the Si conduction band [8, 9] as shown in Figure 1-6. The 2-fold degenerate valleys with smaller in-plane mass Δ_2 are preferentially populated. Intervalley phonon scattering and the effective mass of electrons are reduced, which improves the electron mobility at low and intermediate E_{eff}. At high E_{eff}, however, there are controversies about why the electron mobility is enhanced by strain, since the electron confinement by the inversion-potential at the SiO_2-Si interface lifts the 6-fold degeneracy by an amount similar in magnitude the strain effect [10].

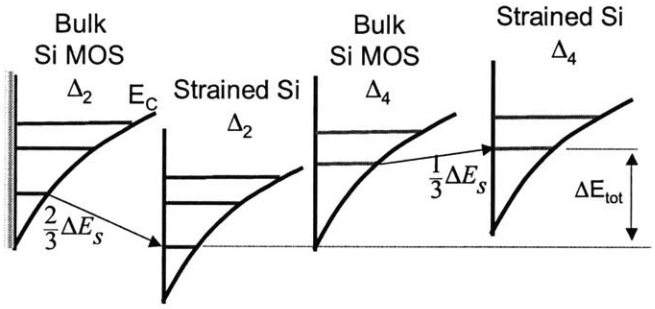


Figure 1-6 Conduction band energy splitting in strained Si.

1.1.2 State-of-the-art strained Si technology

Strained Si technology has been developing rapidly in the past few years. In terms of channel length, K. Rim *et al.* at IBM have fabricated and measured strained Si *n*-MOSFETs and *p*-MOSFETs down to effective channel lengths of about 40 nm and 90 nm respectively [11,12]. In terms of structure, strained Si technology has been combined with SOI technology resulting in SiGe-on-insulator (SGOI) [13,14].

1.2 Direction and Organization of Thesis

As mentioned earlier, the main advantage of strained Si technology is the enhanced performance due to higher carrier mobility. Therefore, it is important to understand the mechanisms of mobility enhancement and to obtain an accurate mobility model. From a practical point of view, there are still many problems to solve in the processing of strained Si.

This thesis focuses on two aspects of strained Si technology. The first study investigates the impact of strain on the various mobility-limiting mechanisms and is discussed in Chapter 2. The second part focuses on the impact of processing on the performance of strained Si n-MOSFETs, in which two major processing steps: ion implantation and thermal processing are investigated for their influence on mobility enhancement. This work is discussed in Chapter 3. Chapter 4 provides a summary and suggestions for future work.

CHAPTER 2 Temperature Dependent Mobility Characterization and Modeling of Strained Si *n*-MOSFETs

Although enhanced carrier transport has been reported in strained Si CMOS for more than a decade, the mechanisms of this enhancement are still not fully understood. This chapter focuses on the impact of strain on three mobility-limiting mechanisms, and investigates the impact of strain on the phonon-limited and surface-roughness-limited mobility. Section 2.1 provides an introduction to carrier transport. Subsection 2.1.1 introduces the concepts of effective mobility and universal mobility, which are the common language used in the study of carrier transport. Subsection 2.1.2 explains the three scattering mechanisms in the Si channel. Section 2.2 describes the experiment. Section 2.3 presents the modeling study and Section 2.4 provides a discussion of the results.

2.1 Introduction to Carrier Transport in Strained Si MOSFET

2.1.1 Effective mobility and the Universal Mobility

Mobility, μ, is a widely used term to characterize carrier transport at low lateral electric fields. For a MOSFET operating in strong inversion in the linear regime and

low lateral field ($V_{DS} << V_{GS}-V_T$), the drain current can be approximately expressed by

$$I_D \approx \mu C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_T)V_{DS} \qquad \text{Eq. 2-1}$$

where C_{ox} is the gate oxide capacitance, W and L are the width and length of the MOSFET respectively, V_T is the threshold voltage, and μ is the in-plane carrier mobility. To extract the low-field mobility term, a low drain voltage (<100 mV) is used to avoid any high lateral-field effects, such as velocity saturation. The effective mobility, μ_{eff}, is found by taking the partial derivative of Eq. 2-1 with respect to the drain voltage:

$$g_D \approx \mu C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_T)+\frac{I_D}{\mu}\left(\frac{d\mu}{dV_{DS}}\right)$$

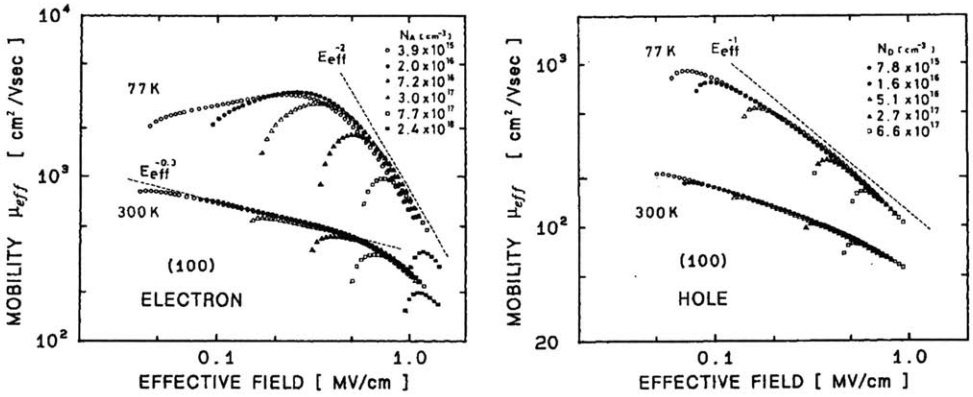
$$\mu_{eff} = \left(\frac{L}{W}\right)\frac{g_d}{Q_{inv}} \qquad \text{Eq.2-2}$$

This definition assumes that $(d\mu/dV_{DS}) \approx 0$, which has been experimentally verified for low drain voltages.

The effective mobility μ_{eff} is often used when comparing the mobility between different devices. When the effective mobility is plotted against the vertical effective field (E_{eff}), different mobility curves converge to the universal mobility curve independent of doping or substrate bias, as shown in Figure 2-1. The vertical effective field is usually defined by

$$E_{eff} = \left(\frac{1}{\varepsilon_{si}}\right)\left(aQ_{depl} + bQ_{inv}\right) \qquad \text{Eq.2-3}$$

where a and b are the weighting factors that are generally obtained empirically. The factor a is usually taken as unity. For electron and hole transport, b is empirically taken as 1/2 and 1/3 respectively to obtain the universal mobility curve [15,16]. Q_{depl} is the integrated space charge in the depletion region under the channel, and Q_{inv} is the concentration of inversion carriers. Q_{inv} is typically obtained by integrating the gate-to-channel capacitance C_{GC} from split CV measurements [17,18].



(a) Electron Mobility (b) Hole Mobility

Figure 2-1 The inversion layer mobility μ_{eff} of (a) electrons and (b) holes for an unstrained Si MOSFET at 300 K and 77 K vs. effective field E_{eff}. From S. Takagi *et al.* [5]

The inversion layer mobility μ_{eff} for unstrained Si MOSFETs follows a universal behavior as seen in Figure 2-1. Similarly, the universal behavior of μ_{eff} in strained Si n-MOSFETs has been demonstrated by experiments and simulation [19,20].

2.1.2 Scattering Mechanisms

Carrier transport in the inversion layer of a MOSFET is different from that in bulk Si. The carriers in the inversion layer are subject to scattering from the oxide interface in the presence of a vertical effective field (E_{eff}). In addition, fixed charge

and interface traps at the oxide interface, and ionized impurities in the channel contribute additional Coulomb scattering centers. In summary, there are three primary scattering mechanisms that limit the mobility of carriers in the inversion layer of a MOSFET: Coulomb scattering, phonon scattering and surface roughness scattering. The three scattering mechanisms correspond to three mobility terms: Coulomb limited mobility μ_C, phonon limited mobility μ_{ph}, and surface roughness limited mobility μ_{sr}. The total effective electron mobility μ_{eff} can be expressed as the Mathiessen's sum of the mobilites limited by the various scattering mechanisms:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \qquad \text{Eq.2-4}$$

Returning to Figure 2-1, although the mobility curves for different doping levels start at different values due Coulomb scattering, they converge as the Coulomb limited mobility increases with increasing inversion layer charge. When μ_C increases, it has less influence on the total mobility. The other two terms, μ_{sr} and μ_{ph} are independent of doping. Thus, curves with different doping converge to a universal mobility curve.

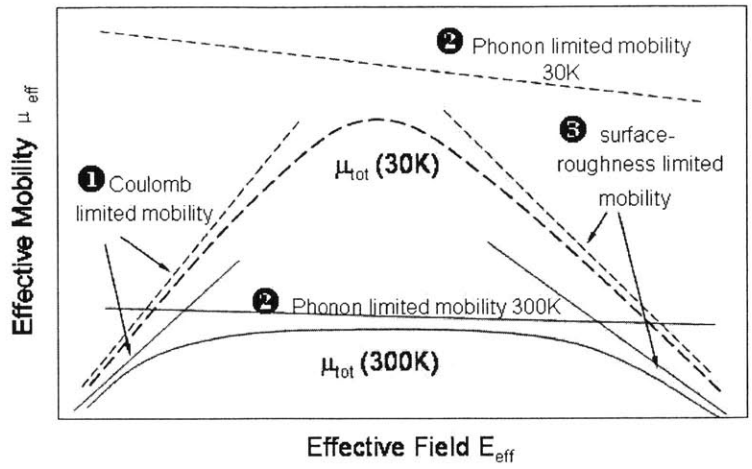


Figure 2-2 Schematic diagram of the total mobility, 3 mobility terms, and their temperature and field dependence. After Takagi, *et al.*[5]

According to Mathiessen's rule and the relative magnitude of the three mobility terms, the total mobility at room temperature is usually a mixture of all three terms. From Eq. 2-4, it can be seen that at a given vertical effective field E_{eff}, the smallest term has the most influence on the total mobility. The Coulomb-limited, phonon-limited, and surface-roughness limited mobility terms dominate at low vertical fields, intermediate fields, and high vertical fields at room temperature respectively (Figure 2-2). As temperature decreases, some of the mobility terms increase, resulting in a higher total mobility. However, the temperature dependence of each term is different. Figure 2-2 schematically illustrates the three mobility terms at 30 K and 300 K. At low temperature i.e. 30 K, μ_{ph} increases much more rapidly than the other two terms, so that μ_{ph} has little influence at 30 K. At this temperature, the μ_C and μ_{sr} terms dominate. Therefore, in order to study the impact of strain on these three terms, temperature dependent measurements and modeling are used here to separate the various terms.

2.2 Temperature Dependent Mobility Characterization

2.2.1 Devices Measured in This Work

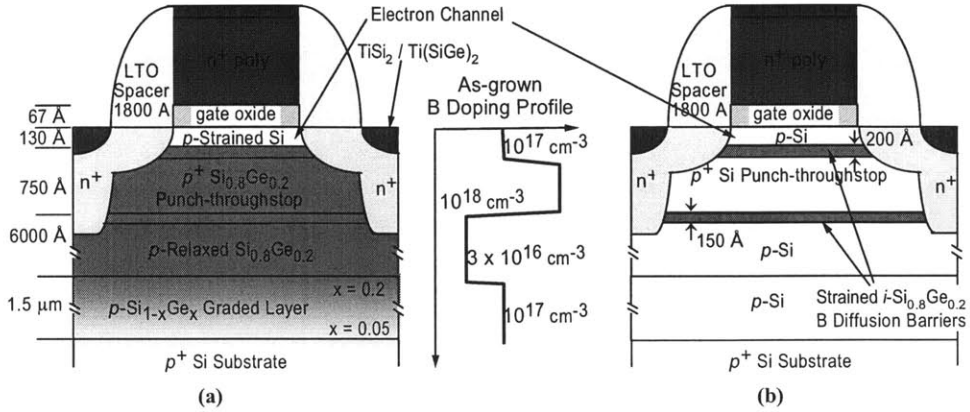


Figure 2-3 Device structure for strained Si *n*-MOSFETs used in this work, from [4]. (a) strained Si, (b) epi Si control devices. From Ref. [4].

Strained Si *n*-MOSFETs measured in this work were previously fabricated by K. Rim, *et al.* at Stanford University as described in [4]. Figure 2-3 is a cross section of the strained Si and epi Si control MOSFETs used in this work. In the epi control devices, two thin layers of strained SiGe (Figure 2-3 b) were inserted above and below the doping peak to serve as boron diffusion barriers so that the doping profiles match those of strained Si devices. Electron transport takes place in a thin strained Si layer under the gate oxide. 60 Å-thick gate oxides were grown by thermal oxidation in O_2 at 800°C. Strained and unstrained Si control devices were fabricated with similar doping profiles, obtained by *in-situ* boron doping during epitaxial layer growth. The retrograde boron doping varies from 3 x 10^{17} cm^{-3} at the surface, to 8 x 10^{17} cm^{-3} at the maximum depletion depth, which is shown in the SIMS profile in Figure 2-4.

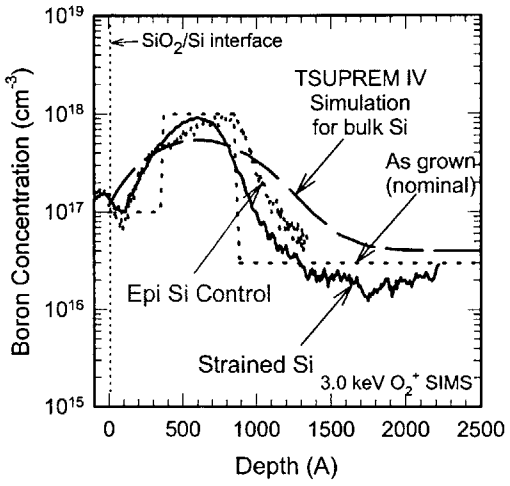


Figure 2-4 Comparison of boron profiles measured by SIMS after processing, and TSUPREM IV-simulated profile. Due to the low thermal budget and presence of the $Si_{0.8}Ge_{0.2}$ diffusion barriers, boron profiles are well matched for the two structures, and doping profile broadening is reduced. From Rim [4].

2.2.2 Mobility Measurement

In order to investigate the mobility behavior of strained Si *n*-MOSFETs, the effective electron mobility μ_{eff} as a function of effective vertical field E_{eff} was extracted in this work using 40 x 40 μm^2 devices according to equations 2-2 and 2-3:

$$\mu_{eff} = \left(\frac{L}{W}\right)\frac{g_d}{Q_{inv}}$$

$$E_{eff} = \left(\frac{1}{\varepsilon_{Si}}\right)\left(aQ_{depl} + bQ_{inv}\right)$$

The effective mobility μ_{eff} is proportional to drain conductance g_d. Ideally, g_d should be measured at zero V_{DS}, which is not practical in the measurement. Therefore, g_d at V_{DS} = 0 V was obtained by measuring I_d at V_{DS} = –20, –10, 10, and 20 mV and interpolating to 0 V. The split C-V method was used to obtain the inversion charge density Q_{inv} and maximum depletion depth, X_{dmax} (Figure 2-5). Gate-to-body

capacitance and gate-to-channel capacitance are denoted as C_{gb} and C_{gc} respectively. The depletion charge Q_{depl} was obtained by integrating the SIMS data (Figure 2-4) over the depletion region. The inversion charge density Q_{inv} was obtained from the integral of the gate-to-channel capacitance C_{gc} over gate voltage V_{GS}.

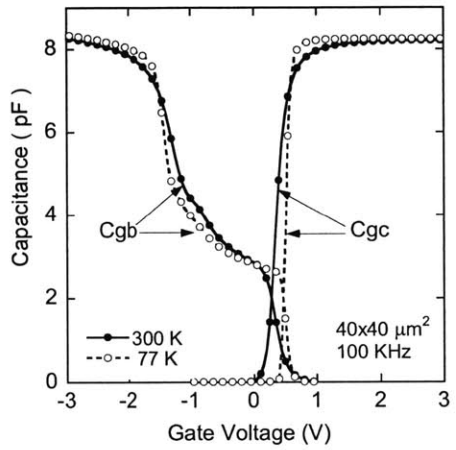


Figure 2-5 Split C-V measurements obtained in this work for strained 40 x 40μm² *n*-MOSFETs at 300 K (closed symbols) and 77 K (open symbols).

In order to further investigate the temperature dependence of the mobility terms, measurements were performed at 8 temperatures: 30, 77, 100, 125, 150, 200, 250 and 300 K (Figure 2-6). At 125 K, the devices were taken to a higher gate bias. It is seen in Figure 6 that the total mobility μ_{eff} increases with decreasing temperature. The slope of μ_{eff} vs. E_{eff} becomes steeper at lower temperatures and higher fields, as the surface roughness mobility term begins to dominate. The extracted mobility enhancement factor for strained Si vs. unstrained Si, at E_{eff}=1 MV/cm, is about 2X at room temperature.

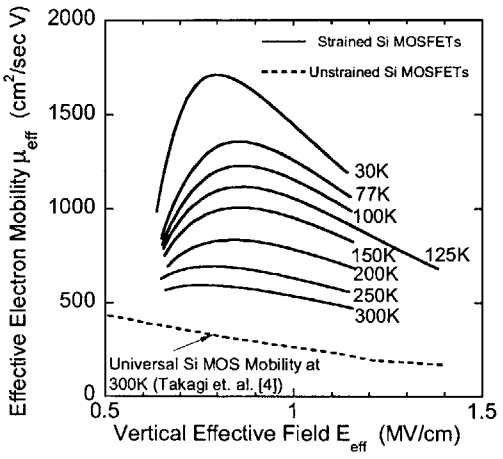


Figure 2-6 Temperature dependent measurements of the effective electron mobility for strained Si *n*-MOSFETs. At 125 K the device was taken to higher gate bias. Universal Si MOS mobility at 300 K from [5] is shown for reference.

2.3 The Mobility Modeling and Results

2.3.1 The Three-term Model

A three-term model was used to extract the various mobility terms from the temperature dependent mobility data by least-squares analysis.

$$\mu_{ph} = A \cdot E_{eff}^{\ m} \cdot T^n \qquad \text{Eq. 2-5}$$

$$\mu_{sr} = B \cdot E_{eff}^{\ r} \cdot \exp\left(-\left(\frac{T}{T_0}\right)^2\right) \qquad \text{Eq. 2-6}$$

$$\mu_C = C \cdot Q_{inv}^{\ l} T^s \qquad \text{Eq. 2-7}$$

Equation 2-5 [5], 6 [5, 21], and 7 show the dependence of each term on temperature T and vertical effective field E_{eff}. A, B, and C are coefficients while m and r give the μ_{eff} dependence on E_{eff}. $Q_{inv}^{\ l}$ accounts for the screening effect of the inversion layer charge density on the Coulomb scattering term.

Previous modeling work on surface roughness mobility of unstrained Si MOSFETs has suggested different temperature dependences of μ_{sr}. Takagi *et al.* took this term as temperature-independent [5], while Mazzoni *et al.* gave a linearly temperature dependent analytical formula for μ_{sr} [21]. In the three-term model used here, T_0 is a fitting parameter that counts for the temperature dependence of μ_{sr}, which turns out to be infinity. Therefore, μ_{sr} of strained Si MOSFETs has no temperature dependence.

Of the nine parameters in the model, r determines the E_{eff} dependence of the surface roughness limited mobility, and is of most interest. This is for two reasons. First, μ_{sr} plays a key role at high fields where modern devices operate. Second, at low temperatures, μ_{ph} has little influence on the total mobility, which enables us to get a fairly accurate estimation of μ_{sr}. In this work, we did not focus on μ_c, since μ_c depends on doping level, oxide quality, etc., which is not a "universal" term. The Coulomb limited mobility increases as the concentration of ionized impurities (i.e. the doping level) decreases. For example, the unstrained Si mobility used here is extracted from the devices with a doping level of 3.9×10^{15} cm^{-3}, while the strained Si mobility is extracted from the devices with a surface doping of about $3\sim8 \times 10^{17}$ cm^{-3}. Therefore, the Coulomb limited mobility of the unstrained Si extracted in this work is much higher than that of the strained Si as seen in the modeling results below.

2.3.2 Fitting the Unstrained Si Mobility with the Three-term Model

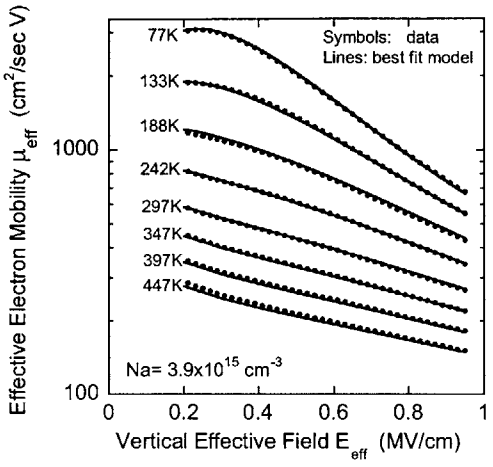


Figure 2-7 Comparison of published mobility data for unstrained Si *n*-MOSFETs at different temperatures (symbols) [5] with the fitted model in this work (lines).

First, the form of the model was verified by fitting published Si MOS temperature dependent mobility data [5] by least-squares analysis. The low temperature mobility measurements of the unstrained control devices fabricated by K. Rim were not successful due to series resistance problems. Therefore, Takagi's temperature dependent unstrained Si mobility data were used here for fitting and comparison. Using a vertical-field dependence of $E_{eff}^{-0.28}$ for μ_{ph} and $E_{eff}^{-2.57}$ for μ_{sr}, best fits between the mobility data and the three-term model were obtained (Figure 2-7). The nine parameters for unstrained Si MOSFETs in the model were extracted by fitting the data over all temperatures and values of E_{eff}. The three mobility terms were then evaluated from the extracted parameters.

The three mobility terms of unstrained Si extracted from the best fit are:

$$\mu_{ph} = 3.50\times10^{7} E_{eff}^{-0.275} T^{-1.99} \qquad \text{Eq. 2-8}$$

$$\mu_{sr} = 6.86\times10^{2} E_{eff}^{-2.57} \qquad \text{Eq. 2-9}$$

$$\mu_C = 2.17\times10^{-4} Q_{inv}^{\ 0.59} T^{0.05} \qquad \text{Eq. 2-10}$$

The units used in this work are MV/cm for the effective field E_{eff}, K for temperature T, cm^2/V-sec for mobility and carriers/cm^2 for inversion layer charge density Q_{inv}.

2.3.3 Fitting the Strained Si Mobility with the Three-term Model

Next, the model was used to fit the strained Si mobility data at all temperatures using the same methodology as for the unstrained Si data (Figure 2-8). Best fits were obtained with $\mu_{sr} \sim E_{eff}^{\ r}$ where $r = -2.6 \pm 0.2$. The similar dependence of μ_{sr} on E_{eff} in both strained and unstrained Si MOSFETs indicates that enhancements will persist to very high E_{eff}. The quality of the fit was lower at 30 K. One potential explanation is that the dependence of the Coulomb term on Q_{inv} is altered at this low temperature.

The three mobility terms of strained Si extracted from the best fit are:

$$\mu_{ph} = 1.28\times10^{7} E_{eff}^{\ -0.719} T^{-1.64} \qquad \text{Eq. 2-11}$$

$$\mu_{sr} = 2.47\times10^{3} E_{eff}^{\ -2.60} \qquad \text{Eq. 2-12}$$

$$\mu_C = 2.43\times10^{-5} Q_{inv}^{\ 0.660} T^{-0.129} \qquad \text{Eq. 2-13}$$

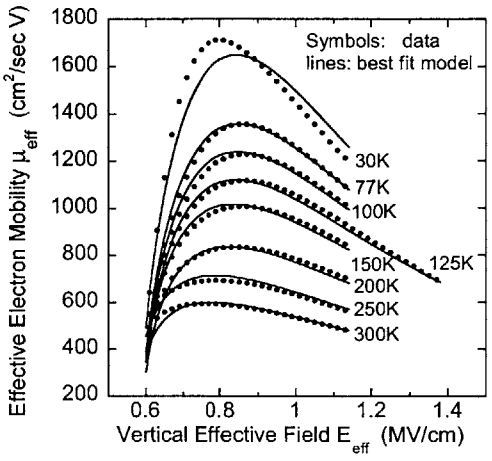


Figure 2-8 Comparison between measured strained Si *n*-MOSFET mobility with the model in this work. Symbols and solid lines represent the experimental data and the best-fit model, respectively.

2.3.4 The Mobility Terms Extracted from Fitting

After the parameters in the three-term model for electron mobility of unstrained and strained Si were obtained, the various mobility terms were calculated using those parameters.

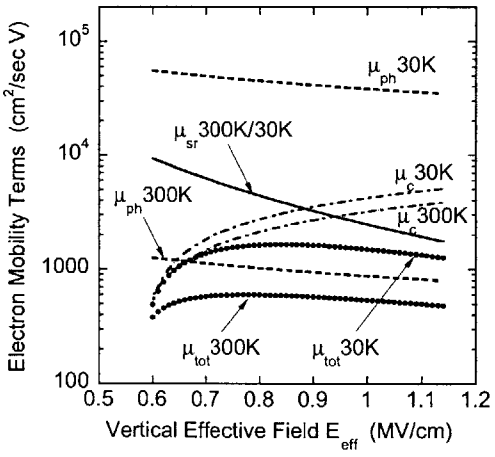


Figure 2-9 Extracted Strained Si *n*-MOSFET mobility terms limited by Coulomb, phonon and surface roughness scattering at 30 and 300 K. Symbols represent the total mobility.

Figure 2-9 illustrates the various terms calculated from the model for strained Si, as a function of E_{eff}. It can be seen that different mobility terms have different temperature dependence. μ_{ph} has the strongest temperature dependence, increasing by two orders of magnitude from 10^3 to about 10^5 when the temperature drops from 300 K to 30 K. The Coulomb term does not change appreciably over the same temperature range. The extracted surface-roughness limited mobility, μ_{sr} has essentially no temperature dependence. The relative magnitude of the three terms is also shown in Figure 2-9. At 300 K, the total mobility rolls off at low field. The phonon-limited mobility begins to dominate at around 0.7 MV/cm, and continue to have a key effect for E_{eff} up to 1.1 MV/cm. At 300 K, since the slope of μ_{ph} is less steep than that of μ_{sr}, the surface roughness term will dominate at higher fields, which is beyond the scale of this figure.

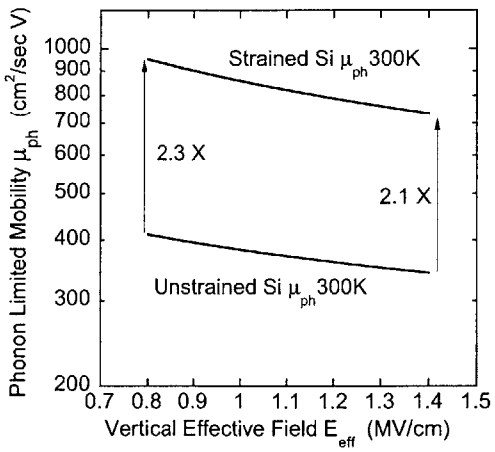


Figure 2-10 Extracted phonon limited mobility for strained and unstrained devices at 300 K.

The comparison of the extracted values for μ_{ph} for strained and unstrained Si MOSFETs at 300 K is shown in Figure 2-10. At room temperature, the

phonon-limited mobility is enhanced by ~2X for strained vs. unstrained devices over the intermediate and high E_{eff} range. Since the fitting of the mobility data of strained Si is performed in a limited E_{eff} range of 0.6~1.2 MV/cm, the magnitude of the phonon limited mobility term (which has weak dependence on the E_{eff}) is more accurate than the exponent of the power function for μ_{ph} in Eq. 2-11.

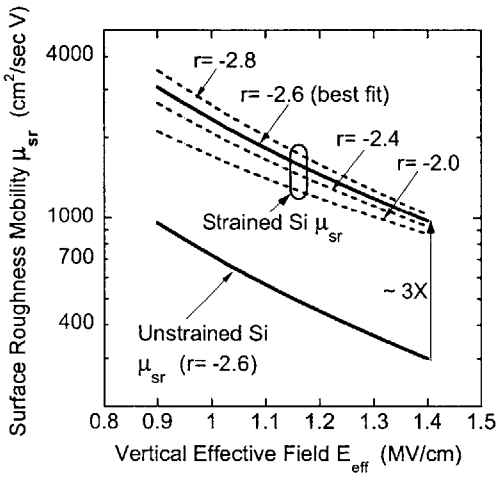


Figure 2-11 Extracted surface roughness limited mobility μ_{sr} for strained and unstrained Si devices. For strained Si, μ_{sr} terms for various values of r are shown ($r = 2.6 \pm 0.2$ gives the best fit to the data).

In Figure 2-11, the extracted surface roughness limited mobility μ_{sr} for strained Si MOSFETs was compared to that of unstrained devices. Best fits between the mobility data and the three-term model were obtained with $\mu_{sr} \sim E_{eff}^{r}$ where $r = -2.6 \pm 0.2$. According to the extraction, the surface roughness limited mobility of strained Si is enhanced by roughly 3X. The slope of μ_{sr} for strained Si devices is very close to that of unstrained devices, which corresponds to the constant spacing between the two curves on a semi-log scale. The similar dependence of μ_{sr} on E_{eff} in strained and unstrained Si MOSFETs indicates that enhancements will persist to very high E_{eff}.

This is consistent with the recently reported room temperature effective electron mobility enhancement of 1.6X at 1.6 MV/cm [19]. Some readers may wonder how a 2X enhancement in μ_{ph} and a 3X enhancement in μ_{sr} result in a 2X enhancement factor in total mobility at 300 K for a reasonably high field as shown in Figure 2-6. The reason lies in the Coulomb limited mobility. The strained Si devices in this work are doped two orders of magnitude higher than the unstrained Si devices from Takagi that were used in the model fitting for unstrained Si. Therefore, the Coulomb mobility of strained Si is much lower than that of the unstrained Si. As mentioned in section 2.3.2, the reason for not using the epi control devices for comparison was that the temperature dependent measurements on those devices were not successful. This reduction in μ_C results in a lower enhancement factor than expected. For example, at 1 MV/cm and 300 K the μ_C of extracted from the strained Si data is only one fifth that of that of unstrained Si.

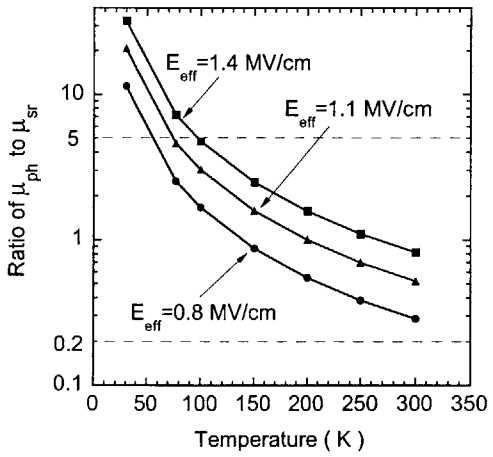


Figure 2-12 Ratio of extracted μ_{ph} to μ_{sr} of strained Si versus temperature at three fixed values of E_{eff}. A high ratio indicates the regime where μ_{sr} dominates the total mobility.

Figure 2-12 compares the relative magnitude of μ_{ph} and μ_{sr} of strained Si at three different E_{eff} from 30 K to 300 K. From Eq. 2-4, it can be seen that the total mobility is dominated by the smallest term. In other words, in the intermediate and high E_{eff} regime where μ_C can be ignored, if μ_{ph} is considerably larger than μ_{sr}, μ_{sr} is the dominant term. For example, if μ_{ph} is five times μ_{sr}, the total mobility μ_{eff} is 5/6 of μ_{sr}, and μ_{ph} has little influence on μ_{eff}. We can use the ratio of μ_{ph} to μ_{sr} as an indicator of the dominant term. When the ratio is above ten, we consider μ_{sr} to be the dominant term. When the ratio is less than one fifth, we consider μ_{ph} the dominant term. For cases where the ratio is between five and one fifth, the total mobility is influenced by both terms. The ratio of μ_{ph} to μ_{sr} increases at higher fields or lower temperatures. For example, at 1.4 MV/cm, the surface roughness term μ_{sr} dominates for T<90 K, while at 0.8 MV/cm, μ_{sr} dominates for T<50 K. From the analytic formula, we can calculate that E_{eff} as high as 3.6 MV/cm is required to get to the μ_{sr} dominant regime at room temperature. Since it is very hard to achieve high E_{eff} (> 2 MV/cm) at room temperature as the gate oxide breaks down for high vertical fields, a low temperature technique is required to effectively study the μ_{sr} dominant regime.

2.4 Accuracy of the Model

In order to estimate the accuracy of the model, we compare our mobility data with the published data from other groups. Any inaccuracies in the assumptions of the mobility extraction technique will introduce error in the modeling results.

Compared to the published mobility data measured by H. Nayfeh *et al.*, [19] the electron mobility of the strained Si MOSFETs in this work is about 20% higher, at the same apparent vertical effective field. This discrepancy may be due to a number of factors. First, the processing techniques are different. The devices fabricated in this work were *in-situ* boron doped during epitaxial layer growth while the devices fabricated by H. Nayfeh *et al.* were doped by ion implantation. The thermal budget used in this work (maximum temperature of 850C) is much less than that in H. Nayfeh's work (maximum temperature of 1000C). Second, the doping profiles are different, which may introduce uncertainties in the calculation of E_{eff}. As D. Vasileska *et al.*'s work on the universal behavior shows, when calculating E_{eff}, the weighting factors for the inversion and depletion charge densities depend on the shape of the doping profile [22]. In this work, a steep doping profile was used, and the doping varies from 3 x 10^{17} at the surface, to 8 x 10^{17} cm^{-3} at the maximum depletion depth, while the doping of H. Nayfeh's devices was fairly uniform over the depletion depth. From the above considerations, we estimate that the uncertainty in the relationship between the mobility and E_{eff} can be as large as 20%. It is important to realize that the actual extracted mobility values themselves are quite accurate, but that the calculation of the vertical effective field can be uncertain.

2.5 Discussion

In summary, temperature and vertical-field dependent measurements have been used to obtain a model that fits the mobility of both unstrained and strained Si

n-MOSFETs. Surface roughness limited mobility of strained Si *n*-MOSFETs is shown to have the same effective field dependence as that of unstrained Si *n*-MOSFETs. The modeling results also suggest that the surface roughness mobility term is itself enhanced by the strain. Further experiments would be necessary to investigate the mechanisms by which the strain might enhance this mobility term.

One possible explanation is that strain reduces the micro-roughness of the strained-Si/SiO_2 interface. Although there has been little study on this topic, extensive study has been made on the relation of the Si/SiO_2 interface roughness and the electron mobility in unstrained Si MOSFETs. Koga *et al.* showed that effective mobility degrades at high E_{eff} by intentionally roughening the Si/SiO_2 interface [23]. T. Yamanaka *et al.*'s study on the correlation between surface roughness and inversion layer mobility in unstrained Si MOSFETs showed that that the mobility is inversely proportional to a power function of the root mean square surface roughness measured by AFM [24].

On strained Si MOSFETs, Sugii *et al.* showed that by chemical-mechanical polishing (CMP) the $Si_{1-x}Ge_x$ buffer layer, the surface roughness of strained Si is considerably reduced, resulting in a higher hole mobility enhancement factors [25]. Theoretical calculation by Fischetti *et al.* indicates that the mobility enhancement of strained Si can be reproduced when assuming a smoother interface roughness for strained Si/SiO_2 [10]. Therefore, a detailed study of the strained Si/SiO_2 interface would be necessary for further understanding of the mobility enhancement in strained Si MOSFETs.

CHAPTER 3 Impact of Thermal Processing and Ion Implantation on the Mobility Enhancement in Strained Si *n*-MOSFETs

This chapter focuses on a critical processing challenge in strained Si technology. In strained Si MOSFETs, a heterostructure of strained Si on relaxed SiGe is grown on silicon wafers. In terms of material properties, such as defect density and thermal and mechanical compatibility, the relaxed SiGe layers substrates are not as perfect as bulk Si substrates. The heterostructures are generally more susceptible to thermal processing because the strained Si layer (if the thickness is above the critical thickness [26]) may begin to relax to its equilibrium state during thermal processing, which is undesirable. Some processing steps play important roles in strain relaxation, such as thermal processing, ion implantation and reactive ion etching (RIE). The latter two steps can introduce defects to the substrates [27]. Ion implantation may assist strain relaxation by introducing ion implantation damage into the lattice. These effects will result in the loss of mobility enhancement. Therefore, understanding the influence of the processing steps on the mobility is very important for strained Si technology.

In this work, the effects of thermal processing and ion implantation are investigated. Section 3.1 is an introduction to the understanding of strained Si processing to date. Section 3.2 describes the experimental design and device

fabrication performed in this work. Section 3.3 is discusses the electrical characteristics and Medici simulations. Section 3.4 describes the mobility characterization and results. Section 3.5 discusses the materials analysis and the mechanisms of mobility degradation during processing. Section 3.6 presents the impact on technology.

3.1 Introduction to the Processing of Strained Si

3.1.1 Critical Thickness and Strain Relaxation in Strained $Si/Si_{1-x}Ge_x$

When a thin crystalline thin film is grown on a crystalline substrate with a different equilibrium lattice constant, strain is introduced into the thin film. As long as the film is thin enough, it will adopt the in-plane lattice constant of the substrate. The strain can be released by breaking some of the deformed bonds, creating dislocations in the crystal structure of the film. For this to happen, the film needs to be thicker than the critical thickness t_{crit}, above which it is energetically favorable for dislocations to be present in the film [26]. In theory, a film with thickness less than t_{crit} can be subject to unlimited thermal exposure without any relaxation of the strain by misfit dislocation formation. It is important to remember that diffusion of the components of the alloy (Si and Ge) can also lead to strain relaxation by a change in composition of the structure. The concept of the critical thickness is important for device fabrication, in which the devices are exposed to thermal processing often at

high temperatures. Maintaining the strain is the key to obtaining the performance improvement in the strained Si MOSFETs.

Houghton studied the critical thickness of strained $Si_{1-x}Ge_x$ on unstrained Si, which is a good starting point for estimating the critical thickness of strained Si on unstrained $Si_{1-x}Ge_x$ [28]. Figure 3-1 shows the calculated kinetically limited critical thickness for strained $Si_{1-x}Ge_x/Si$ at various temperatures and Ge fractions. For example, the equilibrium critical thickness for strained $Si_{0.8}Ge_{0.2}/Si$ is about 120 Å.

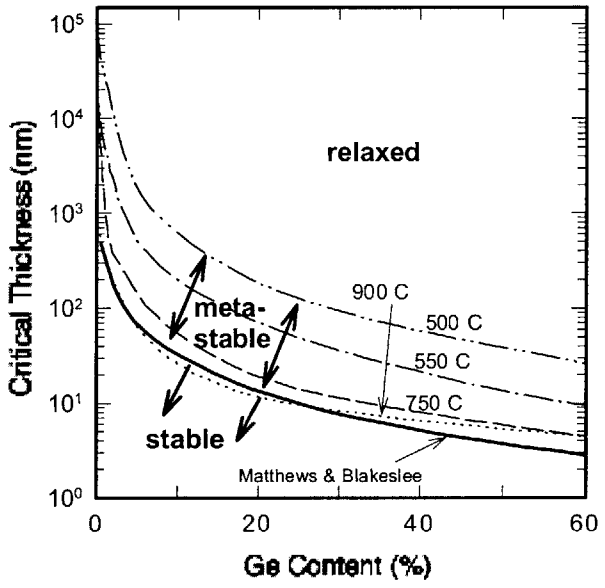


Figure 3-1 Calculated kinetically limited critical thickness for strained $Si_{1-x}Ge_x/Si$ at various growth temperatures. From D. Houghton [28]. Metastable strained layers that are thicker than the critical thickness predicted by Matthews & Blakeslee criteria [29] can be achieved by low temperature epitaxial growth.

Samavedam *et al.* used the Mattews-Blakeslee's (MB) energy minimization criterion [26] to calculate the strained Si critical thickness as a function of Ge fraction in the underlying uniform SiGe layer [30]. They obtained a calculated t_{crit} of about 205 Å for a strained Si layer on $Si_{0.8}Ge_{0.2}$. In the experiments performed in that work, etch pit density measurements were used to characterize the misfit dislocation

density. Misfit dislocations were present for Si cap thicknesses above 110 Å which was grown at 700°C on the $Si_{0.8}Ge_{0.2}$ substrate with a threading dislocation density of 10^5~10^6/cm^2. The $Si_{0.8}Ge_{0.2}$ substrates used in this work have comparable dislocation density. Currie *et al.* studied the channel thickness dependence of electron mobility in strained Si MOSFETs on $Si_{0.8}Ge_{0.2}$ virtual substrate with a threading dislocation density of ~10^5/cm^2, and they found that all the layers thinner than 120 Å are fully strained [31]. Therefore, the critical thickness of the strained $Si/Si_{0.8}Ge_{0.2}$ in this work is estimated to be about 110~120 Å.

When the thickness of a strained Si layer is above t_{crit}, the effective stress makes it favorable for misfit dislocations to be present in the crystal structure. It is necessary to overcome an initial energy to nucleate a dislocation. Thermal processing can provide energy for dislocations to nucleate and later propagate. Particles and defects at a heterointerface can act as dislocation nucleation centers. Each dislocation line relieves a certain amount of strain proportional to the length of the misfit dislocation segment. The density of misfit dislocations can be measured by selective etching of the strained Si surface. The presence of misfit dislocations indicates the strained Si is not fully strained.

3.1.2 Strain Relaxation and Thermal Stability of Strained $Si_{1-x}Ge_x/Si$

The strained $Si_{1-x}Ge_x$ on relaxed Si substrate has been extensively studied due to its importance in many device structures such as the heterojunction bipolar transistor. The strained $Si_{1-x}Ge_x/Si$ system is discussed here as it is a good analogy to the strained $Si/Si_{1-x}Ge_x$ system. It provides useful references and knowledge since the

latter system is not as fully studied. Thermal stability and strain relaxation in the strained Si layer are problems in the processing of strained Si, since the mobility enhancement depends on the strain in the Si layer and its stability. Two problems in the strained $Si_{1-x}Ge_x$ /Si system are discussed first.

The thermal stability of $Si_{1-x}Ge_x$ films has been studied by Houghton *et al.* [28] and Matthews and Blakeslee [26] as previously mentioned (see Figure 3-1). There has been some study on ion implantation effects and relaxation in the strained $Si_{1-x}Ge_x$/Si system. R. Hull *et al.* found significantly enhanced strain relaxation during annealing in Si/strained $Si_{1-x}Ge_x$/Si heterostructures via point-defects introduced by ion implantation of boron and arsenic [32]. This enhanced strain relaxation is the result of the increased nucleation sites introduced by ion implantation. D. Misar *et al.* studied the annealing of Si/strained $Si_{1-x}Ge_x$/Si after phosphorus implantation and suggested that the permanent dislocation loops resulting from the implantation cause strain relaxation [27]. B. Hollander *et al.*, using H+ and He+ to implant the $Si_{1-x}Ge_x$/Si(100) heterostructures, showed annealed samples to have much denser, irregular misfit dislocations than the unimplanted ones, causing the $Si_{1-x}Ge_x$ to relax [33].

3.1.3 Background of Processing Influence on Mobility Enhancement in Strained Si

There has been some study on the materials properties of the strained Si on $Si_{1-x}Ge_x$ buffer layer. Currie *et al.* have studied the effects of strain, well

implantation, thermal budget and channel thickness on the mobility of strained Si MOSFETs [31]. In his work, 13 keV boron and 45 keV phosphorous were implanted into the $Si_{0.7}Ge_{0.3}$ virtual substrate with a dose of $1x10^{12}$ cm^{-2} to the NMOS and PMOS prior to MOSFET processing. It should be noted that this is a relatively low implant dose. After a 1000°C 1 sec rapid thermal anneal (RTA), the measured mobility enhancement was the same of implanted and unimplanted devices. Currie's results agree with the result in this work, in which an implantation dose as low as $1x10^{12}$ cm^{-2} has no effect on the mobility enhancement (see details in sections 3.4).

Currie's study on the thermal budget effect was conducted on NMOS and PMOS on $Si_{0.7}Ge_{0.3}$ virtual substrates with no ion implantation. The RTAs were performed at 1000°C and 950°C from 1 sec to 30 sec. His results showed that the mobility enhancement factor of NMOS was reduced from 1.7X to 1.2X with RTA at 1000°C for 30 sec. It should be noted that the MOSFETs used in his work were made by one-mask short-flow process, in which large geometry ring transistors were made using low-temperature deposited oxide as the gate dielectric. These MOSFETs were not fabricated by the conventional processes in the industry. Therefore, additional detailed studies are required in order to understand the behavior of modern devices.

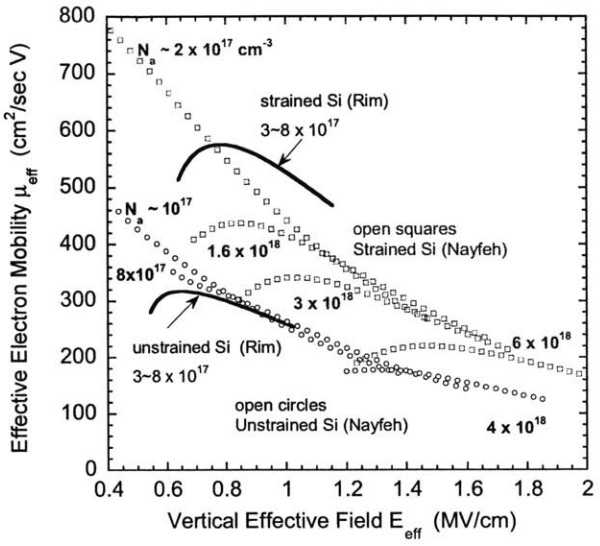


Figure 3-2 Comparison between K. Rim's and H. Nayfeh's effective mobility data of strained Si *n*-MOSFETs on $Si_{0.8}Ge_{0.2}$ substrate and unstrained control devices [4], [16].

Experimental work published so far has given some evidence of the potential influence of processing on the mobility in the strained Si MOSFETs using conventional fabrication processes. Different enhancement factors have been reported by K. Rim *et al.* and H. Nayfeh *et al.* for strained *n*-MOSFETs on $Si_{0.8}Ge_{0.2}$ substrate [4,16]. Figure 3-2 shows that at E_{eff} =1 MV/cm, the mobility of K. Rim's strained Si devices is higher than H. Nayfeh's by 20%. There are some differences between these two process flows. One is the thermal budget. In K. Rim's study, the gate oxide was grown at 800°C, source/drain implant annealing (2 min at 650°C and 15 s at 850°C) and the Ti salicide formation annealing (2 min at 650°C). In H. Nayfeh's processing flow, gate oxide was grown at 800°C, RTA performed at 1000°C for 1 sec, no salicide formation. Another difference is that K. Rim's devices were *in-situ* doped while H. Nayfeh's were doped by ion implantation. It is possible that

the higher thermal budget and ion implantation damage introduced some mobility degradation in H. Nayfeh's devices.

Even in the same process, H. Nayfeh *et al.* showed that the strained Si *n*-MOSFETs with highest boron implantation dose 7 x 10^{13} cm^{-2} (equivalent doping 6 x 10^{18} cm^{-3}) have lower electron mobility enhancement than devices with low doses [16]. There are two possible reasons for this mobility degradation. One is strain relaxation due to implantation induced lattice damage; the other is the higher Coulomb scattering due to higher dopant concentration. To investigate these two mechanisms, a long channel strained/bulk Si *n*-MOSFET process was designed in this work. Neutral Si and Ge were implanted into the channel. The channel doping was kept unchanged assuming channel dopant diffusion is not significantly changed by the ion implantation. Therefore, the mobility degradation due to ion implant damage is separated from the degradation due to ionized impurity Coulomb scattering effects. UT-MARLOWE simulation was used to obtain the damage profiles of Si, B and Ge in order to choose the implantation energies and doses used in the process.

3.2 Experiment Design and Fabrication

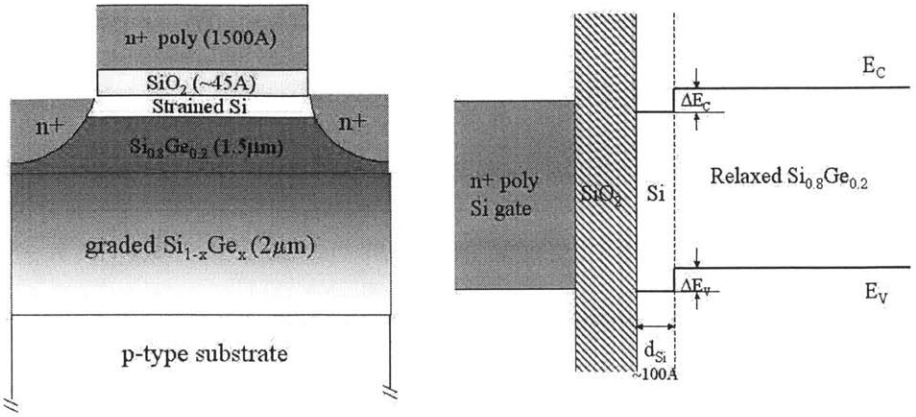


Figure 3-3 (a) Structure of strained Si *n*-MOSFETs after processing. (b) Energy band alignment for a surface strained Si *n*-MOSFET.

The structure of the strained-Si *n*-MOSFETs after fabrication is illustrated in Figure 3-3 (a). Relaxed $Si_{0.8}Ge_{0.2}$ layers were epitaxially grown by M. Lee on a graded relaxed $Si_{1-x}Ge_x$ buffer layer in a UHVCVD reactor. The graded $Si_{1-x}Ge_x$ buffer layer was formed by increasing the Ge content from 0 to 20% over a thickness of 2 μm. The strained Si layer was epitaxially grown on the relaxed $Si_{0.8}Ge_{0.2}$ layer. The as-grown thickness of the strained Si layer was 18 nm. The strained Si was consumed during the gate oxidation and surface cleaning processes. From the CV measurement and simulation, the remaining strained Si layer thickness is estimated to be 100 Å. Figure 3-3 (b) shows the energy band alignment of the strained Si MOSFET structure. The conduction band and valence band in strained Si are both lower than that of relaxed $Si_{1-x}Ge_x$. The offsets ΔE_C and ΔE_V depend on the Ge fraction. In the case of $Si_{0.8}Ge_{0.2}$, it happens that they are both about 125 mV.

The strained Si layer and the $Si_{0.8}Ge_{0.2}$ layer were *in-situ* doped in the UHVCVD reactor. The doping level is 2.5~3 x $10^{17}cm^{-3}$. The CZ control wafers were boron

doped 1 x $10^{17}cm^{-3}$ p-type wafers. This doping difference between strained Si and CZ control devices offsets the threshold voltage (V_{th}) difference introduced by the energy band splitting of strained Si. Therefore, the measured V_{th} of strained Si devices matches that of CZ control devices.

Implant Conditions	Implant Species	Dose (cm^{-2})	Energy (keV)	Simulated Peak Amorphization	Simulated R_P (Å)	Comments
ϕ1	Si	4 x 10^{12}	39	2.5%	160	Match the Damage of B 7 x 10^{13} cm^{-2} 10keV
ϕ2	Si	2.7 x 10^{13}	39	16%	240	Match the Damage of B 5 x 10^{14} cm^{-2} 10keV
ϕ3	Si	1 x 10^{14}	35	54%	170~280	Sub Amorphous B 2 x 10^{15} cm^{-2} 10keV
ϕ4	Si	5 x 10^{14}	30	100%	200	Amorphous B 5 x 10^{15} cm^{-2} 10keV
ϕ5	Ge	3 x 10^{13}	30	60%	100	Match the Damage of Si ϕ3
ϕ6	Ge	1 x 10^{15}	30	100%	200	Typical Dose for Deep Source/Drain As Implant

Table 3-1 The ion implantation conditions used in this work. The peak amorphization and the average project range (R_p) are from UT-MARLOWE simulation. The implantation conditions of Si ϕ1 and ϕ2 are chosen to match the damage profile of boron with doses 7 x 10^{13} cm^{-2} and 5 x 10^{14} cm^{-2} at 10keV.

Si and Ge were implanted into the channel before the gate stack formation. The implant condition matrix is shown in Table 3-1. The damage profiles of the implant conditions ϕ1~ϕ6 are shown in Figure 3-4 and 3-5 as simulated by UT-MARLOWE. In the UT-MARLOWE simulation, normalized interstitial concentration profiles were

generated to represent the degree of amorphization caused by ion implantation damage. In the simulation, a Si substrate was used to approximate the actual multilayer SiGe substrate. It is well known that there is very little difference in the ion implant profiles into Si vs. SiGe at the Ge contents used in this work.

First, the damage profiles were simulated for commonly used boron (7×10^{13} and 5×10^{14} cm^{-2} both at 10keV) and arsenic ion implantation conditions (1×10^{15} at 30 keV) for MOSFET deep source/drain or extension implantation. Then the implantation conditions $\phi 1$, $\phi 2$ of Si were carefully designed to match the damage of the boron (B) profiles, as shown in Figure 3-4. To match the average project range (R_p) of the light boron atoms implanted at 10 keV, the implant energy of Si needs to be larger, around 30 keV. Since Ge and As have very close atomic mass, 72.59 and 74.92 respectively, the damage profiles of Ge implant were assumed to be good matches to those of As under the same implant conditions. The same is true for Si and P, which have atomic masses of 28.09 and 30.97 respectively. Other doses for Si and Ge were chosen to represent the cases in the sub-amorphous and amorphous regime where the Si channel was highly damaged, such as $\phi 3$ and $\phi 4$ of Si. Condition $\phi 5$ for Ge implantation had a similar damage profile as that of $\phi 3$ for Si implantation. This was used to check whether the damage effects depend on the implant species. In summary, the implant doses for Si range from 4×10^{12} cm^{-2} to 5×10^{14}, and 3×10^{13} to 1×10^{15} cm^{-2} for a Ge implant.

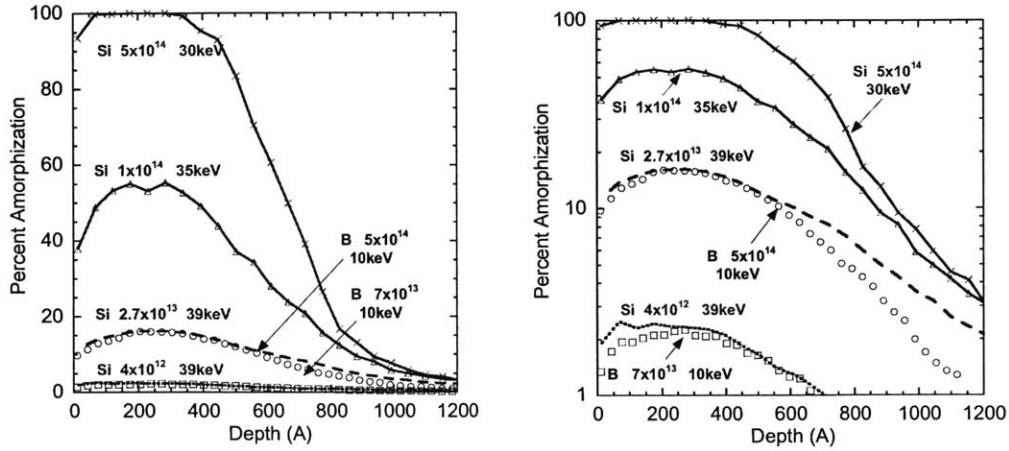


Figure 3-4 Damage profiles for Si implantation ϕ1~ϕ4 in comparison with those of boron implants (doses 7 x 10^{13} cm^{-2} and 5 x 10^{14} cm^{-2}, both implanted at 10 keV). All the profiles were simulated by UT-MARLOWE.

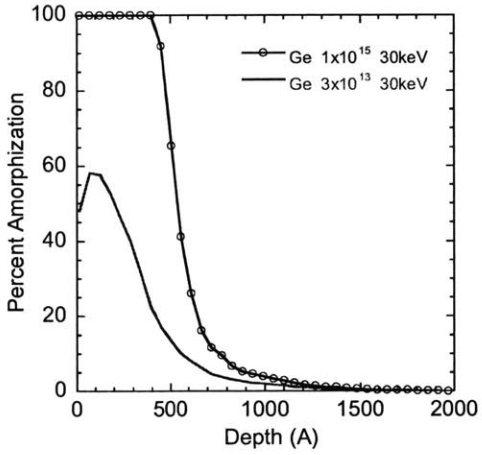


Figure 3-5 Damage profiles of the implant conditions ϕ5 and ϕ6 for Ge, simulated by UT-MARLOWE.

Wafers with Strained Si	CZ Control Wafers	RTA Splits	Implant Species	Implant Conditions
E1	CZ1	RTA1	Si	N | ϕ2
E2	CZ2	RTA1	Si	N | ϕ3
E3	CZ3	RTA1	Si	ϕ1 | ϕ4
E4	---	RTA1 (no reoxidation)	Si	ϕ1 | ϕ4
E5	CZ5	RTA2	Si	N | ϕ2
E6	CZ6	RTA2	Si	N | ϕ3
E7	CZ7	RTA2	Si	ϕ1 | ϕ4
E8	CZ8	RTA3	Si	ϕ1 | ϕ4
E9	CZ9	RTA1	Ge	ϕ5
E10	CZ10	RTA1	Ge	ϕ6

Table 3-2 The experimental matrix used in this work. For wafers with Si implants, there is one implant condition on each half of the wafer, i. e., N | ϕ2 means the left half of wafer has no implant, while the right half of the wafer is implanted with condition ϕ2. RTA1, 2, 3 are the annealing conditions: 1000°C for 1 sec, 1000°C for 10 sec and 950°C for 10 sec respectively

Table 3-2 shows the wafer matrix used in this work. The wafers with epitaxial strained Si/relaxed $Si_{0.8}Ge_{0.2}$ layers are denoted as E1 to E10. The Czochralski control wafers are denoted as CZ1 to CZ10. There are two implant conditions on each wafer for wafers with a Si implant: one implant condition on the left half of the wafer and the other on the right half. For example, N | ϕ2 indicates that the left half of wafer has no implant, while the right half of the wafer is implanted with condition ϕ2. Photoresist was used to protect one half of the wafer while the other half was implanted.

After the implantation, the gate oxide layers of all wafers were grown at 800°C for 30 minutes in a dry oxygen ambient (the total time in furnace was approximately one hour including the temperature ramp up and down). The gate oxide thickness

was measured from 43.6 to 47 Å across the boat. 1500 Å polycrystalline silicon was deposited at 625°C on top of gate oxide. After gate etch, reoxidation was performed at 800°C on all the wafers for 11 minutes (about 50 minutes in furnace) except wafer E4 (see Table 3-2.), which was used to compare with wafer E3 to check the effects of reoxidation. Phosphorus of dose 5 x 10^{15} cm^{-2} with energy 10keV was implanted as a deep source/drain and gate implant.

In order to investigate the effects of thermal processes on damage anneal and mobility behavior, three different rapid thermal anneals (RTAs) were used to anneal the implantation damage, RTA1 at 1000°C for 1 sec, RTA2 at 1000°C for 10 sec and RTA3 at 950°C for 10 sec respectively. In total, 19 wafers were processed successfully. Table 3-2 shows the wafer matrix with the corresponding RTAs and implant conditions. After the RTAs, contact cuts were patterned. 1000 Å Ti and 1 um Al were sputtered. The metal level was patterned using wet etch. The metal was sintered at 400°C for 40 minutes in the forming gas.

3.3 Electrical Characteristics and Medici Simulations

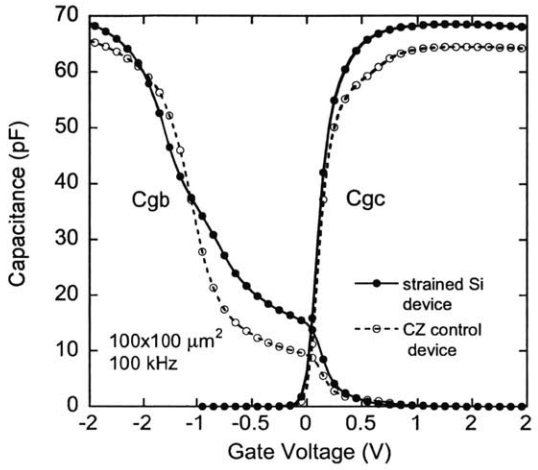


Figure 3-6 Split C-V measurements for a strained Si and a bulk *n*-MOSFET.

Split CV method was used to extract electron mobility from I_d-V_g and split C-V measurements. Figure 3-6 shows the split C-V measurement of wafer E1 and wafer CZ1 on the devices of size 100 x 100 μm^2 with RTA1. The gate to body capacitance (C_{gb}) and gate to channel capacitance (C_{gc}) were measured. From the C_{gc} curve, it is clear that there is some poly-depletion for the devices with RTA1, which indicates that the dopants are not fully activated. The threshold voltages (V_{th}) of both devices are very close. The reason is that the doping levels of epi wafers are higher than those of CZ wafers, which cancels out the V_{th} drop for strained Si devices due to conduction band splits.

The mobility was calculated using Eq. 3-1 and Eq. 3-2 below. The mobility of the devices on the same wafer with the same implant condition can be different by 10% mainly due to processing non-uniformity. In the figures below, a comparison is made between the different mobility curves. However, it should be noted that any difference less than 15% is within the error of this experiment.

$$E_{eff} = \left(\frac{1}{\varepsilon_{Si}}\right)\left(aQ_{depl} + bQ_{inv}\right) \qquad \text{Eq. 3-1}$$

$$\mu_{eff} = \left(\frac{L}{W}\right)\frac{g_d}{Q_{inv}} \qquad \text{Eq. 3-2}$$

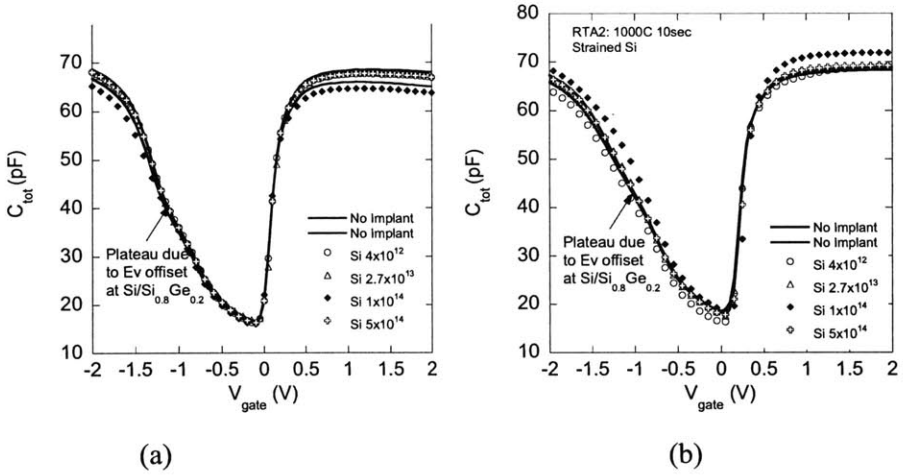
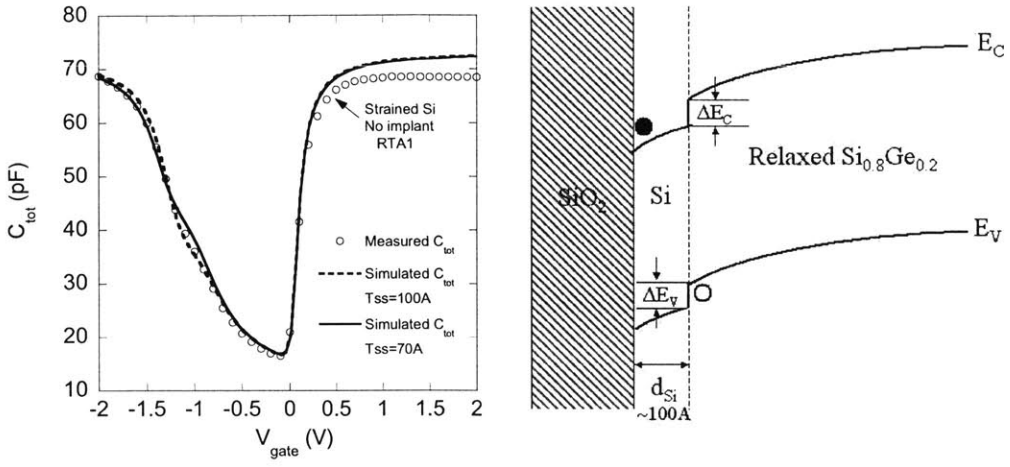


Figure 3-7 Total capacitances C_{tot} vs. V_{gate} of strained Si wafers. (a) wafers with RTA1, 1000°C for 1 sec (b) wafers with RTA2, 1000°C for 10 sec.

The total capacitance C_{tot} was calculated as the sum of C_{gb} and C_{gc}. Figure 3-7 shows the C_{tot} vs. V_{gate} curves of the strained Si devices with different implantation conditions. The C_{tot} curves overlap very well, which indicates that the devices have similar channel doping, band structures and thickness of strained Si layers. In Figure

3-7 (a), the small plateau in the left half of C_{tot} is caused by the discontinuity of the valence band at the strained $Si/Si_{0.8}Ge_{0.2}$ interface as shown in Figure 3-8 (b). The vertical position of the plateau is determined by the thickness of the strained Si layer: the thicker the layer is, the lower the plateau is. The plateau in Figure 3-7 (b) is more subtle than that in Figure 3-7 (a), which indicates a smeared out interface by Ge out diffusion into the strained Si layer during the RTA2 (1000°C for 10 sec). This effect can be simulated by Medici as a means to determine the thickness of the strained Si layer.



(a) (b)

Figure 3-8 (a) Ctot curves simulated by Medici with different thicknesses of the strained Si layer compared with the measured Ctot. The curve with 100 Å strained Si layer matches the measured data better than that of 70 Å. (b) band diagram of a strained Si MOSFET in the depletion regime. Holes are accumulated at the strained Si/ relaxed $Si_{0.8}Ge_{0.2}$ interface due to the band discontinuity.

Figure 3-8 (a) shows the C_{tot} curves simulated by Medici with different thicknesses of the strained Si layers. The dotted curve is the simulated C_{tot} for devices with 100 Å thick strained Si, while the solid curve represents C_{tot} for devices with 70 Å strained Si. The position of the small plateau is higher for the device with thinner strained Si layer. The C_{tot} curve with 100 Å strained Si layer matches the measured data better than that of 70 Å. Figure 3-8 (b) illustrates the band discontinuity at the interface of the strained Si and the relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate of the strained Si MOSFETs. The plateau of the C_{tot} curve is the result of this band discontinuity.

As explained in Section 3.1.1 above, it is reasonable to assume the critical thickness of the strained Si layer on $Si_{0.8}Ge_{0.2}$ of this process is about 120 Å. It should be noted that it is the thickness of the strained Si layer during thermal

processing which determines the strain relaxation behavior, not the final thickness after processing. In this process, the starting thickness of the strained Si layer was about 180 Å. During the processing, the strained Si was partially consumed by surface cleaning and oxidation. Just before the first thermal process gate oxidation, the strained Si layer has gone through two post-implantation cleans and two RCA cleans. The thickness of the strained Si layer at this point was about 130 Å, larger or close to the estimated critical thickness of strained Si on $Si_{0.8}Ge_{0.2}$ substrate. It is likely that misfit dislocations nucleate and propagate during the gate oxidation, reoxidation and RTAs. As discussed in subsequent sections, materials analysis is required to give a detailed picture of the damage profile and the thermal processes.

3.4 Mobility Dependence on Processing Factors

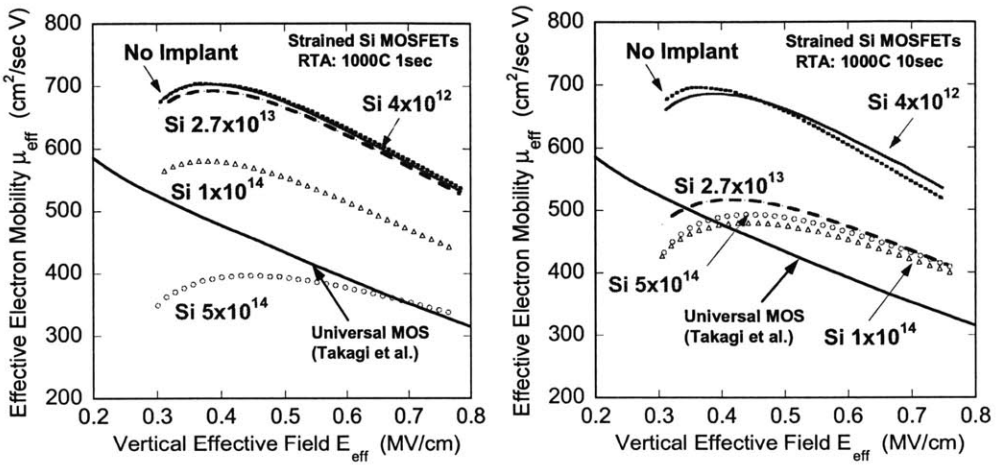


Figure 3-9 The effective mobility vs. E_{eff} for the strained Si devices with different implantation conditions for (a) devices with RTA1, 1000°C for 1 sec, and (b) devices with RTA2, 1000°C for 1 sec. The measurements were made on 100 x 100 μm^2 devices.

Figure 3-9 shows the effective mobility curves for the strained Si devices with different implant conditions. All the devices measured here have the same reoxidation step. Figure 3-9 (a) shows the mobility curves for devices with RTA1 (1000°C for 1 sec). In Figure 3-9 (a), the electron mobility curve for devices with no implant shows an enhancement factor of 1.7X over the universal electron mobility by Takagi *et al.* at E_{eff} = 0.7 MV/cm. It is seen that the effective mobility degrades monotonically with increasing implant dose. No mobility degradation is observed for Si implant doses of 4 x 10^{12} cm^{-2} and 2.7 x 10^{13} cm^{-2}. For doses 1 x 10^{14} and 5 x 10^{14} cm^{-2}, at E_{eff} = 0.7 MV/cm, the enhancement factor degrades from 1.7X to 1.3X and 1.2X~1.0X (mobility range from measurement) respectively, which implies the mobility enhancement from strain induced energy band splitting is reduced.

Figure 3-9 (b) shows the mobility curves for strained Si devices with RTA2 (1000°C for 10 sec). The mobility for devices with no implant in (b) is very close to that in (a), which means that RTA2 without implantation doesn't cause strain relaxation or mobility degradation. This agrees with the observation of S. B. Samavedam *et al.* [30]. Based on their work, strained Si layers are significantly resistant to plastic strain relief by misfit dislocations during high temperature anneal. What causes the degradation is the combination of implantation damage and higher thermal budget (see the mobility curves with implant). Different from (a), the mobility starts to show degradation with the dose of 2.7×10^{13} cm^{-2}. The devices with implant doses 2.7×10^{13}, 1×10^{14} and 5×10^{14} cm^{-2} have the same mobility to within experimental error. Neutral Si atoms scattering may also play a role in the mobility degradation [34], which can be viewed as part of implantation defect scattering.

Comparison between Figure 3-9 (a) and (b) shows that RTA makes a significant difference for devices with intermediate doses, e.g. 2.7×10^{13} cm^{-2} and 1×10^{14} cm^{-2}. For higher thermal budget processing, mobility starts to degrade for devices with lower doses. We can define a ***critical implant dose*** ϕ_{cr} for a certain thermal budget, above which the mobility degrades significantly, but the mobility enhancement still exists. From Figure 3-9, it is seen that ϕ_{cr} for RTA1 is in the range from 2.7×10^{13} cm^{-2} to 1×10^{14}, while the ϕ_{cr} for RTA2 is in the range from 4×10^{12} cm^{-2} and 2.7×10^{13} cm^{-2}. As the thermal budget increases, the ϕ_{cr} decreases. The interaction of thermal processing and implant damage might be responsible for this trend.

The solid-phase epitaxy of Si starts at a relatively low temperature of 500°C [35]. The regrowth rate has an exponential relationship with temperature. Since our first thermal step is gate oxidation at 800°C for an hour in furnace, solid-phase epitaxy of the amorphized layer (in the case of high implant doses) should be completed during this step. However, the end-of-range dislocation loops will be present after the regrowth of the amorphized Si layer. These dislocation loops can act as scattering centers and the nucleus for the misfit dislocations to grow, which result in strain relaxation and mobility degradation.

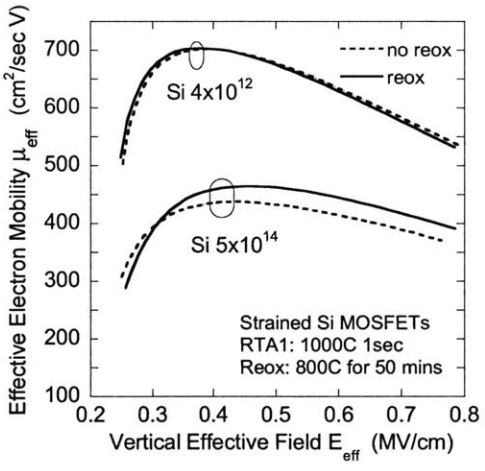
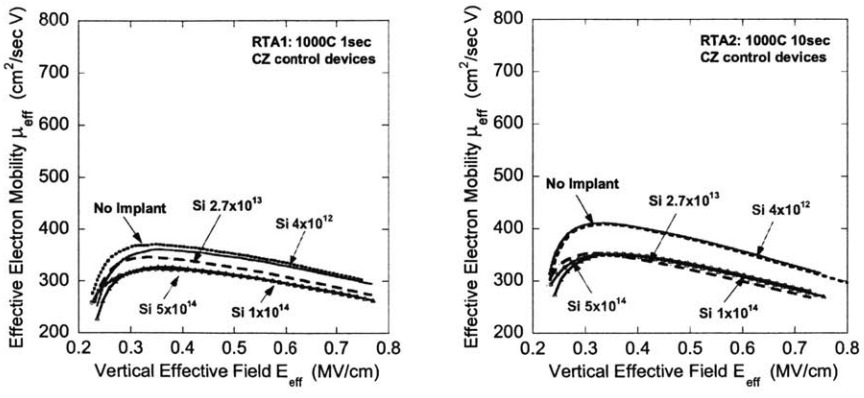


Figure 3-10 Comparison of the effective mobility curves for strained Si MOSFETs with or without reoxidation. The implant conditions are ϕ1 and ϕ4, with same annealing step RTA1.



(a) (b)

Figure 3-11 The effective mobility vs. E_{eff} for the CZ control devices with different implantation conditions for (a) devices with RTA1, and (b) devices with RTA2. The measurements were made on 100 x 100 μm^2 devices.

Figure 3-10 shows the effect of reoxidation on mobility for strained Si wafers with the lowest Si implant dose 4 x 10^{12} cm^{-2} and the highest Si dose 5 x 10^{14}. The reoxidation was performed at 800°C for about 50 minutes in furnace. The solid lines are the mobility curves for devices without reoxidation, and the dotted lines for those with reoxidation. Within the error bar, there is no difference between the devices with and without reoxidation for the low dose 4 x 10^{12} cm^{-2} and the high dose 5 x 10^{14} cm^{-2}.

Figure 3-11 shows the dependence of mobility on implant doses and RTAs for CZ control devices. In the CZ control wafers, there is no issues with strain relaxation and Ge diffusion due to thermal processing, therefore the mobility degradation is mainly due to ion implantation damage. Compared with the strained Si devices, the CZ control devices have much less dependence on implantation dose and thermal budget.

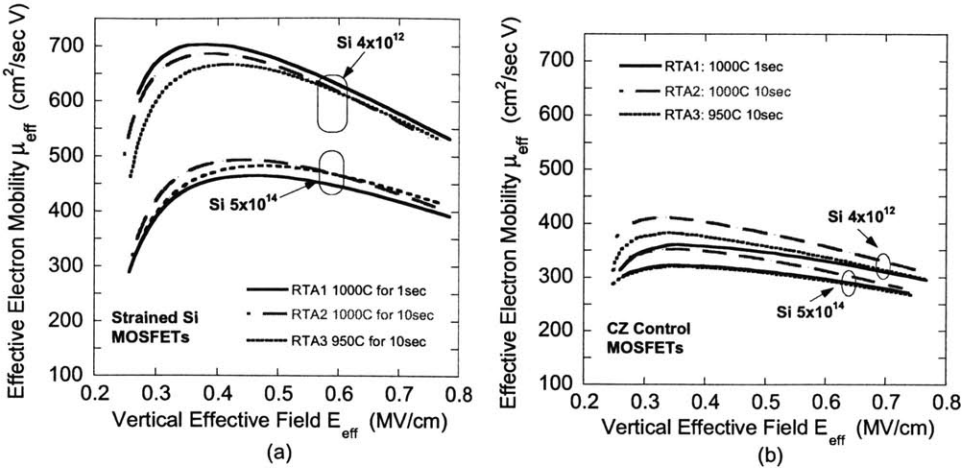


Figure 3-12 Effective mobility vs. vertical effective field E_{eff} for strained Si and CZ control devices with different RTAs. The doses are the lowest, 4 x 10^{12} cm^{-2} and the highest 5 x 10^{14} cm^{-2}. RTA1, 2, 3 are 1000°C for 1 sec, 1000°C for 10 sec and 950°C for 10 sec respectively.

Figure 3-12 compares the mobility curves of devices with 3 RTA splits. RTA1, 2, 3 are 1000°C for 1 sec, 1000°C for 10 sec and 950°C for 10 sec respectively. The comparison is made on devices with the lowest Si implant dose 4 x 10^{12} cm^{-2} and the highest dose 5 x 10^{14} cm^{-2}. Figure 3-12 (a) is for the strained Si MOSFETs and (b) is for the CZ control devices. Compared with the strong RTA dependence seen on intermediate doses, the RTAs used in this work do not have a strong effect on the mobility for doses of 4 x 10^{12} and 5 x 10^{14} cm^{-2}. This is true for both strained Si MOSFETs and CZ MOSFETs. In Figure 3-12 (a), the devices with 4 x 10^{12} cm^{-2} dose implant have the same mobility as the ones without implant. This indicates that the critical doses ϕ_{cr} for these three thermal budgets are higher than 4 x 10^{12} cm^{-2}, thus no degradation is seen for the devices with 4 x 10^{12} cm^{-2} implant.

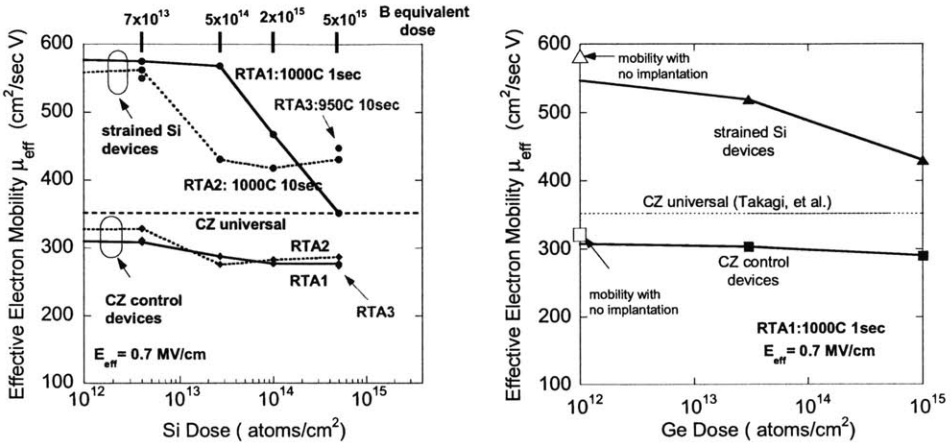


Figure 3-13 Effective mobility at E_{eff}=0.7 MV/cm for strained Si and CZ control devices of different species, doses and RTA, for (a) devices with Si implant, (the equivalent boron doses is shown in the upper x axis), and (b) devices with Ge implants.

Figure 3-13 shows the mobility at E_{eff}=0.7 MV/cm for strained Si and CZ control devices vs. implant doses for different RTAs. The reason to pick this particular field is that at higher field, Coulomb limited mobility has less influence on the total mobility and the measured mobility is closer to the universal mobility for strained Si (see Figure 3-14). The highest field in our measurement is around 0.7 MV/cm. It is seen in Figure 3-13 (a) that the mobility starts to degrade at a certain critical dose Φ_{cr} for strained Si MOSFETs. This critical dose Φ_{cr} depends on the thermal budget. For example, mobility starts to degrade around at dose of 3 x 10^{13} cm^{-2} for RTA1 (1000°C 1 sec), while the critical dose for Si with RTA2 (1000°C 10 sec) is about 4 x 10^{12} cm^{-2}. Below this critical dose, mobility degradation is negligible. As mentioned above, the damage profiles of Si are very close to that of P. Therefore, the critical doses of Si should be good approximations of those of P with

same thermal budgets. The B equivalent doses in term of damage profiles are show in Figure 3-13 (a). From (a), we can estimate the critical dose for B implanted devices with RTA1 (1000°C 1 sec) is about 5 x 10^{14}, while for those with RTA2 (1000°C 10 sec) is about 7 x 10^{13} cm^{-2}.

It should be noticed that the critical doses Φ_{cr} obtained in this work are based on the study of neutral implant Si and Ge without considering Coulomb scattering effects by ionized dopants. The term "equivalent dose" is in terms of the ion implant damage profiles. If Coulomb effects are included, the real critical dose Φ_{cr} for dopant species B, P, and As should only be less than what is observed here.

Figure 3-13 (b) shows the mobility at E_{eff}=0.7 MV/cm for Ge implanted devices with RTA1 (1000°C 1 sec). The critical dose for Ge and thus As with RTA1 is about 1 x 10^{12} cm^{-2}. The highest damage in this process is from Ge with a dose of 10^{15}. From the UT-MARLOWE simulation, the channel is completely amorphized. The mobility extracted from Ge-damaged devices show less degradation than that of Si implanted devices with lower damage levels. The mobility is higher than the universal mobility of CZ devices, which indicates that there is still some strain left in the Si layer.

3.5 Mobility Degradation Mechanisms

Ion implantation and thermal processes are shown to degrade the mobility in the strained Si MOSFETs. Three mechanisms might be responsible for the degradation: strain relaxation due to misfit dislocations nucleation and propagation, residual ion

implantation damage and Ge out-diffusion into the Si cap layer. To verify the potential explanations above, materials analysis was performed. Cross section TEM was used to see the implant damage and misfit dislocations in the layers. SIMS (secondary ion mass spectrometry) was used to obtain Ge diffusion profiles.

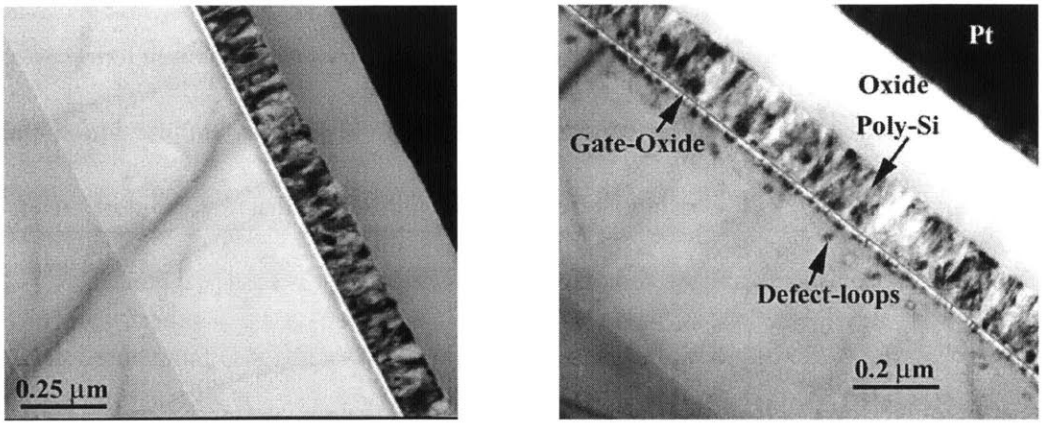


Figure 3-14 Cross section TEM pictures for strained Si devices with RTA1 (1000°C for 1 sec) and Si implants, for (a) devices with no implant, and (b) devices with Si implant Φ 4 (dose 5 x 10^{14} cm^{-2}). TEM courtesy of D. H. Anjum at the University of Virginia.

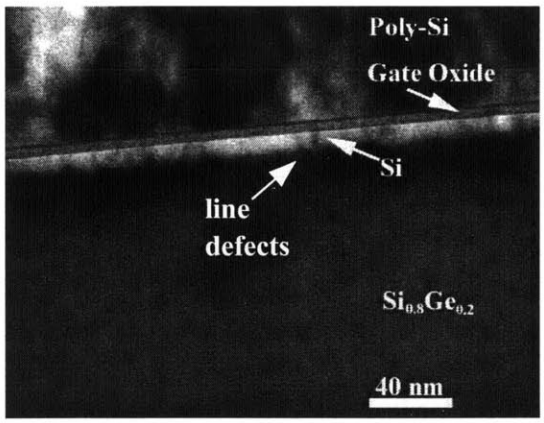


Figure 3-15 Cross-section TEM pictures for strained Si devices with RTA1 (1000°C for 1 sec) and Si implant ϕ4 (dose 5 x 10^{14}). This is an image of higher magnification taken on the same sample as shown in 3-14 (b). TEM courtesy of D. H. Anjum at University of Virginia.

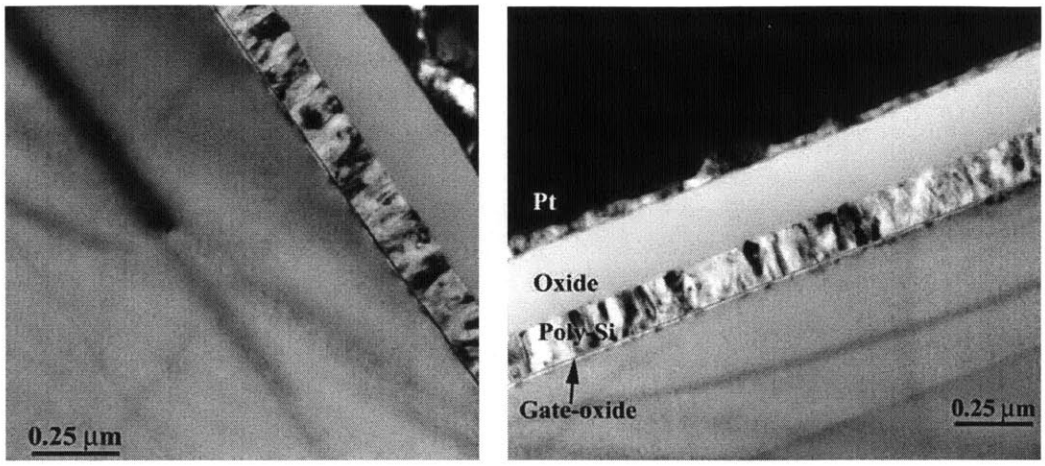


Figure 3-16 Cross-section TEM pictures for strained Si devices with RTA2 (1000°C for 10 sec) and Si implants for (a) devices with Si implant $\phi 2$ (dose 2.7 x 10^{13} cm^{-2}), and (b) devices with Si implant $\phi 4$ (dose 5 x 10^{14}). TEM courtesy of D. H. Anjum at University of Virginia.

For devices without implantation, no damage is observed in the channel as in Figure 3-14 (a). For devices with the highest Si implant dose $\Phi 4$ (5 x 10^{14}) and RTA1 (1000°C 1 sec), implantation damage such as defect loops and dislocations are clearly seen in Figure 3-14 (b) and 3-15. The amount of residual damage depends on the thermal budget. The residual damage is less for devices with RTA2 (1000°C 10 sec) than those with RTA1 (1000°C 1 sec), which means that longer RTA time anneals out implantation damage, as seen in Figure 3-14 (b) and 3-16 (b). For devices with RTA2 (1000°C 10 sec), the residual damage of devices with implant dose 2.7 x 10^{13} cm^{-2} and 5 x 10^{14} cm^{-2} are very similar (Figure 3-16). Figure 3-17 shows the cross-section TEM images of the devices that have been Ge implanted. The amount of residual damage is consistent with the mobility data. The more

residual damage present in the Si channel, the lower the mobility. Therefore, residual implantation damage is one of the mechanisms for mobility degradation seen in this work.

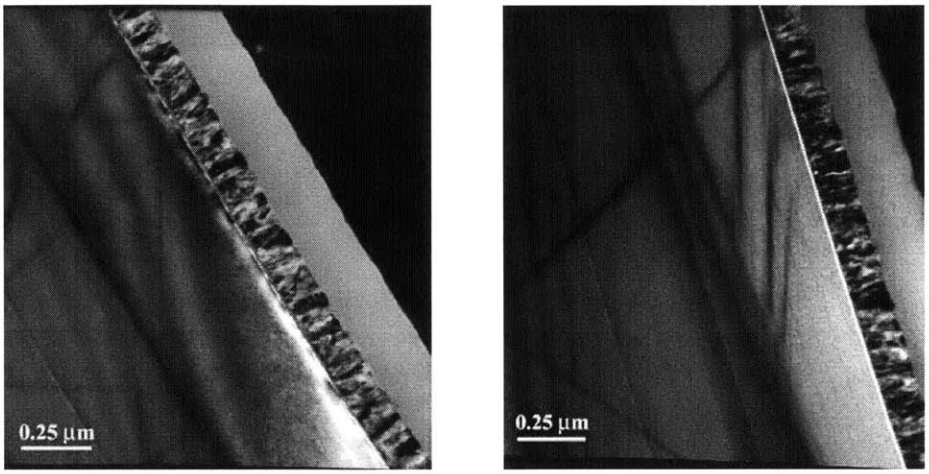


Figure 3-17 Cross-section TEM pictures for strained Si devices with RTA1 (1000°C for 1 sec) and Ge implants for (a) devices with Ge implant ϕ5 (dose 3 x 10^{13} cm^{-2}), and (b) devices with Ge implant ϕ6 (dose 1 x 10^{15}). TEM courtesy of D. H. Anjum at University of Virginia.

In this work, it is seen that a high thermal budget in itself, without implantation, does not degrade the mobility. This agrees with the experimental work by Currie *et al.* [31], where strained Si MOSFETs were fabricated on $Si_{0.7}Ge_{0.3}$ virtual substrates and annealed at 1000°C for 1-30 sec. With no implantation damage in the channel, the mobility enhancement factor is seen to degrade from 1.7X for devices with 1000°C 1 sec RTA to 1.6X for those with 1000°C 10 sec anneal. In section 3.4, the mobility of devices with RTA2 (1000°C 10 sec) seems to reach a plateau with the increasing dose (Figure 3-13 (a)), which means the mobility is independent of the implant doses. One possible explanation is that in RTA2 Ge diffusion becomes the

dominant mechanism for mobility degradation. To verify this hypothesis, SIMS technique was used to obtain Ge profiles in the devices with both RTA1 and RTA2.

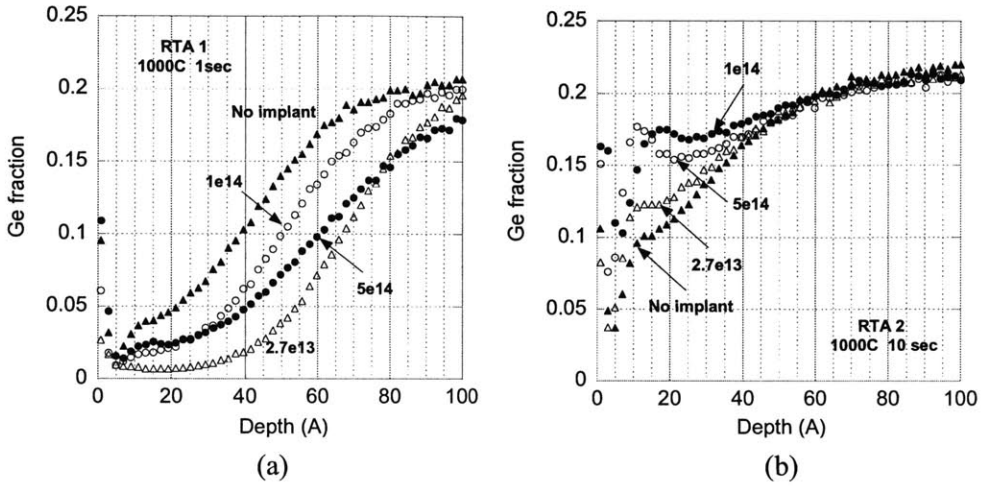


Figure 3-18 SIMS profiles of Ge in strained Si substrates for (a) epi substrate with RTA1 (1000°C 1 sec), and (b) epi substrate with RTA2 (1000°C 10 sec).

Figure 3-18 shows the Ge profiles in the first 100 Å of the strained Si substrates. The first 10~20 Å should be ignored due to SIMS artifacts and the native oxide formation. Moreover, the thickness variation on the strained Si epitaxial layer across the wafer will cause the Ge profiles to shift within roughly 20 Å. This apparently random shifting effect in the profiles should not be treated as Ge diffusion. An example is Figure 3-18 (a) where the Ge profile in the un-implanted substrate seems to diffuse more. If we look more closely, the Ge profiles of no implant, 2.7 x 10^{13}, and 1 x 10^{14} cm^{-2} have the same shape. These profiles will overlap if we shift them by 10 to 20 Å. Therefore, this should be considered as the result of thickness variation rather than Ge diffusion. Comparison between Figure 3-18 (a) and (b) clearly shows that Ge diffuses more in the epi substrate with RTA2 (1000°C 10 sec) than that with RTA1 (1000°C 1 sec). The Ge concentration near the surface is

around 12 to 17 atomic % for substrates with the longer RTA (1000°C 10 sec), while the Ge concentration for substrates with short RTA (1000°C 1 sec) is less than 5 atomic % and within the sensitivity of this particular profiling analysis. The difference in Ge concentration cannot be used to explain the dramatic mobility degradation for devices with high implant damage.

In Figure 3-18 (b), the Ge profile with no implant is shown with solid triangles. No mobility degradation is seen for this sample without implant. The Ge profile shown with open triangles is from the sample that was implanted with 2.7×10^{13} cm^{-2} Si, the mobility enhancement factor of which is degraded from 1.6X to 1.2X at 0.7 MV/cm. The Ge concentration difference of these 2 curves is only a 2 to 3 atomic %, which cannot explain the difference in mobility between these samples. Ge concentration difference among those samples with similar mobility degradation (open triangles for 2.7×10^{13} cm^{-2}, solid circles for 1×10^{14} cm^{-2} and open circles for 5×10^{14} cm^{-2}) is about 5%.

In Figure 3-18 (a), the Ge concentration near surface is about 5 atomic % and much less than the 12 to 17 atomic % observed in (b). However, the mobility degradation is still observed in these low Ge diffusion devices. Therefore, we can conclude that Ge out diffusion does occur with longer RTAs, but it is not the key mechanism to explain the mobility degradation observed in this particular experiment.

The third hypothesis to explain the observed mobility results is strain relaxation by misfit dislocation formation, due to ion implantation damage and thermal processing. Ion implantation damage is shown to enhance the strain relaxation in

$Si/Ge_xSi_{1-x}/Si$ heterostructures by increasing dislocation nucleation probability due to high point-defect concentrations arising from implantation [32]. The evidence of strain relaxation in the electronic measurement is that for all the mobility curves with degradation, the amount of mobility degradation is consistent throughout the E_{eff} range. This suggests that all the three mobility terms, Coulomb, phonon, and surface roughness scattering are affected, which is usually a result of strain relaxation. In the cross-section TEM images, line defects are present in the devices with degraded mobility. The amount of strain relaxation can be calculated from the average spacing of misfit dislocations present in the strained Si layer in TEM images. 70% strain relaxation is estimated for the strained Si layer with 5 x 10^{14} cm^{-2} Si implant and 1000C 1 sec RTA. The mobility enhancement factor of the devices under the same condition is degraded from 1.6X to 1X. 25% strain relaxation is estimated for the strained Si layers with 2.7 x 10^{13}, and 5 x 10^{14} cm^{-2} Si implant and 1000C 10 sec RTA, the mobility enhancement factors of which are both 1.2X. For high dose implant such as 5 x 10^{14} cm^{-2} Si, the mobility seems to recover for longer RTA (i.e. 10 second RTA compared to 1 second). This is because more damage is annealed in longer RTA, as observed by XTEM. There are no misfit dislocations observed in the strained Si layer with no implant. Therefore, strain relaxation by misfit dislocation formation is considered to be the major mechanism of mobility degradation introduced by ion implantation and thermal processing in this experiment.

3.6 Impact on Technology

As, P and B are widely used in current CMOS technology. The typical dose used for P channel implants is about 5 x 10^{13} cm^{-2}, at 30keV, and for B a typical channel dose is about 1 x 10^{14} cm^{-2}. For S/D implants, the typical dose used for As and B is about 1 x 10^{15} cm^{-2} or larger. The critical doses for P, B and As estimated in this work are 4 x 10^{12}~3 x 10^{13} cm^{-2}, 7 x 10^{13}~5 x 10^{14} cm^{-2}, and 1 x 10^{13} cm^{-2}. The critical doses will change with the thermal budgets. Typical P and B doses are close to the critical doses found in this work. Therefore thermal budgets and the implant doses should be carefully designed to avoid mobility degradation. The typical arsenic (As) S/D implants dose is 2 orders of magnitude larger than the critical dose found in this work. In the fabrication of strained Si MOSFETs, it is very likely that As implants will degrade the mobility in the S/D region. Since the S/D implant damage will extend laterally a certain distance, in short channel devices where the lateral damage due to the S/D extension is a proportionally large part of the channel length, the mobility degradation may extend into the channel region itself. In this case the mobility degradation due to implantation damage becomes a larger problem. Ion implantation dose and thermal budget should be both kept low to reduce the effect.

CHAPTER 4 Summary and Future Work

4.1 Thesis Summary

Two different aspects of mobility enhancement in strained Si *n*-MOSFETs have been explored in this work. The first study investigates the impact of strain on the various mobility limiting mechanisms. Temperature dependent measurements and modeling of the effective electron mobility in surface channel, strained Si *n*-MOSFETs is reported. Mobility measurements were taken from 30 K to 300 K. A three-term model was used to fit the data and extract the various mobility terms. Surface-roughness limited mobility of strained Si *n*-MOSFETs is shown to be enhanced by the introduction of strain and have the same effective field dependence as that of unstrained Si *n*-MOSFETs. The results suggest that surface-specific mechanisms may be involved in the strain-induced electron mobility enhancement, which persists to high vertical effective field.

The second part of this work investigates the influencing processing factors on mobility enhancement, particularly the impact of ion implantation damage and thermal budget. Long channel MOSFETs were fabricated on both CZ Si wafers and strained Si/relaxed $Si_{0.8}Ge_{0.2}$ heterostructures. Neutral Si and Ge were implanted into the channel in six different doses ranging from 4×10^{12} cm^{-2} to 1×10^{15} atoms/cm^2, in order to avoid scattering by ionized dopant impurities. Three different

rapid thermal anneals (RTA) were used. It is shown that the mobility enhancement factor is degraded by ion implantation and RTA. For each RTA condition, there is a threshold implantation dose, above which the strained Si mobility starts to degrade significantly. The threshold dose is smaller for devices with higher thermal budget. The degradation is larger for devices with higher implantation doses or larger thermal budgets. Two mechanisms are found to be involved in the mobility degradation introduced by ion implantation and thermal processing in this work: strain relaxation due to misfit dislocations and residual ion implantation damage in the strained Si channel.

4.2 Suggestions for Future Work

In this work, the effect of ion implantation damage and thermal processing on strained Si *n*-MOSFET with the strained Si layer thicknesses above the critical thickness was investigated. When the strained Si layer thickness is below the critical thickness, misfit dislocations formation is not energetically favorable. In that case, ion implantation and thermal processing may have less impact on the performance of the strained Si MOSFETs. This is an important topic for future investigation.

Low temperature measurement is a useful technique to understand the band structure, strained Si thickness, and scattering mechanisms. To further investigate the impact of surface roughness scattering on strained Si MOSFETs, detailed studies of the interface between strained Si and silicon dioxide are required.

Appendix A Example of Source Code for Electron Mobility Calculation.

1) Main Program used to calculate mobility:
filename: calcuH4_100a for wafer 420.7

```
% this program load IV, Cgc, Cgb data, calculate
% gm, Eeff, Qb, Qinv, tox, mobility etc
% x is the concentration of Ge
% the reason why this code is called long is because this one
% give Qb a value and compare that to universal
close all;
clear all;

readme=[
'|   Ion implant damage projetc                                    |'
'|   Temperature =   300 K:                                         |'
'|   Uses C-V for Qinv, Cmin is the cross point              |']
testID='---- 420.7 die H4 100a'

esi=11.9;   eox=3.9; e0=8.854e-12; ege=16; q=1.6e-19; dV=0.05;
%%%%%%%%%%%%%%%% constant, see thesis P89
x=0.2; % for CZ wafer
ealloy=(x*ege+(1-x)*esi)*e0;
% all the parameters are defined in SI
Na=2.5e17;

w=100e-6;
l=100e-6; % SI
%w = input('What is the gate width, w, in micrometers? ')*1E-6;
%l = input('What is the gate length, l, in micrometers? ')*1E-6;
load R2.txt; % IV
load RC14.txt; % the Cgc file
load RC15.txt; % Cgb file
IVfile=R2;
Cgcfile=RC14;
Cgbfile=RC15;
V=[-1:0.05:2];
```

```
%%%% above parameters may need to change for different devices and wafers
%%%%
dl=length(V);
x=[-0.025:0.01:0.025];
Vd=[-3e-2:0.01:0.03];
% 7 curves this time

for i=1:length(x)+1
    ID(:,i)=IVfile((dl*i-(dl-1)):i*dl,3);
    %Id is the 3th column in the data file
end

for i=1:length(x)
    g(:,i)=(ID(:,i+1)-ID(:,i))/0.01;
end

for i=1:length(V)
    %y=ID(i,:);
    %gd(i)=(sum(y)*sum(Vd)-y*Vd')/(sum(Vd)^2-Vd*Vd');
    value=polyfit(x,g(i,:),1);
    gd(i)=value(2);
    if i<=20
        gd(i)=0;
    end
end
% use polyfit to get gd

% caculate gm
for i=1:length(Vd)
    temp(1,i)=0;
    temp(2:dl,i)=ID(1:(dl-1),i);
    gm(:,i)=(ID(:,i)-temp(:,i))/dV;
end

dispiv(testID,V,ID,gd,gm,w,l);

%%%%%%%%%%%%%CV characteristics below
%%%%%%%%%%%%%%%%%%%%

Vgatei=Cgcfile(:,1);
t1=Cgcfile(1:12,2);
Cgc=(Cgcfile(:,2)-sum(t1)/12)/w/l*1e8;
%%%%%%%%%%%%%%%%%%% move Cgc to zero
% Cgc in F
```

```
[y,I]=max(Cgc);
for i=1:length(Cgc)
    if (Cgc(i)<0)
        Cgc(i)=0;
    end
    % offset Cgc to zero

    %if (i>I)
      % Cgc(i)=y;
    %end
    % correction for poly-depletion
end

Vgateb=Cgbfile(:,1);
t2=Cgbfile((length(Vgateb)-6):length(Vgateb),2);
for i=1:length(Vgateb);
    Cgb(i)=(Cgbfile(i,2)-sum(t2)/7)/w/l*1e8;
     %%%%%%%%%% Cgb is in F
end

% Cgc, Cgb are the capacitance per area, pF/cm2, F/m2=1e8pF/cm2

Vmi=-1:dV:1;
if min(Vgateb)==-2
     temp1=20;
end

if min(Vgateb)==-3
     temp1=40;
end

for i=1:length(Vmi)
    Ct(i)=Cgb(temp1+i)+Cgc(i); %%%%%%%%
end

%********* Visually find Cmin from Cgb

done='n';
one=ones(1,41);
figure;
while done == 'n',
    Cmin = input('What is the Cmin in pf? ')/w/l*1e8*1e-12;
    % change Cmin from pf to F/cm2 by *1e-12
```

```
    plot(Vgatei,Cgc*w*l*1e-8,'r',Vgateb,Cgb*w*l*1e-8,'b',Vmi,Ct*w*l*1e-8,'k',[-1:
0.1:3],Cmin*w*l*1e-8*ones(1,41),'-');
    title(['Cgc/Cgb/C vs Vg    ',testID]);
    legend('Cgc','Cgb','Ctotal');
    xlabel('Vg    (V)');
    ylabel('C F');
    grid on;
     done = input('Done? ','s');
end;

disp('Cmin= (pF)');
disp(Cmin*w*l*1e4);
Vt = input('What is Vt? ');


figure;
plot(Vgatei,Cgcfile(:,2),'r',Vgateb,Cgbfile(:,2),'b');
legend('Cgc','Cgb');
xlabel('Vg    (V)');
ylabel('C F');
title(['raw data Cgc, Cgb    ',testID]);
grid on;


figure;
plot(Vgatei,Cgc,'r',Vgateb,Cgb,'b',Vmi,Ct,'k');
title(['Cgc/Cgb/C per area vs Vg    ',testID]);
xlabel('Vg    (V)');
ylabel('C pF/cm2');
legend('Cgc','Cgb','Ctotal');
% plot Cgc vs Vgatei and Cgb vs Vgateb;
% F/m2=1e8pF/cm2
grid on;

%%%%%%%%%%%%%%%%%%%%%%      Qinv
%%%%%%%%%%%%%%%%%%%%%%

Qinv(1)=0;
for i=2:length(Cgc)
    Qinv(i)=Qinv(i-1)+(Cgc(i)+Cgc(i-1))*1e-8*dV/2; % in SI
end

Cox=max(Cgc);
% how to do the average of the curve???
```

```
tox=eox*e0/(Cox*1e-8);
Cd=Cmin*Cox/(Cox-Cmin);
Xd=ealloy/(Cd*1e-8); % here I use the esi*e0, Xd in SI
Qb=Na*Xd*1e6*q;   % ******* doping is about 1e17cm-3, change that into
Qb**********

for i=1:1:dl %%%%%%%
    Eeff(i)=(Qb+Qinv(i)/2)*1e-8/(ealloy);
    % the relative dielectric constant, use ealloy
end
%MV/cm=1e8V/m

%%%%%%%%%% Qb part in file Qb.m %%%%%%%%%%
for i=18:dl
     if Qinv(i)/q*1e-4 >5e10
    Ueff(i)=l*gd(i)/w/Qinv(i)*1e4;
     else
     Ueff(i)=0;
     end
end

% note Qinv(i)=0, not taken into account;
% m2/V/s=1e4 cm2/v/s

for i=1:dl
    Ufe(i,:)=(l/w/(Cox*1e-8))*(gm(i,:)./Vd)*1e4;
end
% m^2/V/s=1e4cm^2/v/s

plot0(V,Eeff,testID,Qinv,Ueff, Ufe,Vgatei,q);
compareU(Eeff,Ueff,testID);
readme
fprintf('Vt=   %6.2f (V)\n',Vt);
fprintf('Na=   %6.2e \n',Na);
dispall(Cmin,w,l,Cox,gd,gm,Xd,tox,Qinv,q,Qb,Ueff,Eeff,testID,Vt);


for n=1:20
     Ctot(n)=Cgb(n);
end
for n=21:length(Cgb)
     Ctot(n)=Cgb(n)+Cgc(n-20);
end
```

```
Ctot=Ctot'.*1e-4;
figure;
plot(Vgateb,Ctot);
title('Ctot vs Vgate in pF');
grid;

save Ctot.txt Ctot -ASCII;
```

2) Program used to plot figures:

```
function plot0(V,Eeff,testID,Qinv,Ueff, Ufe,Vgatei,q)

figure;
plot(V,Eeff);
title(['Eeff vs Vg    ',testID]);
xlabel('Vg    (V)');
ylabel('Eeff    (MV/cm)');
grid on;


figure;
plot(Qinv/q*1e-4,Ueff,Qinv/q*1e-4,Ufe);
grid on;
title(['Ueff and Ufe vs Qinv    ',testID]);
ylabel('Ueff Ufe cm^2/v/s    ');
xlabel('Qinv carriers/cm2 ');
%legend('Ueff','@ Vds=-20mV','@ Vds=-10mV','@ Vds=0mV','@ Vds=10mV','@
Vds=20mV');

figure;
plot(V,Ueff,V,Ufe);
grid on;
title(['Ueff and Ufe vs Vgate    ',testID]);
ylabel('Ueff Ufe cm^2/v/s    ');
xlabel('Vg V ');
%legend('Ueff','@ Vds=-20mV','@ Vds=-10mV','@ Vds=0mV','@ Vds=10mV','@
Vds=20mV');


figure;
plot(Vgatei,Qinv/q*1e-4);
title(['Qinv vs V      ',testID]);
% do the integration, plot Qinv vs Vgatei;
xlabel('Vg    (V)');
```

```
ylabel('Qinv carriers/cm2');
grid on;


figure;
plot(Qinv/q*1e-4,Ueff,'*');
grid on;
title(['Ueff vs Qinv    ',testID]);
ylabel('Ueff cm^2/v/s    ');
xlabel('Qinv carriers/cm2 ');

figure;
plot(Qinv/q*1e-4,Ufe);
grid on;
title([' Ufe vs Qinv    ',testID]);
ylabel(' Ufe cm^2/v/s    ');
xlabel('Qinv carriers/cm2 ');

figure;
plot(Eeff,Ueff);
title(['Ueff vs Eeff    ',testID]);
ylabel('Ueff cm^2/v/s    ');
xlabel('Eeff    (MV/cm)');
grid on;

figure;
plot(Eeff,Ufe);
legend('@ Vds=-30mV','@ Vds=-20mV','@ Vds=-10mV','@ Vds=0mV','@
Vds=10mV','@ Vds=20mV','@ Vds=30mV');
title(['Ufe vs Eeff    ',testID]);
ylabel('Ufe cm^2/v/s    ');
xlabel('Eeff    (MV/cm)');
grid on;

figure;
plot(Eeff,Ueff,'k',Eeff,Ufe);
title(['Ueff and Ufe vs Eeff    ',testID]);
legend('Ueff');
%legend('Ueff','@ Vds=-20mV','@ Vds=-10mV','@ Vds=0mV','@ Vds=10mV','@
Vds=20mV');
ylabel('Ueff cm^2/v/s    ');
xlabel('Eeff    (MV/cm)');
grid on;
```

3) Program used to display the key results:

```
function dispall(Cmin,w,l,Cox,gd,gm,Xd,tox,Qinv,q,Qb,Ueff,Eeff,testID,Vt)

fprintf(testID);
fprintf('\nCmin= %6.2f (pF) \n',Cmin*w*l*1e4);
fprintf('Cox/area= %6.2e (F/cm2)   \n',Cox);
fprintf('max(gd)= %6.2e(S)   \n',max(gd)/(w/l));
fprintf('max(gm)= %6.2e(S)    \n',max(gm(:,5))/(w/l));
fprintf('Xd= %6.2f (A)   \n',Xd*1e10);
fprintf('tox= %6.2f (A)   \n',tox*1e10);
fprintf('maxQi= %6.2e(carriers/cm2)   \n',max(Qinv)/q*1e-4);
fprintf('Qb= %6.2e(carriers/cm2)   \n',Qb/q*1e-4);
fprintf('max Ueff= %6.2f(cm2/v sec)   \n',max(Ueff));


fid = fopen('output.txt','w');
fprintf(fid,testID);
fprintf(fid,'\nCmin= %6.2f (pF) \n',Cmin*w*l*1e4);
fprintf(fid,'Cox/area= %6.2e (F/cm2)   \n',Cox);
fprintf(fid,'max(gd)= %6.2e(S)   \n',max(gd)/(w/l));
fprintf(fid,'max(gm)= %6.2e(S)    \n',max(gm(:,5))/(w/l));
fprintf(fid,'Xd= %6.2f (A)   \n',Xd*1e10);
fprintf(fid,'tox= %6.2f (A)   \n',tox*1e10);
fprintf(fid,'maxQi= %6.2e(carriers/cm2)   \n',max(Qinv)/q*1e-4);
fprintf(fid,'Qb= %6.2e(carriers/cm2)   \n',Qb/q*1e-4);
fprintf(fid,'max Ueff= %6.2f(cm2/v sec)   \n',max(Ueff));
fprintf(fid,'Vt= %6.2f(V)   \n',Vt);

fclose(fid)



Ueff1=Ueff';
save mobility.txt Ueff1 -ASCII;
Eeff1=Eeff';
save Eeff.txt Eeff1 -ASCII;
Qinv1=Qinv'/q*1e-4;
save Qinv.txt Qinv1 -ASCII;
gd1=gd';
save gd.txt gd1 -ASCII;
```

% save the mobility result to the result folder, all the vables to its own directory

Appendix B Fabrication Steps of Strained Si *n*-MOSFETs.

Implant splits:

1) **4 Si implant splits ranging from 4e12 to 5e14 cm $^{-2}$**
2) **2 Ge implant splits ranging from 4e12 to 5e14 cm $^{-2}$**
3) **no implantation**

RTA splits:

1) **1000°C for 1 secs**
2) **1000°C for 10 secs**
3) **950°C for 10 secs**

wafer splits:

1) **10 strained Si wafers**
2) **9 CZ control wafers**

Reoxidation splits:

1) wafer 420.10 has no reoxidatioin.

1) Zero Alignment Marks (etch 1-1.5 μm of Si/SiGe)

- Lithography: Mask CA
- AME5000 (recipe Hasansil- ~92 A/sec) to etch alignment marks
- Asher

2) Field ion implantation

- Lithography: Mask CF (block materials dies)
- ion implantation B11, dose 3e13 cm^{-2}, energy 25 keV, 7 degree tilt, 0 rotation

3) Field Oxide

- 2 p-cleans

- rca clean (SC1 substituted with p-clean)
- LTO deposition (~3000 A)
- Lithography: MASK CD to open active area (clear materials dies)
- AME5000 etch (HASANFOX ~20 A/sec) to dry etch ~2500Å LTO
- Image the LTO using the SEM (NSL)
- Asher
- Wet etch 50:1 HF to etch ~1200Å LTO

4) Body Implants

- ion implantation splits- see implant splits

5) Gate Stack (45 A SiO_2/1500 A poly-Si)

- 45 A gate oxide: tube A1. rec 144, time 30mins
- 1500 A poly: tube A6 rec 461, T=25mins

6) Gate Etch

- Lithography (mask CP) (clear surface analysis and S/D blank die, leave poly on gate blank die)
- Etch poly-Si: AME50000 (rec: KEITH CP)
- Image gate etch and poly stringers (SEM)

7) Reoxidation

- rca clean
- 11mins at 800 ° C in dry O2 ambient. Rec: 800°C REOX

8) Deep S/D and poly-Si I/I

- use resist to block surface analysis dies
- 10 keV, 5e15 cm^{-2} Phosphorus, 0 tilt, 0 rotation (SIMS was used to check the P diffusion)

9) Clear backside

- Hardbake frontside with photoresist
- Etch 30Å reox/1500Å poly/45A gate oxide using BOE dip and AME5000 (rec Tony_LTO) to remove oxide and poly
- asher

10) RTA

- 2 p-clean
- RCA with no HF dip
- 3 RTA splits (rec: mg1000b and mg950)

11) Contact Cuts

- rca clean
- deposit ~2500 A LTO
- lithography (mask CC) (leave LTO on materials dies for metal etch)
- AME5000 (rec Hasanfox) to etch 1750Å LTO.
- remove remaining 1200 LTO wet etch 50:1 HF (overetch so that LTO on poly-Si is removed)
- asher

12) Metal Deposition and etch

- P-clean and HF dip (remove native oxide)
- 1000 A Ti/ 1 μm Al sputtering using ENDURA
- lithography (Mask CM) (clear materials dies)
- wet etch metal using PAN etch to remove Al and 50:1 BOE to remove Ti
- asher
- sinter in TRLtube A3, forming gas 35~40mins

Appendix C Example of Source Code for MEDICI Simulations of C-V.

Filename: SS20M.inp

```
$ this structure is for long channel Strained Si nMOSFET

assign   name=polydope  n.val=8e19
assign   name=welldope     n.val=3.7e17

$ physical dimensions
assign   name=Lgate n.val=100.0
assign   name=Lsd   n.val=9
$ source drain are too narrow to show up in the figures <0.1 um
assign   name=Tpoly n.val=0.150
assign   name=Tlto  n.val=0.025
assign   name=Tox   n.val=0.0046
assign   name=Tsi   n.val=0.200

$ tags
assign   name=xmin  n.val=-@Lgate/2-@Lsd
assign   name=xmax n.val=@Lgate/2+@Lsd
assign   name=ymin  n.val=-@Tox-@Tpoly
assign   name=ymax n.val=@Tsi

assign name=T.CAP   n.val=0.010
$ thickness of strained Si, 100Å
assign name=T.PCH   n.val=0.010
assign name=T.BOT   n.val=0.010

assign name=Y1      n.val=@T.CAP
assign name=Y2      n.val=@Y1+@T.PCH
assign name=Y3        n.val=@Y2+@T.BOT
$ ********************************************************** $

mesh RECTANGU smooth.k=1

$ lateral mesh
x.mesh  x.min=@xmin width=@Lsd h1=@Lsd/3 h2=@Lsd/36
x.mesh  width=@Lgate/4 h1=@Lsd/36 h2=@Lgate/10
x.mesh  width=@Lgate/4 h1=@Lgate/10 h2=@Lgate/10
x.mesh  width=@Lgate/4 h1=@Lgate/10 h2=@Lgate/10
```

```
x.mesh  width=@Lgate/4 h1=@Lgate/10 h2=@Lsd/36
x.mesh  width=@Lsd h1=@Lsd/36 h2=@Lsd/3

$ depth mesh
y.mesh  y.min=@ymin depth=@Tpoly h1=@Tpoly/3 h2=@Tox/2
y.mesh  depth=@Tox h1=@Tox/2
y.mesh  depth=@T.CAP h1=@Y1/25 h2=@Y1/25
y.mesh  depth=@T.PCH h1=@Y1/25 h2=@Y2/25
y.mesh   depth=@T.BOT h1=@Y2/25 h2=@Y3/25
y.mesh  y.max=@ymax h1=@Y3/25 h2=@Tsi/5

eliminate     columns
 +  x.min=@xmin x.max=-@Lgate/2 y.min=@ymin y.max=-@Tox
eliminate     columns
 +  x.min=@Lgate/2 x.max=@xmax y.min=@ymin y.max=-@Tox

eliminate     columns
 +  x.min=@xmin x.max=@xmax y.min=@ymax/2 y.max=@ymax

$ ********************************************************** $

$ left LTO and nitride
REGION     name=4 oxide
+    x.min=@xmin x.max=-@Lgate/2 y.min=-@Tox-@Tlto y.max=-@Tox
REGION     name=4 oxide
+    x.min=-@Lgate/2-@Tlto x.max=-@Lgate/2 y.min=@ymin y.max=-@Tox
REGION     name=5 nitride
+    x.min=@xmin x.max=-@Lgate/2-@Tlto y.min=@ymin y.max=-@Tox-@Tlto

$ right LTO and nitride
REGION     name=6 oxide
+    x.min=@Lgate/2 x.max=@xmax y.min=-@Tox-@Tlto y.max=-@Tox
REGION     name=6 oxide
+    x.min=@Lgate/2 x.max=@Lgate/2+@Tlto y.min=@ymin y.max=-@Tox
REGION     name=7 nitride
+    x.min=@Lgate/2+@Tlto x.max=@xmax y.min=@ymin y.max=-@Tox-@Tlto

$CAP
REGION name=CAP    sige
+ x.min=@xmin x.max=@xmax y.min=0 y.max=@Y1

$PCHANNEL
REGION name=PCHANNEL sige
+ x.min=@xmin x.max=@xmax y.min=@Y1 y.max=@Y2
```

```
$BOTCAP sige
REGION    name=BOTCAP sige
+ x.min=@xmin x.max=@xmax y.min=@Y2 y.max=@Y3

$BUFFER
REGION name=BUFFER sige
+ x.min=@xmin x.max=@xmax y.min=@Y3 y.max=@ymax

$ gate polysilicon
region    name=1 silicon   x.min=-@Lgate/2 x.max=@Lgate/2 y.min=@ymin
y.max=-@Tox

$ gate oxide
region    name=2 oxide     x.min=@xmin x.max=@xmax y.min=-@Tox y.max=0

$ ********************************************************** $

$ contacts
electrode name=drainx.min=@xmax-@Lsd/3 x.max=@xmax y.min=0 y.max=0

electrode name=gate  x.min=-@Lgate/2 x.max=@Lgate/2
+                y.min=@ymin y.max=@ymin+@Tpoly

electrode name=source     x.min=@xmin x.max=@xmin+@Lsd/3 y.min=0 y.max=0

electrode name=bulk bottom

$*************************************************************$
$ poly doping
$profile n-type region=1 uniform n.peak=@polydope

$body doping
profile p-type uniform n.peak=@welldope

$source doping
profile n-type    n.peak=1.700000e+20
+          y.min=0.000000e+00 y.max=0.000000e+00 y.char=1.65e-02
+          x.min=@xmin x.max=-@Lgate/2 x.char=0.5e-02

$drain doping
profile n-type    n.peak=1.700000e+20
+          y.min=0.000000e+00 y.max=0.000000e+00 y.char=1.65e-02
+          x.min=@Lgate/2 x.max=@xmax x.char=0.5e-02
```

```
contact  name=gate   n.polysi resistan=0
contact  name=bulk   neutral resistan=0

$relaxed- Si0.8Ge0.2
material sige
+    x.mole=0.2
+    permittivity=12.73
+    eg.model=0
+    affinity=4.05
+    eg300=1.06

$strained-Si on relaxed- Si0.8Ge0.2
material region=(CAP)
+    x.mole=0
+    permittivity=11.9
+    eg.model=0
+    affinity=4.05+0.126
+    eg300=1.06-0.126+0.126

$strained- Si0.2Ge0.8 on relaxed- Si0.8Ge0.2
material region=(PCHANNEL)
 +  x.mole=0.2
 +  permittivity=12.73
 +  eg.model=0
 +  affinity=4.05
 +  eg300=1.06

$strained-Si on relaxed- Si0.8Ge0.2
material region=(BOTCAP)
 +  x.mole=0.2
 +  permittivity=12.73
 +  eg.model=0
 +  affinity=4.05
 +  eg300=1.06

plot.2d grid boundary fill

plot.1d log doping x.start=0 y.start=0 x.end=0 y.end=0.1

plot.1d log doping x.start=@xmin y.start=0 x.end=@xmax y.end=0

plot.2d x.min=@xmin x.max=@xmax y.min=0 y.max=0.1
contour doping log min=-19 max=-17 del=.1 line=1 fill=false
```

```
plot.2d ^clear x.min=@xmin x.max=@xmax y.min=0 y.max=0.1
contour doping log min=16 max=20 del=.5 line=2 fill=false
```

References

[1] J. Welser, J. L. Hoyt, S. Takagi, and J. F. Gibbons, "Strain dependence of the performance enhancement in strained-Si n-MOSFETs," in *IEEE IEDM Tech. Dig.*, 1994, pp. 947.

[2] K. Rim, J. Welser, J. L. Hoyt, and J. F. Gibbons, "Enhanced hole mobilities in surface-channel strained-Si p-MOSFETs," in *IEEE IEDM Tech. Dig.*, 1995, pp. 1026.

[3] E. A. Fitzgerald, Y. H. Xie, D. Monroe, P. J. Silverman, J. M. Kuo, A. R. Kortan, F. A. Thiel, and B. E. Weir, "Relaxed Ge/sub x/Si/sub 1-x/ structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," *Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena)*, vol. 10, pp. 1807, 1992.

[4] K. Rim, J. L. Hoyt, and J. F. Gibbons, "Transconductance enhancement in deep submicron strained Si n-MOSFETs," in *IEEE IEDM Tech. Dig.*, 1998, pp. 707-710.

[5] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I — effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 2357-2362, Dec. 1994.

[6] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, D. A. Antoniadis, " Strained silicon MOSFETtechnology", in *IEEE IEDM Tech. Dig.*, 2002, pp. 23-26.

[7] T. Vogelsang and K. R. Hofmann, "Electron transport in strained Si layers on Si/sub 1-x/Ge/sub x/ substrates," Applied Physics Letters, vol. 63, pp. 186-8, 1993.

[8] C. G. Van de Walle and R. M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Physical Review B (Condensed Matter)*, vol. 34, pp. 5621-34, 1986.

[9] C. Zeller and G. Abstreiter, "Electric subbands in Si/SiGe strained layer superlattices," *Zeitschrift fur Physik B (Condensed Matter)*, vol. 64, pp. 137-43, 1986.

[10] M. V. Fischetti, F. Gámiz, and W. H?nsch, "On the enhancement electron mobility in strained-silicon inversion layers", *J. Appl. Phys.*, vol. 92, pp 7320-7324, Dec. 2002.

[11] K. Rim, S Narasimha, M. Longstreet, A. Mocuta, and J. Cai, "Low field mobility characteristics of sub-100 nm unstrained and strained Si MOSFETs", in *IEEE IEDM Tech. Dig.*, 2002, pp. 43-46.

[12] K. Rim, J. Chu, H. Chen, K.A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta, H. Zhu, R. Roy, J. Newbury, J. Ott, K. Petrarca, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd, M. Ieong, and H. -S. Wong, "Characteristics and device design of sub-100 nm strained Si N- and PMOSFETs," in *Proc. Symp. VLSI Technol.*, 2002, pp. 98–99.

[13] T. Mizuno, N. Sugiyama, A. Kurobe, and S. Takagi, "Advanced SOI p-MOSFETs with strained-Si channel on SiGe-on-insulator substrate fabricated by SIMOS technology," *IEEE Trans. Electron Devices*, vol. 48, pp. 1612-1618, Aug. 2001.

[14] Zhiyuan Cheng, Matthew T. Currie, Chris W. Leitz, Gianni Taraschi, and Eugene A. Fitzgerald, Judy L. Hoyt, and Dimitri. A. Antoniadis, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates", *IEEE Electron Device Lett.*, vol 22, issue 7, pp. 321 –323, July 2001.

[15] A. G. Sabnis and J. T. Clemens, "Characterization of the electron mobility in the inverted <100> Si surface," in *IEEE IEDM Tech. Dig.*, 1979, pp. 18.

[16] S. C. Sun and J. D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1497-508, 1980.

[17] J. Koomen, "Investigation of the MOST channel conductance in weak inversion," Solid-State Electronics, vol. 16, pp. 801-10, 1973

[18] C. L. Huang, J. V. Faricelli, and N. D. Arora, "A new technique for measuring MOSFET inversion layer mobility," *IEEE Trans. Electron Devices*, vol. 40, pp. 1134-9, 1993.

[19] H. M. Nayfeh, C.W. Leitz, A. J. Pitera, E. A. Fitzgerald, J. L. Hoyt, and D.A. Antoniadis, " Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs ", *IEEE Electron Device Lett.*, vol 24, pp. 248 -250. April 2003

[20] M. Rashed, W. K. Shih, S. Jallepalli, T. J. T. Kwan, and C. M. Maziar, "'Monte Carlo simulation of electron transport in strained Si/Si1-xGex n-MOSFETs", in *IEEE IEDM Tech. Dig.*, pp765 - 768, 1995.

[21] G. Mazzoni, A. L. Lacaita, L. M. Perron, A. Pirovano, "On surface roughness-limited mobility in highly doped n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 46, pp. 1423-1428, July 1999.

[22] D. Vasileska, D. K. Ferry, "Scaled Silicon MOSFET's: universal mobility behavior," *IEEE Trans. Electron Devices*, vol. 44, pp. 577-583, April 1997.

[23] J. Koga, S. Takagi, A. Toriumi, "A comprehensive study of MOSFET electron mobility in both weak and strong inversion regimes, " in *IEEE IEDM Tech. Dig.*, 1994, pp. 475-478.

[24] T. Yamanaka, S. J. Fang, H. Lin, J. P. Snyder and C. R. Helms, "Correlation between inversion layer mobility and surface roughness measured by AFM," *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 178-180, April 1996.

[25] N. Sugii, D. Hisamoto, K. Washio, N. Yokoyama, and S. Kimura, "Enhanced performance of strained strained-Si MOSFETs on CMP SiGe virtual substrate," in *IEEE IEDM Tech. Dig.*, 2001, pp. 737-740.

[26] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers. I. Misfit dislocations," *J. of Crystal Growth*, vol. 27, pp. 118-25, 1974.

[27] D. Misar, P. K. Swain, "Strain relaxation in SiGe due to process induced defects and their subsequent annealing behavior", *Microelectronics Reliability*, vol 38, pp. 1611-1619, 1998.

[28] D. C. Houghton, "Strain relaxation kinetics in Si/sub 1-x/Ge/sub x//Si heterostructures," *J. of Appl. Phys.*, vol. 70, pp. 2136-51, 1991.

[29] F. Schaffler, D. Tobben, H. J. Herzog, G. Abstreiter, and B. Hollander, "High-electron-mobility Si/SiGe heterostructures: influence of the relaxed SiGe buffer layer," *Semiconductor Science and Technology*, vol. 7, pp. 260-6, 1992.

[30] S. B. Samavedam, W. J. Taylor, J. M. Grant, J. A. Smith, P. J. Tobin, A. Dip, A. M. Phillips, and R. Liu, "Relaxation of strained Si layers grown on SiGe buffers" *J. Vac. Sci. Technol. B*, vol 17, pp. 1424-1429, July 1999.

[31] M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, "Carrier mobilities and process stability of strained Si n- and p-MOSFETs on SiGe virtual substrates," *J. Vac. Sci. Technol. B*, vol 19(6), pp. 2268-2279, Nov/Dec. 2001.

[32] R. Hull, J. C. Bean, J. M. Bonar, G. S. Higashi, K. T. Short, H. Temkin, and A. E. White, "Enhanced strain relaxation in Si/GexGe1-x/Si heterostructures via point-defects concentrations introduced by ion implantation," *Appl. Phys. Lett.*, vol 56(24), pp2445-2447, June 1990.

[33] B. Hollander, St. Lenk, S. Mantl, H. Trinkaus, D. Kirch, M. Luysberg, T. Hackbarth, H. J. Herzog, and P. F. P. Fichter, "Strain relaxation of pseudomorphic Si1-xGex/Si(100) heterostructures after hydrogen or helium ion implantation for virtual substrate fabrication," *Nucl. Instr. And Meth. in Phys. Res. B*, vol 175-177, pp357-367, 2001.

[34] P. M. Rousseau, P. B. Griffin, S. Luning, and J. D. Plummer, "A model for mobility degradation in highly doped arsenic layers," *IEEE Trans. Elec. Dev.*, vol 43, pp. 2025-2027, Nov. 1996.

[35] J. D. Plummer, M. D. Deal and P. B. Griffin, *Silicon VLSI Technology - Fundamentals, Practice and Modeling*, New Jersy: Prentice Hall, 2000, ch. 8.