Design of a Continuous-Time Bandpass Delta-Sigma Modulator

by

Xi Yang

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Abstract

An 8^{th}-order continuous-time (CT) bandpass delta-sigma ($\Delta\Sigma$) modulator has been designed and simulated in a 65 nm CMOS process. This modulator achieves in simulation 25 MHz signal bandwidth at 250 MHz center frequency with a signal-to-noise ratio (SNR) of 75.5 dB. The modulator samples at 1 GS/s while consuming 319 mW. On the system level, the feedback topology secures stability for the 8^{th}-order system, achieving a maximum stable input range of -1.9 dBFS. A 2.5-V/1.2-V dual-supply loop filter with a feed-forward coupling path has been proposed to suppress noise and distortion. On the transistor level, a 5^{th}-order dual-supply feed-forward operational amplifier (op amp) and a 4^{th}-order single-supply feed-forward op amp have been designed to enable high modulator linearity and coefficient accuracy.

Thesis Supervisor: Hae-Seung Lee
Title: Professor

Acknowledgments

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I would like to thank my friends, especially Qiannan, Xueting, Xiaoxing, Chen, and Yixiao for always being there and believing in me.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

With the advances of VLSI technology, computational and signal processing tasks are now predominantly performed by digital circuits that are fast, robust and highly integrated. However, signals from the real world are inherently analog. Therefore, analog-to-digital converters (ADCs) are required in many electronic systems to interface with the real world.

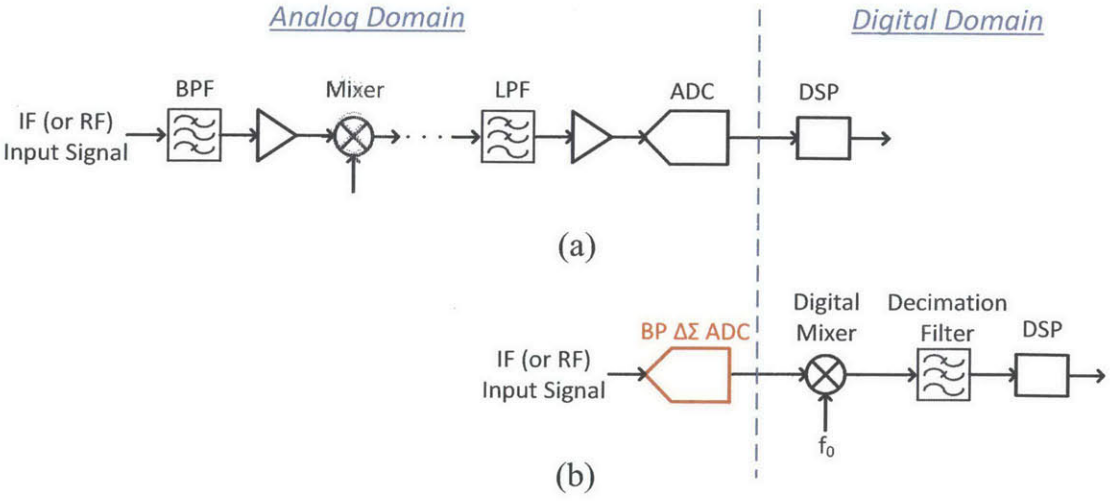


Figure 1-1: Signal processing chain of (a) a traditional and (b) a modern receiver system [1].

One important application of ADCs is in the receiver of communication systems. Figure 1-1(a) shows the signal processing chain of a traditional receiver. High-frequency narrow-band input signals are filtered, amplified, and down-converted repeatedly before finally being digitalized and sent to a digital signal processor (DSP) [1]. The signal processing procedures take place mainly in the analog domain, necessitating power-hungry components such as mixers, low-noise amplifiers (LNAs), and bandpass filters (BPFs).

In the modern receiver systems of today, we attempt to digitize the signal as early as possible, and place as many signal processing operations as possible in the digital domain, in order to take full advantage of technology scaling and software reconfigurability. Such a trend prefers a bandpass type of ADC, hence the bandpass delta-sigma ($\Delta\Sigma$) ADC.

A bandpass $\Delta\Sigma$ modulator digitizes narrow-band analog signals directly from the intermediate frequency (IF) or radio frequency (RF) without down-converting them to the baseband [1]. Figure 1-1(b) shows a receiver system that involves a bandpass $\Delta\Sigma$ ADC. The advantages of bandpass conversion include [1]: (a) the elimination of multiple stages of analog down-conversion and filtering, which leads to significant reduction in power consumption and improved modulator simplicity; (b) the spectral separation of signals from various low-frequency noise, distortion, and the DC offset, now that the signals are preserved at high frequency throughout the analog domain; and (c) more efficient analog-to-digital conversion, because only the in-band signals are digitized and no power is wasted on the conversion of unwanted signals between DC and the lower band-edge.

Today, the trend is towards software-defined radio (SDR) that allows for reconfigurable and multi-standard receivers. The flexibility in the receiver system leads to tough requirements for the ADCs. High speed is required to digitize the signal directly from the carrier frequency. Wide-band operation is needed to cover signal bands of different standards. To detect signals with enough accuracy in the presence of in-band interferers, a large dynamic range and high linearity are indispensable [7].

Continuous-time (CT) bandpass $\Delta\Sigma$ modulators provide a promising solution to

SDR. As is discussed in Chapter 2, CT bandpass $\Delta\Sigma$ modulators have the potential to operate at GHz sampling frequency , to handle signal bandwidth of tens of MHz, and is more power efficient than its discrete-time (DT) counterpart. By employing a large oversampling ratio and a high-order loop filter, a high resolution can also be achieved.

This thesis presents the design of a wide bandwidth, high carrier frequency, and high resolution CT bandpass $\Delta\Sigma$ modulator. The design is simulated with TSMC's 65 nm CMOS process. It achieves a signal bandwidth of 25 MHz and a signal-to-noise ratio (SNR) of 75.5 dB. The sampling rate is 1 GS/s and the center frequency 250 MHz. The modulator consumes a total static power of 319 mW, rendering a figure of merit (FoM) of 1.3 pJ/step. Equations 1.1 and 1.2 show the definitions of the FoM and the effective number of bits (ENOB) respectively, where f_B denotes the signal bandwidth, P the modulator power consumption, and SNDR the signal-to-noise-and-distortion ratio.

$$\text{FoM} = \frac{P}{2 \cdot 2^{\text{ENOB}} \cdot f_B} \tag{1.1}$$

$$\text{ENOB} = (\text{SNDR} - 1.76)/6.02 \tag{1.2}$$

1.2 Previous Work

As is introduced later in this thesis, a CT bandpass $\Delta\Sigma$ modulator consists of an analog loop filter, a coarse quantizer, and several digital-to-analog converters (DACs). The major challenge lies in the design of the loop filter, which is essentially a bandpass filter. In order for the modulator to achieve both wide bandwidth and high resolution, a low-power bandpass filter with high linearity around IF is required.

There are usually two ways to implement the bandpass loop filter. [8] and [9] employ active-RC resonators that realize loop filters of 4^{th}- and 6^{th}- order respectively. With a unique software-based calibration scheme that intends to compensate for PVT variations, [9] is able to achieve a SNDR of 68.4 dB over a bandwidth of 10 MHz. This performance, however, is not sufficient for modern software receiver systems. The loop

filter can also be realized with LC tanks, as is demonstrated in works [10], [11], and [12]. When the center frequency approaches GHz, LC resonators are preferred due to their high resonance frequency. However, the achieved SNDR is quite low.

In recent years, efforts have been made to improve the power efficiency of the modulator. [13] and [14] introduce a new type of RC resonator that requires only one operational amplifier (op amp). This halves the number of op amps in the loop filter and significantly reduces the power consumption. A duty-cycle controlled DAC is also introduced in [14], which halves the number of DACs and further decreases the power consumption. With a 6^{th}-order loop filter, [14] achieves a SNDR of 69 dB, a bandwidth of 25 MHz, and a FoM of only 0.317 pJ/step.

Another trend is towards greater reconfigurability. [3] introduces a design with a tunable center frequency from DC to 1 GHz, a bandwidth from 35 MHz to 150 MHz, and a sampling frequency from 2 GHz to 4 GHz. This tunability is enabled by employing both reconfigurable LC and active-RC resonators in the loop filter. However, the power consumption of this design is quite large.

Table 1.1 compares the performances of several recently reported CT bandpass $\Delta\Sigma$ modulators. For designs using active RC resonators, previous works have failed to achieve SNDR of over 70 dB when bandwidth exceeds 10 MHz. Besides, all the designs thus far are of 6^{th}-order or lower. This is partly because (a) it is difficult for high order modulators to maintain stability, and (b) the SNR-liming factors of the modulator are noise and distortion from the circuit rather than the order of noise-shaping.

In this design, since we are aiming to accomplish both wide bandwidth and high resolution, an aggressive 8^{th}-order topology is adopted. In order to ensure modulator stability at such a high order, a feedback topology is chosen and modified. A 2.5-V/1.2-V dual-supply loop filter with feed-forward coupling path is proposed to suppress noise and distortion from the circuit and to achieve a high SNR. Multistage feed-forward op amps are designed to achieve high modulator linearity and coefficient accuracy. Besides, we also seek to keep a moderate power consumption so that a FoM comparable to the state-of-the-art designs can be achieved.

Table 1.1: Performance summary of recently reported CT Bandpass $\Delta\Sigma$ modulators.

	Schreier 2006 [8]	Lu 2010 [9]	Thandri 2007 [10]	Chalvatzis 2007 [11]	Ryckaert 2009 [12]	Chae 2012 [13]	Chae 2013 [14]	Shibata 2012 [3]
Order	4^{th}	6^{th}	4^{th}	4^{th}	6^{th}	4^{th}	6^{th}	6^{th}
Resonator	Active-RC	Active-RC	LC	LC	LC	New RC	New RC	Active RC/LC
Process	.18 μm CMOS	.18 μm CMOS	.25 μm BiCMOS	.13 μm BiCMOS	90 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
IF [MHz]	44	200	950	2000	2400	200	180-220	0/450/ 1000
Fs [MHz]	264	800	3800	40000	3000	800	800	4000
BW [MHz]	8.5	10	0.2/1	60/120	60	24	25	150/100/ 75
SNDR [dB]	77	68.4	63/59	55/52	40	58	69	71/72/ 63
Power [mW]	375	160	75	1600	40	12	35	750/550/ 550
FoM [pJ/step]	3.81	3.72	162/51	29/20	4.08	0.385	0.317	0.86/0.85/ 3.18

1.3 Thesis Organization

This thesis is organized as follows:

Chapter 2 explains the basics of a CT bandpass $\Delta\Sigma$ modulator. The chapter begins with the introduction to the theory of $\Delta\Sigma$ modulation, with emphasis on two important signal processing techniques, namely oversampling and noise-shaping. The two types of $\Delta\Sigma$ modulators, DT and CT, are then described and compared. The impulse response matching method is introduced that relates CT and DT $\Delta\Sigma$ modulators. The chapter concludes with a general block diagram of a CT bandpass $\Delta\Sigma$ modulator.

Chapter 3 describes the system-level design procedures of the modulator. The desired specifications of the modulator are determined first, followed by the selection of a proper noise transfer function (NTF). Two modulator topologies, the feedback and the feed-forward, are then analyzed and compared. The feedback topology is chosen and modified for this design in order to meet the target specifications. The method of determining the various modulator coefficients is introduced later. Finally, the chapter concludes with a complete block diagram of the proposed CT bandpass $\Delta\Sigma$ modulator.

Chapter 4 and Chapter 5 describe the transistor-level implementation of the modulator. Chapter 4 focuses on the implementation of the loop filter. Two major design challenges, namely the op amp non-ideality and the thermal noise, are addressed examined. A dual-supply loop filter with a feed-forward coupling path is proposed as the solution. The design of the multi-stage feed-forward op amp is also described. Chapter 5 focuses on the implementation of the feedback paths. The design of the quantizer, the DAC driver, and DAC is analyzed and explained respectively.

Chapter 6 presents the simulation results of the proposed CT bandpass $\Delta\Sigma$ modulator. The system-level behavior of an ideal modulator is demonstrated first. The performances of the multi-stage feed-forward op amps are examined next. The transistor-level simulation results of the entire modulator are finally provided and discussed.

Chapter 7 concludes the thesis and makes suggestions for future work.

Chapter 2

Delta-Sigma Modulator Basics

This chapter introduces the basic operations of a $\Delta\Sigma$ modulator. A $\Delta\Sigma$ modulator consists of a loop filter and a coarse quantizer in feedback. Figure 2-1 shows the general block diagram of a $\Delta\Sigma$ modulator. In this chapter, we start from the basic analog-to-digital conversion. We then describe the principles of $\Delta\Sigma$ modulation, which rely on two important signal processing techniques, namely oversampling and noise-shaping. A comparison between DT and CT modulators comes next. The advantages of CT modulators are described and explained. An impulse response matching method, which relates DT and CT modulators, is also introduced. The chapter concludes with a general block diagram of a CT bandpass $\Delta\Sigma$ modulator that is further elaborated on in the following chapters.

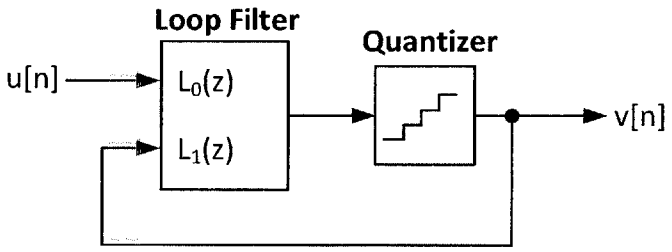


Figure 2-1: General block diagram of a DT $\Delta\Sigma$ modulator [1].

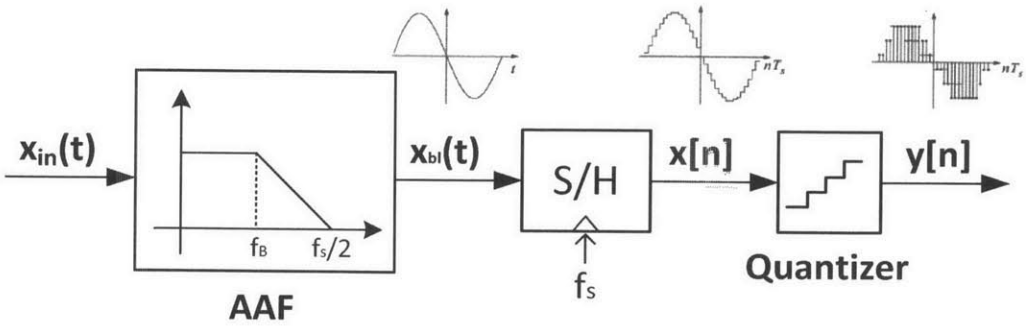


Figure 2-2: Block diagram of a Nyquist-rate ADC [2].

2.1 Analog-to-Digital Conversion

This section introduces the basic operations of an ADC. An ADC converts an analog signal, which is continuous in both amplitude and time, into a digital signal, which is discrete in both domains. Figure 2-2 shows the architecture of a typical ADC. It consists of an anti-aliasing filter (AAF), a sample-and-hold (S/H) circuit, and a quantizer.

The S/H circuit samples the analog input signal at the sampling frequency f_s. According to Nyquist sampling theorem, f_s must be at least twice the signal bandwidth, f_B, in order for the input signal to be reconstructed accurately from the sampled output [15]. Therefore, an AAF that bandlimits the input signal within $\frac{f_s}{2}$ must precede the S/H circuit. The minimum sampling rate, which is essentially twice the signal bandwidth, is referred to as the Nyquist rate f_N. An ADC that samples at f_N is called a Nyquist-rate ADC.

The quantizer breaks the continuity in amplitude by mapping the sampled signal $x[n]$ with a set of discrete references. The characteristic curve of a 7-level quantizer is shown in Figure 2-3(a). Δ refers to the difference between adjacent references. The full scale Y_{FS} refers to the difference between the lowest and highest reference levels. The input step size is called a least significant bit (LSB). Since the gain of the

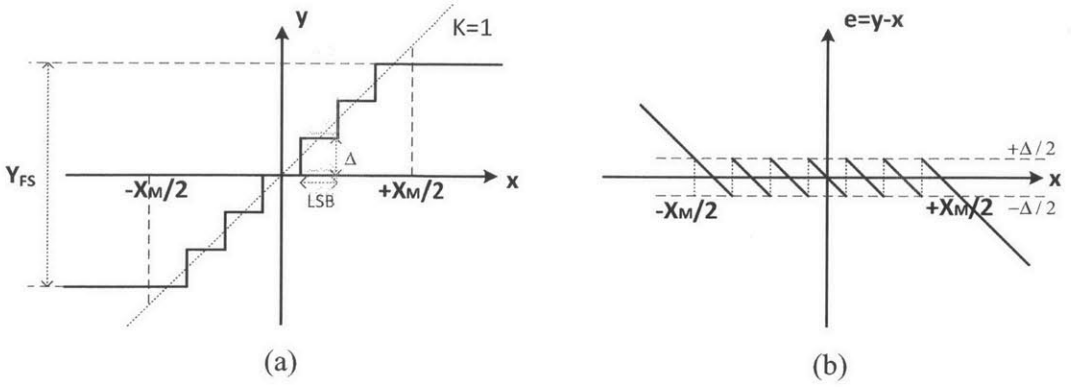


Figure 2-3: Characteristics of a 7-level quantizer: (a) transfer curve and (b) error function.

quantizer is 1, $\Delta = LSB$.

Quantization adds an error to the sampled signal. Figure 2-3(b) illustrates the relationship between the quantization error $e[n]$ and the input signal $x[n]$. Note that if $x[n]$ is within $[-\frac{X_M}{2}, +\frac{X_M}{2}]$, $e[n]$ is bounded within $\pm \frac{\Delta}{2}$. When $x[n]$ exceeds this range, the output signal $y[n]$ is clipped, and the absolute value of $e[n]$ increases monotonically with $x[n]$. This behavior is called overload. X_M is thus referred to as the no-overload input range. The relationship between Δ, X_M, Y_{FS}, and the number of quantization levels, M, and can be expressed as:

$$\Delta = \frac{X_M}{M} = \frac{Y_{FS}}{M-1} \tag{2.1}$$

It appears from Figure 2-3(b) that $e[n]$ has a strong dependence upon $x[n]$. In reality, however, $e[n]$ can be modeled as an additive uniformly-distributed white noise under the following assumptions [15]:

- the quantizer is not overloaded;
- Δ is sufficiently small compared to Y_{FS};
- $x[n]$ is large and busy enough that it traverses many quantization levels from sample to sample.

These assumptions are usually satisfied in practice to a reasonable degree. Fig-

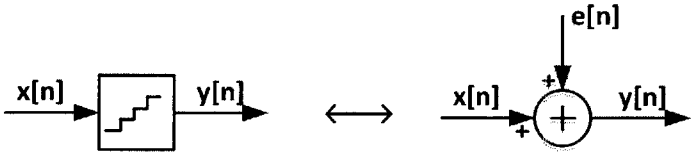


Figure 2-4: Linear model of the quantizer.

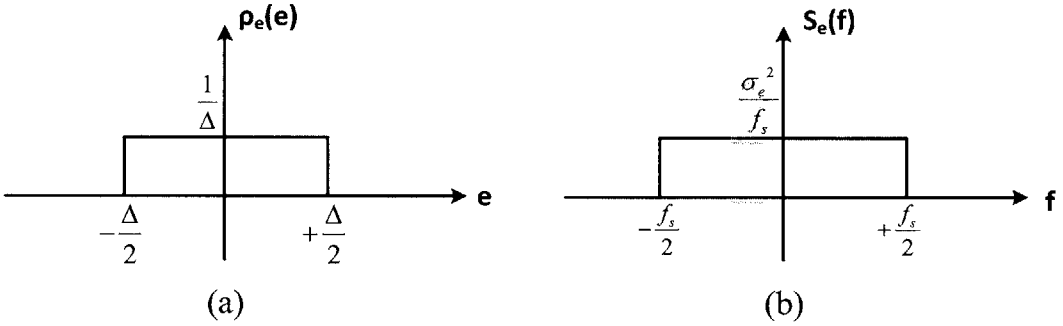


Figure 2-5: Characteristics of the quantization noise of a Nyquast-rate ADC: (a) probability density and (b) PSD.

ure 2-4 shows the linear model of the quantizer. Figure 2-5(a) plots the probability density of $e[n]$ that is uniform across $[-\frac{\Delta}{2}, +\frac{\Delta}{2}]$ with the value of $\frac{1}{\Delta}$. We can thus calculate the variance of $e[n]$ to be:

$$\sigma_e^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.2}$$

Under the white-noise assumption, the power spectrum density (PSD) of $e[n]$ is uniform across the signal band, as plotted in Figure 2-5(b). The noise power and PSD can be calculated as:

$$P_e = \sigma_e^2 = \frac{\Delta^2}{12} \tag{2.3}$$

$$S_e(f) = \frac{\sigma_e^2}{f_S} = \frac{\Delta^2}{12 f_S} \tag{2.4}$$

The signal-to-quantization-noise ratio (SQNR) for a full-scale sine wave input

signal can thus be calculated as:

$$\text{SQNR} = 10log\frac{P_{sig}}{P_e} = 10log\left(\frac{\frac{1}{2}\left(\frac{X_m}{2}\right)^2}{\frac{\Delta^2}{12}}\right) \tag{2.5}$$

Assuming the quantizer is N-bit, i.e. $M = 2^N$, and taking into consideration Equation 2.1, the SQNR can be written as follows:

$$\text{SQNR} = 10log\left(\frac{3}{2}M^2\right) = 6.02N + 1.76 \tag{2.6}$$

From this result we observe that, for a Nyquist-rate ADC, the only way to improve SQNR is to increase the number of quantization levels.

2.2 Delta-Sigma Modulation

A $\Delta\Sigma$ modulator is capable of a much higher SQNR than a Nyquist-rate ADC. The key of $\Delta\Sigma$ modulation lies in the combination of two signal processing techniques, oversampling and noise-shaping [2].

2.2.1 Oversampling

An oversampling ADC samples at a frequency higher than the Nyquist rate. The oversampling ratio (OSR) is defined as:

$$\text{OSR} = \frac{f_s}{f_N} = \frac{f_s}{2f_B} \tag{2.7}$$

Oversampling gives us two major benefits:

Relaxed AAF requirements According to Figure 2-6, an oversampling ADC no longer requires an AAF with sharp transition bands. This is because, for oversampling ADCs, $\frac{f_s}{2}$ is much larger than f_B.

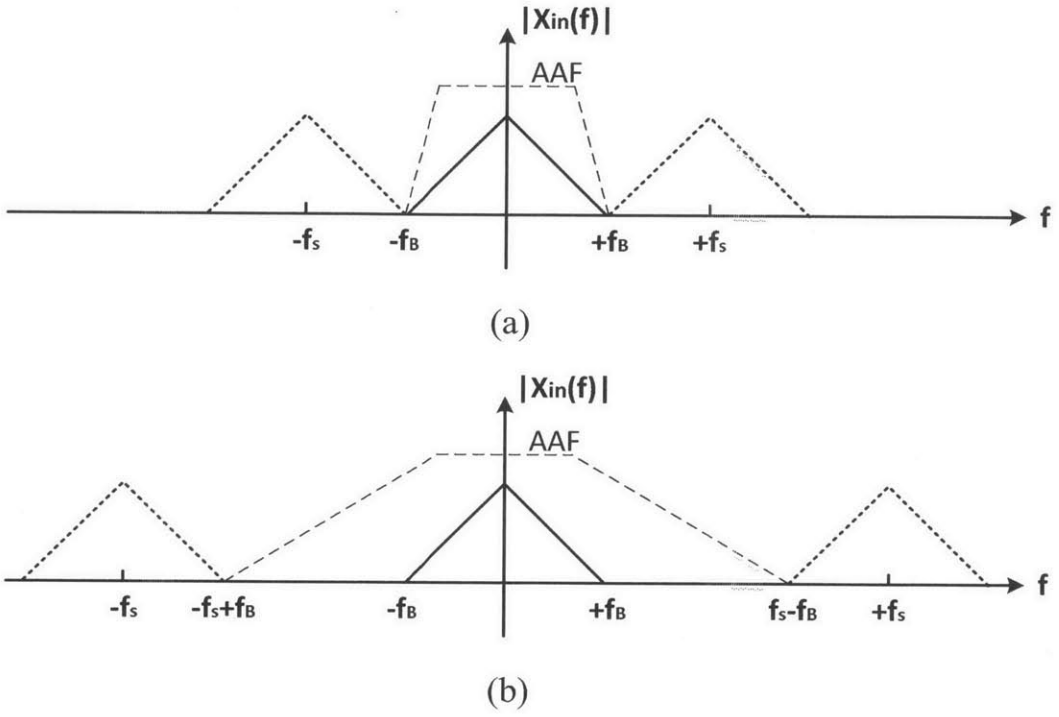


Figure 2-6: Anti-aliasing filters for (a) Nyquist-rate and (b) oversampling ADCs.

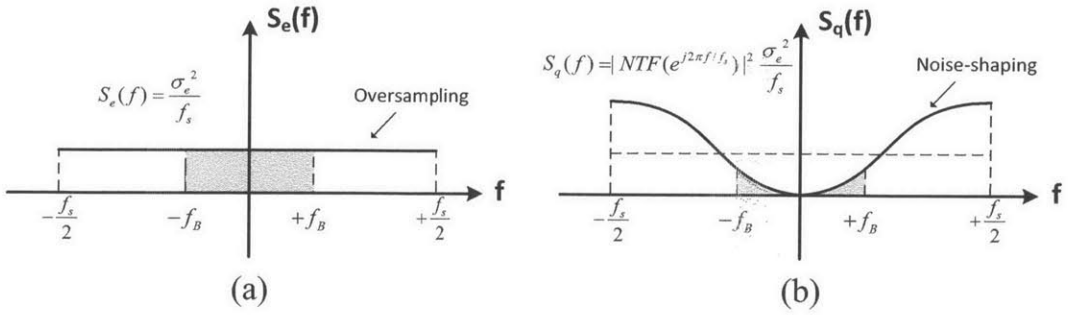


Figure 2-7: PSD of (a) oversampled and (b) shaped quantization noise.

Higher achievable SQNR For an oversampling ADC, the total noise power is still $P_e = \sigma_e^2 = \frac{\Delta^2}{12}$, and the PSD $S_e(f) = \frac{\sigma_e^2}{f_s} = \frac{\Delta^2}{12 f_s}$ across $[-\frac{f_s}{2}, +\frac{f_s}{2}]$, both of which are the same as those of a Nyquist-rate ADC. However, the in-band quantization noise, $P_{e,in-band}$, is now only a fraction of P_e, as is illustrated in Figure 2-7(a). Equation 2.8 shows that the in-band quantization noise is attenuated by a factor of OSR:

$$P_{e,in-band} \equiv \int_{-f_B}^{+f_B} S_e(f)df = \left(\frac{2f_B}{f_s}\right)\frac{\Delta^2}{12} = \frac{1}{\text{OSR}} \cdot \frac{\Delta^2}{12} \tag{2.8}$$

This essentially means that, compared with a Nyquist-rate ADC, the SQNR of an oversampling ADC is now higher by a factor of OSR. Nevertheless, the oversampling ADC is running at a higher speed than its Nyquist-rate counterpart, hence trading speed for resolution.

2.2.2 Noise-Shaping

Based on oversampling, the idea of noise-shaping is to filter the quantization noise so that the in-band noise is further suppressed and a higher SQNR results, as is illustrated in Figure 2-7(b).

Noise-shaping is made possible through a combination of feedback and filtering. According to the block diagram shown earlier in Figure 2-1, Equation 2.9 calculates the modulator transfer function assuming linear model of the quantizer:

$$\begin{aligned} V(z) &= STF(z)U(z) + NTF(z)E(z) \\ &= \frac{L_0(z)}{1 - L_1(z)}U(z) + \frac{1}{1 - L_1(z)}E(z) \end{aligned} \tag{2.9}$$

where STF and NTF denote the signal transfer function and the noise transfer function of the modulator respectively, and the linearized modulator block diagram is redrawn in Figure 2-8.

The result shows that the signal and the quantization noise are filtered differently. By choosing $L_0(z)$ and $L_1(z)$ properly, we can make the NTF a high-pass filter while the STF an all-pass filter. In this way the in-band quantization noise can be

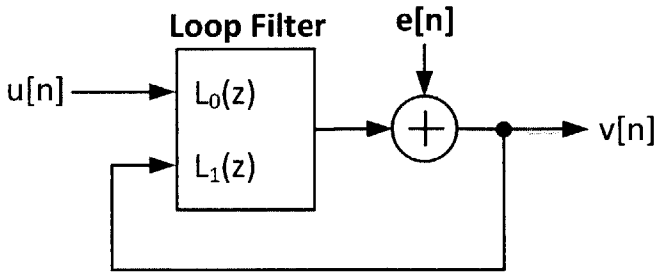


Figure 2-8: Linearized general block diagram of a DT $\Delta\Sigma$ modulator.

suppressed while the signal remains unaffected.

Take a 1st-order DT $\Delta\Sigma$ modulator as an example, the block diagram of which is shown in Figure 2-9. The loop filter of this 1st-order modulator is an integrator with the transfer function:

$$L(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.10}$$

The NTF and STF are calculated below:

$$NTF(z) = \frac{1}{1 + L(z)} = 1 - z^{-1} \tag{2.11}$$

$$STF(z) = \frac{L(z)}{1 + L(z)} = z^{-1} \tag{2.12}$$

which are indeed a high-pass and an all-pass filter respectively.

The PSD of the filtered quantization noise becomes:

$$S_q(f) = |NTF(e^{j2\pi f/f_s})|^2 S_e(f) \tag{2.13}$$

where

$$|NTF(e^{j2\pi f/f_s})|^2 = |1 - e^{-j2\pi f/f_s}|^2 = \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{2.14}$$

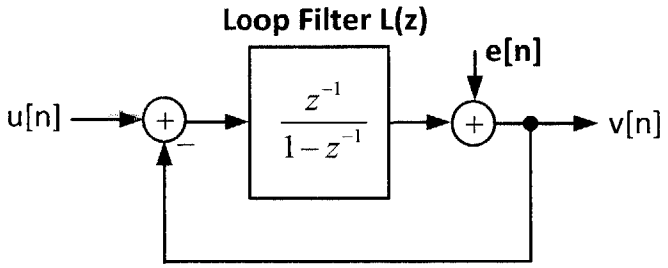


Figure 2-9: Block diagram of a 1st-order DT $\Delta\Sigma$ modulator.

For OSR $\gg 1$, we have $f_B \ll f_s$. Therefore, for the in-band frequencies, we have:

$$|NTF(e^{j2\pi f/f_s})|^2 = \left[2sin\left(\frac{\pi f}{f_s}\right)\right]^2 \approx \left(\frac{2\pi f}{f_s}\right)^2 \tag{2.15}$$

The in-band noise power can thus be calculated as:

$$P_{q,in-band} = \int_{-f_B}^{+f_B} S_q(f)df \approx \frac{\Delta^2}{12f_s}\int_{-f_B}^{+f_B}\left(\frac{2\pi f}{f_s}\right)^2 df = \frac{\pi^2\Delta^2}{36\text{OSR}^3} \tag{2.16}$$

This result shows that the in-band quantization noise power decreases with OSR at a rate of 9 dB/octave, which is an attenuation much greater than that from over-sampling alone.

For an L[th] order NTF, Equations 2.11, 2.15, and 2.16 can be generalized into:

$$NTF(z) = (1 - z^{-1})^L \tag{2.17}$$

$$|NTF(e^{j2\pi f/f_s})|^2 = \left[2sin\left(\frac{\pi f}{fs}\right)\right]^{2L} \tag{2.18}$$

$$P_{q,in-band} = \frac{\Delta^2}{12f_s}\int_{-f_B}^{+f_B}\left[2sin\left(\frac{\pi f}{fs}\right)\right]^{2L} df \approx \frac{\Delta^2}{12}\cdot\frac{\pi^{2L}}{(2L+1)\text{OSR}^{2L+1}} \tag{2.19}$$

Equation 2.19 suggests two additional ways to improve SQNR apart from adding quantization levels: (a) boosting the OSR of the modulator by sampling at a higher

f_s, and (b) increasing the order of the loop filer, which in turn increase the order of the NTF. With a higher-order NTF, the noise power decreases with OSR at a greater rate. Therefore, a $\Delta\Sigma$ modulator is capable of a much higher SQNR compared with a Nyquist-rate ADC. One thing to note here is that, L, the order of the NTF, cannot increase infinitely. The higher the order, the more likely it is for the modulator to go unstable.

The NTF is critical to a $\Delta\Sigma$ modulator because it determines the achievable SQNR. In the design procedure of a $\Delta\Sigma$ modulator, the first step is always to select a proper NTF that fulfills the design specifications. The STF, on the other hand, is a secondary concern. The major design consideration for the STF is to make its in-band gain unity.

2.2.3 Bandpass Delta-Sigma Modulation

So far we have been discussing $\Delta\Sigma$ modulation for lowpass systems, where the signal band is centered at DC, and the highest frequency-of-interest is only a small fraction of f_s. For bandpass modulators, however, narrow-band signals are centered at a carrier frequency f_0. f_B now represents the double-sided bandwidth of the signal. Figure 2-10(a) shows the spectrum of a bandpass input signal. In this section, we look at how this bandpass signal is oversampled and noise-shaped.

In order to oversample the bandpass signal, f_s needs to be much higher than f_B. The definition of OSR $= \frac{f_s}{2f_B}$ still holds. However, it is not necessary that f_s is much greater than f_0. Thus, it is possible that the signal is comparable in frequency to f_s even though it is highly oversampled.

In order to shape the quantization noise, we need to make the NTF a band-stop filter so that the quantization noise around f_0 is suppressed. This necessitates a bandpass loop filter $L_1(z)$. In fact, the only difference between a lowpass and bandpass $\Delta\Sigma$ modulator is the type of loop filter that is employed.

Figure 2-10(b) illustrates the combined effect of oversampling and noise-shaping in the bandpass case. Most of the conclusions that we have drawn from the lowpass $\Delta\Sigma$ modulation can be applied to the bandpass case directly.

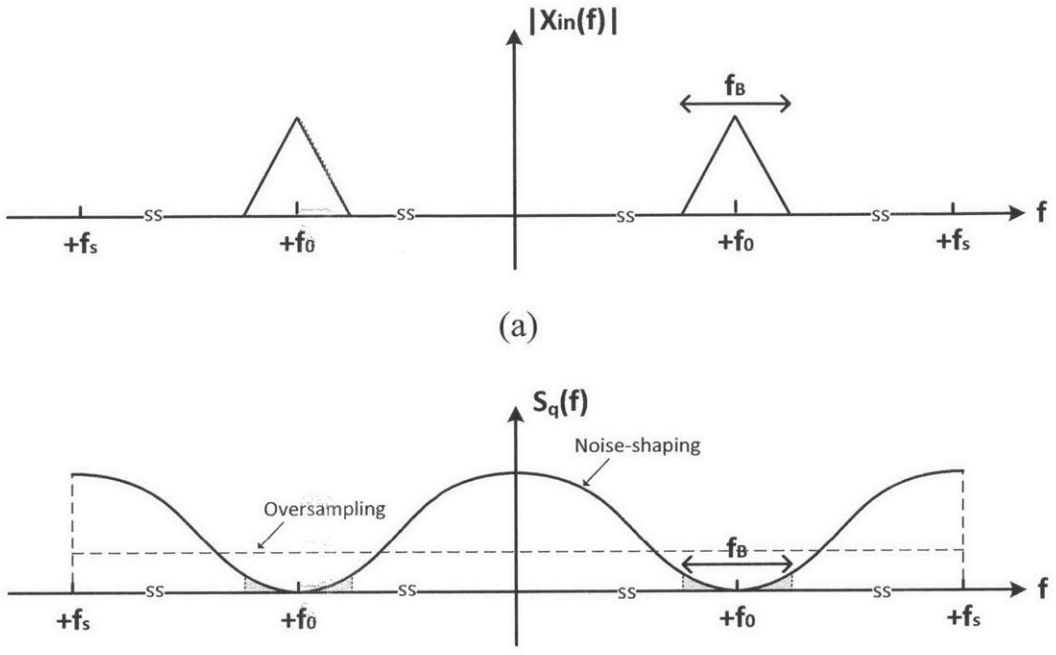


Figure 2-10: (a) Spectrum of a bandpass input signal. (b) PSD of shaped quantization noise for a bandpass $\Delta\Sigma$ modulator.

2.3 Modulator Implementation

Now that we understand the principles of $\Delta\Sigma$ modulation, we examine in this section two types of $\Delta\Sigma$ modulators, namely DT and CT modulators. The major difference between the two types of modulators lies in the nature of the loop filter.

2.3.1 Discrete-time Delta-Sigma Modulator

A DT $\Delta\Sigma$ modulator processes the signal entirely in the discrete-time domain. This necessitates an AAF and an S/H circuit that precede the modulator. Figure 2-11 shows the block diagram of the entire DT $\Delta\Sigma$ ADC [2]. The analog input signal, $x_{in}(t)$, is filtered and sampled first before entering the DT $\Delta\Sigma$ modulator. The output signal from the modulator, $v[n]$, contains both the input signal and the shaped quanti-

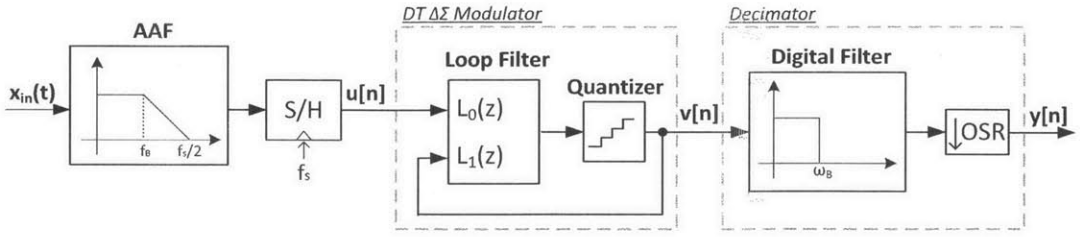


Figure 2-11: Block diagram of a DT $\Delta\Sigma$ ADC [2].

zation noise at the rate of f_s. A decimator that succeeds the modulator down-samples $v[n]$ to Nyquist rate, making the output signal from the ADC, $y[n]$, compatible with the digital blocks that follow.

The transfer function of the DT loop filter can be easily derived from the desired NTF:

$$L_1(z) = 1 - \frac{1}{NTF(z)} \tag{2.20}$$

In actual implementation, $L_1(z)$ and $L_0(z)$ share the same hardware. Once we fix $L_1(z)$, $L_0(z)$ is determined. The STF of the modulator is thus:

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} = L_0(z) \cdot NTF(z) \tag{2.21}$$

The DT loop filter is usually implemented with switched-capacitor (SC) circuits that are accurate and robust under process variations. However, SC circuits require op amps to settle within half the sampling period. The gain-bandwidth requirements of the op amps are usually several times higher than f_s. This makes DT implementation unsuitable for high sampling rate ($\sim$ GHz) and wide-band ($\sim$10 MHz) applications.

2.3.2 Continuous-time Delta-Sigma Modulator

The loop filter of a CT $\Delta\Sigma$ modulator operates in a continuous-time fashion. Figure 2-12 shows the block diagram of an overall CT $\Delta\Sigma$ ADC [2]. Apart from the nature of the loop filter, a significant difference between CT and DT $\Delta\Sigma$ ADCs lies in the point

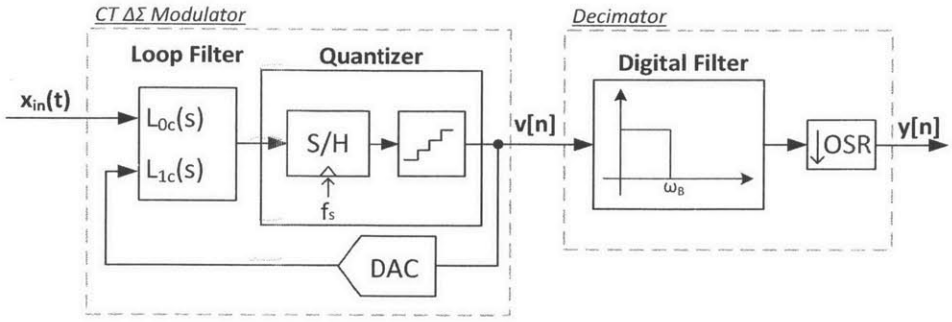


Figure 2-12: Block diagram of a CT $\Delta\Sigma$ ADC [2].

where sampling takes place. The signal in the CT $\Delta\Sigma$ ADC remains continuous until it reaches the quantizer, where both sampling and quantization happen at the same time. The simultaneous sampling and quantization provide a CT $\Delta\Sigma$ modulator with an inherent anti-aliasing filtering characteristic. The frequency components that are to be aliased in-band, as well as the quantization noise, are filtered by the NTF and are thus suppressed. The AAF can thus be removed from the ADC, which saves both power and system hardware.

The CT loop filter can be realized with gm-C or active-RC filters. These filters do not require op amps to settle. This greatly relaxes the gain-bandwidth requirements of the op amps and thus reduces the power consumption of the modulator. The speed of a CT $\Delta\Sigma$ modulator is limited by the excess delay through the op amps, the regeneration time of the quantizer, and the update rate of its DACs [1]. This enables the CT $\Delta\Sigma$ modulator to function at a much higher sampling rate with a much wider signal bandwidth compared with its DT counterpart. Because of its potential of fast operations and power efficiency, CT $\Delta\Sigma$ modulators provide a good solution for high speed and wide-band analog-to-digital conversion.

The transfer function of the CT loop filter, $L_{0c}(s)$, is difficult to determine now that the modulator travels between discrete- and continuous-time domains. Besides, the behavior of the DAC affects the loop as well. To solve this problem, we introduce the impulse response matching method [1].

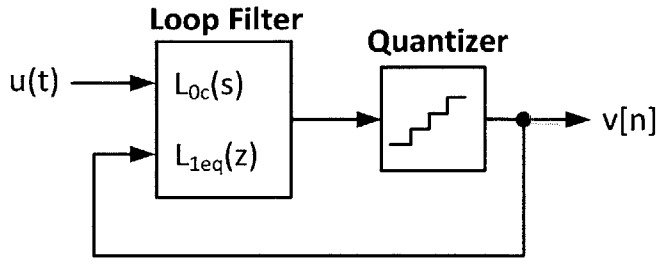


Figure 2-13: Block diagram of a CT $\Delta\Sigma$ modulator incorporating the equivalent DT loop transfer function $L_{1eq}(z)$.

2.3.3 Impulse Response Matching

The output of the CT $\Delta\Sigma$ modulator is a DT signal. We can thus derive a equivalent DT loop transfer function of the CT modulator:

$$L_{1eq}(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}[DAC(s)L_{1c}(s)]\left[\sum_{n=0}^{\infty}\delta(t-nT)\right]\right\} \tag{2.22}$$

where $T = \frac{1}{f_s}$ is the sampling period, and the periodic impulse train models the sampling procedure.

Figure 2-13 shows the block diagram of a CT $\Delta\Sigma$ modulator incorporating $L_{1eq}(z)$. The NTF and STF of the CT $\Delta\Sigma$ modulator are expressed in Equations 2.23 and 2.24 respectively:

$$NTF(z) = \frac{1}{1 - L_{1eq}(z)} \tag{2.23}$$

$$STF(s) = \frac{L_{0c}(s)}{1 - L_{1eq}(z)} = L_{0c}(s) \cdot NTF(z) \tag{2.24}$$

By looking at Equation 2.24, we can observe the anti-aliasing filtering characteristic of the STF from the $NTF(z)$ term it contains.

Equation 2.22 is very complicated and difficult to solve. A practical way to determine $L_{1eq}(z)$ is to find its impulse response. We do this by breaking the feedback loop at the quantizer, inserting an impulse at the output, and sampling the signal

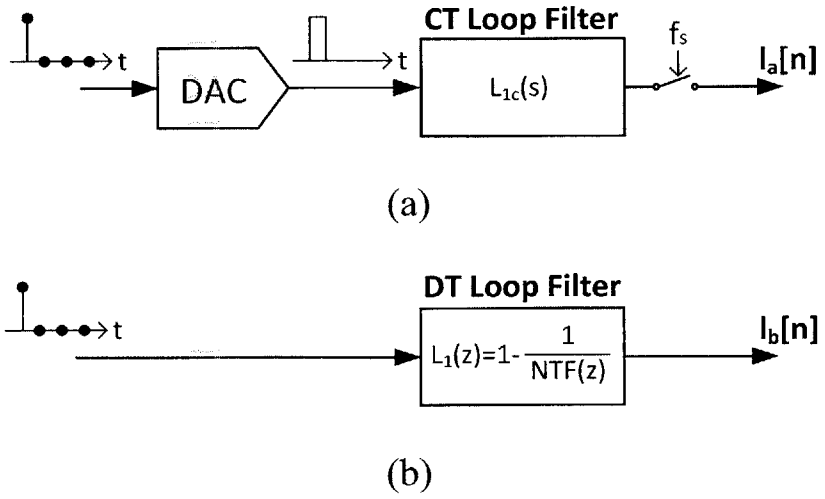


Figure 2-14: Impulse response matching method. (a) Impulse response of of the CT feedback path. (b) Impulse response of the equivalent DT loop filter.

that is coming back to the quantizer, as shown in Figure 2-14(a). The resulting $l_a[n]$ is exactly the impulse response of $L_{1eq}(z)$. In order to obtained $L_{1c}(s)$, the transfer function of the CT loop filter, we need a DT loop filter that gives the same NTF as that of the CT $\Delta\Sigma$ modulator. The transfer function of this DT loop filter, $L_1(z)$, is expressed in Equation 2.20. We then adjust the coefficients of $L_{1c}(s)$ so that $l_a[n]$ matches $l_b[n]$, the impulse response of $L_1(z)$. The resulting $L_{1c}(s)$ is the CT loop filter transfer function that gives the desired NTF.

2.4 Summary

This chapter mainly covers two topics: (a) the principles of $\Delta\Sigma$ modulation, and (b) the comparison between DT and CT $\Delta\Sigma$ modulators.

Compared with its DT counterpart, a CT $\Delta\Sigma$ modulator is capable of a higher sampling rate, a wider signal bandwidth, and better power efficiency. It also has an inherent anti-aliasing filtering characteristic that removes the AAF from the system. Thus, a CT bandpass $\Delta\Sigma$ modulator provides a promising solution for modern soft-

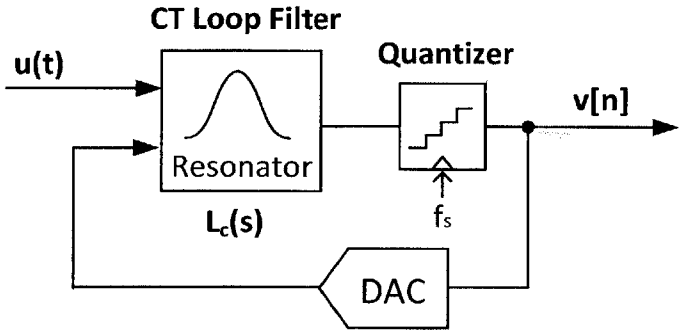


Figure 2-15: General block diagram of a CT bandpass $\Delta\Sigma$ modulator

ware receivers. A general block diagram of a CT bandpass $\Delta\Sigma$ modulator is shown in Figure 2-15.

Now that we have described the basic operations, the following chapters will discuss the implementation of a CT bandpass $\Delta\Sigma$ modulator from both system-level (Chapter 3) and transistor-level (Chapter 4 and 5) points of view.

Chapter 3

Modulator Architecture

This chapter describes the system-level design methodology of the CT bandpass $\Delta\Sigma$ modulator. We first introduce the procedure of determining the modulator specifications. Based on these targets, a proper NTF is selected and its realization examined. Two different modulator architectures, the feedback and the feed-forward, are discussed and compared. The feedback topology is chosen due to its greater stability, better STF, and superior anti-aliasing filtering property. We modify the modulator topology by adding a feed-forward coupling path so that the distortion is reduced and the modulator linearity is improved. We then introduce the method of determining the various coefficients of the modulator that implement the desired NTF.

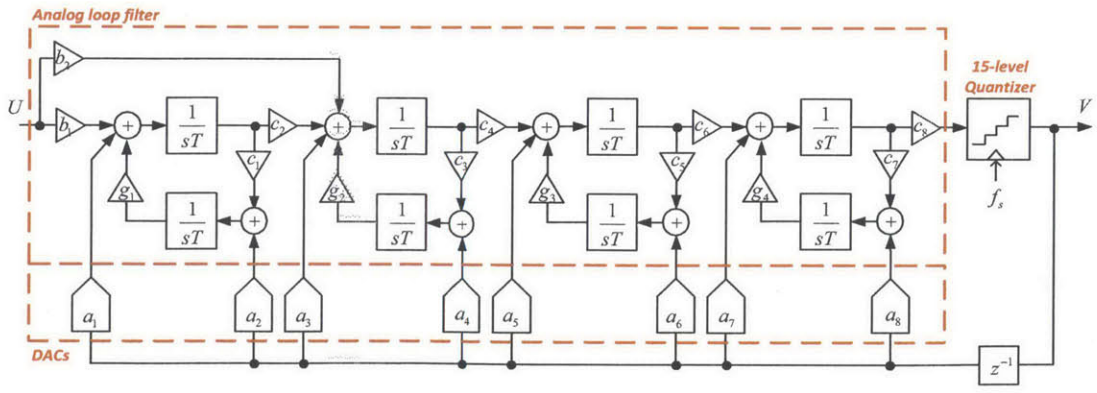


Figure 3-1: Complete block diagram of the proposed CT bandpass $\Delta\Sigma$ modulator

A complete block diagram of the proposed CT bandpass $\Delta\Sigma$ modulator arrives at the end of the chapter and is displayed here first in Figure 3-1 .

3.1 Desired Modulator Specifications

The goal of this thesis is to demonstrate a wide-band, high-resolution, and power efficient CT bandpass $\Delta\Sigma$ modulator that is suitable for software-defined receiver systems. Table 3.1 lists the desired specifications of the modulator. The procedures of determining these specifications are stated as follows.

Table 3.1: Desired modulator specifications.

Parameter	Desired Specification
Modulator Architecture	Continuous-Time Feedback Topology
Sampling Frequency (f_s)	1 GHz
Signal Bandwidth (f_B)	25 MHz
Center Frequency (f_0)	250 MHz ($\frac{f_s}{4}$)
Oversampling Ratio (OSR)	20
Signal-to-Noise Ratio (SNR)	75 dB
Number of Quantization Levels (M)	15
Quantization Step (Δ)	120 mV
Power Consumption	300 mW

For the modulator architecture, as explained in the previous chapter, the CT type of $\Delta\Sigma$ modulator is more suitable for our application due to its high speed, wide bandwidth, and low power consumption capability. In Section 3.4, we will learn that the feedback topology has the benefits of greater stability and better anti-aliasing filtering in the presence of large out-of-band interferers. Both advantages render the feedback topology a better fit for receiver applications than its feed-forward counterpart.

In terms of modulator performance, the sampling rate should be on the order of GHz to achieve both a wide signal bandwidth of about 25 MHz, and a fair OSR,

which is necessary to achieve high resolution. An OSR of 20 is chosen arbitrarily in this design, mandating the sampling frequency to be 1 GHz. For the center frequency f_0, we place it at $\frac{f_s}{4}$ for the following considerations:

- The image signals affect the in-band signal to a minimal degree when $f_0 = \frac{f_s}{4}$.
- Digital down-conversion becomes much easier to implement when $f_0 = \frac{f_s}{4}$.
- The coefficient of the direct feedback path around the quantizer becomes zero when $f_0 = \frac{f_s}{4}$, eliminating the DAC with the most stringent speed requirement.

In order to achieve high resolution, a SNR around 75 dB is targeted.

For the quantizer, we need finer quantization to achieve greater SNR. Meanwhile, the quantizer needs to operate fast enough so that the digital output signals can settle within half a sampling period. A 15-level quantizer is thus chosen as a fair trade-off between speed and resolution. The input range of the quantizer is dictated by be the maximum output signal swing that the loop filter is capable of. For a 1.2 V power supply and a push-pull output stage, the single-ended signal swing of the loop filter can reach as high as 900 mV, hence the differential input range [-900 mV, +900 mV]. The LSB (or Δ) is thus calculated from Equation 2.1 to be 120 mV.

The target power consumption of the modulator is found by scaling the power consumptions of recently published state-of-the-art CT bandpass $\Delta\Sigma$ modulators ([9] [13] [14] [3]) in such a way that a similar FoM is achieved. The definitions of FoM and ENOB are expressed earlier in Equation 1.1.

3.2 NTF Selection

For a well-designed $\Delta\Sigma$ modulator, the SNR should be limited by thermal noise, and the quantization noise should be negligible. A SQNR of 90 dB is thus targeted in this design.

The SQNR of a $\Delta\Sigma$ modulator is determined by three factors: the OSR, the NTF, and the number of quantization levels. The OSR determines the signal bandwidth with respect to the sampling frequency. The NTF decides the extent to which the in-band quantization noise is suppressed. The number of quantization levels gives the

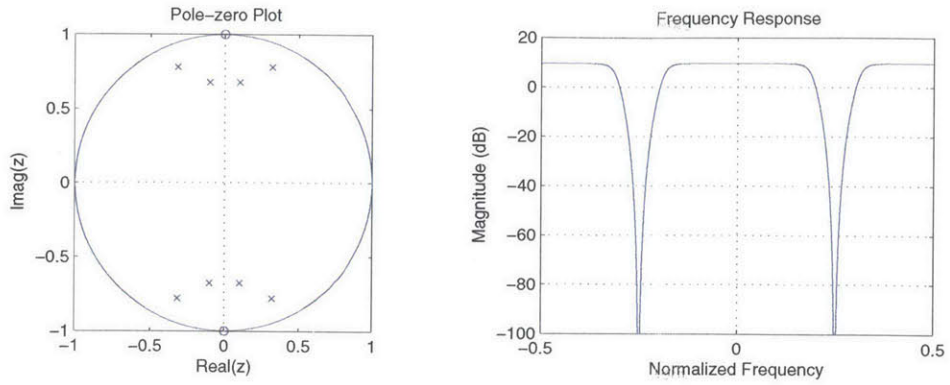


Figure 3-2: Pole-zero plot and frequency response of the desired NTF.

amount of the quantization noise that is to be shaped by the NTF. Both the OSR and the number of quantization levels are pre-determined in the specifications. We need to select a proper NTF that achieves the target SQNR.

By using the delta sigma toolbox [16], an 8^{th}-order NTF is chosen. Its expression is displayed below:

$$NTF(z) = \frac{(z^2+1)^4}{(z^2+0.20z+0.47)(z^2-0.20z+0.47)(z^2+0.64z+0.71)(z^2-0.64z+0.71)} \tag{3.1}$$

The pole-zero plot and the frequency response are displayed in Figure 3-2.

The 8^{th}-order NTF places four of its zeros inside the signal band and the other four in the image band, making possible a 4^{th}-order noise-shaping. All the zeros are located at band center. Although, by optimally spreading the zeros across the signal band, a theoretical SQNR improvement of 10 dB can be achieved, the final SNR of the implemented modulator, which is thermal noise and distortion limited, can hardly be affected by this improvement. Therefore, to simplify the design, we position all the NTF zeros at band center. The maximum out-of-band gain (H_{inf}) of this NTF is 3, which achieves a fair trade-off between stability and the achievable SQNR.

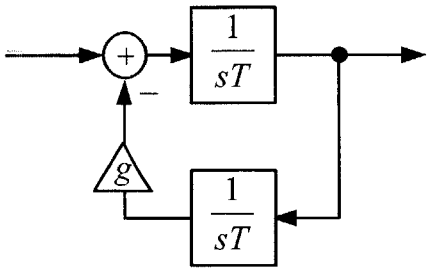


Figure 3-3: Block diagram of a CT resonator.

3.3 Realizing Complex NTF Zeros

Equation 3.1 shows that the desired NTF contains eight zeros at $\pm\frac{j\pi}{2}$. These zeros translate into poles of the loop filter $L_c(s)$. We employ resonators as shown in Figure 3-3 to implement these poles. The transfer function of the resonator is:

$$T_{res}(s) = \frac{sT}{(sT)^2 + g} \tag{3.2}$$

where $T = \frac{1}{f_s}$ represents the sampling period.

The value of g affects the pole locations directly. Since the center frequency is at $\frac{f_s}{4}$, the poles of $T_{res}(s)$ need to be placed at $\pm\frac{2\pi f_s}{4}$. We can thus calculate the value of g to be $\left(\frac{\pi}{2}\right)^2$ or 2.467.

The type of resonator shown in Figure 3-3 forms the building block of the modulator loop filter. In our design, four of them are cascaded to realize the 8^{th}-order NTF. Since two integrators are required to realize one resonator, the whole modulator in turn necessitates eight integrators or eight op amps.

3.4 Modulator Topology

Now that the NTF is chosen, we need to consider the implementation of the modulator. Two commonly used modulator topologies are the feed-forward and feedback topologies, whose block diagrams are illustrated in Figure 3-4 and Figure 3-5 respec-

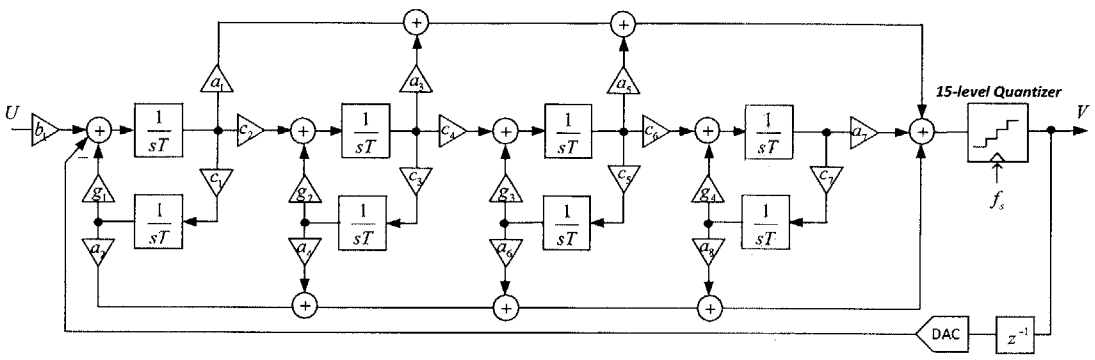


Figure 3-4: Block diagram of an 8^{th}-order feed-forward CT bandpass $\Delta\Sigma$ modulator.

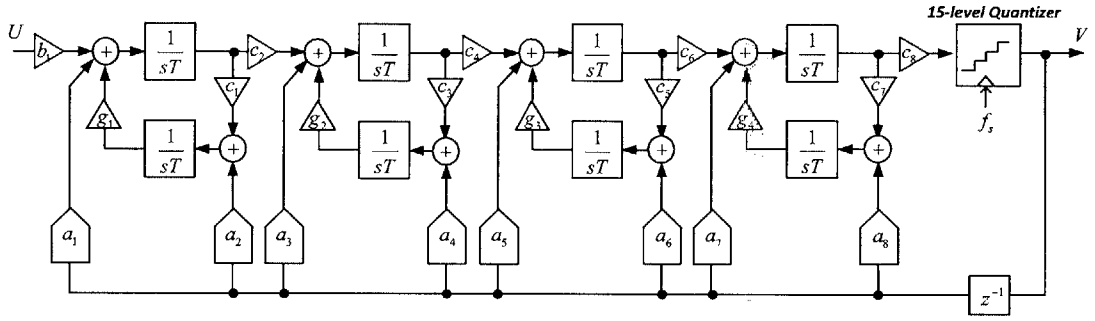


Figure 3-5: Block diagram of an 8^{th}-order feedback CT bandpass $\Delta\Sigma$ modulator.

tively. Each topology has its own advantages and disadvantages, which are discussed and compared in this section.

3.4.1 Feed-forward Versus Feedback Topology

For the feed-forward topology, the major advantage is its low power consumption. The modulator has only one feedback path. At the input summing point, the signal components get cancelled almost entirely, and the loop filter receives only the shaped quantization noise. This largely reduces the dynamic range requirement of the loop filter, hence lowering power consumption.

The feedback topology, on the other hand, contains multiple feedback paths. Therefore, each resonator possesses the signal components that are yet to be can-

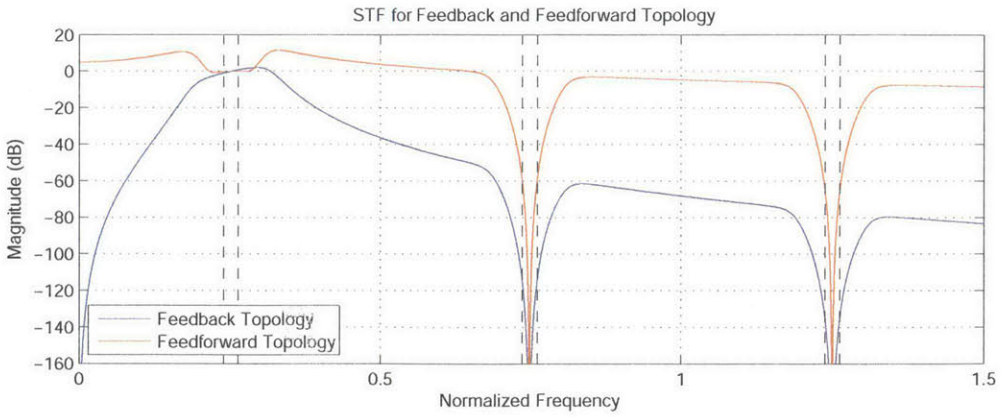


Figure 3-6: STF of both feedback and feed-forward topology.

celled by the succeeding feedback path. The dynamic range requirement of the loop filter thus becomes more strict, with that of the 1st resonator being the most stringent. Therefore, the loop filter of the feedback topology is very power hungry. Besides, the feedback topology requires a couple of DACs in its feedback path whereas its feedforward counterpart needs only one. This again accounts for more power.

Nevertheless, the STF of the feed-forward topology is problematic. Figure 3-6 compares the STF of a feed-forward CT $\Delta\Sigma$ modulator with that of a feedback modulator which realizes the same NTF. Inside the signal band, both STFs are flat at 0dB, which is desirable. Outside the signal band, however, the STF of the feed-forward topology suffers from two serious problems:

Large out-of-band peaking The STF of the feed-forward topology has an out-of-band peaking of 10 dB. This makes the feed-forward modulator much more likely to go unstable, especially in the presence of large out-of-band interferers. Even without out-of-band interferers, behavioral-level simulations show that the maximum stable input amplitude of the feed-forward topology is 4 dB lower than that of its feedback counterpart. This essentially means a 4 dB degradation in SNR.

Poor anti-aliasing filtering characteristic The anti-aliasing filtering characteristic of the feed-forward topology is much worse than that of its feedback counterpart. At the band edge, especially, the alias attenuation of the feed-forward topology

is only 60 dB. This is 50 dB lower that the attenuation from the feedback topology, and is highly insufficient.

The reason for the poor STF of the feed-forward topology is explained as follows. From Equation 2.24, we learn that the STF is the product of the CT loop filter transfer function $L_{0c}(s)$ and the NTF. Inside the signal band, the zeros from the NTF are cancelled by the poles from $L_{0c}(s)$, which gives a flat and unity in-band gain. In the image bands (i.e. in the vicinity of $\frac{3f_s}{4}$ and $\frac{5f_s}{4}$), the STF is dominated by the NTF. The image signals inside these bands are thus suppressed, hence the inherent anti-aliasing filtering property. Outside the signal and image bands, the STF is dominated by $L_{0c}(s)$. For the feedback topology, the $L_{0c}(s)$ gives four zeros at DC. Therefore, from DC to the signal band, the STF ramps up at 80 dB/dec; from the signal band to higher frequencies, it rolls off at -80 dB/dec. For the feed-forward topology, on the other hand, the multiple feed-forward paths in the loop filter create zeros in the vicinity of the signal band. This reduces the effective order of the STF. Therefore, the STF ramps up and down much more slowly than its feedback counterpart, resulting in insufficient alias attenuation. These zeros around the signal band are also the cause of the large out-of-band peaking.

Apart from STF problems, an additional summing op amp is needed in the feed-forward topology between the loop filter and the quantizer. This is undesirable because the summing block introduces additional excessive loop delay (ELD) and may adversely affect the stability of the modulator.

Considering the factors above, we choose the feedback topology for our design. Despite greater power consumption, the feedback topology provides greater stability and a much better STF that is free from out-of-band peaks and allows decent alias attenuation, both of which are advantageous in the context of wireless communications where large blocker signals are present [3].

One thing to note here is that there is always a delay block associated with the quantizer on the modulator block diagrams. This is because the outputs of the quantizer are latched and become only available after one clock cycle delay. The

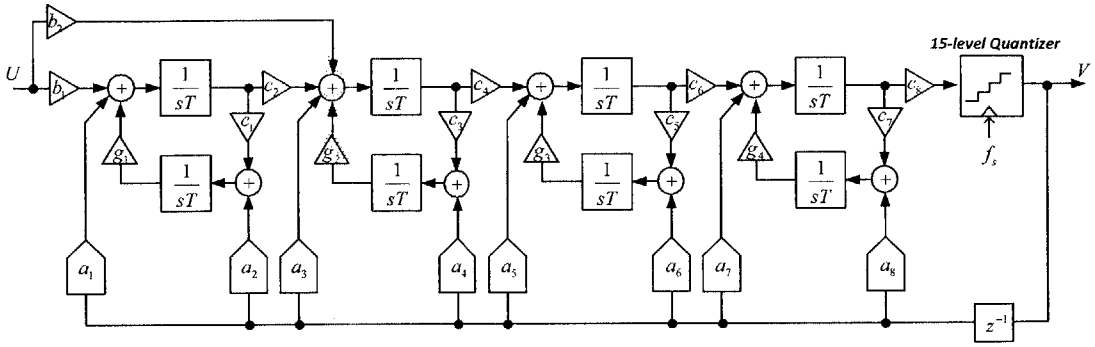


Figure 3-7: Block diagram of the modified modulator topology.

latch is necessary since it helps avoid the metastability issues of the quantizer [17] and synchronizes the quantizer output with the clock. By adding this latch, the delay of the quantizer is fixed and well-modeled.

3.4.2 Modified Feedback Topology

As discussed later in Section 4.1.2, the thermal noise from the 1st resonator is a limiting factor for the achievable SNR of the modulator. Our solution to this problem is to boost the signal swing of the 1st resonator by employing a dual 2.5-V/1.2-V power supply. The signal swing at the output of this resonator thus gets doubled, offering a SNR improvement of 6 dB. However, the distortion from this resonator becomes the new limiting factor.

In an effort to alleviate the distortion, a feed-forward coupling path with the coefficient b_2 is added, as shown in Figure 3-7. Since this path provides another channel for the input signal to travel, the signal components carried by the 1st resonator is reduced, thereby relaxing the swing requirement and easing the distortion. Besides, the coefficient b_1 can be made larger now that the signal components in the 1st resonator become less. As introduced later in Section 4.1.2, increasing b_1 further improves SNR.

This additional feed-forward coupling path does not affect the NTF of the modulator. However, the STF is altered depending on the value of b_2. Figure 3-8 compares the STF of the basic feedback topology with that of the modified topology. The cou-

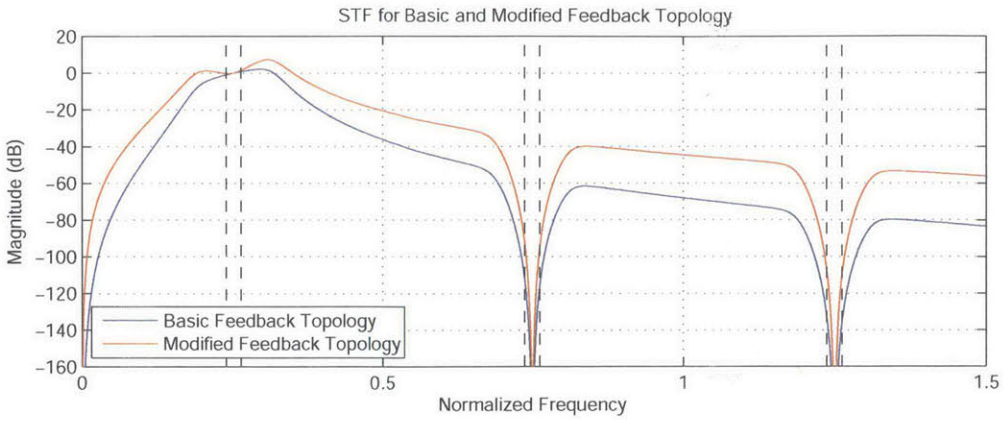


Figure 3-8: STF of both the basic and modified feedback topology ($b_2 = 0.396$).

pling path creates two STF zeros in the vicinity of the signal band, introducing small out-of-band peaks and compromising slightly the anti-aliasing filtering characteristic. But the benefit of SNR improvement outweighs the small STF degradations.

3.5 Determining Coefficients

Now that the modulator topology is decided, we need to specify the modulator coefficients (i.e. a_i, b_i, c_i and g_i in Figure 3-7) that implement the desired NTF. This section explains step by step how each set of coefficients is determined.

3.5.1 Determining Coefficients

We may first look at the basic feedback topology in Figure 3-5. Coefficients c_i's allow the scaling of the output signals of each resonator, and are initially set to unity. Coefficients g_i's determine the location of the modulator center frequency, and are calculated in Section 3.3 to be 2.467. Feedback coefficients a_i's are related to the pole locations of the NTF. These coefficients can be determined using the impulse response matching method introduced in Section 2.3.3. Coefficient b_1 is chosen such that a unity in-band STF results. All the aforementioned coefficients can be determined using the delta-sigma toolbox [16]. Their values are listed in Table 3.2.

3.5.2 Coefficient Scaling

Scaling is a procedure that, by manipulating the coefficients, the output swing of each resonator is altered but the modulator signal and noise transfer functions remain. In this design, we try to maximize the resonator output swings, especially that of the 1st resonator stage, so that the thermal noise can be suppressed and a better SNR results. A dual 2.5-V/1.2-V supply is employed in the 1st resonator stage. The differential signal swing of the 1st stage is thus boosted to 3.2 V. The swing of the other stages is 1.8 V, which is essentially the no-overload input range X_M of the quantizer.

We may now look at the modified modulator topology in Figure 3-7. The input coupling path relaxes the distortion from the 1st resonator and provides room for the coefficient b_1 to increase; however, it degrades STF. In order to determine the value of b_2, extensive transistor-level simulations have been carried out so that the optimum SNR can be achieved. The value of b_2 is 0.396.

The values of the scaled coefficients are listed in Table 3.2. Note that, after scaling, coefficients b_1, a_1 and a_2 go up significantly. We will see later in Section 4.1.2 that these larger values help to suppress the thermal noise from the 1st resonator stage and benefit SNR.

3.6 Summary

This chapter describes the system-level design procedures of the CT bandpass $\Delta\Sigma$ modulator. These procedures include determining the specifications, constructing the NTF, selecting the topology, and calculating the coefficients.

The complete block diagram of the proposed CT bandpass $\Delta\Sigma$ modulator is shown at the beginning of this chapter in Figure 3-1. An 8th-order NTF is selected to fulfill the SQNR target of 90 dB. The NTF is implemented with an analog loop filter of four resonators in cascade, a 15-level quantizer, and eight feedback DACs. A feedback topology is adopted for its greater stability, better STF, and superior anti-aliasing filtering property. An extra input coupling path is added because it alleviates distortion and improves the linearity of the modulator without compromising much of the

Table 3.2: Unscaled and scaled coefficient values.

Coefficient	Unscaled	Scaled	Coefficient	Unscaled	Scaled
b_1	0.1584	1.1405	c_1	1	1.3333
b_2	-	0.3960	c_2	1	0.1389
a_1	0.1244	0.8957	c_3	1	1.3333
a_2	-0.0792	-0.7603	c_4	1	0.6
a_3	0.5503	0.5503	c_5	1	1.25
a_4	-0.2855	-0.3807	c_6	1	1.6667
a_5	1.1032	0.6619	c_7	1	1
a_6	-0.5267	-0.3951	c_8	1	1
a_7	1.2782	1.2782	g_1	-2.4674	-1.8506
a_8	-0.6667	-0.6667	g_2	-2.4674	-1.8506
			g_3	-2.4674	-1.9739
			g_4	-2.4674	-2.4674

STF. The coefficients of the modulator are calculated, scaled, and listed in Table 3.2. From the system level simulation results that are displayed later in Section 6.1, the proposed modulator architecture achieves 92 dB SQNR with a -3 dBFS input signals. This fulfills the SQNR target and justifies the design choices we have made.

In the following chapters, the circuit implementations of the modulator are discussed (Chapter 4 and 5), and the transistor-level simulation results are provided (Chapter 6).

Chapter 4

Loop Filter Implementation

From this chapter, we start to discuss the transistor-level implementation of the proposed CT bandpass $\Delta\Sigma$ modulator. Figure 4-1 shows the top-level schematic. Key building blocks of the modulator include an analog loop filter, a 15-level quantizer, a DAC driver, and 8 DACs.

This chapter focuses on the implementation of the loop filter. Section 4.1 addresses two major design challenges concerning the loop filter, namely op amp non-ideality and thermal noise. Section 4.2 describes and explains the design of the multistage feed-forward op amps. The implementation of the quantizer, the DAC driver, and the DACs are discussed in the following chapter.

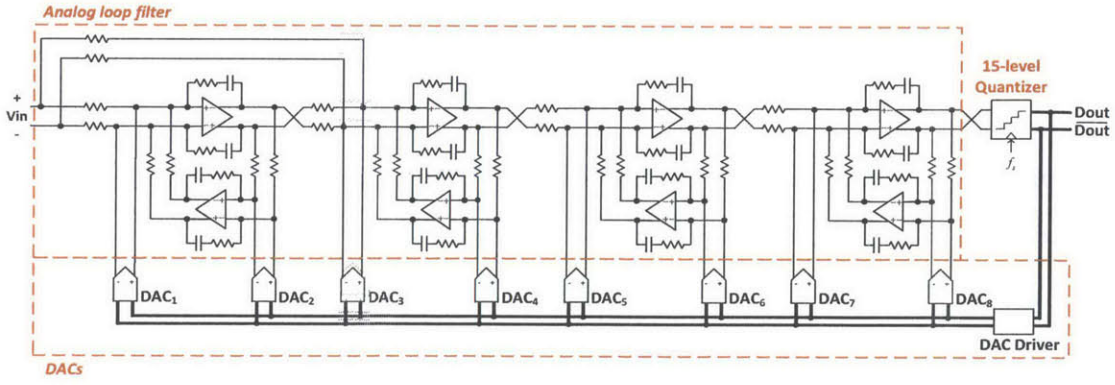


Figure 4-1: Top-level circuit implementation of the proposed CT bandpass $\Delta\Sigma$ modulator

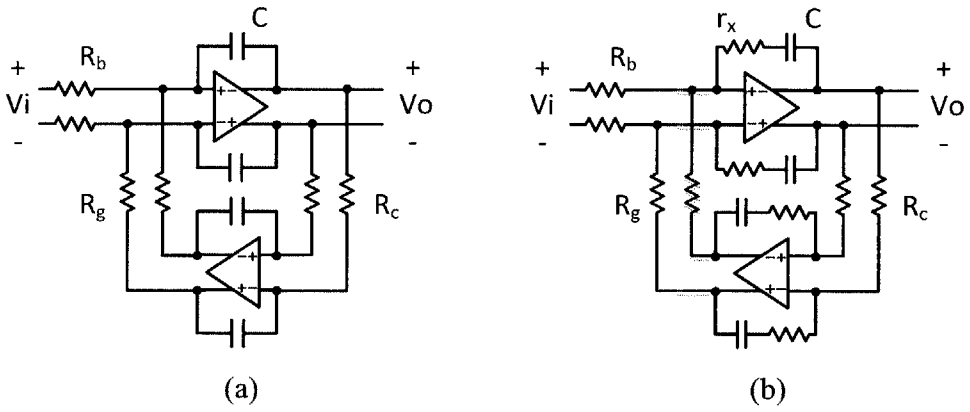


Figure 4-2: Active-RC resonators (a) w/o and (b)w/ series resistor r_x.

4.1 Loop Filter

The loop filter of a $\Delta\Sigma$ modulator provides noise shaping. For the proposed CT bandpass $\Delta\Sigma$ modulator, the loop filter consists mainly of four active-RC resonators in cascade. We choose active-RC resonators over gm-C resonators because of their better linearity.

There are two major challenges in the design of the loop filter:

Op amp non-ideality The finite gain and bandwidth of the op amp distort the loop transfer function and alter the NTF of the modulator. This degrades modulator SNR and may cause instability.

Thermal noise issue Thermal noise from the inter-stage resistors of the first resonator limits the achievable SNR of the modulator.

4.1.1 Op Amp Non-ideality

As is mentioned above, op amp non-ideality causes reduced SNR and even modulator instability. In this section, we mainly study the effects of non-ideal op amps on the behavior of resonators that are the key building blocks of the loop filter.

Figure 4-2(a) shows the circuit of an active-RC resonator. The resistor values are $R_b = \frac{R}{b}$, $R_g = \frac{R}{g}$, and $R_c = \frac{R}{c}$ respectively. R and C are unit resistor and capacitor values. b, g, and c correspond to the modulator coefficients that are listed in Table 3.2. Here we assume for simplicity the unscaled coefficients, i.e. $c = 1$ and $g = \left(\frac{\pi}{2}\right)^2 = 2.467$.

For an ideal op amp, the transfer function of the circuit can be calculated as:

$$\frac{V_o}{V_i}(s) = \frac{sCR_cR_g}{R_b(s^2C^2R_cR_g + 1)} = b \cdot \frac{sCR}{s^2C^2R^2 + g} \tag{4.1}$$

By making $RC = T = \frac{1}{f_s}$, Equation 4.1 becomes:

$$\frac{V_o}{V_i}(s) = b \cdot \frac{sT}{(sT)^2 + g} = b \cdot \frac{\frac{1}{sT}}{1 + \frac{g}{(sT)^2}} \tag{4.2}$$

which corresponds exactly to Figure 4-3(a), the block diagram of an ideal resonator.

Now we need to consider op amp non-ideality. Figure 4-3(b) shows the block diagram of the resonator employing non-ideal op amps with gain $A(s)$. A simplified block diagram is shown in Figure 4-3(c). Compare Figure 4-3(c) with Figure 4-3(a), two error terms appear in the loop. The transfer functions of these error terms are calculated as follows:

$$E_1(s) = \frac{A(s) \cdot \frac{sRC}{sRC+(b+g)}}{1 + A(s) \cdot \frac{sRC}{sRC+(b+g)}} = \frac{A(s) \cdot sRC}{(b+g) + (1 + A(s)) \cdot sRC} \tag{4.3}$$

$$E_2(s) = \frac{A(s) \cdot \frac{sRC}{sRC+1}}{1 + A(s) \cdot \frac{sRC}{sRC+1}} = \frac{A(s) \cdot sRC}{1 + (1 + A(s)) \cdot sRC} \tag{4.4}$$

Equations 4.3 and 4.4 show that the non-ideal op amps introduce additional poles and zeros to the resonator loop. This alters the close loop transfer function of the resonator, resulting in shift in the resonance frequency and undesirable resonator behaviors.

Assume a one-pole model for the op amp, i.e. $A(s) = \frac{A_0}{1+\frac{s}{\omega_c}}$, where $\omega_c A_0 \geq \frac{1}{RC} =$

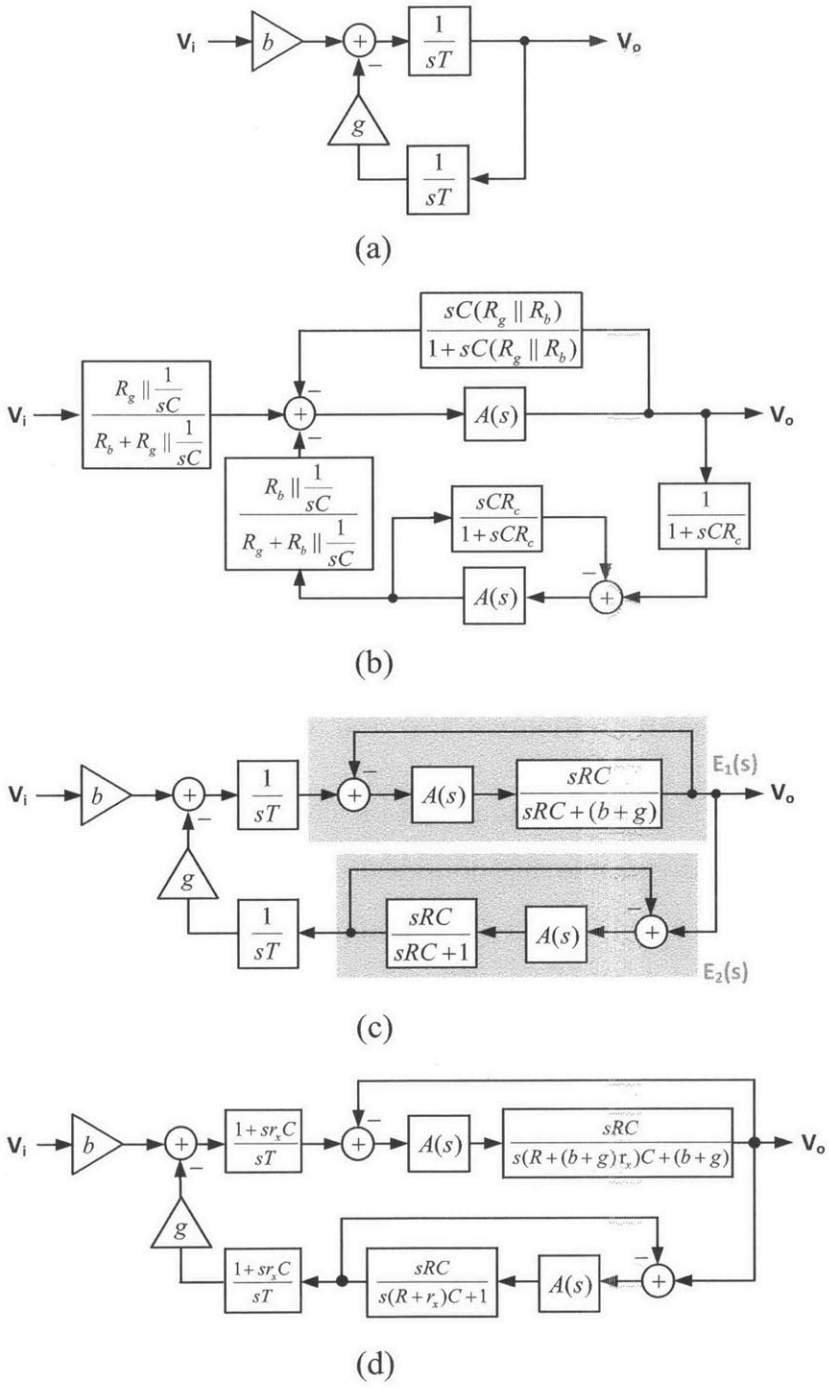


Figure 4-3: (a) Block diagram of an ideal resonator. (b) Original and (c) simplified block diagrams of the active-RC resonator with non-ideal op amp. (d) A simplified block diagrams of the active-RC resonator with non-ideal op amps and series resistors r_x.

f_s, $E_1(s)$ and $E_2(s)$ can be derived as follows:

$$\begin{aligned} E_1(s) &= \frac{sA_0\omega_c}{s^2 + s(\frac{b+g}{RC} + \omega_c(1+A_0)) + \frac{(b+g)\omega_c}{RC}} \\ &= \frac{sA_0\omega_c}{s^2 + s((b+g)f_s + \omega_c(1+A_0)) + (b+g)\omega_c f_s} \end{aligned} \tag{4.5}$$

$$\begin{aligned} E_2(s) &= \frac{sA_0\omega_c}{s^2 + s(\frac{1}{RC} + \omega_c(1+A_0)) + \frac{\omega_c}{RC}} \\ &= \frac{sA_0\omega_c}{s^2 + s(f_s + \omega_c(1+A_0)) + \omega_c f_s} \end{aligned} \tag{4.6}$$

Equations 4.5 and 4.6 show that, both $E_1(s)$ and $E_2(s)$ contains a zero at dc, and two widely separated poles. The approximate value of the poles of $E_2(s)$, for example, are:

$$\begin{aligned} |p_1| &\approx f_s + \omega_c(1+A_0) \approx \omega_c A_0 \\ |p_2| &\approx \frac{\omega_c f_s}{f_s + \omega_c(1+A_0)} \approx \frac{f_s}{A_0} \leq \omega_c \end{aligned} \tag{4.7}$$

where $|p_1|$ is on the order of GHz or above, dominated by the unity-gain frequency of the op amp, and $|p_2|$ is a fraction of ω_c, the dominant pole of the op amp.

Figure 4-4 gives two examples that help us understand the effects of op amp non-ideality. Figure 4-4(a) shows the frequency response of two example op amps. They have the same unity gain bandwidth but different dominant poles. Figure 4-4(b) shows the closed-loop frequency response of the corresponding non-ideal resonators, which deviates from that of an ideal resonator. The zero is moved away from DC, and an additional pole appears at high frequency. Figure 4-4(c) displays the frequency response of the non-ideal resonators in the vicinity of the center frequency. From the graph, it is clear that the resonance frequencies are shifted. Figure 4-4(d) illustrates the transient response of the non-ideal resonators. The difference in resonance frequencies can be observed now in the time domain. In addition, instead of a steady-state resonance, the transient response of the non-ideal resonators either diverges or converges. This is because of the extra phase shift that is introduced to the resonator loop by $|p_1|$ and $|p_2|$. Whether the resonance grows or diminishes depends on the actual locations of $|p_1|$ and $|p_2|$, which are in turn largely determined by the op amp

characteristics. For real op amps that usually contain multiple high-frequency poles, a divergent response is more likely to result, giving rise to modulator instability.

To sum up, op amp non-ideality causes resonance frequency to shift. This changes the NTF and causes SNR to drop. Op amp non-ideality may also leads to growing resonance. This causes stability problems.

In order to mitigate these effects, we take the following measures:

Tune the coefficient of g. We tune the coefficient of g to place the center frequency of the resonator at f_0. Since, for real op amps, it is difficult to calculate the exact value of the resonance frequency, we tune the value of g through simulation. Figure 4-4(e) shows the frequency responses of the non-ideal resonators after we tune the value of g.

Add series resistor r_x. Small resistors with the value of r_x are added to the resonator in series with the capacitors, as shown in Figure 4-2(b). The effect of r_x is to create a left-half-plane (LHP) zero in the resonator transfer function that cancels the high-frequency pole. Figure 4-3(d) shows the simplified block diagram of the resonator with r_x. The loop transfer function now contains two extra zeros at $-\frac{1}{r_x C}$. These zeros help restore the phase shift of the resonator loop, leading to a positive phase margin. Figure 4-4(f) shows the combined effects of r_x and g-tuning in time domain. What used to be a growing response is now almost a steady resonance.

4.1.2 Thermal Noise

Thermal noise limits the achievable SNR of the modulator. Especially for the 1st resonator stage, the noise requirement is very strict if we want to achieve a SNR of over 75 dB. Noise from the succeeding stages is attenuated by the in-band gain of the 1st resonator, hence the relaxed requirements for these stages.

Noise of the 1st resonator stage come from two major sources: (a) the op amp input transistors, and (b) the resistors. By using a large current, as is explained later in Section 4.2.2, noise from the input transistors can be reduced to negligible. Noise

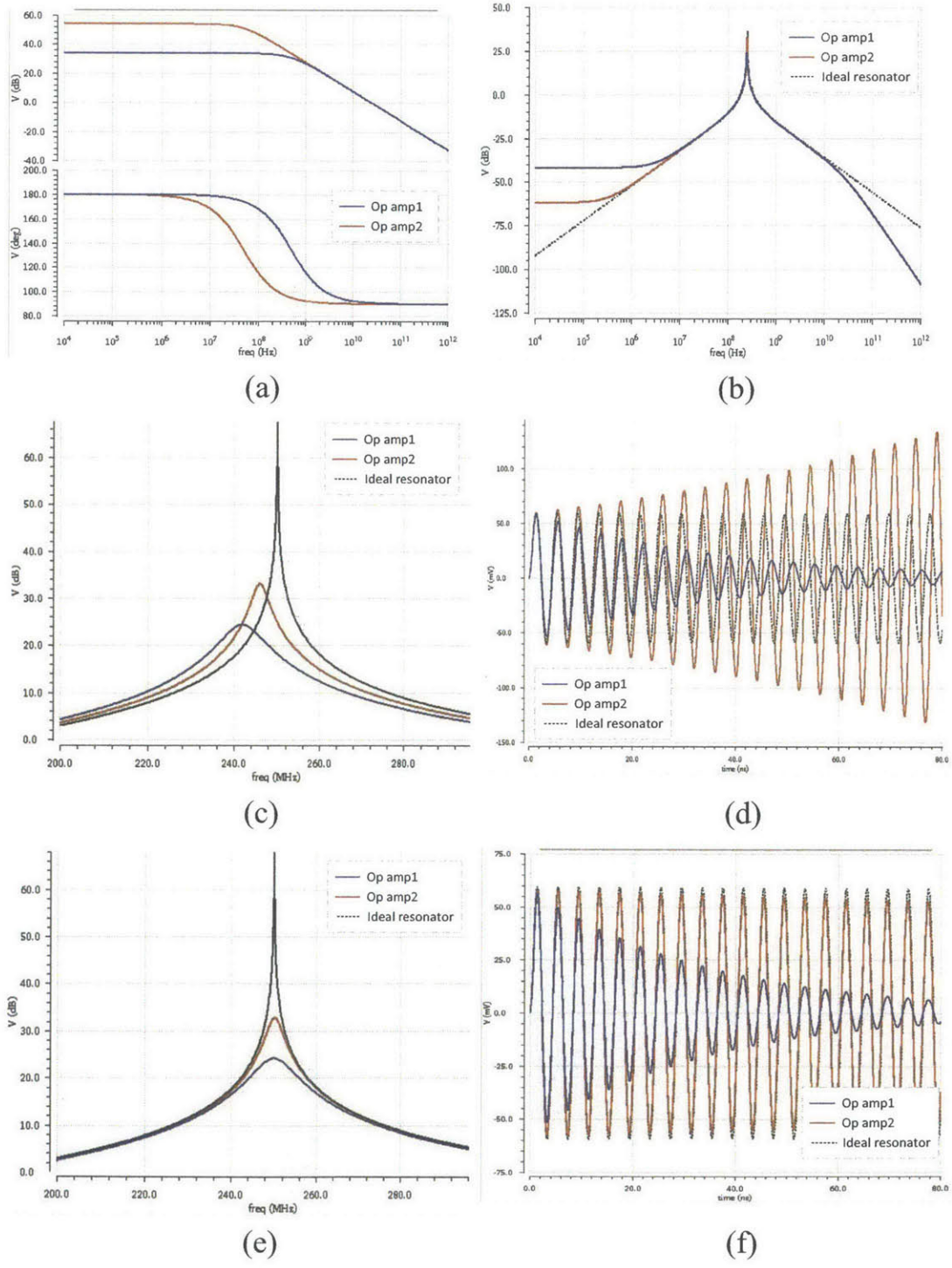


Figure 4-4: (a) Frequency response of two example amplifier. (b) Frequency response, (c) zoomed-in frequency response in the vicinity of f_0, and (d) transient response of the according non-ideal resonators. (e) Frequency and (f) transient response of the non-ideal resonators with r_x and g-tuning .

from the resistors, however, is the limiting factor.

Figure 4-5(a) shows the circuit of a resonator with resistor noise sources, where we still have $R_b = \frac{R}{b}$, $R_g = \frac{R}{g}$, and $R_c = \frac{R}{c}$. Figure 4-5(b) shows the according block diagram. For the 1st resonator stage, the resonator coefficients are $b = b_1$, $g = g_1$, and $c = c_1$ respectively, where the values of b_1, g_1 and c_1 can be found in Table 3.2. Again, for simplicity, we examine the unscaled coefficients where $c_1 = 1$ and $g_1 = \left(\frac{\pi}{2}\right)^2 = 2.467$.

The value of each noise source is written below:

$$\begin{aligned} \overline{v_{nb}^2} &= 2 \cdot 4kTR_b = \frac{8kTR}{b_1} \\ \overline{v_{ng}^2} &= 2 \cdot 4kTR_g = \frac{8kTR}{g_1} \\ \overline{v_{nc}^2} &= 2 \cdot 4kTR_c = 8kTR \end{aligned} \tag{4.8}$$

The noise transfer function of each noise source is calculated as follows:

$$\begin{aligned} T_b(s) &= \frac{\frac{1}{sR_bC}}{1 + \frac{1}{sR_cC} \cdot \frac{1}{sR_gC}} = \frac{sRC \cdot b_1}{s^2R^2C^2 + g_1} \\ T_g(s) &= \frac{\frac{1}{sR_gC}}{1 + \frac{1}{sR_cC} \cdot \frac{1}{sR_gC}} = \frac{sRC \cdot g_1}{s^2R^2C^2 + g_1} \\ T_c(s) &= \frac{\frac{1}{sR_cC} \cdot \frac{1}{sR_gC}}{1 + \frac{1}{sR_cC} \cdot \frac{1}{sR_gC}} = \frac{g_1}{s^2R^2C^2 + g_1} \end{aligned} \tag{4.9}$$

The closed-loop transfer function of the 1st resonator stage is:

$$H(s) = \frac{\frac{1}{sR_bC}}{1 + \frac{1}{sR_cC} \cdot \frac{1}{sR_gC}} = \frac{sRC \cdot b_1}{s^2R^2C^2 + g_1} = T_b(s) \tag{4.10}$$

The input-referred noise spectrum density of R_b, R_g and R_c can thus be calculated

as:

$$\begin{aligned}
\overline{v_{nb,in}^2} &= \overline{v_{nb}^2} \cdot \frac{|T_b(s)|^2}{|H(s)|^2} = 8kTR \cdot \frac{1}{b_1} \\
\overline{v_{ng,in}^2} &= \overline{v_{ng}^2} \cdot \frac{|T_g(s)|^2}{|H(s)|^2} = 8kTR \cdot \frac{g_1}{b_1^2} \\
\overline{v_{nc,in}^2} &= \overline{v_{nc}^2} \cdot \frac{|T_c(s)|^2}{|H(s)|^2} = \frac{8kTR}{(sRC)^2} \cdot \frac{g_1^2}{b_1^2}
\end{aligned} \tag{4.11}$$

For the narrow band signals that center at $\frac{f_s}{4}$, we have $|sRC| \approx \frac{2\pi f_s RC}{4} = \frac{\pi}{2} = \sqrt{g_1}$. Therefore,

$$\overline{v_{nc,in}^2} \approx \frac{8kTR}{g_1} \cdot \frac{g_1^2}{b_1^2} = 8kTR \cdot \frac{g_1}{b_1^2} \tag{4.12}$$

The total input-referred noise from the resistors is:

$$\overline{v_{n,in,total}^2} = \overline{v_{nb,in}^2} + \overline{v_{ng,in}^2} + \overline{v_{nc,in}^2} \approx 8kTR(\frac{1}{b_1} + \frac{2g_1}{b_1^2}) \tag{4.13}$$

The value of g_1 is fixed. Equation 4.13 shows that the noise from the resistors can be reduced by doing the following:

Reduce the unit resistor R**.** The thermal noise from the resistors is linearly proportional to R. Reducing R to $\frac{R}{4}$ gives us 6 dB increase in SNR. Since it is required that $RC = T$, the unit capacitor C needs to be quadrupled. This means the power consumption of the op amp needs to go up by 4 times in order to maintain the same resonator transfer function. In this design, we chose R and C to be such values that a fair trade-off is achieved between noise and power consumption. The unit R and C are 250 Ω and 4 pF for the 1st resonator stage, and 1 kΩ and 1 pF for the following stages. Larger R's and smaller C's are chosen for the 2^{nd}-4^{th} stages, where the noise requirements are not as strict, thereby saving power consumption.

Increase the coefficient b_1**.** Reducing R alone is not enough to achieve the target SNR. Another way to suppress thermal noise is to increase b_1. Doubling b_1 reduces the thermal noise to almost a quarter, giving us almost 6 dB improvement in SNR. From Equation 4.10, the loop gain of the 1^{st} resonator stage is proportional to b_1. This means, if we increase b_1 to twice its value, the signal swing at the output needs

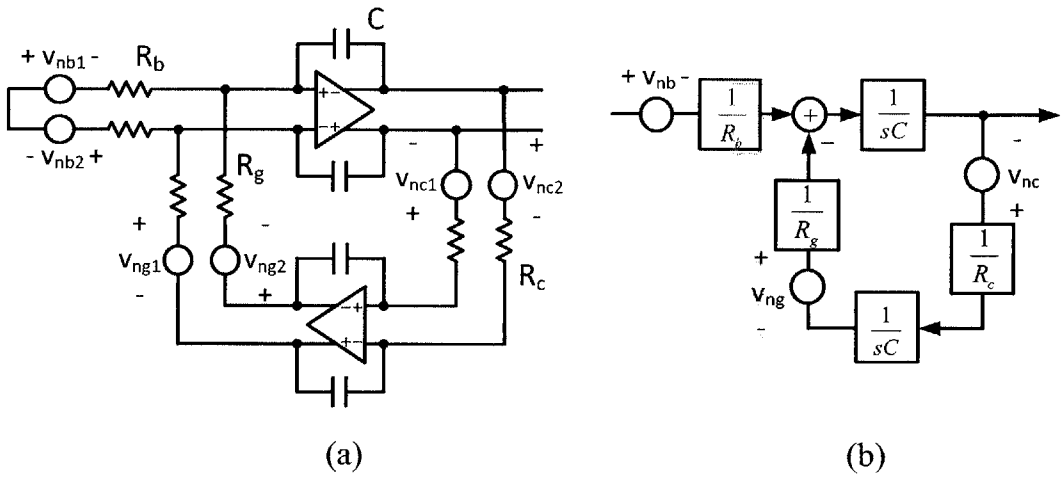


Figure 4-5: (a) Circuit and (b) block diagram for the 1st resonator stage with noise sources.

to be doubled as well. Therefore, we propose a dual-supply resonator design. The input and output stages of the resonator operate under a higher supply voltage of 2.5 V, whereas the other parts of the circuit operate under the normal supply voltage of 1.2 V. In this way, the signal swing is doubled, and a 6 dB improvement in SNR is achieved. Due to the higher power supply voltage, the power consumption of the 1st resonator stage becomes twice as much. However, compared with increasing R alone, this is a better trade-off between power and noise.

In addition, as introduced in Section 3.4.2, the feed-forward coupling path, with the coefficient of b_2, enables us to increase b_1 further. This provides additional noise reduction. As shown in Table 3.2, with both $b_2 = 0.396$ and a dual-supply loop filter, the value of b_1 is boosted by 7 times. This translates into a SNR improvement of almost 17 dB.

4.1.3 Loop Filter Overview

A dual-supply loop filter is designed for the CT bandpass $\Delta\Sigma$ modulator. Figure 4-6 shows the detailed schematic of the loop filter. The shaded op amps, A_1 and A_2, operate under 2.5-V/1.2-V dual power supply. The first resonator stage thus operates

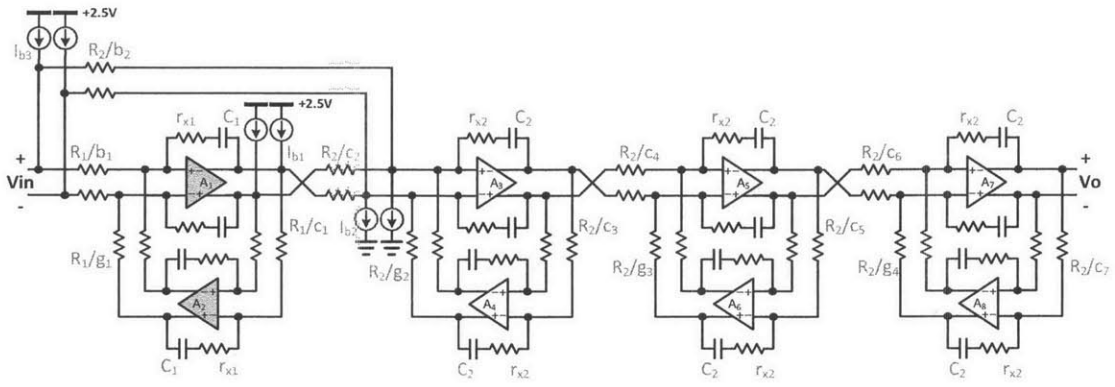


Figure 4-6: Top-level circuit implementation of the loop filter.

at a higher common-mode voltage of 1.25 V, whereas the common-mode voltages of the other stages are 0.65 V. Therefore, current sources with the values of I_{b1}, I_{b2}, and I_{b3} are employed to adjust the difference in common-mode voltages. The values of these current sources are calculated as follows:

$$I_{b1} = \frac{\Delta V_{cm}}{\left(\frac{R_2}{c_2}\right)} \approx 85\ \mu A \tag{4.14}$$

$$I_{b3} = \frac{\Delta V_{cm}}{\left(\frac{R_2}{b_2}\right)} \approx 155\ \mu A \tag{4.15}$$

$$I_{b2} = I_{b1} + I_{b3} \approx 240\ \mu A \tag{4.16}$$

The component values of the loop filter are listed in Table 4.1. The values of the coefficients can be found in Table 3.2.

4.2 Op Amp

Op amps are the key building blocks of the loop filter. The op amps in a CT $\Delta\Sigma$ modulator must satisfy two gain requirements [3]:

Table 4.1: Component values of the loop filter.

	1st stage	2nd - 4th stages
Power supply VDD	Dual 2.5 V/1.2 V	1.2 V
Common-mode Voltage V_{cm}	1.25 V	0.65 V
Unit resistor value R	400 Ω	1000 Ω
Unit capacitor values C	2.5 pF	1 pF
Series resistor r_x	2.5 Ω	7.5 Ω
Tuning factor of g	1.015	1.255
Biasing Current	$I_{b1} = 85\ \mu A$, $I_{b2} = 240\ \mu A$, $I_{b3} = 155\ \mu A$	

High in-band loop gain A very high gain is needed in the signal band to ensure high linearity and sufficient coefficient accuracy. For the feedback topology, a typical in-band loop gain requirement is 40 $\sim$ 50 dB. For a CT bandpass $\Delta\Sigma$ modulator, this requirement can be very difficult to fulfill if the center frequency is at hundreds of MHz.

Moderate loop gain around $\frac{f_s}{2}$ A moderate loop gain of 10 $\sim$ 20 dB is needed in the vicinity of $\frac{f_s}{2}$ to process the injected currents from the feedback DACs. For a bandpass $\Delta\Sigma$ modulator, in particular, this requirement is often automatically fulfilled if the aforementioned high in-band loop gain requirement is met. This is because, for a bandpass modulator, the signal band typically locates within only a few octaves of $\frac{f_s}{2}$.

In our design, the specifications for the op amps are 50 dB of loop gain at 250 MHz for A_1 and A_2, and 40 dB of loop gain at 250 MHz for $A_3 \sim A_8$. These requirements translate into gain-bandwidth (GBW) products of 79 and 25 GHz respectively. For traditional op amp designs with a single-pole roll-off, it is impossible to achieve these GBW requirements. In our design, multistage feed-forward op amps are employed [3] [18] [8] [19]. As is explained later in section 4.2.1, multistage feed-forward op amps have the potential to achieve both high gain and high unity-gain bandwidth

with good phase margin, which renders multistage feed-forward op amps a good fit for our design.

Two different op amp designs are proposed in this work. A 2.5-V/1.2-V dual-supply op amp is designed for the 1st resonator stage (A_1 and A_2). A single-supply op amp is employed in the other resonator stages ($A_3 \sim A_8$). Both op amp designs adopt the multistage feed-forward topology. The basic ideas of multi-stage feed-forward op amps are explained in Section 4.2.1. Sections 4.2.2 and 4.2.3 describe in detail the transistor-level design of the two op amps.

4.2.1 Multistage Feed-forward Op Amp

The basic idea of a multi-stage feed-forward op amp is to combine the high speed of a single-stage amplifier with the high gain of a multistage amplifier by adding them up [3].

As an example, Figure 4-7 shows a 3rd-order feed-forward op amp, which consists of a 1st-order path (g_{mc}), a 2nd-order path (g_{mb1} and g_{mb2}), and a 3rd-order path (g_{ma1}, g_{ma2} and g_{ma3}). Figure 4-8 shows the ideal frequency response of an example 3rd-order feed-forward op amp. From the graph, we observe that the path with the highest gain always dominates the response. Thus, the transfer function follows the 3rd-order path at low frequency, achieving high gain, and switches to the 1st-order path at high frequency, achieving both a high crossover frequency and a good phase margin.

One thing to note here is that the shift from a high-order response to a 1st-order response must take place gradually in order for the op amp to maintain stability [3]. The 2nd-order path and the interstage capacitors enable us to control the transition.

Another thing to note is that a multistage feed-forward op amp is a conditionally stable system. The op amp can go unstable if the signal swing is sufficiently large that causes the effective again of the internal stages to reduce [3]. For a $\Delta\Sigma$ modulator, problem of this kind is avoided because the major feedback loop of the modulator ensures stability and maintains the signal swing throughout the loop filter.

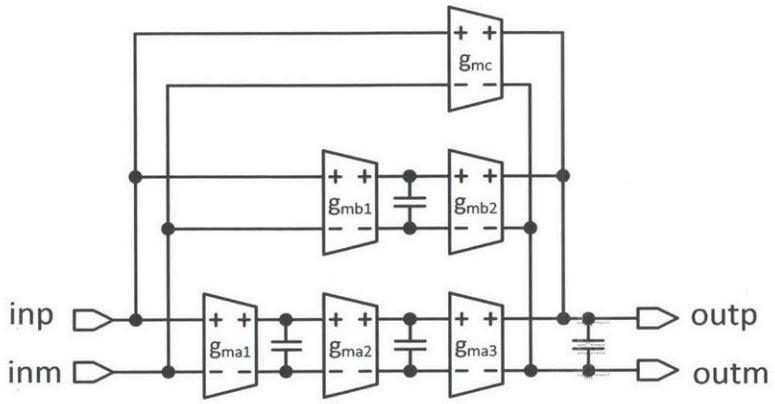


Figure 4-7: Conceptual block diagram of a 3rd-order multistage feed-forward op amp.

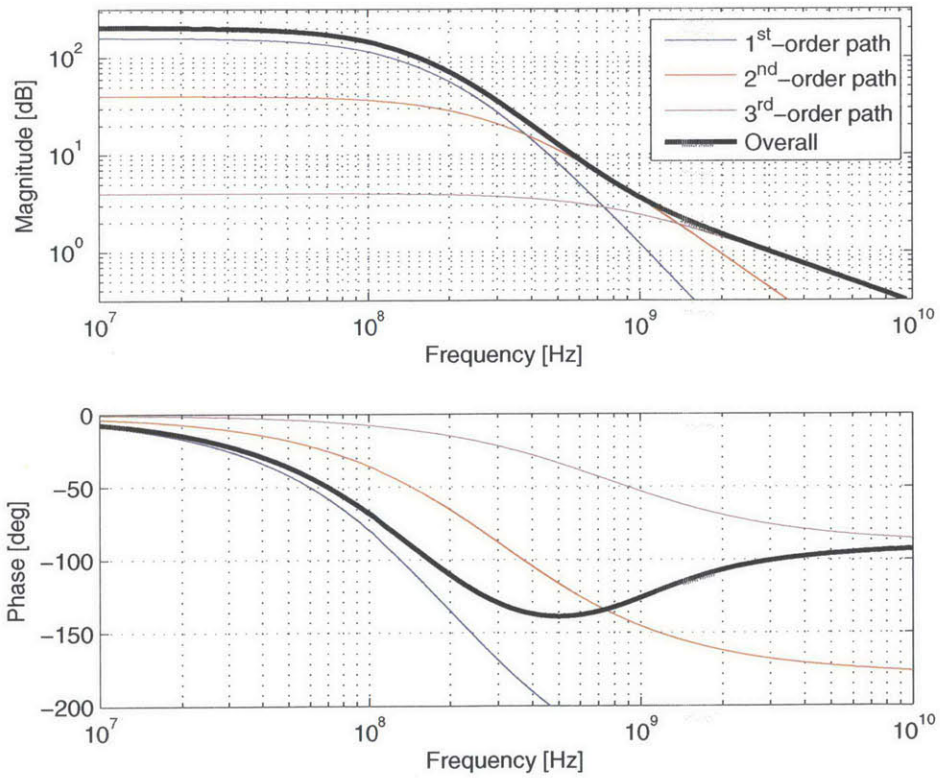


Figure 4-8: Frequency response of an example 3rd-order multistage feed-forward op amp.

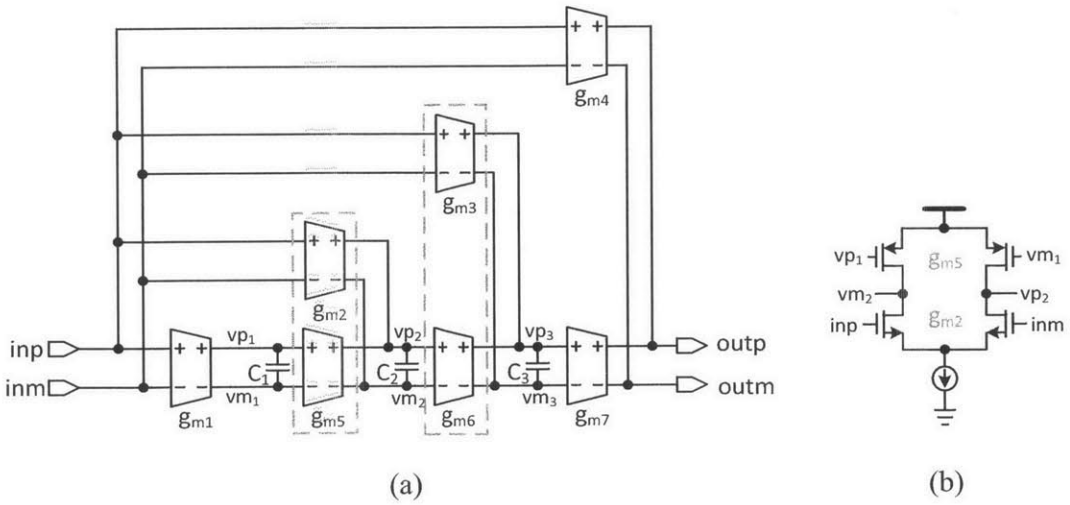


Figure 4-9: (a) Block diagram of the single-supply 4th-order feed-forward op amp. (b) Conceptual circuitry for the current-sharing gm cells.

4.2.2 A Single-supply 4th-order Feed-forward Op Amp

A single-supply 4th-order feed-forward op amp is designed for $A_3 \sim A_8$. Figure 4-9(a) shows the block diagram of this op amp. Compared with the 3rd-order topology displayed in Figure 4-7, this design is more power efficient because it incorporates gm cells among high order paths. For example, g_{m6} is now shared between the 3rd- and 4th-order paths, and g_{m7} is shared among the 2nd-, 3rd-, and 4th-order paths. To further reduce the power consumption, current-sharing is introduced to intermediate gm cells between g_{m2} and g_{m5}, and between g_{m3} and g_{m6}. Figure 4-9(b) shows a conceptual implementation of the current-sharing stage, where both NMOS and PMOS transistors provide transconductance.

Figure 4-10 and 4-11 show the complete schematic of the 4th-order feed-forward op amp. It consists of four stages. The 1st stage implements g_{m1}, the 2nd stage g_{m2} and g_{m5}, the 3rd stage g_{m3} and g_{m6}, and the output stage g_{m4} and g_{m7}. Table 4.2 lists the transistor dimensions, currents, and power consumption of each stage. The op amp consumes a total power of 20.2 mW, more than half of which goes to the output stage. Some special circuit techniques are employed in this op amp and are explained

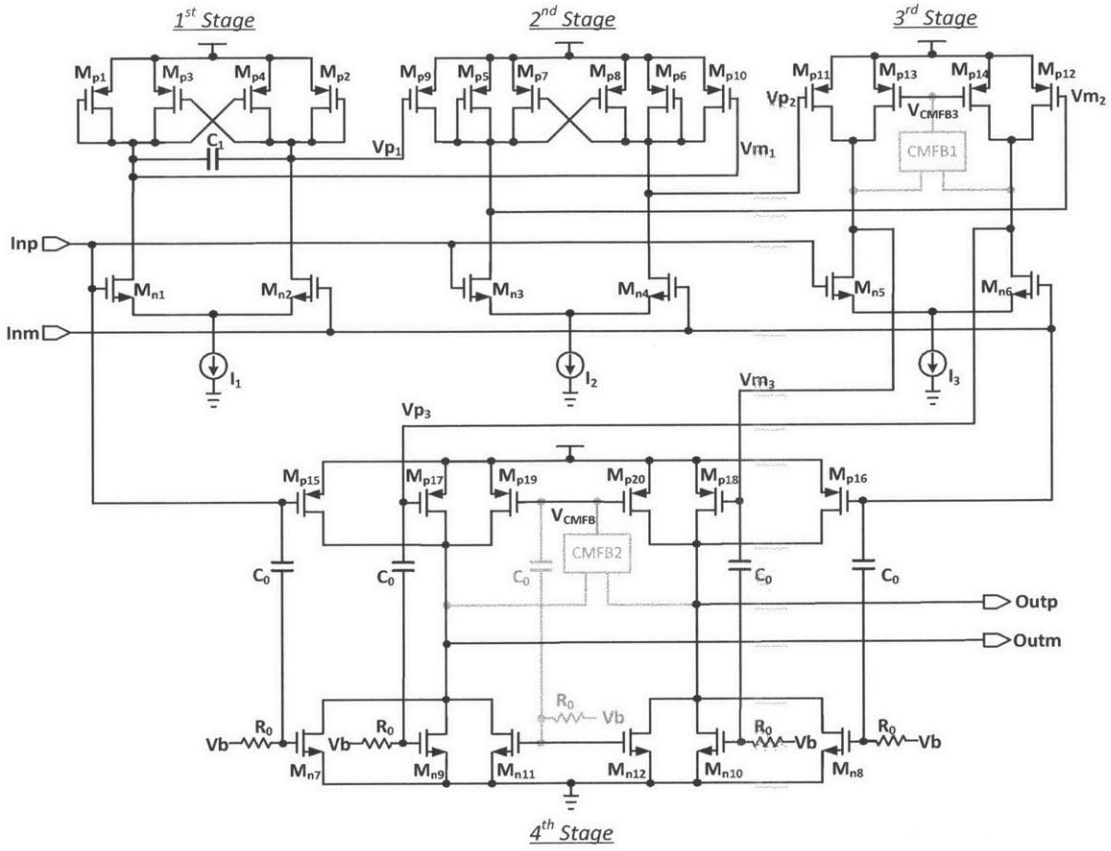


Figure 4-10: Schematic of the single-supply 4$^{\text{th}}$-order feed-forward op amp.

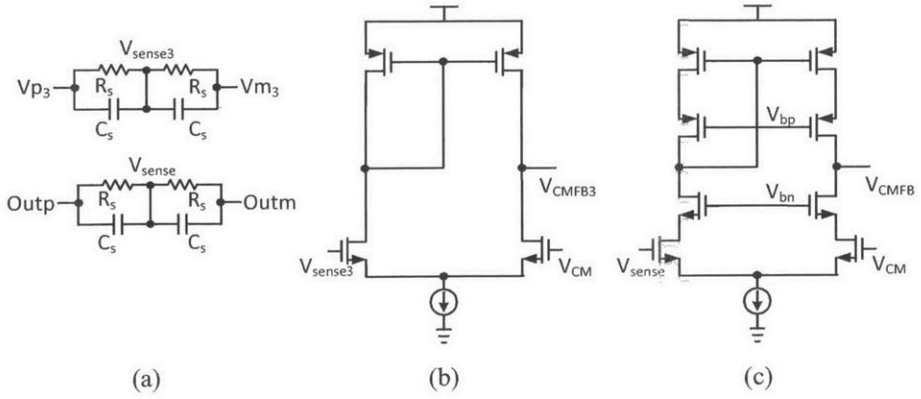


Figure 4-11: CMFB circuity of the 4$^{\text{th}}$-order feed-forward op amp. (a) Sensing network. (b) CMFB op amp for the 3$^{\text{rd}}$ stage. (c) CMFB op amp for the output stage.

Table 4.2: Summary for the 4th-order feed-forward op amp.

1st stage			2nd stage			3rd stage			4th stage		
g_{m1}	M_{n1-2}	$3W_n$	g_{m2}	M_{n3-4}	$2W_n$	g_{m3}	M_{n5-6}	$12W_n$	g_{m4}	M_{n7-8}	$16W_n$
										M_{p15-16}	$32W_p$
			g_{m5}	M_{p9-10}	$3W_p$	g_{m6}	M_{p11-12}	$16W_p$	g_{m7}	M_{n9-10}	$16W_n$
										M_{p17-18}	$32W_p$
$I_1 = 836.4\ \mu A$			$I_2 = 529.3\ \mu A$			$I_3 = 3.57\ mA$			$I_4 = 11.15\ mA$		
						$I_{CMFB1} = 400.8\ \mu A$			$I_{CMFB2} = 367.6\ \mu A$		
$P_1 = 1.0\ mW$			$P_2 = 0.6\ mW$			$P_3 = 4.8\ mW$			$P_4 = 13.8\ mA$		
$W_n = 10\ \mu m$, $W_p = 12.5\ \mu m$, $L = 90\ nm$									$P_{total} = 20.2\ mW$		

as follows:

Current sharing As is mentioned earlier, current-sharing is employed in the 2nd and 3rd stages where both the NMOS differential pair and the PMOS pseudo differential pair serve as gm cells. In the circuit implementation, as shown in Figure 4-10, the PMOS pseudo-differential pair is placed in parallel with the loading, i.e. a cross-coupled PMOS pair for the 2nd stage, and a current mirror for the 3rd stage. In order for the op amp to have a smooth transition in the transfer function, the lower-order paths should be made faster than the higher-order ones, meaning that g_{m2} and g_{m3} needs to be larger than g_{m5} and g_{m6} respectively. Therefore, g_{m2} and g_{m3} are implemented with the differential NMOS pair that provides a greater transconductance, while g_{m5} and g_{m6} are implemented with the pseudo-differential PMOS pair.

Cross-coupled loading network PMOS cross-coupled loading networks are used in the 1st and 2nd stages of the op amp. Take the first stage as an example, the four PMOS transistors, $M_{p1} \sim M_{p4}$, share the same dimension, carry the same dc currents, and have the same small signal transconductance g_m. This type of loading gives three major benefits:

- The cross-coupled loading networks provide well-defined output common-mode for the 1st and 2nd stages, eliminating the need for additional common-mode feedback (CMFB) circuitry. For a multi-stage feed-forward op amp with com-

plicated CMFB loops, this feature is particularly beneficial.

- The biasing points provided by the PMOS cross-coupled pairs offer convenient operating points for the succeeding gm stages that are pseudo-differential PMOS pairs, i.e. g_{m5} and g_{m6}.
- The cross-coupled loading networks provide high gain. The cross-coupled pair, M_{p3} and M_{p4} for example, gives a negative small-signal resistance of $-\frac{1}{g_m}$, which cancels the resistance from the diode-connected transistors M_{p1} and M_{p2}. Therefore, the effective output resistance of this loading network is $\frac{r_o}{2}$, where r_o denotes the output resistance of transistors $M_{p1} \sim M_{p4}$. This gm stage thus provides a gain on the order of $g_m r_o$.

One disadvantage of the cross-coupled loading network is its limited signal swing. Therefore we only employ it in the 1st and 2nd stages of the op amp where the signal swing is still small. As the signal goes through more stages of amplification, its amplitude grows. A simple current mirror loading, together with a CMFB loop, is thus used for the 3rd stage. For the 4th op amp stage, the signal swing becomes even larger, and a push-pull output stage is employed. A CMFB loop is also needed for this stage. The schematics of the sensing network and the CMFB op amps are shown in Figure 4-11, where the values of R_s and C_s are 10 kΩ and 100 fF respectively.

Pseudo-differential push-pull output stage The output stage is the most power hungry part of this op amp. It has the following requirements:

- The signal swing needs to be maximized in order to increase SNR.
- A large current is needed for the signal to swing fast enough.
- A large transconductance is needed to implement the fast 1st-order feed-forward path.

A pseudo-differential push-pull output stage is proposed to fulfill the above requirements. The push-pull topology takes up only $2V_{DS,SAT}$ between VDD and GND, making possible a signal swing of 900 mV out of 1.2 V power supply. The input signals (Inp/Inm and Vp_3/Vm_3) are ac coupled from the PMOS pseudo-differential pairs to NMOS ones. In the small-signal sense, the PMOS and NMOS pseudo-differential

pairs are connected in parallel, maximizing $\frac{g_m}{I_{bias}}$. The values of the coupling resistor R_0 and capacitor C_0 are 25 kΩ and 10 pF respectively.

4.2.3 A Dual-supply 5th-order Feed-forward Op Amp

The 1st resonator stage is crucial to the modulator performance because its noise and distortion are added to the input directly. A dual 2.5-V/1.2-V supply 5th-order feed-forward op amp is designed for A_1 and A_2 to fulfill the 50 dB in-band gain requirement. Figure 4-12 shows the block diagram of this op amp. It has a similar topology to the single-supply 4th-order design. To minimize power consumption, the 2.5 V supply voltage is used only in the input and output stages. Thick lines on the gm cells indicate the place where the 2.5 V power supply is employed.

Figure 4-13 shows the schematic of the input and output stages of the 5th-order op amp that operate under 2.5 V. High-voltage devices, which are denoted with thick gate in the schematic, are employed in the circuit to protect the standard devices from the 2.5 V power supply. These devices, however, are slow, and are thus only used as current sources and cascodes.

According to Figure 4-13(a), the 2.5-V input stage is a folded-and-telescopic gm stage [3]. In a small signal sense, the PMOS and NMOS input differential pairs are connected in parallel, so that the $\frac{g_m}{I_{bias}}$ ratio is maximized. The PMOS cascode devices, M_{pc} and M_{pd}, serve as folded cascode for the NMOS differential pair M_{na} and M_{nb}, and telescopic cascode for the PMOS differential pair M_{pa} and M_{pb}. The common mode voltage is reduced from 1.25 V at the input Inp/Inm to 650 mV at the output Vop/Vom, so as to interface with the subsequent 1.2 V gm stages. 2.5-V devices are employed as current sources.

According to Figure 4-13(b), the 2.5-V output stage has a pseudo-differential push-pull topology that resembles the output stage of the 4th-order feed-forward op amp. The input signal, with a common-mode voltage of 650 mV, is fed to the NMOS pseudo-differential pair M_{ne} and M_{nf}, and are ac-coupled to the PMOS pseudo-differential M_{pe} and M_{pf}. The complementary NMOS/PMOS pairs are employed to maximize the transconductance of the output stage [3]. 2.5-V devices are added as cascodes.

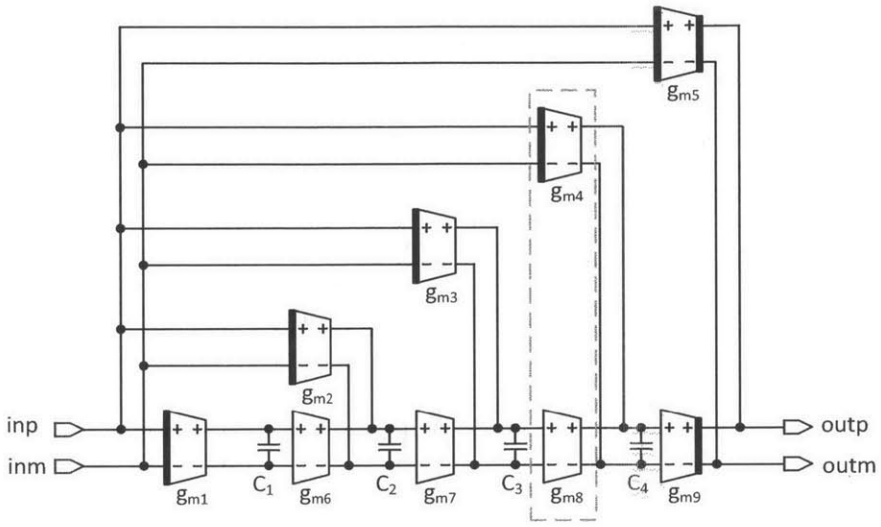


Figure 4-12: Block diagram of the dual-supply 5^{th}-order feed-forward op amp.

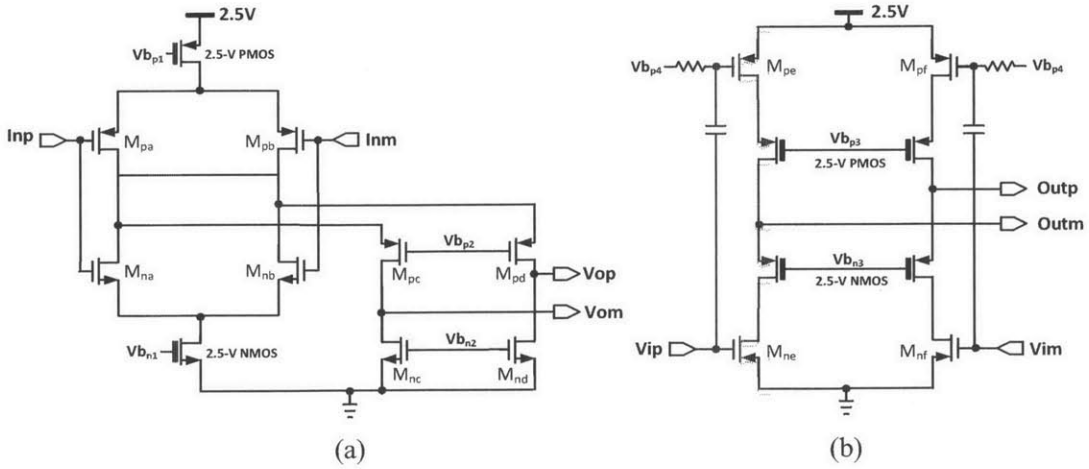


Figure 4-13: (a) Input and (b) output stages of the dual-supply 5^{th}-order feed-forward op amp [3].

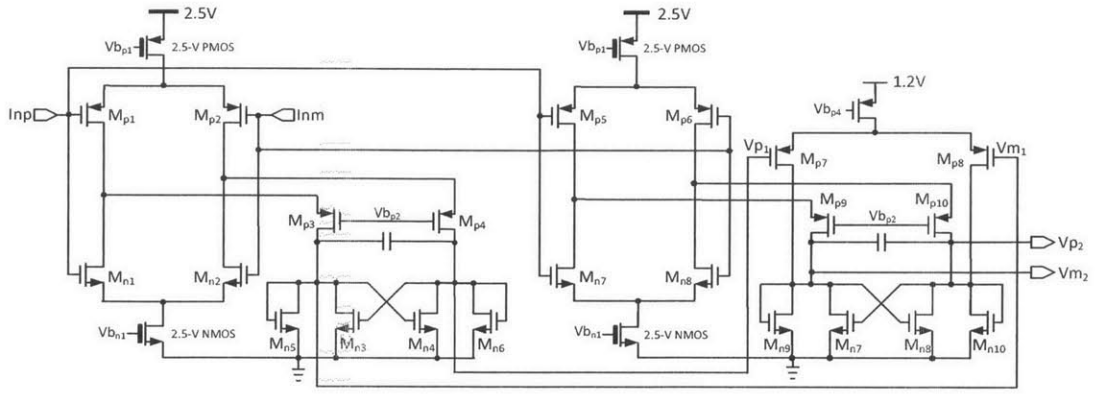


Figure 4-14: Schematic of the 5$^{\text{th}}$-order feed-forward op amp - 1$^{\text{st}}$ and 2$^{\text{nd}}$ stage.

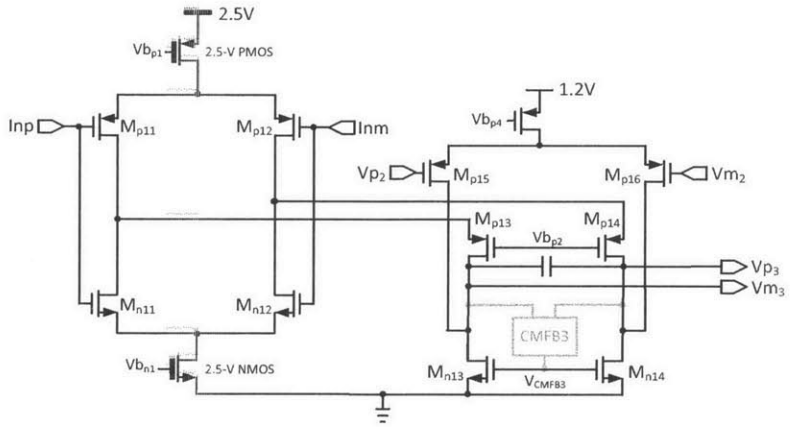


Figure 4-15: Schematic of the 5$^{\text{th}}$-order feed-forward op amp - 3$^{\text{rd}}$ stage.

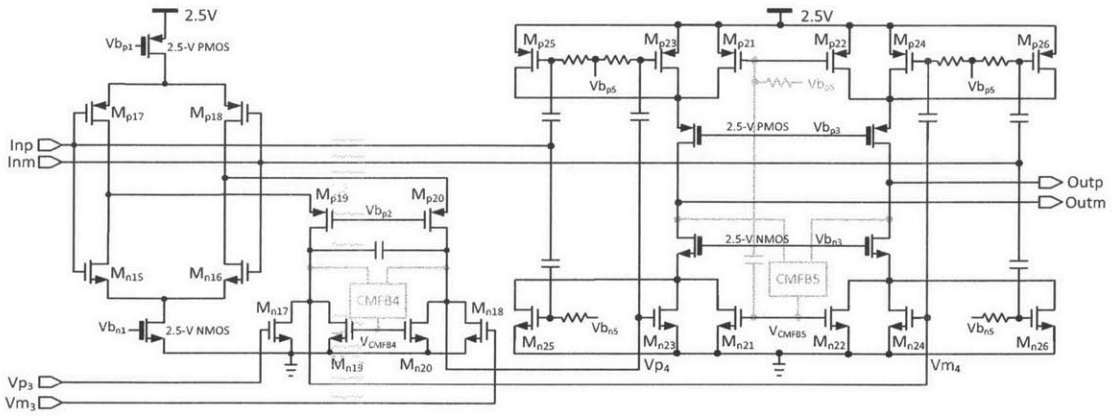


Figure 4-16: Schematic of the 5$^{\text{th}}$-order feed-forward op amp - 4$^{\text{th}}$ and 5$^{\text{th}}$ stage.

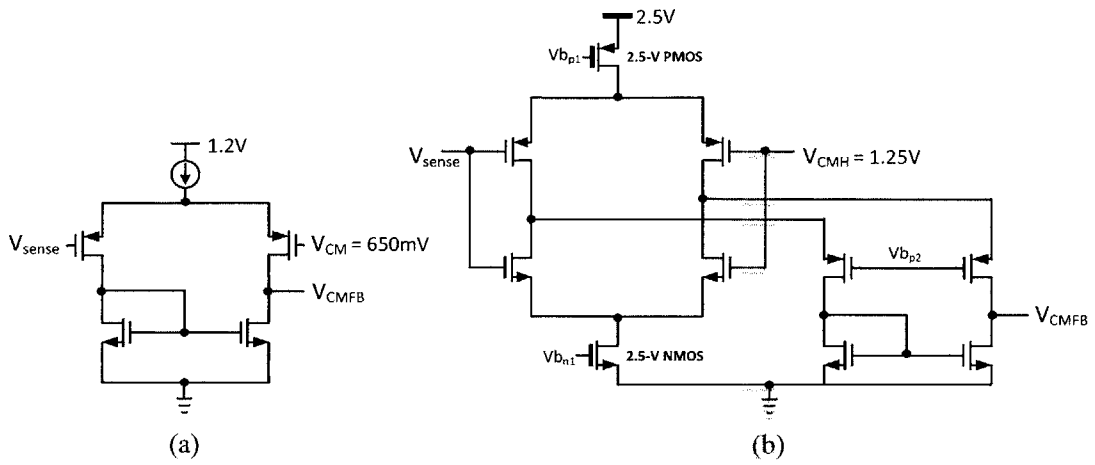


Figure 4-17: Schematic of the CMFB op amp used in the (a) 3rd, 4th, and (b) 5th stage of the 5th-order feed-forward op amp.

Minimum number of devices are stacked between VDD and GND to maximize the output signal swing.

Figures 4-14, 4-15, and 4-16 altogether display the complete schematic of the dual-supply 5th-order feed-forward op amp. The circuit techniques that we have described for the single-supply 4th-order design are employed here as well:

- NMOS cross-coupled loading networks are used in the 1st and 2nd stages of the op amp to provide well-defined common-mode levels.
- NMOS current mirror loads, together with CMFB circuits, are used in the 3rd and 4th stages to increase signal swing.
- Current-sharing is employed in the 4th-stage where the power consumption becomes significant.
- The pseudo-differential push-pull output stage is used.

Figure 4-17 shows the schematics of the CMFB op amps. For the output stage, since the output common mode voltage is 1.25 V, a 2.5-V CMFB op amp is designed.

Operating under high voltage and consuming large current, this dual-supply 5th-order feed-forward op amp is the most power hungry building block of the modulator. Table 4.3 summarizes the transistor dimensions, currents, and power consumptions of this op amp. Just like the 4th-order design, the most power hungry stage for

Table 4.3: Summary for the 5th-order feed-forward op amp.

1st stage		2nd stage		3rd stage		4th stage		5th stage	
g_{m1}	M_{n1-2} $5W_n$ M_{p1-2} $10W_p$	g_{m2}	M_{n7-8} $2W_n$ M_{p5-6} $4W_p$	g_{m3}	M_{n11-12} $4W_n$ M_{p11-12} $8W_p$	g_{m4}	M_{n15-16} $8W_n$ M_{p17-18} $16W_p$	g_{m5}	M_{n25-26} $48W_n$ M_{p25-26} $48W_p$
		g_{m6}	M_{p7-8} W_p	g_{m7}	M_{p15-16} $2W_p$	g_{m8}	M_{n17-18} $6W_n$	g_{m9}	M_{n23-24} $24W_n$ M_{p23-24} $24W_p$
$I_{gm1} = 2.648\ mA$		$I_{gm2} = 1.028\ mA$ $I_{gm6} = 240.3\ \mu A$		$I_{gm3} = 2.013\ mA$ $I_{gm7} = 507.7\ \mu A$ $I_{CMFB3} = 483.4\ \mu A$		$I_{gm4+gm8} = 3.971\ mA$ $I_{CMFB4} = 484.2\ \mu A$		$I_{gm5} = 10.094\ mA$ $I_{gm9} = 5.032\ mA$ $I_{CMFB5} = 5.884\ mA$	
$P_1 = 6.62\ mW$		$P_2 = 2.86\ mA$		$P_3 = 6.22\ mW$		$P_4 = 10.51\ mW$		$P_5 = 52.53\ mW$	
$W_n = 10\ \mu m$, $W_p = 25\ \mu m$, $L = 90\ nm$								$P_{total} = 78.7\ mW$	

5th-order op amp is still the output stage. The currents from the 2nd to the 4th stages grow steadily in order for the op amp transfer function to shift gradually from the high-order to the low-order path. All the input gm cells, i.e. $g_{m1} \sim g_{m5}$, consume considerable amount of current, which serves to reduce the input-referred thermal noise. The 1.2-V intermediate stages, i.e. g_{m6} and g_{m7}, consume negligible amount of power.

4.3 Summary

In this chapter, two major design challenges for the loop filter are described and discussed. For one, op amp non-ideality distorts the loop transfer function, degrades modulator SNR, and brings about stability issues. For another, thermal noise from the resistors of the 1st resonator stage poses a SNR-liming factor. The former problem is alleviated by adding series resistors r_x and tuning the coefficient of g. The latter problem is solved by a employing a 2.5-V/1.2-V power supply in combination with a feed-forward coupling path.

The design of the multi-stage feed-forward op amps is explained in this chapter as well. Two op amps are presented, namely the dual-supply 5th-order and the single-supply 4th-order feed-forward op amps. Circuit techniques, such as current-sharing, cross-coupled loading, and pseudo-differential push-pull output stages, are described.

The simulation results of the two op amps are offered in Section 6.2.

Chapter 5

Feedback Paths Implementation

This chapter describes the design of the feedback paths of the modulator. As shown in Figure 5-1, the feedback paths consist of a 15-level quantizer, a DAC driver, and 8 current-steering DACs. The quantizer digitizes the signal from the loop filter and produces complementary thermometer codes that serve as the output of the whole modulator. The DACs take the codes, convert them back into analog signals, and feed them back into the loop filter. The ELD introduced by the feedback signal paths are critical to the stability of the modulator. Thus, in the design procedure, efforts have been made to ensure a fast and accurate timing. Non-ideality from DAC_1 and DAC_2 affects the modulator directly, demanding stringent noise and linearity specifications from these two blocks. The accuracy requirement on the quantizer, however, is relaxed since any errors from the quantizer are filtered by the NTF and thus are subjected

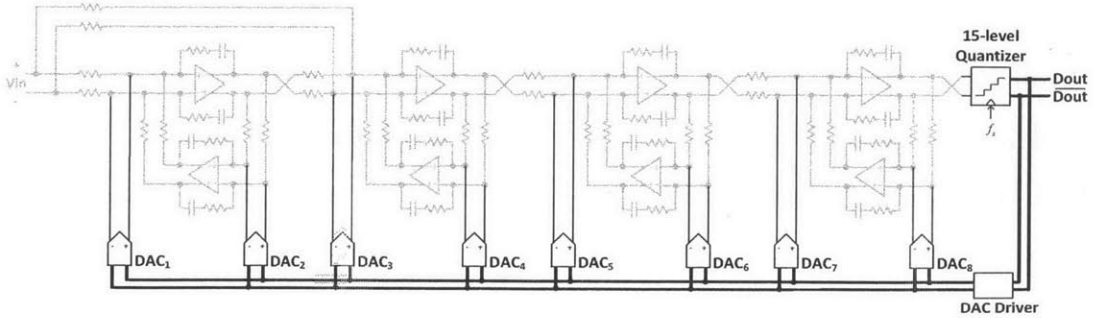


Figure 5-1: Modulator feedback signal paths.

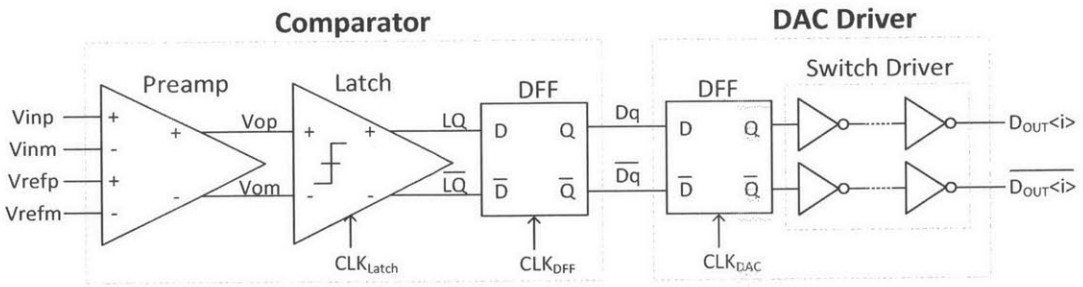


Figure 5-2: Block diagram of the comparator and DAC driver slice [4].

to the same attenuation as the quantization noise.

The organization of this chapter is as follows. Implementation details of the quantizer (Section 5.1), the DAC driver (Section 5.2), and the current-steering DACs (Section 5.3) are explained respectively, followed by the timing analysis of the whole feedback paths (Section 5.4).

5.1 Quantizer

The quantizer is essentially a 15-level flash ADC. It consists of 14 comparator cells, the reference voltages of which are generated from a 15-tap resistive ladder. Each comparator drives a slice of DAC driver, as shown in the block diagram in Figure 5-2. In order to achieve a good trade off between speed and power, the comparator is implemented as a three-stage cascade of a preamplifier, a latch, and a D flip-flop (DFF) [4]. The preamplifier amplifies the input small signal in a continuous-time fashion and serves to reduce the offset of the comparator. The latch produces a rail-to-rail output signal through positive feedback. The DFF samples the rail-to-rail signal and feeds it to both the modulator output and the DAC driver with half a clock cycle delay.

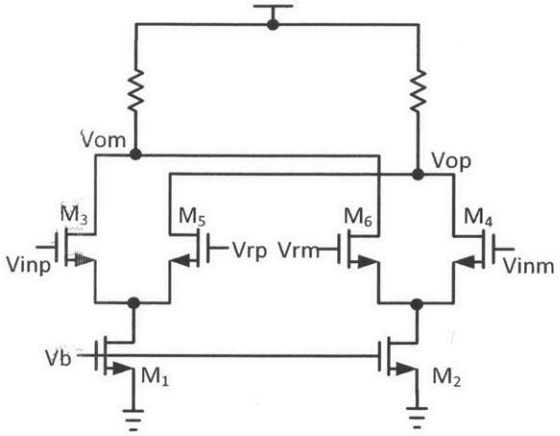
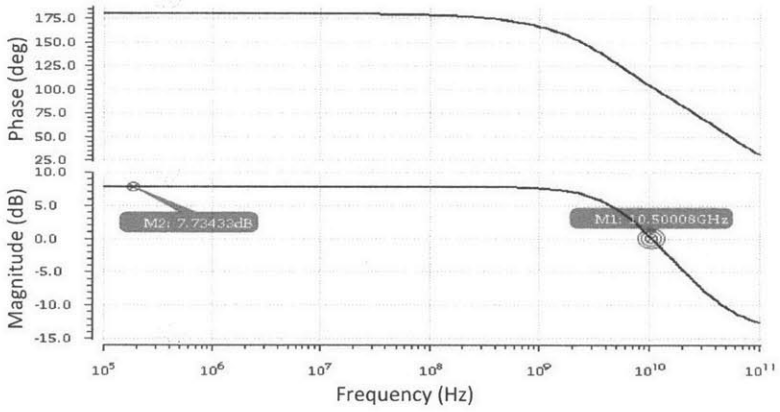
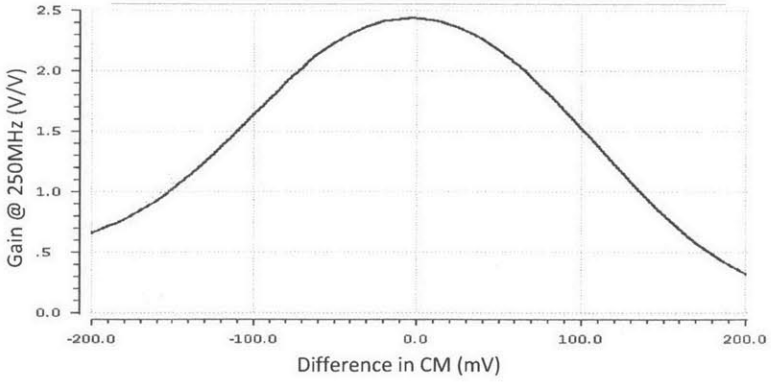


Figure 5-3: Schematic of the preamplifier.



(a)



(b)

Figure 5-4: Preamplifier characteristics: (a) frequency response and (b) gain variation versus CM difference between input and reference signals.

5.1.1 Preamplifier

The preamplifier is a resistive-loaded NMOS differential pair, as shown in Figure 5-3. The purpose of this preamplifier is to compare the differential input signal with a differential reference signal, and amplify the difference [20]. The input referred offset of the comparator is reduced now that the offset from the subsequent latch stage is divided by the gain of the preamplifier. The preamplifier also isolates the latch kick-back noise from the the loop filter output. In this design, the gain of the preamplifier is 2.4 V/V, or 7.7 dB, and the unity gain frequency 10.5 GHz, as shown in Figure 5-4(a).

One major disadvantage of this type of preamplifier is that any common-mode (CM) difference between the input signal and the reference signal results in preamplifier gain reduction [20]. This in turn increases the input-referred offset of the comparator. Figure 5-4(b) shows the simulated preamplifier gain at the center frequency of 250 MHz versus the CM level difference between input and reference signals. In order to maintain a gain above 2.0 V/V, the CM levels of the reference and the input signals should be kept within 80 mV of each other.

5.1.2 Latch

The latch used in this design is a NMOS differential input pair that drives a cross-coupled inverter pair, as shown in Figure 5-5. The purpose of the latch is to accept the signals from the preamplifier and further amplify them to rail-to-rail. The positive feedback introduced by the cross-coupled inverter pair makes possible a fast decision. The absence of static power consumption is another advantage of this latch topology.

The operation of the latch is briefly explained as follows. The latch operates in two phases, namely the pre-charge phase Φ_1 and the evaluation phase Φ_2. During Φ_1 when the clock signal $\mathrm{CLK_{Latch}}$ is low, both latch outputs, LQ and $\overline{\mathrm{LQ}}$, are pre-charged to VDD through small PMOS transistors M_9 and M_{10}. The lower limit on the size of these transistors is determined by their capability to pre-charge the output nodes within half a clock cycle [21]. Thus, both M_5 and M_6 are turned on and their

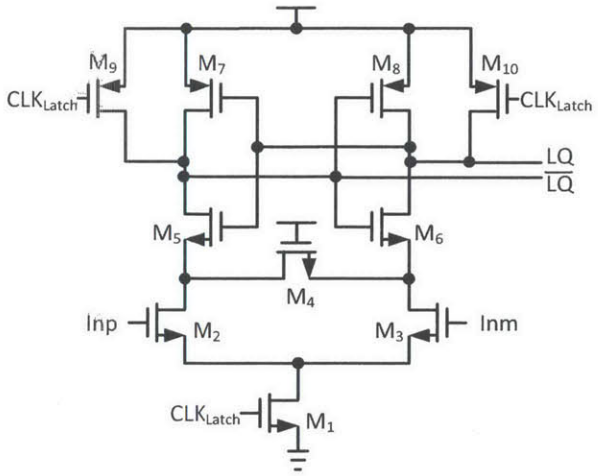


Figure 5-5: Schematic of the latch.

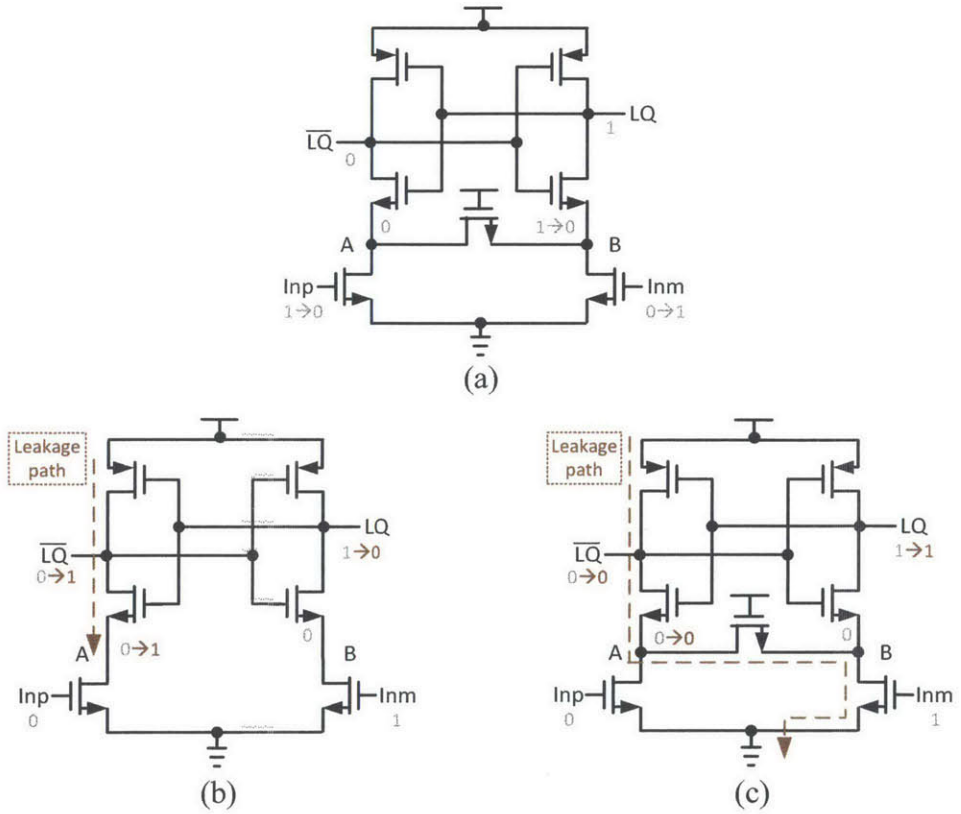


Figure 5-6: Function of the shorting transistor M_4 [5]: (a) Change in input signal during Φ_2; (b) w/o shorting device; (c) w/ shorting device.

sources are charged up to VDD-V_{thN}. The tail transistor M_1 is turned off so that no static power is consumed.

The latch starts evaluation at the rising edge of CLK_{Latch}. M_1 is turned on and begins to conduct current. The differential pair M_2 and M_3 is enabled and starts amplifying the input signal. The signal is further amplified to rail-to-rail through the positive feedback between the cross-coupled inverters consisting of $M_5 \sim M_8$. When the inverter pair flips to its stable state, the latch gives a stable and valid output. No static current is consumed during this phase either.

The shorting transistor M_4 is necessary to maintain the correct output levels throughout Φ_2 despite the changes in the input signal [5]. Figure 5-6 serves as an example. Suppose $\overline{LQ}$ is forced low at the rising edge of CLK_{Latch}, as shown in Figure 5-6(a). If the input signal changes state, $\overline{LQ}$ becomes floating low and is susceptible to the leakage current from the PMOS transistor in the absence of M_4. A wrong output may thus result. This scenario is illustrated in Figure 5-6(b). With M_4, however, a low impedance path from the leaking PMOS transistor to GND always exists, as shwon in Figure 5-6(c). As a result, the leakage current never builds up, and the latch outputs maintain their correct value throughout Φ_2 until the beginning of the next clock cycle. In addition, the shorting switch M_4 also removes the hysteresis effect of the latch by erasing the residual charge from the previous state.

5.1.3 D Flip Flop

The DFF is responsible for latching the comparator output within half a clock cycle delay. A typical sense-amplifier-based flip-flops usually consists of two stages, which is a sense-amplifier (SA) in the first stage and a set-reset (SR) latch in the second, as is displayed in Figure 5-7. For this type of DFF, a fast decision time is achieved due to a strong positive feedback introduced by the cross-coupled inverters from the SA. The differential input pair reduces the offset. Full-swing outputs are provided and no static power is consumed.

In this design, however, both DFF stages are modified due to considerations such as the low supply voltage, the kick-back noise, and the timing of the outputs. The

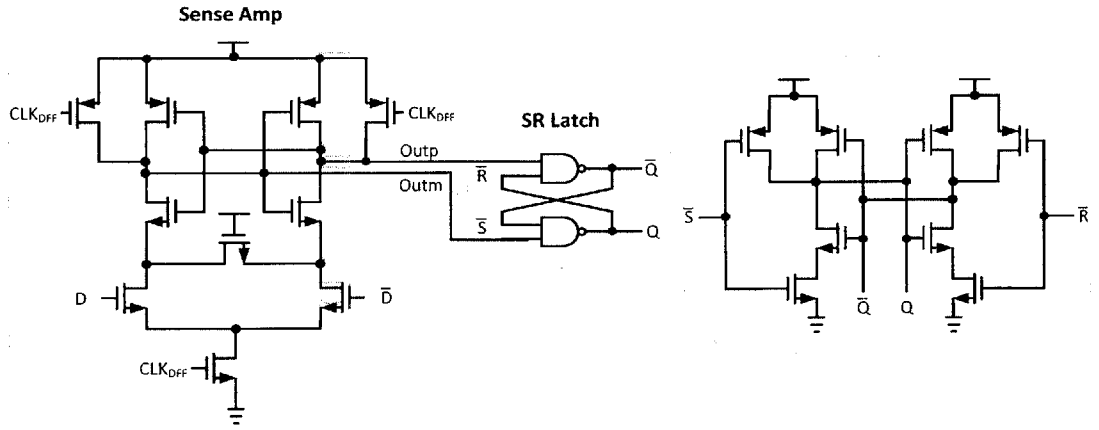


Figure 5-7: Conventional SA-based DFF.

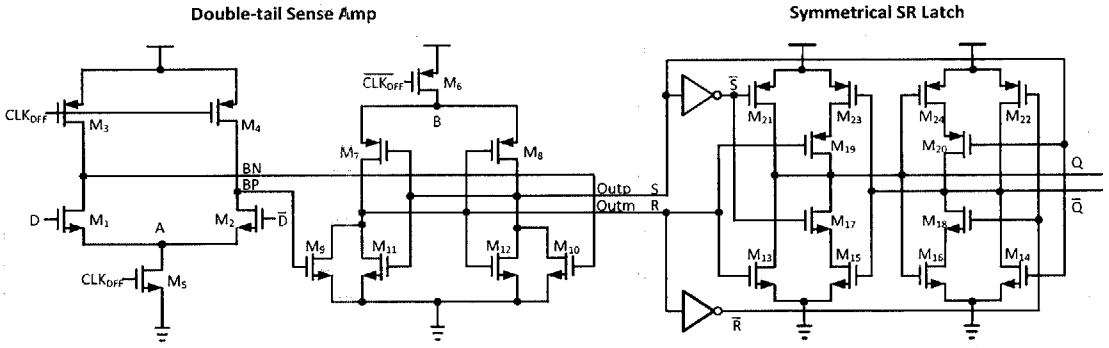


Figure 5-8: DFF with a double-tail SA and a symmetrical SR latch.

resulting DFF consists of a double-tail SA and a symmetrical SR latch. Figure 5-8 shows the schematic of the proposed DFF. The design considerations are explained as follows.

Double-tail Sense Amplifier

A double-tail SA uses one tail for the input stage and the other for the latching stage, as shown in Figure 5-8. Compared to conventional SA, this topology enjoys the following advantages [21]:

- This design is more amenable to low supply voltages since only three transistors

are stacked between VDD and GND.

- The separation of the input from the latching stage makes it possible to optimize speed and offset separately. A large current in the latching stage makes the circuit faster while a small current in the input stage reduces offset.
- Transistors M_9 and M_{10} shield the output from input, thereby reducing kick-back noise.

The operation of the double-tail SA is similar to that of a conventional SA. During the pre-charge phase when $\mathrm{CLK_{DFF}}$ is low, both tail transistors, M_5 and M_6, are turned off. M_3 and M_4 charge nodes BP and BN to VDD, which in turn causes the output nodes, Outm and Outp, to be discharged to GND through M_9 and M_{10}. This is different from the conventional SA, the outputs of which are pre-charged to VDD. Since both tail transistors M_5 and M_6 are turned off during this phase, no static current is consumed.

At the rising edge of $\mathrm{CLK_{DFF}}$, both tail transistors are turned on, and the SA starts evaluating. Suppose the input signal D is high. Node BN is thus discharged to GND, which turns off M_{10}. Outp is then charged up through M_6 and M_8 until the crosse-coupled inverters start regenerate. In the end, Outp is held at VDD and node Outm GND. After the inverter cross-couple has made the decision, further changes in the input signal will not affect the outputs. Take the previous example and suppose D goes low when $\mathrm{CLK_{DFF}}$ is still high. The only change that takes place is the discharge of BP through M_2 and M_5, leaving both outputs unaffected. This is yet another difference between the double-tail and the conventional SA, since a double-tail SA does not require a shorting NMOS transistor.

One thing worth mentioning is that, since a double-tail SA pre-charges its outputs to GND rather than VDD, its connection to the succeeding SR latch is different from that of a conventional SA. Table 5.1 is a truth table of a SR latch. Table 5.2 contracts the truth table of a conventional SA with that of a double-tail SA. By matching Table 5.2 with Table 5.1, we could see that, for the double-tail SA, Outp serves as a set signal S and Outm the reset signal R. For the conventional SA, on the other hand, Outp serves as the inverse reset signal $\overline{\mathrm{R}}$ and Outm the reverse set $\overline{\mathrm{S}}$.

Table 5.1: SR latch truth table.

	S	R	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
Pre-charge	0	0	1	1	Q	$\overline{Q}$
Rest	0	1	1	0	0	1
Set	1	0	0	1	1	0
Invalid signal	1	1	0	0	1	1

Table 5.2: Conventional and double-tail SA truth table.

	Input Signal		Conventional SA		Double-tail SA		DFF Output	
	D	$\overline{D}$	Outp	Outm	Outp	Outm	Q	$\overline{Q}$
Pre-charge	-	-	1	1	0	0	Q	$\overline{Q}$
Evaluation	1	0	1	0	1	0	1	0
	0	1	0	1	0	1	0	1

Symmetrical SR Latch

A cross-coupled NAND gate SR latch is always employed as the second stage of a DFF, as shown in Figure 5-7. The truth table of this type of SR latch is listed in Table 5.1 and its operation is described as follows. When both inputs are high, which happens when the preceding SA is pre-charged, the NAND gates hold their original value and both outputs remain. When the input signal $\overline{S}$ goes low, the output node Q goes high after one gate delay, which in turn brings down node $\overline{Q}$ after another gate delay. Due to the symmetry of the circuit, when $\overline{R}$ goes low, conversely, the output node $\overline{Q}$ goes high first, which then forces Q to be low. The state that both $\overline{S}$ and $\overline{R}$ are low is not permitted, and is eliminated by the preceding SA stage. Therefore, whenever the latch outputs need to change, there is always a timing difference between Q and $\overline{Q}$, and the falling edge always occur one gate-delay after the rising edge [6].

Unlike the cross-coupled NAND gate SR latch, the symmetrical SR latch provides both its complementary outputs with equal delay. This helps the feedback paths of the modulator to achieve precise timing, which is important for the stability and accuracy of the modulator.

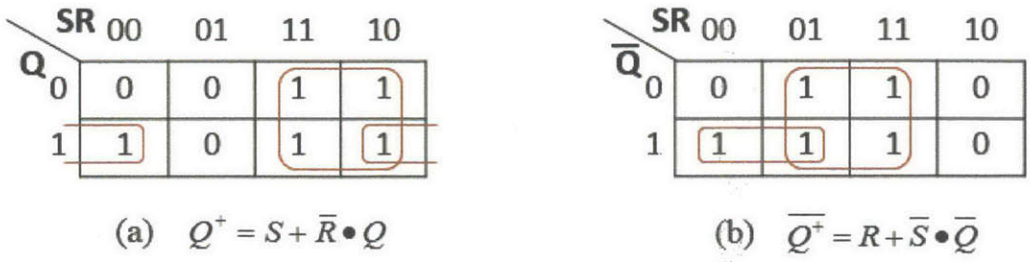


Figure 5-9: Karnaugh maps for both outputs of a SR latch.

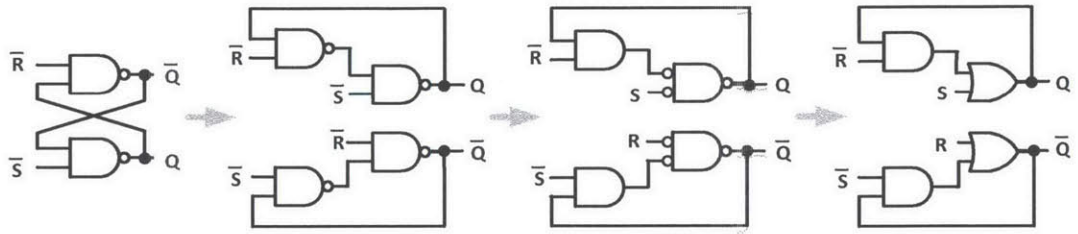


Figure 5-10: Topology evolution of a cross-coupled NAND gate SR latch [6].

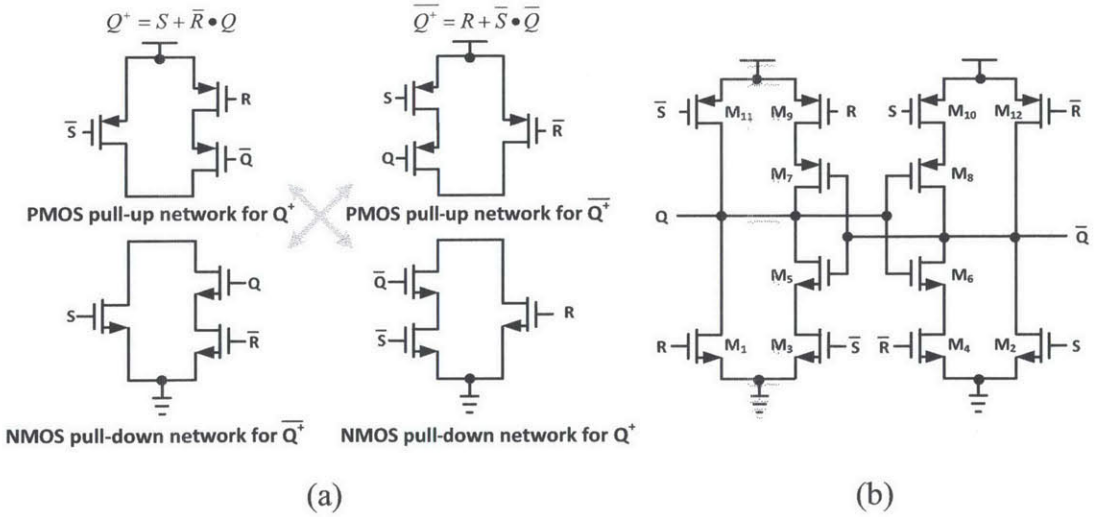


Figure 5-11: (a)Pull-up/down networks that correspond to characteristic equations. (b) Schematic of the symmetric SR latch [6].

The symmetrical SR latch can be constructed as follows. The characteristic equations for the SR latch are written as follows:

$$\begin{aligned} Q^+ &= S + \overline{R} \cdot Q \\ \overline{Q^+} &= R + \overline{S} \cdot \overline{Q} \end{aligned} \tag{5.1}$$

where Q^+ represents a future latch state. The above characteristic equations can be obtained by either looking at the Karnaugh maps for Q^+ and $\overline{Q^+}$, as shown in Figure 5-9, or examining the evolution of a cross-coupled NAND gate latch topology, as shown in Figure 5-10. For each characteristic equation, we can construct both an NMOS pull-down and a PMOS pull-up network, as shown in Figure 5-11(a). Matching a pull-up network with a corresponding pull-down network, we get the schematic as shown in Figure 5-11(b). This is the schematic for the symmetrical SR latch.

The operation of the symmetrical SR latch is explained as follows. When both S and R are low, M_1, M_2, M_{11}, and M_{12} are turned off while M_3, M_4, M_9, and M_{10} are turned on. The circuit is reduced to a cross-coupled inverter pair, and the outputs Q and $\overline{\text{Q}}$ maintain their values. This corresponds to the hold state of the SR latch. When S is high and R is low, M_2, M_4, M_{11}, and M_9 are turned on while M_1, M_3, M_{10}, and M_{12} are turned off. Suppose originally Q is low and $\overline{\text{Q}}$ is high, M_{11} charges up Q while M_2 discharges $\overline{\text{Q}}$ in order to set the output. When S is low and R is high, on the other hand, M_1 discharges Q while M_{12} charges $\overline{\text{Q}}$ so that the output is reset. The state that both $\overline{\text{S}}$ and $\overline{\text{R}}$ are low is not permitted, and is precluded by the preceding SA stage.

From the above analysis, during set and reset states, the charging and discharging of the outputs happen simultaneously, enabling equal delays for both outputs. Besides, only one transistor in each branch is active when the outputs change state, thus allowing smaller sizing for keeper transistors $M_3 \sim M_{10}$ [6].

5.2 DAC Driver

The DAC driver is composed of 14 identical slices, each of which takes a digital bit from the quantizer and drives 8 DAC cells that come from $DAC_1 \sim DAC_8$ respectively. The DAC driver slice is a cascade of a DFF and a switch driver, which is shown earlier in Figure 5-2. The DFF has the same topology as introduced in Section 5.1.3. This DFF topology has the advantage that both outputs enjoy equal delay, thus ensuring simultaneous timing along the true and complementary signal paths of the DAC driver. The switch driver is an optimized inverter chain that drives the succeeding DAC cells. The clock signal CLK_{DAC} is delayed with respect to CLK_{Latch} by such a period of time that the output currents from the DAC are delayed by exactly one clock cycle. The detailed timing diagram of the feedback paths is illustrated and explained later in Section 5.4.

5.3 DAC

As shown in Figure 5-1, the modulator employs 8 15-level DACs to implement the feedback paths from the quantizer output to the analog loop filter. Each DAC consists of 14 identical fully-differential current-steering DAC cells that takes the digital code from the DAC driver and convert it into current signals.

Of all these DACs, DAC_1 and DAC_2 have the most stringent requirements in terms of noise and linearity. This is because they are connected directly to the first resonator, and their noise and non-linearity add directly to the modulator input. Now that the first resonator operates under a power supply of 2.5 V, DAC_1 and DAC_2 need to operate under the same supply voltage as well. This is beneficial to the design, as explained later in Section 5.3.1. The other DACs operate under 1.2 V, and have much more relaxed requirements in terms of noise and linearity.

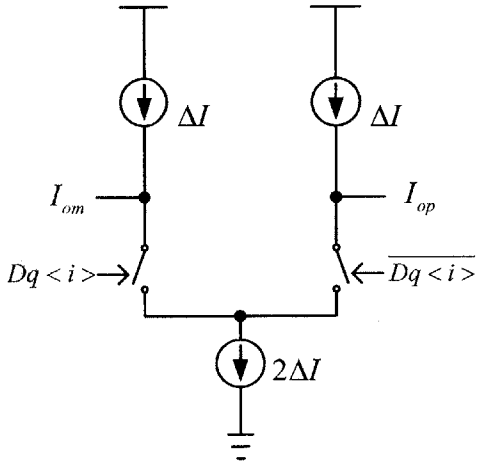


Figure 5-12: Differential current-steering DAC cell.

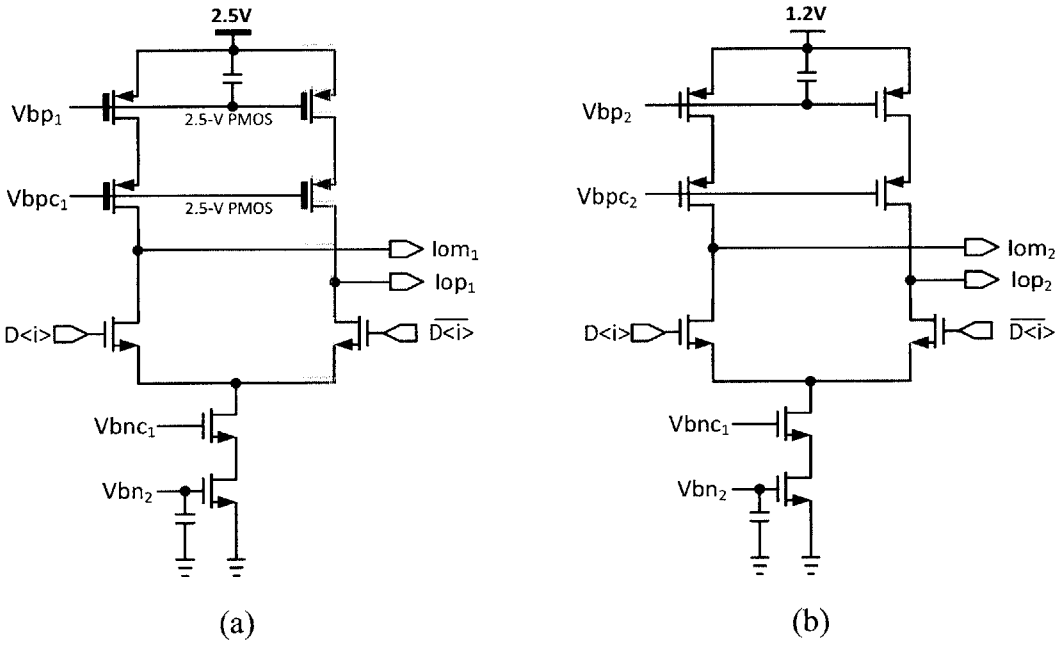


Figure 5-13: Schematics of the differential current-steering DAC cells (a) DAC_{1-2} and (b) DAC_{3-8}.

5.3.1 Current-Steering DAC Cell

A differential current-steering DAC consists of a differential switch, a tail current source, and current mirror loads, as shown in Figure 5-12. The schematic of both DAC_{1-2} and DAC_{3-8} are shown in Figure 5-13. Both the tail current source and current mirror loads employ cascode structures to achieve better current matching. Large capacitors are placed at the gate of the current sources for decoupling. For DAC_1 and DAC_2, noise from the current mirrors affects the modulator SNR. The fact that DAC_1 and DAC_2 are operating under 2.5 V actually helps reduce the noise, because the high supply voltage makes possible very large overdrive voltages on the current mirror transistors. 2.5-V PMOS devices are employed as current mirror loads and cascodes in order to withstand the high power supply voltage.

5.4 Timing of the Feedback Paths

The timing diagram of the feedback paths is shown in Figure 5-14. Clock signals CLK_{Latch} and CLK_{DFF} are provided to the quantizer while CLK_{DAC} goes to the DAC driver. The most important issue in the timing of the feedback path is to make sure that the current signals, I_{op} and I_{om}, are delayed by exactly one clock cycle. Therefore the output signals from the DAC driver, D_{out} and $\overline{D_{out}}$, should settle well within one clock cycle. The exact timing of CLK_{DAC} is thus obtained from simulation to fulfill the aforementioned timing requirements. The timing of the quantizer is more straight forward. At the rising edge of CLK_{Latch}, signals LQ and $\overline{LQ}$ enters evaluation period and produce valid results after some time. The delay between the rising edge of CLK_{Latch} and that of CLK_{DFF} should be longer than the setup and hold time of signals LQ and $\overline{LQ}$ in order for the DFF to produce correct results. Similarly, the delay between CLK_{DFF} and CLK_{DAC} should be longer than the setup and hold time of the DFF.

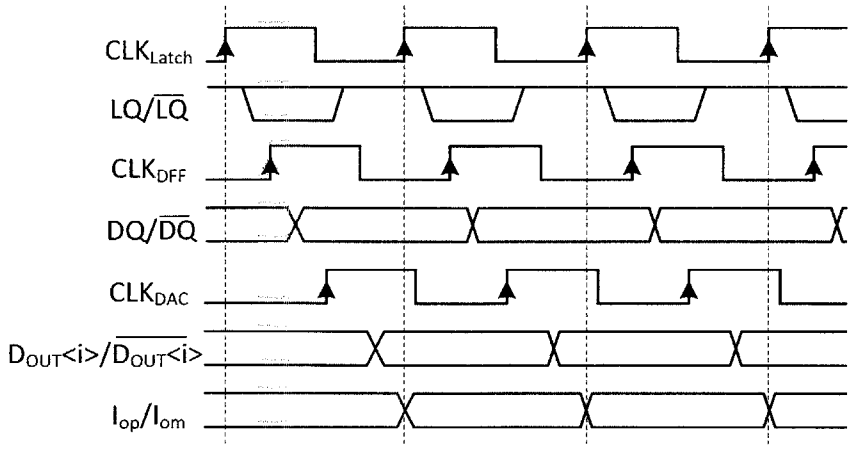


Figure 5-14: Timing diagram of the feedback paths.

5.5 Summary

In this chapter, the transistor-level design for the modulator feedback paths is discussed. Key building blocks, such as the quantizer, the DAC drive, and the DACs, are explained in detail. For the quantizer, the design of a three-stage comparator, which is composed of a pre-amplifier, a latch, and a DFF, is provided. The DFF, especially, is realized with a double-tail SA and a symmetrical SR latch and has the benefits of reduced kick-back noise, amenability to low supply voltage, and equal delay for both true and complementary outputs. This DFF topology is also employed in the DAC driver. For the DAC, a fully-differential current-steering topology is introduced. The timing of the feedback paths is also explained.

Now that we have finished explaining the implementation of the whole CT bandpass $\Delta\Sigma$ modulator, the next chapter presents both system-level and transistor-level simulation results.

Chapter 6

Simulation Results

This chapter presents the simulation results of the proposed CT bandpass $\Delta\Sigma$ modulator. The system-level behavior of an ideal modulator is demonstrated first. The performance of the multistage feed-forward op amps are provided next. The transistor-level simulation results of the whole modulator system are then illustrated and summarized.

6.1 Ideal Performances

This section presents the system-level simulation results of the proposed CT bandpass $\Delta\Sigma$ modulator under ideal operation. The complete block diagram of the proposed modulator is shown earlier in Figure 3-1. We have built and simulated the modulator in Simulink to verify its operation.

Figure 6-1 shows the output spectrum of the modulator with a -3.1 dBFS 253 MHz sine wave input, as well as the STF and the NTF of the modulator. In absence of any non-ideality, the modulator achieves a SQNR of 92 dB, fulfilling our SQNR target of 90 dB.

Inputs of various amplitudes have been applied to the modulator to obtain the SNR versus input amplitude plot, as shown in Figure 6-2. Under ideal operation, the modulator achieves a dynamic range of 92.6 dB and a peak SQNR of 93.9 dB.

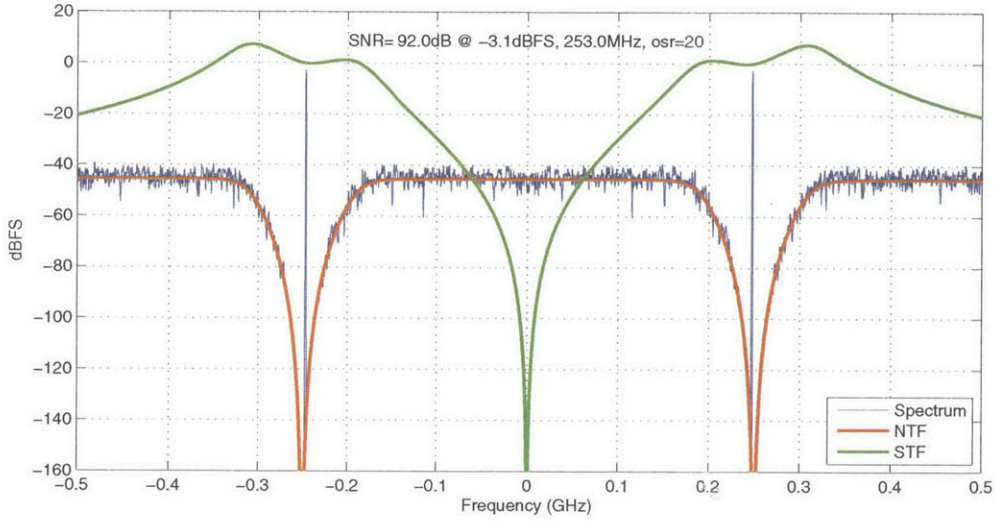


Figure 6-1: NTF, STF, and output spectrum of the ideal modulator with a -3.1 dBFS 253 MHz sine wave input signal.

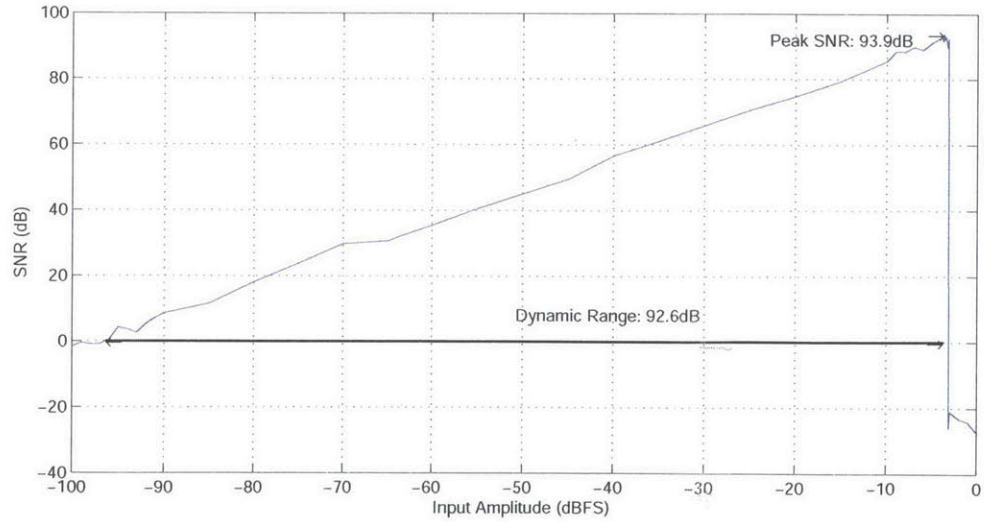


Figure 6-2: SNR versus input level for the ideal modulator.

6.2 Op Amp Blocks

In the proposed $\Delta\Sigma$ modulator, two different op amp designs are employed. One is a dual-supply 5^{th}-order feed-forward op amp. The target in-band loop gain of this op amp is 50 dB. The other is a single-supply 4^{th}-order feed-forward op amp. The target in-band loop gain of this op amp is 40 dB. Besides, the loops should have enough phase margin in order to ensure stability.

Figure 6-3 and 6-4 show the simulated loop gain of the 5^{th}-order (A_1) and 4^{th}-order (A_3) feed-forward op amp respectively. Table 6.1 summarizes the in-band loop gain and phase margin of all 8 op amps. From the results, the 4^{th}-order feed-forward op amp ($A_3 \sim A_8$) satisfy the design requirements perfectly. The 5^{th}-order op amp (A_1 and A_2), however, achieves a larger gain than required at 250 MHz, but the phase margin is a bit low. The power consumption of the two op amps are 20.2 mW and 78.7 mW respectively

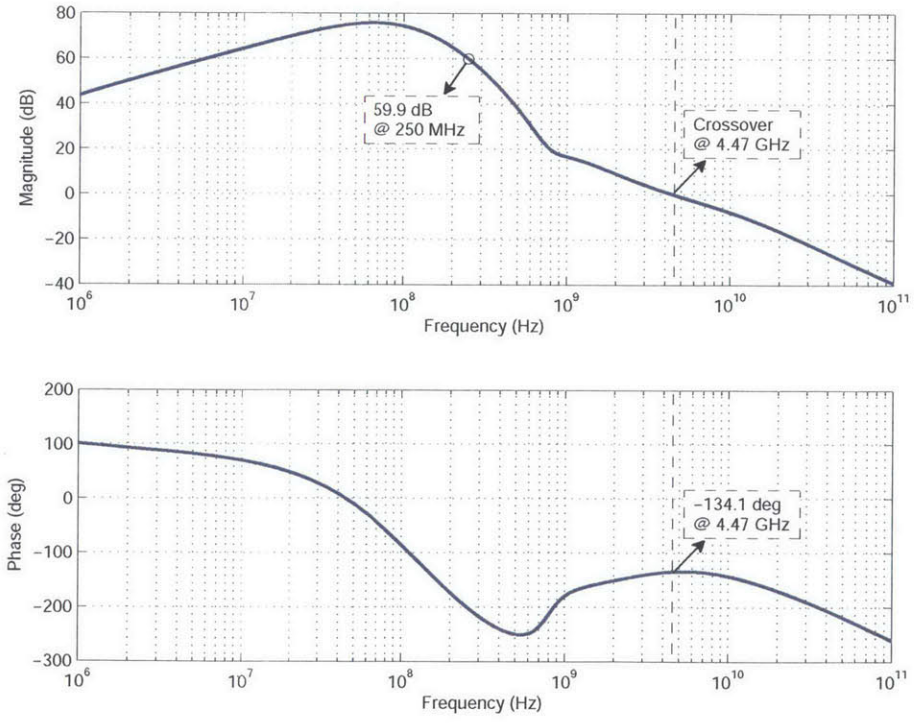


Figure 6-3: Simulated loop gain of A_1 in the 1^{st} resonator stage.

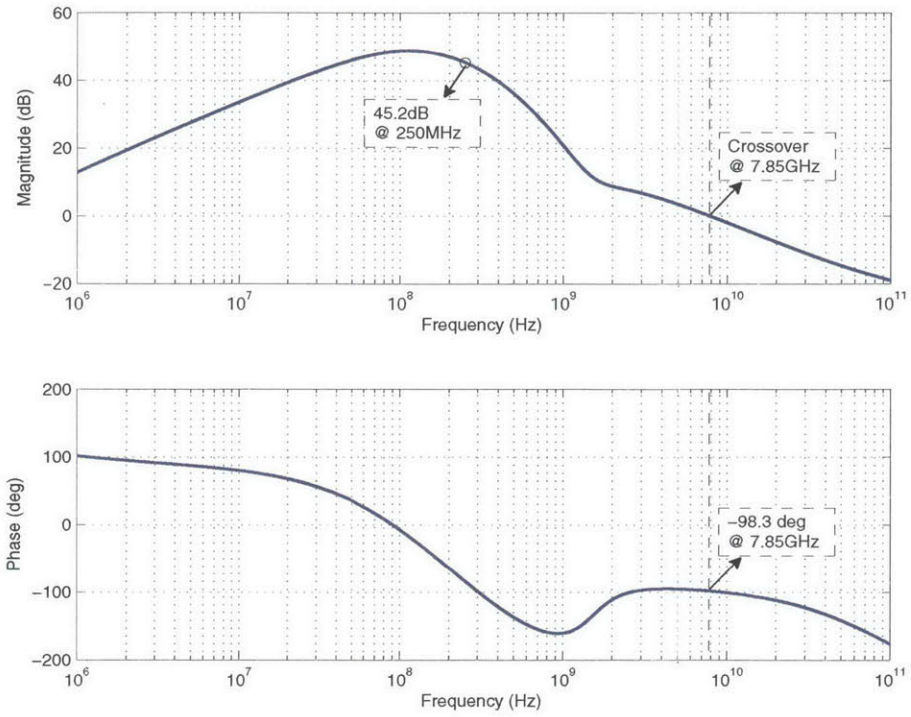


Figure 6-4: Simulated loop gain of A_3 in the 2^{nd} resonator stage.

Table 6.1: Op amp loop gain summary.

	A_1	A_2	A_3	A_4
Loop Gain @ 250 MHz	59.9 dB	62.8 dB	45.2 dB	48.2 dB
Phase Margin	45.9°	42.4°	81.7°	79.5°
	A_5	A_6	A_7	A_8
Loop Gain @ 250 MHz	44.3 dB	48.6 dB	42.6 dB	48.8 dB
Phase Margin	83.3°	79.4°	84°	79.6°

6.3 Overall Modulator Performance

This section provides the transistor-level simulation results of the proposed 8^{th}-order CT bandpass $\Delta\Sigma$ modulator. The modulator is designed and simulated in the TSMC 65 nm CMOS process. The sampling frequency is 1 GHz and the center frequency is at 250 MHz.

Figure 6-5 $\sim$ 6-9 show the output spectrums of the modulator with -3 dBFS input

signals of various frequencies. The signal bandwidth is 250MHz, and a SNR of above 75.5 dB is achieved across the signal band.

Figure 6-10 shows the output spectrum of the modulator with a -10 dBFS two-tone input signal of 237 MHz and 255 MHz. From the spectrum, the IM3 of the modulator is -74.2 dB.

The maximum stable input amplitude is simulated to be -1.9 dBFS. The modulator consumes a static power of 319 mW. The power consumption from each building block is summarized in Table 6.2. The achieved performances are summarized in Table 6.3.

Table 6.2: Static power consumption.

Loop Filter	Dual-supply Op Amp	78.7 mW×2	298.1 mW
	Single-supply Op Amp	20.2 mW×6	
	Biasing Network	19.3 mW	
DAC	DAC Cells	14.7 mW	17.2 mW
	DAC Driver	2.5 mW	
Quantizer	Reference	0.36 mW	3.3 mW
	Comparators	2.9 mW	
Total			319 mW

Table 6.3: Simulated modulator performance.

Technology	TSMC 65 nm CMOS
Architecture	8^{th}-order Continuous-Time Feedback-type Bandpass $\Delta\Sigma$
Sampling Frequency	1 GHz
Signal Bandwidth	25 MHz
Center Frequency	250 MHz
Maximum Stable Input Voltage	-1.9 dBFS/1.45 $V_{p\text{-}p}$ (differential)
SNR	75.5 dB
Power Supply Voltage	2.5 V/1.2 V
Power Dissipation	319 mW

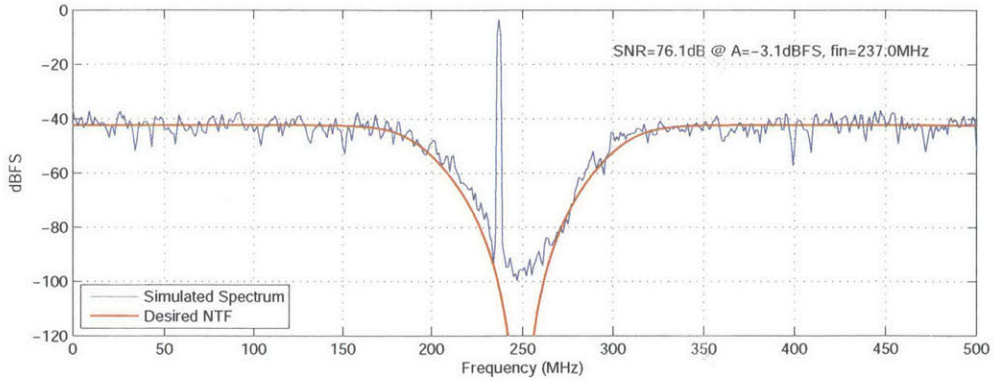


Figure 6-5: Simulated modulator output spectrum with a -3 dBFS 237 MHz input signal (averaged FFT with $N_{FFT} = 1000$, achieved SNR = 76.1 dB).

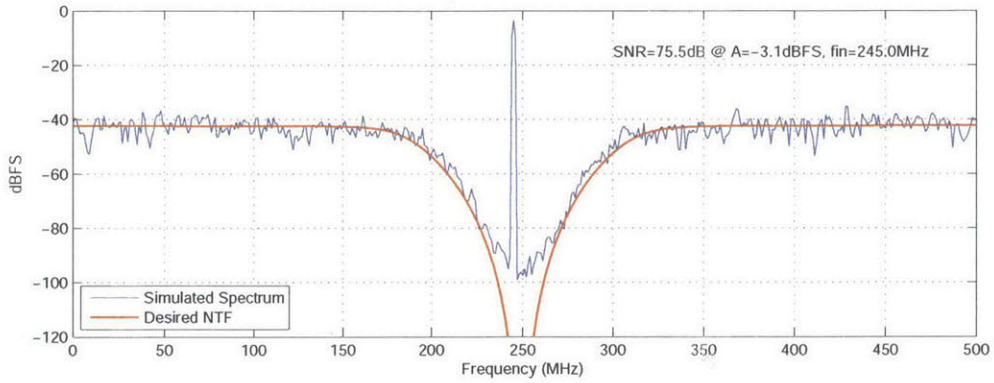


Figure 6-6: Simulated modulator output spectrum with a -3 dBFS 245 MHz input signal (averaged FFT with $N_{FFT} = 1000$, achieved SNR = 75.5dB).

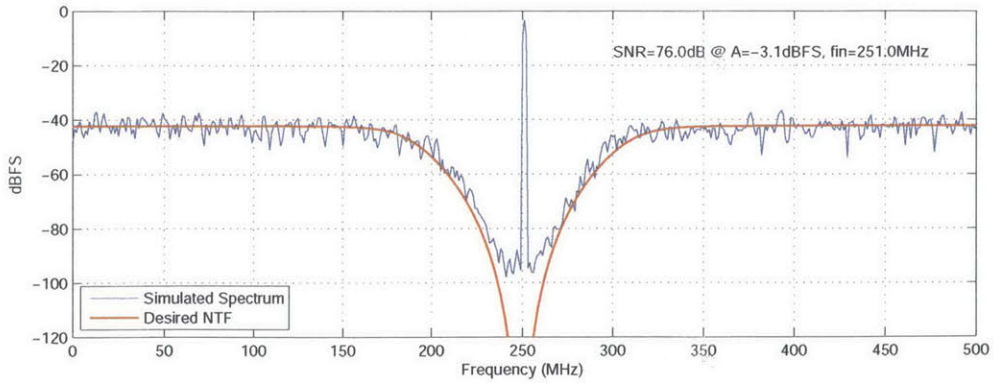


Figure 6-7: Simulated modulator output spectrum with a -3 dBFS 251 MHz input signal (averaged FFT with $N_{FFT} = 1000$, achieved SNR = 76dB).

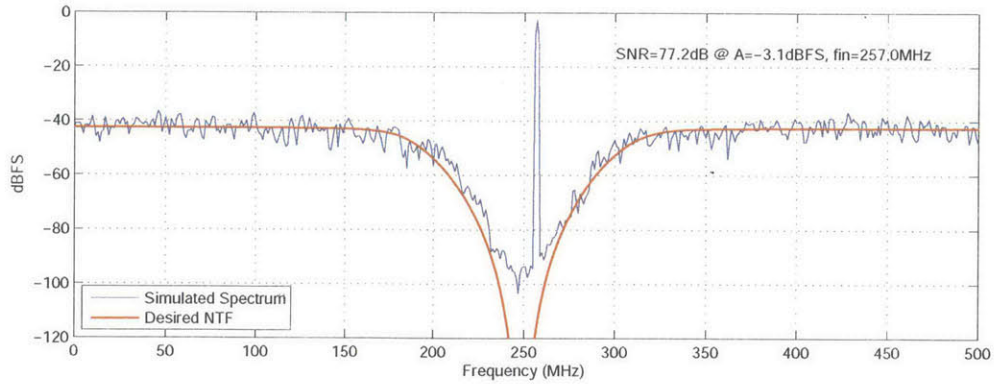


Figure 6-8: Simulated modulator output spectrum with a -3 dBFS 257 MHz input signal (averaged FFT with $N_{FFT} = 1000$, achieved SNR = 77.2dB).

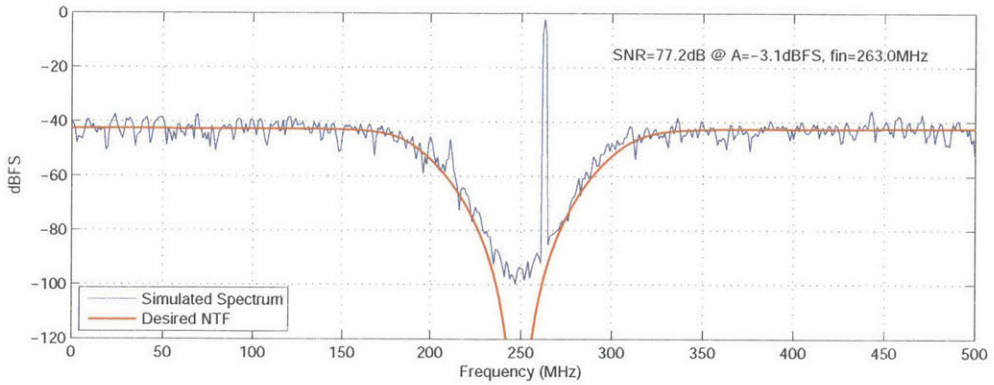


Figure 6-9: Simulated modulator output spectrum with a -3 dBFS 263 MHz input signal (averaged FFT with $N_{FFT} = 1000$, achieved SNR = 77.2dB).

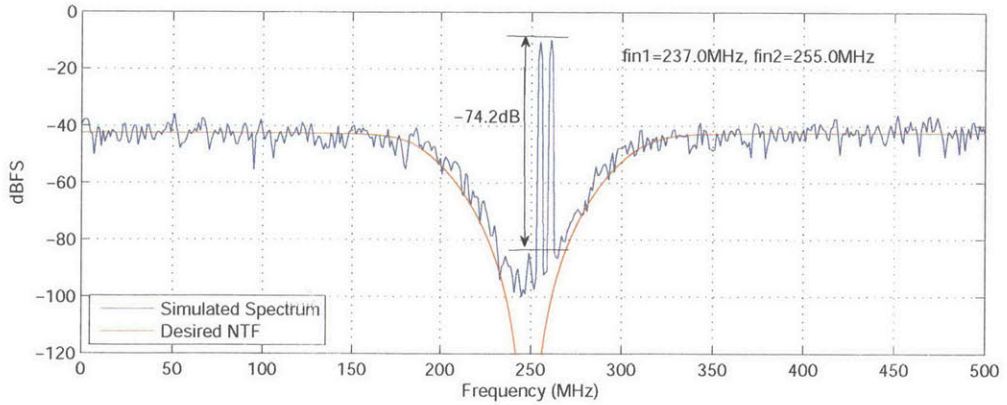


Figure 6-10: Simulated modulator output spectrum with a -10 dBFS two-tone signal at 237 MHz and 263 MHz (averaged FFT with $N_{FFT} = 1000$).

Chapter 7

Conclusions and Future Work

This chapter summarizes the thesis and suggests possible areas of research that can further improve the performance of a CT bandpass $\Delta\Sigma$ modulator.

7.1 Conclusions

A wide bandwidth, high resolution CT bandpass $\Delta\Sigma$ modulator has been proposed in this thesis, and has been designed and simulated in a TSMC 65 nm CMOS process. The achieved signal bandwidth is 25 MHz, with the center frequency of 250 MHz. The achieved SNR is 75.5 dB. The modulator samples at 1 GS/s and consumes a total power consumption of 319 mW.

On the system level, the feedback topology secures stability for the 8^{th}-order system, achieving a maximum stable input voltage of -1.9 dBFS. The SNR-limiting factors for this design are thermal noise and distortion. The additional feed-forward coupling path proves to be effective in suppressing distortion from the loop filter. The employment of a dual 2.5-V/1.2-V supply in the 1^{st} resonator stage successfully reduces the effects of thermal noise. Hence a SNR of 75.5 dB is achieved.

On the circuit level, multi-stage feed-forward op amps achieve high gain and high unity-gain bandwidth simultaneously with a decent phase margin. This op amp topology proves to be particularly suitable for CT bandpass $\Delta\Sigma$ modulators.

7.2 Future Work

In this section, we will discuss both the ways to improve the design proposed by this thesis, and interesting research areas that concern CT bandpass $\Delta\Sigma$ modulators in general.

For this design, our efforts have been mainly focused on the system-level considerations and the implementation of the loop filter. More work is needed for the feedback DACs and the quantizer:

- Mismatches among the DAC elements introduce harmonic distortion to the output and degrades SNDR. Dynamic element matching (DEM) or mismatch shaping needs to be added to the feedback paths in order to improve DAC linearity.
- The quantizer should be further optimized against offsets and process variations. But since the errors from the quantizer are filtered by the NTF, the accuracy of the quantizer is not a major concern.

Besides, the loop filter still needs improving. The op amps in this work are overdesigned, consuming more power than necessary. We can save power by scaling the op amps of intermediate stages, where the noise requirements are not as strict. We should also optimize the op amps according to the specific loading of each stage, so as to achieve greater power efficiency.

For CT bandpass $\Delta\Sigma$ modulators, distortion from the loop filter and thermal noise from interstage resistors limit the achievable SNR. The solution proposed in this thesis is to use a dual-supply loop filter that trades power for performance. Better solutions, however, may exist and are worth exploring:

Modulator architecture innovation For lowpass $\Delta\Sigma$ modulators, innovative modulator topologies, such as mixed feedback and feedforward [22], noise-coupled time-interleaving [23], and cascaded multi-stage noise-shaping (MASH) [24], have been proposed to improve modulator performance. This motivates us to seek system-level solutions for the bandpass $\Delta\Sigma$ modulators as well.

Compensation for op amp non-ideality For CT lowpass $\Delta\Sigma$ modulators, [25] and [26] introduce design methodologies that account for op amp non-ideality when determining modulator coefficients. Therefore, op amps of lower gain-bandwidth requirements can be used, leading to power efficient design. For CT bandpass $\Delta\Sigma$ modulators, it is also worthwhile to study more theoretically the effects of op amp non-ideality on resonator behaviors, and explore the corresponding compensation methods.

Power-efficient resonator design The resonator is the most power hungry building block of the whole modulator. [13] and [14] introduce a single-amp resonator that provides a good solution for power efficient design. It is interesting to further investigate both the potential and the limitations of this resonator topology. This also motivates us to explore other power-efficient resonator topologies.

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