Integration of GaAsP Alloys on SiGe Virtual Substrates for Si-based Dual-junction Solar Cells

by

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High Quality Epitaxial Growth of GaAsP Alloys on SiGe Virtual Substrates for Si-based Solar Cells

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ABSTRACT

Integration of III-V compound semiconductors with silicon is an area that has generated a lot of interest because III-V materials and Si are best suited for different types of devices. Monolithic integration enables the best material to be chosen for each application, enabling new functionalities with the potential of additional miniaturization on a system level. Integration of GaAsP alloys on Si substrates would enable the creation of high efficiency dual-junction solar cells on low cost and light weight Si wafers and would also enable a path for yellow and green light emission devices on a Si platform.

Our work focused on the materials integration problems for multiple pathways to integrate GaAsP alloys on Si substrates. We first addressed the direct integration of GaAsP alloys on Si substrates. Our results showed that despite the low lattice-mismatch conditions at the P-rich end of the GaAsP alloy spectrum, it was difficult to achieve thin films low defect density. We proceeded to focus on the integration of GaAsP alloys on Si via the use of SiGe compositionally graded layers. Through a combination of methods we addressed problems related to antiphase disorder and lattice mismatch between GaAsP and SiGe materials system. We demonstrated the epitaxial growth lattice-matched GaAsP on Si$_{0.88}$Ge$_{0.12}$, Si$_{0.5}$Ge$_{0.5}$, Si$_{0.4}$Ge$_{0.6}$, and Si$_{0.3}$Ge$_{0.7}$ virtual substrates with excellent interface properties. Our studies showed the effects of initiation conditions and intentional strain at the GaAsP/SiGe heterovalent interface. We have established strain-engineering methods at the GaAsP/SiGe heterovalent interface to prevent dislocation loop nucleation and expansion. We were able to attain GaAsP films on Si with a threading dislocation density as low as 1.2x10$^6$/cm$^2$. Our GaAsP/SiGe heterovalent interface research advanced the understanding of such structures.

We developed methods to fabricate optimized GaAsP tunnel junction film, which would be necessary for any current-matched dual junction solar cell design. Prototype dual-junction GaAsP/Si solar cell test devices showed good preliminary performance characteristics and offer great promise for future devices integrated with the newly developed high quality GaAsP/Si virtual substrates.

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Chapter 1: Introduction
1.1. Motivation for Dual-junction Solar Cells on Si

This work focuses on both structural and electrical characterization of III-V compound semiconductors epitaxially integrated on Si substrates, with an ultimate goal of achieving high quality GaAsP/Si dual-junction solar cell performance. The success of large-scale monolithic integration III-V semiconductors and silicon has been limited due to the fundamental incompatibilities between the materials. While many other integration techniques,\textsuperscript{1,2,3,4,5} have been developed in order to bypass the need for direct III-V on Si heteroepitaxy, these have only been moderately successful and haven’t provided a solution for the realization of large area integration of III-V/Si devices. Therefore, monolithic integration of III-V/Si appears to be the best solution available for large area applications.

The importance of high efficiency and low cost solar cells is addressed in this thesis along with the use of low weight and low cost substrates to achieve high efficiency solar cells. The exploration of III-V semiconductor integration on Si substrates has been motivated by the need to realize high efficiency solar cells while using the infrastructure available for Si. Solar cells with different band gaps are grown on top of each other, to conserve area, that can be connected in series epitaxially by using tunnel junction device layers as low resistance contacts between the cells.

Since the individual junctions are connected in series the current gets limited; this reduction is compensated by the increase in the \( V_{\text{OC}} \) value through the addition of the
\( V_{OC} \) of the individual cells, leading to higher power and higher efficiencies. Due to the cells being connected in series, the same amount of current flows through all the individual cells and gets limited by the worst performing cell. To get the maximum efficiency out of the multijunction cell, each individual cell needs to be current-matched. The number of photons being absorbed in each cell can be adjusted by optimizing the thickness of each cell that will result in current matching.

Because of the low density of Si, a high efficiency III-V cell on Si could weigh much lower than that on GaAs, thus increasing the specific power if high efficiencies can be achieved. The high availability, large area and low cost of Si substrates can help to further decrease costs and increase manufacturing capacity. This would allow the transfer of such technologies to large-scale applications.

The current PV cells are expensive as compared to the existing energy technology. The cost can be decreased while maintaining high performance by substituting Si as an alternative substrate in place of Ge or GaAs. The Ge or GaAs substrates account for a significant part of the total PV cost. Si substrate based III-V devices can use the existing manufacturing infrastructure making it economical to scale the production of PV cells without additional capital investment. This provides the motivation to explore metamorphic epitaxy of high quality III-V semiconductors on Si to achieve low-cost and high efficiency solar cells.

While the focus of this work is motivated by the future impact on multi-junction PV
technology, the broad range of materials properties accessible could be applied to many other technologies. The growth of GaAsP and InGaP on Si substrate could be used to create yellow and green LEDs. Access to larger lattice constant on the Si substrate allows the potential for integration of InP based devices onto Si. Further, combining this work with past InAsP grading work encompasses the entire AsP lattice constant and material property spectrum, with the potential of integration with Si technology.  

Integration of III-V compound thin films on silicon substrates have received significant attention for many years because of the potential to integrate III-V compound based semiconductor devices with less expensive and more reliable Si technology. Photovoltaics materials research has recently been motivated by the integration of high-efficiency III-V compound solar cell materials and devices with low-cost Si substrates. InGaP and GaAs solar cells have recently been successfully integrated with Si through the use of Ge virtual substrates with SiGe graded buffers. Another route to achieve this, exists via the growth of GaP directly on Si, followed by lattice and bandgap engineering with III-V graded buffers. The advantage of this approach is the prospect of achieving a 1.7/1.1eV dual-junction solar cell (Figure 1). Geisz et al. have reported that these dual-junction cells possess the highest potential theoretical efficiency of 37% under one-sun AM1.5, using a GaAs_{0.71}P_{0.29}/Si structure, in which the Si can be used as both the lower cell and the substrate.
Multi-junction III–V solar cells fabricated on silicon substrates would reduce the substrate cost and allow monolithic integration with existing Si technology. Lattice mismatched III–V cells on Si substrates have been explored extensively, but the reduction of defect densities resulting from lattice mismatch remains a significant challenge that typically requires complex graded buffer layers. The solar cell structure shown in Figure 1, composed of a lattice matched GaAsP cell grown on a Si cell, could potentially rival the efficiencies of high-efficiency cells on GaAs or Ge. This can result in significant cost savings and improvements in mechanical stability, if sufficiently good minority-carrier transport can be achieved in the III–V alloy. Band gaps of 1.1eV and 1.7eV are nearly optimal for maximum efficiency for two-junction devices.

If the semiconductor material cost can be limited to a small fraction of the system cost, then increased efficiency would improve the entire system without increasing the cost.
significantly. Therefore, higher efficiency solar cells can provide a pathway to lower cost solar energy conversion even if the solar cell itself is more expensive.

Shockley-Queisser limit refers to the maximum theoretical efficiency for a p-n junction solar cell; also know as the detailed balance limit. Radiative transfer between the sun and the solar cell is balanced for calculating the efficiency limit of a semiconductor material with concentrated light under one-sun.\textsuperscript{12} For more practical applications realistic models use band-structure properties of known materials. These calculations were done assuming a single p-n junction, but if multiple materials are used then the efficiency limit increases. The use of higher band gap materials for the top p-n junctions decreases the thermalization of hot carriers in the case of multi-junction solar cells. Whereas, the lower band gap material for the bottom p-n junction reduces the transmission losses of the photons with low energy. While multiple materials can result in the higher efficiency of solar cells, Figure 2 also shows that it is important to have high material quality to realize the benefit of multiple junctions. Therefore, it is important to maintain the high quality of materials when integrating the individual cells. This thesis will address the route of growing the materials with different band gap energies on top of each other and on a single substrate. The different individual cells are then connected in series by tunnel diodes, resulting in a final device with contacts of opposite polarity.
Figure 2: Achieved efficiencies and theoretical efficiency limits (solid lines) estimated by the detailed-balance method for one-sun illumination. Higher material quality leads to higher efficiency.

The two important criteria for achieving high efficiency solar cells are the selection of a set of materials with band gaps that span the solar spectrum to provide a high theoretical efficiency and maintaining high material quality while integrating these materials. The second part is more challenging than the first.

1.2 Background on III-V/Si and Dual Junction Solar Cells on Si

1.2.1. Single junction Si solar cells

Silicon is still the most commonly used material used for fabricating photovoltaic devices and it is mainly due to the robustness of silicon technology that the PV has grown significantly over the last decade. Important factors such as sustainability, cost and environmental impact still dominates the photovoltaic industry activities. There are
several contenders competing with silicon in the solar industry over the past few years. Organic solar cells are already being commercially produced for the consumers. Sustainability, efficiency, low lifetime, durability and stability are still some of the major challenged hindering the progress of organic solar cells. This will make it difficult for the organic solar cells to compete with the silicon technology in the near future.

In the case of inorganic solar cells, Cu(In,Ga)Se₂ solar cells are one of the most promising in terms of both efficiency and stability.¹³ Toxicity issues and expensive materials will make it challenging for these cells to be competitive with that of Si, despite the initial potential shown.¹⁴,¹⁵

Whereas, recent developments in the case of silicon-based solar cells have led to efficiencies almost near the theoretical efficiency limit for a single junction solar cells.¹⁶ Further research is being done to make further improvements in the silicon solar cells through defect control and device optimization. Because of the unique advantages available in the case of silicon, such as abundance, sustainability, no toxicity and long lifetime, the goal of achieving high efficiency solar cells while maintaining low cost needs to involve the use of silicon. This can be achieved with the use of the multi-junction solar cell fabricated on the Si substrate to provide reliability and low-cost infrastructure.
1.2.2. Challenges for dual-junction cells

Multi-junction solar cell design depends on band gap and lattice matching. But there are other variables such as current matching in the subcells of a multi-junction solar cell to maximize the efficiency. That means similar photon absorption rate in all the subcells to produce the same current. Because of the cells being connected in series, the junction producing the least current will limit the current going through the entire stack. Therefore, the cell should be designed such that the same current flows through all the subcells. The current produced by a p-n junction directly depends on the absorptivity of the material and the number of photons having energy more than the band gap of the material. If there are plenty of photons with energy exceeding that of the material’s band gap then even a thin sample can generate the desired current. The same is true for the case where the material has high absorptivity.

Crystalline defects, generated due to the mismatch in the crystal, act as recombination centers for minority carriers. These centers act as a sink for the minority carriers and lower the performance of the photovoltaic device, leading to lower $V_{OC}$, $J_{SC}$ and fill factor.

When the semiconductor absorbs the light, minority carriers are generated governing the performance of the solar cell. The generated carriers diffuse to the built-in field and get used in an outside circuit. The photocarriers that get lost at the defect sites do not contribute to the generation of electricity. These carriers need to diffuse to the built-in
electric field before they recombine at the defect sites to contribute to the generated current. The device needs to be designed in such a way that assists the separation of the carriers. The two key material parameters for solar cell operation are minority carrier lifetime and minority carrier diffusion length. The minority carrier diffusion length should be longer than the thickness of the material needed to absorb the light. Direct band gap materials absorb better than the indirect band gap materials, so thin layers are enough to absorb photons. Defect-free materials have high carrier mobility due to limited scattering. Long minority carrier lifetimes are important in achieving high efficiency solar cells.

It is the non-radiative recombination of the minority carriers, caused by impurities and defects that kill the efficiency of the solar cells. Figure 2 shows ideal materials with no non-radiative recombination. As seen in Figure 2 the material quality is more critical to the efficiency of the solar cell than the number of junctions. Shockley-Read-Hall recombination refers to the non-radiative recombination in the solar cells. They demonstrated that the deep traps act as recombination centers. Therefore, deep traps arising from defects need to be eliminated from solar cells. The heterovalent interface, in the case of III-V and IV semiconductor integration, acts as the source for defects such as threading dislocations (TD) and anti-phase domains (APD). These defects can increase recombination rates, generates deep traps and introduce conductive shunt paths, killing the efficiency of the solar cell.
The material mismatches between GaAsP and Si present many growth complications leading to reduction in material quality. In particular for GaAsP/Si, the incorporation of TD has provided a large barrier for achieving high quality GaAsP/Si devices, especially for minority carrier devices such as solar cells, even when threading dislocation density (TDD) reduction techniques are employed. Addressing other issues such as thermal mismatch can optimize these devices. But it is the impact of TDD on the material quality and the diffusion length that is limiting the performance of the GaAsP/Si solar cells.

In the case of solar cells that are minority carrier devices, the electrons and holes generated from the photons need to diffuse across the p-n junction. Therefore, to maximize the carrier collection, the longer minority carrier diffusion length, \( L_p \), is desired, resulting in higher efficiency. Threading dislocations act as recombination center for these carriers and higher TDD leads to lower diffusion length. This affects the solar cell efficiency and parameters such as \( J_{SC} \), \( V_{OC} \) and FF, all of which contain a diffusion length dependence through minority carrier lifetime.
Yamaguchi developed a theoretical model to understand the impact of TDD on minority carrier properties.\textsuperscript{18,19} Figure 3 plots minority carrier lifetime as a function of TDD. As shown in Figure 3, minority carrier lifetime is strongly dependent on the TDD. Therefore, solar cell parameters such as FF, J\textsubscript{SC}, V\textsubscript{OC} and \(\eta\) also have a TDD dependence because of their relation with the minority carrier diffusion length.\textsuperscript{20}
Figure 4: Theoretical dependence of solar cell parameters (J_{sc}, V_{oc} and efficiency) on threading dislocation density.$^{20}$

Figure 4 shows the theoretical dependence found for J_{sc}, V_{oc}, and $\eta$ on TDD for a single junction cell structure. The strong dependence on TDD, especially for TDD > 1x10^6 cm^-2, indicates that if the TDD can be reduced to ~1x10^6 cm^-2, then it’ll be possible to high efficiencies from GaAsP/Si solar cells. This is because for TDD below ~1x10^6 cm^-2, the distance between threading dislocations becomes larger than the minority carrier diffusion length. Therefore, the diffusion length is no longer being impacted by the recombination of carriers at the dislocation core (Figure 5). Therefore, TDD can be used to characterize the GaAsP films grown on Si and can be correlated to the device performance.
While research for quite a while has been focusing on reducing the TDD incorporated during GaAsP-on-Si epitaxy, TDD below a level where minority carrier devices can be fabricated, hasn’t been achieved. It has been very challenging to control the TDD and reproduce high quality material. Other than TDD in this material system, the thermal mismatch also results in epilayer cracking and wafer bowing which are both detrimental to large area device processing and device performance. 21,22

1.3 Potential Approaches for GaAsP/Si Dual-Junction Solar Cells
To achieve the maximum potential theoretical dual-junction efficiency of 37% under one-sun AM1.5G, the two sub-cells need to have the band gaps of 1.1eV and 1.7eV. While Si conveniently provides the material with 1.1eV band gap for one of the sub-cell, there are multiple semiconductors that satisfy the criteria of having a band gap of 1.7eV, which would be the second sub-cell in the dual-junction solar cell. For this research, we chose GaAsP with a band gap of 1.7eV because of its lattice parameter being closest to that of Si. However, this still result in a 2.7% lattice mismatch that requires the use of compositionally graded buffers to move the lattice parameter from Si to that of GaAsP. We have explored two unique approaches to integrate GaAsP on Si substrate. There is a large lattice mismatch between the GaAs$_{0.71}$P$_{0.29}$ cell (5.59 Å) and the Si cell (5.43 Å), which needs to be accommodated using compositionally graded buffers (Figure 6). The material that will be used for accommodating the lattice mismatch should be transparent to the light that needs to reach the bottom Si cell, otherwise the graded buffer would absorb and lower the solar cell efficiency.
Figure 6: Lattice constant vs energy gap diagram, highlighting the optimal energy gaps of 1.1 eV and 1.7 eV for the maximum theoretical efficiency of a dual-junction solar cell.

Figure 7: Schematic of the two approaches for realizing the solar cell structure.

Two approaches can be envisioned to realize the solar cell structure (Figure 7). The first approach involves the compositional grading using the III-V material only. GaP can be
directly initiated on Si and then compressively graded using GaAs$_y$P$_{1-y}$ till the composition of the top cell. The graded buffer in this case would have band gap above 1.7 eV making it suitable for the fabrication of the solar cell, but high quality GaP integration on Si has been a challenge as explained earlier. Also there will be a thermal expansion mismatch between the GaAs$_y$P$_{1-y}$ graded buffer and the Si substrate, due to the thick III-V graded buffer.

One of the ways to integrate a GaAsP layer on top of a Si substrate is through direct deposition of GaP on Si followed by compressive grading of GaAsP. Among the many III-V compound semiconductors, the lattice constant of GaP is close to that of Si (the lattice mismatch is about 0.37%) at room temperature. Therefore, the effect of lattice mismatch on the growth mode is expected to be minimum. A defect free pseudomorphical nucleation of GaP on Si would allow for a monolithic integration of III-V-based optoelectronics on Si substrates.

One of the advantages of using this approach for the dual-junction solar cells is that the GaP film and the graded buffer of GaAsP will have the band gaps over 1.7eV. This will make the material between the GaAsP cell and the Si cell transparent to the solar spectrum below 1.7eV. So if the top GaAsP cell efficiently absorbs all the photons above 1.7eV, the graded buffer will be completely transparent to the light that should reach the bottom Si cell. This will improve the performance of the bottom cell, increasing the efficiency of the dual-junction cell. Mori has reported TDD values for compressively-
graded \( \text{GaAs}_y\text{P}_{1-y} \) buffers that are superior to the TDD of \( \text{Si}_{1-x}\text{Ge}_x \) graded buffers with corresponding lattice parameter.

However, the GaP/Si interface has proven to be extremely challenging to control. Many of the problems encountered over the years in this pursuit, however, stem from the materials-related issues of the GaP/Si heteroepitaxial system, such as lattice mismatch, thermal expansion mismatch and the polar/non-polar (heterovalent) interface. Despite the interfacial chemistry similarities between GaP/Si and GaAs/Ge system, there are still significant differences between the two systems such as larger lattice mismatch for GaP/Si than GaAs/Ge, higher Si-P reactivity than Ge-As and coefficient of thermal expansion mismatch. These have prevented progress in achieving high quality thin films of GaP on Si.

Since in this structure all the grading will be done in III-V material, it will have a III-V material graded buffer of significant thickness making the thermal expansion mismatch between the III-V and Si more prominent.

Another route to integrate GaAsP on Si substrate that has been explored in this research has been via the use of SiGe graded buffer. SiGe grading can be used to extend the lattice parameter from Si to any composition of SiGe providing a SiGe virtual substrate. Lattice matched GaAsP can be deposited directly on these SiGe virtual substrates to get the 1.7eV band gap for the top sub-cell. Group IV material can also be used for accommodating the lattice mismatch between the two cells in the second approach. Si_{1-}}
$\text{Si}_{1-x}\text{Ge}_x$ graded buffers can be grown on the Si substrate to a composition where it is lattice matched to the GaAs$_y$P$_{1-y}$ cell, followed by the initiation of the III-V material on group IV. $\text{Si}_{1-x}\text{Ge}_x$ graded buffer technology is established and has been proven to provide low dislocation densities, but the challenges with this approach would be the integration of GaAs$_y$P$_{1-y}$ on Si$_{1-x}\text{Ge}_x$ and the need to accommodate some light absorption in the graded buffer.

SiGe is the most advanced relaxed graded buffer technology. It has been optimized to result in very low threading dislocation density, less than $10^6$/cm$^2$ even when graded all the way from Si to Ge. This will be very important in keeping the TDD low in the GaAsP active region of the graded buffer. However, the use of SiGe graded buffer will result in some absorption of the photons with energy below 1.7eV because of the indirect band gap of SiGe alloy. The GaAsP/SiGe heterovalent interface has its own epitaxial challenges, as this interface hasn’t been studied in great detail earlier because of the lack of virtual substrates available for lattice-matching of GaAsP films. It is expected that the GaAsP/SiGe heterovalent interface will exhibit properties between GaP/Si and GaAs/Ge, depending on the composition of interest.
Chapter 2: Materials Growth and Characterization
The research in this thesis is intended to overcome some of the challenges of III-V semiconductor material integration on Si substrates. This work involves the use of several semiconductor growth and characterization techniques. This chapter gives an overview of the growth and characterization techniques that are used throughout the thesis.

2.1 Materials Growth

2.1.1 Ultra-high vacuum chemical vapor deposition (UHVCVD)

Ultra-high vacuum chemical vapor deposition (UHVCVD) was used for the growth of SiGe graded buffers used in this work. The UHVCVD technique was developed to address the issue of low temperature deposition of epitaxial layers. To minimize the impurity incorporation in the epitaxial films at low growth rates, resulting from low deposition temperature, the background contamination of the system must be minimized. The UHVCVD technique uses a turbo-pumped quartz tube furnace evacuated to a background pressure of $10^{-9}$ Torr with background oxygen levels typically $<10^{-10}$ Torr. The precursor gases are injected directly into the turbo-pumped system yielding growth pressures ranging between 1-25 mTorr.

A schematic of the UHVCVD reactor used in the present study is given in Figure 8. This is custom-built vertical reactor designed for SiGe growths. The load-locked system consists of a hot-walled quartz reaction chamber. Turbo molecular pumps backed by a
common foreline, which is maintained at $10^{-3}$ Torr by roots and rotary-vane pumps, evacuate the reaction chamber and load-lock. The reaction chamber is baked out to a background pressure of $10^{-9}$ Torr.

![Diagram of the UHVCVD system](image)

**Figure 8:** Schematic of the UHVCVD system.

The UHVCVD system used in this study employs SiH$_4$ and GeH$_4$ source gases. Dopants are supplied via 1% B$_2$H$_6$ in H$_2$ and 1% PH$_3$ in H$_2$ gases, which can be further diluted with either H$_2$ or Ar via two dilution stages. An added benefit of UHVCVD stems from its hot-walled reaction chamber which allows simultaneous growth on multiple substrates. The growth chamber holds up to ten 150 mm Si wafers at once. This makes
the reactor suitable for the growth of relaxed graded buffers as a batch process. Growth temperatures can be varied from 400°C to 900°C. Growth pressure can be controlled by partially closing a gate valve over the reactor turbo pump. Since film growth occurs on both sides of the wafer in a hot-walled CVD system, use of double side polished substrates is a simple yet effective way to reduce wafer curvature induced by thermal stress.

The threading dislocation density of compositionally graded buffers is exponentially dependent on growth temperature. High growth temperatures are necessary to maximize the relaxation kinetics in graded buffers leading to low threading dislocation density. However, the relatively low cracking temperature of the GeH₄ precursor gas leads to nucleation of solid particles in the gas stream resulting in poor surface morphology of the deposited film.

![Composition plot](image)

**Figure 9:** Growth temperatures used for growing Si₁₋ₓGeₓ compositionally graded buffers via UHVCVD using SiH₄ and GeH₄ precursor gases.
Fortunately, the activation energy for dislocation glide decreases with Ge composition in the graded layers. Consequently, the growth temperature can be reduced when increasing the Ge content in the growing film thereby suppressing gas phase nucleation without sacrificing strain relaxation kinetics. Using SiH₄ and GeH₄ precursors, the growth temperature of the graded buffer was maintained between 0.7Tₘ and 0.8Tₘ as shown in Figure 9, where Tₘ is the absolute melting temperature of the growing Si₁₋ₓGeₓ film.

Prior to growth, Si wafers are typically subjected to a 10 minute piranha clean (3:1 H₂SO₄:H₂O₂) followed by a 1 minute HF dip (10:1 H₂O:HF), which yields a clean hydrogen-terminated surface. This procedure leaves the surface highly hydrophobic. Furthermore, the HF etch terminates the surface with hydrogen bonds, protecting it against the formation of SiO₂. Despite exposure to ambient concentrations of oxygen and water vapor, the surface passivation is sufficiently stable to allow loading of oxide-free silicon wafers into the loadlock of the reactor. Wafers are then immediately loaded into the UHVCVD load-lock, which is pumped down for at least two hours, and typically overnight. Prior to growth, wafers are held at roughly 200°C for 30 minutes to desorb organics. Finally, immediately prior to growth, wafers are subjected to a high-temperature desorption step (typically 900°C) to remove native oxide. A 1 μm homoepitaxial buffer layer is then deposited to bury any residual impurities. Growth of SiGe layers proceeds after homoepitaxial buffer growth.
2.1.2 Metal-organic chemical vapor deposition (MOCVD)

Metal-organic chemical vapor deposition (MOCVD) was used for epitaxial growth of GaAs$_y$P$_{1-y}$ layers on Si$_{1-x}$Ge$_x$ virtual substrates. In MOCVD, controlled pyrolysis of precursor gases occurs as they pass over the heated wafer, depositing the desired reagents (In, Ga, P, etc.) while waste products are carried away (H$_2$, CH$_4$, etc.). Stringfellow provides an excellent reference for MOCVD technology. Growth models used in this study are well-described in. Some of the critical process parameters include reactor pressure, susceptor temperature, gas flow rates and ratios and the ratio of V/III partial pressures.

The close-coupled showerhead configuration prevents mixing of the precursors until ~1cm from the wafer surface and ensures uniform distribution of the gaseous species. This prevents the gases to react until they reach the wafer surface and particle formation. The SiC susceptors are graphite coated and are heated by a graphite resistance heater allowing growth on 2”, 4”, 6” and 8” wafers. This reactor has the unique capability of depositing both group III-V and group IV species, thus allowing the in situ grown GaAsP/SiGe heterostructures demonstrated in this thesis. It also provides real time pyrometry and single wavelength reflectivity data through a Laytec® EpiTT reflectivity measurement system. The growth pressure is controlled via a mechanical roughing pump with a throttle valve that is used for maintaining constant pressure during the semiconductor growth.
Multiple holes in showerhead design help inject precursors uniformly over the wafer surface maintaining a uniform boundary layer thickness and homogeneous gas composition over the rotating susceptor. The N₂-purged glovebox encloses the reactor main chamber preventing the exposure of it to the ambient air during transferring wafers to/from the system. This significantly reduces the surface contamination that makes the deposition of high quality semiconductor growth possible.
Figure 11: Close-coupled showerhead of the MOCVD system.

The susceptor temperature was measured using broadband optical pyrometry with measurement accuracy to within 1°C. This was critical in achieving high film quality of GaAsP on SiGe virtual substrates by precisely controlling the susceptor temperature, as will be mentioned later in the thesis. Calibration was accomplished under well-controlled conditions including freshly cleaned and coated quartzware, uncoated susceptor and growth pressure and gas flow rates. The quartz probes used for measuring the temperature across the susceptor were calibrated with a black-body temperature standard.
In this way, power delivery requirements and thermostat setpoints which provided an accurate and flat temperature profile could be determined for any temperature up to 850°C.

2.2 Materials Characterization

2.2.1 Transmission electron microscopy (TEM)

Transmission electron microscopy was extensively utilized in this work. A transmission electron microscope (TEM) consists of a high-energy (~200keV) electron source and a series of electromagnetic lenses for focusing the electrons into a beam incident on the sample and for image formation. The arrangement of components in a TEM is actually quite analogous to the arrangement of components in a transmission optical microscope, with an electron source and electromagnetic lenses substituted for a light source and optical lenses. Thus, the operation of the TEM can be understood at a rudimentary level using the same sorts of optical ray diagrams that are commonly employed for basic descriptions of light microscopy. One key breakdown in the TEM/optical microscope analogy is that, unlike optical lenses, the characteristics of electromagnetic lenses (magnification, aberrations, etc.) can be adjusted during microscope operation by varying current flows to the lens components, whereas the characteristics of optical lenses is determined during the lens manufacturing process and cannot be adjusted during operation. Thus, correction of lens imperfections (astigmatism in particular) can be
achieved by adjusting current flows in the instrument to obtain a higher-resolution image. Just as transmission optical microscopy requires optically transparent samples, TEM requires an electron-transparent specimen in order for it to be imaged. However, while many materials are optically transparent at macroscopic thicknesses, the semiconductors studied in this work are only electron-transparent at very thin thicknesses, generally less than one micron. Thus, unless the specimen of interest is already electron-transparent (certain nanostructures), TEM requires that the samples be thinned to electron transparency before imaging. This thinning requirement can be very difficult to fulfill for some materials, and the quality of TEM sample preparation often limits the amount of information that can be obtained from the specimen. Thus, successful TEM sample preparation requires a preparation technique that is well suited to the material under study.

TEM samples used in this study were prepared using a combination of mechanical grinding and ion milling. In this work, two different specimen orientations were employed: cross-section and plan-view. Cross-sectional TEM (XTEM) specimens were prepared by gluing the two pieces of the sample face-to-face using epoxy. They were mechanically polished down to a thickness of approximately 8μm, finishing with a 0.3μm SiO₂ slurry grit on both sides. The sample was then ion milled using a Fischione Ion Mill from both sides of the specimen until the specimen was perforated in the center. The specimen area in the vicinity of the perforation was then thin enough for electron-transparency. Preparation of plan-view (PVTEM) samples was similar, except that specimens were thinned from the backside only. Cryo-milling was used in some cases to
prevent the samples from getting over milled.

One of the uses of TEM in this work was to observe crystallographic defects. Defect imaging in this work was achieved through the use of two-beam diffraction conditions.\textsuperscript{27} In this work, 220 two-beam diffraction conditions were employed for imaging of crystallographic defects, including dislocations, stacking faults, and anti-phase boundaries. For cross-sectional TEM, samples for defect imaging were tilted to create a 220 two-beam condition in the vicinity of the $\langle 011 \rangle$ pole. This is found to provide good defect contrast for dislocations and stacking faults\textsuperscript{27} as well as anti-phase boundaries.\textsuperscript{28} Dislocations and stacking faults can be identified based on their resemblance to images of dislocations and stacking faults reported in the literature, taken under similar diffraction conditions. Other diffraction conditions employed in this work were 004 two-beam conditions (for strain layer contrast enhancement) and directly along the $\langle 011 \rangle$ pole (for high-resolution TEM). Imaging the interference patterns arising between diffracted and forward scattered electrons enabling resolution of individual lattice planes can also create high-resolution TEM (HRTEM) images.

In addition to observing material defects, TEM can also be used to unambiguously measure dislocation densities under the correct contrast conditions. However, the small sample area of TEM can limit this. For instance, in cross-sectional TEM, a threading dislocation density of at least $10^8 \text{ cm}^{-2}$ is typically required in order to reliably observe threading dislocations.\textsuperscript{29} Thus, the lack of threading dislocations in a cross-sectional TEM sample only indicates that the TDD is less than $\sim10^8 \text{ cm}^{-2}$ and cannot provide more
information than that. Plan-view TEM can be used to measure lower TDD values because it probes a larger area of the sample. In the TEM used in this thesis, an image taken at 5000x (one of the lowest magnification settings for this instrument) covers a sample area of \(2.2 \times 10^{-7} \text{ cm}^2\). Thus, a TDD of \(4.5 \times 10^6 \text{ cm}^{-2}\) corresponds to an average of one thread per image at this magnification. It is not clear the number of threads that must be counted in order to obtain a reliable average TDD, but it seems clear that TDD values below this level will become increasingly error-prone. TDD measurements in this study were taken using at least thirty images. Error bars and margins of error reported in this work correspond to the 95% confidence interval

### 2.2.2 Differential Interference Contrast (Nomarski) Microscopy

Optical microscopy can provide valuable information about surface morphology in semiconductor processing. Conventional optical microscopy relies on variations in surface reflectivity to create contrast, requiring biological samples to be dyed prior to imaging. There is a very minor variation in the reflectivity of a semiconductor film that makes it difficult to image using standard optical techniques due to poor contrast. The use of differential interference contrast microscopy (Nomarski) enhances the contrast of the semiconductor film. In this technique, the polarized optical light source is divided into two beams that are incident on the sample and then recombined in the microscope. Small variations of sample height produce a different optical path length for the two beams, which results in interference when the beams are recombined. This helps in detecting variations in the surface height of the semiconductor film to the nanometer scale. This
enables imaging samples that have cross-hatch by improving the image contrast.

2.2.3 Etch-Pit Density (EPD)

PVTEM isn’t very useful in measuring the TDD values of Si$_{1-x}$Ge$_x$ virtual substrates that have the TDD values less than $10^6$ cm$^{-2}$, making the use of another technique for measuring the defect density important. A defect etch can be used etch preferentially at the surface of a threading dislocation creating an etch pit. Nomarski microscopy can then be utilized for imaging these pits. Since the sampling area in optical microscopy is large, etch-pit density is a particularly important technique for measuring low defect densities and identifying dislocation pile-ups.
Figure 12: Nomarski images of CMPed SiGe virtual substrate (a) before and (b) after 3 min of EPD etch. The etching treatment produces etch pits as well as additional roughening of the surface.

Schimmel has developed a reliable etch-pit density (EPD) etchant for Si consisting of a mixture of CrO₃, HF, and H₂O.³⁰ The work of Lai further established that a modified version of this etch (8g CrO₃, 200mL HF, 250mL H₂O) can create etch pits on Si₁₋ₓGeₓ virtual substrates with xₓGe up to 70%.³¹ The TDD values of all Si₁₋ₓGeₓ virtual substrates with xₓGe = 70% or less were measured using this etch recipe. The Ge content of the film governs the etching time necessary to form visible etch pits on the surface.
Figure 12 shows the effect of this etching treatment on a Si$_{0.5}$Ge$_{0.5}$ virtual substrate. The sample surface was polished prior to etching to remove the surface roughness and to eliminate any mistake while counting the etch pits. Figure 12a shows a nearly feature-less surface of the sample after 10 min of etching as seen under Nomarski. Figure 12b clearly shows etch pits and the roughness pattern similar to the cross-hatch on Si$_{1-x}$Ge$_x$ virtual substrates. This indicates that the EPD etch probably has some selectivity to strain fields of underlying misfit dislocations, the cause of surface crosshatch.$^{32}$

For EPD measurements of Ge, Baribeau reported that an etchant consisting of 300 mg of iodine dissolved in a 5:10:11 solution of hydrofluoric acid (HF), nitric acid (HNO$_3$), and acetic acid (CH$_3$COOH) was effective at producing producing etch pits in Ge.$^{33}$ Because of the high etching rate of this etchant (300 nm/sec), the Ge virtual substrates are etched with a quick dip of 2 sec in the etchant followed by rinsing with water to remove any etchant species from the surface of the sample terminating any further etching. This has proven effective for TDD determination of Ge virtual substrates, and Luan later correlated the data from this EPD procedure for Ge with PVTEM results and showed that they were in agreement to within a factor of two.$^{34}$

Because of the various sources of error in the EPD measurements, especially when the dislocation density is very high, the data needs to be correlated with other techniques, like PVTEM, to accurately determine the TDD. Factors such as impurity concentration, etch chemistry and the extreme sensitivity of etch selectivity to film doping can also introduce errors in the TDD measurements.
EPD technique usually covers a much larger area of the sample than PVTEM. A standard image through Nomarski is about 1000 times larger than the standard image size for PVTEM. Thus, a typical EPD measurement will provide an average over a much larger area than PVTEM, making it much less susceptible to local fluctuations in TDD on the surface. EPD measurements in this study were taken using at least twenty images. Error bars and margins of error reported in this thesis correspond to the 95% confidence interval.

2.2.4 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is a useful diagnostic tool for characterizing the surface morphology of deposited films. The underlying mechanism for forming an AFM image is a silicon cantilever mounted on a piezoelectric transducer. The tip of the cantilever has a sharp point that is rastered across the sample surface. A constant force is maintained between the cantilever and the sample surface by application of a voltage to the piezoelectric transducer thus generating a digital image of the surface topography. There are two main types of AFM employed in the characterization of semiconductor surfaces: contact-mode and tapping mode. Tapping mode utilizes a vibrating cantilever to minimize electrostatic interaction between the tip and the sample surface. The height of the cantilever is adjusted to provide a constant feedback from the surface, allowing the surface height to be determined as a function of the position on the surface. All of the atomic-force micrographs presented in this thesis utilized tapping-mode imaging. This
technique can be used for areas ranging from 1×1μm to 50×50μm areas and can provide a height resolution on the order of 1nm.

Since threading dislocations intersecting the sample surface leave small cusps at the surface, AFM can also be used to measure threading dislocation densities. However, because practical scan areas in AFM are limited, this technique is only applicable when the threading dislocation is high. As with the other techniques described above, threading dislocation density measurements obtained by AFM should be compared with those obtained by other techniques.

2.2.5 X-ray diffraction (XRD)

XRD can be used to determine the strain state of the epitaxial thin films by measuring both the in-plane and out-of-plane lattice parameter of a semiconductor layer. In the case of semiconductor alloys such as Si_{1-x}Ge_{x}, the in-plane and out-of-plane lattice parameters can be used to determine the composition x_{Ge} according to Vegard’s Law. It states that the lattice parameter of the alloy is a linear interpolation of the lattice parameter of the pure substances. GaAs_{y}P_{1-y} alloy compositions in this work were also determined, through Vegard’s law, by interpolation of lattice parameter between GaP and GaAs.

By using the technique described by Matney and Goorsky the 004 and 224 diffraction peaks of each epitaxial layer of interest were measured and their locations were compared to the 004 and 224 peaks of the substrate to determine in-plane and out-of-plane lattice...
Both 004 and 224 diffraction peaks from each layer as well as the substrate were measured to determine the strain state. Figure 13 shows the angle of the x-ray beam’s incidence and exit for these diffraction peaks relative to an exactly oriented (001) semiconductor wafer. Because the angle of incidence equals the angle of exit for 004 peak it is named as symmetric, while the 224 peak is asymmetric.

Figure 13: Schematic illustration of the angle of incidence and exit of the x-ray beam relative to the wafer surface for both 004 and 224 reflections. The 224 diffraction condition in this case displays the glancing-incidence geometry, which was used in this work.

The values of $2\theta$ and $\omega$ (the angle between the sample stage and the diffracting plane) for the 004 and 224 diffraction peaks of the substrate and each layer of interest were measured for each sample. The difference in peak positions between the layer diffraction
peaks and the substrate diffraction peaks is then calculated and used to estimate the composition and strain state.

Triple-axis reciprocal space maps, in which a series of $\theta/2\theta$ scans are taken at various $\theta$ values, are useful for determining strain and composition and are more accurate than $\theta/2\theta$ scans. The strain and the composition of the sample can be determined using one or both of these techniques.

### 2.2.6 Secondary ion mass spectroscopy (SIMS)

Secondary ion mass spectroscopy (SIMS) was used to measure chemical concentration of various species as a function of depth in epitaxial films. Alloy composition as a function of depth and information on a wide variety of dopants and impurities can be obtained from the SIMS data. This involves sputtering of the film to remove material from the film. Information on the concentration of chemical species can be determined by analyzing the removed material via mass spectroscopy. A focused ion beam is used to ionize the material from the sample and the secondary ions are then accelerated through a magnetic field. The mass of the ions governs their trajectory through the magnetic field, allowing them to be separated so that their concentration can be measured independently.\(^{37}\)

A plot of concentration versus depth in the structure can be determined by evaluating the chemical concentration of the species as the etch progresses deeper into the sample.
SIMS samples a finite volume below the sputtered surface resulting in ion mixing artifacts for layer thicknesses on the order of the sampling depth. By minimizing the energy of the incident beam these artifacts can be limited. The Evans Analytical Group performed the SIMS analysis in this work.
Chapter 3: Direct Integration of GaP on Si
3.1 Direct Initiation of GaP on Si via Multiple Deposition Approaches

A very small lattice mismatch (0.37% at 300K) between gallium phosphide (GaP) and Si makes GaP the most suitable III-V material for direct epitaxial integration on Si. However, previous attempts have shown the presence of defects such as stacking faults (SF) and anti-phase boundaries (APB) in the GaP films.\textsuperscript{38} Despite the lattice-matched condition of GaP on Si, low defect density GaP on Si (i.e., free of stacking faults, free of anti-phase domains, and with a dislocation density less than $10^6$/cm$^2$) has not been reported in the literature.\textsuperscript{39} In contrast, the analogous GaAs/Ge interface has been demonstrated to be controllable and under the proper conditions, low defect density GaAs can be grown epitaxially on Ge. Ting, et al.,\textsuperscript{40} showed that the use of 6° offcut (100) Ge substrates combined with the proper surface annealing sequence, prior to the initiation of GaAs epitaxy in an appropriate temperature window, could produce high-quality GaAs thin films on Ge. However, similar success in the GaP/Si system has yet to be truly realized. Over a range of growth conditions, GaP on Si tends to grow with a three-dimensional island morphology with a high density of microstructural defects, including stacking faults, threading dislocations and twins.\textsuperscript{41}

Direct deposition of GaP on Si was attempted initially. The Aixtron metal-organic chemical vapor deposition (MOCVD) reactor (close coupled showerhead design) we used for our experiments has the unique ability to grow III-V compounds along with group IV semiconductors. The Si substrates used in this study were (001) oriented with 6° offcut
towards the nearest {111} plane. The specification of the 6° offcut is important because it provides a step structure which suppresses and eliminates APD, which is detrimental to the material quality, during the growth of III-V compounds on group IV semiconductors. Prior to the growth, Si wafers were subjected to a 10 minute piranha clean (3:1 H₂SO₄:H₂O₂) followed by a 1 minute HF dip (10:1 H₂O₂:HF), which yields a clean hydrogen-terminated surface. Homoepitaxial Si was deposited on these wafers at 850°C to bury the surface contaminants and obtain a pristine surface for subsequent heteroepitaxy. This was followed by a 10 min anneal at 850°C to recover the double-stepped surface structure. GaP was initiated on Si using CVD and atomic layer deposition (ALD) at various temperatures and initiation conditions. The samples were characterized with plan-view and cross-sectional transmission electron microscopy (PVTEM and XTEM) to study the microstructure and interface quality of the final film, atomic force microscopy (AFM) to examine the surface morphology and x-ray diffraction (XRD) to determine the lattice constant and degree of lattice-matching.

It was observed that some parameters have a significant effect of the film quality. The growth temperature of GaP affects the morphology of the film. The GaP films grown via CVD technique at 850°C exhibited very rough surface with a root mean square (RMS) roughness of 28 nm (Figure 14a). The Nomarski image of this sample shows droplet formation at the surface. This can be attributed to TMGa being exposed to a very high temperature and melting at the surface and increased reactivity between P and Si that spoils the double-stepped surface structure important for achieving high quality III-V thin films. To avoid these issues the growth temperature was lowered to 500°C and the
surface morphology shows improvement as compared to when the growth temperature was higher. This can be seen in the Nomarski image of the GaP film (Figure 14b). This improvement in the film morphology by lowering the growth temperature led us to explore atomic layer deposition (ALD) at lower temperatures to initiate the films at the slow growth rate, allowing the precursors to cover the entire wafer and prevent three-dimensional island morphology.

Figure 14: Nomarski images of GaP films deposited at (a) 850°C and (b) 500°C on Si substrates.

The MOCVD reactor was calibrated to precisely control the flux of precursors to mimic an ALD process. The ALD process utilized in this study involved a flux of either TMGa or PH₃ giving enough time to physically adsorb on the Si wafer surface. This was
followed by purging the precursor with N2 or H2 to get rid of the excess precursor in the chamber. Then the other precursor was introduced to react with the adsorbed species. This was again followed by the purge with N2 or H2. This process was then repeated for 20-25 cycles. All the steps were of the same duration between 6-10 sec. After getting the initial deposition via ALD, the rest of the film was grown via CVD mode.

Figure 15: RMS roughness of the GaP films grown via CVD and ALD techniques. In the case of ALD, the precursor used to initiate the deposition is indicated. The carrier gas and the deposition temperatures are also mentioned.

Figure 15 summarizes the RMS roughness data for various growth techniques, ALD initiation conditions, growth temperatures and carries gases. The film quality is better for the case of ALD films as compared to the CVD deposited films at low temperatures. The
ALD initiation conditions and the carrier gases don't affect the film quality significantly. However, these films show much improved results than the high temperature CVD growth of GaP.

GaP deposited at 850°C using CVD exhibited three-dimensional island initiation and poor adhesion at the interface (Figure 16). Whereas, planar GaP films on Si were obtained at lower temperature (500°C) using the ALD technique. AFM images confirmed the better quality of films through ALD as compared to CVD, where the RMS roughness of films grown via ALD was almost two orders of magnitude lower than those grown via CVD (Figure 17). The results illustrate that parameters such as the growth temperature, substrate orientation, growth rate and technique can affect the film quality considerably. While V/III ratio, growth ambient and ALD initiation sequence have an insignificant impact on the films. Low temperature and using the ALD technique on offcut Si substrates yielded GaP films with best surface morphology.
Figure 16: Cross-sectional <220> bright field TEM images of (a) GaP on Si grown via CVD at 850°C and (b) GaP on Si grown via ALD at 500°C.

Figure 17: AFM scans of (a) GaP on Si grown via CVD at 850°C and (b) GaP on Si grown via ALD at 500°C.

However, despite getting a planar surface morphology in the GaP films, the threading dislocation density (TDD) was observed to be high (~ 10^8 cm^-2). High TDD makes the GaP films on Si unsuitable for solar cell processing and our approach will have to be modified to advance the film quality before progressing to solar cell fabrication. To
improve the film quality the deposition needs to be initiated at a low temperature to avoid the P and Si interaction. This is restricted by the limitation of an MOCVD reactor that uses PH$_3$ as a precursor for P. PH$_3$ doesn’t crack readily at temperatures lower than ~450°C, significantly slowing the growth rate.

This led us to collaborate with Prof. Steve Ringel’s group at the Ohio State University (OSU). Direct deposition of GaP on Si was performed in a Varian Gen II solid source molecular beam epitaxy (MBE) chamber with a valved P$_2$ cracker with a background pressure below $2 \times 10^{-10}$ Torr. The growth in this case can be initiated at temperatures as low as 325°C due to the availability of P$_2$ as a precursor. The particulars of this heteroepitaxial growth process have been detailed elsewhere, but it should be noted that the bulk of the GaP grown for these samples was done at significantly lower temperatures than that of the MOCVD samples discussed above. This has resulted in the elimination of stacking faults from the GaP films on Si using migration enhanced epitaxy in a MBE reactor. Though this led to the elimination of anti-phase domains and stacking faults, the TDD still remains high for device processing. This led us to explore an approach that can account for the 0.37% lattice mismatch between GaP and Si.

### 3.2 Structure for Closer Lattice-Matching

We explored the integration of III-V on various compositions of Si$_{1-x}$Ge$_x$ substrate. The next step in the evolution of III-V/IV epitaxy is the exploration of integrating III-V materials onto a mixed Si$_{1-x}$Ge$_x$ substrate. This integration process is appealing because
Si$_{1-x}$Ge$_x$ grading is an established technology capable of TD density $<1 \times 10^6$ cm$^{-2}$ when graded completely to Ge. Therefore successful integration of GaAsP on SiGe will lead to low TDD virtual substrates for III-V based devices on Si.

![Lattice-mismatch vs. temperature relationships for the GaP/Si(Ge) and GaAs/Ge systems](image)

Figure 18: Lattice-mismatch vs. temperature relationships for the GaP/Si(Ge) and GaAs/Ge systems, showing how the addition of 12% Ge effectively bridges the lattice-mismatch between the GaP film and underlying SiGe.

The lattice constant can cover the entire compositional range from GaP to GaAs by changing the Ge content of the Si$_{1-x}$Ge$_x$ alloy. This makes it possible to grow lattice matched GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ heterostructures across all compositions of GaAs$_y$P$_{1-y}$. GaP was grown on Si$_{0.88}$Ge$_{0.12}$ virtual substrates which make them lattice matched at 325°C (Figure 18). Extremely low TDD of $1 \times 10^5$ cm$^{-2}$ can be achieved for this composition of Si$_{1-x}$Ge$_x$ alloys. This section will describe the successful heteroepitaxial integration of lattice matched GaP/Si$_{0.88}$Ge$_{0.12}$ (Figure 19).
Figure 19: Schematic illustration of GaP/Si$_{0.88}$Ge$_{0.12}$ growth structure for reduced interfacial misfit.

The SiGe templates were grown via UHVCVD on Si(001) offcut 6° toward <111>, with an average grading rate of 10% Ge μm$^{-1}$ and a 1 μm thick cap layer of a composition of Si$_{0.88}$Ge$_{0.12}$. EPD analysis showed a TDD of 1-3×10$^4$ cm$^{-2}$ (Figure 20) and XRD confirmed the composition to be 12% Ge. The 6” virtual substrate wafers were cleaved into smaller pieces before wet chemical cleaning and further deposition in MBE.
GaP/Si$_{0.88}$Ge$_{0.12}$ structures were initiated with a strained Si cap layer following a 550°C pre-epitaxy anneal (Figure 19). AFM analysis was done after the GaP MEE deposition and each subsequent MBE deposition to evaluate the quality of the GaP/ε-Si/Si$_{0.88}$Ge$_{0.12}$. Figure 21a displays a reduction in RMS roughness as compared to the as-received surface after ε-Si epitaxy and GaP MEE. The cross-hatch smoothened out as GaP MBE deposition was done at 680°C and was grown to a thickness of 1 μm (Figure 21b). This difference is because of the high ad-atom surface mobility at 680°C coupled with thick lattice matched growth.
Figure 21: (a) AFM after Piranha + HF last ex-situ wet etching, 550°C anneal, Si epitaxy, and GaP MEE. (b) AFM after 1 µm total GaP epitaxy.

To evaluate the crystal quality and layer relaxation of the 1 µm GaP on Si_{0.88}Ge_{0.12} XRD reciprocal space mapping (RSM) was done. Figure 22a shows a (004) RSM of GaP/Si_{0.88}Ge_{0.12}. The GaP layer is slightly tensile with respect to the Si_{0.88}Ge_{0.12} virtual substrate as shown by the Si_{0.88}Ge_{0.12} layer peak being away from the Si than the GaP film. The lattice mismatch will increase with increasing temperature because of the difference in the coefficient of thermal expansion between GaP and SiGe (Figure 18). The relaxation of the GaP film at the room temperature is very similar to that of GaP/Si grown under identical conditions (Figure 22b).

Analysis of the GaP on Si_{0.88}Ge_{0.12} RSM peaks yields full-width at half-max (FWHM) values similar to those of the GaP/Si (ω_{FWHM} = 310 arcsec and ω-2θ_{FWHM} = 53 arcsec).
This indicates that GaP/Si$_{0.88}$Ge$_{0.12}$ is of high crystalline quality and is free of such defects as stacking faults, microtwins and APDs.

Figure 22: High resolution (004) TA-XRD RSMs of (a) GaP/Si$_{0.88}$Ge$_{0.12}$ and (b) GaP/Si showing identical degrees of relaxation.

Figure 23 shows PVTEM and XTEM images indicating higher TDD and APDs nucleation whereas XRD results imply that the GaP/Si$_{0.88}$Ge$_{0.12}$ is of high quality. The TDD calculated from PVTEM resulted in the defect density of $\sim$1-3x$10^7$ cm$^{-2}$ in the GaP film, higher than that of the underlying SiGe virtual substrate. XTEM images do not indicate any presence of misfit dislocations at the interface between $\varepsilon$-Si and Si$_{0.88}$Ge$_{0.12}$ substrate.
Self-terminating APDs are visible in Figure 23b at the GaP/e-Si interface. The higher TDD is likely due to the formation of a threading dislocation from a large APD. However, this shows significant improvement with a reduction in the TDD by ~10x than the previously reported results in the case of direct deposition of GaP film on Si substrate.

3.3 Summary

This chapter summarized the successful integration of GaP film on Si wafer via a Si$_{0.88}$Ge$_{0.12}$ virtual substrate bridging the lattice mismatch between GaP and Si. The TDD in the GaP film was lowered by ~10x than the previously reported GaP/Si results. These improvements will open up the opportunities for future progress.
Further research will be done to understand the temperature dependence on the film quality by depositing GaP on higher Ge content SiGe virtual substrates (Si$_{0.85}$Ge$_{0.15}$ and Si$_{0.80}$Ge$_{0.20}$). This will help develop fundamental understanding of the misfit magnitude and sign at the heterovalent interface, leading to the lowest TDD in the GaP film.
Chapter 4: Integration of GaAsP on SiGe
Due to the inability of the current research directions to lower the dislocation density to the device quality level, in the III-V/Si system, it is apparent that alternative approaches must be considered. An innovative approach, which involves engineering the Si substrate’s lattice constant prior to III-V deposition, can be used to accommodate for the mismatch in both III-V and IV materials. In this way, the lattice mismatch can be addressed in a material system and under growth conditions that are independent from the III-V device layers. Hence, a wider range of growth conditions (temperature, growth rate, etc.) may be accessible to achieve optimal lattice relaxation than can be provided by the III-V layers. The Si$_{1-x}$Ge$_x$ alloy system is well-suited for this application since by increasing the Ge content ($x$) during growth of a Si$_{1-x}$Ge$_x$ epitaxial layer on Si, the lattice constant can be increased from that of Si to Ge, providing a close lattice match for subsequent GaAsP-based device growth. This chapter presents results on the integration of GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$/Si to investigate the integration of films between the two extremes of GaP/Si and GaAs/Ge. It stands to reason that the growth behavior of lattice-matched GaAs$_y$P$_{1-y}$ on Si$_{1-x}$Ge$_x$ will be some combination of the behavior of the GaAs/Ge and GaP/Si systems and will depend on the alloy composition chosen. One aim of this study is to investigate different alloy combinations to better understand the transition from GaAs/Ge behavior to GaP/Si behavior.

4.1 Experimental Procedures

All the growths in this study utilized (100) Si substrates with a 6° offcut towards the nearest {111} plane. The specification of the 6° offcut is important because it provides,
with proper substrate annealing, a step structure that suppresses and eliminates anti-phase disorder, which is detrimental to material quality, during the growth of III-V compounds on group IV semiconductors. Prior to the growth, Si wafers were subjected to a 10 minute piranha clean (3:1 H₂SO₄:H₂O₂) followed by a 1 minute HF dip (10:1 H₂O:HF), which yields a clean hydrogen-terminated surface. The initial SiₓGe₁₋ₓ growth was conducted in an ultra high vacuum chemical vapor deposition (UHVCVD) reactor at a nominal growth pressure of 25 mTorr. The growth was done at 900°C with SiH₄ and GeH₄ precursors. After the growth of a homoepitaxial Si layer, SiₓGe₁₋ₓ was compositionally graded at a rate of Δx₉Ge = 0.10/µm to Si₀.₅Ge₀.₅ and capped with a 1.5 µm thick, fully relaxed Si₀.₅Ge₀.₅ layer. The surface morphology of the graded buffer evolves during growth as adatom diffusion is influenced by surface strain fields generated by the orthogonal arrays of misfit dislocations within the graded buffer. This can cause deep surface cross-hatch which leads to dislocation pile-ups and increased threading dislocation density. To maintain low pile-up density and minimize the surface roughness of the final layer, Ge virtual substrates were grown in two intervals. The compositionally graded buffer was grown by increasing the Ge fraction in 200 nm (2% Ge) intervals to an initial composition of Si₀.₅Ge₀.₅. The wafers (with Si₀.₅Ge₀.₅ cap) were then removed from the reactor and planarized using a chemo-mechanical polishing (CMP) step to remove the surface crosshatch. After planarization, the virtual substrates were subjected to two consecutive piranha/HF cleaning procedures, as described earlier. The first piranha/HF etch was preformed to remove any residual CMP slurry particles from the Si₀.₅Ge₀.₅ surface, while the second was done to prepare the wafers for growth.
Subsequent deposition was performed in a specially designed Aixtron (close-coupled showerhead) metal-organic chemical vapor deposition (MOCVD) reactor that has the unique ability to grow III-V compounds as well as group IV semiconductors. All growths for this phase of the study were completed at 100 Torr using N₂/H₂ carrier gas with SiH₄, GeH₄, AsH₃, PH₃ and tri-methyl gallium (TMGa) as precursors for the Si, Ge, As, P and Ga, respectively. Before loading the Si₀.₅Ge₀.₅ virtual substrates into the MOCVD reactor, they were chemically cleaned with the procedure noted earlier. Prior to initiation of epitaxy the Si₀.₅Ge₀.₅ virtual substrates were annealed in the reactor at 825°C in N₂ for 10 minutes to drive off any moisture from the surface and desorb any native oxide. Si₀.₅Ge₀.₅ was homo-epitaxially grown at 825°C under an H₂ ambient to bury any remaining contaminants and to ensure a pristine surface for subsequent growth. If necessary, further compositional grading of Si₁₋ₓGeₓ was carried out at 750°C under H₂, after which the wafer was annealed under a N₂ ambient in order to obtain a double-stepped surface. N₂ was used to prevent any potential etching of the Si₁₋ₓGeₓ that could ensue at an elevated temperature due to the presence of H₂. The substrate was then quenched to the GaAsP nucleation temperature, locking in the surface step structure.⁴⁶

The work of Ting⁴⁷, Groenert⁴⁸ and others have concluded that the high-quality growth of GaAs on Ge by MOCVD can only be achieved within certain growth temperature windows, and thus growth temperature was also explored in this experiment series. Our adaptation of the GaAs on Ge procedure of Ting uses a growth temperature of 650°C and produces good results, so GaAs₀.₅P₀.₅ growth temperatures of 650, 700 and 725°C for this series. The temperatures were increased over the optimal GaAs on Ge temperature based
on the hypothesis that the temperature window will move to higher temperatures due to the increased melting point of the GaAs$_y$P$_{1-y}$ layers and Si$_{1-x}$Ge$_x$ virtual substrates as compared to GaAs and Ge, respectively. Lattice-matched GaAs$_y$P$_{1-y}$ was initiated on the Si$_{1-x}$Ge$_x$ at 650, 700 and 725°C with a relatively high V/III ratio (257) with a low TMG flow to grow a thin (100 nm) nucleation layer at a slow growth rate, after which the V/III ratio was reduced (TMGa flow increased) to 102 for the remainder of the film growth in order to grow at a faster rate. After the GaAs$_y$P$_{1-y}$ growth, the layer was capped with a very thin (10Å) strained GaAs layer or lattice-matched In$_x$Ga$_{1-x}$P layer so as to prevent the post-growth surface roughening due to uncontrolled non-stoichiometric depletion of As and P species as the wafer cools to the room temperature. Post-growth analysis of all the films grown in this study included plan-view and x-sectional transmission electron microscopy (PVTEM and XTEM) and x-ray diffraction (XRD).

4.2 Discussion

In this experiment set, lattice-matched GaAs$_y$P$_{1-y}$ layers were grown directly on Si$_{0.5}$Ge$_{0.5}$, Si$_{0.4}$Ge$_{0.6}$ and Si$_{0.3}$Ge$_{0.7}$ virtual substrate compositions; the corresponding lattice-matched GaAs$_y$P$_{1-y}$ compositions are $y_{\text{As}} = 46\%$, 58\%, and 68\%, respectively. The GaAsP films across all compositions exhibited a planar surface morphology over the entire sample area (6” wafer).

The homoepitaxy of Si$_{1-x}$Ge$_x$ in MOCVD is a very critical step as it buries the surface exposed to atmosphere after the pre-epitaxial clean. Figure 24 shows the effect of the
homoepitaxial layer grown in the MOCVD reactor on the film quality of GaAs$_y$P$_{1-y}$. Si$_{1-x}$Ge$_x$ was compositionally graded on the Si substrate to Si$_{0.3}$Ge$_{0.7}$ in UHVCVD and the wafer was cleaned before loading it into the MOCVD reactor. Direct initiation of GaAs$_y$P$_{1-y}$ on Si$_{0.3}$Ge$_{0.7}$ resulted in defects at the heterovalent interface, whereas high quality interface was obtained when a layer of Si$_{0.3}$Ge$_{0.7}$ was homoepitaxially grown before the GaAs$_y$P$_{1-y}$ initiation. This proves that the atmospheric exposure contaminates the Si$_{1-x}$Ge$_x$ surface and makes it difficult to recover a clean enough surface for GaAs$_y$P$_{1-y}$ heteroepitaxy.

Figure 24: Cross-sectional <220> bright field TEM images of (a) GaAsP initiated on Si$_{0.3}$Ge$_{0.7}$ without a homoepitaxial layer and (b) GaAsP initiated on Si$_{0.3}$Ge$_{0.7}$ with a homoepitaxial layer.

Figure 25 shows cross-sectional TEM micrographs taken of the GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$/Si(100) films grown at 725°C in this study. Images were taken in g(220) and g(004) (latter not shown) diffraction conditions, at various locations throughout the samples, in order to highlight any defects. XTEM of all three samples clearly reveal a high-quality
crystalline interface between $\text{Si}_{1-x}\text{Ge}_x$ and $\text{GaAs}_{y}\text{P}_{1-y}$ with no rampant dislocation nucleation, anti-phase boundaries, stacking faults, or other crystalline defects.

Figure 25: Cross-sectional $<220>$ bright field TEM images of $\text{GaAs}_y\text{P}_{1-y}$ on (a) $\text{Si}_{0.5}\text{Ge}_{0.5}$, (b) $\text{Si}_{0.4}\text{Ge}_{0.6}$ and (c) $\text{Si}_{0.4}\text{Ge}_{0.7}$ virtual substrates on $6^\circ$ offcut towards the nearest $\{111\}$ plane Si (001) substrate.

Figure 26: Representative plan-view TEM image of $\text{GaAs}_{0.58}\text{P}_{0.42}$ layer grown on $\text{Si}_{0.4}\text{Ge}_{0.6}$ virtual substrate. A threading dislocation can be seen in the image.
The samples in this series were also characterized by x-ray diffraction (XRD) to measure
the degree of lattice-matching of the GaAs$_x$P$_{1-y}$ layer to the Si$_{1-x}$Ge$_x$ virtual substrate. XRD
analysis confirmed the near lattice matching of Si$_{1-x}$Ge$_x$ and GaAs$_x$P$_{1-y}$. PVTEM (Figure
26) was used to quantify the threading dislocation densities and all the samples exhibited
threading dislocation densities $\sim$10$^7$/cm$^2$, a significant improvement over previously
reported results.

The interface quality is comparable with GaAs film grown on Ge, and an order of
magnitude improvement in the TDD was achieved for GaAs$_x$P$_{1-y}$/Si$_{1-x}$Ge$_x$ as compared to
GaP/Si. Another interesting result observed was the decrease in the TDD in the III-V
films with the increasing mismatch of the underlying Si$_{1-x}$Ge$_x$ buffer with respect to Si.
Intuitively, one would expect the TDD to increase with increasing mismatch with silicon.
The counter-intuitive trend observed may be due to the propensity to nucleate
dislocations more easily as P content is increasing in the film. We suspect that is the
deleterious interaction between P and Si at the III-V/IV heterovalent interface is involved
in aiding the higher dislocation nucleation rate. Also, despite lattice-matching of the
GaAsP films with the underlying SiGe virtual substrate, an increase in the TDD of the
GaAsP films by almost 10x-100x was observed as compared to the SiGe virtual substrate.

Therefore there are other sources leading to dislocation nucleation at the heterovalent
interface other than those arising from the lattice mismatch. This increase in the TDD at
the heterovalent interface is studied in more detail in the next chapter.
It was also observed that the growth temperature/process window shrinks down for the high quality integration of GaAsP on SiGe as the P content increases in the film (see Figure 27). The control over process parameters needed to be very precise to get high-quality lattice-matched GaAsP film on Si$_{0.5}$Ge$_{0.5}$ as compared to Si$_{0.3}$Ge$_{0.7}$. This is consistent with the fact that the growth window expands as the composition approaches GaAs/Ge and integration of GaP directly on Si is still a challenge, so the growth window hasn’t yet been figured out. This is verified by the high quality GaAsP growth on Si$_{0.3}$Ge$_{0.7}$ at all the temperatures explored, 650, 700 and 725°C. Whereas APD-free GaAsP film on Si$_{0.5}$Ge$_{0.5}$ was obtained only at 725°C. The other temperatures resulted in the GaAsP film being very defective.

Figure 27: Process/growth window for GaAsP/SiGe heterovalent interface.
4.3 Conclusions

We have explored various processes for lattice-matched GaAs$_y$P$_{1-y}$ growth on Si$_{1-x}$Ge$_x$ virtual substrates using the process for high-quality GaAs growth on Ge as a reference. Although the interface and film quality are very sensitive to growth parameters, we have outlined the growth conditions here to achieve specular GaAs$_y$P$_{1-y}$ layers with low surface roughness and no observed twin boundaries or stacking faults when deposited on Si, Si$_{0.5}$Ge$_{0.5}$, Si$_{0.4}$Ge$_{0.6}$ and Si$_{0.3}$Ge$_{0.7}$ virtual substrates. The difficulty in achieving such high quality films increases as the SiGe surface becomes more silicon-rich. The resulting high-quality GaAs$_y$P$_{1-y}$ virtual substrates provide a promising pathway for III-V/Si device technologies. In particular, the lattice constants near 0.56nm are attractive to creating yellow-green devices integrated on silicon as well as creating high efficiency solar cells on silicon.
Chapter 5: Controlling epitaxial GaAsP/SiGe heterovalent interfaces
5.1 Initiation conditions

Because of the high dislocation density typically produced in GaAs$_{1-y}$P$_{1-y}$ films without controlled nucleation, a series of experiments were done with different initiation sequences on Si$_{0.35}$Ge$_{0.65}$ virtual substrates before the heteroepitaxial film was grown. The Si$_{0.35}$Ge$_{0.65}$ layer was exposed to different precursors (TMGa, AsH$_3$ and PH$_3$) for various durations before growing the GaAs$_{1-y}$P$_{1-y}$ layer at 725°C. This can be summarized in Table 1.

<table>
<thead>
<tr>
<th>Initiation Sequence</th>
<th>PH$_3$</th>
<th>AsH$_3$ + PH$_3$</th>
<th>TMGa + AsH$_3$ + PH$_3$</th>
<th>AsH$_3$</th>
<th>AsH$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td>3 sec</td>
<td>3 sec</td>
<td>-</td>
<td>3 sec</td>
<td>10 sec</td>
</tr>
</tbody>
</table>

Table 1: Summary of the initiation sequences for GaAsP integration on SiGe.

Analysis through XTEM and PVTEM reveals that the best quality GaAs$_{1-y}$P$_{1-y}$ film was obtained when the Si$_{0.35}$Ge$_{0.65}$ surface was exposed to AsH$_3$ for 3 seconds at 725°C (Figure 28).

Exposure to PH$_3$ for 3 seconds resulted in a heavily defective GaAs$_{1-y}$P$_{1-y}$ film. This can be attributed to the reaction between Si and P at the heterovalent interface, which is difficult to avoid because of the high reactivity between the elements. Scanning tunneling microscopy (STM) studies have revealed that exposure of Si (100) surfaces to phosphine leads to the generation of excessive amounts of vacancies and surface disruption due to
ejected silicon atoms.\textsuperscript{50} This interaction disrupts the double-stepped surface of underlying substrate, which is important for preventing the formation of APD. The effect of Si and P interaction becomes less profound as the fraction of PH\textsubscript{3} in the reactor decreases, which is seen as the initiation condition shifts from only PH\textsubscript{3} to PH\textsubscript{3} + AsH\textsubscript{3} and finally to only AsH\textsubscript{3} initiation.

With a moderate exposure to AsH\textsubscript{3} (3 seconds), a thin layer of the precursor adsorbs to the Si\textsubscript{0.35}Ge\textsubscript{0.65} surface. The adsorbed layer helps prevent the underlying silicon from interacting with PH\textsubscript{3}. When the TMGa and PH\textsubscript{3} are introduced to the chamber along with the already flowing AsH\textsubscript{3}, the PH\textsubscript{3} reacts with the metal organic rather than the Si, thereby reducing the formation of unwanted surface morphology. This ultimately

Figure 28: TDD in GaAsP on SiGe using different initiation conditions.

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improves the quality of the GaAs\textsubscript{y}P\textsubscript{1-y} film and reduces the density of threading dislocation.

While a moderate exposure to AsH\textsubscript{3} prior to film growth greatly improved the GaAs\textsubscript{y}P\textsubscript{1-y} quality, prolonged exposures to AsH\textsubscript{3} increased the threading dislocation density in the film. The interface quality exhibited defects at the interface and a high TDD when exposed to 10 seconds of AsH\textsubscript{3} prior to the film growth. It has been reported that prolonged exposure to AsH\textsubscript{3} etches Si surfaces\textsuperscript{51} and Ge\textsuperscript{52} that again prevents the surface from maintaining the necessary double atomic step height. It was noticed that prolonged exposure to AsH\textsubscript{3} and presence of any PH\textsubscript{3} before the growth deteriorates the film quality.

Our findings show that 3 seconds of exposure with AsH\textsubscript{3} is sufficient to prevent any reaction between Si and P, and is also not long enough to start etching the Si\textsubscript{0.35}Ge\textsubscript{0.65} surface. From these experiments it was found that the optimal sequence for initiation is exposing the Si\textsubscript{0.35}Ge\textsubscript{0.65} surface with 3 seconds of AsH\textsubscript{3} before growing the III-V film. For all the experiments described ahead, this initiation sequence was used.

5.2 Strain experiments

To understand the effect of strain at the interface on the defect density in GaAs\textsubscript{y}P\textsubscript{1-y}, GaAs\textsubscript{y}P\textsubscript{1-y} was epitaxially grown on Si\textsubscript{1-x}Ge\textsubscript{x} virtual substrates with different strain conditions. Three compositions of GaAs\textsubscript{y}P\textsubscript{1-y} were 0.2% tensile, lattice-matched and
0.2% compressively strained with respect to underlying Si_{0.35}Ge_{0.65}. All of the GaAs\textsubscript{y}P\textsubscript{1-y} films were grown at 725°C with a 3 seconds AsH\textsubscript{3} initiation before PH\textsubscript{3} and TMGa were introduced (Figure 29). The same experiments were repeated on Si\textsubscript{0.15}Ge\textsubscript{0.85} virtual substrates at 650°C with a 3 sec AsH\textsubscript{3} + PH\textsubscript{3} initiation before TMGa was introduced. As previously mentioned, GaP/Si initiation is the most problematic, whereas GaAs/Ge is the most tolerant, and therefore a Ge concentration of 85% is expected to be more tolerant than the 65% Ge at the interface, but less tolerant than GaAs/Ge.

Figure 29: Schematic illustrations of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsP on 65% Ge virtual substrates fabricated as a part of this study.

Note that 0.2% strain is a very small amount of strain for typical lattice-mismatched epitaxy. In systems with zinc-blende/zinc-blende interfaces or diamond cubic/diamond cubic interfaces (i.e. homovalent), this level of strain does not produce a high density of
threading dislocations in the film. Therefore, one would expect little effect on the quality of the GaAsP in these various films.

Figure 30: Cross-sectional <220> bright field TEM of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsP on 65% Ge virtual substrates.

Figure 31: Representative plan-view <220> bright field TEM image of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsP, grown on Si$_{0.35}$Ge$_{0.65}$ virtual substrates.

Surprisingly, a 0.2% compressively stressed GaAs$_{0.68}$P$_{0.32}$ film deposited on Si$_{0.35}$Ge$_{0.65}$ exhibits $10^9$ cm$^{-2}$ TDD in stark contrast to the lattice matched and 0.2% tensile strained films, which exhibited $10^6$ cm$^{-2}$ TDD (Figure 30 and Figure 31). Thus, a small amount of lattice-mismatch at these interfaces can result in very low yield because of the drastic increase in defect density that occurs if the interface is just slightly mismatched.
compressively. Both of the strained films were grown beyond their critical thickness. Any relative increase in threading dislocation density caused by relaxing the thin film should be seen equally for both signs of strain. To explain the vastly different threading dislocation densities in the GaAs$_y$P$_{1-y}$ films, we propose that an elevated level of point defects accumulate at a compressively strained GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ interface, which condense and form dislocation loops. The loops then expand and lead to high TDD (Figure 32 and Figure 33).

Figure 32: Mechanism for diffusion imbalance, loop nucleation and thread formation.
Figure 33: (a) Dislocation Loop at GaAsP/SiGe interface and (b) dislocation half loop at GaAsP/SiGe interface.

Figure 34: Cross-sectional <220> bright field TEM of (a) 0.2% tensile strained and (b) 0.2% compressive strained GaAsP on 85% Ge virtual substrates.

Similar results were observed for the GaAs$_y$P$_{1-y}$/Si$_{0.15}$Ge$_{0.85}$ interface experiments (Figure 34), where the dislocation density increases in the case of a compressively strained GaAs$_y$P$_{1-y}$ film, even though this interface is very close in composition to the GaAs/Ge interface. These results indicate that tensile strain is better for the GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ heterovalent interface, whereas compressive films lead to dislocation nucleation. This is
further substantiated by the interface quality of the following two systems; GaAs/Ge and GaP/Si. While GaAs films have 0.08% tensile strain with respect to the underlying Ge substrate, GaP films are 0.37% compressively strained with respect to Si at 300K. The GaAs/Ge system has a very broad process window, which results in high quality interface. Even though the GaP/Si system is similar to GaAs/Ge, defects have proven difficult to control at this interface. However $\text{Si}_{0.88}\text{Ge}_{0.12}$ virtual substrates grown on Si provide a nearly ideal lattice-matched template for GaP epitaxy. GaP grown on lattice matched $\text{Si}_{0.88}\text{Ge}_{0.12}$ exhibits an improvement in the TDD by almost an order of magnitude as compared to direct integration of GaP on Si.

Closer examination of the heterovalent interface shows that threading dislocations do not glide far from the loop nucleation event at the interface that produced them. This behavior is consistent with the low degree of mismatch; nucleation occurs, but there is a relatively low driving force for glide. It is likely that the loops condense when the film is very thin, and the image force on the part of the loop closer to the surface pulls the upper part of the loop to the surface, resulting in two threading dislocations when the film is below the critical thickness. Thus, the threads do not glide as there is not yet a large enough over stress. As the film passes through the critical thickness, there is an abundance of threading dislocations due to this interface nucleation mechanism. Therefore, only a fraction of these threading dislocations need to glide short distance to produce enough misfit to relieve the strain. Many of the threading dislocations will remain near their nucleation events.
The origin of the point defects at the interface is likely due to an imbalance in the interdiffusion of group III, V and IV species across the heterovalent interface. This has been verified through SIMS analysis across the heterovalent interface (Figure 35). The high concentration of point defects then condenses and form dislocation loops when the film is thin.

![Graph showing concentration of species across depth](image)

Figure 35: SIMS analysis across the heterovalent interface shows the imbalance in the interdiffusion of species across the interface. This leads to point defect accumulation.

The driving force for point defect condensation is a super saturation of these defects above the equilibrium concentration. Point defects of interest at the GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ interface are interstitial atoms and vacancies. Under a strain state of compression, vacancies are more thermodynamically favored; conversely under a strain state of tension vacancies are thermodynamically unfavorable. Interstitial atoms exhibit an inverse...
relation to strain compared to vacancies. If an excess of vacancies were the source of point defect condensation into dislocation loops, we would expect to see a reduction of loops and thereby threading dislocation density in a tensile strained interface and an increase for a compressively strained interface. This trend is readily observed in the strain study above.

With this knowledge in hand, we discovered that using strain to compensate for this nucleation event in different ways could improve the quality of the GaAs$_y$P$_{1-y}$ film. In one case, thin strained layers of GaAs$_y$P$_{1-y}$ above the GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ interface were introduced as a means to prevent the dislocation loops at the interface from expanding into threading dislocations. A 15 nm thick lattice-matched GaAs$_y$P$_{1-y}$ layer was initiated and grown in the conventional manner followed by a thin tensile-compressive zone of GaAs$_y$P$_{1-y}$ films was grown before further continuing with the lattice-matched layer (Figure 36).

The 0.2% tensile and compressive layers were 10 nm in thickness, which is below the critical thickness for this amount of mismatch. The tensile film was inserted to prevent the dislocation loops present at the heterovalent interface from expanding to the surface and creating threading dislocation segments that are permanently frozen in the film. The purpose of the compressive film was to compensate for the strain introduced from the tensile layer.
Figure 36: Schematic diagram of the loop-trapping structure with a thin tensile-compressive (t-c) zone.

From the XTEM images of this sample, closed loops were observed at the heterovalent interface. Many of the loops have a height of 15 nm, which corresponds to the thickness of the lattice-matched layer under the strained zone, confirming that the loop was prevented from expanding by the strained zone (Figure 37). The loops observed in XTEM have flat features at the top, further indicating that the zone formed a barrier inhibiting the expansion of the loops; however some of the loops observed at the interface had expanded to a height of 60nm (Figure 38), suggesting that more strain and/or thickness would improve the film even further. These loops were also visible in the PVTEM images of the sample and the dimensions matched with those seen through
XTEM. The strained zone was effective in containing the loops at the interface as many were prevented from expanding and the threading dislocation density in the strained zone sample was slightly lower than the conventional lattice matched film sample.

![Figure 37: XTEM and PVTEM of the trapped dislocation loop at the GaAsP/SiGe interface.](image)

Because excessive point defect concentration at the interface leads to an increase in the threading dislocation density, minimizing their concentration or suppressing their formation should improve the material quality even further. From the previous

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experiment, strain is a viable parameter for affecting the interface quality. We therefore have 2 parameters: tension or compression at the interface on the film side, and tension or compression on the substrate side. The underlying Si_{1-x}Ge_x virtual substrate can be completed with a slightly strained layer after which GaAs_{y}P_{1-y} can be initiated with a strained layer. With the success in containing the dislocation loops from expanding, next attempts were made to suppress the loop nucleation entirely at the interface (Figure 39).

![Figure 39: Schematic of structures grown to test suppression of dislocation loop nucleation.](image)

In the second sample from the left in Figure 39, the tensile-compressive zone used in the loop trapping experiment was moved down to the interface. Plan view TEM data reveals that the threading dislocation density of the GaAs_{y}P_{1-y} film was equal to the threading dislocation density of the underlying Si_{1-x}Ge_x virtual substrate. Since the threading dislocation density did not increase at the heterovalent interface, the t-c zone has been shown to prevent dislocation nucleation. However the use of a c-t zone (compression on the Si_{1-x}Ge_x-side and tension on the GaAs_{y}P_{1-y}-side, first sample on the left in Figure 39)
at the interface resulted in dislocation nucleation at the interface and led to high TDD. This showed the importance of tensile layer existing under any compressive layer.

![Threading Dislocation Density (cm⁻²)](image)

**Figure 40:** TDD in GaAsP on SiGe with various strain conditions. Tensile strain at the heterovalent interface suppresses the formation of threading dislocations.

The last set of experiments (the two samples on the right in Figure 39) examined the necessity of the paired strain layer at the interface and if solely straining the Si₁₋ₓGeₓ layer under the GaAsₚ₁₋ᵧ was enough to suppress defect nucleation. Lattice matched GaAsₚ₁₋ᵧ was grown on Si₀.₃₅Ge₀.₆₅ virtual substrates that were terminated with either a tensile strained layer or a compressive layer. Additionally, a lattice matched GaAsₚ₁₋ᵧ on
unstrained Si$_{0.35}$Ge$_{0.65}$ sample and compressive-tensile structure were grown as control samples. Plan view TEM data reveals that tensile strain in only the Si$_{1-x}$Ge$_x$ virtual substrate yielded the best quality GaAs$_y$P$_{1-y}$ films—better than the previous best tensile-compressive zone sample and substantially better than a completely unstrained structure. The compressive strain capped Si$_{1-x}$Ge$_x$ virtual substrate exhibited a large increase in threading dislocation density, which reinforces our results that any compressive strain at the interface without a tensile layer leads to an increase in defect density. The results of the strain experiments are summarized in Figure 40.

5.3 Summary

Thus, with the experiments described herein, the use of initiating Si$_{1-x}$Ge$_x$ films with a short AsH$_3$ exposure, followed by the use of tensile layers near the heterovalent interface, resulted in the lowest threading dislocation densities in the GaAs$_y$P$_{1-y}$ films. All the results are summarized in Figure 41.
We have developed initiation and strain-engineering methods at the GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ heterovalent interface to prevent high defect densities in GaAs$_y$P$_{1-y}$/Si$_{1-x}$Ge$_x$ interface. The use of such invention will allow a plethora of III-V devices to be integrated on silicon substrates, such as multi-junction solar cells and visible In$_x$Ga$_{1-x}$P LEDs.
Chapter 6: GaAsP/Si dual-junction solar cells
6.1 GaAsP grading

High quality material, low resistance tunnel junction and minimal device fabrication losses are required to achieve the maximum efficiency from the GaAsP/Si dual-junction solar cell. Both the approaches to integrate the GaAs0.71P0.29 film on Si substrate have their own limitations. With the first approach of integrating GaP directly on Si, the buffer between GaAs0.71P0.29 and the Si sub-cells is ideal optically as it is transparent to the photons that have energies below the GaAsP bandgap and above the Si bandgap. But as had been described earlier, even though significant progress was made in achieving APD-free GaP films, the TDD remains relatively high to achieve high efficiency minority carrier devices. On the other hand, while GaAsP films of very low TDD were achieved via the second approach by using compositionally graded SiGe buffer. The SiGe graded buffer is going to absorb some of the light below 1.7eV, limiting the performance of the bottom Si cell.

This led us to explore a hybrid approach to achieve the dual-junction solar cell on Si. The direct band gaps of Si and Ge lie at 3.5eV and 0.805eV. Assuming linear variation of the direct band gaps from Si and Ge, it can be calculated that for a composition of Si0.35Ge0.65, the direct band gap will be at 1.75eV. So if the transition from SiGe to GaAsP is made at Si0.35Ge0.65 then the absorption of light in the graded buffer can be minimized. With the significant progress made in improving the GaAsP film quality on Si0.35Ge0.65 virtual substrate, a hybrid structure was designed such that lattice matched
GaAsP was deposited on $\text{Si}_{0.35}\text{Ge}_{0.65}$ followed by compositional grading to $\text{GaAs}_{0.71}\text{P}_{0.29}$, which will act as the top cell. The schematic of this structure is shown in Figure 42.

![Schematic of GaAsP integration of Si via hybrid approach.](image)

Figure 42: Schematic of the GaAsP integration of Si via hybrid approach.

This needs compressive compositional grading from $\text{GaAs}_{0.63}\text{P}_{0.37}$ to $\text{GaAs}_{0.71}\text{P}_{0.29}$, after the deposition of lattice matched GaAsP on $\text{Si}_{0.35}\text{Ge}_{0.65}$. As compared to tensile grading, compressive GaAsP relaxation is not subject to cracking or dislocation dissociation; therefore along with the absence of phase separation, extremely high grading rates can be employed with minimal deterioration of final film quality. The higher grading rates would be advantageous for future GaAsP/Si cell technologies since reduced epitaxial growth time and thickness addresses both cost and possible thermal strain issues.
To accommodate for the 0.32% strain between the two compositions of GaAsP, the compositional grading was done at 3 different grading rates (0.8%μm⁻¹, 1.2%μm⁻¹ and 1.6%μm⁻¹) at 725°C. Table 2 summarizes the TDD, calculated via PVTEM, obtained through various grading rates. The fastest grading rate resulted in the lowest dislocation density. Figure 43 shows the Nomarski images of the GaAsP films with compressive graded buffer. The samples with the highest defect density also shows deeper cross-hatch and higher surface roughness. XTEM image of the GaAsP with 1.6%μm⁻¹ grading rate confirms a clean GaAs₀.₇₁P₀.₂₉ cap layer (Figure 44). As this grading rate resulted in the lowest TDD, this rate was used to fabricate all the solar cells discussed in this thesis.

<table>
<thead>
<tr>
<th>Grading rate (%μm⁻¹)</th>
<th>TDD (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>1.81x10⁷</td>
</tr>
<tr>
<td>1.2</td>
<td>6.11x10⁶</td>
</tr>
<tr>
<td>1.6</td>
<td>3.01x10⁶</td>
</tr>
</tbody>
</table>

Table 2: TDD of GaAsP with respect to the grading rate of the compressively graded buffer.
Figure 43: Nomarski images of GaAsP films with compressive grading rates of (a) 0.8%\(\mu m^{-1}\), (b) 1.2%\(\mu m^{-1}\) and (c) 1.6%\(\mu m^{-1}\).

Figure 44: XTEM image of the GaAsP graded buffer with 1.6%\(\mu m^{-1}\) grading rate on SiGe virtual substrate. This image shows low defect density in the Ga\textsubscript{As}\textsubscript{0.71}P\textsubscript{0.29} cap layer.
6.2 Process and Testing

After the GaAsP grading optimization, device structures were fabricated for the optimization of the tunnel junction and the dual-junction solar cell. The samples were rinsed with acetone, methanol and isopropanol to clean the surface before starting the fabrication. The four main steps in the processing sequence are mesa formation, n- and p-type contact formation and metallization. Photolithography and anisotropic wet etching are used to isolate the tunnel junction structures into separate mesas. The key to successful photolithography is the use of a thick photoresist (AZ5214), required for adequate coverage over the device's vertical topography. The 1 µm thick resist is crucial for all three processing steps following mesa formation. The AZ5214 processing sequence was optimized for the present application; with HMDS deposited to eliminate resist adhesion problems. Evaporated and photolithographically patterned metal contacts were used for both the n- and p-type contact grids. Silicon dioxide film was deposited using an STS plasma enhanced chemical vapor deposition (PECVD) system, to act as a passivation layer and anti-reflection coating (ARC). This oxide layer was also used for photolithography and metal deposition. Buffered oxide etch (BOE) was used to etch the oxide for contact opening. Specific fabrication steps for the tunnel junction structures and the dual-junction solar cells will be discussed in the respective sections.

These devices were tested on a four-point probe station for dark I-V and an AM1.5G light source was used to measure the light I-V. The results and the device structures will be discussed in the following sections.
6.3 Tunnel Junction

The main goal of the tunnel junction is to provide a low electrical resistance and optically low-loss connection between two subcells. Without it, the p-doped region of the top cell would be directly connected with the n-doped region of the bottom cell. Hence, a p-n junction with opposite direction to the others would appear between the top cell and the middle cell. Consequently, the photovoltage would be lower than if there would be no parasitic diode. In order to decrease this effect, a tunnel junction is used. It is simply a wide band gap, highly doped diode. The high doping reduces the length of the depletion region. Hence, electrons can easily tunnel through the depletion region. The GaAsP and Si sub-cells can be connected in series epitaxially by using tunnel junction device layers as low resistance contacts between the cells. A tunnel junction requires sharply defined highly doped regions to allow tunneling. It is important to limit the diffusion of the doping layers so that the dopants don’t diffuse while continuing further epitaxy. This will not only smear out the sharp dopant profile that is required for tunneling but will also dope the neighboring region disrupting the type of doping required. Also, high incorporation of doping species \(10^{19}-10^{20} \text{ atoms cm}^{-3}\) is necessary for tunnel junctions. At the same time material degradation, due to higher concentration of doping species, should be limited.

The dopants usually used for achieving p-n junction in GaAsP films are Zn (p-type) and Si (n-type). These could be used for doping the tunnel junction as well. But the challenge
with Zn and Si is that their diffusivity is very high in GaAsP films. This disrupts the sharp doping profile and also diffuses the doping species to the neighboring regions. Therefore two precursor sources were added to the MOCVD system to get access to dopants that have low diffusivities in GaAsP and can lead to higher concentration of doping species. Bromotrichloromethane (BCCl₃) and diethyl-tellurium (DETe) were added to provide C (p-type) and Te (n-type) dopants.

The tunnel junction was grown after the GaAsP grading at GaAs₀.₇₁P₀.₂₉ to minimize the exposure time of the tunnel junction to higher temperatures. Since the GaAsP initiation on SiGe and GaAsP grading was done at 725°C under H₂ ambient, to avoid complicated growth structure, the initial tunnel junction structure was grown at the same temperature. H₂ ambient was used to get higher growth rate and lesser epitaxy duration to keep the exposure of the tunnel junction to a high temperature to a minimum. Figure 45 shows SIMS scans of Ga, As, P, Zn, Si, C and Te from the tunnel junction grown at 725°C in the GaAs₀.₇₁P₀.₂₉ film. This structure shows reasonable amount of Te incorporation in the film but the same wasn’t the case with the C incorporation. Also to note here is the Zn concentration is extremely high, this will be an issue once more material is deposited on top of the tunnel junction to create the top GaAsP subcell. Zn will start diffusing and will disrupt the doping profile in the neighboring region. It was also observed that the presence of C slows the growth rate of the GaAsP film, so for the future tunnel junction structures the growth time was increased for the C-doped film.
Dopants tend to get incorporated easily in higher concentrations at lower temperatures. So the similar tunnel junction structures were repeated at 650°C and 600°C to increase the C incorporation in the GaAsP films. Increased doping concentration of C in the GaAsP film was observed as the temperature was reduced. Figure 46 shows SIMS scans of As, P, Zn, Si, C and Te from the tunnel junction grown at 600°C in the GaAs\textsubscript{0.71}P\textsubscript{0.29} film. This sample shows higher concentrations of both C and Te in the GaAsP film, sufficient to create a tunnel junction. However, two issues with this sample were the high level of Zn doping that would make it difficult to achieve lower doping for creating the base of the top GaAsP subcell and the shift in the composition of the GaAsP film when it
was being doped by C. Through XRD it was verified that C incorporation in the GaAsP film creates a shift in the composition of the film by 9% atomic concentration, this mismatch in the composition generated defects at the tunnel junction. The higher doping of the film will be tackled by raising the temperature after the tunnel junction growth. The flow of AsH₃ and PH₃ were adjusted to accommodate the shift in the composition of the GaAsP caused by the C incorporation.

Figure 46: SIMS profile of GaAsP film grown at 600°C with a C-Te tunnel junction (highlighted).

Adjusting the composition in the C-doped region, the final tunnel junction structure was fabricated Figure 47. This tunnel junction when characterized electrically on the four-
point probe station showed negative resistance as expected out of a well functioning tunnel junction. The I-V curve is shown in Figure 48. With this success in achieving the tunnel junction dual-junction cells were fabricated and will be described in the next section.

Figure 47: Schematic of the fabricated tunnel junction device grown on the GaAsP film integrated on Si via SiGe graded buffer.
6.4 Dual-junction GaAsP/Si Solar Cells

After the optimization of the GaAsP graded buffer and the tunnel junction, to gain an early assessment of the photovoltaic potential for this materials system, a few first-generation, unoptimized GaAsP/Si dual-junction solar cells were fabricated. As mentioned in the previous section, the Zn doping was very high after the tunnel junction growth at 600°C, which won’t be suitable for the growth of the base of the top cell that will require lower doping values. To address that issue, the growth temperature was raised to 650°C. During this temperature raise the AsH₃ and PH₃ overpressure was continuously changed to avoid any surface undulation due to the exposed GaAsP surface.
as the As and P incorporation in the GaAsP film is dependent on the growth temperature. The thicknesses and doping for various parts of the solar cells were calculated and optimized through PC1D computer program in collaboration with Masdar Institute of Science and Technology.

![Figure 49: Schematic of the GaAsP/Si growth for the dual-junction solar cell.](image)

From the results of the dual-junction cell simulation, three cell structures were grown to evaluate the performance of the solar cells. Structure A didn’t have a window or a back surface field (BSF) layer. Structure B had an InGaP window layer but no BSF layer. Structure C had both an InGaP window layer and an AlGaAsP BSF layer. The thicknesses and doping of the fabricated structure C are shown in Figure 49. Everything, other than the presence of the window layer and the BSF layer, is identical in the
structures A, B and C. The growths were done on a p-type Si substrate using the methodology described in the previous chapters. As mentioned earlier the growth temperature for the top GaAsP cell was raised to lower the Zn incorporation in the film. This was verified through the SIMS analysis on structure A (Figure 50).

![Graph showing SIMS analysis](image)

Figure 50: SIMS analysis of the GaAsP subcell and tunnel junction grown on SiGe virtual substrate. Growth temperatures are indicated on the plot.

A clear drop in the Zn concentration is visible once the growth temperature was raised from 600°C to 650°C. It should be noted that both the tunnel junction and the GaAsP cell were grown under H₂ ambient to increase the growth rate. Other than the advantage of the lesser epitaxy growth time, it also keeps the contaminants low to prevent the possibility of unintentional doping. The tunnel junction dopant profiles still looked sharp after growing over a micron of III-V film on top of it. The emitter and the base of the top
GaAsP cell were doped with Si and Zn respectively. The surface was capped with a thin GaAs layer to provide an ohmic contact. The XTEM of the structure A shows the entire III-V film grown over the SiGe virtual substrate (Figure 51). There are some dislocations visible under the tunnel junction, which are due to the temperature variation and the transition from N$_2$ to H$_2$. However, the GaAsP cell is defect free in the pretty wide region shown in the XTEM image.

Figure 51: XTEM structure of structure A with GaAsP cell and the tunnel junction. This image also shows the different temperatures used for growing various segments of the solar cell.

Dual-junction cells were fabricated from all the three structures for device testing. The deposition of the Si cell was done in UHVCVD reactor, which deposits the junction on both the sides of the wafer. The junction from the back-side of the wafer was removed by manual grinding. 25 microns of material was removed which is sufficient to get rid of the
junction. The wafer was then rinsed with acetone, methanol and isopropanol. The front of the wafer, with the GaAsP cell was covered with the photoresist (AZ5214), so that it doesn’t get affected by the piranha and the HF clean, which was done to clean the back surface before the metal deposition. 200nm Al was deposited on the back of the wafer to form p-type contact. This deposition was done in Temescal FC-2000 Electron Beam Evaporator. This was followed by rapid thermal annealing at 300°C for 5 min to allow the Al to spike through Si using Heatpulse 410 Rapid Thermal Annealing. 80nm silicon dioxide was deposited on the front of the wafer serve as both the ARC and also provide passivation for the cells. After photolithography and buffered oxide etch, Ni/Ge/Au (10nm Ni, 25nm Ge and 100nm Au) was deposited to form the n-type top contact. The sample was then subjected to rapid thermal annealing at 450°C for 30 sec.

Figure 52: Schematic of the fabricated GaAsP/Si dual-junction cell.
Using this process flow dual-junction cells were fabricated from structures A, B and C. The cell area varied from $0.25 \text{cm}^2$ to $14 \text{cm}^2$. Dark and light $i-V$ measurements were then performed on these cells. Larger cells showed better performance because of the lesser perimeter to surface area ratio that prevents leakage in the cells. The $i-V$ curve for the structure A is shown in Figure 53. This shows a rectifying behavior with $1.22 \text{V} V_{oc}$, $1.7 \text{mA/cm}^2 J_{sc}$ and a fill factor of $29\%$.

![Figure 53: Dark and light current-voltage characteristics of an unoptimized GaAsP/Si dual-junction solar cell (structure A).](image)

Considering that these cells have not been optically optimized (non-optimal AR coating, metal shading losses and no light trapping) to simplify fabrication and subsequent analysis, the results achieved are quite reasonable, and are consistent with PC1D calculations. PC1D and some initial absorption modeling results predict that due to the
presence of a thick GaAsP layer and SiGe graded buffer, the Si cell is heavily shaded from the photons that should be reaching the Si cell. This limits the performance of the device as the dual-junction cell is series matched and the $J_{SC}$ will be limited by the worst-performing cell, which in this case is Si as it isn’t getting enough light. The indirect bandgap of the SiGe graded is absorbing the good portion of that due to the graded buffer being very thick. So these results are in good agreement with the predictions from modeling. Since the bottom subcell is heavily shaded, limiting the performance of the dual-junction cell, it was difficult to distinguish the effect of the presence of the window layer and the BSF layer in structures A, B and C. These were just some preliminary devices, there is a huge scope for improvement in the fabrication process as well. The I-V curve shows that cells are leaky, this could be because of the surface passivation issue. With the fabrication process optimized, optimized AR coating and contact optimization the cell performance can be improved, as it is not being limited by the material quality. Further optimization can be achieved by thinning the thickness of the SiGe graded buffer and also the GaAsP cell thickness to push the current up from the bottom Si cell.
Chapter 7: Conclusions and Future Research Directions
7.1 Summary of Experimental Results

This thesis has explored two different ways to integrate GaAsP thin films on Si substrate to realize the feasibility of a two-cell tandem structure using silicon as both the substrate and lower cell and GaAsP as the upper cell. This work has made several advancements in this area that bring the goal of monolithic integration at a commercial level many steps closer to realization. This work, which has demonstrated the ability to suppress antiphase disorder and stacking fault formation and to fabricate low TDD of GaAsP/GeSi/Si, removes two fundamental materials obstacles to the monolithic integration of III-V materials and devices on Si.

Through a combination of MOCVD, ALD and MBE deposition techniques, the understanding of GaP/Si interface was further improved. This interface historically has proved to be very hard to control despite being very similar to GaAs/Ge. Through the use of SiGe graded buffers, the Si lattice constant was increased to that of Si$_{0.88}$Ge$_{0.12}$, which is lattice-matched to GaP. Migration enhanced epitaxy and lower growth temperatures helped realize antiphase domain free and low TDD GaP films on Si substrate. The TDD obtained through this route was the lowest for this material system reported so far.

The other route for fabricating the high efficiency dual-junction solar cells was through a combination of SiGe and GaAsP compositionally graded buffers be used to create a platform for GaAsP on Si. In order to achieve this goal, it was required to develop a process for lattice-matched growth of GaAsP on SiGe virtual substrates. Various
processes for lattice-matched GaAsP growth on SiGe virtual substrates were explored, using the understanding of the GaAs /Ge interface as a starting point. These results showed that the growth process was highly dependent on Ge content of the SiGe virtual substrate, growth temperature, and surface treatment of the SiGe virtual substrate immediately before growth. GaAsP material quality was generally found to be improved with increasing Ge content of the SiGe virtual substrate, increased growth temperature, and minimization of the air exposure of the SiGe virtual substrate prior to growth of the GaAsP layer. Using these optimizations, specular GaAsP layers with low surface roughness and no observed twin boundaries or stacking faults levels were grown on Si$_{0.5}$Ge$_{0.5}$, Si$_{0.4}$Ge$_{0.6}$ and Si$_{0.3}$Ge$_{0.7}$ virtual substrates.

The dislocation nucleation mechanism under lattice-matched conditions was explored at the GaAsP/SiGe heterovalent interface. Through the optimization of the initiation conditions and intentional strain at the interface, the dislocation nucleation at the interface was controlled and completely suppressed. This provided GaAsP films with very low TDD (~1x10$^6$ cm$^{-2}$), equal to the underlying SiGe virtual substrate's TDD. Through this technique a robust GaAsP/SiGe platform was established that is viable for minority carrier devices on Si such as high efficiency dual-junction solar cells and visible LEDs.

Further optimization in GaAsP grading was done to access a dual-junction solar cell on Si substrate. This was followed by the successful demonstration of a tunnel junction structure in the GaAsP film, which is required to provide a low resistance connection
between the Si and GaAsP subcells. Prototype dual-junction GaAsP/Si solar cell devices were fabricated and tested. They show good preliminary performance characteristics and offer great promise for future devices integrated with the newly developed high quality GaAsP/Si virtual substrates.

7.2 Future Research Directions

Numerous applications exist for GaAsP/SiGe/Si heteroepitaxy, each of which faces its own unique challenges beyond the mere suppression of antiphase disorder and TDD. To build on the preliminary device work presented in this thesis, it is necessary to further optimize processing and device design of the dual-junction solar cell. One exciting aspect of multijunction cell development is that there are still many possibilities to explore. The challenge is to achieve the necessary quality in a configuration that makes optimal use of each material. Optimized AR coating, contact chemistry, metallization and surface passivation will definitely improve the device performance. As is visible from the device results is that the bottom Si cell is not getting enough photons, so thinning the graded buffer layer and the top GaAsP cell will boost the current coming from the bottom cell. Design parameters such as doping and thickness of various layers can be improved further. Current matching can be achieved by optimizing the thickness of each cell so that the proper numbers of photons are absorbed and collected in each sub-cell.

Another idea for the future work is to layer transfer the high quality GaAsP film grown over SiGe virtual substrates over Si substrates. This can be achieved through wafer
bonding the GaAsP films and the Si wafer. Through this approach GaAsP cell can be integrated directly over the Si cell, removing any graded buffer in between the two subcells. This will prevent any losses due to the absorption of the photons in the graded buffer, which will improve the efficiency of dual-junction solar cells. Once the GaAsP layers are transferred, the underlying SiGe virtual substrate can be reused for the deposition of GaAsP films, reducing the cost of the whole process. The economic viability and competitiveness of multijunction solar cell systems will continue to improve over time. Process technologies, particularly techniques with commercial scalability, can be expected to progress, as will designers' understanding of materials behavior. As mentioned earlier, this high quality GaAsP/SiGe platform also gives access to the visible spectrum of the light providing the opportunity to build LEDs on Si substrates.
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