New Architecture for USB Powered Battery Charger

by

Hao (Steven) Zhou

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Engineering in Electric Engineering

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Abstract

The goal of this project is to design and simulate a new architecture for a USB-powered battery charger chip. The chip is designed to be able to deliver constant-current/constant-voltage charge regulation to the battery when ample power is available. The total power to the chip must also meet the specification of the USB port. The chip is also required to operate at an output voltage greater than 3.6V no matter how low the battery voltage discharges to, unless the load is so large such that the battery is required to supply additional current to the load. Furthermore, this new architecture is designed with improvements in both the charging efficiency as well as USB current limit violation time.

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Title: Associate Professor

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Title: Design Engineer
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Chapter 1

Introduction

The goal of this Master of Engineering thesis is to design, model, and simulate a new architecture for a battery charger powered by a Universal Serial Bus (USB).

1.1 Motivation For Project

Over the past decade, there has been a drastic increase in the number of portable devices ranging from cell phones to palm pilots to portable media players. These devices are often powered by a rechargeable battery cell that is required to be recharged on a regular basis. In the past, most of the charging has been done via wall outlets; however over the past few years, more and more of these portable devices have transitioned to using USB ports as a means to recharge their batteries. The most notable of these devices are the portable media players that often need to be connected to a computer in order for media files to be transferred. However, unlike drawing current from a wall outlet, there is a specification that limits the amount of average current that can be drawn from a USB port. In addition, in order to safely charge these batteries without the risk of damaging the cells, it is usually common practice to employ a constant current-charging algorithm while charging along with a constant voltage algorithm once the battery voltage reaches a specified voltage level. Thus, a power management integrated circuit (PMIC) is required to ensure the proper charging without violating the USB specifications.
1.2 Old Architecture

PMICs that regulate battery charging via the USB port are not a novel idea in the analog industry. One way such PMICs are designed is through the use of a linear regulator. In this topology, the battery is connected to a source voltage through a power MOSFET. The gate of that transistor is then controlled through error amplifiers that insure the accurate constant current and constant voltage charging behavior of the charger. Figure 1-1 depicts a part of the block diagram of the LTC 4061 that demonstrates the power path of the charger of the 4061.[1]

![Diagram of the power path of the LTC4061 charger](image)

Figure 1-1: Power path of the LTC4061 charger

The $R_{PROG}$ resistor can be used to set the level of the constant current into the battery, and the gate voltage of the transistors is adjusted depending on the $R_{PROG}$ resistor and the battery voltage. When the battery voltage goes up, the gate voltage goes down, so that the FET drain-source voltage decreases such that the same current flows through the battery. Similarly on the constant voltage side, as the battery voltage approaches the float voltage, the gate voltage of the FET increases such that
constant voltage is maintained across the battery.

The main disadvantage of this topology is efficiency. When the battery voltage is low, the charge transistor has a large voltage drop and a lot of power is dissipated in it. Suppose the user wants to charge the battery at 500mA, \( V_{cc} \) is at 5V, and the battery voltage is at 3V, then essentially 40 percent of the power is lost in the power FET. Furthermore, the previous architecture acted solely as a charger as input power is transferred to the battery, and since the battery could be at any voltage during the charging cycle it could not be used to power external loads. In the new topology, the output and battery nodes are separated by a transistor, and thus the output node can be controlled independently to regulate at a certain voltage and supply power to the external load.

Although there are various different architectures that employ the idea of linear chargers, all of them share the same problems of lack of efficiency. Due to this, architectures for switching regulators were designed. One example of such architecture is the LTC4088, whose block diagram is shown in figure 1-2.[2]

![Block diagram for the LTC4088](image)

**Figure 1-2: Block diagram for the LTC4088**

The LTC4088 has two main blocks. The first block is essentially a buck converter that regulates output voltage, \( V_{out} \), at 300mV above the battery voltage. The reason
why it is 300mV is somewhat arbitrary, but it’s more or less due to the on resistance of the charge FET connecting $V_{out}$ and BAT pins, as well as the maximum programmable current through that FET. The second block of the charger is the constant-current, constant-voltage regulator, which essentially acts the same way as it did before in the linear charger. As noted, one of the main advantages of this architecture is the fact that the voltage across the charge FET is now fixed at 300mV, which is a huge improvement over the linear charger, and the efficiency is drastically improved. However, one point to note with this architecture is that the output voltage can not drop below a threshold voltage, in this case 3.6V, no matter what the battery voltage falls to. The reason for this lower-bound (deck) threshold voltage is so that the system load, which is powered by $V_{out}$, will still be operational regardless of what the battery voltage is. Thus, in the case that the battery is discharged to extremely low voltages, there is again a significant percentage of power that is dissipated through the charge FET; however it is still a lot more efficient than in the case of the linear charger. Table 1-1 demonstrates the percent input power loss through the charge FET with varying battery voltages with a 500mA programmed current.

<table>
<thead>
<tr>
<th>Battery Voltage (V)</th>
<th>Linear Charger Percent Input Power Loss in Charge FET</th>
<th>Switching Charger Percent Input Power Loss in Charge FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>50%</td>
<td>31%</td>
</tr>
<tr>
<td>3.0</td>
<td>40%</td>
<td>17%</td>
</tr>
<tr>
<td>2.3</td>
<td>34%</td>
<td>8%</td>
</tr>
<tr>
<td>2.6</td>
<td>26%</td>
<td>8%</td>
</tr>
<tr>
<td>2.9</td>
<td>22%</td>
<td>7%</td>
</tr>
</tbody>
</table>

Table 1.1: Percent input power loss through charge FET with 0.5A charge current

Even though this topology significantly improves the efficiency of the charger, there is still some room for improvement, especially since the 300mV difference between $V_{out}$ and BAT pins is more than what is nowhere near necessary if the programmed charge current is set at relatively low values. This issue concerning efficiency is one of the improvements in the new architecture.
1.3 New Architecture

The new architecture, whose block diagram is shown in figure 1-3, incorporates in its design two significant improvements over its predecessors. As mentioned before, one area of improvement in the new architecture is in its charging efficiency. The way such a task can be accomplished is by connecting the gate of the charge FET to ground thus connecting the $V_{out}$ and BAT pins so that the power dissipated through that FET is at a minimum, no matter what the level of charge current the charger is programmed for. However, by doing so, the $V_{out}$ and BAT pins are essentially tied to each other via the small on-resistance of the charge FET. However, as the battery voltage drops below the threshold voltage, the gate voltage of the charge FET can no longer be grounded, and must be set such that the voltage at the $V_{out}$ pin is set to the threshold voltage. Essentially, the major improvement here is that when the Battery voltage is above 3.6 Volts, the 300mV differential that was present in the LTC 4088 is no longer required.

![Block diagram for new architecture](image)

Figure 1-3: Block diagram for new architecture

The second major improvement in the new architecture is the lowering of USB current limit violation time during a transient step on the load. When the user
pulls a transient step, it takes a while before the input current limit loop servos into regulation. In that period of time, the current being pulled from the USB port may exceed the 500mA limit that is specified by the USB port. During this transient, the excess current that the charger demands is pulled from a 120μF capacitor inside the USB port. Due to this, the longer the violation time, the lower the voltage at the output of the USB port becomes. Thus, that violation time needs to be as low as possible. Significant improvement was made in the design of the new architecture to decrease the USB current limit violation time.

1.4 Organization

Chapter 2 describes the gate drive design for the switchers in order to size the switch transistors. Chapter 3 delves into the analysis of the dynamic behavior of a buck regulator and also discusses the circuitry required to stabilize average inductor current control. Chapter 4 depicts an error analysis for the average input current and average inductor current. Furthermore, after the analysis for average current control along with the error analysis, chapters 5 through 7 will analyze the design of circuitry to stabilize the three loops of constant input current limit, constant battery current control, and constant battery voltage control. Lastly, chapter 9 will tie the three control loops together and demonstrate how the loops interact with each other to achieve the proper behavior of the battery charger.
Chapter 2

Gate Drive Design

2.1 Gate Drive Logic

Figure 2-1: Model for the power stage

Figure 2-1 depicts the model for the power stage. Q1 is the gate voltage of the PMOS, and Q2 is the gate voltage of the NMOS. The diodes depicted represent the body diodes of the two switches. A non-overlapping gate control topology was used in this architecture. Essentially, in this topology the PMOS and NMOS are never on at the same time. Thus, logic is required to ensure that when the Q1 goes low, Q2 is already low, and also when Q2 goes high, Q1 is also already high.

The logic of the gate drive circuitry is depicted in Figure 2-2. The SWON signal goes high to set the PMOS switch on, and goes low to turn the PMOS switch off. As can be noted, when the SWON signal goes high, the NGATE voltage goes low, thus shutting off the NMOS, and only when the NMOS is completely shut off does the
PGATE voltage start too fall, thus turning on the PMOS. When the SWON signal goes low, the PGATE voltage goes high first, thus shutting off the PMOS. Once the PMOS is completely shut off, the NGATE voltage starts to rise, which turns on the NMOS. Conversely, when the SWON node goes low, the PGATE node goes high first, thus shutting off the PMOS; and only when the PMOS shuts off does the NGATE voltage start to go high, thus turning on the NMOS switch.

\[ \text{SWON} \rightarrow \text{PGATE} \rightarrow \text{NGATE} \]

Figure 2-2: Logic for gate drive

### 2.2 Sizing the Switching Transistors

In order to correctly size the switching transistors, an analysis of power loss of these transistors needs to be completed. There are three main sources of power loss: conduction loss, switching loss, and capacitance loss. Conduction loss is lower with a higher W/L ratio of the transistor due to the lowering of the transistor’s on-resistance. Capacitive loss is a result of charging and discharging of transistor capacitances, thus the smaller the devices, the less capacitance is present. In order to use the smallest possible size of the transistors, a minimum value for the length should be used. Thus, given the available 0.6um CMOS process, the length of the switching transistors should be set to 0.6um. However, taking electrostatic discharge (ESD) into consideration, the NMOS switcher needs to be doped with an ESD layer which is roughly 0.3um in width. Thus, the length of the NMOS switcher needs to be 0.9um.

The power loss in the switches is analyzed through one switch cycle. Since the switcher is typically programmed to run from 500mA to 1.5A of current through
the inductor, we will assume for analysis sake that an average current of 0.75A is being used and that the current does not vary significantly within a switching cycle. Furthermore, since the buck converter intends to step down 5V at Vin to anywhere between 3.6V to 4.2V at V_out, we will assume a duty ratio, D, of 0.8 for this analysis. In addition, the switching frequency, f_sw, for this application is 2.25MHz.

2.2.1 Case 1: Conduction Stage

During this stage, one of the switches is fully on while the other is fully off. All of the inductor current flows through the on switch, which essentially behaves like a resistive device with some small on-resistance. Thus, the power loss in this stage is dominated by conduction loss through the on switch. Figure 2-3 depicts the behavior of the switch when the PMOS is fully on, and the NMOS is shut off.

![Figure 2-3: Behavior of the switcher when the PMOS switch is fully on](image)

In this case the total energy lost in one cycle in this stage is equal to:

\[ U_{\text{diss}} = D \times T_{\text{sw}} \times I_L^2 \times R_{\text{dsp}} = 2 \times 10^{-7} \times R_{\text{dsp}} \]  \hspace{1cm} (2.1)

2.2.2 Case 2: PMOS turn off stage

When the gate of the PMOS switch goes high, the switch pin voltage starts to fall rapidly through the discharge of capacitor, \( C_u \), shown in figure 2-4. Once the voltage at the \( V_{\text{sw}} \) node falls to a diode drop below ground, the body diode of the NMOS turns on and the current through the PMOS, \( I_p \), goes to zero. However, during that
transition, there is switching loss through the PMOS due to the non-zero $I_p*(V_{in} - V_{sw})$ product.

Once the body diode of the PMOS turns on, there is conduction loss through the diode. However, since the diode is really on for a really small percentage of one cycle, that loss can be ignored. Lastly, the NMOS switch turn on to complete the switching period. Figure 2-4 demonstrates the different steps in the switching transition when the PMOS turns off, neglecting overlap time.

Even though this switching loss can be significant, the dominant power loss of this stage can be attributed to the gate drive capacitive loss of the two switches. Thus, the power dissipated in one of these switches in one transition is equal to what's shown in equation 2.2 under the assumption that the gate capacitance is linear and is being charged to $V_{in}$.

$$U_{diss} = Q_g * V_{gate} \approx \frac{1}{2} * C_{n,p} * V_{in}^2$$ (2.2)

2.2.3 Case 3: PMOS turn on stage

When the PMOS switch is turning on, the NMOS needs to be turned off first, the inductor current again flows through the body diode of the NMOS. Once the gate of the PMOS goes low, current begins to flow through the PMOS, and the voltage at the switch node rises. Again, there is switching loss due to the nonzero $I*V$ product across the switches but this loss is dominated by the power loss in the charging and discharging of the gate capacitors.

2.2.4 Power Loss Analysis

The goal in sizing the transistors is to minimize the power dissipated in a cycle. The bigger the devices, the larger the gate capacitances and smaller the on-resistance, which increases capacitive loss but lowers conduction loss.

The total per cycle power loss in a PMOS is equal to, given $L = 0.6 \mu m$: 

26
Figure 2-4: Transition for PMOS switch turning off

\[ U_{diss} = D \cdot T_{sw} \cdot I_{L}^2 \cdot R_{dss} + \frac{1}{2} \cdot C_p \cdot V_{in}^2 \]  
(2.3)

\[ = 2 \cdot 10^{-7} \cdot R_{dss} + 17.5 \cdot C_p \]  
(2.4)

\[ = 2 \cdot 10^{-7} \cdot \frac{L}{W} + 17.5 \cdot C_{op} \cdot W \cdot L \]  
(2.5)

\[ = 2 \cdot 10^{-7} \cdot \frac{5.17 \cdot 10^4 \cdot 0.6}{W} + 17.5 \cdot 2.5 \cdot 10^{-15} \cdot W \cdot 0.6 \]  
(2.6)

\[ = \frac{1.55 \cdot 10^{-3}}{W} + 2.625 \cdot 10^{-14} \cdot W \]  
(2.7)

For maximum efficiency, by setting the derivative to be equal to zero, \( W = \)
Due to the on-chip size constraints for both switches as well as the other sources of power loss such as the power loss through the body diodes of the transistors during switching, which increases with size and was not accounted for in my first-order analysis, I decided to size my PMOS to be 160,000/0.6, and my NMOS to be 60,000/0.9.
Chapter 3

Dynamic Behavior of Buck Converter

Before designing the control system, a dynamic model of the buck converter must be formulated. This can be done by analyzing the average model of the buck converter.[3] This model essentially analyzes the average behavior over one cycle of the converter, and is used to determine the transfer function relating small signal perturbations between state variables such as duty cycle, $d$, output voltage, $\bar{V}_{out}$, inductor current, $\bar{i}_L$, etc. The simplified circuit formulation of a synchronous buck regulator is shown in figure 3-1.

![Diagram of a synchronous switch buck converter](image)

Figure 3-1: Model for a synchronous switch buck converter

Assuming that $q(t)$ is 1 when the PMOS switch is closed, and a 0 when the switch is open, the time domain equations that represent the behavior of the buck converter are formulated in equations 3.1 and 3.2.
\[ C_{\text{out}} \frac{\partial v_{\text{OUT}}}{\partial t} = i_C = i_L - i_R = i_L - \frac{v_{\text{OUT}}}{R_{\text{out}}} \quad (3.1) \]

\[ L \frac{\partial i_L}{\partial t} = (v_{\text{IN}} - v_{\text{OUT}}) \ast q(t) - v_{\text{OUT}} \ast (1 - q(t)) \quad (3.2) \]

Assuming that the local average of a variable is defined as \( \bar{x}(t) = \frac{1}{T} \int_{t-T}^{t} x(\tau)d\tau \), and duty ratio as \( d(t) \). The state equation of the average output voltage and inductor current simplifies to:

\[ C_{\text{out}} \frac{\partial v_{\text{OUT}}}{\partial t} = i_L(t) - \frac{v_{\text{OUT}}(t)}{R_{\text{out}}} \quad (3.3) \]

\[ L \frac{\partial i_L}{\partial t} = v_{\text{IN}}(t) \ast q(t) - \bar{v}_{\text{OUT}}(t) \approx v_{\text{IN}}(t) \ast \bar{q}(t) - \bar{v}_{\text{OUT}}(t) \]

\[ = d(t) \ast v_{\text{IN}}(t) - v_{\text{OUT}}(t) \quad (3.4) \]

The approximation can be made due to the fact that \( v_{\text{IN}}(t) \) and \( i_L(t) \) have small ripples and their average values do not vary rapidly. Given equations 3.3 and 3.4, we can now analyze the small signal behavior of the buck converter by substituting the variables with its DC and small signal components, i.e. \( \bar{v}_{\text{IN}}(t) = V_{\text{IN}}(t) + \bar{v}_{\text{in}}(t), d(t) = D(t) + \bar{d}(t), i_L(t) = I_L(t) + \bar{i}_L(t), \) and \( v_{\text{OUT}}(t) = V_{\text{OUT}}(t) + \bar{v}_{\text{out}}(t) \). Doing so, we get,

\[ C_{\text{out}} \left( \frac{\partial \bar{v}_{\text{OUT}}(t)}{\partial t} + \frac{\partial V_{\text{OUT}}(t)}{\partial t} \right) = I_L(t) + \bar{i}(t) - \frac{V_{\text{OUT}}(t) + \bar{v}_{\text{out}}(t)}{R_{\text{out}}} \quad (3.5) \]

\[ L \left( \frac{\partial I_L(t)}{\partial t} + \frac{\partial \bar{i}_L(t)}{\partial t} \right) = (D(t) + \bar{d}(t)) (V_{\text{IN}}(t) + \bar{v}_{\text{in}}(t)) - (V_{\text{OUT}}(t) + \bar{v}_{\text{out}}(t)) \quad (3.6) \]

Due to the small perturbations in the small signal terms, we can ignore their second order effects, thus equations 3.5 and 3.6 can be simplified to: [3]
\[
C_{\text{out}} \frac{\partial \tilde{V}_{\text{OUT}}(t)}{\partial t} + C_{\text{out}} \frac{\partial V_{\text{OUT}}(t)}{\partial t} = I_L(t) + \frac{\tilde{v}_{\text{out}}(t)}{R_{\text{out}}} - \frac{V_{\text{OUT}}(t)}{R_{\text{out}}} 
\]

(3.7)

\[
L \frac{\partial I_L(t)}{\partial t} + L \frac{\partial \tilde{i}_{\text{in}}(t)}{\partial t} = D(t) * V_{IN}(t) + D(t) * \tilde{v}_{\text{in}}(t) + \tilde{d}(t) * V_{IN}(t) - V_{\text{OUT}}(t) - \tilde{v}_{\text{out}}(t) 
\]

(3.8)

We can then subtract out the DC portions of the signal from equations 3.7 and 3.8 to get the small signal response of the buck converter. Doing this, and assuming that there is sufficient filtering at the input such that \( \tilde{v}_{\text{in}}(t) = 0 \), we get:

\[
C_{\text{out}} \frac{\partial \tilde{V}_{\text{OUT}}(t)}{\partial t} = \tilde{I}_L(t) - \frac{\tilde{v}_{\text{out}}(t)}{R_{\text{out}}}. 
\]

(3.9)

\[
L \frac{\partial \tilde{I}_{\text{in}}(t)}{\partial t} = \tilde{d}(t) * V_{IN} - \tilde{v}_{\text{out}}(t). 
\]

(3.10)

Taking the first derivative of equation 3.9 and substituting it into equation 3.10, we get:

\[
L C_{\text{out}} \frac{\partial^2 \tilde{V}_{\text{OUT}}(t)}{\partial t^2} + \frac{L}{R} \frac{\partial \tilde{V}_{\text{OUT}}(t)}{\partial t} + \tilde{v}_{\text{out}}(t) = \tilde{d}(t) * V_{IN}(t) 
\]

(3.11)

Taking the Laplace transform of equation 3.11 and simplifying, we get a frequency domain response of the output voltage to the duty ratio, shown in equation 3.12.

\[
\frac{V_{\text{out}}(s)}{D(s)} = \frac{V_{\text{IN}}}{L C_{\text{out}} s^2 + \frac{L}{R_{\text{out}}}}. 
\]

(3.12)

Using equations 3.9 and 3.10, we can also formulate a block diagram for the dynamic behavior of the buck converter shown in figure 3-2.

Given the block diagram, the transfer function from \( D(s) \) to \( I_L(s) \) can be easily derived, and is shown in equation 3.13.
Figure 3-2: Block diagram for the dynamic behavior of the buck converter

\[
\frac{I_I(s)}{D(s)} = \frac{V_{IN} \cdot \frac{1}{sL}}{1 + \frac{1}{sL} \cdot \frac{R_{out}}{1 + sR_{out}C_{out}}} = \frac{V_{IN} \cdot (1 + sR_{out}C_{out})}{s^2 L R_{out}C_{out} + sL + R_{out}}
\]  

Equation 3.12 shows that the transfer function from duty ratio to output voltage has a double pole due to the LC tank, and given variable values of load resistance and capacitance, it becomes difficult to compensate. Thus, it is not a great idea to use voltage control to stabilize the behavior of the buck converter. However, from equation 3.13, we can conclude that there is a double pole and single zero in the transfer function from duty ratio to inductor current. This makes compensating the system a lot more manageable. This equation becomes extremely useful in determining the compensation required to stabilize the average current control loop described in section 3.1, as well as the compensation required to stabilize the three outer loops as described in chapters 5 through 7.

3.1 Analysis of Average Current Control

3.1.1 Reason for Average Current Control

Due to the dynamic behavior of the buck converter shown in equations 3.9 and 3.10, current mode control was selected instead of voltage mode control.\[4\] Current control has the benefit of the extra zero it adds to the transfer function from duty ratio to the control signal. Furthermore, in order to eliminate slope compensation problems that arise with peak current mode control, average current mode control was selected.
3.1.2 Stabilizing Average Current Control

Figure 3-3 depicts the block diagram for the average current control loop. \( \tilde{v}_c \) is defined as the command inductor current, and \( \tilde{i}_{out} \) be the actual inductor current. \( H(s) \) is defined to be \( \frac{V_{IN} \cdot (1 + sR_{out}C_{out})}{s^2L_{out}C_{out} + sL + R_{out}} \) (equation 3.13). \( G_{acc}(s) \) represents the transfer function from the error signal (between the command inductor current and the actual inductor current) to the voltage signal controlling the duty cycle of the buck converter. Dividing that signal by the peak voltage, \( V_m \), of the ramp signal determines the duty cycle. \( G_{acc}(s) \) can be implemented using some amplification stage to minimize error along with the correct internal compensation network to ensure loop stability. The actual circuit implementation of this stage will be discussed later in this section, but before doing so, analysis of the poles and zeros of the \( H(s) \) function must be carried out.

The frequency response of the average current control loop needs to cross over with reasonable phase margin at a frequency below a quarter the switching frequency in order for the average circuit model calculations to remain valid. With the switching frequency of this application being 2.25Mhz, the frequency response of the loop gain needs to crossover before roughly 600KHz for all modes of operation and all load conditions.

Analysis of \( H(s) \)

\[
H(s) = \frac{V_{IN} \cdot (1 + sR_{out}C_{out})}{s^2L_{out}C_{out} + sL + R_{out}}, \quad \text{and it has a zero at} \quad \frac{1}{R_{out}C_{out}}, \quad \text{and two poles that have a geometric mean of} \quad \frac{1}{\sqrt{LC_{out}}}.
\]
This means that at high frequencies, there is a fixed level of attenuation, with 20dB/dec roll-off. Thus, at the desired crossover frequency of 600 KHz, the gain from the zero will be roughly \(600Khz \times 2\pi \times R_{out} \times C_{out}\) and the attenuation from the two poles will be roughly \(\left(600Khz \times 2\pi \times \sqrt{L \times C_{out}}\right)^2\).

Thus, the total gain at 600 KHz due to \(H(s)\) is approximately equal to

\[
\frac{V_{in}}{R_{out}} \times \frac{600Khz \times 2\pi \times R_{out} \times C_{out}}{(600Khz \times 2\pi \times \sqrt{L \times C_{out}})^2} = \frac{V_{in}}{R_{out}} \times \frac{R_{out}}{600Khz \times 2\pi \times L}
\]

\[(3.14)\]

Since the battery charger is powered by the USB port, \(V_{in}\) is equal to 5 volts, and typical battery chargers in industry use an inductor size of 3.3uH. With these numbers, it can be calculated that \(H(s)|_{s=2\pi \times 600KHz} \approx 0.4\)

**Analysis of \(G_{acc}(s)\)**

In order to cross over at 600 KHz, \(G_{acc}(s)\) needs to have a gain of approximately 6 at 600 KHz for \(V_{in} = 2.5V\). \(V_{in}\) was chosen to be 2.5V because it allows for 100% duty ratio and it is high enough so that the \(V_{duty}\) value has a sufficient dynamic range. \(G_{acc}(s)\) also can't contribute too much negative phase around the crossover frequency due to the fact that there is already a pole in the system from \(H(s)\) that contributes -90 degrees of phase. Thus, a feasible implementation for \(G_{acc}(s)\) would be to use pole-zero compensation at the output of a high gain GM-Amp. Implementing this technique will allow for a constant gain around the crossover frequency without the addition of too much negative phase. As seen in appendix A, the amplifier was designed using the principles of a current mirror amplifier with a pole-zero-pole compensation at the output. The resistor R1 sets the high frequency gain of the amplifier around the crossover frequency of the average current control loop. In appendix A, Figure A-1 shows the circuit implementation, and figure A-2 demonstrates the frequency response of the amplifier. It can be seen that at the frequency around crossover, the gain of the amplifier is roughly 12dBs with very little negative phase, which is the desired behavior. The means for measuring the current and for implementing the current control are described in the next chapter.
Chapter 4

Analysis of Integrate and Hold Technique

4.1 Motivation

A integrate and hold circuit is useful in tracking the average of the input voltage when the input is connected and holding that average when the input is disconnected.[5] Such a technique is extremely useful in measuring the input current as well as the inductor current. In measuring both the input current and inductor current, the average SW node voltage when the PMOS switch is on needs to be first determined. Once found, the inductor current is equal to the supply voltage minus the average high-side SW node voltage divided by the on-resistance of the PMOS switch. The input current is then equal to the inductor current multiplied by the duty ratio. The sample and integrate circuit shown in figure 4-1 demonstrates how the average high-side SW node voltage can be calculated. When the PMOS switch is on, transistor MP2 is turned on and the voltage on the SWAVG node is integrating to the correct value through the RC network. When the PMOS switch is off, MP2 is turned off and the voltage at the SWAVG node is held. Transistor MP4 is added to reduce the error of the sample and integrate circuit by sinking the gate charge from MP2 as MP2 shuts off, thus reducing the parasitic charge flow into the capacitor during transitions.
4.2 Implementation of Sample and Integrate

Even though the sample and integrate technique is used in both measuring the input current and inductor current, there is a significant difference between the two. The reason for this is because the input current switches to zero as the PMOS switch is turned off, thus making the current discontinuous, whereas the current through the inductor remains continuous.

4.2.1 Input Current Measurement

Figure 4-2 demonstrates the implementation for input current measurement. MP1 and MN1 are the power switches for the buck converter. The SW node is a pulsing signal that goes roughly between ground and VBUS every switching cycle. $V_{GSH}$ is the control signal for the switch that connects the SW node to the RC network.
when MP1 is on. The reason for the input current measurement circuit is to extract out the average voltage on the SW node when the SW node is high, and hold that average value when the SW node is low. That average voltage then servos the drain voltage of MP2 through a high gain amplifier. Furthermore, MP2 is sized to be a ratio, $\alpha$, times smaller than MP1, thus the current flowing through the sense FET (MP2) is approximately $\alpha$ times smaller than the average current flowing through MP1, when the SW node is high. The value for $\alpha$ is set depending on whether or not the input current regulation is .1 amp, .5 amp, or 1 amp. In .1 amp mode, the input signal TENTHAMP is high and ONEAMP is low and $\alpha$ is set to be 200; in .5 amp mode, both the input signals are low and $\alpha$ is set to be 1000; and lastly, in the 1 amp mode, the signal TENTHAMP is low and ONEAMP is high, and $\alpha$ is set to be 2000. The reason for the variable ratio in the three different mode of operation is because the voltage at the VCLPROG node will be servoed to be 1.2V while the loop is in regulation with a fixed RC network at the VCLPROG node. Lastly, the VSAMPLE signal controls the switch between the drain of MP3 and the RC network, and only connects the two when MP1 is high. This modulates the measured current by the duty ratio, $d$, thus the input to the negative terminal of the OPAMP does not fluctuate rapidly. Doing so ensures a fairly accurate measurement of the input current.

4.2.2 Average Inductor Current Measurement

Figure 4-3 depicts the circuit representation of the average inductor current measurement. This circuitry is somewhat similar to the average input current circuitry in that it still attempts to find the average voltage of the SW node when the SW node is high. It also servos that average voltage onto the drain of MP2. However, in this case, MP2 is sized to be exactly one thousand times smaller than MP1. Thus, the current through MP2 is roughly one thousand times smaller than the current flowing through the inductor. That sense current is then amplified through a 1K$\Omega$ resistor in order to extract out the average inductor current in terms of a voltage, which can then be used in stabilizing the average current loop.
4.3 Error Analysis

The bigger the RC time constant in the sample and integrate circuit, the more precisely the input signal can be tracked. However, the RC product can’t be too large because it adds an extra pole in the frequency response. Thus, R was picked to be 11667Ω and C to be 20pF, which results in a pole beyond the crossover frequency of the loop. Unfortunately, this leads to significant error in tracking the average input current. Ideally, the exact average voltage of the SW node when the SW node is high can be extracted. However, as the RC product decreases, the averaging node, between the resistor and the capacitor actually tries to track the slope of the SW node more and more. Thus even though there is no cumulative error during the sampling phase, the error during the hold phase is drastically increased as the RC product decreases. This behavior is demonstrated in MATLAB simulations shown in figures 4-4 and 4-5. The error is analyzed under varying RC products, average inductor currents, and duty ratios, and is depicted in table 4-1. The percent error is calculated to be equal to $100 \times \frac{\text{SWAVG}_{\text{actual}} - \text{SWAVG}_{\text{desired}}}{\text{SWAVG}_{\text{desired}}}$. The reason for picking duty ratios of .72 as the lower bound is because when the battery voltage is low, the output node needs to be at 3.6V which is .72 of VBUS.

As expected, the lower the average inductor current, the worse the error gets due


<table>
<thead>
<tr>
<th>Inductor Current (A)</th>
<th>Duty Ratio</th>
<th>C=100pF</th>
<th>C=20pF</th>
<th>C=1pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.20</td>
<td>0.72</td>
<td>1.59</td>
<td>7.72</td>
<td>32.3</td>
</tr>
<tr>
<td>0.50</td>
<td>0.72</td>
<td>0.64</td>
<td>3.09</td>
<td>12.9</td>
</tr>
<tr>
<td>1.00</td>
<td>0.72</td>
<td>0.32</td>
<td>1.54</td>
<td>6.46</td>
</tr>
<tr>
<td>0.20</td>
<td>0.84</td>
<td>1.27</td>
<td>6.10</td>
<td>22.4</td>
</tr>
<tr>
<td>0.50</td>
<td>0.84</td>
<td>0.51</td>
<td>2.44</td>
<td>8.95</td>
</tr>
<tr>
<td>1.00</td>
<td>0.84</td>
<td>0.25</td>
<td>1.22</td>
<td>4.48</td>
</tr>
</tbody>
</table>

Table 4.1: Percent error for average input current measurement

to the fact that the average SW high voltage is closer to the VBUS voltage thus a smaller deviation due to error causes a higher percentage error. A lower duty ratio also leads to higher error because the hold period of the sample and integrate is increased, where a constant error is present. However, looking at the numbers in the case of using a 20pF capacitor, the worst case error present is roughly 8%. This 8% error can be more or less eliminated by trimming the sense FET MP2 to an optimal size.

4.3.1 Implementation of Average Inductor Current Control

Figure 4-6 depicts the circuit implementation of the average inductor current control. As described in section 4.2.2, the $V_{GSH}$ signal is used to control the connection between the switch pin and the RC circuit. MP2 acts as the switch transistor and MP4 is sized to be half the size of MP2 to alleviate error due to the charge dump when MP2 turns off. The ilimopamp is a high gain amplifier with a DC gain of 10000 and a unity gain crossover frequency of roughly 12 MHz. The circuit implementation of this amplifier is shown in figure A-3, and its frequency response is shown in figure A-4 of appendix A. Given the proper behavior of the ilimopamp and the sample and integrate circuitry, the voltage at node VAOC is equal to $1\Omega$ multiplied by the inductor current. That voltage then gets compared to a command current, represented as an input node, $V_c$, to generate an amplified signal that determines the duty voltage. That voltage is then compared to a PWM waveform to generate the duty ratio of
the converter. The circuit implementation of the comparator is shown in figure A-5 of appendix A. The frequency response of the comparator, figure A-6 of appendix A, shows the high gain feature of the comparator and figure A-7 shows that the comparator has an approximate delay of 13ns, which is sufficiently fast.
Figure 4-4: Matlab simulation for average input current measurement for duty ratio of 0.72
Figure 4-5: Matlab simulation for average input current measurement for duty ratio of 0.84
Figure 4-6: Circuit implementation for average inductor current control
Chapter 5

Input Current Limit Control

5.1 Overview

Since the chip is powered by the USB port, there must exist some circuitry to control the amount of current the chip draws from the USB port. Thus one of the major loops that control the command inductor current is the input current limit control loop. In a typical application, the USB port is able to supply a DC current of 100mA or 500mA due to the USB specifications. However, it is possible that in some situations the chip might want to be programmed to pull as much as 1A or more from the power source; thus, all modes of operation is also supported by this chip.

5.2 Stabilizing Input Current Limit Control

5.2.1 Analysis of Blocks of Input Current Limit Control

Given that the average current loop has a cross over frequency of 600 KHz, the frequency response from the command current node, \( V_c \), to the actual inductor current has a DC gain of roughly \( 1\Omega^{-1} \) with a pole at 600KHz. Thus, in order for that pole to have a minimal effect on input current limit loop, the loop should cross over at a frequency below 200 KHz under all operating and load conditions. In a buck converter,
\[ i_{IN} = d \cdot i_{OUT} \]  \hspace{1cm} (5.1)

Substituting the signals with its nominal and small signal components and eliminating the product of small signal components, we get:

\[ I_{IN} + i_{in} = D \cdot I_{OUT} + \tilde{d} \cdot I_{OUT} + D \cdot \tilde{i}_{out} \]  \hspace{1cm} (5.2)

Subtracting out the nominal portions from equation 5.2, we can get an expression for the small signal response for the input current, shown in equation 5.3.

\[ \tilde{i}_{in} = I_{OUT} \cdot \tilde{d} + D \cdot \tilde{i}_{out} \]  \hspace{1cm} (5.3)

The input current then gets scaled down by \( \alpha \) depending on the mode of operation and passed through the RC network of the sample and integrate circuit, which is modeled by the transfer function of \( SI_{icd}(s) \). Given our method of sizing the resistors and capacitors of the RC network, we can approximate \( SI_{icd}(s) \) to be unity gain for frequencies below the cross over frequency, and thus can be ignored. Since there are three different modes of operation, 100mA, 500mA, and 1A input current limit criteria, \( \alpha \) can vary between 200, 1000, and 2000.

The scaled down input current then needs to be passed through another RC network, \( CLP(s) \), in order to convert the sense current back to a voltage in order for it to be regulated. The difference between that voltage and a fixed bandgap voltage (1.2V) then gets amplified to produce the command signal \( v_c \). The RC network is thus designed to have a resistor in parallel with a capacitor. The resistor size is set to be 2.4K due to the sense current of 500uA and the reference voltage of 1.2 volts.

The complete block diagram for the input current limit loop is shown in figure 5-1.

Before the analysis of the entire loop can be made, we must first formulate the transfer function from \( \tilde{v}_c \) to \( \tilde{d} \). Applying black’s formula on the block diagram we get the result in equation 5.4.
\[
\frac{\dot{d}}{\dot{v}_c} = \frac{1}{H(s)} \left( \frac{1}{1+\beta} \right) H(s) \frac{1}{V_m^2 G_{acc}(s) H(s)} = \frac{1}{H(s)} \frac{1}{\beta v_c} \tag{5.4}
\]

Since \(\beta v_c\) is essentially 1 for frequencies less than the crossover frequency of the input current loop, we can simplify equation 5.4 to:

\[
\frac{\dot{d}}{\dot{v}_c} \approx \frac{1}{H(s)} = \frac{s^2 LR_{out} C_{out} + sL + R_{out}}{V_{in} (sR_{out} C_{out} + 1)} \tag{5.5}
\]

Thus, at high frequencies, \(f\), the transfer function will have a 20dB/dec gain, and the gain will be equal to what’s shown in equation 5.6.

\[
\frac{R_{out}}{V_{in}} \left( \frac{f \cdot 2\pi \cdot \sqrt{L \cdot C_{out}}}{f \cdot 2\pi \cdot R_{out} \cdot C_{out}} \right)^2 = \frac{R_{out}}{V_{in}} \frac{f \cdot 2\pi \cdot L}{R_{out}} = \frac{f \cdot 2\pi \cdot L}{V_{in}} \tag{5.6}
\]

Given the inductor size of 3.3uH, and an input voltage of 5 volts, the transfer function has a unity gain at roughly 200 KHz, and +20dB/dec gain. Thus, we can simplify the transfer function from the duty ratio to the input current to be approximately that shown in equation 5.7 at frequencies around the desired crossover frequency of the input current loop.

\[
\frac{\dot{I}_{in}}{\dot{v}_c} = D \frac{\dot{I}_{out}}{V_c} + I_{out} \frac{\dot{d}}{V_c} \approx D + I_{out} \cdot 8 \cdot 10^{-7} s \tag{5.7}
\]
We would like the DC gain from \( \tilde{i}_{in} \) to \( \tilde{v}_c \) to be at least 200 in order to reduce the error between the command input current and the actual input current. Since there are three different modes of operation, we want to design the error amplifier, \( G_{clprog}(s) \), to have variable \( g_m \), so the gain around the cross over frequency is different for each mode of operation given the same RC compensation network at the output. The error amplifier, whose schematic is shown in figure A-8 of appendix A, was thus designed to have the frequency response characteristics shown in figure 5-2.

5.2.2 Choosing the CLPROG Network

![Frequency response of error amplifier for input current limit loop in all three modes](image)

Figure 5-2: Frequency response of error amplifier for input current limit loop in all three modes

Given this, we have a fixed gain of roughly \( 5.9 \times 10^{-3} \times CLP(s) \) from \( \tilde{i}_{in} \) to \( \tilde{v}_c \) through the feedback branch and the amplifier stage. The upper limit for the gain from \( \tilde{v}_c \) to \( \tilde{i}_{in} \) in the forward loop at 200 KHz is \( D + I_{out} \times 8 \times 10^{-7} \times 2\pi \times 200 KH z \leq 2 \).
Thus, we want the CLPROG network to have a pole at roughly 7 KHz with its DC gain of 2400, such that the loop will cross over at the desired 200 KHz. Thus the capacitor size is required to be at least 10nF. To be on the safe side, the capacitors were sized to be 20nF to ensure a loop cross over frequency below 200 KHz.

Note that the zero in the transfer function from $\tilde{v}_c$ to $\tilde{i}_{in}$ varies, but in the worst case, when its zero is at its lowest frequency, the entire loop still crosses over at 200 KHz. Also, if the zero of the transfer function from $\tilde{v}_c$ to $\tilde{i}_{in}$ actually occurs at a high frequency beyond 200 KHz, the zero at roughly 30 KHz in the $G_{clprog}(s)$ network improves the phase margin of the loop transfer function.

5.3 Circuit Implementation

![Circuit Diagram]

Figure 5-3: Circuit implementation for input current measurement

The circuit implementation of the input current measurement is shown in figure 5-3. As described in section 4.2.1, the voltage at the SWAH3 node is averaging the
on voltage of the SW node when the PMOS switch is on, and holding the value when the PMOS switch is off. That voltage is servoed to the SWAH4 node through the high gain amplifier $c_{limopamp}$.

Depending on the modes of operation, MP1, MP2, and MP3 are controlled to set the ratio, $\alpha$, between the PMOS switch and the sense transistors. This is done so that the nominal current flowing through MP4 in all three modes of operation is the same. The VSAMPLE input is then used to control the switches MN1, MN2, and MN3, such that the current flowing down MP4 is shunt to ground when the PMOS switch is off. Thus, the current flowing through MN3 is equal to the current flowing through MP4 multiplied by the duty ratio of the converter. This current is therefore the input current divided by alpha.

Since $\alpha$ is proportionally set in the three different modes of operation, the nominal current flowing through RCLPROG is equal to 500µA independent of mode of operation, thus making the nominal voltage at the VCLPROG node 1.2 volts when the control loop is in regulation.
Chapter 6

Constant Battery Current Control

6.1 Overview:

The batteries used in the application of the chip are typically made of Lithium Ion cells. Even though battery charging can be done by simply feeding current into the battery, the life of the battery is drastically shortened if there is no regulation on the amount of current being fed into the battery or of the final float voltage. For Lithium Ion batteries, a typical charging system is considered to be CCCV (constant current constant voltage) charging. In such a system, the battery is charged with a fixed current, usually determined by the battery size, until its reaches a float voltage, at which point the charger enters its constant voltage phase where the current flowing into the battery tapers off in order to maintain a constant voltage at the battery node.

In addition to maintaining a constant charging current into the battery until the float voltage is reached, it is also required for this application that the system output voltage be maintained above 3.6V regardless of how low the battery voltage is. The 3.6 volts is considered to be the lower deck voltage, and circuitry is required to maintain the output voltage to be a minimum of 3.6 volts regardless of the battery voltage.

The first part of the constant battery current control analysis will focus on maintaining constant current assuming that the battery voltage is above the lower deck voltage. The second part of the analysis will demonstrate the effect the lower deck
circuitry will have on stabilizing the constant battery current control.

6.2 Stabilizing Constant Battery Current Loop without Lower Deck

6.2.1 Analysis of different blocks of the constant battery current control loop without the Lower Deck

The current through the inductor gets split into two branches, part of the current flows into the battery to charge it, while the rest flows through the output node to power the load device. For simplicity, the external load at the output is modeled to be a resistor in parallel with a capacitor. Typically, the load capacitance of the device is at least 10uF due to the capacitance of an external device that is being powered by the charger as well as any additional capacitance the user adds for output filtering.

In the battery branch, the output node is connected to the battery through an internal power transistor. This transistor is sized to be 120K/\mu\Omega in order for it to have a sufficiently low on resistance while not taking up too much space on chip. In the case when the battery voltage is above the lower deck voltage of 3.6 volts, the gate of the transistor is grounded to ensure minimum power dissipation through the device. Furthermore, the Lithium Ion battery is modeled as a small resistor in series with a huge capacitor.

The amount of current flowing through the battery then gets measured by a sense transistor that delivers one thousandth of the battery current. That current is then converted into a voltage by a resistor the user sets at the VPROG node. Thus, when the servo loop is complete, the programmed constant battery current is equal to the reference voltage (1.2V) divided by the RPROG resistor multiplied by 1000. The user may choose to charge the battery at anywhere between 500mA and 1.5A, thus the resistors they use will range from 2.4K\Omega to 0.8K\Omega respectively.

The outlining schematic for the output load as well as battery current measurement is shown in figure 6-1. The IBCGMAMP node is used to better compensate the
entire loop gain, and will be discussed later in this section.

The difference between VPROG node voltage and the reference voltage is then amplified through an error amplifier which outputs the voltage for the command current. The transfer function of the error amplifier is represented by $G_{prog}(s)$. The complete block diagram for the constant battery-current loop without LD regulation is shown in figure 6-2.

Once again, we would like the constant battery current loop to have a cross-over frequency lower than 200 KHz. Thus, in the frequencies of interest, $\frac{\tilde{I}_{bat}}{V_C} = 1$, due to the high frequency cross-over of the minor loop.
Load(s) = \frac{1}{s R_{\text{out}} C_{\text{load}} + 1} \star \frac{R_{\text{load}}}{R_{\text{load}} + R_{\text{onmp2}} + R_{\text{bat}}} \quad (6.1)

where,

\[ R_{\text{out}} = \frac{R_{\text{load}}}{R_{\text{onmp2}} + R_{\text{bat}}} \quad (6.2) \]

and \( \frac{1}{\alpha} \) is fixed to be \( \frac{1}{1000} \) in this loop.

What makes this loop slightly difficult to compensate variations in the load resistance, load capacitance, battery resistance, and PROG resistor. We must first analyze the range of variation in these variables before designing the error amplifier, \( G_{\text{PROG}}(s) \) and its compensation network.

In order for the battery current loop to be in regulation, there can not be a huge load at the output. If such a load existed, then the constant input current limitation loop will be in charge of current regulation. The extreme case is where the input can supply 5 watts of power (1A input current limit conditions) and the user programs for 500mA of battery charge current, while the battery is at 3.6V. Thus, there can be a maximum of 3.2W of power into the load while still having the constant battery current loop be in regulation. 3.2W of power at 3.6 volts translates to a minimum load resistance of 4\( \Omega \). Since it’s possible for the external load to draw no power from the output node of the charger chip, the load resistance at the output node could be infinitely large. The equivalent load capacitance can also vary quite a bit, but in general it is between 10\( \mu \)F to 100\( \mu \)F.

The internal battery resistance varies with each individual battery, but is typically around .05 to 0.2 ohms. \( R_{\text{onmp2}} \) is typically equal to .07\( \Omega \) given the size of the transistor, thus making the resistance looking down the battery branch approximately .12 \( \Omega \) to .27 \( \Omega \). Lastly, the PROG resistor, as mentioned before, can vary between 0.8\( K \Omega \) to 2.4\( K \Omega \).

Given the relative sizes of \( R_{\text{load}} \) to \( R_{\text{onmp2}} \) and \( R_{\text{bat}} \), the Load(s) transfer function can be simplified to \( \text{Load}(s) = \frac{1}{s(R_{\text{onmp2}}+R_{\text{out}})C_{\text{load}}+1} \), thus the pole location of the transfer function can vary anywhere between 6 KHz in the high internal battery
resistance and high load capacitance case to 130 KHz in the low battery resistance and low load capacitance case.

The DC gain of the loop from $\tilde{v}_c$ to $\tilde{v}_{\text{prog}}$ also varies from 0.8 in the 1.5A charge mode to 2.4 in the 0.5A charge mode. Thus, an error amplifier needs to be designed such that acceptable operation is achieved under all varying DC gain settings and load pole frequencies.

6.2.2 Analysis of Constant Battery Current Error Amplifier

In order to reduce the error between the command battery current and the actual battery current, a high gain amplifier is needed. The amplifier was designed to have a DC gain of roughly 150.

In one extreme case, where the DC gain from $\tilde{v}_c$ to $\tilde{v}_{\text{prog}}$ is equal to 2.4 and the load pole is at 130 KHz, the gain at 200 KHz from $\tilde{v}_c$ to $\tilde{v}_{\text{prog}}$ is equal to roughly 1.6. Thus, the gain of the amplifier at 200 KHz must be lower than 0.67.

In the other extreme case, where the load pole is at 6 KHz, and the DC gain from $v_c$ to $v_{\text{prog}}$ is equal to 0.8, the gain of the amplifier should be greater than 1.25 at 6 KHz in order to ensure that the loop does not cross-over at a frequency lower than that of the load pole.

As long as the condition is met such that the gain of the error amplifier is greater than 1.25 at 6 KHz, and less than 0.67 at 200 KHz, the cross-over frequency of the entire loop will be guaranteed to be between 6 KHz and 200 KHz, with at worst a 90 degree negative phase contribution from the load transfer function. Thus, as long as the error amplifier does not contribute more than 60 degrees of negative phase at any frequency between 6 KHz and 200 KHz, the loop gain will cross-over with sufficient phase margin.

A slight adjustment of the circuit was made to further improve the phase margin of the circuit. The idea behind the improvement is that when the battery charge current is programmed to be high, the entire gain from $v_c$ to $v_{\text{prog}}$ decreases, thus the error amplifier can have a higher high frequency gain, which can be accomplished by supplying the amplifier with more bias current. Essentially, the IBCGMAMP
node from figure 6-1 can be connected to a current mirror in the error amplifier to supply the error amplifier with more tail current. The reason for this circuitry is to decrease variation in the high frequency gain of the loop under different charge current conditions. Thus, we narrow down the range of possible cross-over frequencies of the loop transfer function and a more precise compensation circuit can be employed to improve the phase margin of the loop.

The circuit implementation of the constant battery current error amplifier and its frequency response are shown in figures A-9 and A-10 of appendix A.

6.3 Stabilizing Constant Battery Current Loop with Lower Deck Regulation

If the battery voltage is too low, we need to maintain the lower deck voltage of 3.6 volts at the output node, given the user-determined constant charge current. A means to maintain the lower deck voltage at the output given a constant charging current is for the gate of MP2 in figure 6-1 to no longer be tied to ground. By controlling that gate voltage, the drain to source resistance of MP2 can be adjusted to the appropriate level. Thus the topology of the battery current measurement and output load with the lower deck considerations is shown in figure 6-3.

Figure 6-3: Circuit topology of battery current measurement with lower deck circuitry
### 6.3.1 Analysis of Blocks in Control Loop

Since the lower deck amplifier controls the gate voltage of the charge FET, it also controls the gate voltage of the battery current sense FET. Thus, by changing the gate voltage, additional small signal change to the battery sense current are added.

The block diagram for the entire loop is shown in figure 6-4:

![Block Diagram for Constant Battery Loop with Lower Deck Amplifier](image)

**Figure 6-4: Block Diagram for Constant Battery Loop with Lower Deck Amplifier**

The load impedance may be modeled as:

\[
Load(s) = \frac{R_{out}}{sR_{out}C_{out} + 1} = \frac{R_{on} * R_{load}}{sR_{out}C_{out} + 1 * R_{load} + R_{on}}
\]  

(6.3)

where

\[
R_{out} = \frac{R_{load}}{R_{on} + R_{bat}} \approx \frac{R_{load}}{R_{on} + R_{bat}}
\]  

(6.4)

The reason why the approximation can be made is that when the lower deck amplifier is in regulation, the drain to source resistance of the charging FET, MP2, is quite large compared to the battery’s internal resistance.

We can further conclude that:

\[
\frac{\tilde{I}_{bs1}}{\tilde{I}_{out}} = \frac{1}{sR_{out}C_{out} + 1} * \frac{R_{load}}{R_{load} + R_{on}} * \frac{1}{\alpha} = \frac{1}{sR_{out}C_{out} + 1} * \frac{R_{load}}{R_{load} + R_{on}} * \frac{1}{1000}
\]  

(6.5)

\[
\frac{\tilde{I}_{bs2}}{\tilde{I}_{out}} = \frac{R_{on}}{sR_{out}C_{out} + 1} * \frac{R_{load}}{R_{load} + R_{on}} * Idiode(s) * g_{m(sense)}
\]  

(6.6)
since the sense FET is \( \frac{1}{1000} \) the size of the charge FET, \( R_{on} \ast g_m(\text{sense}) \) is equal to \( \frac{1}{1000} \). Therefore,

\[
\frac{\tilde{i}_{hs2}}{\tilde{i}_{out}} = \frac{1}{sR_{out}C_{out} + 1} \ast \frac{R_{load}}{R_{load} + R_{on}} \ast \frac{1}{1000} \ast Idiode(s) \tag{6.7}
\]

Essentially, in order for the battery current loop to remain stable, we need to design \( Idiode(s) \) such that it has high DC gain, and has a dominant pole at a low enough frequency such the transfer function has a cross-over frequency lower than the cross-over frequency of the constant battery control loop. If that condition can be satisfied, the magnitude of \( \tilde{i}_{hs2} \) is much smaller than that of \( \tilde{i}_{out} \) at the cross-over frequency, and thus the right hand branch of the block diagram would be insignificant and can be ignored leaving us with the block diagram much similar to the one in figure 6-2 for when the lower deck circuitry was not required. The only difference in this case is that the load pole can actually occur at a much lower frequency due to the higher \( R_{on} \) resistance. In the extreme case, the battery might go as low as 2.7 volts, which leaves a voltage drop of 0.9 across the drain and source of the charge FET, MP2. If we are regulating at the minimum current of 500mA, it leads us to conclude that the largest drain to source resistance of MP2 is equal to 1.8Ω. Thus, the lowest frequency for the load pole is now at 900 Hz. Looking at the frequency response of the error amplifier in figure A-9 of appendix A, we can conclude that under the lowest gain conditions (1.5A programmed battery charge current), the loop gain transfer function will still cross-over at a frequency beyond 6 KHz. Thus, given that, as was shown in the case of no lower deck voltage regulation considerations, the constant battery current loop will be stable and cross-over with sufficient phase margin.

### 6.3.2 Analysis of the Lower Deck Regulator Circuitry

The transfer function for \( \tilde{v}_{out} \) to \( \tilde{v}_{gate} \), \( Idiode(s) \), needs to be designed in such a way that its transfer function will reach unity gain before the cross-over frequency of the loop. The ideal diode not only must have the important property of setting the gate voltage of the charging FET to the appropriate value in order to maintain a 3.6 volts
output when the battery voltage is low, but it must also be able to quickly discharge the gate voltage to ground when the load actually needs to draw current from the battery in the case when the power limitation at the input is less than the power needed at the load. Under that condition, the battery is actually supplying current into the load, and the output voltage is set to be regulated at 15mV below the battery voltage. Lastly, the ideal diode circuitry must have the functionality that when the battery voltage is above 3.6 volts, which leads to the output voltage to be greater than 3.6 volts, the gate voltage of the charge FET needs to be grounded to ensure the least amount of power dissipation through the charge transistor. One possible circuit implementation of this lower deck circuitry, \( I_{\text{diode}}(s) \), is shown in figure 6-5.

![Figure 6-5: Circuit Implementation of the Ideal Diode Functionality](image)

Analyzing this circuit, we find that all the conditions are met. When both the battery node and output node voltages are above 3.6 volts, the signal at node VT1 is set to high, thus shutting off the transistor MP4. With MP4 turned off, the VGATE node will discharge through MN4 and the charge transistor will be fully turned on.

When the battery node is below 3.6 volts, the amplifier \( I_{5} \) whose schematic is shown in figure A-11 of appendix A, will regulate the output node to be near 3.6 volts with negative feedback. This is because as the output voltage goes too high, VT1
will increase, thus decreasing the VGATE voltage, which will decrease the resistance of the charge FET leading to a decrease in the output voltage. A miller capacitance was added between the positive terminal of the amplifier, I5, and the VGATE node to produce a dominant low frequency pole that will allow the gain of the frequency response of Idiode(s) to start to decrease at a very low frequency. The transfer function, Idiode(s), from VOUT to VGATE is shown in figure A-12 of Appendix A, and it can be noted that at roughly 3 KHz, the gain of Idiode(s) has already dropped to unity gain, which is sufficiently lower than the cross-over frequency of the constant battery current loop under all modes of operation.

Lastly, if the power requirement at the load is too high for the input to supply, I5 will simply ground the gate of MP4, and the common gate amplifier through the branch R3 and R4 will set the output voltage to be roughly 15 mV below the battery voltage. Another important point to note in this circuit regards operation under a sudden load pulse. Suppose the circuit is in lower deck regulation, where the output is being regulated at 3.6 volts with some VGATE voltage, and a sudden slug of current is pulled from the output such that current needs to be drawn from the battery. In this case, the VGATE voltage needs to be discharged immediately to ensure that the output node does not fall too far below the battery voltage. This was accomplished through the use of a high speed comparator. The FASTON node goes high when the output voltage drops to 45 mV below the battery voltage, and once that node goes high, MN5 is immediately turned on to discharge the gate capacitor of the charge FET.
Chapter 7

Constant Battery Voltage Control

7.1 Overview

Once the battery is near full charge, the current supplied to the battery should decrease in order to maintain a constant voltage at the battery node. It is also required for the error in the float regulation to be extremely small, so that the actual regulated voltage will have less than 0.5% error from the desired 4.2 Volts.

7.2 Stabilizing Constant Battery Voltage Control Loop

Stabilizing the constant battery voltage loop is relatively simple due to the lack of varying modes of operation which were present in both the constant battery current loop and the input current limit loop. Also, since the battery voltage is above 3.6V, which is the case when the constant voltage control is in regulation, the charge FET is fully turned on, thus making the resistance looking down the charge FET branch a lot less resistive than the resistance looking into the load. Thus, the the transfer function of the incremental battery voltage is equal to the internal battery resistance times the incremental inductor current multiplied by the load pole.

The battery voltage then gets down scaled by 4.2/1.2 and the result is compared
to the reference voltage and amplified through a high gain amplifier to produce the voltage for the command current.

The Block Diagram for the Constant Voltage Control Loop is shown in Figure 7-1.

![Block Diagram for the Constant Voltage Control Loop](image)

Figure 7-1: Block diagram form constant voltage control loop

Again, in the frequencies of interest (below the crossover frequency), $\frac{i_{\text{out}}}{v_{c}} = 1$.

$$\text{Load}(s) = \frac{R_{\text{bat}}}{sR_{\text{on}}C_{\text{out}} + 1} \quad (7.1)$$

$R_{\text{on}}$ is the series resistance of the charge FET with its gate grounded and the internal battery voltage of the battery. We have concluded previously that the on-resistance of the charge FET is roughly .07Ω and the internal battery resistance ranges from .05Ω to .2Ω. Thus, the load pole again ranges from 6 KHz to 130 KHz, with the DC gain from $\frac{i_{\text{out}}}{v_{c}}$ to $\frac{d}{\dot{d}}$ ranging from .0143 to .0571.

The error amplifier $G_{\text{comp}}$ is designed to have a DC gain of 1500 to limit DC error of the constant battery voltage regulation. Given this, the DC of the entire loop varies from 20 to 80. Thus operation is acceptable as long as the $G_{\text{comp}}(s)$ drops to a gain of 1500/80 before the earliest possible load pole at 6 KHz.

The circuit implementation and its frequency response is shown in figures A-13 and A-14 of appendix A.
Chapter 8

Interaction between Control Loops

Sections 5 through 7 have described methods such that each control loop will remain stable and behave appropriately under the appropriate load conditions. For instance, if the battery is at 3.6 volts supporting a load of 1.8 watts, the charger is programmed for 500mA of constant charging current, and the input current limit is set to 500mA, the duty cycle of the switcher will be controlled by the input current limit loop. This is because under these conditions, the battery wants to sink 1.8 watts of power, but the power supplied at the input is limited to 2.5 watts. Thus, the constant battery current and the constant battery voltage loops are asking for more inductor current, but the input current limit loop is limiting the inductor current since the power drawn from the load and battery sums to be greater than the input power supply. Now, suppose the load is disconnected, then the input current limit loop and the constant battery voltage loop are asking for more current but the 500mA battery charge current regulation is limiting the amount of inductor current. Even though each individual loop has been shown to be stable and can regulate the inductor current appropriately, circuitry is still required to decide which of the three loops should actually be used to control the inductor current.
8.1 Minimizer Circuit

Essentially, the inductor current should be controlled by the loop that is requesting the smallest inductor current. The reason for this is that each of the loops acts as a restriction to how much current can actually flow through the inductor. That is, the default conduction of each control loop is to deliver power, the control signal seeks only to retard power. In order to satisfy all three restrictions, the actual inductor current must be controlled by the loop that commands the least amount of current. In order to accomplish this, the outputs of the error amplifier for all three loops must be passed into a minimizer circuit that chooses the lowest command current out of the three. This can be accomplished using a simple circuit as shown in figure 8-1.

Figure 8-1: Circuit implementation for minimizer circuit

The signals VC1, VC2, and VC3 are the outputs of the error amplifiers of the three loops. Thus, if all three error amplifiers are connected together through this minimizer circuitry, the resulting circuit looks like what is shown in figure A-15 of appendix A. This entire circuit is named erroramp, and it takes as input the scaled measurements of input current, battery current, and battery voltage as well as information about the modes of operation for input current limit loop and the constant battery current loop, and outputs a voltage that commands the inductor current.

The motivation behind choosing a circuit such as a minimizer to decide which loop is in control is so that there is a smooth transition from one loop to the next. Suppose VC1 is the output of the error amplifier for the input current limit loop, VC2 is the output of the error amplifier for the constant battery current loop, and a large
load step is pulled at the output node, forcing the chip to transition from constant battery current control to input current limit control. What would happen is that the VC2 node will increase but stabilize at a certain value such that the inductor current will be equal to the programmed constant current for the battery plus the current demanded by the load. However, as the inductor current is rising to meet those criteria, the input current is also increased, and the CLPROG node of figure 4-1 will start to rise, which will lead to the decrease of the voltage on the VC1 node. At some point, the voltage at node VC1 will fall below the voltage at node VC2, and the input current limit loop will be in control of the inductor current. Naturally, when this happens, the inductor current will start to decrease, resulting in less current flowing into the battery, which will cause a decrease in the voltage on the PROG node (Figure 6-3) and a consequent rise in the VC2 node. Due to this design topology for the minimizer circuit, errors due to transistor matching and offset are not really a problem due to the large gains of the outer loops.

Simulations demonstrating the correct behavior in the transitions between control loops are shown in appendix B.

8.2 Improvement on Input Current Violation

Even though transition between loops will occur with changes in load conditions, these transitions are not instantaneous. This becomes a huge problem when there is a large increasing current step at the output node, because the input current limit loop can't start regulating immediately, and the inductor current is controlled by one of the other two loops. Thus, the inductor current will be regulating at a current that violates the input current specification of the USB port, which will lead to a decrease in the input voltage. Since the input voltage is the source of power for all of the circuitry in the chip, a significant decrease in that voltage can lead to erroneous chip behavior.

In order to ameliorate the effect of input current violation, we would want to make the input current limit loop able to respond as quickly as possible, while drastically
slowing down the response of the other two loops. The way this was accomplished was to set a slew rate limitation on the VC2 and VC3 nodes of figure A-15 in appendix A. By doing so, the command current from the constant battery current loop and the constant battery voltage loop will increase slowly, and thus will drastically hinder the response speed of the constant battery current and constant battery voltage loops to an increasing load step at the output. Thus, the inductor current will not rise as fast, and the time for which the input current limitation is violated is drastically decreased.
Chapter 9

Conclusion

This thesis delved into the design and simulation of a new architecture for a USB-powered battery charger chip. The two main advantages of the new architecture over its predecessor are the improved charging efficiency as well as the decrease in USB current limit violation time.

The battery charger chip was designed using a synchronous switching buck converter with average current control. It had three main loops that limited the maximum specified current drawn from the USB port, regulated constant charging current into the battery when power is available and battery is not fully charged, and maintained a float voltage of 4.2 volts for a nearly charged battery. While regulating all this, the chip maintains the ability to regulate the output voltage at or above 3.6 volts regardless of the battery voltage as long as there is sufficient power from the USB port.

Simulations of these behavior are shown in appendix B.
Appendix A

Schematics and Behaviors

Figure A-1: Circuit for error amplifier of average current control loop
Figure A-2: Frequency response for the error amplifier of average current control loop
Figure A-3: Circuit implementation of ilimopamp
Figure A-4: Frequency response of opamp
Figure A-5: Circuit implementation of PWM comparator
Figure A-6: Frequency response of PWM comparator

Figure A-7: Transient response of PWM comparator
Figure A-8: Circuit implementation of error amplifier for input current limit
Figure A-9: Circuit implementation of error amplifier for constant battery current loop
Figure A-10: Frequency response for error amplifier for constant battery current loop
Figure A-11: Implementation for lower deck amplifier

Figure A-12: Frequency response for Idiode(s)
Figure A-13: Circuit implementation for battery voltage error amplifier

Figure A-14: Frequency response for battery voltage error amplifier
Figure A-15: Circuitry for the complete error amplifier for all three loops with minimizer circuitry
Figure A-16: Complete high level schematic of battery charger
Appendix B

Simulation Results
Figure B-1: Response to a 1A load step increase at the output w/ battery voltage at 3.2V. Constant current charging and input current limit both set to 500mA
Figure B-2: Response to a 1A load step decrease at the output w/ battery voltage at 3.2V. Constant current charging and input current limit both set to 500mA
Figure B-3: Response to a 1A load step increase at the output w/ battery voltage at 3.2V. Constant current charging and input current limit both set to 1A.
Figure B-4: Response to a 1A load step decrease at the output w/ battery voltage at 3.2V. Constant current charging and input current limit both set to 1A.
Figure B-5: Response to a 1A load step increase at the output with battery voltage at 4.15V. Input current limit both set to 500mA.
Figure B-6: Response to a 1A load step decrease at the output w/ battery voltage at 4.15V. Input current limit both set to 500mA.
Figure B-7: Response to a 1A load step increase at the output w/ battery voltage at 3.8V. Constant current charging and input current limit both set to 1A.
Figure B-8: Response to a 1A load step decrease at the output w/ battery voltage at 3.8V. Constant current charging and input current limit both set to 1A.
Figure B-9: Response to a 1A load step decrease at the output w/ battery charging to float voltage. Constant current charging set to 500mA
Bibliography


