Particle Generation in a Chemical Vapor Deposition/ Plasma-Enhanced Chemical Vapor Deposition Interlayer Dielectric Tool

by

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Submitted to the Department of Materials Science and Engineering in partial fulfillment of the requirements for the degree of

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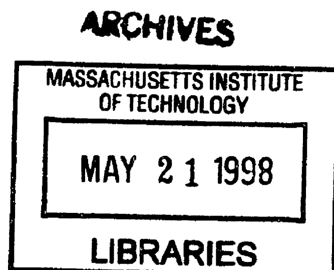

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Abstract

The interlayer dielectric plays an important role in multilevel integration. Material choice, processing, and contamination greatly impact the performance of the layer. In this study, particle generation, deposition, and adhesion mechanisms are reviewed. In particular, four important sources of interlayer dielectric particle contamination were investigated: the cleanroom environment, improper wafer handling, the backside of the wafer, and microarcing during process.

Thesis Supervisor: Professor L. C. Kimerling
Title: Professor of Materials Science and Engineering and Director, MPC

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Chapter 1

Back End of Line Chemical Vapor Deposition: The Interlayer Dielectric

1.1 Effects on Circuit Performance

In recent years, the need for innovative ways to shrink chip geometries has resulted in the development of highly complex, multilevel devices. Circuit designers are not only shrinking transistors and metal lines, they are also building vertically. Today's microprocessors already have 3 or 4 metal layers, while current trends are predicting as many as 8 layers in the future.[1] Each additional metal layer requires an insulating layer to electrically isolate it from the existing metallization. Because the insulating layer is deposited between metal layers it is called an interlayer dielectric (ILD).

The ILD plays a very important role in the electrical performance and reliability of the circuit. The dielectric constant of the ILD material as well as the thickness of the film contribute greatly to the capacitance of the circuit through the following relationship

$$C = \frac{\varepsilon_r \varepsilon_o A}{L} \tag{1.1}$$

where C is the capacitance, ε_r is the dielectric constant of the material, ε_o is the dielectric constant of free space, A is the area of the metal lines, and L is the ILD thickness.

In turn, the circuit capacitance impacts other aspects of circuit performance. Crosstalk or electrical interaction between metal lines is determined by the capacitance of the ILD layer. For a given ILD thickness, crosstalk decreases as the dielectric constant decreases, where as for a set dielectric constant, crosstalk increases as the ILD thickness decreases. The capacitance of the ILD layer also limits the speed of the circuit. The time delay of the circuit, τ, is directly related to the circuit capacitance, C, such that

$$\tau = RC \quad (1.2)$$

where R is the resistance of the metal lines.

The AC power dissipation of the ILD layer is controlled by dielectric constant and layer thickness. As the field between two metal lines alternates, the atoms in the dielectric material attempt to follow the field. The transient motion of the atoms dissipates heat resulting in power loss. Materials with higher dielectric constants follow the field more readily than materials with lower dielectric constants, therefore the transient motion and the power loss of higher dielectric materials is greater. The number of transient atoms also affects power loss. The more material subjected to the field, the more transient motion and power loss that occurs.[2] Power dissipation is, therefore, directly proportional to the dielectric constant and thickness of the ILD layer.

It has been shown that the choice of ILD material and the thickness of the layer can greatly modify circuit performance. A low dielectric constant material can reduce capacitance, thereby lowering power consumption and crosstalk, while increasing circuit speed. Although many materials exist with acceptable dielectric constants, the deposition of a dielectric film which is suitable for use as an ILD is not an easy task. Several materials issues must be addressed.

1.2 Materials Design Criteria

An ILD film must have the appropriate electrical, mechanical, and chemical properties. Among these properties are good gapfill capability and step coverage, low water content, low stress, good adhesion to other integrated circuit (IC) layers, stability at processing temperatures, low defect density (to be discussed in-depth in Chapter 2), uniform thickness and composition, and the potential for global planarization.[3] Each of these

concerns will be discussed individually.

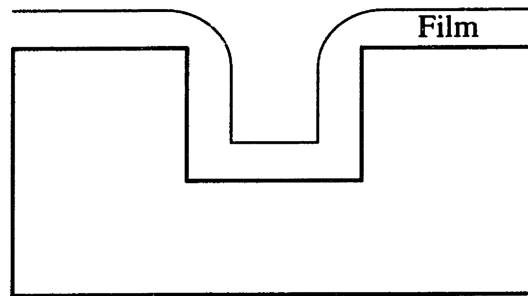


Figure 1.1: Conformal deposition

In order to completely isolate the metal lines, the ILD film must fill the spaces between metal lines within a single layer, as well as those between adjacent metal layers. This requires a conformal film with good gap-fill capabilities. As shown in figure 1.1, a conformal film is a film which has uniform thickness across the substrate regardless of the substrate topography. Conformality of the film is determined by the surface mobility of the reactant species. If the reactant species easily stick to the surface of the substrate, the film thickness will be determined by the arrival angle of the reactant molecule. As shown in figure 1.2, locations with greater arrival angles will have more deposition and those with smaller arrival angles will have less deposition. As a result, the upper corners of the metal lines will have the greatest amount of deposition. This effect is sometimes referred to as loafing.[4] Such non-conformal deposition often results in the formation of voids between metal lines. Voids are a reliability issue because they can increase the risk of crack propagation, collect chemicals during process, and cause breaks in metal lines if etched open during planarization.[5] If reactant species have high surface mobility, the reactant molecules move easily along the surface of the substrate resulting in conformal film deposition. At low pressures, reactant molecules with high surface mobility can become a problem. If the mean free path of the reactant molecules becomes longer than the distance between metal lines, the molecule will overshoot the edge of the metal line

and shadowing will occur.[6] As shown in figure 1.3, shadowing is similar to loafing in that voids may form between metal lines.

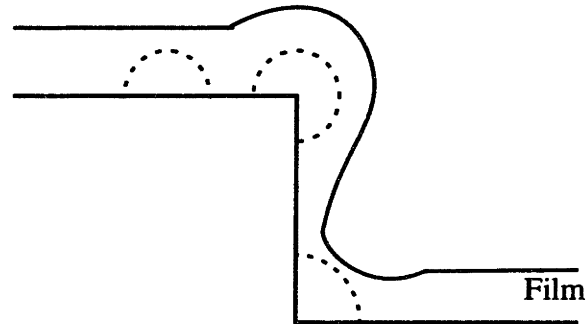


Figure 1.2: The amount of deposition is dependent on the angle of arrival of the reactant species to the substrate surface.

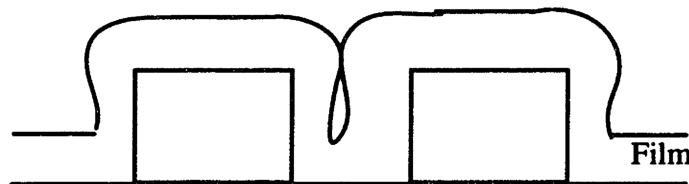


Figure 1.3: Shadowing during deposition can result in the formation of voids between metal lines.

The best gap-fill is achieved with flow-like deposition. Although the deposition is non-conformal, there is no film build-up on the upper corner of the metal lines. As shown in figure 1.4, the upper corners of the metal lines are rounded off as the valleys between the metal lines are filled. Thus, flow-like deposition greatly reduces void formation.

The presence of moisture in the ILD film can greatly alter its electrical performance. The dielectric constant of the film is increased, as well as the capacitance and the RC time delay. Furthermore, if the water is driven off during process, performance-damaging free charges can be left behind.[7] The chemical structure of the film is also a concern. When exposed to moisture OH ions can be formed in the film. If an OH ion replaces an atom

within the network, a substitutional defect is created.[8] Most likely the bond formed will be less rigid than the original bond. As the flexibility of the network increases, it becomes more prone to crack propagation.[9] The presence of moisture can also introduce H atoms to the film. If an incorporated H atom is driven off during processing, a dangling bond may result. A dangling bond is extremely reactive and may cause impurities to be incorporated into the film.[10] Film adhesion can also be affected by water incorporation. Large amounts of moisture within the ILD film can cause blistering and delamination during subsequent processing steps.[11]

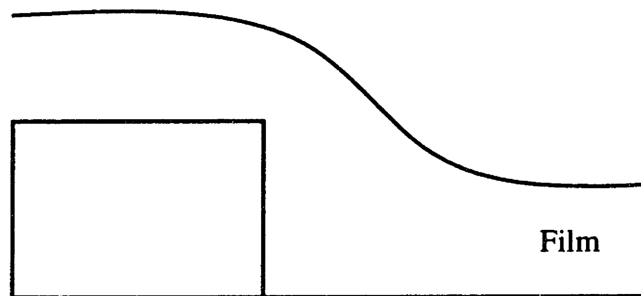


Figure 1.4: Flow-like deposition

The mechanical stress of the ILD layer should be neutral to slightly compressive, in order to balance the tensile stress of the metallization layers. High ILD stress can result in lower crack resistance and shorter time to failure.[12] Furthermore, large ILD stresses can cause wafer warpage. Excessive wafer curvature is undesirable because it can lead to difficulties in planarization.

In order to avoid delamination problems, the ILD material must adhere to metallization layers and other layers it may contact. Good adhesion requires the formation of chemical bonds at the materials interface. If the formation of such bonds does not readily occur, the reaction can sometimes be facilitated by a short etch or deposition step.

Processing temperatures of the ILD layer are limited by the material properties of the metallization. Current IC technology uses aluminum metal lines. Given that the melting point of aluminum is 660°C, the ILD process temperature must not exceed 450°C to avoid softening previously laid metal lines.

As previously discussed, many electrical properties of the ILD layer depend on the thickness and dielectric constant of the layer. Because dielectric constant is determined by chemical make-up, the composition of the ILD layer must uniform throughout. To avoid local variations in circuit performance, the ILD layer must have an uniform thickness and composition.

The ILD layer must be planarized before the next metallization layer is deposited. Simply put, planarization is a large scale smoothing of the wafer's topography. Although there are many levels of planarization, global planarization is the most desirable for multilevel interconnect technology. As shown in figure 1.5, global planarization fills the gaps between metal lines, while reducing the overall step height of the layer. Planarization of the ILD layer is necessary to ensure good metal step coverage and a field flat enough for the lithography depth of focus used to pattern metal lines and vias.[13] The resolution and depth of focus of the lithography tool are limited by the following relationships

$$Resolution = \frac{K_1 \lambda}{(NA)^2} \quad (1.3)$$

$$DepthofFocus = \pm \frac{K_2 \lambda}{(NA)^2} \quad (1.4)$$

where K_1 and K_2 are coefficients determined by the optical system and the photoresist, λ is the wavelength, and NA is the numerical aperature.[14] Shorter wavelengths required to resolve the shrinking feature sizes of today's technology, result in a significantly reduced

depth of focus. Planarization techniques are necessary to reduce height variations on the ILD surface to within the depth of focus. If proper planarization is not achieved valleys in the ILD layer can cause metal stringers and thin areas in the film may result in etch-out of metal plugs.[15]

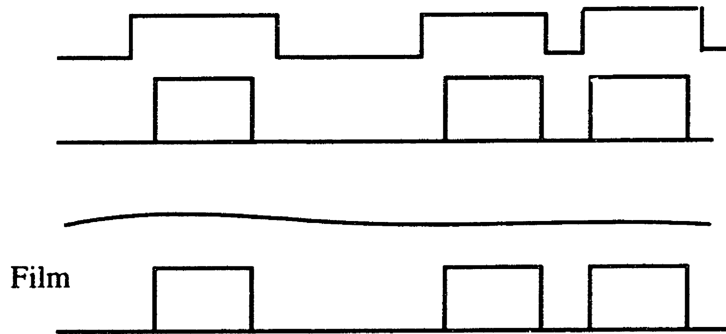


Figure 1.5: Global planarization results in significant step reduction and large-scale smoothing.

1.3 Materials Choice and Processing

Currently, silicon oxide is the most widely used material in ILD technology. With a relative dielectric constant of 3.9, silicon oxide provides adequate insulation for metal layers, while reducing crosstalk between metal lines. Given this dielectric constant, the capacitance, RC time delay, and power dissipation of silicon oxide are undesirably high. Nonetheless, silicon oxide ILD technology continues to be used because its deposition techniques are well developed and have proven themselves adaptable to IC technology. In this study, the ILD layer is made up of three silicon oxide films: a thin plasma enhanced tetraethyl orthosilicate (PTEOS) film, a sub-atmospheric chemical vapor deposition (SACVD) oxide film, and a thick PTEOS film. The use of multiple dielectric films is necessary to fulfill ILD materials design requirements.

The thin PTEOS film is used to form a barrier layer between the metal layer and the porous SACVD film. The PTEOS film is deposited by decomposing tetraethyl orthosilicate (TEOS) in the presence of oxygen through the following reaction.

$$O_2 + Si(OC_2H_5)_4 \rightarrow SiO_2 + volatileorganics \quad (1.5)$$

A RF plasma increases the ion bombardment energy to the reaction surface, increasing the surface mobility of the reactant gases. The result is the deposition of a conformal CVD film at low process temperatures. The higher ion bombardment energy also increases the density of the deposited film making it less susceptible to water absorption. The thin PTEOS film serves as a moisture barrier between the metallization layer and the hygroscopic SACVD film.

The SACVD film does not adhere well to the thin PTEOS film. In order to improve the adhesion between these two films, the surface of the thin PTEOS film is treated prior to SACVD deposition. The treatment is a nitrogen plasma which is ignited by high frequency RF and sustained by low frequency RF. The nitrogen plasma treatment forms oxynitride on the surface of the PTEOS film which aids in SACVD adhesion.

The SACVD film has flow-like deposition and is used for its gap-fill capability. The SACVD oxide is deposited by reacting ozone with TEOS at sub-atmospheric pressures. Because ozone is a highly reactive species, TEOS SACVD deposition can take place at low temperatures. The detailed mechanism for TEOS/O_3 deposition is not completely understood. The most recent model states that upon entering the chamber, the ozone disassociates creating atomic oxygen which then reacts with the TEOS in the following reactions.

$$O_3 \rightarrow O_2 + O \quad (1.6)$$

$$O + Si(OC_2H_5)_4 \rightarrow SiO_2 + volatileorganics \quad (1.7)$$

The flow-like deposition is explained by the fact that the vapor pressure of a droplet of radius *r* follows the Kelvin equation:

$$\log\left(\frac{p}{p_o}\right) = \frac{2\gamma V}{rRT} \quad (1.8)$$

where γ is the surface tension, V is the molar volume, T is the temperature in Kelvin, and p_o is the vapor pressure of a planar surface.[16] The upper corner of the metal line has a higher vapor pressure of reactant species, therefore the deposition rate will be lower. The lower corner of the metal line has a lower vapor pressure of reactant species, therefore the deposition rate will be higher.[17]

Although the gap-fill capabilities of the SACVD are an essential part of the three-film ILD design, it also has many undesirable properties which must be considered. The SACVD film is highly porous which makes it susceptible to water absorption and difficult to planarize controllably. Furthermore, the SACVD deposition process is sensitive to pressure changes. Large changes in pressure can result in particulate contamination through homogeneous nucleation events, therefore the chamber purge and pump down ramp rates are tightly controlled.

In addition to the drawbacks of the SACVD film itself, the SACVD deposition process can cause oxide build-up throughout the chamber. In order to prevent particulate contamination due to oxide build-up, the chamber is in-situ cleaned before any subsequent deposition steps. During the cleaning step, the chamber is filled with C_2F_6 and O_2. Using high frequency RF, a plasma is struck and maintained first with a small showerhead-susceptor spacing, then a large showerhead-susceptor spacing. The small spacing focuses the plasma clean on the surfaces of the susceptor and showerhead, while the large spacing extends the clean to the entire chamber. After the clean gases are purged from the chamber, a thin layer of PTEOS film is deposited to prepare the chamber for further deposition processes. The thin oxide layer ensures that each wafer sees a similar chamber environment.

The thick layer of PTEOS oxide, deposited over the SACVD film, is used to compensate for the deficiencies of the SACVD film properties. The thick PTEOS layer acts as a dense moisture barrier for the porous SACVD film beneath it. The density of the PTEOS film also helps to control material removal during the planarization process. An attempt to planarize the porous SACVD film would result in a nonuniform, uncontrollable material removal rate.

Much like SACVD deposition, the PTEOS film deposition requires an in-situ C_2F_6 and O_2 clean. The PTEOS clean process reduces particulate contamination caused by oxide build-up within the chamber. The clean is followed by a short oxide deposition step which prepares the chamber for the next wafer.

Following ILD deposition, chemical-mechanical polish (CMP) is used to achieve global planarization of the ILD layer. CMP combines the conventional mechanical polishing technique of a rotating platen and wafer holder with the chemical polish of an alkaline-based particulate slurry. In order to effectively planarize an entire wafer, approximately 0.8-1.0 μ of the deposited ILD layer is removed during planarization. The material removal rate is controlled by the Preston equation

$$R = K_p p v \qquad (1.9)$$

where R is the material removal rate, p is the pressure applied to the wafer, v is the relative velocity between the wafer and pad, and K_p is a proportionality constant which is a function of the ILD layer mechanical properties, slurry size and composition, and polishing pad surface.[18] CMP is an effective global planarization method because smaller features are smoothed more quickly than the larger features and the polishing rate is higher at the peaks than the valleys. When properly controlled CMP is capable of 90-95% step height reduction and global planarization on the millimeter scale.[19]

The polishing mechanism of CMP is not yet fully understood. Current CMP knowledge sites a four step material removal process: hydrogen bonds are formed on slurry particles and the wafer surface, hydrogen bonds are formed between the slurry particles and the wafer surface, molecular bonds are formed between the slurry particles and the wafer surface, and oxide bonds are broken at the wafer (or slurry) surface as the slurry particle moves away from the wafer surface.[20] Although understanding is incomplete, a number of conclusions can be drawn from current knowledge: material removal is not based on mechanical abrasion, the formation of H bonds is affected by the presence of water and the pH of the slurry, and the size and composition of slurry particles are important.[21]

Proper choice of polishing pads is essential for CMP. Rigid pads increase planarization distances, but they may also bend the wafer during polishing causing within die ILD thinning. Soft pads increase within wafer uniformity, but they remove equal amounts of material from all wafer surfaces thereby defeating the planarization process. In order to achieve a balance between global and local planarization, a set of two pads is used in CMP, one rigid and one soft.[22]

Because both the platen and the wafer holder are rotating it is difficult to ensure uniform polishing. In order to guarantee uniform polishing across the wafer surface every point on the wafer must travel at the same relative velocity to the platen, there must be a uniform distribution of slurry across the wafer surface, and the wafer should be symmetrical. Although uniform slurry distribution is difficult to achieve because the slurry always arrives at the wafer edge first, the other two requirements are easily met. All wafers are symmetric except for the notch edge and platen movement patterns have been designed to ensure that every point on the wafer sees the same polish pad velocity.[23]

Finally, slurry and polished material can build-up on the polishing pad, reducing the pad lifetime and degrading the material removal rate. In order to reduce this effect, the polishing pad is conditioned regularly. In this manner, the pad is keep free of debris and retains its original roughness longer.[24]

Chapter 2

Particulate Contamination

2.1 Yield Impact

In addition to the film qualities described in Chapter 1, it is important that the ILD layer have low defect density. A defect is defined as a localized non-uniformity within the film which may be detrimental to circuit performance. Defect density can greatly impact the die yield of a wafer. For identifiable and randomly distributed defects, yield is roughly related to defect density through the following relationship

$$Y = e^{-DA} \tag{2.1}$$

where D is the defect density of a wafer and A is the active area of a single die.[25] Assuming that each ILD layer is a critical level or major defect generator, the yield of a microprocessor with N ILD layers each with defect density D would be

$$Y = e^{-NDA} \tag{2.2}$$

As shown above, multilevel metallization technology dramatically increases the yield impact of the ILD layer, therefore it is imperative that the ILD film relatively defect-free. Particles are one of the largest known contributors to ILD defects. A particle larger than one tenth the area of the technology's critical dimension can adversely impact yield. The current 0.35 μ technology has a particle size tolerance of 0.035 μ diameter.

2.2 Yield Loss

Yield can be affected by particles in a variety of ways. A few of the most obvious concerns are discussed. A particle which falls on metal lines before ILD deposition can be particularly harmful. A large particle can bridge two metal lines, preventing gapfill and

creating a void beneath the particle. As explained previously voids are extremely detrimental to product reliability. During subsequent processing steps, the void can become filled with contaminants, cause metal etch-through, and many other undesirable events. If the particle is metallic, there are many other issues to consider. A metal particle which spans two metal lines may result in a short between the metal lines. Furthermore, if a metal particle is large enough to span the post-polish ILD layer it can also cause a short between metal layers.

During burn-in an integrated circuit is repeatedly thermal cycled to temperatures much higher than process temperatures. The ILD layer experiences a great deal of physical stress during this process. Because a particle is a non-uniformity within the film, it disrupts the uniformity of the stress fields creating focal points. Particles become weak points within the ILD layer at which plastic deformation and crack propagation is likely to occur. Because failures are more likely to occur after prolonged use rather than during initial testing of the circuit, particles in the ILD layer pose a reliability issue.

Particles can also be an issue during planarization. A particle embedded in the film can be pulled out or etch more quickly than the rest of the ILD layer during CMP. When a particle is pulled out of the film by the motion of the polisher, a hole is left in the ILD layer. The hole introduces a local variation in the thickness of the ILD film. Similarly, if the particle material etches more quickly than the ILD layer, ILD thinning occurs near the particle site. The ILD layer is no longer globally planar. ILD thickness variations can cause metal to collect in lower topography areas. If not completely removed during metal polish, the metal-filled valleys can form shorts between metal lines during subsequent metallization steps.

The via etch process is also vulnerable to particle contamination. A particle embedded in the ILD layer near an intended via location can greatly complicate via etching. If the

etch rate of the particle varies from that of the ILD layer, overetch or underetch can occur. Overetch can result in metal line breakthrough, where as under-etch can lead to insufficient metallization or loss of contact. Both cases are undesirable and may lead to die kill or reliability issues.

Chapter 3

Particle Generation, Deposition, and Adhesion

3.1 Generation

Despite efforts to eliminate particles from the manufacturing environment, generation takes place on all levels including cleanroom, wafer, and tool. The particles vary greatly in size, shape, and composition depending the source. Mechanically generated particles are often quite large, where as particles created through chemical reactions are usually less than 0.5 μ. As a result, the particle size distribution tends to be bimodal, with particle sizes clustered around 0.2-0.3 μ and 10-20 μ. Smaller particles are generally more abundant than larger particles.[26]

3.1.1 Cleanroom Environment

In a Class 1 cleanroom there is an average of 1 particle (0.12 μ or greater) per cubic foot in the process area, however particle levels can fluctuate locally depending on equipment, process, cleanroom design, and human presence. People are responsible for one of the most variable particle contributions. The particle generation rate for the average person is estimated at 200-300 counts/s for particles larger than 0.3 μ. Assuming an air flow velocity of 1 ft./s and 1 $ft.^2$ area per person, in a class 1 cleanroom, the particle density in the immediate vicinity is the equivalent of a class 100 cleanroom.[27] As a result, when wafers are handled by people, the wafer is exposed to a class 100 cleanroom environment.

3.1.2 Improper Wafer Handling

Proper wafer handling is essential in maintaining clean wafer surfaces. All wafer motions are considered wafer handling including cassette-cassette wafer transfers, loading and unloading the tool, and lot box carrying. Improper wafer handling techniques can cause wafer damage such as scratching or chipping which result in particle generation.

3.1.3 Process Equipment

Process equipment is another large source of particles within the cleanroom. There are several mechanisms for particle generation within a tool. Among them are mechanical wear, chemical reactions with chamber components, and build-up of deposition materials.[28] Repetitive valve or robot motions can result in mechanical abrasion of tool components. Although there are no visible signs of wear, a substantial number of particles are generated by this mechanism.[29] Chemicals introduced to the chamber for wafer processing may also react with the chamber components creating unwanted products which can be detrimental to wafer cleanliness. Furthermore, process chemicals can adhere to chamber surfaces causing build-up. When such a layer reaches a critical thickness, flaking occurs increasing the particulate contamination of the chamber.

3.2 Deposition

In order to impact yield, generated particles must be transported to the wafer's surface. The total deposition velocity of particles, V, on the wafer's surface can also be defined as

$$V = \frac{J}{C_o} \tag{3.1}$$

where J is the flux of particles to the wafer surface and C_o is the concentration of particles near the wafer surface.[30] Significant particle transport mechanisms include gravity, diffusion, electrophoresis, and thermophoresis. The total particle deposition velocity, V, is the sum of the velocity contributions of these mechanisms, such that

$$V = V_G + V_D + V_E + V_T \tag{3.2}$$

where V_G is the gravitational component, V_D is the diffusion component, V_E is the electrophoresis component, and V_T is the thermophoresis component.[31] A brief description of each component of the deposition velocity follows.

3.2.1 Gravitational Forces

The gravitational force, F_G, on a spherical particle is defined as

$$F_G = \frac{4}{3}\pi r^3 \rho \tag{3.3}$$

where r is the particle radius and ρ is the density of the particle. The gravitational component of the deposition velocity, V_G, for a particle is determined by equating the gravitational force with the Stokes drag force acting on the particle.[32] For a constant pressure, the deposition velocity attributed to gravitational forces increases with particle size. As pressure decreases, Stokes drag force decreases causing V_G to increase.

3.2.2 Brownian Motion

Brownian motion governs the interactions between a particle and the molecules surrounding it. As gas molecules bombard a particle, differences in the magnitude and direction of the collisions cause a net push in one direction. Because the motion of the bombarding gas molecules is random, the sequential movements of the particle are also random.[33] As the particle size decreases it becomes increasingly susceptible to collisions from surrounding molecules, therefore Brownian motion is the dominant mechanism of transport for small particles.[34]

3.2.3 Electrophoresis

Electrophoresis is motion of electrically charged particles in an electric field. Unlike the previously mentioned mechanisms, electrophoresis is a conditional mechanism, that is it does not apply to every case. Electrophoresis only serves as a transport mechanism when the particles are electrically charged and an electric field is present. Transport is controlled by Coulomb forces defined as

$$F_C = \frac{q^2}{4\pi\varepsilon_o\varepsilon l^2} \tag{3.4}$$

where q is the charge, ε is the dielectric constant of the surrounding medium, ε_0 is the

dielectric constant of free space, and l is the distance between charge centers. Depending on the charge character Coulomb forces can be either attractive or repulsive forces. Attractive forces are responsible for particle deposition.[35] Electrophoresis increases the velocity of particle deposition by V_E. Electrophoresis plays a greater role in smaller charged particles, than in larger charged particles. Gravitational forces continue to dominate transport of larger particles.

3.2.4 Thermophoresis

Thermophoresis particle motion caused by a thermal gradient. The increased kinetic energy of gas molecules at elevated temperatures creates a net force on the particle pushing it towards the lower temperature region.[36] As a result, particles travel down the thermal gradient. Depending on the relative temperature of the wafer and its environment, particles are transported to or from the wafer surface. A wafer that is at a lower temperature than its environment attracts particles, causing them to be deposited on the surface. Thermophoresis increases the velocity of deposition by V_T. The effects of thermophoresis increase at low pressures and small particle sizes.

3.3 Adhesion

If a particle transported to the wafer surface is to impact yield, it must adhere to the wafer surface. Adhesion forces for dry, uncharged particles are dominated by Van der Waals forces and electrostatic contact induced electrical double layer forces, although gravity can play a role in large particle adhesion. The adhesion of charged insulating particles is further affected by electrostatic image forces.

3.3.1 Gravitational Force

The gravitational force acting on a single particle of radius r is defined in equation 3.3. Gravitational forces only play a significant role in the adhesion of extremely large

particles (on the order of tens of microns in size). For the most part, other adhesion forces are so large that adhesion due to gravitational forces can be neglected.[37]

3.3.2 Van der Waals Forces

Van der Waals forces are intermolecular electrostatic forces with three components: dipole-dipole interactions, dipole-nonpolar interactions, and interactions between nonpolar bodies or dispersion forces. The non-polar dispersion forces, originating from quantum mechanical polarization, tend to dominate the adhesion forces.[38] The Van der Waals forces during particle deposition can be estimated as a summation of the interactions between individual atoms in the particle and the wafer. The geometry of such an interaction is approximated as a sphere interacting with a plane. Van der Waals forces, F_{VdW}, can be described in terms of the Hamaker constant as

$$F_{VdW} = \frac{rH_{123}}{6z^2} \quad (3.5)$$

where r is the particle radius, z is the distance between the particle and the wafer, H_{123} is the Hamaker constant of the system (a particle of material 1, on a wafer of material 2, in a medium 3).[39] The Hamaker constant can be calculated using material properties. The values of the constant include imaginary components and show frequency dependence. For the most part the Hamaker constant is positive indicating that Van der Waals forces are attractive. At small distances and small particle sizes, Van der Waal forces are large enough to cause elastic or plastic deformation of the particle. Particle deformation increases the contact area between the particle and the wafer, therefore the adhesion force increases with particle deformation. The viscoelastic nature of many particle materials, results in a time dependent adhesion force.[40]

3.3.3 Electrostatic Contact Induced Electrical Double Layer Forces

When two different materials are placed in contact differences in local energy states and work functions of the two materials cause electrons to flow between the two materials until an equilibrium state is reached. The difference in potential, defined as a contact potential of the two materials, creates a double layer charge region at the interface. In semiconductors, the double layer charge region can extend 1 μ or further into the wafer.[41]

3.3.4 Electrostatic Image Forces

Electrostatic image forces can increase adhesion of small, charged particles. The electrostatic image force is the same as the Coulomb force defined in equation 3.4. When the particle is on the wafer surface, the distance between charge centers becomes $2r$. The charge of the particle, q, can be written

$$q = 4\pi\varepsilon_o r^2 EC \tag{3.6}$$

where C is capacitance and E is the electric field. The image force becomes

$$F_I = \frac{\pi\varepsilon_o r^2 E^2 C^2}{\varepsilon} \tag{3.7}$$

In conductors, the excess charges are balanced by contact flow, however in insulators contact flow does not occur, therefore the attraction between the charges becomes significant.[42]

Chapter 4

ILD Deposition Tool

4.1 Loadlock and Chamber Components

A modified AMAT Precision 5000 was used for ILD deposition. As shown in figure 4.1, it is a cluster tool is made up of four CVD chambers, a loadlock, a storage elevator, a robot, and a cassette handler. Slit valves are used to isolate the loadlock from the chambers, as well as the external environment.

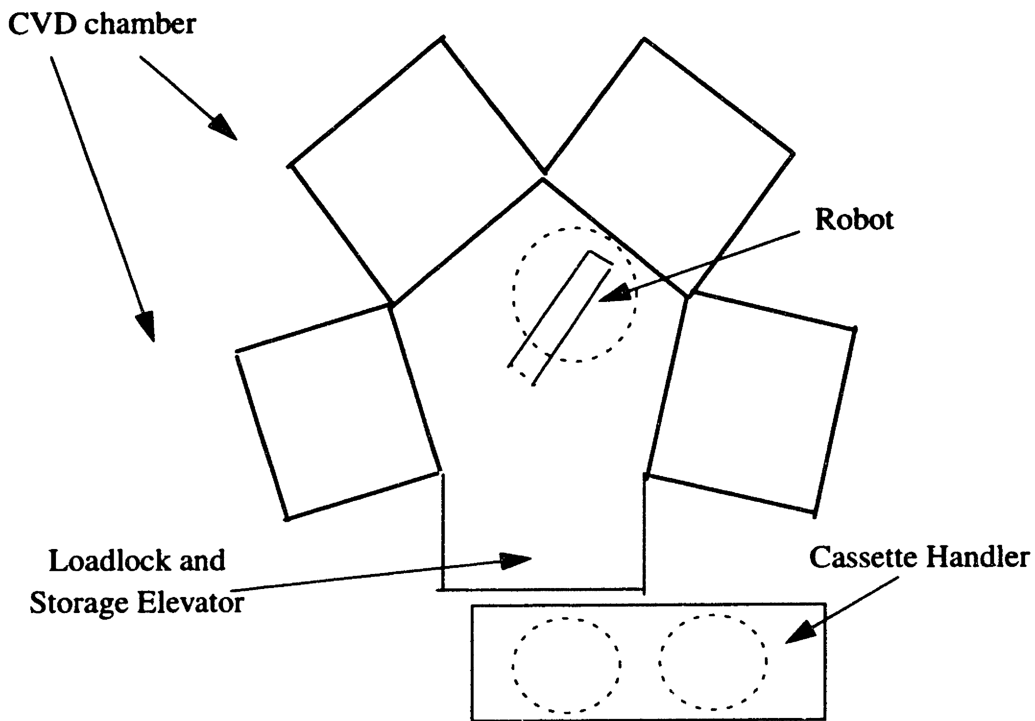


Figure 4.1: Multichamber ILD deposition tool.

The aluminum alloy loadlock is used to transition wafers between the cleanroom environment and the chamber environment. The loadlock also helps to confine process gases that may escape during transfer. Within the loadlock are two vents and a nitrogen purge. The purge flows continuously during processing, while the position of the vents are

varied depending on the loadlock pressure which is desired. Diffusers are located on each of the vents to help reduce motor vibrations.

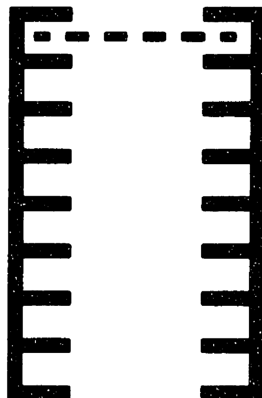


Figure 4.2: Wafer in top slot of eight slot wafer storage elevator

The storage elevator and robot are located in the loadlock. A cross-section of the storage elevator is shown in figure 4.2. The storage elevator has eight wafer slots, divided into two groups of four. The slots, which are open in the center, are made from aluminum alloy. A robot is used to transfer wafers from the elevator to the chambers.

The robot arm is made from aluminum alloy and the robot blade is made from stainless steel. As shown in figure 4.1, the storage elevator is located between the robot and the cassette handler. During wafer loading and unloading the robot reaches through the storage elevator to the cassette to pick up the wafers. As the arm passes back through the storage elevator, the wafers are released. The storage elevator serves an a holding area for the wafers during process.

Each CVD chamber is a single-wafer, parallel plate reactor. The wafer is loaded onto the wafer lift fingers, lowered onto the susceptor, and remains on the susceptor during deposition. The reactant gases flow through the lid. The blockerplate and showerhead serve to distribute the gas flow and maintain a uniform deposition rate across the surface of the wafer.

Both the showerhead and blockerplate are made of aluminum alloy. All areas on the showerhead except the inner diameter of the holes and the rim, which contacts the gas box mounting plate, are anodized to minimize corrosion. The blockerplate is not anodized. The showerhead and blockerplate are attached to the gas box mounting plate with stainless steel screws. The screws are evenly spaced at six locations around the circumference. The blockerplate also has three more even spaced radial screws positioned closer to the center. During PTEOS deposition the gas box mounting plate, blockerplate, and showerhead are RF hot.

The upper surface of the susceptor is made of anodized aluminum and sits on the ceramic isolation arm. The susceptor is grounded by a braided aluminum grounding strap. During ILD process, movement of the susceptor controls the distance between the showerhead and susceptor. Just below the susceptor is the ceramic wafer lift hoop and wafer lift fingers. The fingers can be raised and lowered through holes in the susceptor and are used to support the wafer during transfer.

4.2 Cleanroom Set-up and Mechanical Sequence

The loadlock and its peripheral cluster of CVD chambers are located in the service area at the rear of the tool, while the cassette handler and I/O slit valve open into the process area at the front of the tool. In order to confine the dirtier maintenance and repair procedures used in the service area from the cleaner air of the process area, the service area and process area are separated by paneling. The opening of the tool and the cassette handler are further enclosed by paneling, as shown in figure 4.3. An air filter known as the hepa filter sits above the paneled area. The filter helps to clean the air near the face of the tool, while the blowers positioned above the tool opening serve to maintain laminar air flow.

The hepa also helps to balance positive air flow from the process area.

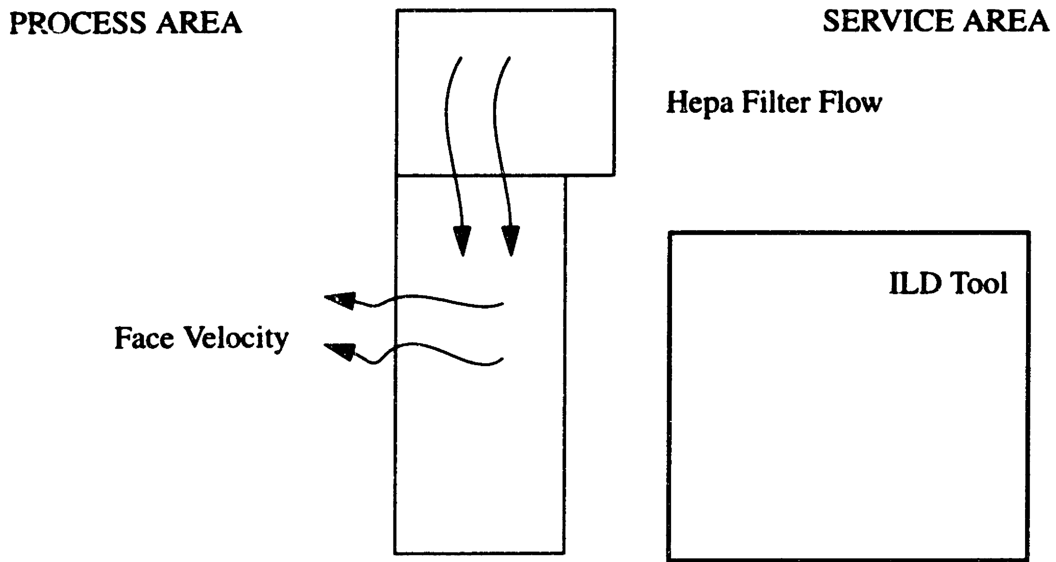


Figure 4.3: Tool enclosure which separates the process area from the service area.

The tool is manually loaded from the process area by a manufacturing technician using the ergo loader (not shown in figure 4.1) in the cassette handler. Once the cassette is loaded into the cassette handler mechanism, the robot is responsible for all wafer movement within the tool. The I/O slit valve is opened and the wafers are transferred from the cassette to the storage elevator by the robot. The storage elevator has eight wafer slots, however only four are used at a time. Four wafers are introduced to the storage elevator beginning with the uppermost slot. The entire loadlock and storage elevator are then pumped down. During process, each wafer is transferred from the storage elevator to a CVD chamber beginning with the uppermost slot. In the chamber, a thin PTEOS deposition, plasma treatment, and SACVD deposition take place. During the in-situ SACVD clean step, the wafers are transferred to the lower four slots of the storage elevator beginning with the fifth slot. After the SACVD chamber clean has been completed, the wafers are returned to the process chambers. Once again the wafer transfer sequence begins with the uppermost wafer and moves toward the bottom of the storage elevator.

After the thick PTEOS deposition, the wafers are returned to the storage elevator filling the top slot first. The loadlock is vented. Finally, the robot returns the fully processed wafers to the cassette, emptying the storage elevator from top to bottom.

Chapter 5

Analysis Techniques for Particulate Contamination

5.1 Metrology Tools

5.1.1 Surfscan 6200

The Surfscan 6200 is a metrology tool which uses light scattering to detect defects on the surface of the wafer. A diagram of the scanning technique used to detect defects is shown in figure 5.1. A 90 μ spot size laser beam with incident angle of 90° is moved in a linear path back and forth across the wafer surface while the wafer is moved perpendicular to the laser motion. When the laser beam encounters a defect on the wafer, the light is scattered away from the point of incidence. The scattered light is collected by the tool's optical system which converts it to an electrical pulse. If the signal is large enough, the tool interprets it as a defect. The Surfscan 6200 is able to detect particles as small as 0.09 μ depending on system noise.

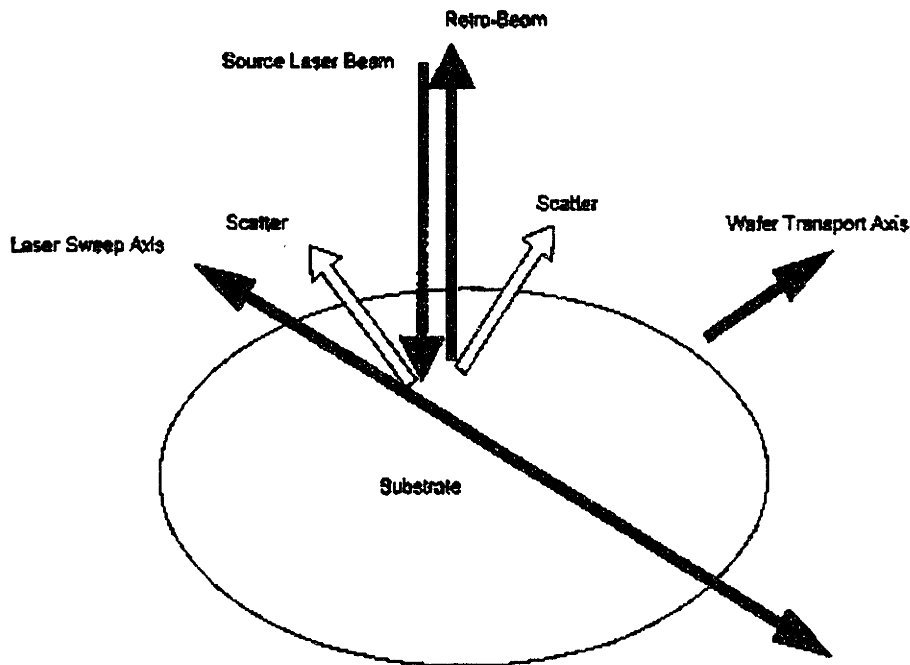


Figure 5.1: Surfscan 6200 scanning method.[43]

The tool's software creates a map of the wafer indicating the location and size of defects on the surface of the wafer. The defects are also counted and sorted by size into bins. The limits of the bins vary and are determined by the user. As shown in figure 5.2 the defect count and size information are displayed on the screen, as well as the wafer map. Very large defects or a great number of defects close to each other are interpreted as area defects. Area defects are counted separately and are not included in the point defect total.

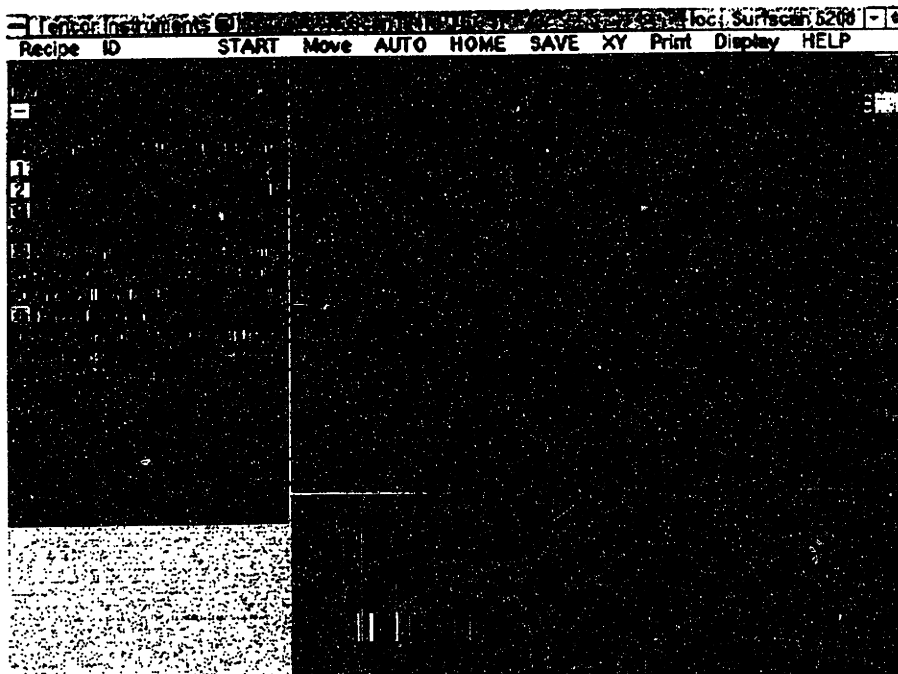


Figure 5.2: Wafer map from Surfscan 6200

In this study, the Surfscan 6200 is used to detect particles on bare-silicon and PTEOS oxide deposited wafers. In both cases, a recipe was used with defect bins defined as 0.16-0.5 μ, 0.5-2.0 μ, and 2.0-100 μ. The wafer maps were printed with the notch at 6 o'clock, unless otherwise specified.

5.1.2 Surfscan 7600

The Surfscan 7600 is also a metrology tool used to detect defects, however the Surfscan 7600 is specifically designed to measure defects on patterned wafers or wafers with high surface roughness. The Surfscan 7600 uses light scattering to detect the wafer

pattern, as well as defects. A diagram of the Surfscan 7600 scanning technique is shown in figure 5.3. A laser with a 25 μ diameter beam scans the wafer linearly at a 10° incident angle, while the wafer moves in the transverse direction. At a 10° angle the spot size of the laser becomes 25 μ by 140 μ. Scattered light is collected in two locations: the pattern viewing channel and the particle viewing channel. The pattern viewing channel located just above the wafer is at a 90° angle. Because the amount of light scattered by the pattern is greatest at this angle, the viewing channel is able to identify the pattern signal with very little noise. The particle viewing channel is located to the side of the wafer, at a 10° angle. Lower angle collection minimizes light scattering from the pattern and enables the Surfscan 7600 to detect particles as small as 0.15 μ. The two scattered light signals are combined, filtered, and analyzed. Periodic signals are interpreted as the wafer pattern, while stray signals are considered defects.

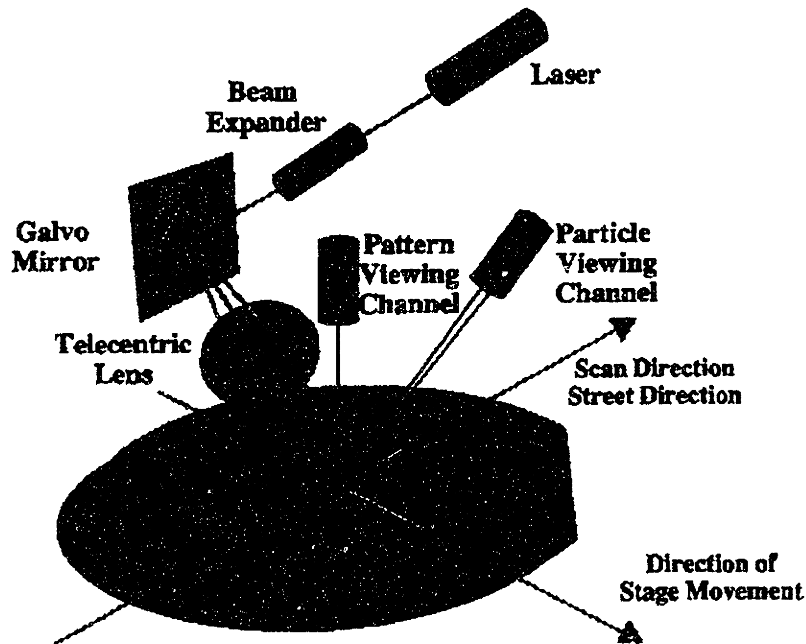


Figure 5.3: Surfscan 7600 scanning method [44]

The Surfscan 7600 uses these electrical signals to generate a wafer map and defect count for each wafer. As shown in figure 5.4, the wafer map shows the location of each defect, but not the size. Unlike the Surfscan 6200, the Surfscan 7600 does not place the defects in size bins, nor does it differentiate between point defects and area defects.

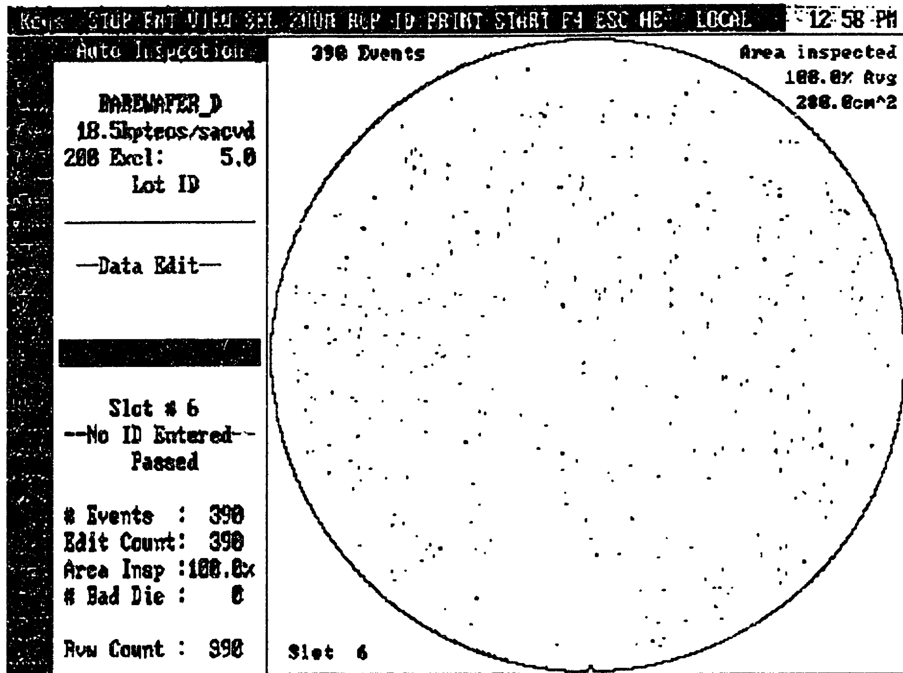


Figure 5.4: Wafer map from Surfscan 7600

Although the Surfscan 7600 is designed to measure patterned wafers, for this study the Surfscan 7600 was used to scan bare silicon and ILD deposited wafers. The roughness of SACVD oxide makes it difficult to detect particles using the Surfscan 6200. Because the Surfscan 6200 misinterprets the roughness of the film as particles, there are a great number of false detections. On the Surfscan 7600 the same scanning techniques which make it possible to resolve the particles in a patterned wafer make it possible to detect defects in a film which contains rough SACVD oxide. For consistent measurements, the bare silicon wafers were also pre-scanned using the Surfscan 7600 prior to deposition.

5.2 Particle Test Fires

Particle test fires are used to monitor the particle performance of the ILD deposition tool. Bare silicon wafers are transferred to an empty cassette using a vacuum wand. The wafer is deposited with the ILD film and then scanned for particles using a Surfscan 7600. The ILD tool particle monitor is wafer-based, meaning the frequency of the monitor is determined by the wafer throughput of the chamber. The particle count for each chamber is verified every few hundred wafers.

In a healthy tool, particle counts should be low. The particles which are present should be randomly distributed across the surface of the wafer. High particle counts or clustered particles are a sign that there is something wrong with the tool. Particle counts are used as the primary indicator of tool cleanliness, while the location of the particles on the wafer is used for tool diagnosis purposes. An upper limit is set for the test fire particle count. If the test fire particle count exceeds this limit the chamber is considered out of control. Production is stopped on the chamber until the particle count is reduced.

After a particle out of control, repeated test fires must show that the particle count of the chamber is below the upper particle limit before it can be used for production. Repeated test fires are needed to ensure that the particle source has truly been eliminated. Many particle sources generate intermittent particle excursions, therefore a single test fire does not sufficiently ensure that the particle levels in the tool are acceptable.

Trends in test fire particle counts can help determine the state of the tool. Sudden changes in particle counts can often be correlated with events recorded in workstream to help determine the particle source. Slow changes in particle levels can also be monitored and correlated with changes to the tool. Evaluating trends and possible sources is part of the particle reduction process.

5.3 Particle Troubleshooting

5.3.1 GFA Analysis

The location and density of the particles on the test fire wafer can be useful in determining the source of particles. When particles are focused in a specific area of the wafer, that area is called a gross failure area (GFA). When combined with knowledge about the wafer's orientation during processing, the GFA can reveal useful information about the particle source. While troubleshooting particle excursions, the position of the notch can be defined by the notch-alignment tool. Notch-alignment is usually defined by the hours on a analog clock. For instance, 12 o'clock is defined as the notch straight up. Following notch-alignment, the orientation of the wafer is known and can be followed through each process step. The location of the particles can be correlated with particle producing components in that location. For example, if the wafer is notch-aligned to 6 o'clock and there is a GFA opposite the notch, the source of particles could be the slit valve or the slit valve o-ring.

5.3.2 Wafer Maps

Saved wafer maps from each test fire can be useful for determining particle sources. In many instances, a GFA occurs even if the particle count is not out of control. When a chamber does go out of control, the saved wafer maps can be reviewed to determine when the problem started. The date on which the particles were first generated can then be correlated with the events recorded in workstream. Saved wafer maps are also helpful in recognizing sudden, strong GFA appearances. Intermittent GFAs can also be evaluated more readily. By comparing saved wafer maps, it is possible to determine if the particle source is the same as the last out of control or if the particle source has changed.

5.3.3 Scanning Electron Microscope (SEM) and Energy Dispersive X-ray Analysis

Once an out of control tool or repeated GFA is identified, more information about the source of the particles can be learned from scanning electron microscope (SEM) and

energy dispersive X-ray (EDX) analysis. Pictures from the SEM can help to determine the exact size and shape of the particles. The surface roughness of the particles can also add information about its source. For example, a smooth, perfectly spherical particle was most like formed by homogeneous nucleation, where as a large jagged particle may have been formed through mechanical abrasion. A picture from the SEM can also be used to differentiate between scratches and particles, an area where the Surfscan 7600 is deficient.

Furthermore, the SEM can be used to determine the location of the particles in the film. A picture of the surface of the wafer will reveal if the particle is embedded in the film or sitting on the surface. If the particle is embedded further analysis can be completed by cross-sectioning the wafer. A SEM cross-section will show exactly where in the ILD layer the particle is located, whether it be in one of the films or between films.

EDX can be used to provide compositional analysis of the particles. Given a particle's composition, a list of possible sources within the tool can be generated. By systematically isolating each of the possible particle sources, the root cause of particles can be pinpointed and eliminated.

5.3.4 Tool and Recipe Partitioning

Mechanical partitioning and recipe sectioning are also used to determine particle sources. Mechanical partitioning is used to isolate mechanical motions of the tool. Silicon test wafers are pre-scanned and then put through a sequence of mechanical motions within the tool. The sequence models the motions of the tool during process, isolating each movement. After mechanical partitioning, the wafers are post-scanned and the number of particles added by each movement is determined. A particle source is sought in the motion which adds the most particles or produces a GFA which matches the out of control GFA.

Recipe sectioning is similar to mechanical partitioning in that it too helps to isolate the source of particles. Rather than isolating a particular motion, recipe sectioning isolates the particle source to a particular process step. Silicon test wafers are pre-scanned, then run through the dirty chamber progressively adding a process step to each wafer. The wafers are post-scanned to determine the number of particles added by each process step. Like in mechanical partitioning, a particle source is sought in the process step which adds the most particles or duplicates the out of control particle GFA.

Chapter 6

Investigated Sources of Particulate Contamination

6.1 Test Wafer Reliability and Wafer Handling

Test wafers introduced to the process line are required to meet cleanliness specifications determined by the manufacturer. These standards are chosen such that test fire particle levels will not be statistically affected by the initial particle levels of the test wafer, therefore the test fire wafers are not measured prior to use in the ILD area. Ideally, test wafer cleanliness does not deteriorate between introduction to the process line and use in a test fire.

In order to evaluate the quality of test wafers in the process area, wafers were taken from several cassettes in the process area and scanned using the Surfscan 7600. Over 3 days a total of 28 wafers were scanned. Out of control wafer maps were also reviewed for repeated GFAs.

Of the 28 test wafers scanned, the maximum number of particles found on a single test wafer was four. Although the number of wafers scanned cannot statistically verify that test wafers in the process area are not of poor quality, it does suggest that it is not a regular occurrence.

The review of out of control wafer maps for one month revealed that several out of control test wafers had long, narrow, localized defects much like the one shown in figure 6.1. Of the 58 out of control maps, 18 of the wafer maps had this GFA. Using these 18 wafer maps, the number of particles which were not part of the GFA was estimated and subtracted from the total particle count of the test wafer. Excluding the particles in the GFA substantially reduced particle counts for each wafer, such that only 8 of the 18 wafers

were still out of control. The GFA seems to have caused 17% of particle out of controls for the month.

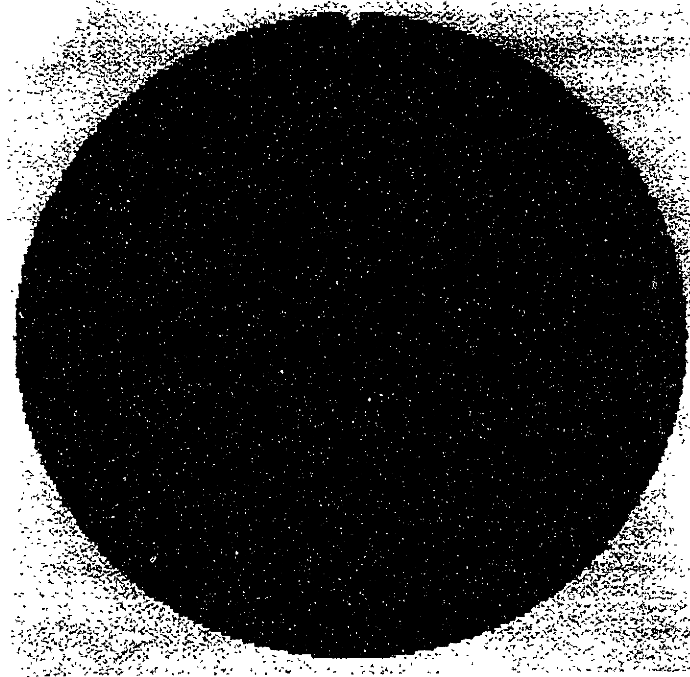


Figure 6.1: Scratch-like GFA on test wafer surface

The GFA is not a known characteristic of the ILD process, rather it is attributed to scratches created during test wafer transfer with a vacuum wand. Thus, the particle performance of the tool is complicated by wafer handling issues. Scratches not only damage the wafer surface, they also introduce particles to the wafer surface. Product wafers are not handled using the vacuum wand, therefore, in this case, particle generation caused by scratches does not pose a yield concern. Nevertheless, the validity of the particle monitor is questionable. Improper handling was shown to affect 31% of the total particle out of controls for a month causing 17% false reports. As a result, valuable time and materials were wasted chasing particle sources that did not exist.

6.2 Cleanroom Microcontamination

The air flow at the face of the tool and the proximity of contamination sources control

particle contamination levels during loading and unloading. Ideally, all extraneous sources of particulate contamination should be eliminated from the loading area, including gowned technicians, areas of stagnant air, and geometries which collect particles. In reality, these sources cannot be eliminated. To prevent particulate contamination from being deposited on the wafer during loading and unloading, air flow near the tool face must be controlled. Ideally, there should be no net air flow at the tool face. The process area should have a laminar downward flow. The resulting positive pressure of the process environment should be balanced by the parallel downward flow of the tool's hepa filter. As shown in figure 4.3, this type of flow prevents process area and human contaminants from being deposited on the wafers and tool level contaminants from being expelled into the process environment. In addition, a constant flow is maintained through the ergo loader and cassette handler reducing particulate build-up.

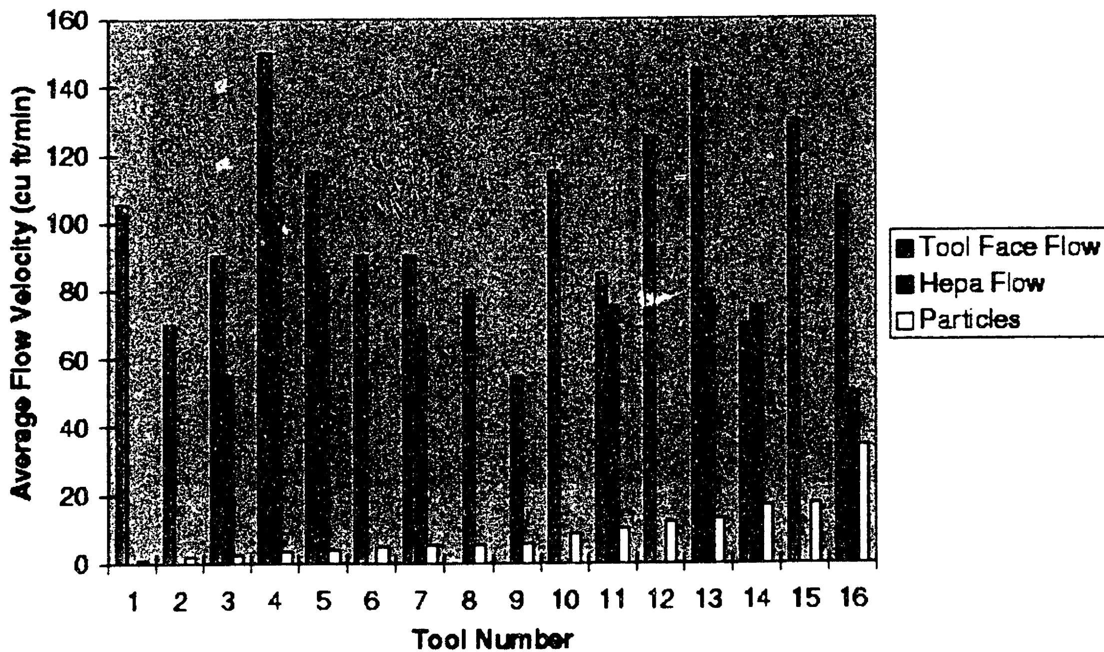


Figure 6.2: Tool face and hepa flows

An microcontamination evaluation of the ILD process area was completed. Among other procedures, the audit included flow velocity measurements of the hepa filter and tool face for each tool, an inspection of the paneling which separates the process area from the maintenance area, and a visual inspection of the general cleanliness of the loading area. the hepa and tool face velocities were measured using a windvane anomometer.

As shown in figure 6.2, it was found that the flow velocities varied greatly from tool to tool. The median particle counts for each tool during the week of the audit are also shown in figure 6.2. No correlation was seen between hepa or tool face velocities and particle counts. Nonetheless, the process area and hepa filter velocities for three tools were balanced such that the face velocity of these three tools was zero. The median weekly particle counts for these three tools over a 2 month period are shown in figure 6.3. As shown, balancing the face velocity of these tools did not dramatically reduce median particle counts. No correlation was seen between particle counts and flow velocities.

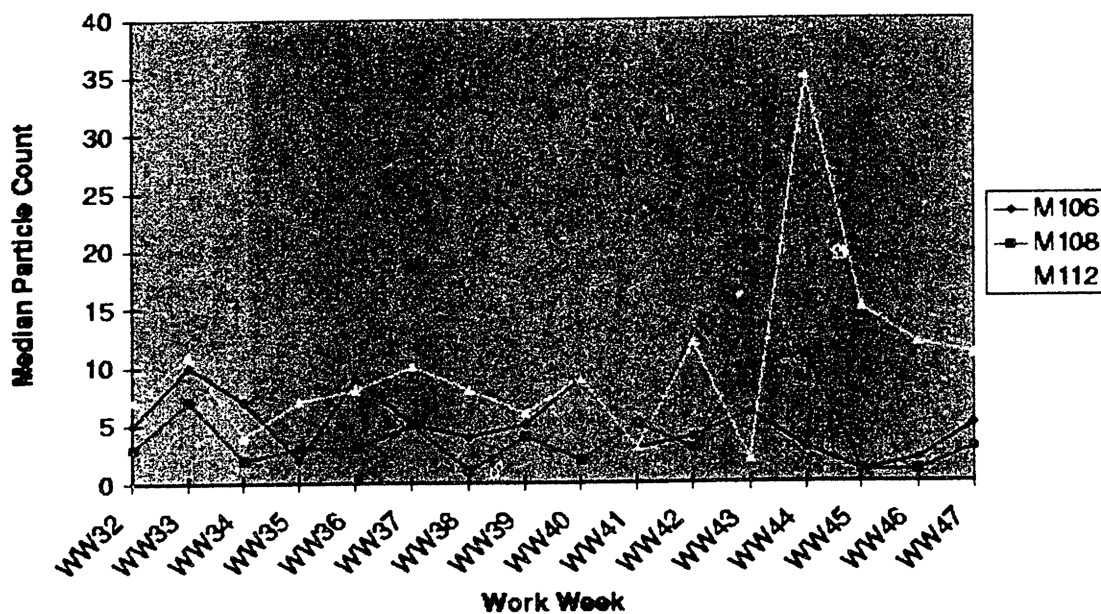


Figure 6.3: Median particle counts for flow-balanced tools

The paneling inspection revealed that the side panels used to isolate the AMAT tool loading area from the maintenance were loose. Several of the screws which are used to hold the panels in place were either loose or missing. Isolation of the loading area is important to control the flow across the wafer surface. Loose side panels may result in turbulence due to trapped or misguided air flow. Non-laminar flow is more likely to stir-up particles, depositing them on the wafer surface. In order to remedy the situation, the screws were replaced or properly tightened. No correlation was seen between paneling changes and median particle counts.

During the visual inspection of the loading area, a white powdery build-up, most likely composed of silicon oxide, was seen on many of the mini-environment ionizer tips. The ionizer tips are located directly above the ergo loader where particles dislodged from the ionizer tips can fall directly on the wafer surface. The ionizers were installed with the tool to eliminate the potential for electrostatic discharge (ESD). It was believed that ESD hindered the performance of process tools. The ionizers were meant to control ESD. After noting the particulate build-up, the calibration of the ionizers was checked. None of the mini-environment ionizers were calibrated. Improper calibration caused the ionizers to attract and collect particles. The ionizer tips were cleaned at the same time as the three tool face velocities were balanced. Once again, no correlation was seen between ionizer tip cleanliness and particle performance.

6.3 Backside Particles

The backside of the wafer is in direct contact with several surfaces during the ILD deposition process including the wafer blade, storage elevator, lift fingers, and the susceptor. While in contact with these surfaces, particles which may have been collected during the manufacturing process can adhere to the wafer's backside. Depending on the strength of adhesion, the particles may be transferred to the front of the neighboring wafer

via (1) flow through the loadlock and the storage elevator caused by N_2 purge/vent, open and closing chamber slit valves, or open and closing the I/O slit valve, (2) mechanical vibrations caused by transfer from the storage elevator to the cassette, or (3) physical backside to frontside contact during cassette handling.

6.3.1 Verification of the Presence and Transfer of Backside Particles

Because the Surfscan 6200 uses light scattering to detect particles, it can only measure particles on a well-polished surface. In order to study backside particles, it was necessary to flip the wafer over such that the polished side of the wafer became the backside. In order to quantify the particles which were transferred to the wafer's frontside, a test wafer accompanied the deposited wafer through the mechanical motions of transfer to and from the storage elevator.

Two test wafers were notch-aligned to 6 o'clock and prescanned using the Surfscan 6200. Pre-scan particle counts were less than 15. Using a vacuum wand, the wafer nearest the front of the cassette was turned so that its polished side faced the back of the cassette. The wafers were then notch-aligned again to 6 o'clock. The wafers were loaded into the tool and the wafers were transferred to the storage elevator filling the uppermost slot first. The upper wafer was polished side down and the lower wafer polished side up. The lower wafer remained in the storage elevator while the unpolished side of the upper wafer was deposited with ILD film. Following the deposition, the wafer was transferred back to the upper slot in the storage elevator. Both wafers were then transferred back to the cassette uppermost slot first.

The movement of the test wafers in this study closely follows wafer movement during process. The greatest deviation from process is that when the upper wafer is returned to the storage elevator there is already a wafer in the slot beneath it. Particles which fall from the backside of the wafer during return to the storage elevator will be deposited on the

wafer beneath it. In contrast, during process, when a wafer is returned to the storage elevator particles which drop from its backside fall onto the floor of the storage elevator.

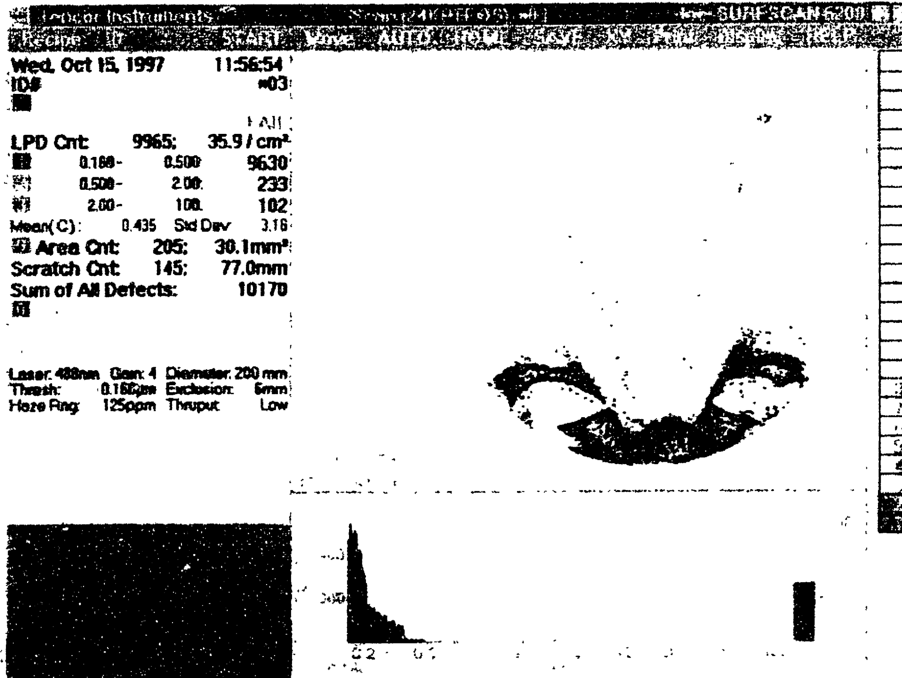


Figure 6.4: GFA seen on backside of the ILD-deposited wafer..

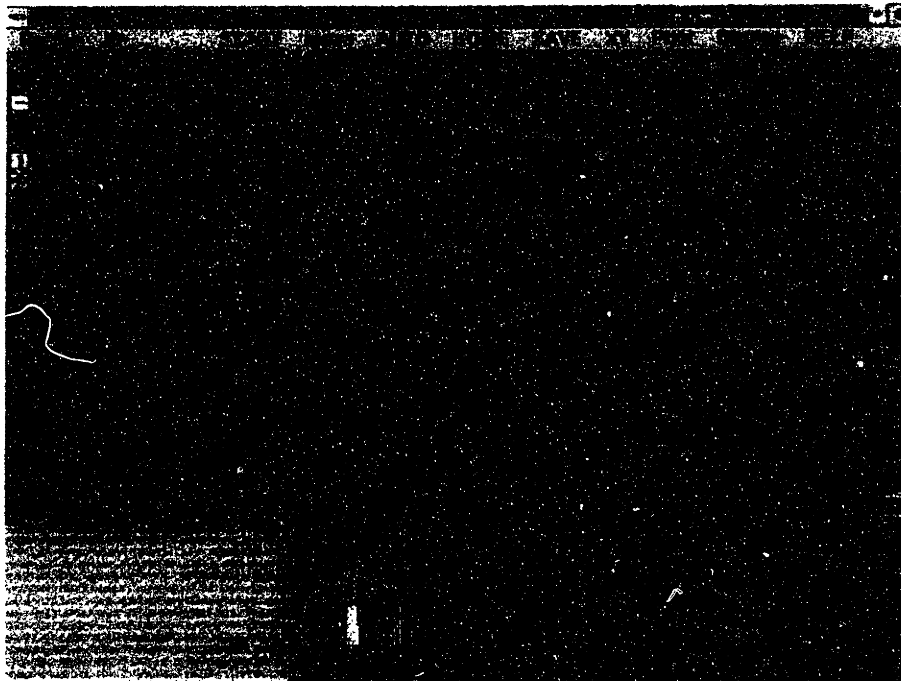


Figure 6.5: Particles which were transferred to from the backside of the ILD deposited wafer to the front of the collection wafer.

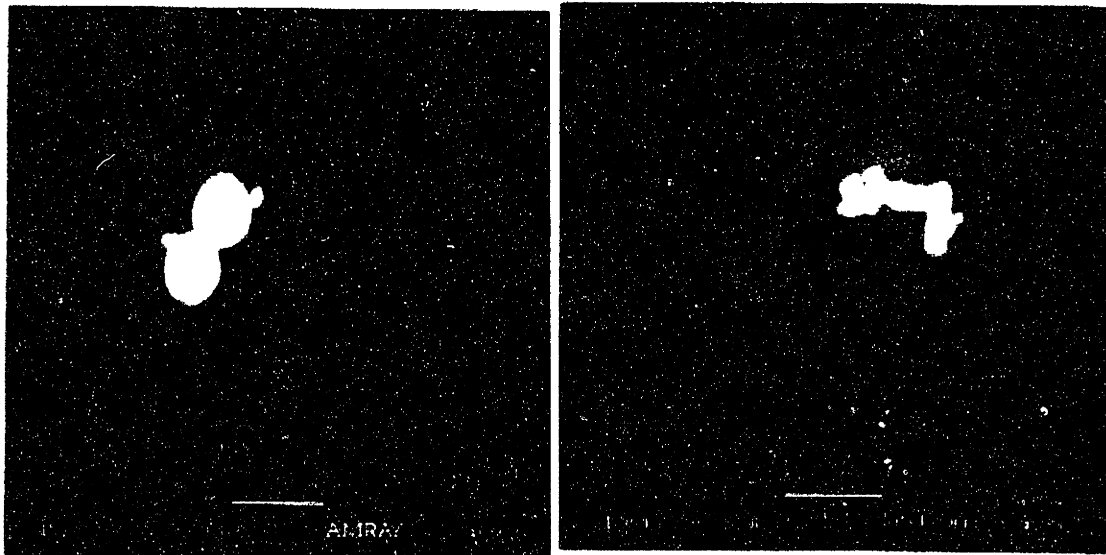
The wafer closest to the front of the cassette was turned so that its polished side once again faced the front of the cassette. The wafers were notch-aligned again to 6 o'clock and scanned using the Surfscan 6200. Post-deposition particle counts for these wafers are shown on the wafer maps in figures 6.4 and 6.5. The particle counts shown are misleading because the wafers were scratched during vacuum wand handling. Furthermore, large area defects and scratches were caused by placing the polished side of the wafer on the susceptor. Because of surface damage, particle count absolute values are not relevant. Nonetheless, by using the wafer map to subtract scratches, it is possible to make a rough estimate of the particle count.

The tools and chambers selected for testing were chosen randomly and were not considered dirty tools at the time of testing. The backside GFA shown in figure 6.4 was observed on at least three tools and five chambers. Although the number of particles varied from 8 to 90, transfer of particles from the backside of the wafer to the front of a neighboring wafer was also witnessed repeatedly.

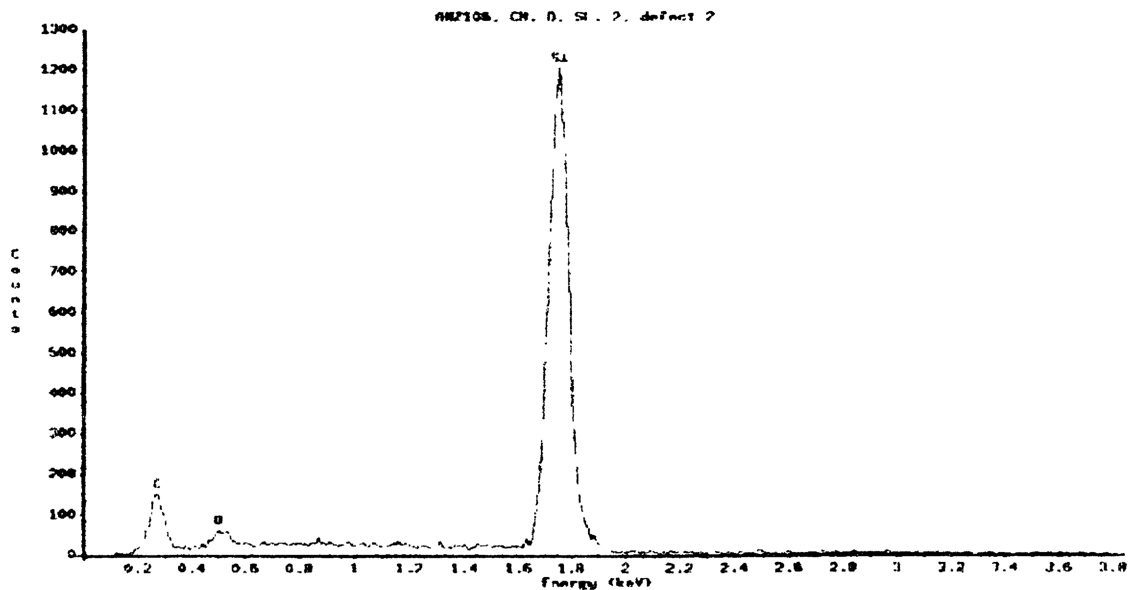
The GFA seen on the backside of the wafer shows particle accumulation near the throttle valve, where as the particles transferred to the front of the neighboring wafer are uniformly distributed across the wafer surface. There is no apparent correlation between the density of backside particles and the density of particles transferred to the front of the wafer. The distribution of particles transferred to the front of the wafer indicates that gravity alone is not responsible for particle transfer. Other factors such as particle size, composition, gas flow, and mechanical vibrations may also play a role.

Backside particles and particles transferred to the wafer front were analyzed using the SEM and EDX. Representative photos and spectra of the major oxide particle types are shown in figure 6.6. (Representative photos and spectra of particles containing aluminum are not available.) Two types of oxide particles were found on the backside of the wafer:

uniformly sized spherical particles near 1 μ in diameter and irregular sized and shaped oxide particles. In addition, a few slightly rough and jagged particles containing C, O, F, Al, Si, and sometimes Mg were also seen. All three major particle types were transferred to front of the wafer.



(a) (b)



(c)

Figure 6.6: Representative SEM photos and EDX spectrum of oxide particles seen on the backside of the ILD deposited wafer: (a) Spherical oxide particles, (b) irregular oxide particles, (c) representative oxide spectra

6.3.2 Mechanical Partitioning of the ILD Tool to Determine Backside Particle Contribution

Mechanical partitioning was used to verify that the particle source was not in the storage elevator or loadlock. A test fire wafer was prescanned using the Surfscan 6200. The wafer was then transferred into the storage elevator and left there for approximately 2-3 minutes. After returning the wafer to the cassette, it was post-scanned using the Surfscan 6200. The number of particles added was less than 5. This number is much less than the particles seen previously, therefore it is unlikely that the storage elevator is the source of particles deposited on the unprocessed wafer.

6.3.3 Recipe Partitioning of the ILD Process to Determine Backside Particle Contribution

In order to determine which part of the recipe was contributing the most backside particles, the recipe was divided into three sections: thin PTEOS and SACVD deposition, SACVD clean, and thick PTEOS deposition. Six test wafers were notch aligned to 6 o'clock and prescanned using the Surfscan 6200. All prescan particle counts were less than 17. The wafers were then turned in the cassette such that beginning with the wafer in the rear of the cassette every other wafer had the polished side facing the back of the cassette. The wafers were notch-aligned to 6 o'clock again. The first two wafers were moved into the storage elevator filling the uppermost slot first and ensuring that the polished sides of the wafers were facing each other. The unpolished side of the upper wafer was deposited with a thin PTEOS film and a SACVD film and returned to the storage elevator. Any particles falling off the backside of the deposited wafer during transfer were collected by the wafer below it in the storage elevator. Beginning with the top wafer, the two wafers were then returned to the cassette.

The next two wafers were moved into the storage elevator in the same manner as before, with polished sides facing each other. A SACVD in-situ chamber clean was completed on the deposition chamber. Following the chamber clean, the upper wafer was

placed polished side down in the chamber for approximately 4-5 minutes. The wafer was then returned to the top slot of the storage elevator, allowing backside particles to drop off onto the wafer beneath. As before, both wafers were returned to the cassette.

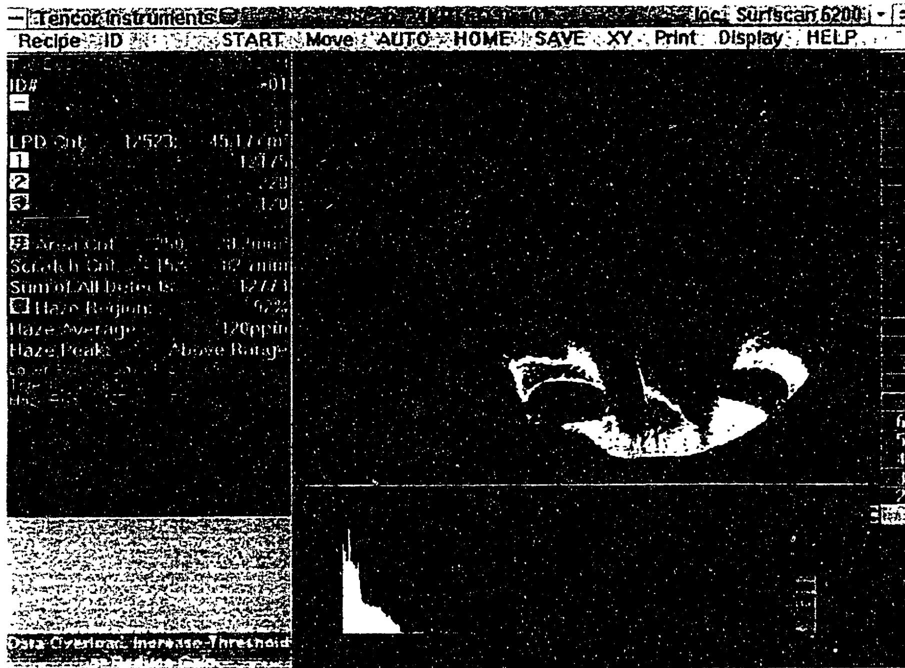


Figure 6.7: GFA seen on backside of the wafer SACVD deposited with polished side down.

The last two wafers were also moved into the storage elevator with polished sides facing each other. The upper wafer was moved into the chamber and its unpolished side was deposited with a thick PTEOS film. The wafer was returned to the top slot in the storage elevator. Particles which fell from the backside of the deposited wafer were collected by the wafer in the second slot of the storage elevator. Both wafers were then returned to the cassette.

All wafers were turned so that the polished side once again faced the front of the cassette. The wafers were again notch-aligned to 6 o'clock. The Surfscan 6200 was used to scan each wafer. Wafer maps of the SACVD deposited wafer and its corresponding backside particle collection wafer are shown in figures 6.7 and 6.8 respectively. The GFA

on the side of the wafer which was in contact with the susceptor during SACVD deposition is similar to the GFA seen following the entire ILD deposition process. The particles are focused near the throttle valve. Figures 6.9-6.11, shows the particle size distribution across the surface of the wafer. Medium to large particles are focused near the throttle, while the smaller particles are distributed more evenly across the wafer. The collection wafer has approximately 34 particles added. There is no correlation between the density and size distribution of the backside particles and the particle collected on the wafer beneath it.

Figure 6.8: Particles which were transferred to from the backside to the front of the wafer after SACVD deposition.

Both wafers were analyzed using the SEM and EDX. As shown in figure 6.12 and 6.13, the particles found on the backside of the wafer were similar to those observed on the wafer deposited with the entire ILD recipe: two types of oxide particles and C, O. Si, F, and Al particles. The majority of the particles were oxide. The particles which fell on the wafer beneath it were not as diverse in shape or composition. The particles collected

were overwhelmingly composed of C, O, Si, F, and Al and had jagged, rough edges as shown in figure 6.13. Particle sizes ranged from 1-2 μ in diameter to 0.5 μ in diameter. A few scratches were also seen on the wafers surface.

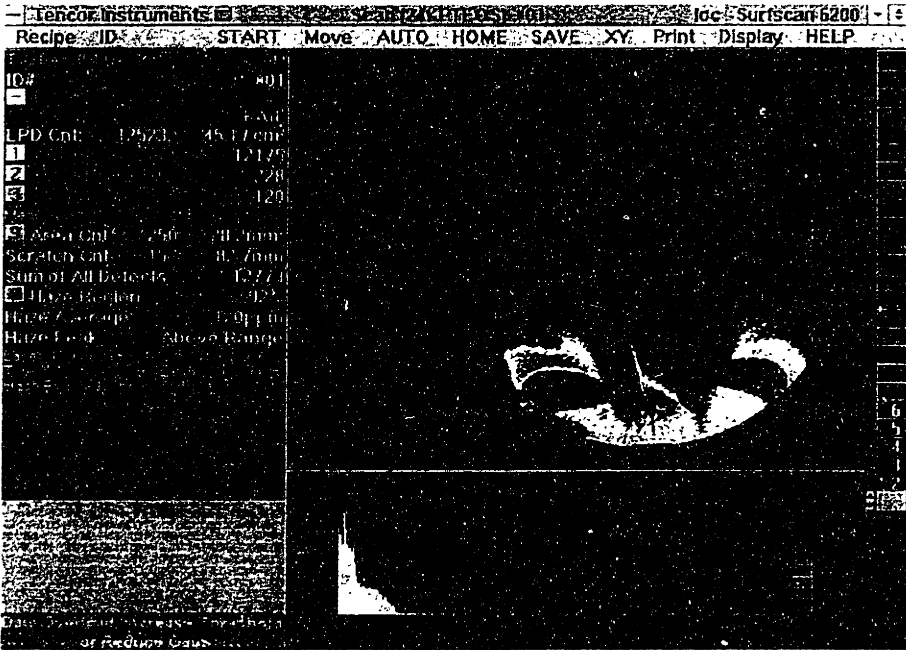


Figure 6.9: Particle distribution of 0.16-0.5 μ size particles on the backside of SACVD deposited wafer.

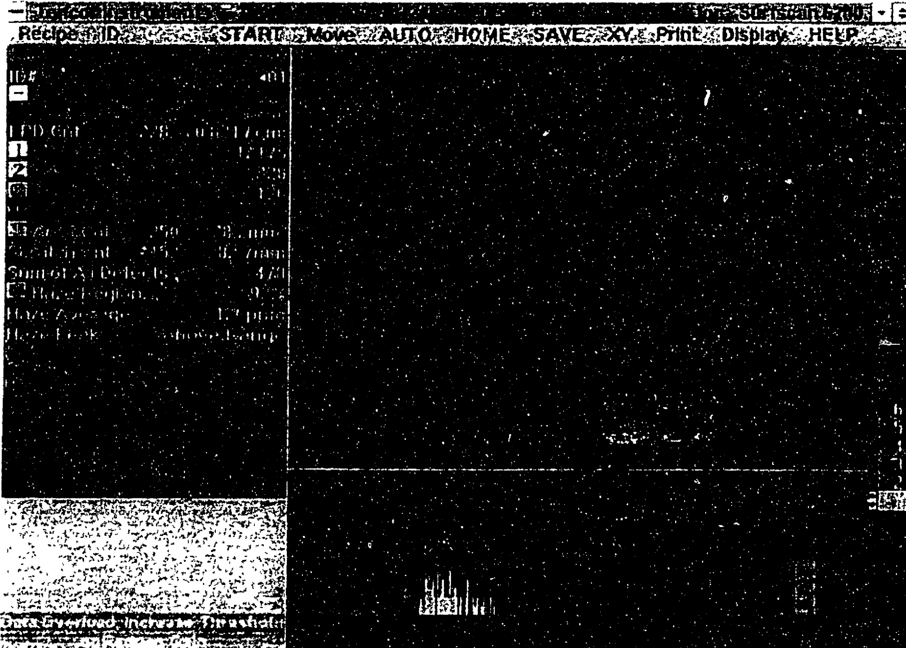
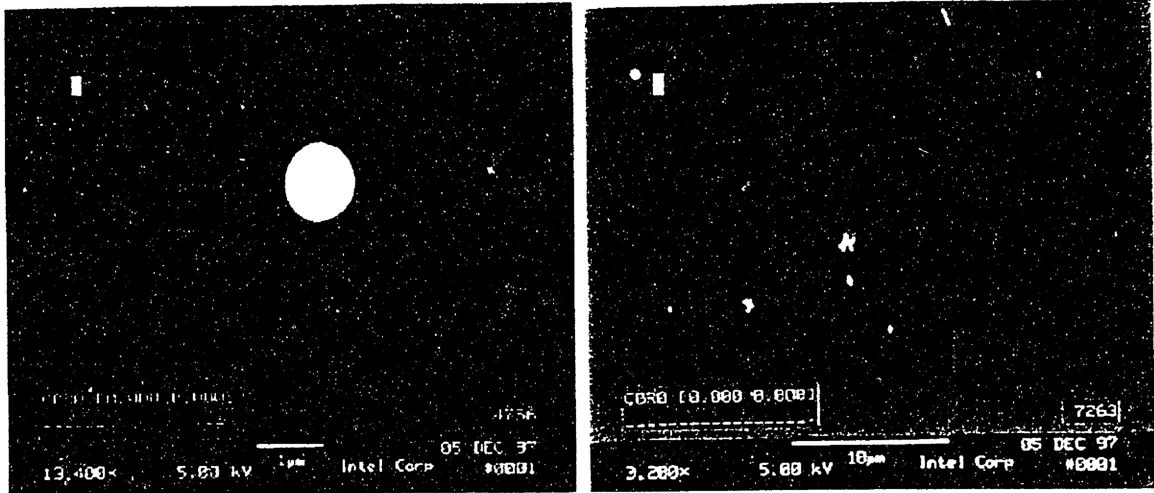


Figure 6.10: Particle distribution of 0.5-2.0 μ size particles on the backside of SACVD deposited wafer.

Figure 6.11: Particle distribution of 2.0-100 μ size particles on the backside of ILD deposited wafer.



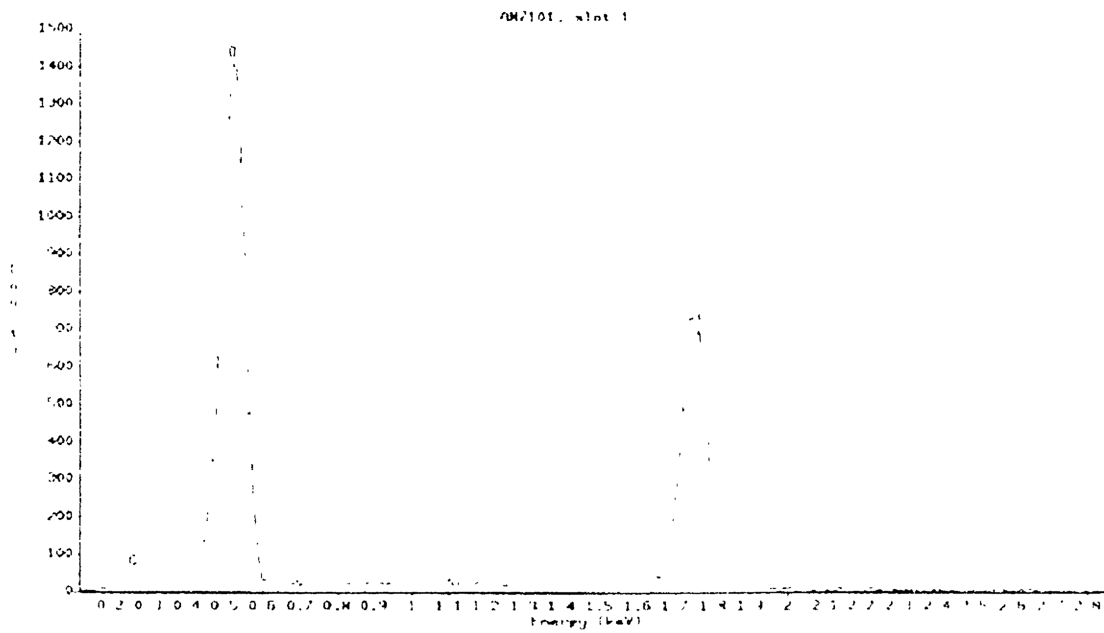
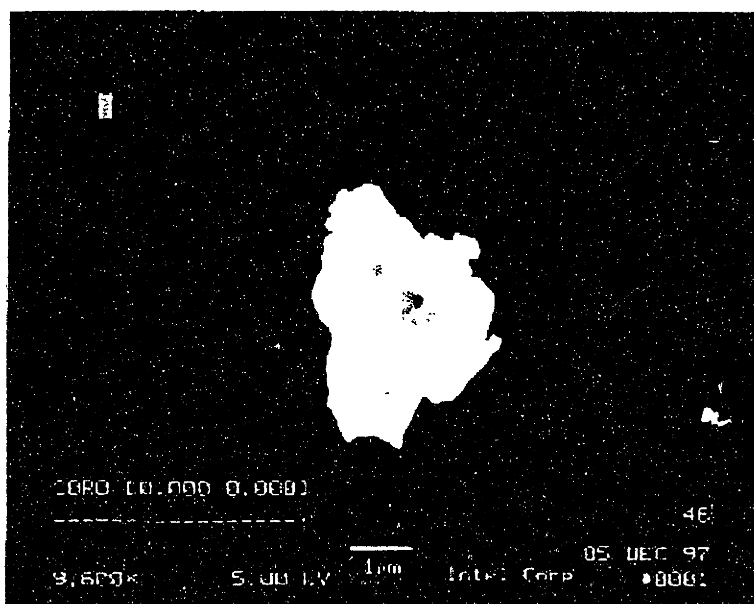
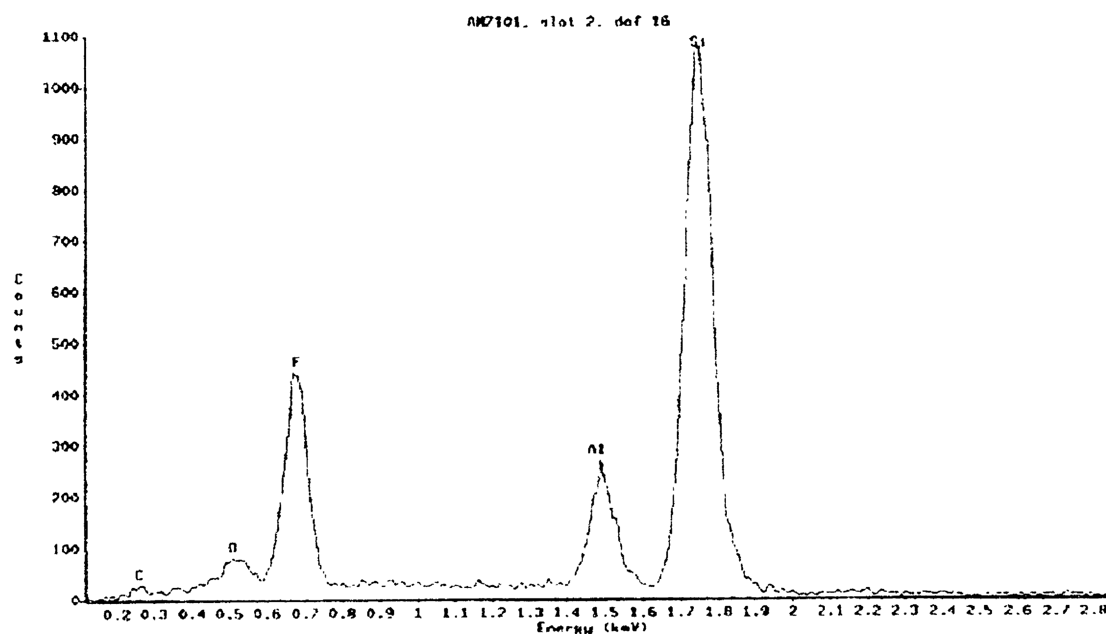


Figure 6.12: Oxide particles found on the backside of the SACVD deposited wafer (a) Spherical particle (b) irregularly shaped particle (c) representative EDX spectrum



(a)



(b)

Figure 6.13: Representative SEM photo and EDX spectra from non-oxide particles seem on the backside of SACVD deposited wafers: (a) rough, jagged aluminum particle (b) representative EDX spectrum

Maps of the wafer which was placed in the chamber after the SACVD clean and its corresponding collection wafer are shown in figures 6.14 and 6.15 respectively. The backside GFA of this wafer deviates from previous backside GFAs. The particles shown by the Surfscan 6200 are focused at the center and edges of the wafer and the particle size distribution is random. More particles were collected on the wafer beneath this wafer than the wafer deposited with. Once again the particles collected are evenly distributed across the surface.

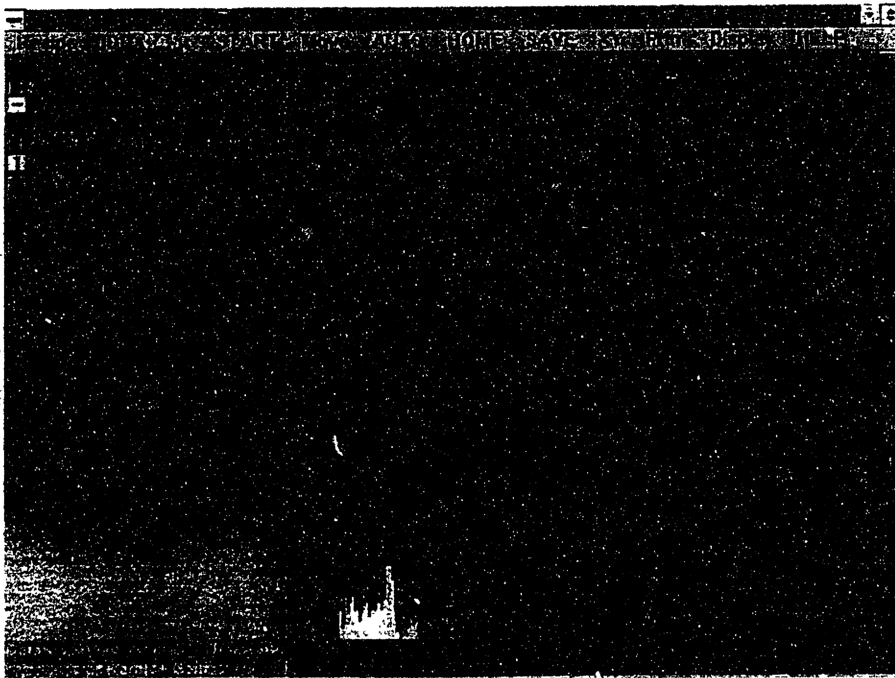


Figure 6.14: GFA seen on backside of the wafer after SACVD clean.

As shown in figure 6.16, SEM and EDX analysis revealed that many of the dense particle regions on the wafer's backside were actually scratches on the wafer's surface caused by contact with the blade, susceptor, and wafer lift fingers. In addition to scratches, dense areas of both oxide and C, O, Al, F, Si particles were seen. Photos of these particle regions are shown in figure 6.17. Once again a high proportion of the particles found on the corresponding collection wafer were rough, jagged-edged, and aluminum-based with diameters ranging from 0.25 to 1.5 μ.

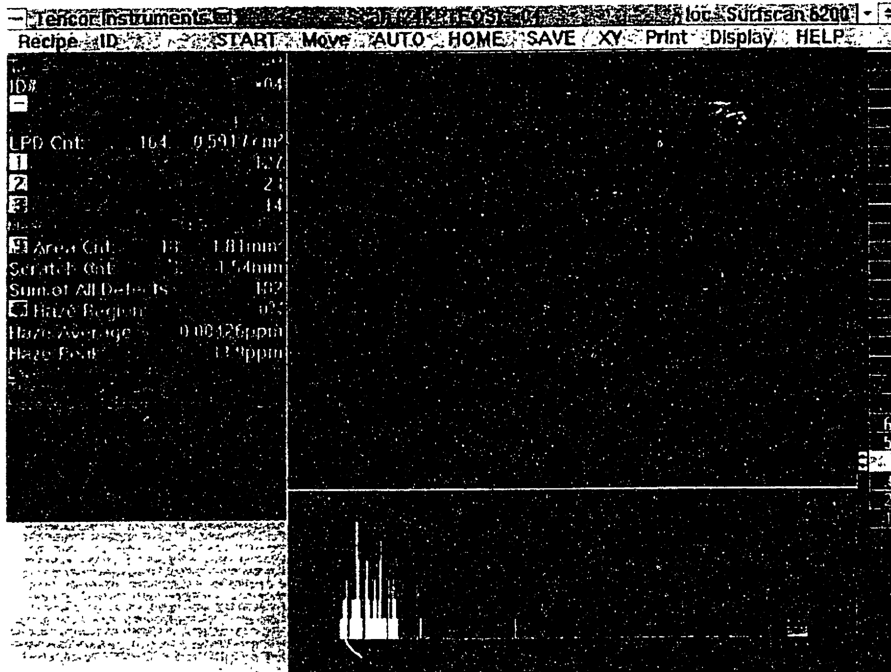


Figure 6.15: Particles which were transferred to from the backside to the front of the wafer after SACVD clean.

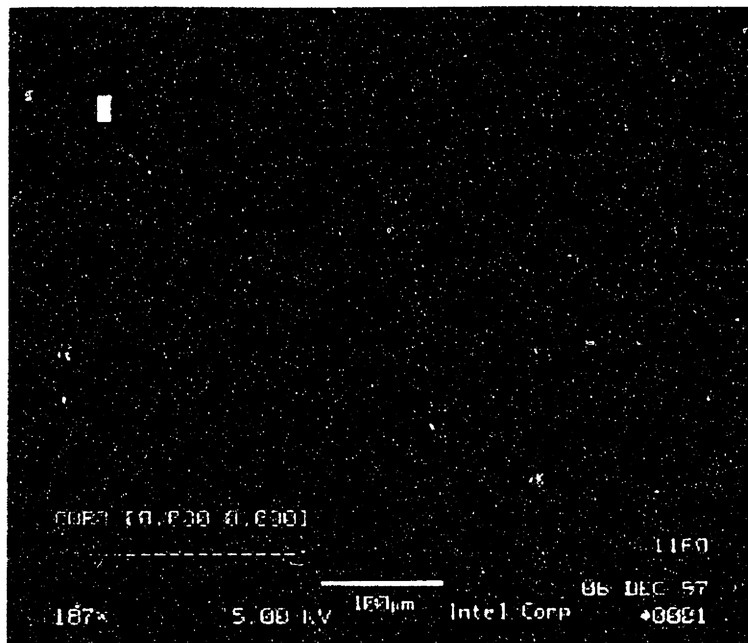
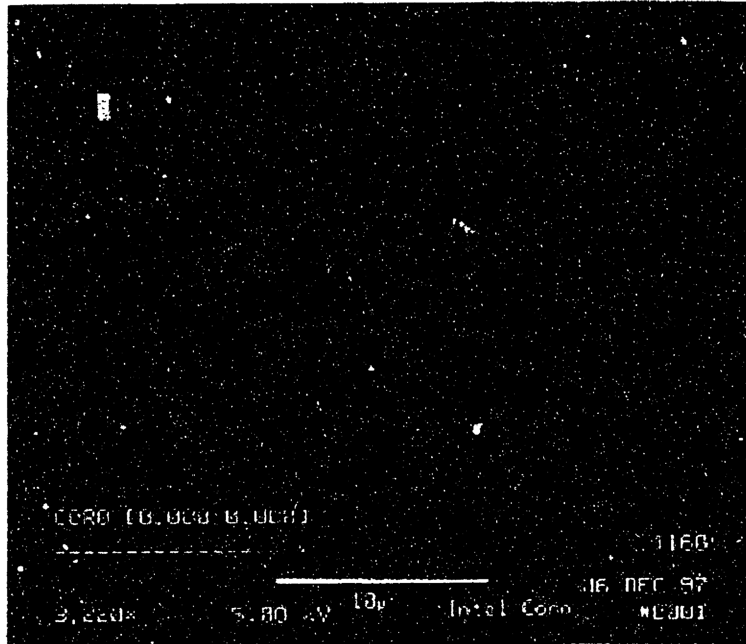


Figure 6.16: Scratches seen on the backside of wafer placed in chamber after SACVD clean



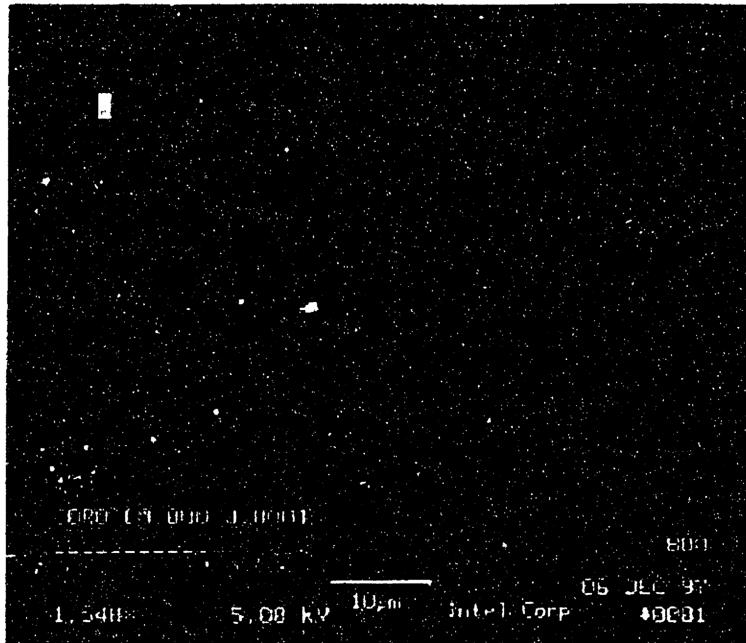


Figure 6.17: Representative photos of densely distributed particles (a) oxide particles, (b) non-oxide particles.

Maps of the wafer deposited with a thick PTEOS film and it corresponding particle collection wafer are shown in figures 6.18 and 6.19 respectively. The GFA on the backside of the processed wafer is quite similar to the GFA observed on the wafer which was placed in the chamber after SACVD clean. There are gross particle areas in the center and on the edges of the wafer. The number of particles transferred to the wafer beneath is higher for the thick PTEOS film than for either the SACVD deposition or the chamber clean. Collected particles are evenly distributed across the wafer without obvious clustering of like particle sizes.

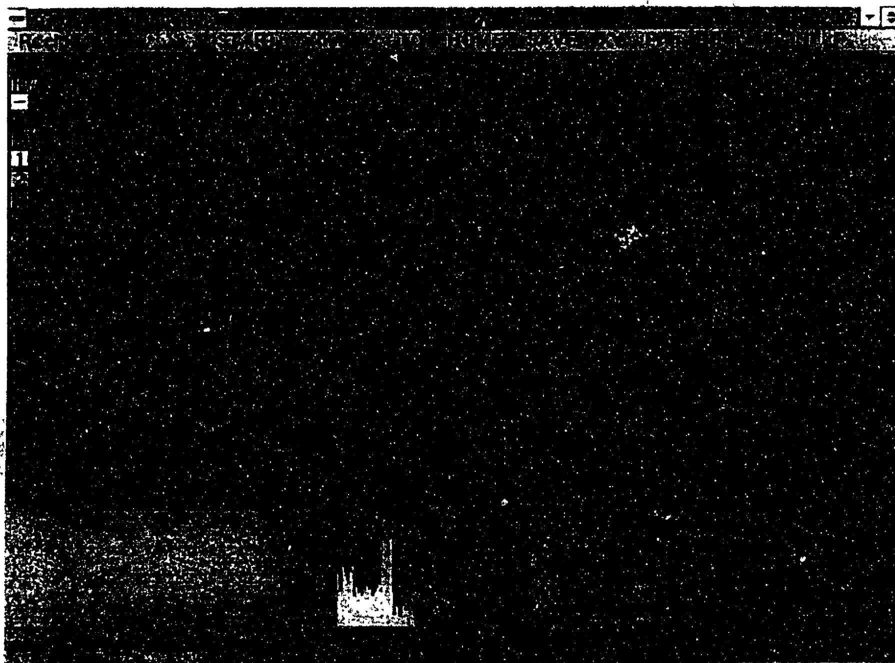


Figure 6.18: GFA seen on backside of the wafer PTEOS deposition.

SEM photos confirm that like the wafer which entered the chamber after SACVD clean, many of the particles read on the wafer deposited with PTEOS were scratches or abrasions on the wafer surface. The center and edges of the wafer were most heavily damaged. As shown in figure 6.20, many of the large abrasions were accompanied by clusters of particles. The particles shown in figure 6.20 were composed of O, Al, F, and Si, although oxide particles were also found amongst scratches. The majority of the

particles on the collection wafer were once again rough, jagged-edged particles with Al, Si, O, F, C composition.

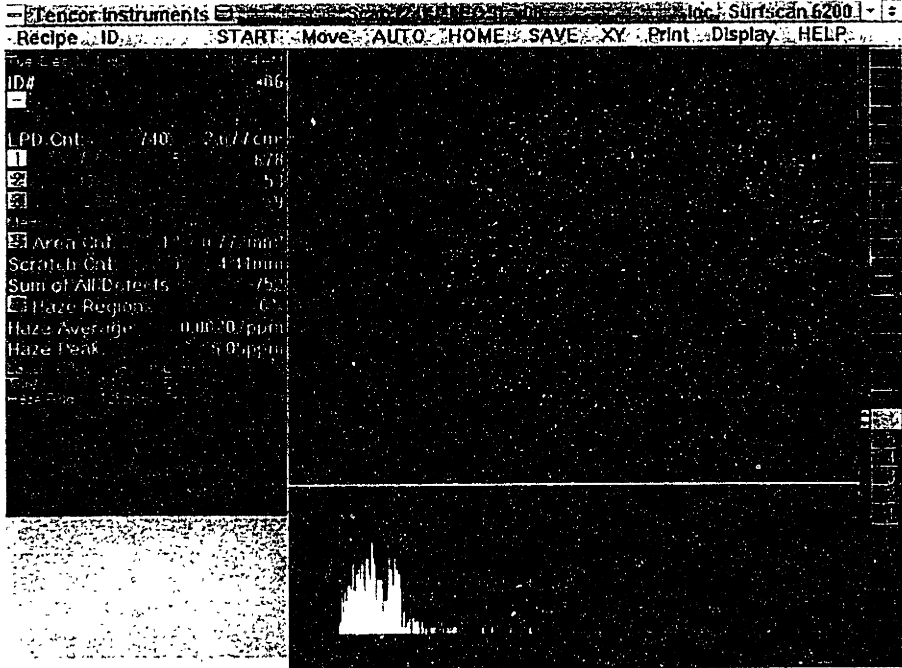


Figure 6.19: Particles which were transferred to from the backside to the front of the wafer after SACVD clean.

Figure 6.20: Particles found amongst backside scratches on PTEOS wafer.

A review of backside wafer maps for each recipe section indicates that the backside GFA seen after ILD deposition is dominated by the SACVD deposition step. The GFAs seen after SACVD clean and PTEOS deposition are attributed mostly to scratches and do not correspond with the final ILD deposition GFA. In all cases, the particles seen on the back of the wafer are a mixture of oxide and aluminum particles. The largest number of particles transferred from the back to the front of the wafer is seen during PTEOS deposition step. In every case, however, the majority of the particles transferred to the front of the wafer are aluminum. Aluminum particles which were collected under the SACVD deposited wafer are most likely generated by ozone susceptor corrosion. Because ozone is a highly reactive gas, it reacts corrosively with many metals. The relatively easy oxidation of aluminum allows ozone to be particularly harmful to the susceptor surface. The presence of aluminum-based particles amongst scratches on the SACVD clean wafer and PTEOS wafer seems to indicate that aluminum particle generation may be caused by the wafer sliding on the susceptor. Although oxide particles are not as much of a yield concern as aluminum particles, they still pose substantial reliability issues. Spherical oxide particles are most likely formed through homogenous nucleation during SACVD deposition, while irregularly shaped oxide particles are probably the result of heterogeneous nucleation during either SACVD deposition or PTEOS deposition.

The SACVD backside GFA seems to indicate that the particles are traveling towards the throttle valve, but are not making it out of the chamber or that the pressure variations on the way to the throttle valve cause particulate fall out. The larger particles near the throttle valve seem to reinforce the first idea. This can be cured by increasing the flow through the chamber or lowering the pressure drop or purge levels so that the particles have time to be pulled out of the chamber. The number of aluminum particles created by

scratching can be reduced by adjusting the flow within the chamber to avoid hockey-puck-like floating movements during transfer.

6.4 Showerhead and Blockerplate Electrochemical Corrosion

By design, the lid, showerhead, and blockerplate are RF hot during PTEOS deposition. Contact between the RF input, in the mounting plate of the ILD tool, the showerhead and blockerplate meant to ensure a zero potential gradient across the three components. If proper contact is not made, local potential gradients may develop causing electrochemical corrosion. The resulting damage to the lid, showerhead, and blockerplate introduces particulate contamination within the process chamber.

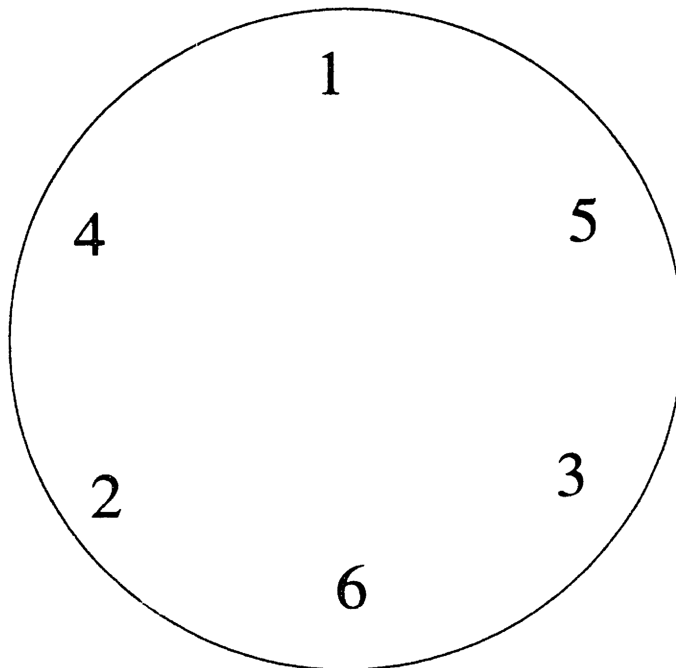


Figure 6.21: Order and positions of torque measurements

During preventative maintenance, pitting and oxide build-up was noticed consistently on the back rim of the showerhead and blockerplate. The pitting was focused near the screw holes and matching pit marks were also located around the screw holes in the gas box lid. In order to evaluate the showerhead-lid and blockerplate-lid contacts, the break

torque of each screw on two tools and eight chambers was measured. For the sake of uniformity, break torques for each chamber were measured using the star pattern shown in figure 6.21. The numbers on the figure indicate the order in which the screw break torques were measured. Measurements are shown in figure 6.22. On the average, the break torques of the screws in locations 4, 1, and 5 are lower than 2, 6, and 3. A visual inspection of the back rim of the showerhead revealed that pitting and building up were most prevalent in at locations.

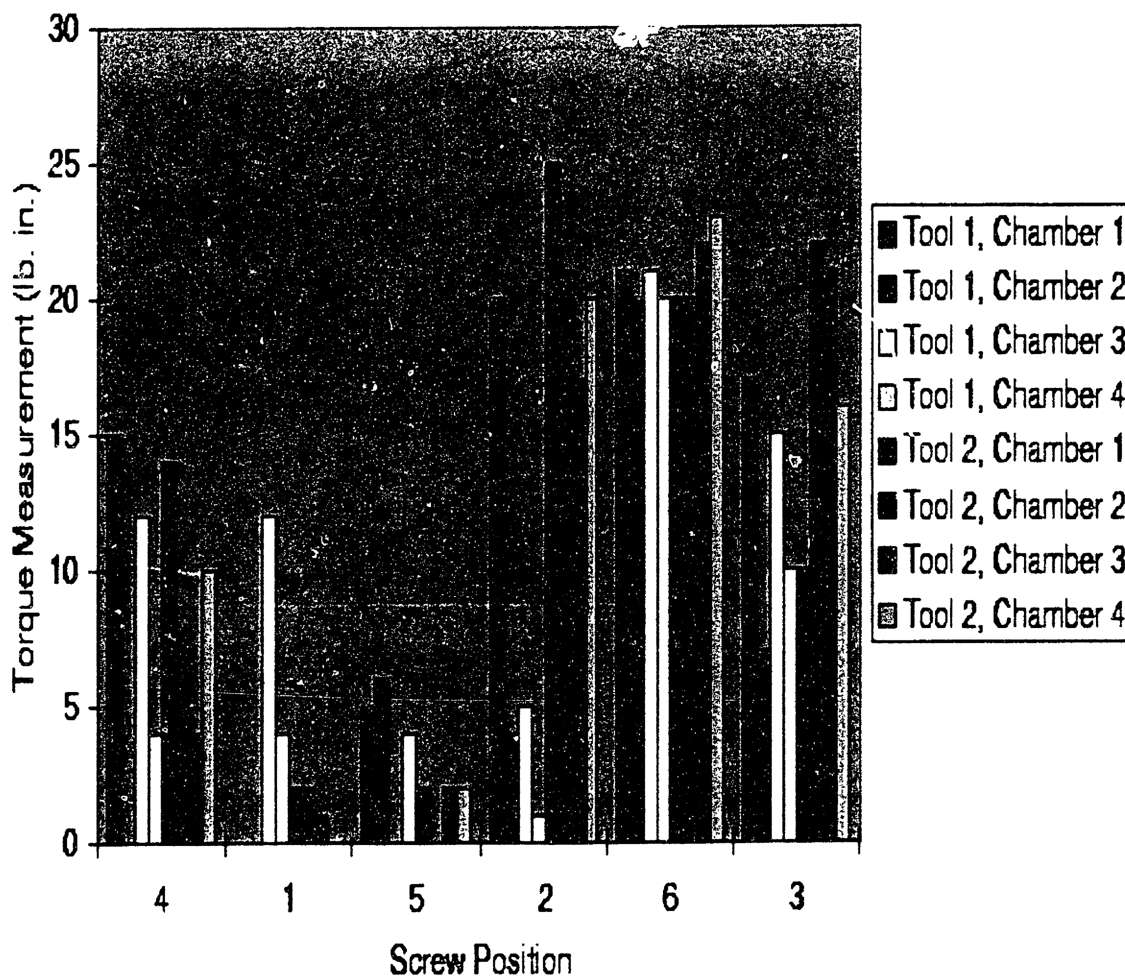


Figure 6.22: Correlation between torque measurements and screw position.

The correlation between pitting and build-up and break torques seems to indicate that there is varying contact between the lid and the showerhead. The surface damage is most likely electrochemical corrosion resulting from dielectric breakdown. Insufficient contact between the two surfaces can create a local potential difference and allow reactant gases to be trapped between the two surfaces. At very small spacings, fields associated with the potential gradient can become high enough to cause dielectric breakdown. When microarcing occurs the aluminum surface can be locally oxidized through the following reactions

$$Al \rightarrow Al^{3} + 3e \tag{6.1}$$

$$3O_2 + 4Al^{3} + 12e \rightarrow Al_2O_3 \tag{6.2}$$

The ionization the takes place prior to oxidation is responsible for the creation of electrochemical pits. The surface damage and oxide build-up seen on the back rim of the showerhead and blockerplate are consistent with electrochemical corrosion.

Chapter 7

Conclusion

7.1 Test Wafer Cleanliness and Wafer Handling

Test wafers provided by the vendor are required to meet specific standards of cleanliness. In order to ensure the validity of the particle monitor, the particle levels of the test wafers must be remain low prior to use in the particle test fire. It has been shown that the dirty test wafers are rarely introduced to the process area, therefore initial test wafer cleanliness should no longer be a concern. In contrast, improper wafer handling was responsible for 31% of the out of control test fires in a month, of which 17% were false reports. Improper handling of the wafers during cassette to cassette transfer causes wafer damage and creates particles which adhere to the wafer surface. The wafer damage during cassette to cassette test wafer transfer can be reduced by using an automated wafer transfer tool such as the Kensington wafer transfer system. Automated wafer transfer, minimizes wafer exposure to dense particulate contamination near the technician and eliminates the possibility of wafer scratching caused by improper handling during transfer.

7.2 Cleanroom Microcontamination

During ILD processing, wafers are exposed to the cleanroom environment during manual loading and unloading at the face of the tool. In order to minimize transport of particles to the wafer surface, it is important to control air flow in the loading area near the face of the tool. The air flow at the face of the tool should be zero, the positive pressure of the laminar flow in the processing area should be balanced by the laminar flow of the hepa filter over the tool. Zero net flow minimizes particle transfer from the technician to the wafer surface and decreases release of particulate contamination from the tool environment. Continuous air flow in the ergo loader, reduces the possibility of particle

build-up due to stagnant air. Furthermore, secure side panels help to minimize turbulent flow. Removal of particle sources such as dirty ionizers tips from the loading area minimizes chances of particulate contamination.

7.3 Backside Particles

The backside of the wafer comes in contact with the wafer blade, storage elevator, lift fingers, and the susceptor during ILD processing. These surfaces can collect particles through mechanical wear during transfer or chemical interactions during deposition. When the wafer is placed in contact with these surfaces, particles adhere to the backside of the wafer. The existence of a large number of backside particles during the ILD process has been shown. The majority of backside particles are located on the wafer edge nearest the throttle valve. The particle size distribution indicates that larger particles are closest to the throttle valve. The majority of the backside particles appear to be generated during the SACVD deposition step. The particles were silicon oxide or C, O, Al, F, Si containing particles, 0.5-2 μ in size of varying from spherical to jagged in shape. The spherical particles are most likely build-up from the SACVD deposition process, where as the jagged particles are likely to be generated by flaking of reaction products created by unwanted reactions of process chemicals with the process chamber. The existence of backside particles is clear, the extent of backside particle transfer to other wafer surfaces is yet unclear.

It is apparent from the study that larger backside particles are more likely to be transferred to neighboring wafer surfaces. Gravity plays a greater role in the transport of large particles. Adhesion of a large particle on the backside of the wafer is opposed by gravitational forces, while for the same large particle transfer is favored. Preferred transfer of large particles was demonstrated with inverted wafers, however Van der Waals adhesion forces of a particle to a smooth surface are less than those to a rough surface.

Van der Waals forces between a particle and a rough surface are greater because the contact area is greater. Particles are less likely to be transferred from the rough surface of the wafer backside than the polished surface of an inverted wafer. Smaller particles are even less likely to be transferred because the gravitational force opposing adhesion is small. Although it appears that backside particle transfer does occur, the high degree of particle transfer seen with an inverted wafer is not completely representative of transfer which occurs during process.

7.4 Showerhead and Blockerplate Electrochemical Corrosion

There is evidence of pitting and oxide build-up on the chamber lid, showerhead, and blockerplate. Damage to the chamber components can generate unwanted particles within the process chamber, therefore it is desirable to determine the mechanism of corrosion. The formation of pits and oxide near screw holes is most likely a result of an electrochemical reaction. It was shown that the corrosion damage was most evident near the loose screws. The lack of proper contact between the lid and the showerhead may have trapped reactant gases between the two surfaces and caused local potential gradients. When a thin layer of gas experiences a large potential, dielectric breakdown can occur. Microarcing can locally ionize the metal surface, creating pits by removing portions of the metal and oxidizing the surface. Uniform contact between the showerhead and lid is necessary to avoid introduction of particulate contamination due to electrochemical corrosion.

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