Design and Manufacturing of an Ion Electrospray Propulsion System Package and Passively-fed Propellant Supply

by

Louis Evan Perna

S.B., Aerospace Engineering, Massachusetts Institute of Technology (2009)

Submitted to the Department of Aeronautics and Astronautics
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Abstract

Satellites under 500 kilograms have been growing more popular with the miniaturization of high-performance electronics and instruments. Constellations and formations of satellites consisting of thousands of small satellites will enable inexpensive, on-demand, global access to spaceborne assets. The only impediment to the adoption of small satellites and their exploitation in radical new space system architectures is an absence of high-specific-impulse, scalable, benign propulsion options. Available technologies are too resource inefficient for small satellites, too inflexible, or pose a threat to primary launch payloads.

An emergent technology, electrospray propulsion, is inherently scalable, benign, applicable to a wide range of mission types, and resource efficient. Research in the MIT Space Propulsion Laboratory over the past decade has been focused on developing robust electrospray propulsion systems scaled to the needs of small spacecraft. The Ion Electrospray Propulsion System (iEPS) is the synthesis of this work and features a fully-integrated power processing unit (PPU), propellant supply, and electrostatic ion accelerator designed for use in CubeSats. To meet the objectives of the iEPS project, development was necessary for all three components. The work described here focused on a redesign of the thruster module package and initial design and testing of a compact, passive propellant supply system.

A MEMS package was designed, manufactured, and tested. It comprised and contained critical electrospray components in close, precise proximity and maintained electrical isolation between high voltage electrodes. Additionally, the package provided for structural and electrical attachment interfaces for the PPU and propellant supply. Design rationale is presented and iterative improvements described for both the package components and manufacturing processes. A prototype passive propellant supply system was designed and tested. The results of integration and testing for both components are presented with discussion of challenges and potential improvements.

Thesis Supervisor: Paulo C. Lozano
Title: Associate Professor of Aeronautics and Astronautics

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I would not have made it to this point without the collaboration and support given me by my colleagues in the MIT Space Propulsion Laboratory and AeroAstro. The many hours of hard work put forth by my friends and colleagues in the SPL have made possible the success of the iEPS project. Without their use (and, let's face it, abuse) of my precious hardware, the iEPS package design would not have made the strides it has these past three years. I thank you for the candid feedback and excellent ideas along the way. Your support outside the laboratory has made my return to the Boston area better than I could have hoped for. Friendship saw me through those periods of living in the clean room and subsisting off of class notes in preparation for quals.

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Chapter 1

Introduction

Today's world continuously relies on spaceborne assets for communication, weather forecasting, national defense, mapping, and scientific exploration. Historically, satellites providing such capabilities have weighed on the order of two thousand kilograms and cost tens of millions of dollars just to launch [1]. Thanks to advances in electronics, solar cell efficiencies, batteries, and digital instrumentation, systems on the order of tens or hundreds of kilograms can accomplish many of the same missions as their gargantuan predecessors while requiring less time and money to design, manufacture, and launch.

Small satellites have become a centerpiece of modern university research. However, federal governments and large corporations have grown interested in the implementation of small satellites, because not only do they make space access cheap, they enable new mission architectures based around simultaneous operation of hundreds to thousands of distributed satellites [2]. The concept of cheap, fast, on-demand, global communications and imaging has spurred investment in small satellite business development by federal governments and international corporations. The satellite industry is truly in an exciting transitional phase.

Unfortunately, a critical fact is impeding the immediate adoption and exploitation of the small satellite form factor—no suitable established propulsion technologies exist to meet the needs of small satellites. Several options meet one or more of the mass, volume, power, and performance requirements, but none of them check every

box. They all trade their benefits for crippling drawbacks. Without an appropriate propulsion technology, the small satellite revolution cannot occur.

Ionic liquid (IL) electrospray thrusters are emerging as the missing piece of the propulsion puzzle that will meet the industry demand. Systems employing IL electrosprays are inherently scalable from the nano-level up, so they fit naturally with the tight volume requirements of spacecraft such as CubeSats. Additionally, their high- and variable-specific-impulse performance capabilities are attractive to engineers designing to a tight mass budget. Along the same lines, the zero-vapor-pressure propellant can be delivered passively, thus avoiding the bulk and power draw of pressure vessels and valves. And finally, the efficiency of electrosprays nears unity when they are operated in pure ionic or droplet mode, so the overall propulsion system efficiency is driven by the power processing unit, not by the electrostatic engine.

1.1 Space Propulsion Basics

In order to speak to the relative strengths and weaknesses of current and future propulsion technologies, one must understand the basics. A rocket is simply a device which accelerates and expels a propellant mass in order to accelerate the vehicle mass by reaction. From Newton's laws of motion, it can be said that the force on the rocket is the same as that on the propellant, and both are equal to their corresponding instantaneous mass multiplied by their instantaneous acceleration [3]. If the propellant is accelerated to a velocity c, then the force on the vehicle, F_v, must be equal to c multiplied by the rate at which mass leaves the vehicle, $\dot{m}_p$.

$$\vec{F}_v(t) = m_v(t)\vec{a}_v(t) = \dot{m}_p(t)\vec{c}(t) \tag{1.1}$$

This mass-acceleration relation can be manipulated to eliminate the time dependence. Doing so reveals that the velocity change is a function of the propellant mass ejected and the exhaust velocity, c. First, the identity $\dot{m}_v = -\dot{m}_p$ is substituted.

$$m\frac{dv}{dt} = -c\frac{dm}{dt} \tag{1.2}$$

$$\int_{v_0}^{v_f} dv = -c\int_{m_0}^{m_f} \frac{dm}{m} \tag{1.3}$$

$$\Delta v = c\ln\left(\frac{m_0}{m_f}\right) \tag{1.4}$$

For a given ratio of final to initial mass, the change in velocity is directly proportional to the exhaust velocity. Looking at the equation another way reveals that the exhaust velocity for a given maneuver will determine the amount of propellant required. A high exhaust velocity leads to a low required propellant mass.

$$m_p = m_0 - m_f \qquad\qquad m_p = m_0\left(1 - e^{-\Delta v/c}\right) \tag{1.5}$$

Propulsion systems are categorized by their exhaust velocity, or more traditionally, their specific impulse, I_{sp}. Specific impulse is defined such that multiplying the specific impulse (in seconds) by the acceleration due to gravity at Earth's surface yields the exhaust velocity.

$$c = gI_{sp} \tag{1.6}$$

When the energy used to accelerate the propellant comes from a constrained source, a relationship between specific impulse and thrust develops. The kinetic energy exhausted with the propellant comes from the source $\mathbb{P}$ at some non-ideal conversion rate, η. Arranging this relationship correctly and substituting Equation 1.1 elucidates the inverse relationship between thrust and specific impulse at fixed power.

$$\eta\mathbb{P} = \frac{1}{2}\dot{m}c^2 \qquad \overset{F=\dot{m}c}{\Longrightarrow} \qquad F = \frac{1}{I_{sp}}\left(\frac{2\eta\mathbb{P}}{g}\right) \tag{1.7}$$

In the case of an electric propulsion device, the available power is almost certainly

limited to a maximum value, so when a thruster operates at a higher specific impulse, the thrust necessarily goes down.

Generally speaking, traditional chemical propulsion systems operate in a high-thrust, low-I_{sp} regime, whereas electric propulsion devices operate in the opposite corner. Air-breathing jet engines and hybrid designs bridge the gap.

1.2 Electrosprays as Propulsion

In an electrospray, an intense electrostatic field is maintained in the presence of a conductive fluid. A capillary-style setup is drawn in Figure 1-1. In response to the electric stress on its surface, the fluid deforms into a predictable shape known as a Taylor cone. The shape results from a balance between electrostatic and surface tension forces [4]. At the cone's apex, liquid is pulled from the bulk and accelerated toward the downstream electrode. This configuration is known as the cone-jet mode. Should the surface electric field be high enough, ions from the conductive liquid can be directly evaporated from the surface. When this evaporation becomes dominant, eliminating the cone-jet behavior altogether, the electrospray is in a high-I_{sp} regime and is operating with near-unity efficiency.

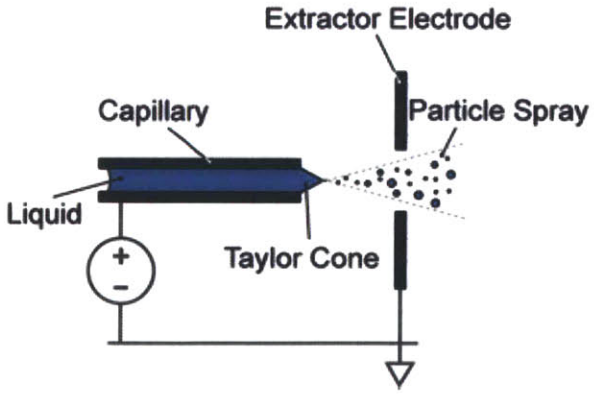


Figure 1-1: A capillary-style electrospray device is depicted in cross-section. Conductive liquid is introduced to a region of strong electric field where its surface deforms into a Taylor cone-jet and liquid is accelerated.

A single electrospray emitter operating in the ionic mode generates a thrust on the order of tens of nanonewtons. When arrayed in the hundreds, the thrust level

reaches the micronewton range. The low-thrust configuration of a single emitter or small group of emitters would be ideal for the precise control of a satellite carrying a sensitive scientific instrument. Exactly such a system was designed for the LISA Pathfinder mission. Scaling up, the thrust levels become attractive for small satellite missions which desire orbital maneuvers, attitude control, or even interplanetary transfer. While there is some interest from the scientific community regarding the former, the latter application is what will enable growth of the small satellite industry.

Thus, the manufacture of arrayed electrospray emitters became a focus of electrospray research in the MIT SPL. Legge's success with fabrication of porous emitter tips in a one-dimensional array prompted Courtney's efforts to manufacture a planar array. Along the way, a package was developed which encapsulated the emitter array and provided a method for attaching and aligning an extractor. Courtney successfully demonstrated ion emission from porous metal array, but encountered major issues in the reliability of the device and its manufacture [5, 6].

1.3 A Need for Thruster Development

As mentioned, the individual components of an electrospray thruster array were well-developed, and Courtney's success in forming a planar array and corresponding extractor encapsulated in a compact form factor was a great step in the direction of producing a flight-worthy design. Much work remained, however, before a robust thruster head could be reliably produced. Furthermore, the issues of developing a dedicated, flight-like power processing unit and a compact, long-term propellant supply had not yet been addressed. Thus, the iEPS team began work on developing such hardware and exploring the lifetime performance of porous-substrate-based ionic liquid electrospray emitters.

The work described herein focused on the development of the thruster package and a protoype propellant supply system. Chapter 2 concentrates on the redesign of the thruster package and extractor components in response to the successes and failures seen with Courtney's work. The manufacturing of the thruster frame and

extractor components is outlined in Chapter 3. A general evaluation of the success of the package redesign is given in Chapter 4 with thoughts on improving upon the iEPS 2.2F design. The prototype propellant supply system is described in Chapter 5. Proof-of-concept test results are presented, design methodologies are explained, and the results of the prototype implementation are given. Final thoughts regarding the work and its future direction appear in Chapter 6.

Chapter 2

Design of an Improved Electrospray Thruster Package

Individual electrospray emitters have been studied for decades; however, in order to achieve thrust levels of interest even to microsatellites, they must be arrayed and operated in parallel. The MIT Space Propulsion Laboratory has been working over the past decade on manufacturing techniques and emitter designs that enable the packaging and simultaneous operation of hundreds of electrospray sources in one device. Courtney described the first Ion Electrospray Propulsion System (iEPS) which successfully demonstrated the capabilities and performance desired; however the system had several flaws, ranging from logistical to operational [6, 7]. Improving upon Courtney's thruster was the impetus for the redesign of the thruster package which has come to be known as the iEPS 2.x series of devices. Several design iterations were performed based on the results of manufacturing, assembly, and test, all culminating in the iEPS 2.2F configuration which is intended to fly in early 2015. The details of and rationale for the various designs are captured here along with considerations and concepts for future changes.

2.1 Lessons from the Original iEPS Package and Redesign Goals

Courtney developed and tested the first iteration of the iEPS device [6]. The thruster's performance was promising; however, if development of the device was to continue, several issues needed to be addressed ranging from an extreme lifetime limitation to ease of assembly. The majority of the issues could be directly addressed through changes to the device package.

2.1.1 Initial Design

The first version of the iEPS package was an all-silicon, highly-enclosed design with gold-coated silicon grids. A cross-section of the device is depicted in Figure 2-1. Laser-cut stainless steel grids later replaced the silicon grids in an attempt to reduce beam interception.

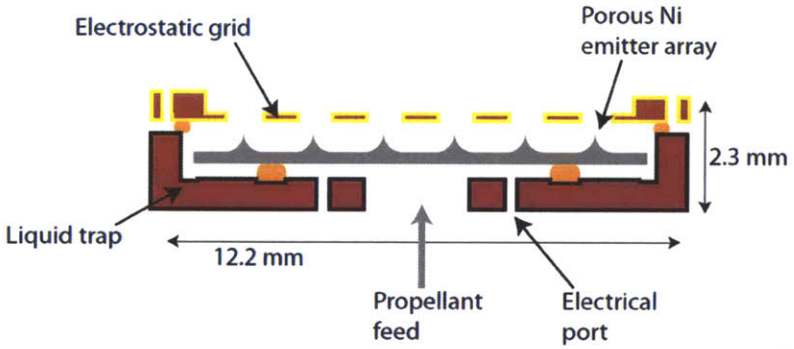
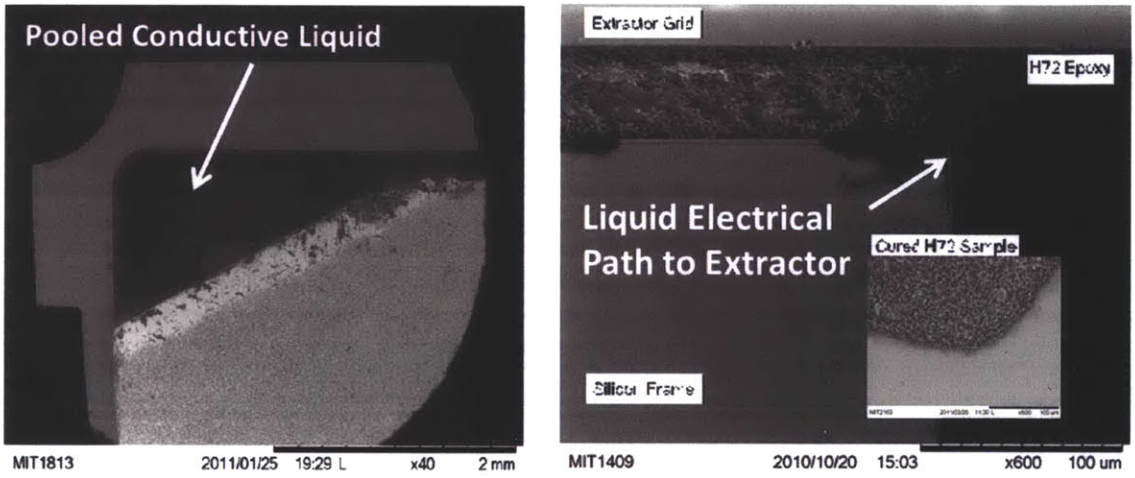


Figure 2-1: A cross-section of the original iEPS design [6].

2.1.2 Current Leaks Due to Propellant Accumulation

Within the first few minutes of operation, the iEPS device would often begin to draw the maximum available current from the high-voltage amplifier, sometimes with little to no beam current measured downstream. Inspection of the devices suggested that this was due to the formation of liquid current paths between the emitter and extractor via the device packaging [8]. It appeared as though excess liquid propellant would wick

into and pool in the package interior. Once the high potential difference was applied, the liquid would climb the package walls and bridge the insulating gap provided by the silicon oxide surface of the frame. Electron micrographs of liquid contamination are provided in Figure 2-2. These low impedance pathways were carrying most or all of the current running through the device, thus reducing the beam current or preventing electrospraying altogether.



(a) (b)

Figure 2-2: Evidence of excess liquid (a) pooling in the original package design and (b) bridging the emitter-electrode gap [6].

2.1.3 Arduous Grid Alignment, Assembly, and Removal

Alignment of the extractor apertures to the tips was achieved through manual use of a jig which held the grid and frame in alignment during epoxying. Precise alignment was achieved with the addition of a microscope and x-y-z stage with micrometer control. This assembly method worked for the gold-coated silicon grids which had alignment marks and were flat. In the case of the preferred steel grids, warping from the laser-cutting process made assembly difficult. Alignment often took tens of minutes with this configuration. Unfortunately, because of the need for the epoxy to cure over time, well-aligned grids often shifted before the adhesive had fully set, negating the benefits of the painstaking alignment process.

Moreover, once attached with epoxy, the silicon grids could not be removed without destruction of the frame. This made post-test analysis overly destructive and also meant that grids and emitters could not be unpaired. Reconfiguration, thorough inspection, and re-alignment were impossible.

2.2 Design of a New Thruster Package

2.2.1 Package-level Considerations

In the redesign of the iEPS package, all of the beneficial properties of Courtney's design needed to be maintained while eliminating the failure modes, improving upon alignment and assembly, and maintaining heritage with the emitter manufacturing methods and test equipment still used in the SPL. At its most basic, the package needed to provide a base onto which the emitter substrate could be mounted and the emitter pattern aligned. From there, the package had to insulate the two close-proximity, high-voltage electrodes from one another. To maintain heritage, the propellant port dimensions were initially held constant and the extractor aperture pattern was kept to match emitter fabrication. To avoid formation of propellant shorts, an open design was conceived. Alignment occurring as a byproduct of assembly was included. And finally, support for a grid downstream of the extractor was added as a feature.

These concepts led to the initial iEPS 2.0 design, and experience with the 2.0 design shaped the changes which led to the first flight design, iEPS 2.2F. These two package designs are shown in Figure 2-3 as exploded and collapsed views. The package comprises four layers as depicted in Figure 2-4, the bottom three of which are permanently bonded together into a frame. Each layer has material and geometric features important to the overall device's functionality. The rationale for the features of each layer follows.

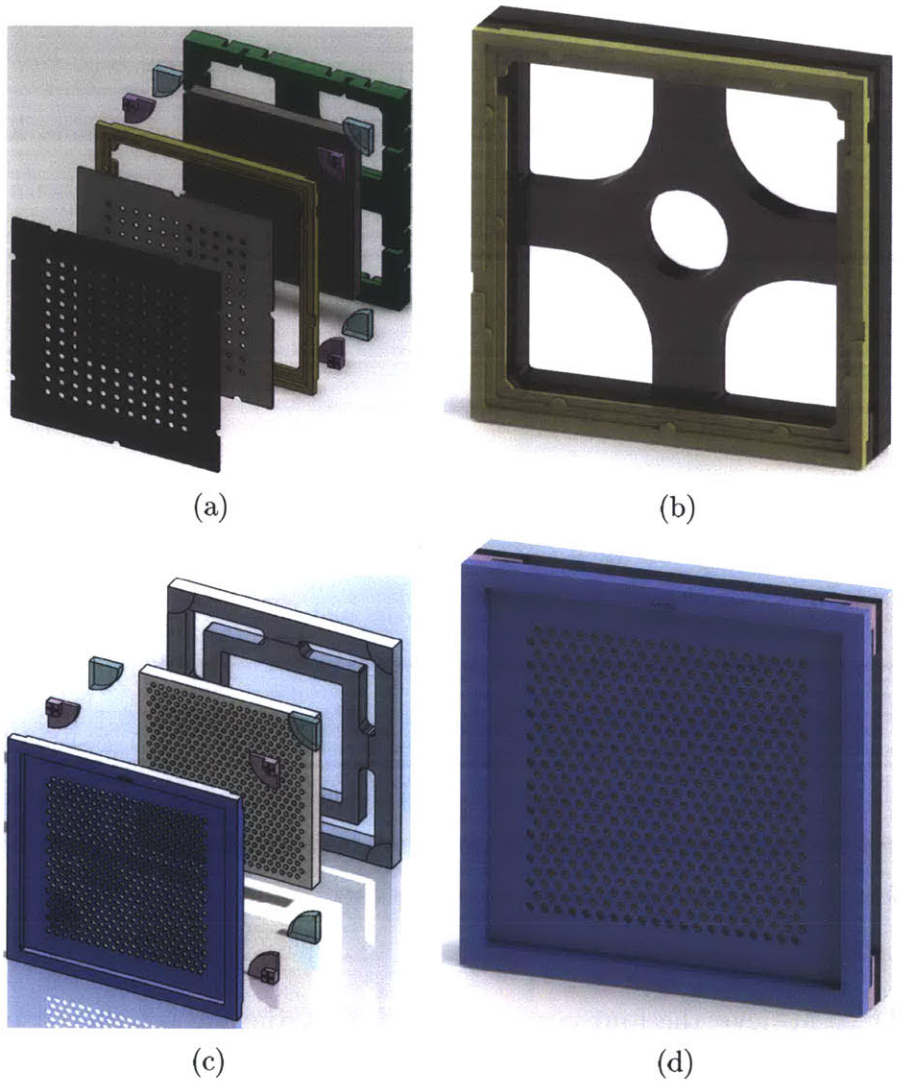


Figure 2-3: Exploded and collapsed views of the (a,b) iEPS 2.0 and (c,d) iEPS 2.2F designs as modeled with CAD software.

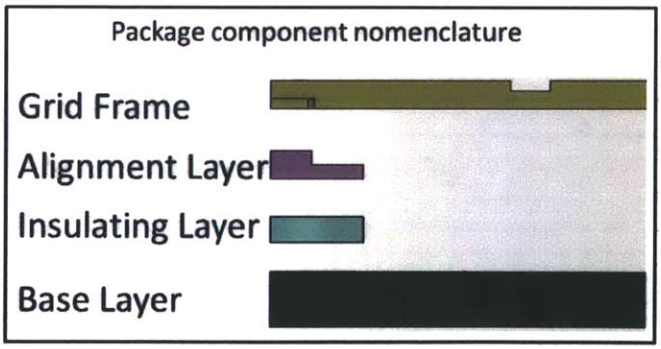


Figure 2-4: A cross-section view of iEPS 2.0 with layer nomenclature. In the case of the uppermost layer, the unibody design is simply referred to as an extractor.

2.2.2 Base Layer Design

The base layer, or layer one, serves four main purposes in iEPS 2.x: (1) serving as the main structural component of the device, (2) providing a mounting location for the emitter substrate, (3) acting as the first line of defense against accumulation of propellant and formation of current leaks, and (4) providing an interface for mounting to test setups and eventually, propellant reserves.

Backbone of the Package Frame

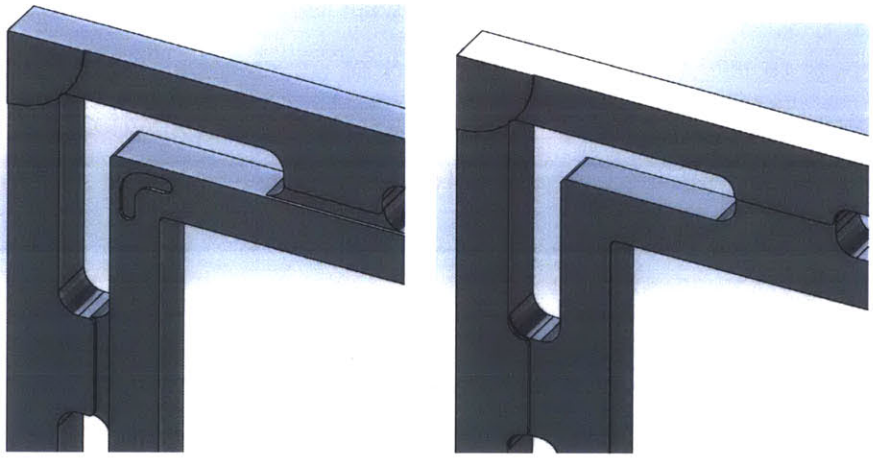
A striking difference between the previous design and the design of the iEPS 2.x package is the shift toward a very open structure. With this change, the rigidity and strength of the box-like, uni-body 1.0 frame was lost. To compensate for this change and to allow for the liquid trap features described in the subsequent section, the base layer was chosen to be thick, nominally 1 mm. This thickness was maintained throughout the design iterations, despite the eventual elimination of the liquid traps. Corners in the etched geometry were rounded to avoid stress concentration when under load as silicon is a brittle material and will easily cleave along crystal planes when mildly stressed.

In order to achieve the four-corner pillar design, the face of the base layer was recessed 25 to 30 μm everywhere except for at rounded areas at the corners as depicted in Figure 2-5. These pedestals provided the bonding surface for the second layer and held the glass away from the interior where bonding was not intended.

Figure 2-5: An isolated view of a frame base layer corner where a pedestal is defined to prevent bonding anywhere but at the corners.

Fixture for the Emitter Substrate

An essential purpose of the frame, the base layer provided a surface onto which the emitter substrate could be affixed. The emitter substrate was adhered with an epoxy applied directly to the bare silicon surface. This was done manually with no coarse alignment assistance for the placement of the substrate chip. After some experiences with emitter chips debonding and worries about liquid transfer from substrate to frame, two design variations were introduced with iEPS 2.2, each of which addressed an individual problem. The first added small recesses to the central area of the base layer which were meant to act as epoxy wells for better adhesion to the structure. In the second, the entire substrate interface bed was recessed in order to introduce areas for epoxy at the chip edge where the interior bridged to the exterior of the frame. Placing epoxy there was meant to block liquid from wetting the silicon surface of the frame. The bed could also potentially act as a rough alignment feature for the emitter chip. Eventually, only the recessed bed variation was included in the iEPS 2.2F design, not as a way of preventing liquid transfer, rather as an optional feature to accommodate off-nominal emitter chip thicknesses (those in excess of 1 mm). Examples of the epoxy wells and chip bed variations may be found in Figure 2-6



(a) (b)

Figure 2-6: Examples of (a) the epoxy wells in iEPS 2.2 to improve emitter chip bonding and (b) the chip bed recess to improve bonding, block liquid movement, and accommodate over-tall chips.

First Defense Against Current Leaks

The most crippling failure of the original iEPS design was the development of current leaks within seconds or minutes of initial operation due to the transport of excess liquid propellant. To avoid this issue in iEPS 2.x, an open architecture was adopted. This move to an open design necessitated an increase in the footprint of the frame to 13 mm $\times$ 13 mm in order to maintain compatibility with the heritage emitter chip size.

The emitter chip was separated from the extractor supports by a gap, and the liquid would have to travel from the center of the chip edge along one of the frame arms to reach one. This was a change from about a 1-mm path along the electric field to 7 or more mm, mostly transverse to the field's pull. The liquid path is illustrated in Figure 2-7. Additionally, features were added to the design which further impeded the transport of liquid and the formation of a continuous liquid path, some of which were in the base layer. These features appear in the 2.0 and 2.1 designs as nominally 750-μm deep trenches in the outer structure of the base layer. The trenches were intended to act as traps for the conductive propellant which would be unlikely to move down into them, against the attraction of the electric field. Initially, two design variations were made: one with five trenches etched into the upper and lower face of each corner support arm and the other with three above and two below. With the changeover to the 2.1 design, the number of trenches was changed to two above and one below in one design and none in the other. The reduction was an attempt to recover structural integrity. Eventually, it was determined that the trenches were unnecessary for liquid trapping with the open architecture and were done away with for the 2.2 design.

Interface to Test and Propellant Supply Equipment

Lastly, the base layer was also used as the interface between the thruster and operational support hardware. The underside of the thruster was kept flat for stable placement on surfaces. In the center, a porthole was included to allow for wetting

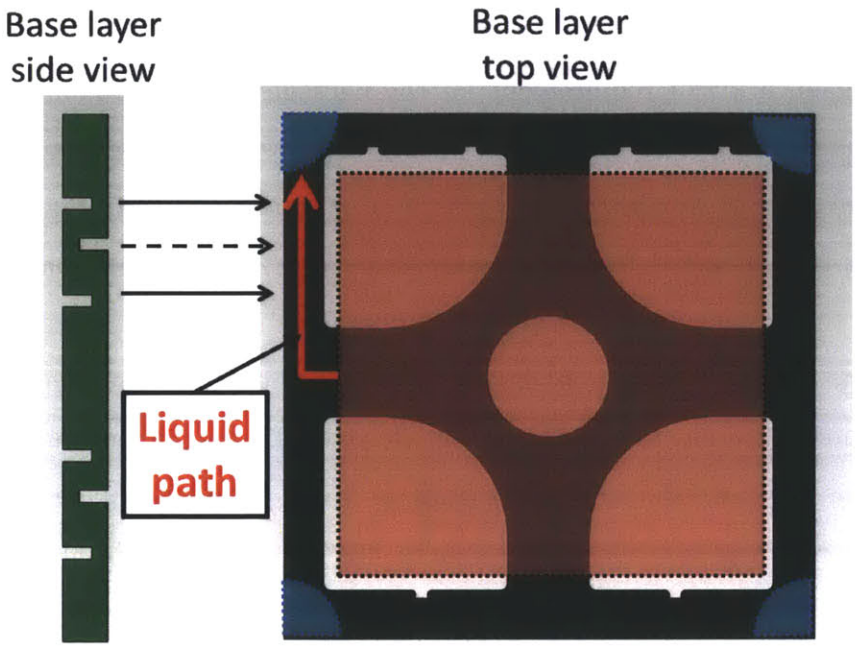


Figure 2-7: An illustration of a path that propellant would need to traverse in order to reach the corner posts and climb to the extractor electrode.

from the backside of the emitter chip and for connection of a propellant reservoir. In the iEPS 2.0 and 2.1 designs, the circular porthole was maintained at the heritage diameter of 3 mm. After testing showed that hydraulic impedance could reduce performance, the port was increased in area for version 2.2 as seen in Figure 2-8. Both square and circular ports were designed, the circular with a 6-mm diameter and the square with a 7-mm width. These amounted to approximately four- and seven-fold area increases, respectively. The square variant was chosen for the iEPS 2.2F configuration.

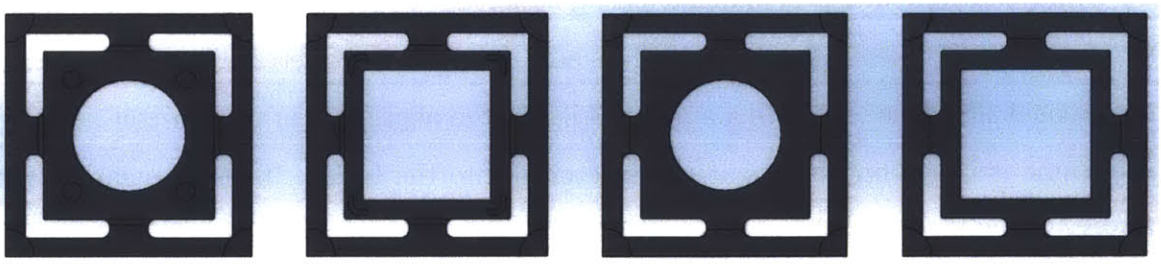


Figure 2-8: The four variations of the base layer in iEPS 2.2 showing the two port variants and the variation between epoxy wells and recessed chip bed.

2.2.3 Insulating Layer Design

As mentioned, a major requirement for the package is the electrical isolation of the high voltage electrodes. In Courtney's original design, this was achieved through the combination of an oxide layer grown on the the silicon frame and the epoxy separating the extractor from the frame. In iEPS 2.2, the isolation is provided by a 500-μm thick glass layer of Corning Pyrex 7740. This layer is anodically bonded to both the base and alignment layers above and below it. Anodic bonding results in a siloxane layer forming between the Pyrex and bare silicon on each face. The combination of these siloxane layers and the thick glass lead to an insulating layer capable of resisting approximately 125 to 460 kV between the electrodes [9]. As the thruster is intended to operate two orders of magnitude below that, it is likely that only a defect in materials could precipitate a short through the frame. Surface contamination, however, is not precluded, but that is the reason for the open design of the thruster frame.

By virtue of the process used to shape the insulating layer, the walls interior to the frame come to a sharp inward-facing horizontal edge. This surface geometry further acts to prevent formation of liquid pathways as any liquid which reaches the apex will (1) be unlikely to traverse it due to surface tension and (2) may electrospray onto the grid or emitter substrate rather than reach the extractor.

2.2.4 Alignment Layer Design

To avoid the difficulties of manual or jig-assisted alignment, a design was desired which made alignment of the emitter tips and the extractor apertures a feature of the component interface. As with Courtney's iEPS, the alignment of the emitter array to the frame is based on alignment marks etched into the frame. These appear on the upper face of each corner post as a crosshair as shown in Figure 2-9. The crosshairs are aligned at a wafer level to the shape of the corner posts. The corner posts act as a keyed interface to corresponding recesses in the underside of the extractor frame. Tolerances between the post walls and the extractor frame define part of the alignment

scheme as is described in Section 2.2.6.

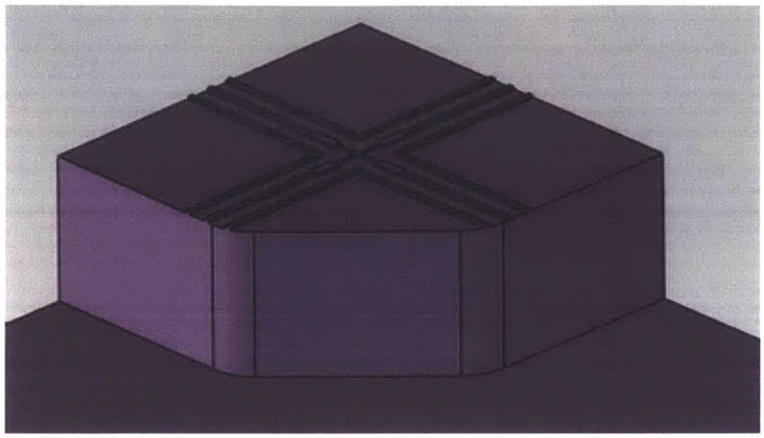


Figure 2-9: Each corner post of the frame is topped with an alignment crosshair for reference in machining the emitter array.

2.2.5 Extractor Layer Design

Two main extractor types were designed and manufactured: the grid frame with metal extractor grid and the unibody silicon extractor. While the grid frame was originally preferred for its thin, rigid, sputter-resistant tungsten grid and support for a downstream grid, the latter design was adopted for iEPS 2.2F due to the reliability of yield and geometry and due to the compatibility with batch production.

Grid Frame and Metal Extractors

The original extractor design was made of two components: a silicon grid frame and the metal aperture grid(s) which it held. Solid silicon was used to form the grid frame. Rigid tungsten foil was used for the extractor and accelerator grids, as it could be made thin without risking significant deflection under electrostatic loading.

The grid frame is a square structure which is designed to support the metal grids at their edges and is shown in Figure 2-10. Recesses for interfacing with the package frame are at the corners of the underside of the grid frame. The upper side features two levels at which grids can be fit. The deeper level is for the necessary extractor. The upper level can be fit with a secondary grid to modify the velocity of the extracted

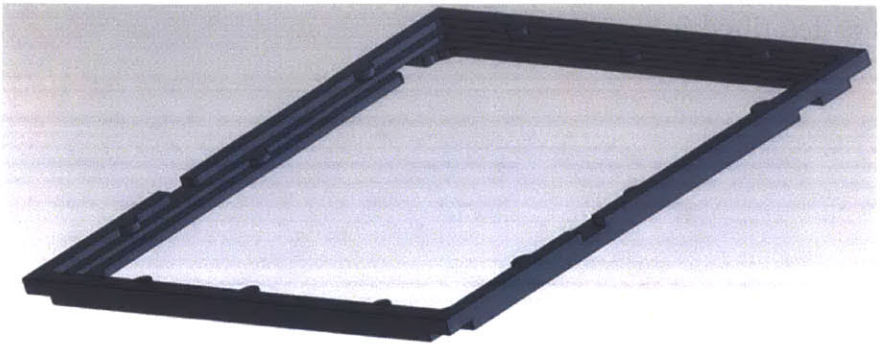


Figure 2-10: To support the use of metal extractor grids, a silicon grid frame was designed to fit and align to the thruster frame. It contains a secondary level for the attachment of a downstream accelerator grid.

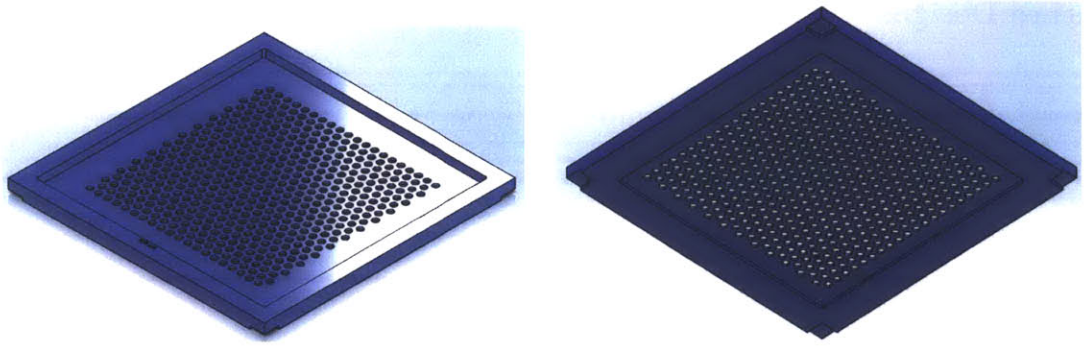
propellant. The depths of these levels is determined by the desired extractor-to-accelerator grid spacing. Additional recesses were added to the underside and top level to accomodate electrode leads.

Alignment keys are designed into both levels of the extractor for positioning of the metal extractor grids. These relied on tight tolerances between circular shapes. The key pattern for the extractors and accelerators were different so that there was no confusion regarding which similarly-sized piece fit where.

Unibody Silicon Extractor

Due to poor controllablity of the metal etching and the serial manufacturing process involved, a move to a silicon-based component design was made. The silicon extractor was designed to be a single component. The underside of the silicon extractor is identical to the grid frame described above, however the upper side is simply a single well, at the bottom of which are the extraction apertures in a silicon sheet. Figure 2-11 shows both sides of the unibody extractor.

A silicon-on-insulator wafer was used to precisely define a flat plane for the underside of the extractor which is level with the tops of the frame corner posts. This is achieved by the alignment recess features and central hole on the underside only etching to the depth of a uniformly-buried silicon oxide layer. The thickness of the silicon aperture grid was initially intended to be nominally 100 to 150 μm, however



(a) (b)

Figure 2-11: The unibody silicon grid uses an SOI wafer to achieve a uniform underside and DRIE etching to achieve deep, vertical sidewalls. Alignment of the apertures to the corner recesses is performed precisely at the wafer level.

in an attempt to reduce beam impingement, this was later reduced to a desired 20 to 30 μm. Control of this thickness in processing was found to be difficult, so the end thickness varies among production runs, dies on the wafer, and even across an individual extractor.

A metal coating was added to the design of the extractor for three reasons. The first was to allow for easy soldering to the component. Second was to improve charge relaxation in the grid so that any beam impingement charge can be redistributed quickly to maintain an even extractor potential. The final reason was to protect the underlying silicon from atmospheric oxygen and moisture so that it does not oxidize. Operational erosion of the metal layer will occur in a near-vacuum where the reduced presence of oxygen will oxidize the silicon much more slowly.

Variations in the design included three aperture diameters and various solder well shapes. Aperture diameters tested were 250, 275, and 300 μm, and the largest was chosen for the iEPS 2.2F configuration. Solder well variations tested included 200, 300, and 400 μm circles and rounded slots, and long U-shaped raceways of the same widths. Both through holes and pots were tested. It was determined that the simple rounded slot wells worked, and that the variation in diameter was not critical; so they were chosen in the interest of structural integrity and manufacturing ease.

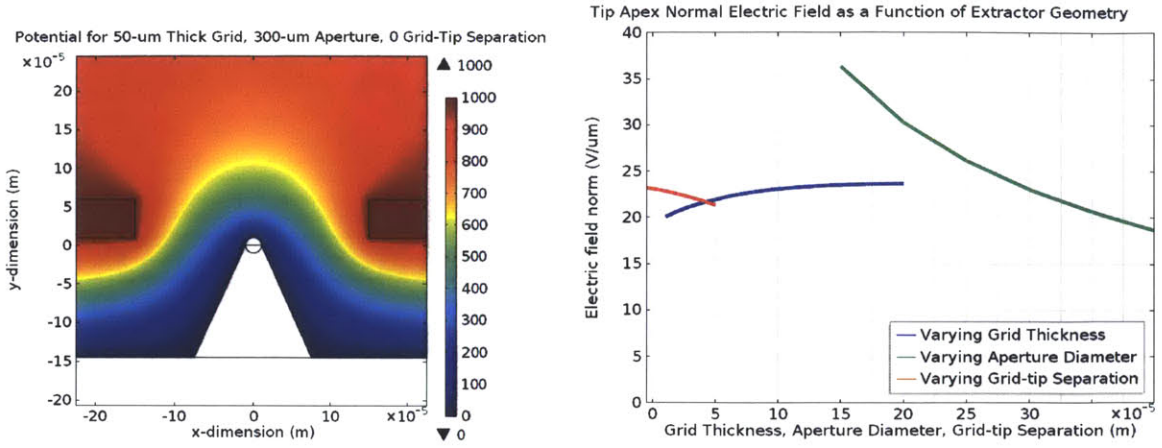
Future Designs

Several design variations of the unibody silicon extractor were considered, but not fabricated. The two main drivers were reduction of beam current and an interest in adding an acceleration grid.

Any propellant which impinges upon the extractor electrode directly reduces the performance of the device in terms of thrust, efficiency, and lifetime. Two-dimensional electrostatic modeling of the effect of dimensional variation between the aperture and emitter was done to inform considerations of increasing aperture diameter and reducing grid thickness. An example field solution and the field dependence with geometry are presented in Figure 2-12.

It was found that the shape of the extractor electrode downstream of the extractor opening has little effect on the tip electric field intensity. Over the range in which aperture variations have been produced, the aperture diameter changes the electric field intensity at the emitter tip by ± 5 to 10%. These two results lead to the conclusion that large, diverging apertures in a thick grid can achieve similar emission conditions as slightly smaller cylindrical apertures, while potentially reducing beam impingement and without losing rigidity. Thus, a new extractor design utilizing isotropic etching was conceived and is conceptually illustrated in Figure 2-13. An added benefit of such a design is the potential for an improved depth uniformity across the wafer with the use of a different etch technique. The downside, though, is that the mask geometry will depend on the substrate thickness.

A downstream grid adds the capability of operating in multiple specific impulse and thrust regimes with a single system when power-limited. This capability has the potential to allow the use of a single propulsion system for drastically different maneuvers. Coffman showed the relationship between flight time and change in I_{sp} and the effects of efficiency on this reduction [10]. By reducing the specific impulse at fixed power, the thrust can be increased to directly reduce the mission time. Inversely, the specific impulse can be increased in order to reduce propellant consumption across the same impulse change. With these multi-modal benefits in mind, a conceptual



(a) (b)

Figure 2-12: A two-dimensional electrostatic model was made in COMSOL Multiphysics to better understand the influence of emitter geometry and position on the tip electric field intensity. An example field solution is presented in (a) and the geometric dependencies in (b). Note that there is an insensitivity to grid-tip separation and downstream shape in the range shown, but that aperture diameter is sensitive to small openings. Aperture diameters of interest range from 200 to 400 μm.

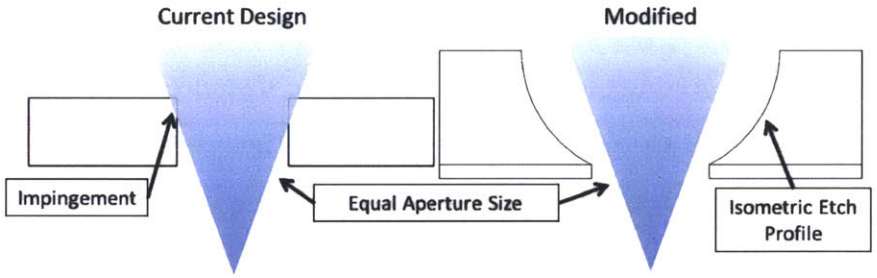


Figure 2-13: A divergent aperture is conceptually shown to reduce the amount of beam impingement on the extractor despite the increased thickness of the grid.

design for a dual-grid, unibody extractor component was devised.

Achieving multiple grid layers in a solid component will require the bonding of multiple thin wafers. The extractor is constructed as described in the previous section; however the thickness of the upper portion will need to be reduced in consideration of the inter-electrode gap desired and any separation layers that need to be accommodated. A second wafer would be patterned with the accelerator apertures and then bonded to the extractor layer. Another option is to replace the second wafer with a thin film metal on an insulator as the downstream grid.

A requirement for this component would be electrical isolation of the two elec-

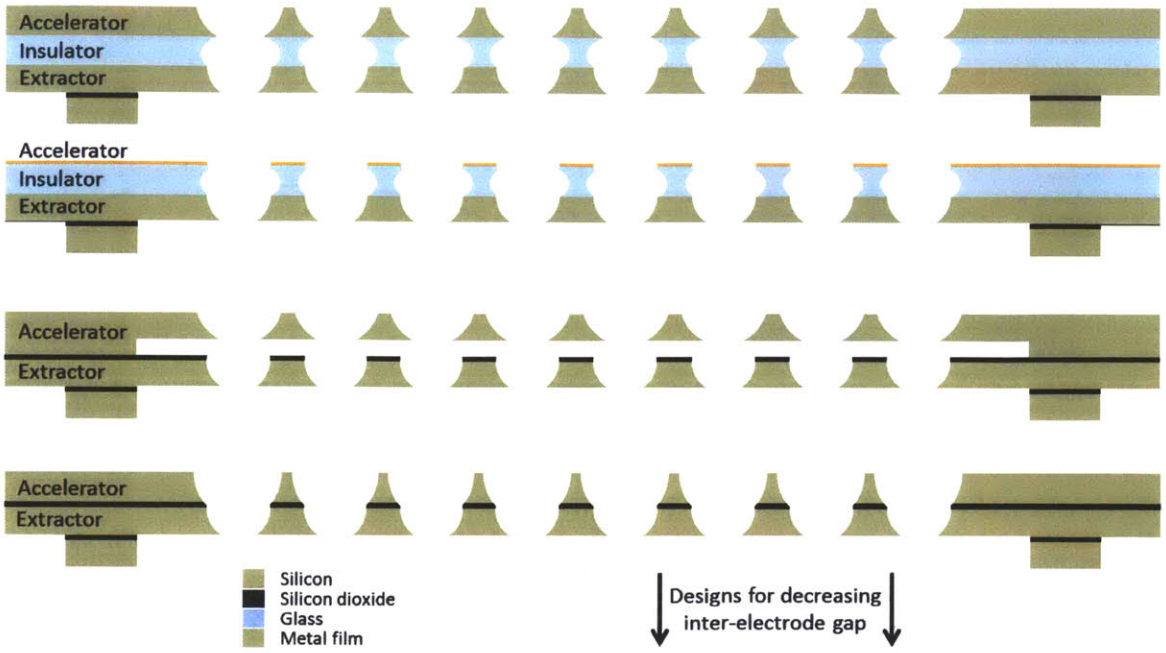


Figure 2-14: Depending on the desired electrode spacing in a unibody dual-grid extractor-accelerator component, there are multiple design options including oxide-insulated, oxide-insulated with offset, glass-insulated, metalized glass, or more.

trodes while also maintaining a small inter-electrode distance. This can be achieved by bonding wafers with oxidized surfaces such that there is an insulating plane between them. Alternatively, a thin layer of glass could be used as a separator similar to its use in the thruster frames. The choice between these options will be based on the optimal inter-electrode gap and the availability of thin glass substrates. A cross-section for each concept is shown in Figure 2-14.

2.2.6 Component Alignment Schemes

For efficient operation, it is desirable for the emitter tips to be coaxial with the extractor apertures. Misalignment can cause asymmetric electric fields, off-axis propellant acceleration, and increased beam impingement. As the tips are on the order 10 μm in diameter and the apertures have been sized between 250 and 300 μm, a maximum misalignment in the 10 to 20 μm range has been deemed acceptable. The alignment scheme developed for iEPS 2.x utilizes low-tolerance interfaces during assembly to orient precisely aligned, manufactured features to one another. In short, crosshairs on

the alignment layer dictate the position of the emitter tips, and the interface between the frame corner posts and the extractor recesses defines the position of the apertures. In the case of the grid frame, alignment of the metal extractors implemented another low-tolerance interface. Alignment inaccuracy during manufacturing of the alignment features determines the minimum achievable misalignment in practice.

Of the four frame-extractor interfaces, two opposing corners have a 50-μm tolerance, one has a 20-μm tolerance, and the final corner has a -2-μm tolerance. This final corner has an expected zero-tolerance once undercutting during etching is accounted for. The larger tolerances provide for ease of assembly, but by pushing the extractor into one corner, the alignment error can be driven, in principle, to zero. The alignment interfaces are shown with their tolerances in Figure 2-15. In practice, there will be an imperfection, however with the constraints of the design, the misalignment is limited. For a bi-directional linear displacement, the maximum misalignment is $\sqrt{20^2 + 20^2}\ \mu m = 28.3\ \mu$m. A rotational misalignment introduces more complicated geometry, however the maximum center-to-center misalignment of a single aperture with respect to the frame is less than 50 μm, and the average across all apertures is below 36 μm. In practice, these values do not hold due to inaccuracies inherent to the frame, extractor, and emitter manufacturing techniques which misalign the alignment features with respect to one another.

Alignment of the etched features in the two components is a result of wafer-level alignment on an optical stage during photolithograpy. This introduces misalignment which varies in magnitude across the wafer. While the misalignment can be less than ten micrometers at the alignment marks themselves, in general it increases radially, so the central dies will be best aligned, and the edge dies will the most misaligned. Photolithography misalignment will be largest between the aperture positions and the extractor alignment recesses as these are aligned on opposite sides of the wafer using virtual positions in an alignment tool.

Due to difficulties in controlling the exact geometry of the metal etching, the alignment between the grid frame and the metal grids was unpredictable as it involved trial and error in choosing the design of the extractor photolithography mask. This

was a main reason for developing the unibody extractor.

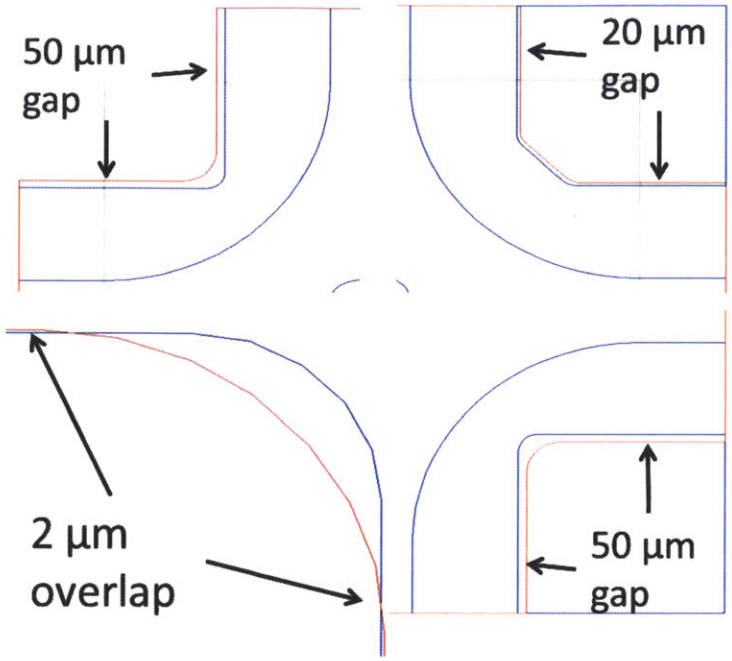


Figure 2-15: The four corner posts slot into recesses on the extractor underside. This allows for alignment of the apertures to the frame. Because the emitter tips are also frame-aligned, this should result in a low misalignment of tips to apertures.

Updates to the alignment scheme will likely include tighter tolerances and modified emitter alignment marks. Tighter tolerances are desired as it has been determined through experience that ease of assembly will not suffer from less "wiggle" room, and that the best alignment is actually achieved through additional adjustments with a microscope. Modifications to the alignment marks will make spotting them in the microscope used for emitter manufacturing easier, and they will reduce the occasional confusion with the wafer-level alignment marks.

Chapter 3

Manufacturing the Thruster Package

All components of the iEPS 2.x thruster package were manufactured in the MIT Microsystems Technology Laboratory using well-understood microelectromechanical systems (MEMS) and integrated circuit (IC) industry tools and processes. These processes ranged from the complicated chemistry of high temperature reacting gas film growth and deposition to simple manual application of masking materials. Each device layer was processed separately before being assembled into the package. The three layers of the thruster frame were permanently bonded at the wafer level, while the extractor layer was attached once emitter manufacturing and assembly were completed.

In part, this chapter summarizes the manufacturing processes at various device levels including the challenges encountered in developing and executing a successful process. Additional detail is provided for the processes in Appendix A. First, though, a short introduction to the types of processes used is given.

3.1 Microfabrication Basics

In order to inform the discussion of component manufacturing, a summary of the basic processes employed is provided with reference to their general applicability to this work. Where prudent, additional process detail is provided where context dictates.

3.1.1 Raw Materials

In the manufacturing of MEMS and IC devices, the standard form of raw material is the wafer. These are most commonly composed of single-crystal silicon formed into a thin disk, though also common are quartz, glass, and gallium arsenide. Additionally, bonded silicon wafers with an intermediate silicon oxide layer, known as silicon-on-insulator (SOI) wafers, can be sourced pre-made. Dopants can be used in the semiconductors to precisely control the bulk conductivity. These wafers come in standard sizes. The purity, doping, conductivity, and dimensional statistics are tracked by the manufacturer and tightly controlled. The work discussed here used silicon, Corning Pyrex 7740, and SOI wafers exclusively in the 150-mm (6 in.) diameter standard.

3.1.2 Thin Film Growth and Deposition

While the base material comprises the final structure, it is often necessary to modify the surface in order to define features, protect the pristine condition of the surface, or alter the surface properties for functionality. This can be achieved by initiating a chemical reaction at the surface or by mechanical or chemical deposition of material. All three types were employed for all three aforementioned reasons.

Thermal Oxide Growth

Pure silicon naturally reacts with oxygen to produce silicon dioxide. When the bare silicon of a wafer is exposed to the air, a thin (on the order of tens of ångströms) native oxide layer will form. At high temperatures (800 to 1200 °C), at high oxygen concentrations, and in the presence of water vapor, this process accelerates, though the thickness growth rate slows as it is is diffusion-limited. Furnaces have been developed to provide these conditions and are regularly used to grow oxide on silicon in the range of a few hundred nanometers to two micrometers at the extreme. This process will consume some of the surface silicon, and if the oxide is removed, the wafer loses some thickness. Thermal oxide growth was primarily used in this project

for protection of pristine silicon bonding surfaces and as an etch mask for shallow etches.

Polycrystalline Silicon Deposition

By pyrolysis, an amorphous polysilicon layer can be deposited on a substrate. This process occurs at high temperature (575 to 650 °C) such that silane (SiH_4) spontaneously decomposes into silicon and hydrogen. The deposition rate is on the order of 10 nm/min and depends on the temperature and on the silane concentration which can be controlled directly or also through control of a non-reacting nitrogen background flow. For this work, Polysilicon is deposited as an etch mask against hydrofluoric acid for the Pyrex insulating layer.

Chemical Vapor Deposition

In chemical vapor deposition (CVD), volatiles or a mix of reacting gases are introduced to the surface of a wafer and the products are deposited. This is usually done at low pressure (milli- or microTorr) and enhanced by energizing the gases into the plasma state. CVD can deposit various films on a substrate based on the chemicals introduced, however the thickness is limited by the stresses introduced in the formation of the film which, if too high, can delaminate the film. For the work herein, plasma-enchanced CVD (PECVD) was employed to deposit a thick silicon dioxide layer on the extractor substrate to be used as a hard mask resistant to plasma etching.

Electron Beam Physical Vapor Deposition

Electron beam (e-beam) evaporation employs a hot filament and accelerating electrode to bombard a target with electrons, thereby heating it to its melting point. Some of the melted target material then vaporizes under vacuum and condenses on any cold (below melting) surfaces it encounters. If a substrate is placed in the chamber with the vapor, it will be coated by the heated material. Rotating and moving the substrate can ensure even film deposition. The thickness of the layers deposited are limited by film stresses. Additionally, due to material incompatibilities, it may be

necessary for a final surface film to be preceded by an adhesion layer film. E-beam evaporation was used to deposit metal on the unibody silicon extractors as a way of preventing oxidation, improving surface charge relaxation, and enabling soldering.

3.1.3 Contact Photolithography

Contact Photolithography is a method for precisely defining two-dimensional patterns in a light-reactive surface film. This film can then be used as a protective mask for defining patterns in underlying films, for selectively removing substrate material by etching, or for selectively preventing deposition of other materials. Generally, the pattern is initially produced on a metal-coated glass plate using laser writing or on transparent plastic film by printing. These masks can then be used to protect a spun-on liquid or laminated film polymer from ultraviolet light. Hexamethyldisilazane (HMDS) is often deposited on the substrate prior to coating with liquid photopolymer to promote adhesion. The polymer will react when dosed with the light and either become more soluble (positive) or less soluble (negative) in a developing solution. The polymer is then selectively dissolved, exposing the underlying material. Exposed material can be acted upon by plasma, acids, or physical deposition processes. Exposure of the pattern can be precisely aligned (usually within 10 micrometers of two points) to existing features on the wafer using an x-y stage and microscopes. In the case of the work described here, photolithography of positive spin-on photopolymer was extensively used to protect surfaces from wet and dry etches. In total, ten patterns, not including version variations, are used for to form any one iEPS 2.x package configuration.

3.1.4 Wet Etching and Cleaning

Wet etching and wet cleaning are the submersion in an acid, base, or reactive bath in order to remove material. The benefits of wet processing are its low-tech requirements and amenability to batch processing. However, fluid dynamics and local reaction product buildup can lead to variation of etch rates across samples in the same bath.

Moreover, delicate devices often have difficulties surviving the mechanical forces of the bath and subsequent drying processes. Also, insufficient drying can ruin small components. While there are myriad uses for wet processing, in this work it was mainly used to strip organic materials, to pattern or remove oxide and silicon films, and to etch glass. The common "piranha" solution used to remove organics and metals consists of a 1:3 mixture of hydrogren peroxide and sulfuric acid.

3.1.5 Deep Reactive Ion Etching

Deep Reactive Ion Etching (DRIE) is a variation on RIE which uses alternating polymer deposition and directed plasma etching to achieve high-aspect-ratio anisotropic removal of substrate material. It is also commonly known as the Bosch Process. The etch step employs sulfur hexafluoride plasma which eschews fluorine radicals that react with the silicon. The etch rate drops with the depth of the target surface (diffusion limitation) and the exposed area (reaction loading). This technique is used to form the features seen in the silicon components of this work ranging from a few micrometers deep to through etches of the millimeter-thick base layer.

3.1.6 Anodic Bonding

When multiple wafers need to be semi-permanently or permanently fused, there are several bonding techniques to choose from. In this work, anodic bonding was used to permanently fuse the three layers of the thruster frame. In anodic bonding, two substrates are held between opposite polarity electrodes, inducing an electric field within the material. Depending on the material composition, charge carriers will flow to one or both surfaces. With the correct setup, depletion or concentration of charge can occur at the substrate interface and precipitate a chemical reaction between the surfaces resulting in the formation of a continuous material. In this work, anodic bonding between bare silicon and Pyrex was performed twice per frame stack. At high temperature (250-400 °C), transport of sodium ions away from the contact area results in a negative volume charge near the interface. A corresponding positive

volume image charge gathers in the silicon, and the strong electric field between the two pulls oxygen ions from the glass which react with the silicon crystal to form a siloxane bonding layer.

3.1.7 Wafer Dicing

As the basic raw material for processing is much larger than any individual device, it is common to process many devices on one substrate in parallel. Once wafer-level processing is complete, the devices are separated out. This is achieved in this work by using a dicing saw. The dicing saw uses a thin, rotating blade controlled on a vertical stage to precisely cut into a wafer on a planar translational and rotational stage. Micrometer precision is achievable and the most commonly used blade was 240-μm thick.

3.2 Thruster Frame and Extractor Layer Manufacturing

Herein is presented the manufacturing process for forming the thruster frame and extractor components. Considerations which drove the process choices are explained and the steps are given in some detail. More detail on the process specifics (chemicals, tools, settings) is available in Appendix A. Challenges encountered on the road to manufacturing success are discussed with corresponding solutions or workarounds given.

3.2.1 Materials

The thruster frame, extractor frame, and unibody extractor were all formed from silicon and glass 150-mm wafers. All of the silicon wafers used were formed in the $\langle 100 \rangle$ crystal orientation and had both sides polished flat and smooth. Because the components are not used for integrated circuits, the conductivity of the silicon wafers was not considered critical.

For rigidity, and to enable the deep interlaced trench etches of the iEPS 2.0 and 2.1 designs, base layer wafers were chosen to have a nominal 1-mm thickness. The combined thickness of the insulating and alignment layers was made one millimeter to conform to the heritage emitter substrate thickness and were nominally 500-μm thick each. The thickness of extractor frame only needed to match or exceed the combined corner recess depth and extractor thickness, and optionally the accelerator thickness and grid separation distance. Surplus alignment layer wafers were used for the grid frame manufacturing. Because of the SOI-based design of the unibody extractor, the thickness was limited to the available combinations of device and handle thicknesses; in consideration of assembly ease a minimum 150-μm device layer was chosen for the corner recesses which resulted in a handle thickness range of 500- to 600-μm.

3.2.2 Wafer Preparation

Before any other processing steps are begun, basic cleaning is performed on all wafers, and for the plain silicon wafers, an oxide layer is grown. When delivered from the manufacturer, the double-side-polished (DSP) silicon, silicon-on-insulator (SOI), and Pyrex wafers are obstensibly clean, however as a precaution they all undergo piranha cleaning in order to remove any particulates. Furthermore, the silicon wafers are run through a traditional Radio Corporation of America (RCA) clean to prepare them for high-temperature processing. The RCA clean removes particulates and metals which can irreversibly contaminate oxidation tools.

Once RCA-cleaned, the silicon wafers are thermally oxidized in the presence of steam to grow a 0.5 μm layer of silicon dioxide. This layer is not critical for insulation, so rapid growth is acceptable; its main purposes are to protect the pristine silicon surface so that it is prime for bonding and to provide a hard mask film for short DRIE etches. This process is highly amenable to batch processing with the possibility of oxidizing hundreds of wafers at once. Wafers slated for the base layer, alignment layer, and multi-component extractor grid frame undergo this oxidation.

3.2.3 Base Layer

Out of the three layers that make up the thruster frame, the base layer was the only one to undergo design changes in moving from iEPS 2.0 to 2.2F. Despite these changes, the manufacturing process for the layer remained fairly static—changes came in the form of new mask designs and different etch depths. In short, the processing involves oxidation of the wafer, patterning of nested and primary masks, DRIE through the wafer, and DRIE of nested features. Challenges seen in the manufacturing of the base layer were a direct result of the deep etches employed in forming the through features in the thick wafer.

Process Design

Three levels of features were included in the base layer, two of which were on the upper face. Thus, a nested mask patterned in the thermally-grown oxide was used to etch the upper face recess everywhere but the corner pedestals. The deep etches, especially those of iEPS 2.0 and 2.1 utilized two coats of thick photoresist to ensure that the mask lasted until etch-through. In iEPS 2.2 and beyond, the deep etch on the top side was much shallower (0 to 200 μm), so only a single coat of thick resist was needed. For iEPS 2.2F, should no chip bed be desired, the wafer could be replaced with a single-side polished wafer. Because the pedestal etch was done after etch-through, the wafer was mounted to a handle so that it was compatible with the DRIE tool.

Process

The base layer manufacturing process is shown conceptually in Figure 3-1 and summarized in Table 3.1. The process begins during wafer preparation when the silicon is decontaminated, stripped of native oxide, and then a thin oxide film is grown. The wafer is then prepared for coating with photoresist by depositing HMDS. A layer of thin photoresist is spun on to a thickness of about one micrometer. After a short curing step, the wafer can be mounted in order to coat the other side identically.

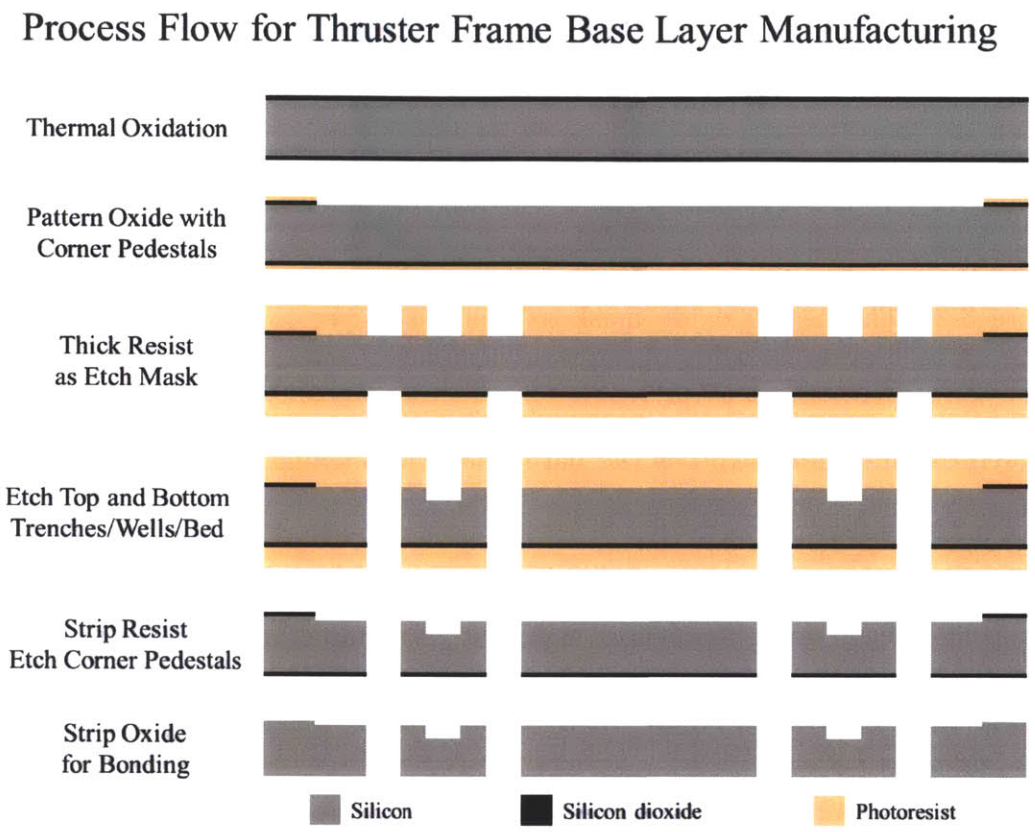


Figure 3-1: The base layer manufacturing process is summarized in cross-section form.

After curing, this photoresist is then exposed to intense UV light on top with the pedestal feature mask shown in Figure 3-2. The thin resist is developed to expose the silicon where energized with UV and fully cured to set it. A buffered oxide etchant is used to pattern the oxide layer, and the photoresist is then stripped in a piranha solution.

HMDS is again deposited to promote adhesion of thick photoresist. A coat is applied to both sides with a short cure in between. An additional coat is given to the bottom and then also to the top if extra-deep etching is expected there. The resist is then cured. Interval exposure is used to pattern the top and bottom with their respective deep etch masks as depicted in Figure 3-3, both aligned to the pattern etched in the oxide layer. Intervals of exposure and rest prevent the polymer from overheating, yet still deposit the required exposure energy. Development of both sides is performed simultaneously, and the resist is cured to fully set. Another dip in

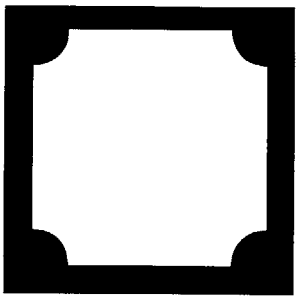


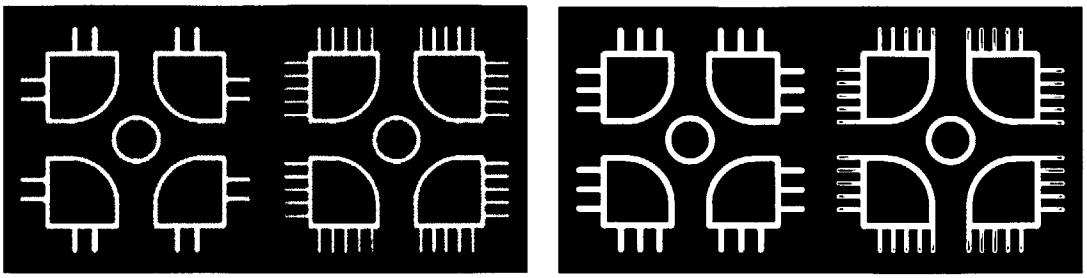
Figure 3-2: The nested oxide mask on the base layer top side defines the corner pedestals to prevent bonding of the insulating layer to the central area of the frame.

buffered oxide etchant exposes the bare silicon for etching. At this point the wafer top side would appear as in Figure 3-4.

Monitoring the etch rate and depth, the top and bottom sides are etched to the appropriate depth doing the deeper etch first. If required, a handle wafer is mounted before etch through occurs to prevent tool damage. After etch through, the base layer appears as in Figure 3-5. The handle is dismounted (if used), the photoresist is stripped in piranha solution, and the wafer is mounted to the handle with the top exposed. Using the oxide mask on the top side, the pedestals are defined by etching the exposed face by 20 to 30 μm. The base layer wafer is then dismounted and cleaned in preparation for bonding.

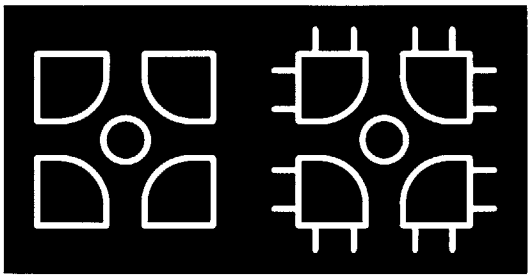
Challenges

The systematic issues encountered in the manufacturing of the base layer directly stemmed from the deep etches required to create through holes. In the iEPS 2.0 and 2.1 designs, the photoresist masking the deep trench etches needed to hold up against a 750 μm DRIE. This meant applying thick resists, usually in multiple layers. During etching, pinholes in the resist would appear and expose the silicon to the plasma in small (approximately 0.5 mm) spots scattered across the wafer surface. These appeared at a time in the etch such that they were only a few hundred micrometers deep on average at etch completion; however, by chance it would sometimes happen that pinholes on opposite sides would line up and be deep enough to etch through. Through holes in the final wafer caused issues when near the edges where the vacuum

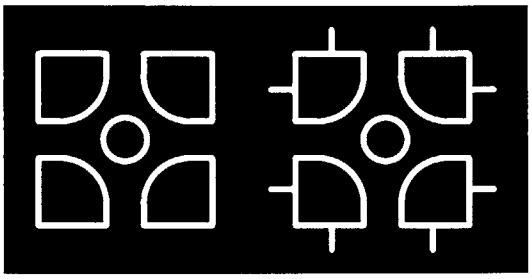


(a) iEPS 2.0 Bottom

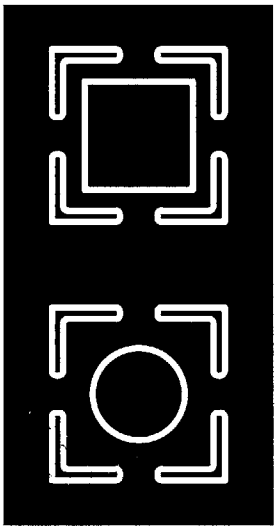
(b) iEPS 2.0 Top



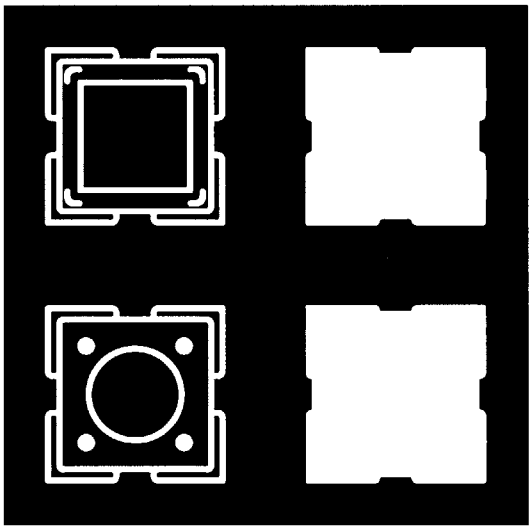
(c) iEPS 2.1 Bottom



(d) iEPS 2.1 Top



(e) iEPS 2.2 Bottom



(f) iEPS 2.2 Top

Figure 3-3: These are the masks used for the top and bottom of the base layer. Multiple designs were included in each mask until iEPS 2.2F when the square port and chip bed were downselected (upper mask in (e) and upper right mask in (f)).

system of the bonding aligner was meant to take hold. The inability to lift the base layer wafers led to repeated failed alignment attempts and often forced manual alignment under a microscope.

The source of the pinholes was likely the use of multiple layers of resist. Applying multiple layers requires a non-standard curing schedule in which the first layer is

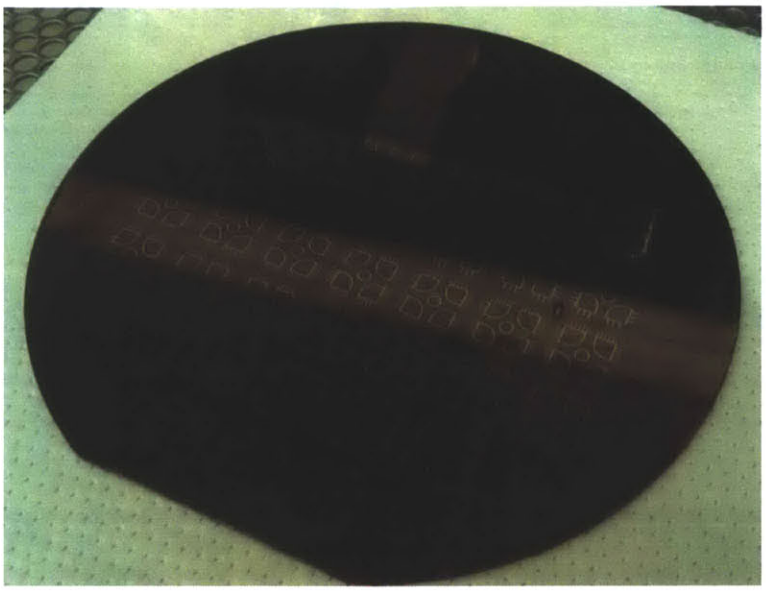


Figure 3-4: A base layer wafer is coated in thick photoresist in preparation for deep DRIE. Note the faint pattern of the nested oxide mask underneath the photoresist patterned with the iEPS 2.0 top mask.

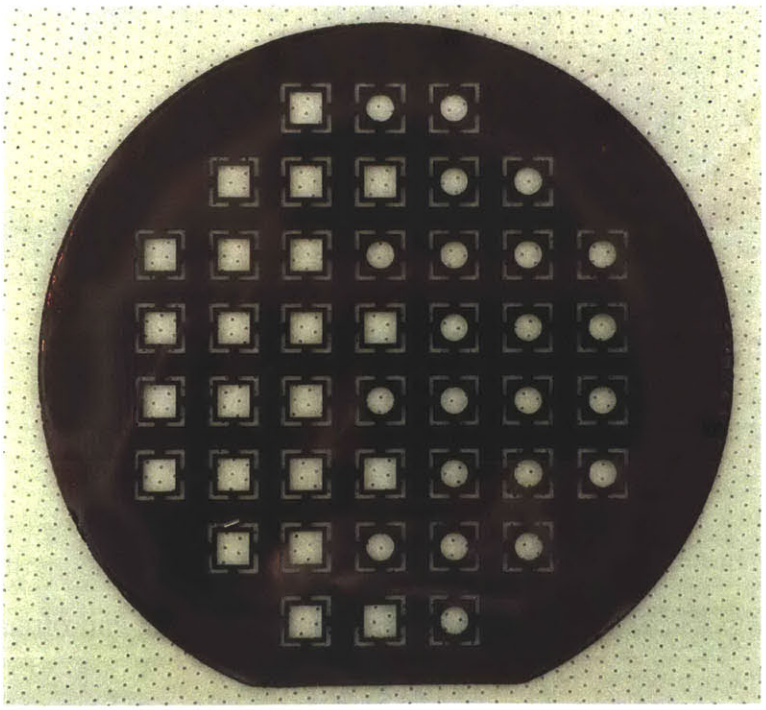


Figure 3-5: A base layer has been etched through with the iEPS 2.2 design.

Table 3.1: Base Layer Summarized Manufacturing Process Flow

Material: ⌀150 mm × 1 mm DSP ⟨100⟩ silicon wafer		
Step	***Process***	***Specifics***
0.0	**RCA Clean**	
1.0	**Wet Thermal Oxidation**	Grow 500 nm
2.0	**Nested Mask Patterning**	
.2	Thin resist coating	Top side, 1 μm
.4	Pattern exposure	Masks: Top: pedestal
.5	Develop	
3.0	**Oxide Patterning**	
.1	Buffered oxide etch	Clear exposed oxide
.3	Strip resist	Piranha
4.0	**Etch Masking**	
.2	Thick resist coating	Both sides, design-specific thickness
.4	Pattern exposure	Masks: Top: chip face, Bot: base bottom
.5	Develop	Both sides simultaneous
5.0	**Oxide Patterning**	
.1	Buffered oxide etch	Clear exposed oxide
6.0	**Deep Feature Etching**	
.3	Bottom side etching	Etch to design-appropriate depth
.7	Top side etching	Etch through
.10	Strip resist	Piranha
.13	Top side etching	Etch pedestal height (25 to 30 μm)

partially cured in order to deposit the second. This split curing process appeared to cause either the trapping of gases in the the resist or incomplete curing. Attempts to solve the problem with longer cure times resulted in compromised photoresist before etching even began. The only solution found was to mask the wafer edges during etching with vacuum-compatible adhesive tape, a time-consuming and highly-manual process.

3.2.4 Insulating Layer

The conceptual process for manufacturing the insulating layer did not change throughout the device design cycle, however the process details required tweaking and experimentation. While Pyrex is a fairly common MEMS material, it is not commonly etched very deeply, rather it is used as a protective layer and viewing window for device operation. The basic process for feature formation was based on work done by K. Payer, an MTL staff member, on etching microfluidic channels in glass.

Process Design

Two main factors determined the design of the manufacturing process for the insulating layer: the resistance of glass to standard MEMS etching processes in concert with the need for through holes.

The most effective method of etching glass is to use hydrofluoric acid which dissolves the amorphous material isotropically. Hydrofluoric acid affects silicon at a negligible rate over the time scales of the glass etch, so polysilicon film was chosen for the etch mask. Because the etch is isotropic and the rest of the frame features are etched anisotropically, the etch mask for the insulating layer needed to take this into account. Accordingly, the mask uses only a thin exposed area, offset 250 μm inward to the frame from the corresponding base and alignment layer features. This results in the horizontal etch progression meeting the correct location once the depth has reached the wafer center plane.

Achieving symmetry in the layer shape meant etching through from both sides, requiring that the polysilicon etch mask would need be patterned on both sides. Rather than etch the alignment marks solely into the polysilicon which both forces it through additional (damaging) handling and risks over-development of one side of the photoresist mask, the alignment marks were shallowly etched into the glass itself with a buffered oxide etchant.

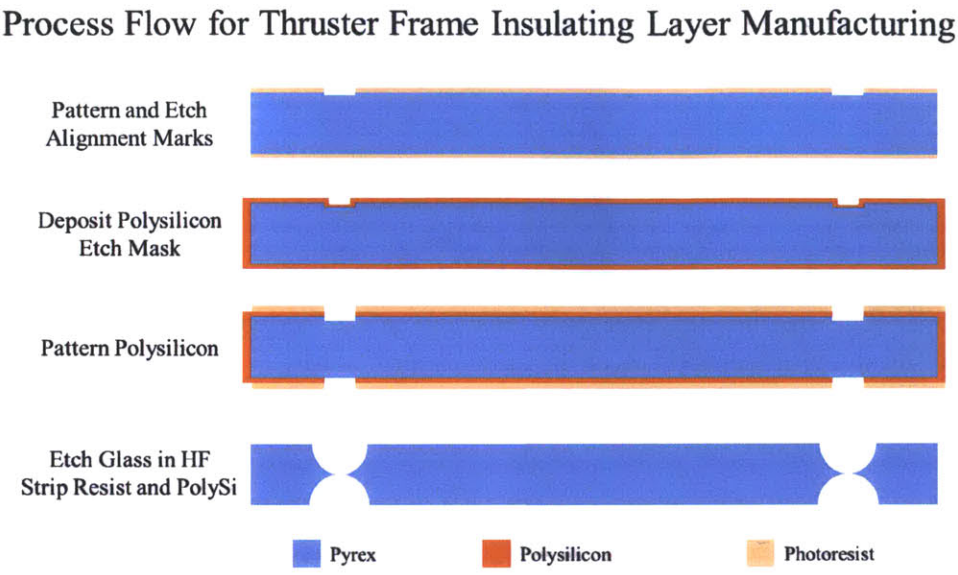


Figure 3-6: The insulating layer manufacturing process is summarized in cross-section form.

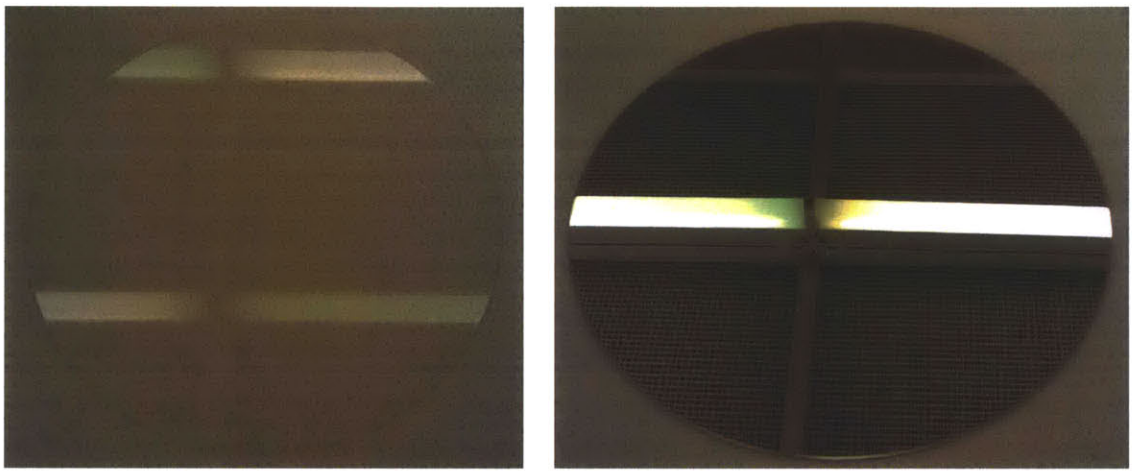
Process

The insulating layer manufacturing process is shown conceptually in Figure 3-6 and summarized in Table 3.2. A piranha clean and HMDS coating are used to prepare the wafers for spin coating on both sides with a micrometer of thin photoresist. After curing, the resist is exposed to ultraviolet light on one side with the mask shown in Figure 3-7. The exposure time is increased by about 50% from that used on silicon substrates to account for energy lost to transmission through the transparent substrate. Development and complete curing of the polymer is followed by a buffered oxide etch to pattern the glass with the alignment features to a depth of 250 nm. The resist is stripped in piranha to prepare the Pyrex for polysilicon deposition.

In a furnace, polysilicon is deposited to a thickness of 250 nm or more. The difference before and after deposition is highlighted in Figure 3-8. After HMDS, another coat of thin resist on both sides, and curing; the same mask as before is aligned to the etched alignment marks and patterned to both sides. The pattern is developed, the alignment marks are coated in resist, and the resist is fully cured. A short plasma etch is used to remove the polysilicon from the wafer where exposed.

Hydrofluoric acid is used to etch through from both sides at an overall rate of

Figure 3-7: The insulating layer only has one mask to define the etch lines on both sides for the deep anisotropic etch in hydrofluoric acid.



(a) (b)

Figure 3-8: A Pyrex insulating layer wafer is shown before and after polysilicon deposition. The polysilicon acts as an etch mask against hydrofluoric acid

about 5 μm/min for a 49% HF solution. After rinsing, the resist is stripped in a piranha solution. A 1:20:20 by volume solution of nitric acid, glacial acetic acid, and hydrofluoric acid is used to remove the polysilicon mask. Another piranha clean prepares the wafer for bonding. The final condition of the insulating layer wafer is featured in Figure 3-9.

Challenges

Difficulties in processing the insulating layer stemmed from the fragility of the polysilicon mask, fragility of the wafers, and directly or indirectly from the optical transparency of glass. Transparency affected both the initial photolithography used to pattern the wafer with alignment marks and the experimentation with the etch time

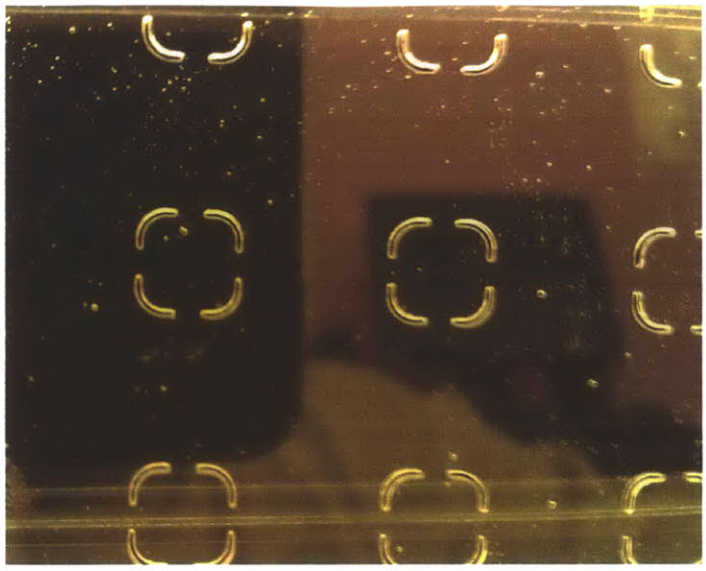


Figure 3-9: Through holes are seen in the insulating later after the hydrofluoric acid etch and removal of the photoresist and polysilicon films. The pitting seen is a result of defects in the polysilicon layer due to imperfect deposition and damage during handling.

for the glass, while the fragility of the polysilicon film reduced the quality of the final etched product. Wafer fragility simply reduced the production yield until experience led to added precaution, especially during or after specific processes.

Photolithograpy on Transparent Substrates

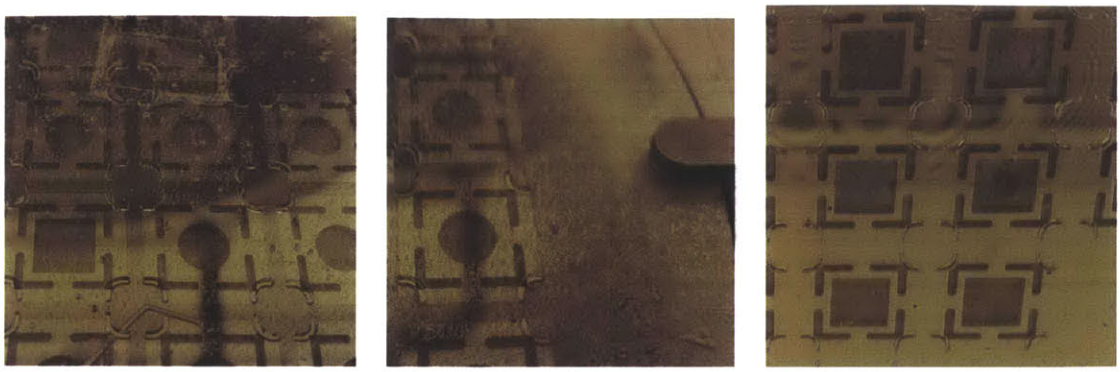
Following the standardized procedure for exposing the thin resist used in the MTL, the buffered oxide etch for patterning the glass with alignment marks seemed to have no affect on the Pyrex. Inspection with a microscope and fluoroscope revealed no issues with the development of the photoresist; however these inspection methods were affected by the glass transparency, so what appeared to be a cleared area was actually protected by a thin layer of photoresist. Rather than extend the development time and lose fidelity in the exposed feature shape, the exposure time was increased by 50%. This resulted in excellent results. It is likely that this is necessary because of the transparency of Pyrex to the upper half of the ultraviolet wavelength spectrum, so energy which reaches the substrate surface does not reflect back into the photoresist for another chance at absorption as would happen with a polished silicon substrate.

Determination of the Pyrex Etch Rate

Table 3.2: Insulating Layer Summarized Manufacturing Process Flow

Material: ⌀150 mm × 0.5 mm Corning Pyrex 7740 wafer		
Step	***Process***	***Specifics***
0.0	**Piranha Cleaning**	
1.0	**Alignment Mark Patterning**	
.2	Thin resist coating	Both sides, 1 μm
.4	Pattern exposure	Mask: Top: insulating layer
.5	Develop	
2.0	**Alignment Mark Etching**	
.1	Buffered oxide etch	Etch 250 nm
.3	Strip resist	Piranha
3.0	**Polysilicon Deposition**	Deposit 250 nm
4.0	**Etch Mask Patterning**	
.2	Thin resist coating	Both sides, 1 μm
.4	Pattern exposure	Mask: Top & Bot: insulating layer
.5	Develop	
5.0	**Polysilicon Etching**	Expose glass for wet etching
.1	DRIE top	Etch to glass
.2	DRIE bottom	Etch to glass
6.0	**Glass Etching**	
.1	Hydrofluoric acid wet etch	Etch through
.3	Strip resist	Piranha
.5	Strip polysilicon	Hydrofluoric, nitric, acetic acid mix

The next place where the transparency of the Pyrex made processing difficult was in the determination of the through-etch time for the glass. Because of a lack of consistent literature on deep etch rates for Pyrex in hydrofluoric acid, the etch-through time was approached experimentally. Determination of etch-through during the etch process was impeded by the polysilicon mask as it obscured the small features from macroscopic assessment. Viewing the etched features under a microscope was difficult because the difference between a through hole and a thin layer of transparent glass was nearly imperceptible, especially during the first experiences of attempting to



(a) (b) (c)

Figure 3-10: Wafers with flawed polysilicon masking are shown in (a) and (b) with scarring resulting from unintended contact with the hydrofluoric acid during etching. The wafer in (c) had a thicker polysilicon film which held up better to handling and does not exhibit scarring. A base layer is used as a background (bonded in the case of (a) and (b)).

gauge the difference. Luckily, the precision of the etch is not critical to the assembly of the device and etch through is simply verified by blowing compressed air through the wafer and looking for evidence of a through flow. This method is destructive to the released portion of the polysilicon mask, but now that the approximate etch time is known, a slight over-etch is used to mitigate failure.

Polysilicon Etch Mask Quality

As an etch mask, polysilicon works very well against hydrofluoric acid. The only issue encountered was that if the film is too thin, it is easily scarred during basic handling. These scars, while minor or imperceptible beforehand, lead to large trenches and pits in the Pyrex wafer after etching. Since they appear everywhere, the flaws can coincide with areas meant for bonding to the base and alignment layers and reduce the strength of the bond. Additionaly, the already fragile glass is further weakened by the removal of material. An appropriate thickness of polysilicon leaves a mirror finish that only appears slightly translucent. A 250- to 300-nm thickness should be sufficient. The effects of mask scarring can be seen Figure 3-10.

Substrate Fragility

Finally, the Pyrex wafers themselves are much more fragile than the silicon wafers, so care must be taken in their handling to prevent accidental cleaving. Wafers tended to

break after high-temperature processes or rough mechanical handling such as polysilicon deposition, piranha cleaning, or spin drying. For example, four of six wafers that had just undergone the furnace process of polysilicon deposition were broken during removal from the tool.

3.2.5 Alignment Layer

Like the insulating layer, the manufacturing process of the alignment layer remained static through the design iterations of iEPS 2.x. As the simplest to manufacture, the alignment layer posed few challenges.

Process Design

Processing for the alignment layer was fairly simple to design as it has no complex features or difficult vertical dimensional requirements. Similar to the base layer and extractor grid, the multiple features on the top side utilized the thermally-grown oxide as a mask. Unlike those layers, the oxide mask etch did not need to be nested as it was very shallow and could be subsequently patterned with thick photoresist. An alternate process order could be used as in the base layer, and the alignment crosshairs could be etched after the deep etches on both sides, but doing so would require mounting to a handle wafer which is unnecessarily time consuming.

Process

The alignment layer manufacturing process is shown conceptually in Figure 3-11 and summarized in Table 3.3. The process begins during wafer preparation when the silicon is decontaminated, stripped of native oxide, and then a thin oxide film is grown. The wafer is then prepared for coating with photoresist by depositing HMDS. A layer of thin photoresist is spun on to a thickness of about one micrometer. After a short curing step, the wafer can be mounted in order to coat the other side identically. After curing, this photoresist is then exposed to intense UV light on top with the corner post alignment mark mask shown in Figure 3-12. The thin resist is developed

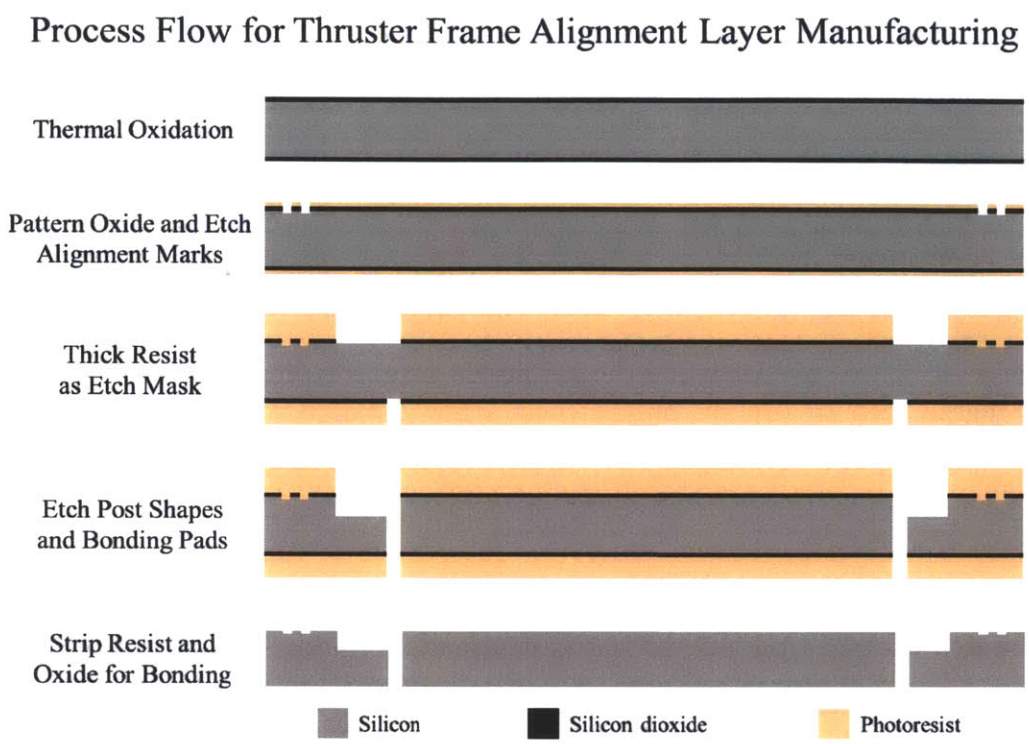
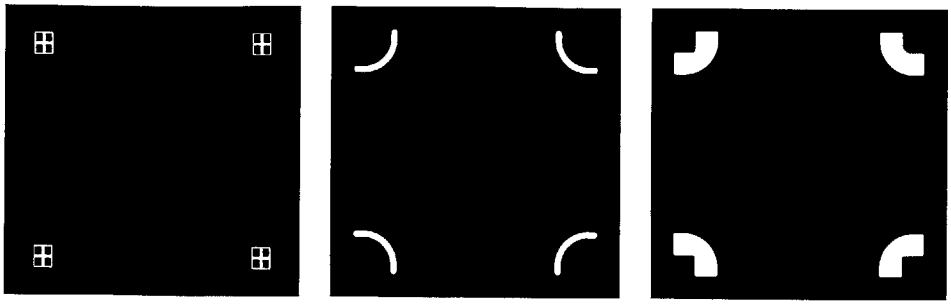


Figure 3-11: The alignment layer manufacturing process is summarized in cross-section form.

to expose the silicon where exposed to UV and fully cured to set it. A buffered oxide etchant is used to pattern the oxide layer, and the photoresist is then stripped in a piranha solution.

A short DRIE etch is used against the patterned oxide to define the alignment marks to a depth less than one micrometer. HMDS is again deposited to promote adhesion of thick photoresist. A coat is applied to both sides with a short cure in between, and then resist is cured before exposing. Interval exposure is used to pattern the top and bottom with their respective deep etch masks as depicted in Figure 3-12, both aligned to the pattern etched in the oxide layer. Intervals of exposure and rest prevent the polymer from overheating, yet still deposit the required exposure energy. Development of both sides is performed simultaneously, and the resist is cured to fully set. Another dip in buffered oxide etchant exposes the bare silicon for etching.

Monitoring the etch rate and depth, the top and bottom sides are etched to the appropriate depth, doing the deeper (bottom) etch first. If required, a handle



(a) (b) (c)

Figure 3-12: Three masks define the alignment layer features. The corner post alignment marks seen in (a) are only etched a few hundred nanometers where as the bonding pads edges and corner post shapes in (b) and (c), respectively, are etched through.

wafer is mounted before etch through occurs to prevent tool damage. The handle is dismounted (if used), the photoresist is stripped in piranha solution, and the wafer is stripped of oxide in preparation for bonding.

Challenges

The alignment layer did not present any problems of significant difficulty. Only when the corner post alignment marks were etched too deeply ($> 1\mu$m) was there the issue of an inability to coat the wafers evenly with photoresist for deep etching. This was easily avoided after the initial mistake.

3.2.6 Thruster Frame Bonding and Dicing

Forming the thruster frame from the component layer wafers required cleaning, alignment, bonding, and dicing. While none of these steps is uncommon, the latter three presented specific challenges which led to the implementation of small process changes in order to improve rates of success.

Process Design

Dicing did not receive any special design consideration, though special techniques were implemented as discussed in the Challenges section, below. Bonding the glass between

Table 3.3: Alignment Layer Summarized Manufacturing Process Flow

Material: ⌀150 mm × 0.5 mm DSP ⟨100⟩ silicon wafer		
Step	***Process***	***Specifics***
0.0	**RCA Clean**	
1.0	**Wet Thermal Oxidation**	Grow 500 nm
2.0	**Nested Mask Patterning**	
.2	Thin resist coating	Both sides, 1 μm
.4	Pattern exposure	Masks: Top: alignment crosses, Bot: bonding pad
.5	Develop	Both sides simultaneous
3.0	**Oxide Patterning**	
.1	Buffered oxide etch	Clear exposed oxide
.3	Strip resist	Piranha
4.0	**Alignment Mark Etching**	Etch 1 μm deep on top side
5.0	**Etch Masking**	
.2	Thick resist coating	Both sides, design-specific thickness
.4	Pattern exposure	Masks: Top: post shapes, Bot: bonding pad
.5	Develop	Both sides simultaneous
6.0	**Oxide Patterning**	
.1	Buffered oxide etch	Clear exposed oxide
7.0	**Deep Feature Etching**	
.3	Top side etching	Etch to design-appropriate depth
.7	Bottom side etching	Etch through
.10	Strip resist	Piranha

two silicon wafers was considered somewhat experimental. Based on literature, the initial bond was to be halted before the current decayed to near-zero, specifically at 15 mA [11]. Experimentation led to running the second bond a second time to ensure charge depletion was complete.

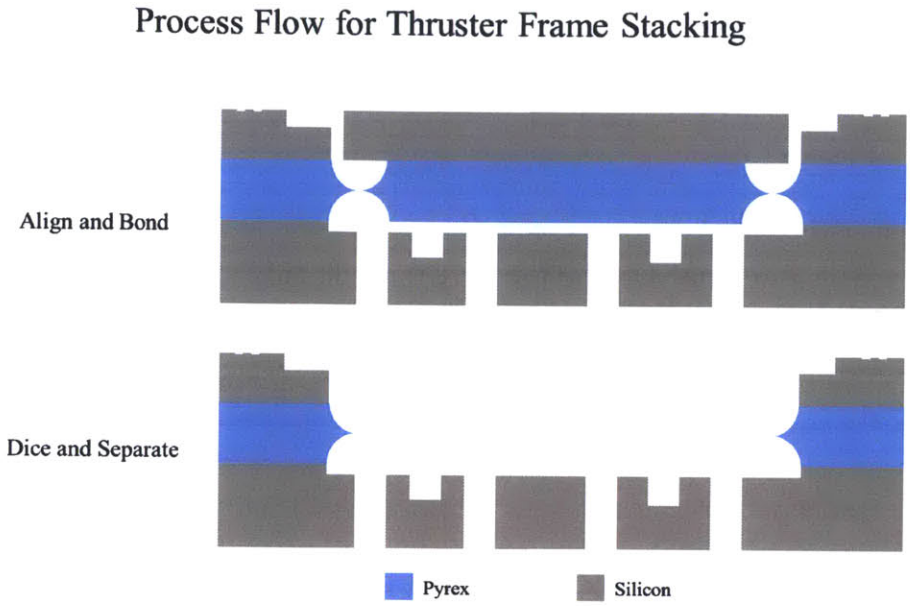


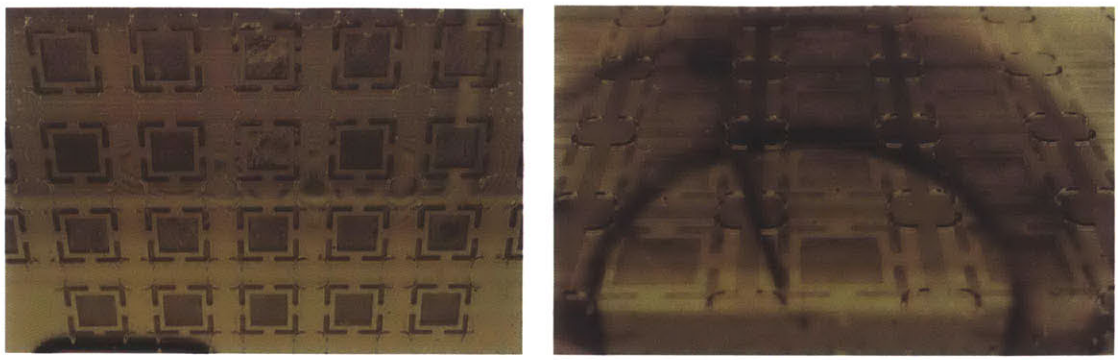
Figure 3-13: The thruster frame bonding and dicing process is summarized in cross-section form.

Process

The process for stacking, bonding, and dicing is shown conceptually in Figure 3-13 and summarized in Table 3.4. To begin, all three thruster frame layers are thoroughly cleaned in piranha solution and the silicon surfaces are stripped of native oxide with a buffered oxide etchant. The insulating layer and one of the other layers are aligned with a microscope and stage. After clamping in the aligned position, the alignment is inspected under a microscope.

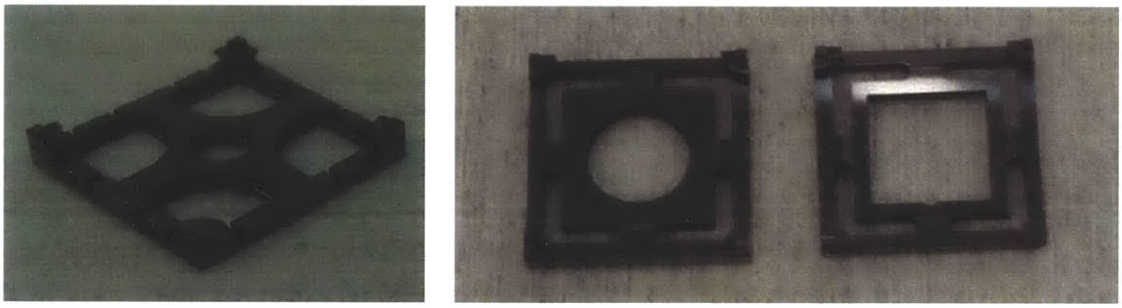
The wafers are then placed in the bonding tool, raised to a temperature at which the glass conducts (250 to 400 °C), and compressed. A high potential (800 V) is placed across the wafers with the Pyrex wafer as the negative electrode. The current is flowed until the value has decayed to about 10 % of the initial current and then the wafers are cooled. The insulating and base layers are shown before and after bonding in Figure 3-14.

Returning to the alignment tool, the bonded pair is aligned and clamped to the remaining silicon layer. The alignment is inspected by looking through the holes in the alignment or base layer and observing macroscopic symmetry across the dies.



(a) (b)

Figure 3-14: Wafers are shown before (a) and after (b) anodic bonding. Notice the darkening of the image where bonding has occurred and no air gap remains between the insulating and silicon layers.



(a) (b)

Figure 3-15: Diced and separated frames are shown from the iEPS 2.1 (a) and 2.2 (b) designs.

The wafers are then placed in the bonding tool, raised to temperature again, and compressed. This time the high potential is placed across the wafers with the bonded pair as the negative electrode (effectively the Pyrex again). The current is flowed until the value has decayed to near-zero (< 0.5 mA) and the wafers are cooled.

To separate the bonded frames from one another, the wafer is diced. Depending on the dicing tool used, precautions may need to be taken as described in the Challenges section below. Once separated, the thruster frames appear as in Figure 3-15.

Challenges

Stacking, bonding, and dicing of the iEPS 2.x frame wafers has been the manufacturing stage most consistently fraught with issues. Some of them stem from imperfections

Table 3.4: Thruster Frame Stack Manufacturing Process Flow

Material: Base layer, insulating layer, alignment layer wafers		
Step	***Process***	***Specifics***
0.0	**Wafer Surface Cleaning**	
.1	Remove particles	Piranha all frame layers
.3	Expose silicon surface	Buffered oxide etch on base and alignment layers
1.0	**Wafer Alignment**	Between silicon and Pyrex layers
2.0	**Anodic Bonding**	
.2	Heating	Increase stack temperature
.4	Apply voltage	Glass at high negative potential
.5	Remove voltage	Stop at cutoff current value
.6	Cooling	Allow stack to cool
3.0	**Wafer-stack Alignment**	Between stack and remaining silicon
4.0	**Anodic Bonding**	
.2	Heating	Increase stack temperature
.4	Apply voltage	Glass at high negative potential
.5	Remove voltage	Stop after nearly fully decayed
.6	Cooling	Allow stack to cool
5.0	**Dicing**	
.3	Cut first direction	13 mm die width, 3 mm separation
.5	Cut second direction	13 mm die width, 3 mm separation
6.0	**Separate Dies**	Soak in acetone or UV

in the component wafers, some from the difficulty of the uncommon bonding arrangement, and some from the design of the structures. Device yield has improved over the course of the project due both in part to design changes and to experience with the manufacturing process.

Wafer-to-wafer Alignment Issues

Alignment between wafer pairs encountered three main issues: manufacturing oversights reducing process flexibility, wafer defects preventing tool operation, and tool flaws introducing alignment error. With experience, each of these came to be miti-

gated through workarounds.

Unfortunately, there were production runs in which wafer-level alignment marks were not etched into the underside of the base layer. This occurred either as an oversight in etching or due to an oversight in the production of the base layer masks such that alignment marks were not written by the laser. Regardless, this flaw prevented flexibility in bonding of the stack in any acceptable permutation. Because of the way the alignment tool functions, not having underside alignment marks on the base layer requires that the base layer be lifted by the machine. If the alignment marks had been there, bonding order would have been flexible enough to skirt around the issue of edge through holes.

As mentioned in the manufacturing challenges of the base layer, incidental through-hole formation at the wafer edges sometimes prevented the bonding aligner from grasping the wafer for alignment. The through holes were prevented in subsequent runs via manual masking with polyimide tape during deep etches. In cases where the edge through holes were an issue, the wafer was repeatedly translated and rotated within the acceptable bounds for alignment until the vacuum was able to draw tightly enough to lift the wafer. This weak vacuum undoubtedly led to some shifting during alignment. When the aforementioned method failed, the Pyrex and base layers were aligned manually under a microscope and clamped for bonding. Though not ideal, manual alignment still yielded average results.

Finally, the reality of an imperfect alignment tool led to poorer alignment than is possible. Errant contact during close proximity, inexact focal planes, and uneven clamping are common with the alignment tool, but with experience these can be avoided and mitigated. Initially, though it cannot be easily checked, alignment was likely off by about 15 to 20 μm at the alignment marks. With an understanding of the quirks of the tool, the alignment has been improved to less than 5μm misalignment and usually near exact at the marks.

Non-standard Bonding Configuration

While anodic bonding is one of the more robust MEMS bonding processes, and it is often used for sandwiching silicon between glass substrates, the sandwiching of glass

between silicon wafers is uncommon and resulted in unpredictable behavior and thus unknown bond quality. It is expected that in an anodic bond, the current drawn at a specific voltage will decay exponentially as charge is depleted and an insulating layer forms. This was the general behavior seen during the first of the two bonds. However, during the second bond, the behavior was often erratic, sometimes appearing to have a background decay behavior and sometimes not, as observed by Despont [11]. In some trials, a repeat of the second bond was observed to behave with a smooth current decay as seen with the first bond, however this was not a consistent finding. The current decay for one such case is presented in Figure 3-16. In some cases, compression and electrostatic forces inside the bonder crushed regions of the wafer and shorted the stack during bonding, so the full current decay was not achieved. Regardless, the bond seemed to take hold, though possibly weakly, as long as current flowed through the wafer stack (and not through a short) at a level of around ten milliamperes for at least a few tens of seconds.

Barriers to Simple Dicing

Dicing of the wafer stack was made difficult solely because of the presence of the glass layer—a more robust blade was necessary to cut through it. Despite the use of a specialty blade, the two millimeter stack still requires three or four passes to cut each line. Moreover, the blade slowly wears down, so the vertical height settings for automated cutting need to be periodically adjusted. All in all, these factors result in the dicing process taking several hours. During this time, the water lubricating the saw softens the adhesive tape which helps the vacuum chuck hold the wafer pieces in position as they are cut. By the time cutting is three-quarters complete, dies begin to release from the tape and are damaged by the saw or begin to flush away with the water stream. This was especially detrimental during initial runs when whole columns of dies would release and shift and thus require individualized dicing later.

Through experience, dicing has been made an efficient, successful process. A top layer of tape is used to help keep the dies drier during dicing; the water flow level is reduced to near minimum safe level; and the cuts are made in an order such that once the tape releases, only individual dies shift and can be salvaged.

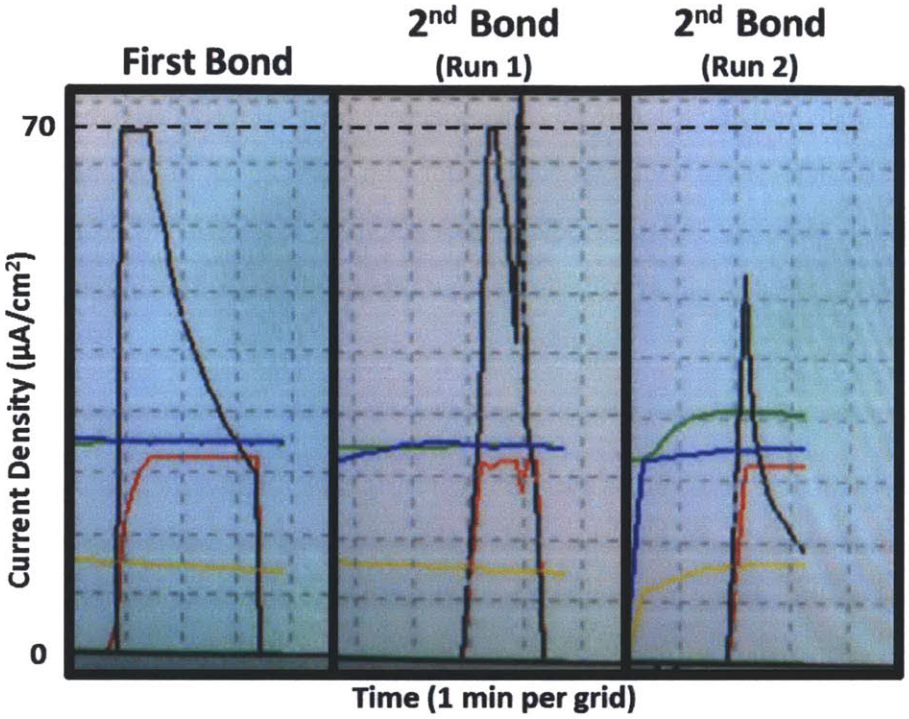


Figure 3-16: Here are shown the observed current draws (black) for the bonding of one frame stack. The first bond decays as expected, however the second bond is erratic. A re-attempt of the second bond exhibits the desired decay characteristic. This result is not consistently repeatable. The other traces are wafer temperature (blue, green), applied potential (red), and heater control signal (yellow).

3.2.7 Extractor Frame

The original extractor frame manufacturing process was similar to that of the base layer due to their similar number of feature planes. Were the extractor frame and metal grid combination not later abandoned for the unibody extractor, the manufacturing process would more closely resemble that of the unibody extractor in order to have more control over vertical dimensions.

Process Design

Depending on the desired inter-grid spacing and the requirements on grid-to-tip separation, the process for the extractor frame manufacturing process resembles either the base layer or the unibody extractor process more. For small inter-grid spacing, the thermally-grown oxide is sufficiently thick for the initial etch of the extractor well

pattern. Should this need to be deeper, a thick PECVD oxide layer would withstand a longer etch. Important to this decision is knowing that the final separation would be less than the initial etch due to a rate decrease with depth. To achieve tight control of the grid-to-tip separation, an SOI wafer can be used as in the unibody extractor process such that the upstream aperture plane is level with the top of the corner posts. Otherwise, the separation is dependent on the etch-depth accuracy.

Process

The grid frame manufacturing process is shown conceptually in Figure 3-17 and summarized in Table 3.5. In the simplest design, the process begins during wafer preparation when the silicon is decontaminated, stripped of native oxide, and then a thin oxide film is grown. The wafer is then prepared for coating with photoresist by depositing HMDS. A layer of thin photoresist is spun on to a thickness of about one micrometer. After a short curing step, the wafer can be mounted in order to coat the other side identically. After curing, this photoresist is then exposed to intense UV light on top with the extractor key mask shown in Figure 3-18. The thin resist is developed on both sides simultaneously to expose the oxide where energized with UV and fully cured to set it. A buffered oxide etchant is used to pattern the oxide layer, and the photoresist is then stripped in a piranha solution.

HMDS is again deposited to promote adhesion of thick photoresist. A coat is applied to both sides with a short cure in between. An additional coat is given to the bottom and then also to the top if deep etching is expected on top. The resist is then cured. Interval exposure is used to pattern the top with the accelerator key mask and the bottom with the corner recesses and central hole mask as depicted in Figure 3-18, both aligned to the pattern etched in the oxide layer. Intervals of exposure and rest prevent the polymer from overheating, yet still deposit the required exposure energy. Development of both sides is performed simultaneously, and the resist is cured to fully set.

Monitoring the etch rate and depth, the top is etched with the oxide mask to define the extractor key features to a depth beyond the inter-grid separation. The

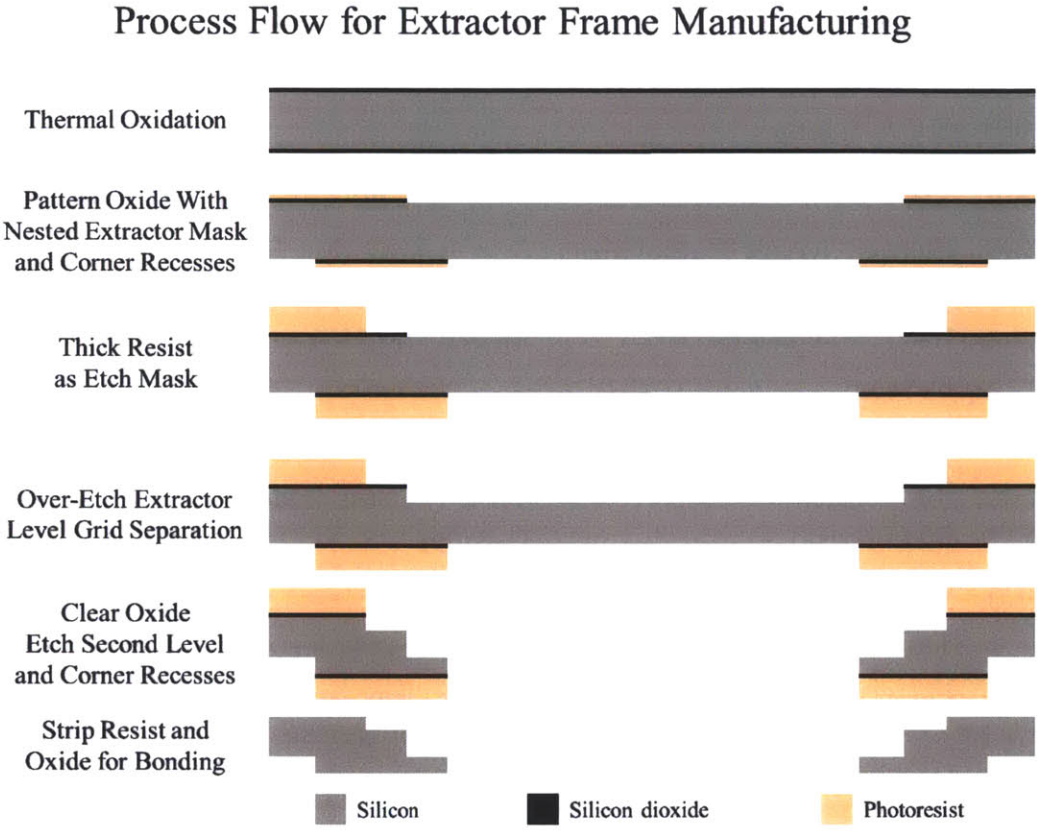


Figure 3-17: The grid frame manufacturing process is summarized in cross-section form.

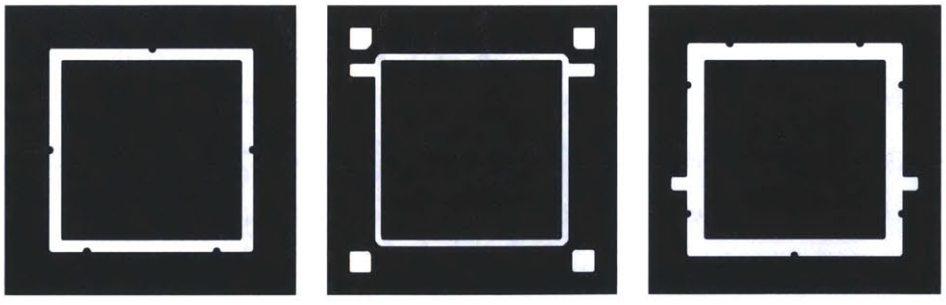


Figure 3-18: The grid frame is defined by three masks: (a) the extractor key frame, (b) the corner recesses and bottom through hole, and (c) the accelerator key frame.

Table 3.5: Extractor Frame Summarized Manufacturing Process Flow

Material: ⌀150 mm × 0.5 mm DSP ⟨100⟩ silicon wafer		
Step	***Process***	***Specifics***
0.0	**RCA Clean**	
1.0	**Wet Thermal Oxidation**	Grow 500 nm
2.0	**Nested Mask Patterning**	
.2	Thin resist coating	Both sides, 1 μm
.4	Pattern exposure	Masks: Top: extractor slot
.5	Develop	
3.0	**Oxide Patterning**	
.1	Buffered oxide etch	Clear exposed oxide
.3	Strip resist	Piranha
4.0	**Etch Masking**	
.2	Thick resist coating	Both sides, design-specific thickness
.4	Pattern exposure	Masks: Top: accelerator slot, Bot: corner and center recesses
.5	Develop	Both sides simultaneous
5.0	**Deep Feature Etching**	
.1	Top side etching	Over-etch past grid separation depth
.2	Buffered oxide etch	Clear extractor mask and bottom oxide
.5	Top side etching	Etch to leave recess depth thickness
.7	Bottom side etching	Etch to recess depth (through)
.9	Strip resist	Piranha

oxide is then etched in a buffered oxide etchant to remove the mask on top and to expose the silicon on bottom. The top side is then etched to define the accelerator key pattern and level. The etch is stopped to leave the thickness of the desired corner recess depth. The bottom side is then etched through (with a handle wafer to prevent tool damage if necessary).

After etch through, the handle is dismounted (if used), the photoresist is stripped in piranha solution, and the oxide is removed to allow conduction. A dicing saw is employed to separate the extractor grids from one another.

Challenges

Similar to the alignment layer, the grid frame process did not present significant challenges in manufacturing. Because this component was abandoned for the unibody design, the difficulties of precise deep etch control were not encountered.

3.2.8 Unibody Extractor

The unibody extractor presented the most difficult individual layer manufacturing challenges. Processes not involved in the manufacture of the thruster frame were introduced in order to achieve the desired grid thinness and conductivity. In the end, the desired control over grid thickness and uniformity were unachievable due to tool imperfections, though they should be easily achieved on state-of-the-art equipment.

Process Design

Because the unibody extractor would not have a separate, flat extractor inserted, vertical dimensions and conductivity presented more of an issue than in the extractor frame. Therefore, the unibody extractor is formed from an SOI wafer to control the emitter-aperture separation distance and uniformity and then coated in a gold layer. The thickness of the grid is determined by the depth of the initial aperture etch and the etch rate reduction with depth during the second etch. Because of the unavailability of SOI wafers with a thin (< 500 μm) handle layer, the second etch needed to be deep (> 400 μm). So that a sufficiently rigid grid remained by the time the second etch reached the buried oxide in the apertures, the over-etch of the initial aperture features necessitated a thick (1.25 μm) PECVD oxide mask. Masking of the dies as they etched through to the buried oxide was implemented due to radial etch rate non-uniformity in the tool.

Process

The unibody extractor manufacturing process is shown conceptually in Figure 3-19 and summarized in Table 3.6. Processing begins with a decontamination of the

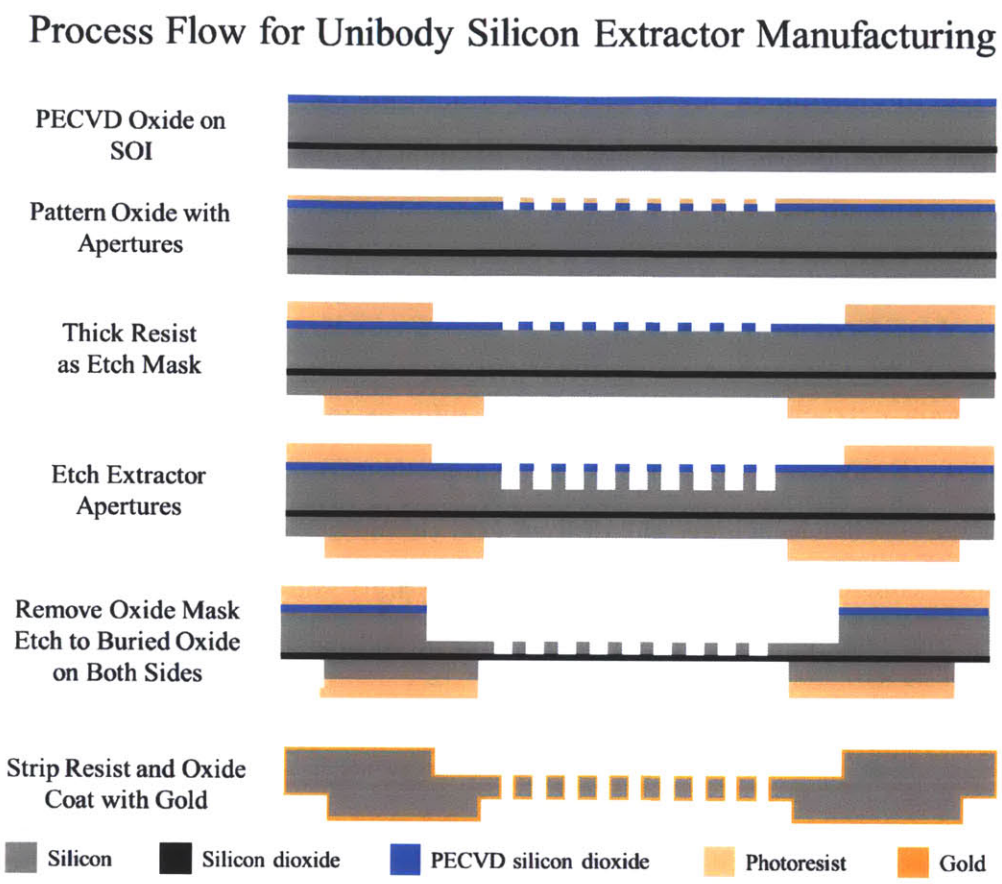
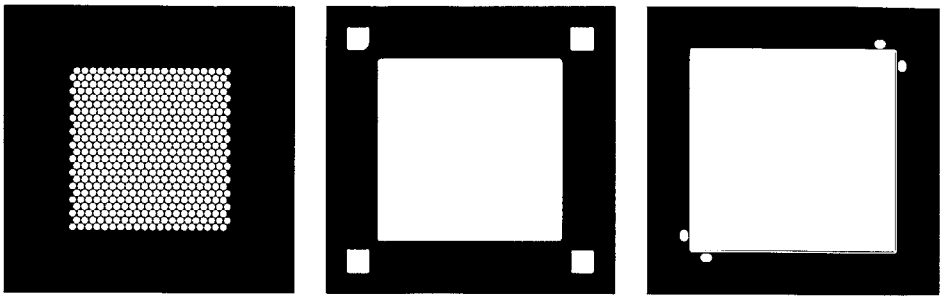


Figure 3-19: The unibody extractor manufacturing process is summarized in cross-section form.

SOI wafer in a piranha solution. A thick layer (1.25 μm) of PECVD silicon dioxide is deposited on the handle surface. The wafer is then prepared for coating with photoresist by depositing HMDS. A layer of thin photoresist is spun onto the oxide to a thickness of about one micrometer. After curing, this photoresist is then exposed to intense UV light on top with the aperture mask shown in Figure 3-20. The thin resist is developed to expose the oxide as patterned and fully cured to set it. A buffered oxide etchant is used to pattern the oxide layer, and the photoresist is then stripped in a piranha solution.

HMDS is again deposited to promote adhesion of thick photoresist. A coat is applied to both sides with a short cure in between. An additional coat is given to the handle side. The resist is then cured. Interval exposure is used to pattern the handle side with the central hole and solder well mask and the bottom with the corner



(a) (b) (c)

Figure 3-20: The unibody extractor is defined by three masks: (a) the extractor apertures, (b) the corner recesses and central hole, and (c) the grid top and solder wells.

recesses and central hole mask as depicted in Figure 3-20, both aligned to the pattern etched in the oxide layer. Intervals of exposure and rest prevent the polymer from overheating, yet still deposit the required exposure energy. Development of both sides is performed simultaneously, and the resist is cured to fully set.

Monitoring the etch rate and depth, the apertures are etched with the oxide mask to a depth beyond the desired grid thickness based on the predicted etch rate difference during the second etch. The oxide mask is then removed with a buffered oxide etchant. Using the photoresist mask, the handle etching continues until the buried oxide layer is reached in all of the apertures. Etch nonuniformity may cause certain dies to reach completion before others—this is discussed in the subsequent section. The device side is then etched through to the buried oxide layer, as well (with a handle wafer to prevent tool damage if necessary).

After etch through, the handle is dismounted (if used), the photoresist is stripped in piranha solution, and the oxide is removed to allow conduction. As soon as possible, the wafer is mounted in the vacuum chamber of an electron-beam vapor deposition tool to mitigate the formation of a native surface oxide layer in atmosphere. Titanium is then deposited as an adhesion layer (10 nm) for the subsequently deposited outer gold layer (100 nm). First the upstream aperture (device) side is coated and then then the handle side. A planetary rotating mount is used to ensure coating of the aperture interiors and even distribution of the metal layer. A dicing saw is then employed to separate the extractor grids from one another. After dicing and before separation,

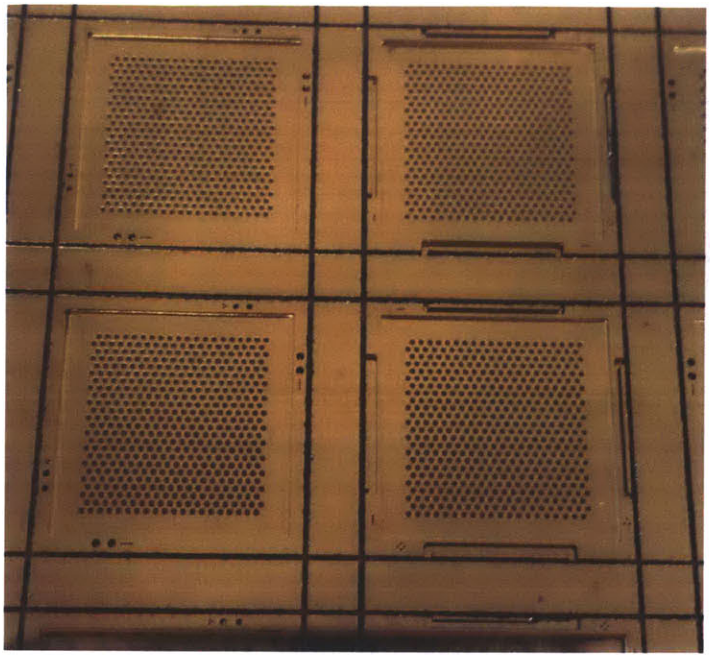


Figure 3-21: Unibody extractors are shown mounted on adhesive tape after having undergone dicing. Note the experimental solder well designs included for testing.

the grids appear as in Figure 3-21

Challenges

A major challenge in the development of the unibody extractor manufacturing process was the discovery of an extreme radial and azimuthal non-uniformity in the etch rate of the DRIE tool being used. Initial attempts at manufacturing resulted in edge dies completely losing their grid material before central dies had reached the buried oxide layer. Poor thermal conduction and incomplete oxide removal were considered as potential causes; however, improved heat conduction and ultrasonic agitation of the buffered oxide etch for the small apertures did not ameliorate the issue. Thus, an inherent spatial etch rate non-uniformity was the only remaining explanation.

The etch rate non-uniformity had not radically affected previous manufacturing efforts, because the depth accuracy was not necessarily critical between dies or the etches were shallow enough for a small spatial etch rate difference to be imperceptible. In the case of the unibody extractor, where a 500- or 600-μm total etch depth was necessary, a 5% difference in etch rate between wafer locations could result in one grid

Table 3.6: Unibody Extractor Summarized Manufacturing Process Flow

Material: ⌀150 mm × 150:0.5:500-μm Device:BOx:Handle ⟨100⟩ SOI wafer		
Step	***Process***	***Specifics***
0.0	**Piranha Cleaning**	
1.0	**Thick Oxide Deposition**	1.25 μm PECVD on handle
2.0	**Nested Mask Patterning**	
.2	Thin resist coating	Handle sides, 1 μm
.4	Pattern exposure	Mask: Handle: apertures
.5	Develop	
3.0	**Oxide Patterning**	
.1	Buffered oxide etch	Clear exposed PECVD oxide
.3	Strip resist	Piranha
4.0	**Etch Masking**	
.2	Thick resist coating	Both sides, design-specific thickness
.4	Pattern exposure	Masks: Top: aperture well, Bot: corner and center recesses
.5	Develop	Both sides simultaneous
5.0	**Deep Feature Etching**	
.1	Top side etching	Over-etch desired grid thickness
.2	Buffered oxide etch	Clear aperture mask
.5	Top side etching	Etch down to buried oxide
.7	Bottom side etching	Etch to buried oxide (through)
.9	Strip resist	Piranha
6.0	**Metal Deposition**	
.1	Buffered oxide etch	Remove deposited and native oxides
.4	Deposit adhesion layer	10 nm titanium
.5	Deposit main conductor	100 nm gold
7.0	**Dicing**	
.3	Cut first direction	13 mm die width, 3 mm separation
.5	Cut second direction	13 mm die width, 3 mm separation
8.0	**Separate Dies**	Soak in acetone or UV

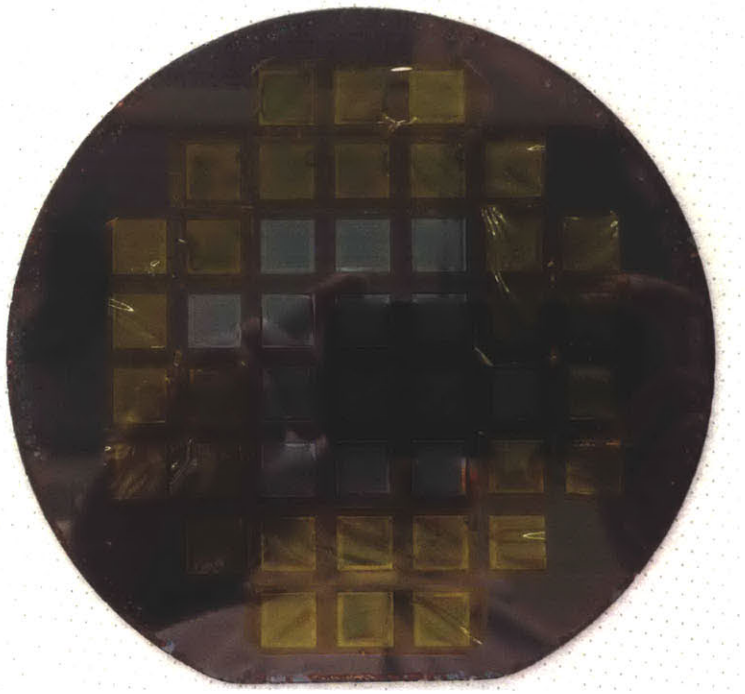


Figure 3-22: A wafer of unibody extractors is shown during the second etch to thin the grid and clear the apertures to the buried oxide. The outer dies are masked with polyimide tape to prevent further etching while the central dies finish.

being etched away before another had reached the buried oxide layer in its apertures. Periodicaly rotating the wafer during etching effectively eliminated the azimuthal variation, but the radial variation remained such that central areas etched more slowly. The only recourse was to manually mask completed dies with polyimide tape, moving radially inward. An example of a wafer masked in this way is pictured in Figure 3-22. This method led to successful production of many extractors, however die-to-die uniformity was not achieved. An etch tool without noticeable etch rate non-uniformity would completely solve this issue.

Chapter 4

Evaluation of Microfabricated Components

Assessment of the success of the iEPS package redesign was done through liberal use of the thruster frames and extractor components during developmental tests for the iEPS project. Much of the information gathered about the performance of the package was qualitative and anecdotal as direct testing of certain features (e.g. prevention of liquid current pathways, breakdown voltage) was not deemed necessary given that failures were not observed during operation. General assessments are herein made regarding the performance of the iEPS 2.x against the goals set out in Chapter 2 and data is provided as where available.

4.1 Structural Robustness of Thruster Frames

Over its lifetime, an iEPS thruster frame will not see its most inhospitable environment in space, but rather in the laboratory as it is being cleaned and joined with the other device components. Many structural failures of thruster frames were observed throughout the package's development. Here, the failures and successes of the thruster frame structure are summarized.

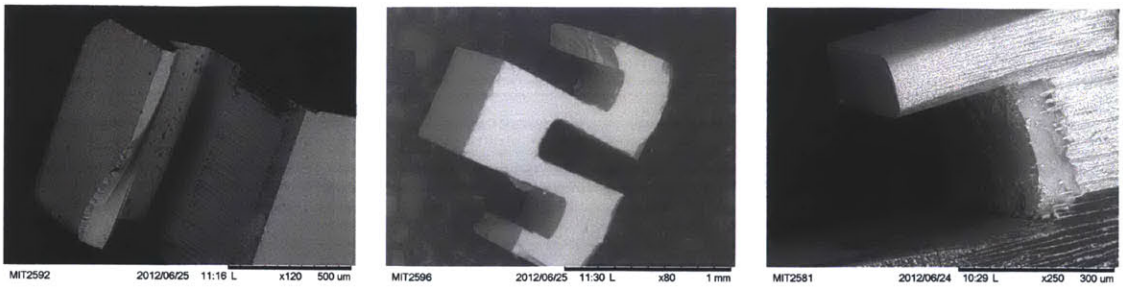


Figure 4-1: These scanning electron micrographs show some remnants of the first production run of iEPS 2.0 thruster frames. The deep liquid-trapping trenches proved to be an Achilles heel leading to the eventual removal of the features in iEPS 2.2 and beyond.

4.1.1 Handling Failures

Because of the highly-manual nature of the iEPS thruster assembly process, the thruster frame must be able to withstand the mechanical forces of general handling and cleaning. Structural failure of the base layer was the major impetus for the design changes made from iEPS 2.0 to 2.1, and some of the changes made for 2.2. Less than 20% of the very first batch of iEPS 2.0 thruster frames yielded usable devices. Many of the frames were damaged just during the dicing and separation process, and those that survived more often than not went on to fail during the emitter chip attachment and patterning process. It became evident that the weakness in the structure was the inclusion of the deep trenches. Figure 4-1 shows a collection of fractured frame spans.

The number of trenches was dramatically reduced between iEPS 2.0 and 2.1 with one half of the frames not having trenches at all. The no-trench design proved to be much more robust to assembly activity. Moreover, testing demonstrated the open design's effectiveness for preventing liquid shorts without the trenches. Therefore, trenches were altogether abandoned in iEPS 2.2. Thruster frames no longer needed to be treated overly delicately and survived repeated chest-height drops onto hard surfaces. Most failures are now due to excessive force or shock causing debonding between layers or fractures near the corners.

4.1.2 Bonding of Corner Posts

As discussed in Chapter 3, the uncommon bonding arrangement of the iEPS 2.x thruster frame led to unpredictable current decay behavior during bonding of the second interface. This, combined with insulating layer surface defects and an inevitable level of particulate contamination, led to failures of the corner post bonds. Many of these failures were observed immediately after die separation, but some did not occur until the package assembly phase when the bonds were stressed.

Yield values were tracked for the four most recent production runs of thruster frames. Of the 176 corner posts manufactured per wafer, the post-dicing yields were 72%, 85%, 85%, and 95%. However, because of the failed posts are distributed among multiple thruster frames, these corner post yields result in 72%, 66%, 61%, and 80% thruster frame yields, respectively.

Improving the bonding quality will be a matter of ensuring insulating layer surface quality and ensuring low particle count during stacking. Addressing the issue of the unpredictable second bond may take more experimentation and experience.

4.1.3 Temperature Range Compatibility

The iEPS thruster frames are made of silicon and glass which have different thermal expansion coefficients. Because they are bonded at high temperature (350 °C), the thruster frame bond planes are under stress at room temperature. Heating will relieve some of the stress, but cooling, especially rapidly, could cause immediate debonding. Anecdotally, the thruster frames are robust to rapid cooling—they have been dipped in liquid nitrogen during the course of experimentation. Boiling liquid nitrogen is at 77.4 K, a temperature 220 K below room temperature and 546 K below the bond zero-stress temperature. Such a test is promising, but what is yet untested is how the frames will handle the repeated thermal cycling experienced in low Earth orbit. Limited thermal cycling occurs during assembly as the thruster is heated for both drying and epoxy curing and then quickly brought back to room temperature.

4.2 Isolation of the High Voltage Electrodes

A main requirement of the thruster package was the electrical isolation of the emitter and extractor potential surfaces. This requirement meant that the structure itself needed to be insulating to potential differences on the order of 10^3 volts and that the liquid current pathways as observed in Courtney's experiments were mitigated [6]. Both objectives were met.

4.2.1 Prevention of Liquid Shorting

At the time of this writing, no iEPS 2.x thruster has failed due to the pooling of liquid on the frame and its subsequent transport and shorting of the high voltage electrodes. This can be considered a success of the transition to an open package architecture with iEPS 2.x. Non-transient shorting that has occurred has been due to liquid bridging the gap between the emitter and extractor or due to liquid leaking from a propellant vessel connection. In the case of the former, over-filling or excessive back pressure were the causes. Liquid leaking from the connection to a propellant vessel was seen during experimentation with assembly methods and has been eliminated as a common issue.

A recent test lasting 60 hours showed evidence of liquid traveling along one of the base layer support arms. Had the test been run longer, it is possible that a liquid short could have occurred. Should longer test runs fail for such a reason, shallow trenches could be etched into the top face of the base layer arms with mild structural consequences.

4.2.2 Structural Insulation

As designed, the thruster frame should be capable of withstanding potential differences across the insulating layer on the order of 10^5 volts. As tested, the thruster frame has withstood sustained DC voltages of up to 5 kV, and sustained square wave voltages in the hundreds and thousands of volts range.

One instance of permanent shorting of the package has been observed. This occurred during a multi-day firing test. Backsputtering of propellant and test chamber materials on the thruster head was evident. A high-impedance ($M\Omega$) was measured between the emitter and extractor. It was not determined if the buildup of a conductive film from backsputtering or structural breakdown had occurred. A best-effort was made at cleaning the thruster head; however, this did not clear the short.

4.3 Alignment of Emitter and Extractor Features

Alignment in the iEPS 2.x design series was designed to be a result of assembly. In theory, perfect manufacturing would allow for exact alignment of the emitter tips and apertures by perfect assembly. In reality, the misalignment of etched frame and mask features was non-zero and varied between production wafers and across the face of any one wafer. Alignment and accuracy of emitter manufacturing has not been characterized but is likely imperfect. When these facts are combined, the result is that the assembled alignment of iEPS 2.x components is still lacking. Though this sounds disappointing, in truth the alignment of apertures to emitter tips is simpler and more immediately accurate than in the original design.

Simply by placing the extractor grid frame or unibody extractor down on the thruster frame as intended, the emitters are aligned to within the diameter of their apertures. It would be possible to extract a beam from the thruster head with this rough alignment, but probably very inefficient due to beam interception. If the extractor component is then pressed into the zero-tolerance corner and fixed in place, the alignment is likely better, but not as good as it can be made by inspection and adjustment under a microscope. The simple alignment scheme described was used for three thruster heads, two with the extractor frame and tungsten grids and one with a unibody silicon grid. Scanning electron microscope (SEM) images were taken through the apertures at the four corners and at the center of the aperture array to see the relative position of the tips and apertures. Three samples were taken from each of the five regions and imported into a CAD software. Circles were fit to the

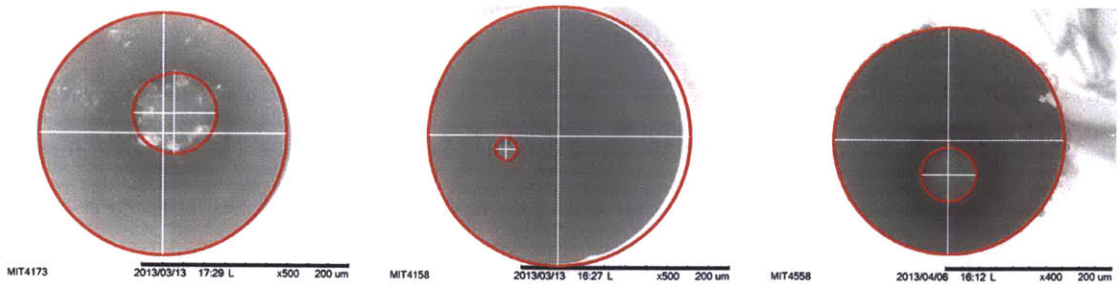


Figure 4-2: SEM images were captured of the emitter tips through the apertures of three thruster heads assembled using the iEPS 2.x alignment scheme. Circles were fit to the apertures and tips in a CAD program to measure the center-to-center misalignment.

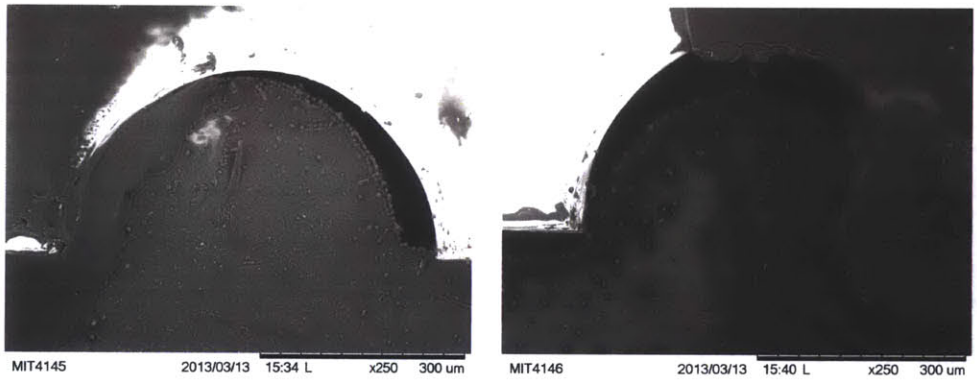


Figure 4-3: SEM images of the interface between a metal extractor grid and the extractor frame are shown. The misalignment is on the order of 100 μm.

apertures and tips as shown in Figure 4-2. Center-to-center distances were recorded and averaged. These results are summarized in Figure 4-5. The average misalignment values are far above of the 10 to 20 μm goal mentioned in Chapter 2.

Contributing to the misalignment of the metal extractor apertures was the alignment interface between the extractor frame and the metal grid. Figure 4-3 shows typical grid key interfaces where the alignment could be off by over 100 μm. This misalignment and the inconsistency of the grid formation process led to the abandonment of the two-component extractor design.

By adjusting the position of the extractor under a microscope, the alignment can be improved. Automated image recognition software implemented by F. Mier-Hicks of the SPL was used to calculate misalignment values by sampling the same five regions mentioned above on four assembled thruster heads. Example image analyses output

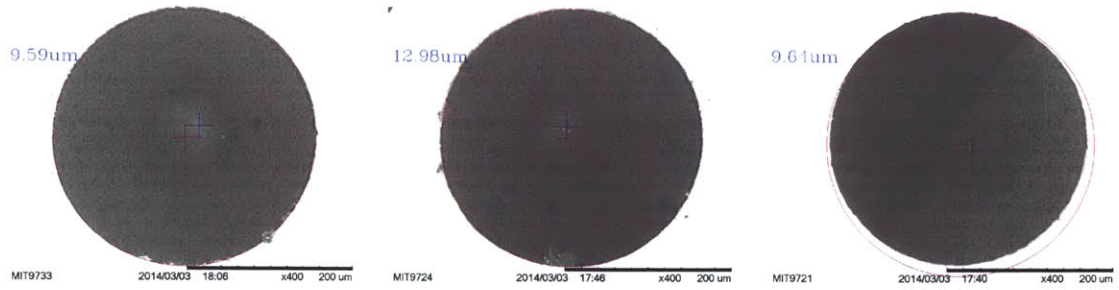


Figure 4-4: SEM images were captured of the emitter tips through the apertures of three thruster heads assembled using the iEPS 2.x alignment scheme followed by adjustment under a microscope. Circles were fit to the apertures and tips using automated image recognition software implemented by F. Mier-Hicks of the SPL.

by this software are shown in Figure 4-4. The misalignment values are summarized in Figure 4-5. Manual alignment under a microscope is significantly better than that seen with the simple alignment scheme. A sub-25-μm misalignment is achieved in all four cases with three meeting the goal of falling below 20μm.

Future designs for assembly-level alignment of iEPS will attempt to preclude the need for any alignment under a microscope in order to achieve average misalignment on the order of those seen with microscope alignment. Tighter tolerances in the extractor-frame interface will reduce the amount of slop available to the grid, and feedback from the iEPS team indicates that ease of assembly will not be affected by such a tightening. Changes to the alignment marks for emitter manufacturing will be made so that they are more easily seen under a poor quality microscope and thus any misalignment in the manufacturing of emitters will be eliminated. And finally, a rotation rather than a translation may be implemented so that the alignment step will only require manipulation along one degree of freedom.

4.4 Performance of Extractor Electrodes

All of the extractor designs fabricated were capable of performing the task of extraction. As mentioned previously, the two-component extractor design was discontinued for reasons involving the manufacturing of the metal electrode. Significant use has been made of the unibody extractor, and a more detailed discussion can be had

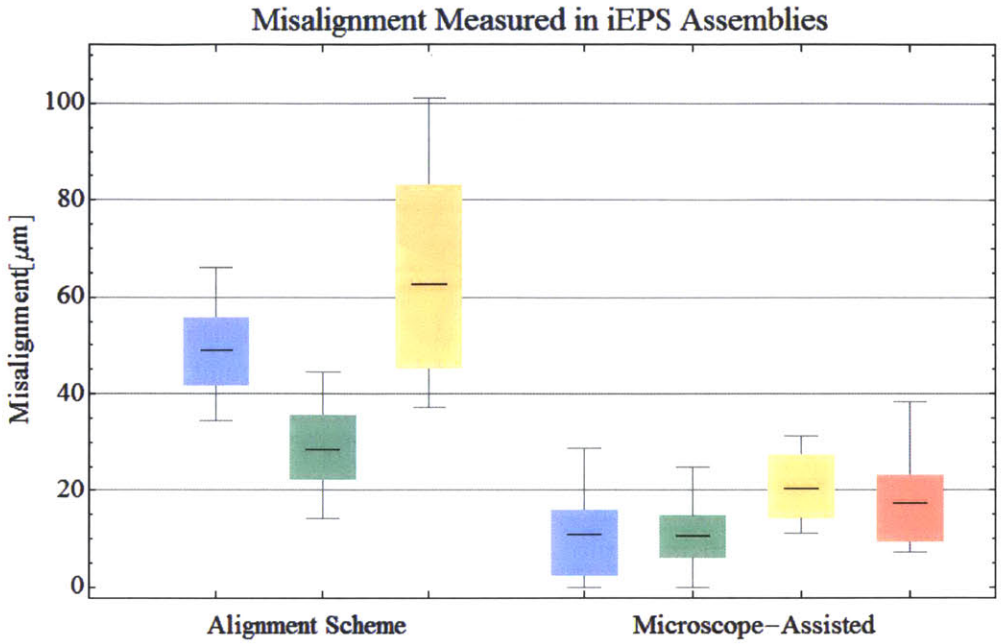


Figure 4-5: Measurements were made of the center-to-center misalignment of seven thruster head assemblies. Three used the basic alignment scheme built into iEPS 2.x and four were adjusted under a microscope. The average is indicated by the dark line. Three samples were taken at each corner of the aperture grid and three at the center.

regarding its performance.

Initially, three variations of the extractor aperture diameter were produced at 250, 275, and 300 micrometers. Testing showed no consistent difference in the performance effected by the three sizes. Therefore, the iEPS 2.2F design utilizes the 300-μm diameter in hopes of reducing the intercepted beam fraction.

The first tests of the unibody extractors clearly demonstrated the aversion of solder to a bare silicon surface. For this reason, various solder pots, holes, and raceways were included in a test batch of extractors. Additionally, a metallic layer was deposited onto the surface. Copper was tried first, but its tendency to oxidize made it less than desirable, so gold was substituted. For iEPS 2.2F, a simple solder pot was chosen, and the gold coating has not been altered.

Chapter 5

Passive Propellant Supply Design and Testing

Unlike the majority of modern electrostatic ion propulsion systems, ionic-liquid electrosprays do not use a gaseous propellant. Zero-vapor-pressure liquid propellants must be transported to the ion extraction region by some process, because they will not expand in the vacuum of space. In traditional liquid propulsion systems, complex pumping and valve arrangements are designed to guide and throttle the propellant and to provide the necessary pressure differential to push the liquid into the high-pressure combustion chamber. A gaseous system would lack pumping machinery, but would introduce a complex set of flow controllers. Designing such systems on the microscale has been an active area of research. Alternatively, based on work in the MIT Space Propulsion Laboratory which led to the use of porous electrospray emitters [12, 6], the propellant supply system for iEPS was designed around the concept of passive transport of ionic liquid by capillarity. A prototype system was developed which served as a precursor to a flight-ready design which will accompany the thruster on its first spaceflight.

5.1 Benefits of a Passive Supply

A passively-fed system offers several main benefits over active fluid management. First and most attractive, the system requires no pressurization; so power, mass, and volume budgets are not spent on actuators, turbomachinery, or pressure vessels. Consequently, the system has no failure modes which present a risk of violent depressurization, so nearby components are not in danger. Moreover, throttling of the thruster is solely controlled by the propellant extraction process within the maximum rate of fluid transport through the capillary matrix—no feedback control loop needs to manage the upstream propellant state.

At present, the main challenges of a passive system, as discussed later, are posed by the design of the capillary network and the management of soluble gases.

5.2 Prototype Design

The goal of the passive propellant system is to provide propellant to the emitter array without the use of moving parts. Beyond this, basic requirements of an electrospray propellant supply are the general containment of liquid, insulation of the conductive propellant from high potential differences, and provision for an interface between the thruster head and satellite bus.

5.2.1 Transport by Porosity Gradient

On the microscale, hydrophilic liquids will wick to the region they are in contact with which minimizes surface energy. Therefore, motion is overall in the direction of decreasing radius of curvature. This is the principle which drives transport of water up a tree trunk or fuel up a lantern wick. Continuous evaporation and combustion lead to the draining of water from the ground and oil from the lamp. Inspired by these natural and artificial systems, the iEPS system is designed to encourage liquid transport to the tips by keeping a general gradient of large to small pores from the supply reservoir to the emitter.

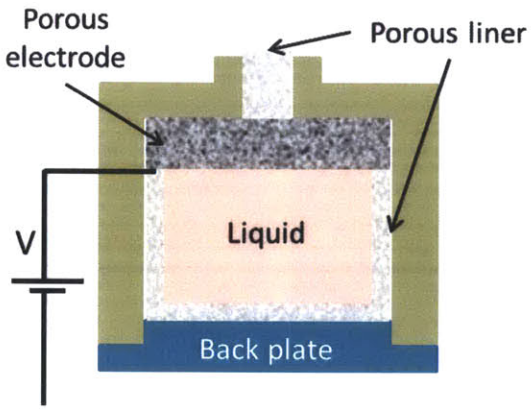


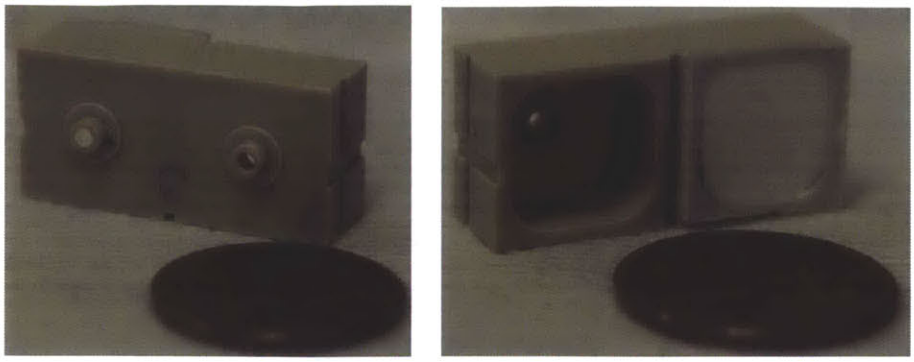
Figure 5-1: A cross-section view of the prototype passively-fed propellant supply system for the iEPS thruster.

5.2.2 Prototype Concept

The initial concept for the propellant vessel prototype is depicted in cross-section in Figure 5-1. In this design, the propellant is stored in an insulated cavity lined with porous material and connected to the thruster through a conductive porous electrode and a wick in the port. An external power supply applies the emission potential to the liquid via the conductive electrode. The electrode's large surface charge capacity aids in avoiding electrochemical breakdown of the propellant as described by Brikner [13]. A back plate acts as a cap to contain the liquid after insertion of the porous materials and filling.

5.2.3 Prototype Production

Based on the aforementioned concept, a prototype tank was designed and fabricated as shown in Figure 5-2. The goals of iEPS thruster testing at the time drove the sizing of the prototype tank cavity as described in Section 5.4. A single-body, two-tank design was conceived to allow for simultaneous firing of opposite polarity thrusters at one time. Polyether ether ketone (PEEK) plastic was chosen for the tank body and back plate due to its low-outgassing in vacuum, its ability to insulate the two propellant chambers from one another, its machinability, and its resilience to radiative environments. Acrylic backplates were also manufactured to provide a window into



(a) (b)

Figure 5-2: These manufactured prototype propellant vessels were made from PEEK plastic for the iEPS 2.0 and 2.1 frame design. An acrylic cap is closing one side (b) to hold in the porous inserts, one of which can be seen. One cent U.S. coins included for scale.

the internal state of the propellant feed. A port was machined to fit the port hole on iEPS 2.0 and 2.1 frames. A later version included pegs on one side for alignment and mounting to the satellite bus.

Liquid transport was provided by porous material inserts. The walls of the cavity were lined with laboratory-grade glass fiber filter paper. A 1-mm thick porous stainless steel chip was chosen for the internal electrode. In the port, more glass filter paper was used to connect the metal chip to the underside of the thruster emitter substrate.

5.3 Testing by Evaporative Analog

To demonstrate a proof of concept, the prototype tank was tested for complete emptying of propellant through the port. In order to facilitate testing, evaporation was used as an analog for electrospraying. Isopropyl alcohol was chosen for the evaporative analog as it did not cloud the acrylic window back plates as would acetone, yet it quickly evaporated at laboratory conditions, unlike water.

5.3.1 Procedure

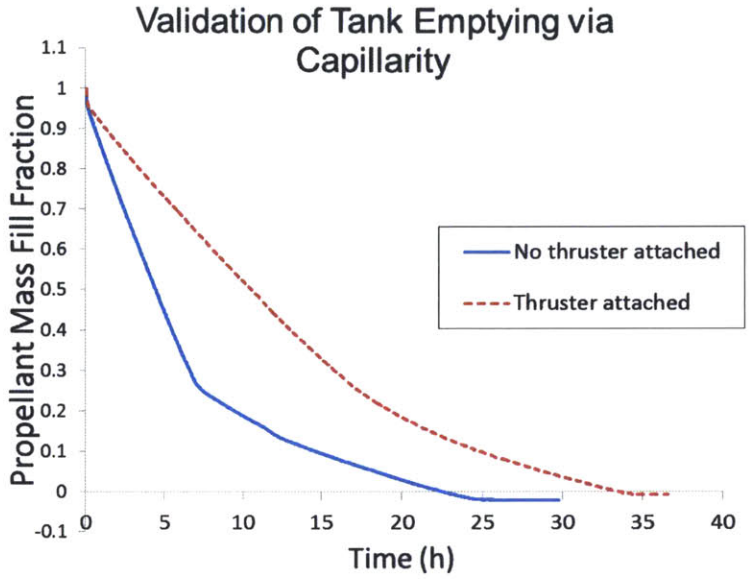
The dry mass of the tank components was measured before and after assembly. The porous components were wet with a dropper while inside the tank, then the assembly was submerged and capped to prevent the trapping of air bubbles. With the port hole blocked, the exterior of the tank was dried. The assembly was then placed on a zeroed digital mass balance, port facing up. The balance had a baffle to prevent extreme measurement fluctuations due to air movement. The mass was collected ten times per second by a computer, averaged over one minute, and stored to a data file along with the time elapsed. The evaporation test was performed both with and without an accompanying iEPS thruster initially filled with isopropyl alcohol covering the port. The observed evaporation rates were in the tens of milligrams per hour. For a thruster firing at 50 μN with 2000 s I_{sp}, the expected mass flow rate is 11.5 mg/h, so the mass flow rate is in the right regime.

5.3.2 Analysis

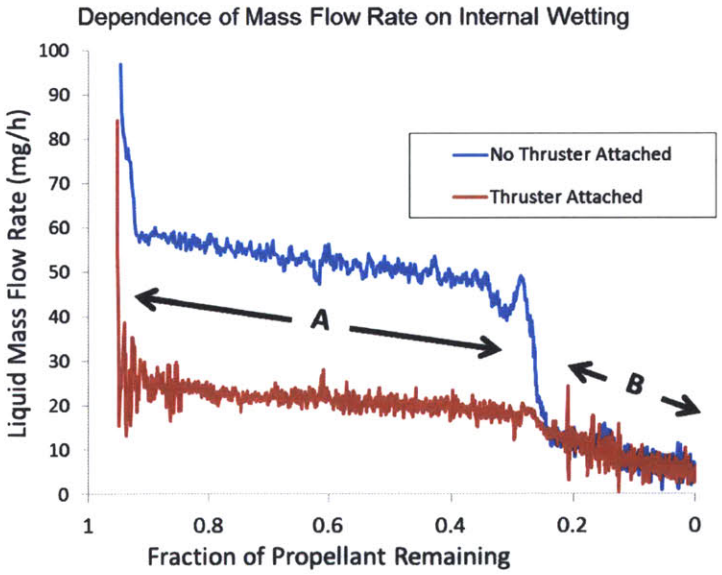
Analysis of the mass data showed an apparent relationship between the mass flow rate and the fill fraction of the system. Plotting the smoothed (6-minute moving average) mass flow rate versus the fill fraction, there appear to be two regions in Figure 5-3. Based on the fill fraction, the mass remaining at the transition corresponds to the liquid mass which is held by the glass fiber and porous metal. Thus the transition seems to occur due to an emptying of the main cavity. After the transition, the remaining mass flows out at the same rate regardless of the presence of the emitter chip.

Ample Liquid Supply Regime

The first region corresponds to the presence of free-flowing liquid in the cavity. A steady decrease is seen in the mass flow rate. This can be attributed to the increasing hydraulic impedance as the transport distance between the free liquid and the air increases as shown in Figure 5-4. In this region, the hydraulic impedance is no longer



(a) The propellant fill fraction during evaporative testing as a function of time. Note that two main linear regions appear in both traces. One test was performed with an iEPS thruster covering the port and one without.



(b) The mass flow rate during evaporative testing as a function of propellant fill fraction. The two main regions of evaporation rate are highlighted. The second region does not seem to be flow-restricted by the thruster head.

Figure 5-3

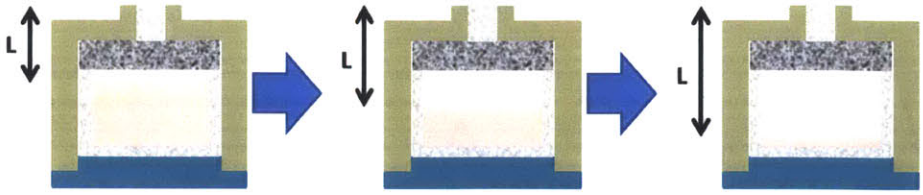


Figure 5-4: As the liquid is drained in the presence of gravity, the minimum transport distance between the bulk and the air increases.

dominated by the presence or absence of the thruster head. This would suggest that the internal components are determining the transport rate.

Drying Regime

During the second regime in which the porous material is drying out, the evaporation rate is limited by how quickly the liquid can redistribute inside the pores. Examining the second region more closely, the evaporation rate seems to remain fairly constant when plotted against the inverse root of time. A rate change seems to manifest in this range and the two setups seem to converge on one rate. This final region just before complete exhaustion may be controlled by diffusion of the remaining alcohol vapors through the port hole to equilibrate the internal and external alcohol concentrations. Evaporation is no longer involved, so if the diffusion rate is low enough, the exterior of the tank can be seen as as having a constant alcohol concentration; and thus, the presence of the thruster becomes wholly unimportant.

5.3.3 Test Limitations

It is clear that, though the evaporative experiments demonstrate validity of the porous transport concept, there are limitations which leave questions unanswered.

First is the use of an evaporative liquid as the analog propellant. The ionic liquids used in the thrusters have a zero vapor pressure, so it is possible that the two-phase mixture in the tank has some affect on the transport rates, especially near the end when the free-flowing liquid has been exhausted. Moreover, air must be transported into the tank to replace the evaporated liquid volume, so this will most certainly

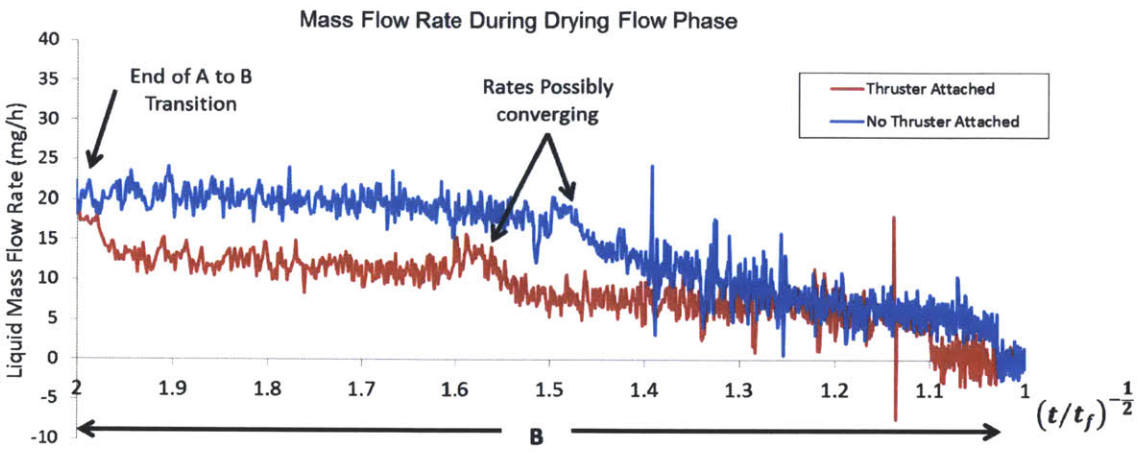


Figure 5-5: With very little liquid left, the mass flow rate appears to have a near-constant value when plotted against the inverse square root of the time.

change the mass flow rate. In the case of a thruster, a vacuum can form when propellant depletes as there is no significant ambient pressure to oppose it.

Because of the nature of the laboratory, a microgravity environment cannot be maintained over the course of the evaporation tests. It it therefore unknown what effects microgravity will have on the liquid transport. Fortunately, due to the relative magnitudes of the gravitational force and surface tension force at a micro scale, effects are likely negligible. The only conceivable failure mode would be the detachment and isolation of a propellant blob in the center of a large reservoir cavity. In such a scenario, the small forces seen by the satellite exterior would likely reunite the propellant with a porous surface in due time.

5.4 Sizing Considerations for Mission Design

The size of the vessel is driven by mission requirements and vessel requirements. For a given mission, there are a total firing time and a mass and volume envelope which must be considered. From a propellant supply standpoint, the structure must be manufacturable, rigid, and fillable. These considerations all go into shaping the propellant tank design for a specific mission.

5.4.1 Internal Volume Estimation

The internal volume is found from the thruster performance, propellant density, and porosity of any internal components.

Assuming the mission specifies the required thrust, F, specific impulse, I_{sp}, and total burn time, t_b, only the propellant density, ρ_p, is then necessary to determine the propellant volume requirement for the thruster:

$$V_p = \frac{t_b F}{\rho_p g I_{sp}},$$

where g is the acceleration due to gravity at Earth's surface.

Knowing this value, the internal volume of the tank then needs to accommodate the free liquid volume and the solid volume of saturated porous inserts. If the porosity and volume of a given component are p_i and V_i respectively, then the internal volume requirement can be found. It becomes simply the volume of the propellant plus the volume of the n porous inserts that the propellant isn't occupying.

$$V_f = V_p + \sum_{i=1}^{n} (1 - p_i) V_i$$

In practice, the values of V_i will depend on the final dimensions of the tank, and thus, on V_f. Iteration is then used to converge on a solution.

When the porous inserts are not rigid and swell when wet due to internal forces, the expanded-state porosity must be used to solve for the internal volume. The porous insert is then sized based on a measured expansion factor.

5.4.2 Vessel Structure and Arrangement Trades

Rigidity, total volume, electrical isolation, and lengthening of torque arms all push the propellant vessel form factor design into a different space. For rigidity and machinability, the preference is to have large, thick features which go against the leanness of aerospace design. Thick walls are good for electrical isolation, but so is significant spacing between the high voltage cavities and thruster heads. For long, effective

torque arms, the thrusters should be in disparate, tight groups. Conversely, volume considerations drive the thrusters together and thin out the walls as much as possible. Finding a happy medium within the envelope these create can be a challenge.

Experience with the PEEK plastic has dictated that a 1-mm wall thickness works well for rigidity and machinability, but it can be thinned should there be a need for a smaller form factor. More rigid and machinable insulators which do not outgas significantly in vacuum are difficult to come by, but would be an excellent option for a vessel material.

Designing the vessel to fit in a given geometry often leads to an attempt to minimize one dimension. This is done by adjusting the others within the remaining design space to accommodate the thruster head, vessel walls, internal components, and propellant volume. While this is reasonable within a certain region of the geometry, the effect of dimensional manipulations grows nonlinear as one dimension approaches the order of the minimum wall or porous insert thickness. At a certain point, the cross section of the vessel along one plane is mostly taken up by solid or porous material and the dimensions in the other planes explode in order to meet the propellant volume requirements as a larger internal volume fraction is taken up by porous material. Such a high-aspect-ratio design is horribly volume inefficient and poses challenges from a filling, manufacturing, and liquid transport standpoint. Additionally, certain dimensions can only be decreased so far before exposing the thruster frame to structural damage. Awareness of the propellant volume and dimensional requirements of the propellant supply concept will prevent impossible design scenarios.

Tight packing of thrusters onto a unibody, multi-cavity vessel can be an excellent way of saving on overall volume, however this risks device failure should a leak or liquid accumulation cause an inter-thruster short. Additionally, if the thruster is meant to act as a reaction control system (RCS), the thrusters should be placed at distant, opposing locations in relation to the spacecraft center of mass. Torque performance losses and risk must be accepted in a trade for a tight volume arrangement. Such issues become less constricting when designing for unidirectional thrusting.

5.5 Propellant Management Challenges

Two aspects of working with ionic liquid propellants and porous materials make atmospheric propellant management difficult. First, ionic liquids are by nature excellent solvents and often readily absorb atmospheric gases. Second, imbibition of liquids into porous solids in atmosphere allows for the trapping of gaseous pockets in the interior of the porous matrix. Both phenomena present challenges for the assembly and operation of a full iEPS configuration.

Dissolved gases (e.g. water vapor, carbon dioxide, argon) readily precipitate from solution as an ionic liquid is exposed to vacuum. Such precipitation can be prevented with sufficient capillary pressure so that the gases then escape by diffusion at the liquid surface. In the case of a passively fed propellant system, the pores in the main reservoir are not sufficiently small so gas (and pressure) buildup will occur if not mitigated. The prototype design outlined above does not account for gas precipitation in the main chamber.

Gas pockets trapped in the porous structure by imperfect imbibition are eventually transported to the exterior as the propellant drains. Once at the surface, capillary pressure is lost and the gas violently expands. The sudden introduction of an atmosphere between the high voltage electrodes is nearly guaranteed to generate an electrical breakdown, shorting the electronics, thermally damaging the electrodes, and decomposing some of the remaining propellant. The violent expansion can also deposit propellant on surfaces, potentially causing a permanent short.

The aforementioned challenges necessitate that the propellant vessel be filled with thoroughly outgassed liquid at vacuum so that no gas can be trapped in the porous pieces. Barring the use of a large vacuum chamber and a space suit, the small propellant vessels must be filled in a high-vacuum chamber. Attempts were made at very-low-pressure-fed and gravity-fed filling inside the chamber; however, contamination remained an issue in the first case and outgassing in the transfer lines stymied the latter. While concentrating on the gas buildup issue, changes to the tank design were made which facilitated simpler filling methods, but these were not part of initial

prototyping.

5.6 Results of Thruster-Vessel Integration

Propellant-vessel-integrated testing of the iEPS thruster head led to design changes for the thruster frames, extractors, and propellant vessel and to the demonstration of added testing capability.

Experience with attaching the thruster frame to the propellant supply interface led to the downselection of the base layer of iEPS 2.2F and the inclusion of solder wells in the extractor design. Propellant vessels have taken the firing time of an iEPS thruster head from a few hours with constant flow rate decay predicted by Legge to recent tests with firing times on the order of 100 hours, thus enabling exploration of the next set of lifetime-limiting phenomena for electrospray arrays [5].

With the experience derived from trial implementation of the propellant supply prototype, a first flight design for the iEPS propellant supply has been developed which implements features and propellant management techniques for mitigation of gas precipitation and trapping phenomena.

Chapter 6

Summary and Future Work

The Space Propulsion laboratory has been developing the Ion Electrospray Propulsion System over several years in pursuit of a viable, flight-worthy, scaled electrospray thruster. The initial design of the thruster head was successful, but plagued by issues surrounding the design of the device package. In addition, dedicated designs for a power processing unit and propellant supply vessel were still needed. This work sought to redesign the iEPS package and to begin design and testing on a passive propellant supply system.

In the previous chapters, an updated design was presented for the iEPS package. The design was conceived to directly address the flaws of the first design while including new features. Manufacturing processes were developed and tweaked to be reliable. The resulting components underwent testing and redesign, culminating in the downselection of a uniform design for first flight, iEPS 2.2F. Qualitative and quantitative assessments of the package performance were discussed in relation to root causes and possible steps toward an improved design.

Design considerations for and test results from the implementation of an experimental passive propellant vessel were shared. Proof of concept was demonstrated within limitations. The results of early propellant supply system work has gone on the inform a much improved design which addresses the challenges faced by the prototype.

6.1 Assessment of Success

In its goal of improving upon the iEPS package, this work was, in general, successful. The major testament to this success has been the dramatic increase in the amount of test data being collected in the laboratory from iEPS 2.x thruster modules.

Isolation of the two high voltage electrodes has been complete in terms of the package structure. Liquid no longer pools and bridges the separation region as observed with the previous design. This development has been a boon to the iEPS project as it has allowed for long-term firing of the electrospray arrays. Exploration into the behavior of the full system over days of firing has begun. At the time of this writing, thruster lifetime records are being broken on a bi-weekly basis.

Changes to the thruster frame-extractor interface have enabled disassembly and rapid thruster turnover. Thruster frame-emitter pairs can now be inspected after firing, reused after cleaning, and paired with different extractor designs. While still not as simple as desired, alignment of the extractor apertures to the emitter tips is much less tedious than before. Precise alignment is still lamentably best achieved by manual adjustment under a microscope.

Outside of the unpredictability of the thruster frame wafer bonding, the manufacturing process for the iEPS 2.x design is stable and repeatable. The major challenges to success were addressed within the process design for each layer. As seen with the iteration through the designs of the base layer, the manufacturing process is flexible enough to accommodate design changes, and any added complexity for the sake of package improvement can be managed.

6.2 Room for Improvement

Though overall a success, the iEPS 2.x redesign has room for improvement in the areas of structural integrity, alignment, and extended capability.

Improvements to the package design will be a part of ongoing efforts in the iEPS program. The ability of the thruster frame corner posts to withstand the abuse of

repeated assembly and cleaning will necessitate strong, reliable bonding. Although bonding quality is improving with experience, methods for increasing the yield will be sought.

As previously mentioned, the iEPS 2.x automatic alignment scheme could not achieve the goal misalignment window. This failure is likely due to a compounding of manufacturing inaccuracies and overly generous interface tolerances. With the next version of iEPS, changes will be made to reduce the amount of slop between the extractor recesses and the corner posts. Additionally, clearer alignment marks will be provided for the emitter tip machining process. Finally, design concepts for alignment schemes will be drafted in the search for an easily-assembled, simple, repeatable, and mechanically-restrictive design.

Regarding added capabilities, with the abandonment of the extractor grid frame component, the ability to mount a downstream grid to the iEPS 2.x package was lost. Concepts were presented in Chapter 2 and may be pursued in order to add multi-modal performance to the device. Analyses will need to be made to determine the optimal design envelope.

The rapid improvements seen in the technology readiness of iEPS over the past few years have been exciting, to say the least. A successful first flight seems to be on the horizon, just beyond which lies the dawning of the era of electrospray propulsion.

Appendix A

Detailed Manufacturing Processes

The following pages contain the details of the manufacturing processes used to produce the thruster frames, extractor grid frame, and unibody silicon extractor. All of the equipment utilized resides in the MIT Microsystems Technology Laboratory and was accessed between January 2012 and May 2014.

Time estimates are given for a batch of 25 wafers or less, except when labeled "ea." meaning the process time scales with the number of wafers.

Table A.1: Base Layer Detailed Manufacturing Process Flow

Material: ⌀150 mm × 1 mm DSP ⟨100⟩ silicon wafer				
Step	***Process***	***Machine***	***Time (min)***	***Specifics***
0.0	**RCA Clean**	RCA wet station		
.1	SC1		10	10 min in 5:1:1 DIH_2O:27% NH_4OH:30% H_2O_2 at 75 °C ± 5 °
.2	Rinse		10	5 dump rinse cycles
.3	Oxide removal		1	1 min 50:1 DIH_2O:HF
.4	Rinse		10	5 dump rinse cycles
.5	SC2		10	10 min 6:1:1 DIH_2O:37%HCl:30% H_2O_2 at 75 °C ± 5 °
.6	Rinse		10	5 dump rinse cycles
.7	Spin, Rinse, & Dry		10	
1.0	**Wet Thermal Oxidation**	THERMCO furnace	240	Grow 500 nm
2.0	**Nested Mask Patterning**			
.1	HMDS		22	
.2	Thin resist coating		2 ea.	Top side, 1 μm OCG 825-20 at 2 kRPM
.3	Soft bake resist		30	30 min at 95 °C

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.4	Pattern exposure	Electronic Visions 620	4 ea.	Masks: Top: pedestal, 2 s exposure
.5	Develop		2 ea.	1:15 m:ss in OCG 934
.6	Spin Rinse & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 120 °C
3.0	**Oxide Patterning**			
.1	Buffered oxide etch		10	10 min
.2	Rinse			5 dump rinse cycles
.3	Strip resist		10	Piranha
.4	Rinse		10	
.5	Spin, Rinse, & Dry		10	
4.0	**Etch Masking**			
.1	HMDS		22	

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.2	Thick resist coating		10 ea.	Both sides, double coating, 10 μm each, AZ P 4620 at 1.2 kRPM, 10 min bake at 95 ° between sides
.3	Soft bake resist		30	30 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	10 ea.	Masks: Top: chip face, Bot: base bottom, expose 4×(15 s on, 15s off)
.5	Develop		5 ea,	4:00 m:ss agitating, flipping
.6	Spin, Rinse, & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 95 °C
5.0	**Oxide Patterning**			
.1	Buffered oxide etch		10	Clear exposed oxide
.2	Rinse		10	5 dump rinse cycles
.3	Spin, Rinse, & Dry		10	10 min
6.0	**Deep Feature Etching**			

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.1	Etch alignment marks	Surface Technology Systems	16 ea.	20s (0.3 μm) both sides
.2	Protect alignment marks & edges		5 ea.	Cover alignment marks and top face near edge with polyimide adhesive tape
.3	Bottom side etching	Surface Technology Systems	720 ea.	iEPs 2.0, 2.1: 750 μm; iEPS 2.2: 900 μm
.4	Remove tape		5 ea.	Peel off polyimide tape
.5	Mount to handle wafer		5 ea.	Mount wafer to handle wafer using photoresist, etched side down, bake 30 min 95 °C
.6	Protect alignment marks & edges		5 ea.	Cover alignment marks and top face near edge with polyimide adhesive tape
.7	Top side etching	Surface Technology Systems	60 ea.	Etch through (or 750 μm for iEPS 2.0, 2.1)
.8	Remove tape		5 ea.	Peel off polyimide tape
.9	Dismount from handle wafer		720	Soak in acetone to dissolve photoresist
.10	Strip resist		10	Piranha
.11	Mount to handle wafer		5 ea.	Mount wafer to handle wafer using photoresist, top side out, bake 30 min 95 °C
.12	Protect alignment marks & edges		5 ea.	Cover alignment marks and top face near edge with polyimide adhesive tape

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.13	Top side etching	Surface Technology Systems	10 ea.	Etch pedestal height (25 to 30 μm)
.14	Remove tape		5 ea.	Peel off polyimide tape
.15	Dismount from handle wafer		720	Soak in acetone to dissolve photoresist

Table A.2: Insulating Layer Detailed Manufacturing Process Flow

Material: ⌀150 mm × 0.5 mm Corning Pyrex 7740 wafer				
Step	***Process***	***Machine***	***Time (min)***	***Specifics***
0.0	**Particle removal**			
.1	Piranha cleaning		10	10 min piranha
.2	Rinse		10	5 dump rinse cycles
1.0	**Alignment Mark Patterning**			
.1	HMDS		22	
.2	Thin resist coating		4 ea.	Both sides, 1 μm OCG 825-20 at 2 kRPM, 8 min bake between sides
.3	Soft bake resist		30	30 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	4 ea.	Mask: Top: insulating layer, 2 s exposure
.5	Develop		2 ea.	1:15 m:ss in OCG 934
.6	Spin, Rinse, & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 120 °C

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
2.0	**Alignment Mark Etching**			
.1	Buffered oxide etch		19	10 min at 25 nm/min Etch 250 nm
.2	Rinse		10	5 dump rinse cycles
.3	Strip resist		10	Piranha
.4	Rinse		10	5 dump rinse cycles
.5	Spin, Rinse, & Dry		10	
3.0	**Polysilicon Deposition**		240	520 °C, 200 mT SiH_4, Deposit 250 nm
4.0	**Etch Mask Patterning**			
.1	HMDS		22	
.2	Thin resist coating		4 ea.	Both sides, 1 μm OCG 825-20 at 2 kRPM, 8 min bake between sides
.3	Soft bake resist		30	30 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	4 ea.	Mask: Top & Bot: insulating layer
.5	Develop		2 ea.	1:15 m:ss in OCG 934
.6	Spin, Rinse, & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.8	Coat aligns& edge		4 ea.	Paint alignment marks and wafer edge with photoresist, bake 10 min
.9	Hard bake resist		30	0 min at 120 °C
5.0	**Polysilicon Etching**			Expose glass for wet etching
.1	DRIE top		10 ea.	30 s Etch to glass
.2	DRIE bottom		10 ea.	30 s Etch to glass
6.0	**Glass Etching**			
.1	Hydrofluoric acid wet etch		50	50 min at 5 μm/min to etch through
.2	Rinse		10	5 dump rinse cycles
.3	Strip resist		10	Piranha
.4	Rinse		10	5 dump rinse cycles
.5	Strip polysilicon		2	1:20:20 Hydrofluoric, nitric, acetic acid mix
.6	Rinse		10	5 dump rinse cycles
.7	Spin, Rinse, & Dry		10	

Table A.3: Alignment Layer Detailed Manufacturing Process Flow

Material: ⌀150 mm × 0.5 mm DSP ⟨100⟩ silicon wafer				
Step	***Process***	***Machine***	***Time (min)***	***Specifics***
0.0	**RCA Clean**	RCA wet station		
.1	SC1		10	10 min in 5:1:1 DIH_2O:27% NH_4OH:30% H_2O_2 at 75 °C ± 5 °
.2	Rinse		10	5 dump rinse cycles
.3	Oxide removal		1	1 min 50:1 DIH_2O:HF
.4	Rinse		10	5 dump rinse cycles
.5	SC2		10	10 min 6:1:1 DIH_2O:37%HCl:30% H_2O_2 at 75 °C ± 5 °
.6	Rinse		10	5 dump rinse cycles
.7	Spin, Rinse, & Dry		10	
1.0	**Wet Thermal Oxidation**	THERMCO furnace	240	Grow 500 nm
2.0	**Nested Mask Patterning**			
.1	HMDS		22	
.2	Thin resist coating		4 ea.	Both sides, 1 μm OCG 825-20 at 2 kRPM, 8 min bake between sides

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.3	Soft bake resist		30	30 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	4 ea.	Masks: Top: alignment crosses, Bot: bonding pad, 2 s exposure
.5	Develop		2 ea.	1:15 m:ss in OCG 934
.6	Spin Rinse & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 120 °C
3.0	**Oxide Patterning**			
.1	Buffered oxide etch		19	10 min
.2	Rinse		10	5 dump rinse cycles
.3	Strip resist		10	Piranha
.4	Rinse		10	5 dump rinse cycles
.5	Spin, Rinse, & Dry		10	
4.0	**Alignment Mark Etching**		8 ea.	Etch 0.3 μm deep on top side
5.0	**Etch Masking**			

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.1	HMDS		22	
.2	Thick resist coating		5 ea.	Both sides, single coating, 10 μm each, AZ P 4620 at 1.2 kRPM, 10 min bake at 95 ° between sides
.3	Soft bake resist		60	60 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	10 ea.	Masks: Top: post shapes, Bot: bonding pad, expose 2×(10 s on, 15s off)
.5	Develop		5 ea.	2:30 m:ss agitating, flipping
.6	Spin, Rinse, & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 95 °C
6.0	**Oxide Patterning**			
.1	Buffered oxide etch		10	Clear exposed oxide
.2	Rinse		10	5 dump rinse cycles
.3	Spin, Rinse, & Dry		10	10 min

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
7.0	**Deep Feature Etching**			
.1	Etch alignment marks	Surface Technology Systems	16 ea.	20s (0.3 μm) both sides
.2	Protect alignment marks & edges		5 ea.	Cover alignment marks and top face near edge with polyimide adhesive tape
.3	Top side etching	Surface Technology Systems	70 ea.	150+ μm
.4	Remove tape		5 ea.	Peel off polyimide tape
.5	Mount to handle wafer		5 ea.	Mount wafer to handle wafer using photoresist, etched side down, bake 30 min 95 °C
.6	Protect alignment marks & edges		5 ea.	Cover alignment marks and top face near edge with polyimide adhesive tape
.7	Bottom side etching	Surface Technology Systems	280 ea.	Etch through
.8	Remove tape		5 ea.	Peel off polyimide tape
.9	Dismount from handle wafer		720	Soak in acetone to dissolve photoresist
.10	Strip resist		10	Piranha
.11	Spin, Rinse, & Dry		10	

Table A.4: Thruster Frame Stack Detailed Manufacturing Process Flow

Material: Base layer, insulating layer, alignment layer wafers				
Step	***Process***	***Machine***	***Time (min)***	***Specifics***
0.0	**Wafer Surface Cleaning**			
.1	Remove particles		10	10 min Piranha of all frame layers
.2	Rinse		10	5 dump rinse cycles
.3	Expose silicon surface		10	10 min Buffered oxide etch on base and alignment layers
.4	Rinse		10	5 dump rinse cycles
.5	Spin, Rinse, & Dry		10	10 min
1.0	**Wafer Alignment**	Electronic Visions 620		
.1	Align wafers		15 ea.	Insulating with either base or alignment layers
.2	Clamp aligned wafers			
.3	Inspect alignment		3 ea.	Look through insulating layer
2.0	**Anodic Bonding**	Electronic Visions 501		
.1	Load wafers in bonder			
.2	Heating		14 ea.	Raise to 350 °C

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.3	Compress stack			1000 N (lower may be safer)
.4	Apply voltage		3 ea.	Glass at negative 800 V
.5	Remove voltage			Stop at 15 mA
.6	Cooling		90 ea.	Cool below 50 °C
.7	Inspect bond		5 ea.	Bonded areas have no air gap and are darkened
3.0	**Wafer-stack Alignment**			
.1	Align wafers		15 ea.	Bonded pair and remaining silicon layer
.2	Clamp aligned wafers			
.3	Inspect alignment		3 ea.	Look through outer layer through holes
4.0	**Anodic Bonding**	Electronic Visions 501		
.1	Load wafers in bonder			
.2	Heating		14 ea.	Raise to 350 °C
.3	Compress stack			1000 N (lower may be safer)
.4	Apply voltage		10+ ea.	Pair at negative 800 V
.5	Remove voltage			Stop when current decays below 0.1 mA (or reasonable value)

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.6	Repeat bond		15 ea.	Try to ensure fully bonded
.7	Cooling		90 ea.	Cool below 50 °C
5.0	**Dicing**	Disco DAD-2H/6T		
.1	Set up tool		10 ea.	Use glass cutting blade. Calibrate blade height. 13 mm wide steps across dies + 240 μm blade width, 3mm between dies. Three or four cuts through thickness
.2	Mount stack		10 ea.	Tape wafer stack on both sides with diesaw tape, mount and align on stage, calibrate test cut
.3	Cut first direction		90 ea.	13 mm die width, 3 mm separation
.4	Rotate stage			90°
.5	Cut second direction		110 ea.	13 mm die width, 3 mm separation. look for releasing dies and collect
.6	Unmount stack			
6.0	**Separate Dies**			

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.1	Release dies		720	Soak in acetone or UV expose to soften adhesive
.2	Inspect frames		30 ea.	Look for failed bonding, etch defects

Table A.5: Extractor Frame Detailed Manufacturing Process Flow

Material: ⌀150 mm × 0.5 mm DSP ⟨100⟩ silicon wafer				
Step	***Process***	***Machine***	***Time (min)***	***Specifics***
0.0	**RCA Clean**	RCA wet station		
.1	SC1		10	10 min in 5:1:1 DIH_2O:27% NH_4OH:30% H_2O_2 at 75 °C ± 5 °
.2	Rinse		10	5 dump rinse cycles
.3	Oxide removal		1	1 min 50:1 DIH_2O:HF
.4	Rinse		10	5 dump rinse cycles
.5	SC2		10	10 min 6:1:1 DIH_2O:37%HCl:30% H_2O_2 at 75 °C ± 5 °
.6	Rinse		10	5 dump rinse cycles
.7	Spin, Rinse, & Dry		10	
1.0	**Wet Thermal Oxidation**	THERMCO furnace	240	Grow 500 nm
2.0	**Nested Mask Patterning**			
.1	HMDS		22	
.2	Thin resist coating		4 ea.	Both sides, 1 μm OCG 825-20 at 2 kRPM, 8 min bake between sides

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.3	Soft bake resist		30	30 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	4 ea.	Masks: Top: extractor slot
.5	Develop		2 ea.	1:15 m:ss in OCG 934
.6	Spin Rinse & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 120 °C
3.0	**Oxide Patterning**			
.1	Buffered oxide etch		10	10 min
.2	Rinse		10	5 dump rinse cycles
.3	Strip resist		10	Piranha
.4	Rinse		10	5 dump rinse cycles
.5	Spin, Rinse, & Dry		10	
4.0	**Etch Masking**			
.1	HMDS		22	

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.2	Thick resist coating		5 ea.	Both sides, single coating, 10 μm each, AZ P 4620 at 1.2 kRPM, 10 min bake at 95 ° between sides
.3	Soft bake resist		60	60 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	10 ea.	Masks: Top: accelerator slot, Bot: corner and center recesses
.5	Develop		5 ea.	2:30 m:ss agitating, flipping
.6	Spin, Rinse, & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 95 °C
5.0	**Deep Feature Etching**			
.1	Top side etching	Surface Technology Systems	70 ea.	Over-etch past grid separation depth
.2	Buffered oxide etch		10	Clear extractor mask and bottom oxide
.3	Rinse		10	5 dump rinse cycles
.4	Spin, Rinse, & Dry		10	
.5	Top side etching	Surface Technology Systems	110	Etch to leave recess depth thickness

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.6	Mount to handle wafer		5 ea.	Mount wafer to handle wafer using photoresist, etched side down, bake 30 min 95 °C
.7	Bottom side etching	Surface Technology Systems	70	Etch to recess depth (through)
.8	Dismount from handle wafer		720	Soak in acetone to dissolve photoresist
.9	Strip resist		10	Piranha
.10	Rinse		10	5 dump rinse cycles
.11	Spin, Rinse, & Dry		10	
6.0	**Dicing**	Disco DAD-2H/6T		
.1	Set up tool		10 ea.	Use silicon cutting blade. Calibrate blade height. 13 mm wide steps across dies + 240 μm blade width, 3mm between dies. Two or three cuts through thickness
.2	Mount wafer		10 ea.	Tape wafer on one side with diesaw tape, mount and align on stage, calibrate test cut
.3	Cut first direction		45 ea.	13 mm die width, 3 mm separation
.4	Rotate stage			90°

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.5	Cut second direction		45 ea.	13 mm die width, 3 mm separation. look for releasing dies and collect
.6	Unmount wafer			
7.0	**Separate Dies**			
.1	Release dies		720	Soak in acetone or UV expose to soften adhesive
.2	Inspect extractors frames		30 ea.	Look for broken grid frames

Table A.6: Unibody Extractor Detailed Manufacturing Process Flow

Material: ⌀150 mm × 150:0.5:500-μm Device:BOx:Handle ⟨100⟩ SOI wafer				
Step	***Process***	***Machine***	***Time (min)***	***Specifics***
0.0	**Particle removal**			
.1	Piranha cleaning		10	10 min piranha
.2	Rinse		10	5 dump rinse cycles
1.0	**Thick Oxide Deposition**	Centura 5300 DCVD	8 ea.	1.25 μm PECVD on handle
2.0	**Nested Mask Patterning**			
.1	HMDS		22	
.2	Thin resist coating		4 ea.	Handle side, 1 μm OCG 825-20 at 2 kRPM
.3	Soft bake resist		30	30 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	4 ea.	Mask: Handle: apertures
.5	Develop		2 ea.	1:15 m:ss in OCG 934
.6	Spin Rinse & Dry		10	
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.8	Hard bake resist		30	30 min at 120 °C
3.0	**Oxide Patterning**			
.1	Buffered oxide etch		12	12 min to clear exposed PECVD oxide
.2	Rinse		10	5 dump rinse cycles
.3	Strip resist		10	Piranha
.4	Rinse		10	5 dump rinse cycles
.5	Spin, Rinse, & Dry		10	
4.0	**Etch Masking**			
.1	HMDS		22	
.2	Thick resist coating		5 ea.	Both sides, single coating, 10 μm each, AZ P 4620 at 1.2 kRPM, 10 min bake at 95 ° between sides
.3	Soft bake resist		60	60 min at 95 °C
.4	Pattern exposure	Electronic Visions 620	10 ea.	Masks: Top: aperture well, Bot: corner and center recesses
.5	Develop		5 ea.	2:30 m:ss agitating, flipping
.6	Spin, Rinse, & Dry		10	

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.7	Inspect pattern		1 ea.	Check developed pattern under microscope and fluoroscope for resolution and development quality
.8	Hard bake resist		30	30 min at 95 °C
5.0	**Deep Feature Etching**			
.1	Top side etching	Surface Technology Systems	60 ea.	Over-etch desired grid thickness
.2	Buffered oxide etch		12	12 min to clear aperture mask
.3	Rinse		10	5 dump rinse cycles
.4	Spin, Rinse, & Dry		10	
.5	Top side etching	Surface Technology Systems	450 ea.	Etch down to buried oxide, mask completed dies while others finish if necessary
.6	Mount to handle wafer		5 ea.	Mount wafer to handle wafer using photoresist, etched side down, bake 30 min 95 °C
.7	Bottom side etching	Surface Technology Systems	125	Etch to buried oxide (through)
.8	Dismount from handle wafer		720	Soak in acetone to dissolve photoresist
.9	Strip resist		10	Piranha
.10	Rinse		10	5 dump rinse cycles

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.11	Spin, Rinse, & Dry		10	
6.0	**Metal Deposition**			
.1	Buffered oxide etch		10	10 min to remove deposited and native oxides
.2	Rinse		10	5 dump rinse cycles
.3	Spin, Rinse, & Dry		10	
.4	Deposit adhesion layer	Temescal VES-2550	9	10 nm titanium
.5	Deposit main conductor	Temescal VES-2550	16	100 nm gold
7.0	**Dicing**	Disco DAD-2H/6T		
.1	Set up tool		10 ea.	Use silicon cutting blade. Calibrate blade height. 13 mm wide steps across dies + 240 μm blade width, 3mm between dies. Two or three cuts through thickness
.2	Mount wafer		10 ea.	Tape wafer on one side with diesaw tape, mount and align on stage, calibrate test cut
.3	Cut first direction		45 ea.	13 mm die width, 3 mm separation

Step	*Process*	*Machine*	*Time (min)*	*Specifics*
.4	Rotate stage			90°
.5	Cut second direction		45 ea.	13 mm die width, 3 mm separation. look for releasing dies and collect
.6	Unmount wafer			
8.0	**Separate Dies**			
.1	Release dies		720	Soak in acetone or UV expose to soften adhesive
.2	Inspect extractors		30 ea.	Look for damaged grids, flawed apertures

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