A Comparative Study of High Voltage Analog Switch Topologies

by

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S.B. EE, M.I.T., 2013

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science
at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
June 2014

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Abstract

The design of electrical switches continues to develop as the demand on performance specifications increases and device fabrication processes improve. They have application in automated test equipment, variable gain feedback amplifiers, sample and hold circuits, and other switched capacitor circuits. In this document, four high voltage analog instrumentation switches were designed using different topologies. The four switches were then compared with respect to various important switch performance characteristics.

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Acknowledgments

I would like to express my gratitude to Linear Technology for giving me the opportunity to work with their excellent engineers on this project. This project would not have been completed without the help, training, and patient teaching of my thesis supervisor at Linear Technology, Adam Shou. I would also like to thank Brian Hamilton, for guiding me, keeping the project on track, and for making me start writing up this document early enough.

I would also like to thank Professor David Perreault, my MIT thesis supervisor for making sure my project stayed on track, and for reviewing this document. My thanks go to the EECS department at MIT for the VI-A program.

My gratitude also goes to Tyler Hutchison and John Fiorenza for their help and encouragement through the process. The car talks will always be remembered fondly. Thilani and Wendi, your guidance was invaluable. Eko, thank you for making me get my driver’s license.

On a more personal note, I would like to express my sincere gratitude to my family for always encouraging me through the toughest of times. I thank God for the opportunities He has given me, and for giving me the support of a loving family to take on challenges, even from thousands of miles away. For the family that’s closer to MIT, thank you for looking out for me.

And for all the wonderful people I have had the pleasure of meeting during my time at this great Institute, I am grateful. I was blessed to have an ever supportive academic advisor, Jing Kong, who took the time to make sure I stayed on the path towards a fruitful and successful semester, every semester. For all the friends, and my fellow course 6-1 students, thank you for the fun times that we had on this wild journey.
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Chapter 1

Introduction

High voltage analog switches have application in many fields, for example in medical devices like ultrasounds, motor drive, power conversion and switched-mode power supplies, and in automotive applications. They are also important in automated test equipment (ATE) setups where it is important to be able to electrically control the turn on and off behavior of the switches used. All characteristics of the switch that affect the accuracy of the ATE measurements have to be taken into consideration.

The main difference between low voltage and high voltage switches is the range of voltages that can be applied between the terminals of the switch. Low voltage normally applies to up to 15V. The 150 volt switches discussed in this project can take up to 150V between the two terminals T1 and T2, allowing a wide swing in signal voltage.

There are two types of high voltage switches: power switches and instrumentation switches. Power switches are designed to carry large currents, therefore very low on resistance, wide robust operating region, and good thermal behavior are the most essential electrical characteristics. On the other hand, instrumentation switches usually carry lower current, which leads to a requirement of relatively constant on resistance over a wide range of currents, low charge injection, and very low leakage current, which would lead to voltage offset, especially when used in current sensing applications.

The switches were designed in a BCD, non Silicon On Insulator (SOI) process
which provides bipolar, CMOS and DMOS (double diffused MOS) devices. However, using a non SOI process means that the parasitic devices, which could lead to latch up risks, have to be taken into account.

1.1 Thesis organization

Since the purpose of this project is a comparison of switch topologies, each chapter will cover a different aspect of the switch design, explain the concept, quantify the specification and perform a comparison of the expected behavior of each topology. Additional circuitry may be added to improve performance.

Chapter one introduces the topologies, and later chapters will cover important electrical characteristics for each switch topology, gradually increasing the functionality and complexity of the switch from the simplest form to a complete system. Finally, tests will be performed side-by-side for a complete comparison of all four topologies.

1.2 Devices used

The high voltage PMOS (HVPMOS) devices are double diffused drain MOSFETs with a lightly doped drain profile. The spacing between the drain contact and the gate is long so that it can allow up to 150V between drain and source. These devices are large and take up a lot of space on the die because of the large spacing required for junction isolation between the drain and the body, and between the body and the substrate. They were used mainly in the input signal path and as high voltage cascode devices in the switch control circuitry. Figure 1-1 shows a simplified cross section of the HVPMOS device used in this project.

The P- region beside the drain is known as the drain extension area and takes over the blocking voltage. These devices have the disadvantage of a low current-load capacity because the P- area demands a large part of the surface of the semiconductor. [3] This device also has a parasitic vertical PNP device shown in the figure.
Other low voltage MOSFETs are also used in this project. These devices are smaller and offer good device matching.[6] They are also more accurate because of better parameter control in the process, and thus were used for more accurate current mirrors and low voltage comparators.

Table 1.1 below summarizes the main transistors used in the design and schematics shown in this document, and their maximum operating voltages. The extended drains of the HVPMOS and HVNMOS are indicated on the symbol with three diagonal lines for easy recognition.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Symbol</th>
<th>VDS max</th>
<th>VGS max</th>
<th>VBS max</th>
</tr>
</thead>
<tbody>
<tr>
<td>HVPMOS</td>
<td><img src="image" alt="Symbol" /></td>
<td>150</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>LV PMOS</td>
<td><img src="image" alt="Symbol" /></td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>HVNMOS</td>
<td><img src="image" alt="Symbol" /></td>
<td>150</td>
<td>15</td>
<td>0</td>
</tr>
<tr>
<td>LV NMOS</td>
<td><img src="image" alt="Symbol" /></td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 1.1: Table showing main transistors used in this project
Chapter 2

Topologies and operation

A simple switch topology would use a single high voltage MOSFET between the switch terminals. For example, with a single HVPMOS device, as shown in figure 2-1 below, with the drain-body and source-body diodes explicitly shown.

![Figure 2-1: Single HVPMOS switch](image)

This switch would only work for unipolar application, i.e. one voltage is known to be always higher than the other. If the body and the source are tied together, the drain-body diode would be forward biased when the source voltage falls below that at the drain. Additionally, this single MOSFET switch would carry some part of any AC signal via the drain-body diode, even when the switch is off.

Since the HVPMOS devices in this process are not symmetric, the body-source breakdown voltage is much lower than that at the body-drain junction. Thus two PMOS devices were used in series between the switch terminals, enabling design of symmetric bi-directional switches without this restriction, enabling the switch to stand 150V in either direction. This also adds a middle node which allows more control over turn on and turn off behavior of the switch.
For this project, two main topologies are covered; drain coupled, and source coupled switch topologies, which both provide a symmetric bi-directional switch. They differ by which of the HVPMOS nodes are connected together.

2.1 Drain coupled switch

The first drain coupled switch topology (DC1) uses two HVPMOS devices connected at their drains. A simplified version of the topology is shown below. Devices P1 and P2 are 150V HVPMOS transistors, and their shared drain node is labeled DP. Their gates will be referred to as GP1 and GP2 respectively.

![Simplified drain coupled switch topology](image)

Figure 2-2: Simplified drain coupled switch topology

The VGS generators shown in the schematic control the gate drive voltages for P1 and P2 depending on the external control voltage “ON” which signals for the switch turn on/off behavior. For the switch to be turned off (open), pin ON is pulled low (VM) and for the switch to be on (closed), it’s pulled high (VM + 5V). Since P1 and P2 have independent source and gate voltages, two separate (but identical) VGS generators are required. When the “ON” signal is high, both VGS generators turn on P1 and P2, creating a low resistance channel path from T1 to T2.

When the switch is on and operating normally (low load current), the voltages at T1, DP, and T2 are approximately equal, and with a VSG of about 5V, both P1 and P2 are in triode mode of operation, behaving like linear resistors.

For switch turn off, node DP is pulled down to VM by current $I_{PD}$ to ensure that the body diodes of P1 and P2 are reverse biased, regardless of the voltage levels at
T1 and T2.

This topology has limitations due to leakage current and the fact that the maximum voltage across the terminals has to be limited to prevent turn on of the vertical PNP parasitic device that is part of the HVPMOS structure.

For the purpose of this study, the node labeled T1 was considered the input side and T2 the output, where the input is connected to a voltage source, and the output to the load.

### 2.2 Drain coupled switch v2

Figure 2-3 below shows a simplified schematic of the second drain coupled switch topology, DC2.

![Simplified drain coupled switch topology, version 2](image)

Figure 2-3: Simplified drain coupled switch topology, version 2

Similar to DC1, this topology uses two HVPMOS devices connected at the drain. However, the body ties for P1 and P2 are changed to give a new topology, DC2. The body is biased to the higher of the drain and source voltage of P1 (and P2) by a maxer circuit. The behavior of a two input maxer is simply described by equation 2.1.

\[
V(OUT) = \max(V(IN1), V(IN2))
\]  

(2.1)

In this case the two maxer inputs were the drain and source voltages of HVPMOS
devices P1 and P2, and the maxer gave the higher voltage as output which was used to bias the body, ensuring that the parasitic vertical PNPs associated with the HVPMOS device structures can be kept off. P1 and P2 each require their own maxer circuit for their body. The maxer has a MOS gate at each input, thus it does not require input current that would be taken from the main signal path. The maxer circuit and other reasons/advantages for using a maxer will be discussed in section 4.3.

### 2.3 Source coupled switch

In contrast to the drain coupled topologies, this source coupled switch (SC1) uses the two HVPMOS devices connected at their sources. A simplified version of the switch topology is shown below. Similar to the drain coupled version, devices P1 and P2 are 150V PMOS transistors, and their shared source node is labelled SP. Since P1 and P2 share a source, with their gates connected (node GP), only one VGS generator is required.

The main operation of this topology is similar to that of the drain coupled switches previously described. However, for switch turn off, current $I_{PU}$ is used to pull up the middle node SP to VP voltage, ensuring that the body diodes of P1 and P2 are reverse biased when the switch is off.

![Simplified source coupled switch topology](image)

Figure 2-4: Simplified source coupled switch topology
2.4 Source coupled switch v2

The source coupled switch can also be implemented using a maxer for the body tie of the common bodies of P1 and P2 as shown below. This gives the fourth and final switch topology, SC2. Given the common body node, this topology can be implemented with one three-input maxer whose output is the highest of the T1, T2 and SP voltages.

\[ V(OUT) = \max(V(IN1), V(IN2), V(IN3)) \]  

This maxer ensures correct body bias even during the switch turn off transient as the source is pulled up to VP.

![Simplified source coupled switch topology, v2](image)

Figure 2-5: Simplified source coupled switch topology, v2

Given the topologies introduced above, some comparison points can already be noted.

<table>
<thead>
<tr>
<th></th>
<th>DC1</th>
<th>DC2</th>
<th>SC1</th>
<th>SC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of VGS generators</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Number of maxers</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2.1: Expected size comparison

From this, it can be expected that switch topology DC2 would have the largest die size when fabricated in silicon, and SC1 the smallest. Depending on the implementation of the VGS generators and maxers, the relative sizes will determine the
final size of the switch topologies. This is an important point to note since die size directly defines the cost of the final integrated circuit.
Chapter 3

DC Characteristics

This chapter deals with the DC characteristics of previously introduced switch topologies DC1, DC2, SC1, and SC2, namely; on resistance, on and off leakage current, and short circuit current. These are very important characteristics in a switch.[5]

3.1 On Resistance

For a switch to more closely approximate ideal behavior, it is desired that the on resistance is minimized, reducing the voltage drop across the switch when closed.

As previously mentioned, the HVPMOS features a lightly doped extended drain which enables it to carry the full current when “on”, and block high voltages when “off”.

Total switch on resistance is a sum of the channel resistance $R_{ch}$ and the resistance due to the drain extension, $R_{dd}$.

For a MOSFET in triode, the source-to-drain current is given by:

$$I_{DS} = \frac{W}{L} \mu C_{ox}(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS} \quad (3.1)$$

Assuming that the $V_{DS}$ is small when the switch is in triode, we can assume that $\frac{V_{GS}}{2}$ is negligible, and derive the channel resistance as in equation 3.2.
\[ R_{ch} = \frac{L}{W} \cdot \frac{1}{\mu C_{ox}} \cdot \frac{1}{(V_{GS} - V_{th})} \]  

From this, it can be seen that the channel resistance is proportional to \( \frac{L}{W} \) and inversely proportional to the gate overdrive voltage. Assuming that the gate overdrive voltage will be approximately the same for P1 and P2 in a given switch topology, then the channel resistance will depend only on the \( \frac{W}{L} \) ratio of P1 and P2. Thus for a fairer comparison between topologies, P1 and P2 have the same length and width in all topologies considered in this project.

Figure 3-1 below shows the dependence of on resistance of a single HVPMOS device on the gate-source voltage. The device used in this test has the same \( \frac{W}{L} \) ratio as P1 and P2 in the switch topologies.

![Plot of on resistance vs VSG](image)

**Figure 3-1: On resistance vs VSG**

From figure 3-1, it can be seen that the dependence of on resistance on gate overdrive voltage is greatly reduced at a \( V_{SG} \) greater than 4V. The extended drain is then the main factor in the on resistance of the switch, and is the limiting factor in the total resistance. In order to have control over the switch resistance for current limiting purposes, a \( V_{SG} \) was chosen such that \( R_{ch} \) was about 10% of the total switch \( R_{ON} \).

The resistance of the extended drain depends on the sheet resistance of the drain.
material, and the length of the drain extension region, $L_{dd}$.

\[ R_{dd} \propto \frac{W}{L_{dd}} \]  

(3.3)

Given that $L_{dd}$ is fixed in the device process, $R_{dd}$ can only be altered by changing the width of the device. Given the measurements in figure 3-1, the drain resistance can be approximated to be about 80Ω.

Given the strong dependence of switch on resistances $R_{ch}$ and $R_{dd}$ on the width of the device, the same width was used in devices P1 and P2 in all switch topologies, in order for them to all have approximately the same on resistance.

Total switch resistance is also known to be related to the breakdown voltage, $V_B$ of the device, that partly determines the voltage rating of the device. [1]

\[ R_{DS(ON)} \propto V_B^{2.6} \]  

(3.4)

The high voltage rating of the HVPMOS devices explains the relatively high on resistance of these switches.

This figure only shows the range of $V_{SG}$ values when the switch is sufficiently turned on. Not shown in the figure is the 165MΩ resistance at VSG below 0.3V. Thus for switch turn off, VSG was set to -1V to ensure behavior close to ideal.

### 3.2 Leakage current

Leakage current is an important DC characteristic of a switch because of the loss of current and the voltage offset it causes. It is desirable to minimize the switch leakage current in both on and off states of the switch.

The main causes of leakage in the switches are the reverse biased diodes in the main switch path. At low reverse bias voltage, diode current is approximately independent of voltage, but increases with temperature. However, at a reverse bias greater than a few $\frac{kT}{q}$, the diode reverse current is given by [7]
\[ i_{rev} = \frac{A q n_i}{2 \tau_0} w(v) \]  \hspace{1cm} (3.5)

where \( A \) is the area of the junction, \( n_i \) is the intrinsic carrier concentration, \( \tau_0 \) is the carrier lifetime in the depletion region, and \( w \) is the width of the depletion region, which depends on the applied reverse bias voltage, \( v \). The intrinsic carrier concentration \( n_i \) depends on temperature as shown in the equation below:

\[ n_i \propto T^{3/2} \]  \hspace{1cm} (3.6)

It is thus expected that the leakage current of diodes in the HVPMOS devices will increase with size, temperature, and reverse bias voltage.

In the following sections, expected leakage current will be discussed with the aid of schematics of main switch path devices, explicitly showing the diodes. Actual behavior will depend on the implementation of all parts of the switch design and will be revisited and further discussed later.

3.2.1 On Leakage

When the switch is on and functioning normally in DC conditions, with low load current, it is expected that for the drain coupled switch, T1, DP and T2 will be at approximately the same voltage. And similarly for the source coupled switch, T1, SP and T2 voltages are expected to be very close.

Figure 3-2 below explicitly shows the diodes in the main switch path that contribute to the leakage current when the switch is on. The pull up and pull down current sources have cascode devices that add high voltage drain-body diodes, which also contribute to leakage current and have thus also been included for each topology. Since the switch is on, the terminals and middle nodes (DP or SP) are expected to be at about the same voltage. Thus the drain-body and source-body diodes of P1 and P2 in all topologies are essentially shorted out and are not explicitly shown in figure 3-2.

For DC1, diodes D1, D2 and D5 are the main causes of leakage current, leading
to the expectation that leakage current will increase with increasing voltage at the terminals T1 and T2 as this increases the reverse bias voltage across D1, D2 and D5.

Similarly, for DC2, D1, D2 and D3 are reverse biased. However, D1 and D2 currents are sourced by the maxer, and do not contribute to the leakage current measured at the terminals. As T1 voltage increases, the reverse bias on D3 increases as well, and as such, the leakage current is expected to increase with terminal voltage. Less on leakage current is expected in DC2 than in DC1.

For SC1, D3, D4 and D5 are expected to be the main causes of leakage current. D5 leakage current can provide the leakage current to D3 and D4 from VP, and any extra (/deficit) current flows to (/from) the terminals and is measured as leakage. Thus for SC1, it is expected that leakage current will increase with terminal voltage, crossing the point of zero leakage when D5 current is exactly equal to the sum of D3 and D4 currents.

With the maxer in SC2, D3 and D4 currents are provided by the maxer and D5 is expected to be the main cause of leakage current, whose magnitude is thus expected to decrease with terminal voltage, to a final value of 0 when D5 has 0 volts across it.
3.2.2 Off Leakage

Off leakage depends on the behavior of the diodes shown in figure 3-3.

When a drain coupled switch is tuned off, the common drain node DP is pulled down to VM. For DC1, the measured leakage current will thus depend on diodes D1, D2, D3 and D4, and is expected to increase with increasing terminal voltage.

For DC2, reverse leakage current is supplied by the maxers. Only D4 and D5 currents are measured at the terminals. Since the maxers hold the bodies of P1 and P2 close to their respective source/terminal voltages, D4 and D5 have only a small reverse voltage across them. Thus the leakage current measured at the terminals is expected to be small and approximately constant for DC2 in off state, over the range of T1 voltages.

For turn off of the two source coupled topologies, the sources and bodies of P1 and P2 are pulled up to VP, thus the maxer is not needed and is not shown in figure 3-3. As a result, the same diodes, D1 and D2, determine leakage current in both SC1 and SC2 topologies. Their reverse bias voltage reduces as terminal voltage increases, leading to reduced leakage current measured at the terminals.
3.3 Short circuit protection

It is desirable that the switches are protected in the event of a short circuit. Take for example SC1, which is replicated below.

If T2 is tied to ground, and T1 voltage is slowly increased, then at low voltages, P1 and P2 are in triode and behave like resistors, and the voltage divides equally between the two devices. Assuming a body diode forward voltage of 0.7V, when T1 voltage reaches 1.4V, the body diode of P1 will be turned on, turning on its parasitic vertical PNP device. As T1 voltage is further increased, the voltage across P1 does not increase and most of the drop falls across P2, and the switch no longer behaves resistively. Thus in order to prevent this from happening in SC1, assuming an $R_{ON}$ of 200Ω the maximum current that the switch should carry is 7mA as derived below:

$$I_{\text{max}} = \frac{0.7V}{\frac{R_{ON}}{2}} = \frac{0.7}{100} = 7mA$$  \hspace{1cm} (3.7)

Similarly for DC1, if T1 voltage is increased as T2 is tied to ground, when T1 reaches about 1.4V, the drain-body diode on P2 clamps its $V_{DS}$ to 0.7V and as T1 is further increased, extra voltage falls across P1 while that across P2 is fixed.

However, the switches with maxers for body bias (DC2 and SC2) can go to much higher voltage difference between terminals without turn on of the vertical PNP of P1 or P2. If the maximum $V_{BS}$ is clamped at 7V by the maxer, this would give a 10x increase in the range of differential voltage in which switch behavior is resistive.

In the case that the switch is forced into a short circuit condition, with a large
voltage applied between its terminals, it is important to protect the main switch HVPMOS devices P1 and P2 from damage. A short circuit current limit was chosen to prevent the body diode (and parasitic vertical PNP) from turning on in such a DC condition.

Different mechanisms may be used to limit the short circuit current. For the four topologies, these mechanisms were implemented within the VGS generator scheme, reducing the $V_{SG}$ in order to reduce the current that the switch will carry. The following subsections will introduce the VGS generator schemes used in each switch topology.

### 3.3.1 Drain coupled switch VGS generator

As previously mentioned, the VGS generator controls the turn on and turn off behavior of the switch, as well as the short circuit current limiting. For the drain coupled topologies, current limiting is implemented by reducing the gate overdrive voltage on P1 or P2 when a short circuit condition is sensed.

A simplified schematic of the VGS generator used for the drain coupled switch topology is shown in figure 3-5 below.

The main switch HVPMOS devices, P1 and P2 each require a separate VGS generator in the drain coupled switch topologies. For each device, the source, gate and drain would be connected to the appropriately labeled terminals of the VGS generator.

When the switch is on and operating normally (low load current), the gate drive is generated by the voltage drop across resistor R1. The maximum $V_{SG}$ is clamped by the zener diode, U12. Since node VSB2 is the buffered source voltage from P1, the gate voltage generated will be referenced to the source as required.

For switch turn off, current source I4 is connected and the Schottky diode U11 is forward biased. The Schottky forward voltage drop, in addition to the $V_{SG}$ of the source follower device U9, ensure that the $V_{SG}$ of P1 is negative, ensuring complete turn off of the HVPMOS.

The value of R1 is chosen to give a 5V gate overdrive when the switch is on. The
step up of the $V_{SC}$ of the source follower has to be compensated for. This could be done by increasing the resistor size, but use of the diode connected HVPMOS device, U4 ensures that the source follower $V_{SG}$ is better canceled out over temperature and process variations.

In the case of a short circuit condition, if for example T1 is pulled up to VP and T2 is shorted to ground, most of the voltage drop occurs across P1, putting P1 in saturation and leaving P2 in triode, and the switch carries a large current. The strategy used to limit the current in this topology is to reduce the gate overdrive voltage on P1 to a value that limits the current to a known and acceptable amount. The short circuit condition is sensed by replicating the gate, drain, and source voltages of P1 onto P1DUMMY (in the VGS generator), an HVPMOS similar to P1. Thus the current through P1DUMMY is representative of the P1 current. The $\frac{W}{L}$ ratio of P1DUMMY is scaled from that of P1 so that less current can be used in the VGS generator during current limiting, saving on power consumption. This also saves some space on the die since P1 and P2 have large width $W$ to minimize on resistance.

Since this VGS generator circuit employs feedback to control the VGS from the
sensed current, the loop stability was tested using Middlebrooks Null Double Injection Method [4], breaking the loop at the drain of device MN1. Using this method, the loop was found to be stable. Stability was also tested under different load, source and temperature conditions and the results showed loop stability in all the tested conditions.

The same VGS generator was used for both drain coupled switch versions; DC1 and DC2.

### 3.3.2 Source coupled switch VGS generator

For SC1, a simple VGS generator with Zener and Schottky diodes for turn on and turn off mechanisms was implemented, as shown in figure 3-6 below.

![Simplified VGS generator for SC1](image)

Figure 3-6: Simplified VGS generator for SC1

The main input to this VGS generator is the source voltage, which is buffered by HVPMOS U1 source follower. The output gate voltage used to drive the shared gate, node GP. The VGS generator turn on/off is controlled by node ONVGS, which goes up to VM + 5V, and for turn off, it goes to VM.

The Zener diode DZ1 is reverse biased to give a 5V VGS for switch turn on. For switch turn off, a small current from device I4 is used to pull the gate voltage above
the source, forward biasing the Schottky diode. The low Schottky forward voltage, in addition to the $V_{SG}$ of the source follower creates a negative source-gate voltage, to ensure that P1 and P2 are completely off.

This VGS generator implements turn on and turn off of the switch, but does not include any short circuit current limiting. This adds to the advantage of SC1 in simplicity and die space savings. It also aids in the comparison of topologies by enabling any shortcomings or advantages of the simplicity of this VGS generator scheme to be shown clearly in the final comparison.

For switch topology SC2, with the maxer, a different VGS generator scheme was used to take advantage of the body bias scheme to incorporate short circuit protection. In the case of a short circuit, if for example T1 is tied to VP and T2 is grounded, most of the voltage drop falls across P2, pushing P2 into saturation while P1 remains in triode. With the maxer, the bodies of P1 and P2 are essentially both connected to T1 voltage, which will be higher than T2. This creates a separation in the body and source voltages for P2. Simplifying P1 as a resistor, the main switch devices can be viewed as in figure 3-7.

![Figure 3-7: Simplified SC2 short circuit model](image)

From this representation, it can be seen that as the switch current increases, the source-body separation for P2 increases, and by the body modulation effect, P2's threshold voltage is increased, reducing the effective gate overdrive voltage and thus the drain-source current in the switch main devices P1 and P2. This topology thus has self-protecting behavior for short circuit conditions.

To more reliably limit the amount of short circuit current, the short circuit con-
dition above is replicated in the VGS generator, as shown in figure 3-8 below, using scaled down dummy devices, a scaled amount of the short circuit current limit, and the maximum targeted body and source separation voltage. This VGS generator then creates a constant VGS that would limit the maximum switch current to 30mA, i.e. a constant VGS of about 3.5V.

![Figure 3-8: Source coupled switch current limiting VGS generator.](image)

Current ILIM shown in figure 3-8 is a scaled amount of the current limit and is drawn through a HVPMOS device PDUM, which is a scaled version of the main HVPMOS devices in the main switch path, P1 and P2. The VBS set by the circled devices is the chosen maximum VBS of 7V. The VGS of PDUM is therefore the VGS that would enable PDUM to carry current ILIM, as is shown as VGS SET in the
dashed square. This voltage is then copied to VGS OUT, referencing it to the source voltage VS. The outputs of this VGS generator are thus VSbuf, a buffered copy of the source voltage, and VG, the gate drive voltage.

The table below summarizes the comparison of the DC characteristics discussed in this chapter. Since it is difficult to summarize the expected leakage current behavior, the table will only include expected on resistance and a comparison of the VGS generators designed. The simplicity of the VGS generator circuit is expected to correspond with the size of the circuit, especially where many HVPMOS devices are needed. The VGS generators can also be compared by whether each has current limiting capabilities. The current limits were all set to 30mA as previously described.

<table>
<thead>
<tr>
<th>-</th>
<th>DC1</th>
<th>DC2</th>
<th>SC1</th>
<th>SC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>RON (Ω)</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Simple VGS generator circuit</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✗</td>
</tr>
<tr>
<td>Current limiting</td>
<td>✓</td>
<td>✓</td>
<td>✗</td>
<td>✓</td>
</tr>
</tbody>
</table>

Table 3.1: VGS generator comparison

Given that the P1 and P2 devices in each topology have the same $\frac{W}{L}$, they are all expected to have a total on resistance, between terminals T1 and T2, of about 200Ω.

The drain coupled topologies have both simplicity and current limiting abilities, whereas both of the source coupled versions have one or the other.
Chapter 4

Charge Conservation

An ideal switch passes all charge from the input to the output. In this study, charge conservation refers to maintenance of the same input charge required by the switch over a wide range of slew rates, for a fixed input voltage step size. Charge conservation is a key design parameter for an instrumentation switch and is an important focus of study in this document, because charge loss leads to a voltage offset. Charge loss that is linear with input step size is tolerable in most applications as it causes a constant gain error that can be fixed by calibration, whereas non-linear gain error is not easily calibrated out.

The ideal input charge vs slew rate plot would be flat up to 1000V/μs, as shown in figure 4-1. This requires that even as the input slew rate increases, no extra charge is taken from the signal path and lost in the switch’s internal capacitances. The figure also shows the measured behavior from switch topology SC1, which does not include a maxer circuit.

The main sources of charge loss in all the switch topologies are:

- The protection diodes at fast slewing nodes which may be momentarily forward biased during a slew transient.

- Turn on of the parasitic vertical PNP device that is part of the isolated high voltage PMOS devices used in the main switch.
A protection diode was used from gate to source on HVPMOS source followers and on HVPMOS cascode devices, as shown in figure 4-2, to prevent the gate voltage from being pulled more than a diode drop above the source voltage, as shown in the figure. If the input to a source follower (VIN) is connected to T1 during fast rising slew, and its output is capacitively loaded, the gate of the HVPMOS U1 may be pulled more than 5V above the source during slew, leading to gate oxide breakdown. By having the diode between the gate and source, the source follower input directly charges the load capacitance, pulling up the source of U1.

This diode therefore leads to charge loss when the source follower input is connected to any of the nodes on the main signal path. If the diode is forward biased during fast rising slew, a lot of current is directly taken from the main signal path and used to charge up internal switch capacitances.

Figure 4-2 simplifies the source follower load as a capacitor $C_{load}$. The protection diode is forward biased when all the source current (IS) is being used to charge the load capacitance. Thus the maximum slew rate, below which the protection diode is not forward biased, is determined by the current, IS, and the load capacitance.

A couple of ways were studied to help reduce the effects of charge loss through
the protection diode on the source follower by ensuring that the protection diodes are not forward biased during fast rising slew, and that the source followers have a sufficient gate overdrive voltage and proper behavior is maintained within the range of slew rates studied.

**Method 1:** Increasing the DC current to the source follower would keep the protection diode reverse biased to a higher slew rate. This is however undesirable as it also leads to an increase in the DC power consumption of the switch.

**Method 2:** To increase the current only during slew, without increasing DC power consumption, a feed-forward capacitor is used to provide extra current during fast rising slew, as shown in figure 4-3 below.

During rising slew of VIN, the capacitor provides current to the cascode device. U3 stays in cutoff during this transient. The amount of added current is proportional to the slew rate at VIN. The equations below demonstrate how this feed-forward capacitor can be used to eliminate the dependence on slew rate.

\[
SR_{in} \cdot C_{ff} + IS = SR_{out} \cdot C_{load} + ISF
\]

(4.1)

Assuming: \( SR_{in} = SR_{out} = SR \):

\[
SR \cdot (C_{load} - C_{ff}) = IS - ISF
\]

(4.2)
Thus by matching the feed-forward capacitor with the load capacitance, the turn on of the protection diode can theoretically be prevented at all slew rates. U1 also gets enough current to prevent collapse of its $V_{SG}$, maintaining proper source follower behavior.

During fast slew current boost, the cascode device U2 has to carry a lot of extra current and its $V_{SG}$ may increase transiently. This could force M1 into triode and significantly reduce the amount of current (IS) it can source. U2 therefore is sized with high $\frac{W}{L}$ in order to minimize the variation of its $V_{SG}$ when the slew boost feed-forward capacitor kicks in.

During falling slew, the feed-forward capacitor sinks current to the input of the source follower. Depending on the slew rate and capacitor size, the feed-forward capacitor may draw more current than the current source provides. This extra current would thus be drawn from forward biasing the protection diode on U2 at fast falling slew. Thus the low voltage NMOS, U3, was added so that the extra current is sourced from the power supply, VP, as shown in the figure. U3 is off at slow slew and turns on just before the cascode device is forced off. The U3 device size depends mainly on the size of the feed-forward capacitor and the amount of current from the current source. The larger the feed-forward capacitor size, the higher the $\frac{W}{L}$ of U3. The larger the
current source, the smaller the $U_3 \frac{W}{L}$ ratio needed.

The main trade-off with this method is that it leads to increase in the input capacitance of the switch.

Method 2, using only a feed-forward capacitor, was chosen due to its simplicity and easy scalability. Method 1 is not easily scaled to prevent charge loss at fast slew rates when the source follower is loaded with a large capacitor since that would mean a large increase in DC power consumption. Additionally, since these protection diodes are not the biggest source of charge loss, more space and care was taken with the biggest source of charge loss, which is described in the next section.

4.2 Vertical PNP

The HVPMOS devices P1 and P2 between the terminals T1 and T2 have parasitic vertical PNP devices associated with their layout. The base of the PNP is the HVPMOS N-type body, the emitter is the P-drain extension, and the collector is the P-type substrate. Measurements of the drain side PNP behavior are shown in figure 4-4.

The test setup shows that gate, body and source were tied together to ensure that the channel between drain and source was turned off, and the body-source diode shorted out. This measurement gives data about the drain-side vertical PNP behavior, which is more significant than that of the source-side vertical PNP due to the relative doping levels of the drain extension and the source.

From the figure, it can be noted that the drain and source currents (id and is) are equal until a drain voltage of 0.5V. The drain side vertical PNP was measured to have a high $\beta$ (up to 273 from the measured data) and low turn on $V_{be}$ of about 500mV. This means that this PNP is very easily turned on transiently and will carry a lot of current to the substrate instead of from T1 to T2 as is ideal for a switch. This parasitic device is the main cause of charge loss in the switches, taking current directly from the main signal path to the substrate. Substrate current is also undesirable because it can lead to latch up issues due to other parasitic devices.

Assuming again that T1 is connected to a voltage source, and T2 is capacitively
loaded, the input slew rate at which this PNP device is turned on will depend mainly on the on resistance of the switches and the load capacitance. At a given load capacitance, the amount of current required to drive the output at the same slew rate, SR is given by the product of the capacitance and the slew rate. With that current, and a known switch on resistance, the slew rate at which the vertical PNP is turned on is given by:

\[ V = IR \]  \hspace{1cm} (4.3)

\[ V_{be} = C_{load} \times SR \times R_{on} \]  \hspace{1cm} (4.4)
\[
SR = \frac{V_{be}}{C_{load} \times R_{on}}
\]  

(4.5)

It can thus be expected that this turn on slew rate will be higher for lower switch on resistance, and lower load capacitance.

The available SPICE model for the HVPMOS device did not include a model for the vertical PNP device to the substrate. However, a behavioral model was made from the measured data shown in figure 4-4, using ideal current sources to model the instantaneous substrate current. The implementation of the model is shown in appendix A. However, this simplified model does not include any dynamic components, like that body-drain capacitance and the body-substrate capacitance, due to their dependence on the device layout in silicon.

The behavioral model of the vertical PNP was added to the main switch devices P1 and P2 in order to see its effect on charge conservation as slew rate is varied. This vertical PNP charge lost to the substrate was found to be the major source of charge loss. Thus it was important to prevent this charge loss by preventing the vertical PNP from turning on transiently. This could be achieved by tying the device body to the higher of the drain or source voltage for P1 and P2. This required the design of a maxer circuit to create the body bias, and that the maxer is fast enough to maintain the vertical PNPs in an “off” state at high slew rates. The maxer is further discussed in the next section of this document.

### 4.3 Maxer circuit

The maxer circuit takes two voltages as inputs, and its output is the higher of the input voltages. An easy two-input maxer circuit would use two diodes and a pull down current. However, diodes tend to have long turn off times due to the reverse recovery charge, which would slow down a diode maxer as it switches between the two inputs. Thus, the current mirror based maxer circuit shown in figure 4-5 was used.

The maxer input voltages IN1 and IN2 are buffered by source followers (U30 and
Figure 4-5: Maxer circuit schematic

U33), before being fed to the mirror maxer. The behavior of the maxer shown above is mostly determined by the devices in the current mirror, M4, M5 and M6. Since the inputs to the maxer can be anywhere in the 150V range, low voltage devices are used in the mirror, and high voltage cascodes used to carry the extra voltage. $I_{PU}$ is chosen to be $2.5I_{PD}$. Since device M4 is diode connected, it is in saturation and takes $I_{PD}$. If IN1 is at a higher voltage than IN2, then M5 is in saturation and carries $I_{PD}$ and M6 is in triode and only gets the remaining $0.5I_{PD}$. Given that M6 is in triode, $V_{MAXHiZ}$ is close to IN1 voltage, so the buffered output of the maxer, VMAX, also follows IN1. Since IN1 is buffered by a source follower, VMAX is about one HVPMOS $V_{SG}$ above IN1.

The drain coupled switch topology requires two maxers since the sources of P1 and P2 are separate. Each maxer thus takes the source and drain voltages of a HVPMOS as inputs, and outputs the body bias voltage. Given that the maximum $V_{BS}$ for these devices is 13V, as in table 1.1, a voltage clamp was added between the buffered maxer input from the source, and the output node to the body. The clamps are especially needed during short circuit conditions when T1 and T2 could be up to 150V apart, and also during very fast slewing of either terminal voltage when T1 and T2 may be momentarily separated during slew.

When the drain coupled switch is turned off, the drain is pulled down to VM, and
since this should not affect the maxer output, the maxer does not need to be turned off when the drain coupled switch is turned off.

The source coupled switch can use one two-input maxer since P1 and P2 share source and body nodes. The inputs to this maxer would be T1 and T2, and the output would be the body bias voltage. This maxer would then have to be turned off with the switch, so that the body can be pulled up to VP with the source, preventing $V_{BS}$ breakdown.

Alternatively, a three input maxer could be used. This maxer would take T1, T2, and the source SP as inputs, and output the highest of the three voltages, which would be used to bias the body. Since this maxer should be able to follow the source to VP during switch turn off, this maxer would not need to be turned off when the switch is turned off. The maxer would follow the source and ensure that the $V_{BS}$ remains within the accepted range. The three input maxer is based on the same mirror maxer, only adding one more stem to the mirror, and scaling up $I_{PU}$ to $3.5I_{PD}$, as depicted in figure 4-6.

![Figure 4-6: Three input maxer circuit schematic](image)

Thus by simply adding feed-forward capacitors to all source followers at high slew rate nodes in the signal path, charge loss via the protection diode can be prevented in
all switch topologies. However, charge loss by the vertical PNP can only be prevented in the switch topologies with maxers, i.e DC2 and SC2.
Chapter 5

Charge injection

This chapter examines the turn on and turn off transient behavior of the switch topologies, and the turn off charge injection during this transient. Turn off charge injection is measured as the product of the load capacitance and the change in output voltage during the turn off transient.

From the test shown in figure 5-1, the charge injection would be measured as:

\[ Q_{\text{inj}} = c_{\text{load}} \times \Delta V_{T2} \]  

(5.1)

This change in output voltage could affect ATE measurements and/or cause other unwanted behavior in the circuitry on the other side of the switch. It is therefore beneficial to minimize the effects of the turn off transient on the output voltage.

The voltage increase on the capacitively loaded output node T2 when the switch is turned off could be due to the HVPMOS channel charge, or a result of capacitive coupling. When the switch is on, P1 and P2 channels are filled with holes, and when the switch is turned off, the channel charge may move to the output, increasing the
amount of charge on the load capacitor, and thus the T2 voltage. This is known as charge injection.

To check if channel charge is the main cause of the $\Delta VT_2$, using source coupled switch topology SC1 for test, a $V_{SC}$ of -1V is applied to the output side device P2 to ensure that there is no channel charge between drain and source during the slew of the common source node, SP, to the top rail, VP. This reduced $\Delta VT_2$ by only 20% suggesting that channel charge is not the main cause of the rise in T2 voltage, but that the increase in the T2 voltage is mainly due to capacitive coupling from the gate and/or body. Furthermore, since the switch is designed to be symmetric, there is no pre-defined input or output terminal, and the timing of turning off the output side device, P2, before turn off of P1 cannot be implemented. It would however be applicable to a multiplexer where the input and output terminals are defined.

To determine which capacitor is the main contributor to the feed-through, an external capacitance is added in parallel with some of the HVPMOS capacitances as shown in figure 5-2.

In switch topology SC1, the capacitances that affect the output voltage are $C_{gd}$ and $C_{db}$. The charge injection is expected to follow the behavior shown in the equation:

$$Q_{inj}(SC1) = (C_{gd} \times \Delta VGD) + (C_{db} \times \Delta VDB)$$  \hspace{1cm} (5.2)
These capacitances pull up the output at turn off since the gates, source and body have to be pulled up to VP at turn off, i.e. $\Delta VGD$ and $\Delta VDB$ could be up to 150V. By changing the external capacitance, the output voltage was found to be more sensitive to feed-through from $C_{pd}$ than that from $C_{db}$. The effect of $C_{db}$ is further reduced in SC2 due to the buffers at the maxer input that shield the effect of body slew from the terminals.

For the drain coupled topology DC1, the $\Delta VT2$ is dependent on $C_{gs}$ and $C_{db}$.

\[
Q_{inj}(DC1) = (C_{gs} \times \Delta VGS) - (C_{db} \times \Delta VDB)
\]  

For this topology, during turn off, the gates are pulled up, while the drain is pulled down. The $\Delta VGS$ is up to 6V (from 5V to -1V $V_{SG}$), while $\Delta VDB$ could be up to 150V. Thus, this topology has much less charge injection at switch turn off.

Additionally with the maxer in DC2, the bodies of P1 and P2 are held at the terminal voltages as the drain is pulled down, thus the effect of $C_{db}$ is minimal.

Given this, turn on and turn off transient behavior are further discussed below for each topology, with the goal of using a turn on/off timing sequence to minimize the $\Delta VT2$ during the transient.

### 5.1 Drain coupled switch turn off

In order to turn off the drain coupled switch, the VGS generators of P1 and P2 need to be turned off, and the common drain, DP, pulled down to VM to ensure that the body diodes of the HVPMOS devices stay reverse biased, irrespective of the voltage levels of T1 and T2. As previously mentioned, the maxer does not need to be turned off as the bodies still need to follow the source voltages as they may change even as the switch is off.

During the turn off transient, the goal is to minimize $\Delta VT2$, while ensuring that the P1 and P2 are also protected during the transient. To minimize $\Delta VT2$ during the drain pull down transient, drain pull down needs to start after P1 and P2's $V_{SG}$ are both at -1V. This will ensure that the channels of both devices are off and reduce
the effect of that charge path on T2.

The switch turn off sequence would thus be:

1. Turn off P1 and P2’s VGS generators.
2. Wait till $V_{SG}$ goes negative.
3. Pull common drain, DP, down to VM.

Since it is known that the $V_{SG}$, when “on”, is clamped at a maximum of 5V with the help of the Zener diode in the VGS generator, a delay can be added to wait until the $V_{SG}$ drops from 5V to -1V for turn off.

### 5.2 Drain coupled switch turn on

For turn on, the VGS generators need to be turned back on and the drain, DP, pulled up from VM to a voltage between T1 and T2. Ideally, T2 should not be affected by the transient slewing of the drain back up from VM. If the VGS generators of P1 and P2 are both turned on once the switch enable signal is received, then DP will move towards the T1 voltage, pulled up by current from the input through the channel in P1, and T2 will try to follow DP. If T1 is higher than T2 when the turn on signal is received, T2 will first be pulled down towards the drain, then both the drain and T2 will be pulled up towards T1. Ideally, T2 would remain at its “off” voltage until the drain has caught up with it, then both nodes would be pulled up towards T1 voltage. The ideal turn on sequence to achieve that behavior would then be: turn on the input side VGS generator, pull up the common drain DP towards the input voltage, and finally, turn on the output side VGS generator. However, for a single switch, since it is not known which of T1 or T2 will be the input or output terminal, the switch has to be completely symmetric and both VGS generators must be turned on simultaneously. The ideal turn on sequence is therefore:

1. Turn off the drain pull down current,
2. Pull up the drain by an additional current source, to the lower of T1 or T2 voltages,

3. Turn on the VGS generators for P1 and P2.

This way, if T1 was at a higher voltage than T2 just before the switch was turned on, then the drain is pulled up to T2, and when P1 and P2 VGS generators are turned on, T2 and the drain are pulled up to T1 voltage. If T2 voltage was higher than T1, then the drain is pulled up to T1 and when P1 and P2’s VGS generators are turned on, T2 is quickly pulled down towards T1 voltage. This leads to the minimum switch turn on time.

To achieve this sequence, a drain pull up current source is added so that the drain is pulled up from the power supply VP instead of from T1 during the turn on transient. This current source would be turned on as soon as the switch turn on signal was received, and would need to be turned off after the common drain has been pulled up to the lower of the T1 or T2 voltages.

The signal to turn off the drain pull up current needs to be generated by comparators between the common drain, DP, T1 and T2. The drain coupled switch is known to be in the “off” condition when the drain is at a voltage lower than both T1 and T2. Thus, if the drain is lower than both T1 and T2 but the control signal has been received to turn the switch on, then the drain pull up current should be on, and turned off as soon as one of the comparators toggles.

However, the swing between T1 and the drain could be up to 150V, thus a simple differential pair comparator between the two nodes would not be implementable since the absolute maximum VGS of the input devices would be exceeded. As an alternative, information from the mirror maxer was used. The cascode nodes from the current mirror devices were used as comparator inputs as shown in figure 5-3, with the rest of the maxer circuit removed for clarity.

Even though the buffered maxer inputs, IN1B and IN2B, can swing up to a 150V, the HVPMOS cascode devices U1 and U2 would protect the low voltage current mirror devices from the large voltage swing, and thus their sources provide suitable
voltage nodes for use in a differential pair-based comparator.

This comparator would be used in both maxers in the drain coupled switch topology and the outputs from the two comparators (DLO1 and DLO2) used to control the drain pull up current source, turning it on when both comparators indicate that the drain voltage is lower than the terminal voltage.

The Schottky diode used this way creates a threshold so that the drain pull up stops before the drain voltage is greater than that at T1 or T2.

To prevent false turn on of the drain pull up current, the \(\overline{\text{SR}}\) latch shown in figure 5-4 is used so that the drain pull up current is only latched at the initial turn on transient.

The inputs dlo1 and dlo2 are the outputs from the two maxer comparators in the DC2 maxer, and DOFFB is the inverse of the external switch "ON" signal which is also used to control the drain pull down current. DPU is then used to control the
drain pull up current, and ONVGS is used to turn on the VGS generators after the drain pull up. DPU is level shifted to be referenced to VP, and then used to turn on/off the drain pull up current source.

With these turn on and turn off/on sequences, the T2 voltage change is minimal during the turn off/on transients and thus the measured turn off charge injection is low.

### 5.3 Source coupled switch turn off

Similarly to the drain coupled version, the goal here is to minimize ΔVT2 during the turn off transient, thus reducing the charge injection measured. For turn off of the source coupled switch topologies, the VGS generator has to be turned off, and the source and body have to be pulled up to VP to keep P1 and P2 drain-body diodes reverse biased, irrespective of the T1 and T2 voltage levels. The gate of P1 and P2 (node GP) also needs to be pulled up to keep the VSG of P1 and P2 negative, and gate, source and body pulled all the way up to VP to avoid exceeding the absolute maximum VGS and VBS ratings of the devices.

Similarly to the drain coupled switch, for minimal ΔVT2 during turn off, the sequence should be:

1. Turn off the P1 and P2 VGS generator
2. Wait till VSG is negative.
3. Turn on source pull up current.

Since the VSG of this topology when "on" is known and constant, a fixed delay can be used as VSG changes from 3.5V when on, to -1V when fully off. This translates to a short, fixed delay which just needs to be long enough to ensure that the VSG goes to -1V. After this delay, the source is pulled up to VP. This rising slew needs to be sufficiently slow so that VSG remains negative, keeping P1 and P2 off. This can be achieved by using a relatively small pull up current on the source. A pull
up feed-forward capacitor on the gate pull up current in the VGS generator is also used to ensure that the gate and the source slew at about the same rate, maintaining negative $V_{SG}$ during the transient.

### 5.4 Source coupled switch turn on

For turn on, a similar scheme was used as that used in the drain coupled switch. To ensure minimal $\Delta V_{T2}$ during the turn on transient, the VGS generator of P1 and P2 was kept off until the source had been pulled down to the higher of the T1 or T2 voltages. A comparator between T1, T2 and the source was added, using the three-input maxer to signal when the source was close to either T1 or T2 voltages. The comparator is shown in figure 5-5 below.

![Figure 5-5: Three way maxer comparator](image)

The comparator output SHI is high (VM + 5V) when the source is higher than both T1 and T2 voltages, and goes low (VM) when the source voltage is close above T1 or T2 voltages, whichever is higher. SHI is then used with a flip-flop as shown in figure 5-6 below, to control the source pull down current source.

The D flip-flop ensures that the SPD voltage, used to control the source pull down current is latched as soon as the switch “ON” signal is received, and uses SHI from
the comparator to turn the current source off after the appropriate pull down has been achieved.

ONDEL is the “ON” signal delayed by the time it takes for the $V_{SG}$ to go from 3.5V to -1V. OFFDEL is the inverse of ONDEL. They are then used to create the ONVGS signal which is then used to control the VGS generator’s turn on/off timing. The pull down current in the maxer, IPD, is reduced when the switch is turned off. This is to facilitate body pull up. BPD in the above latch is used to return IPD to its normal DC current level to ensure that the body is correctly biased when the switch is turned back on.

With these turn on/off sequences and controls in place, the effect of the transients on the switch terminals is minimized, minimizing the measured charge injection. However, since the turn on control depends on comparators in the maxer, switch topologies DC1 and SC1 do not have turn on control sequence implemented, for simplicity.
Chapter 6

Robustness and Protection

It is important that the main switch devices, P1 and P2, are protected from breakdown over a wide range of operating conditions. The following section summarizes the protection of the devices under various extreme transient conditions. The cases are further discussed in the section following each table.

6.1 Drain coupled switch

Table 6.1 summarizes conditions in which devices need protection when the drain coupled switch is “on”. Switch DC2 is considered here, since the cases for DC1 are a subset of those for DC2. The schematic of switch topology DC2 is repeated below for reference, also showing the added turn on current sources.

![Simplified DC2 with maxer and turn on drain pull up.](image)

**Case 1a** considers the effects of fast rising slew on the P1 $V_{SG}$. The amount of
increase in $V_{SG}$ is controlled by the speed of response of the current limiting in the
VGS generator. Use of a feed-forward capacitor in the VGS generator also serves to
pull up the gate as fast as T1, reducing the transient increase in $V_{SG}$.

Fast rising slew of T1 can cause transient turn on of the body-source diode and
the associated vertical PNP, as in case 1b. This would lead to substrate current
and charge loss. A Schottky diode is used in the maxer to clamp the maximum
body-source voltage, preventing the body-source diode from turning on.

Fast T1 rising slew can also lead to P2 drain side vertical PNP turn on, as in case
1c. This is prevented by ensuring that the maxer is fast enough to prevent vertical
PNP turn on up to 1000V/μs.

Case 1d considers the effect of large capacitive load on T2. As T1 voltage goes
high at a fast slew rate, the drain also is also pulled up fast. This is due to P1 going
into saturation and acting as a current source, providing enough current to pull up
the drain at a high slew rate. The body of P2 follows the drain since the maxer
output follows the higher voltage. Since T2 slew is slowed down by the large $C_{load}$,
the body may be pulled more than the absolute maximum acceptable voltage above
the source of P2. Thus the $V_{SG}$ on P1 needs to be decreased when this condition occurs, reducing the current source effect and allowing the drain to stay close to T2 voltage, thereby preventing the absolute maximum $V_{BS}$ of P2 from being exceeded. This requires sensing of the $V_{BS}$ separation of P2, information which can be obtained from the VBS clamp in the maxer circuit, as shown in figure 6-1 below.

![Figure 6-1: VGS clamp](image)

The clamp used in the maxer circuit is shown in the box in figure 6-1. It serves to limit the maximum body-source voltage. If the body-source voltage of P2 exceeds the set clamp voltage, the voltage drop across resistor R3 turns on device U15. This current is then used to turn on device 12 (circled in figure 6-1) by reverse biasing the Zener diode U2. 12 is used to short the gate and source voltages of P1.

During normal behavior, when the body-source voltage is within the set limits, and the clamp is not on, the pull up current overwhelms the pull down current so that the Schottky diode is forward biased, keeping device 12 normally off. The threshold
point at which I2 is turned on can be controlled using the current mirror ratio and the degeneration resistor R1. The sizing of device U16, relative to that of U15, also determines the threshold by determining the amount of current used by the VGS clamp circuit.

The body of I2 is connected as shown to keep the body above both drain and source, preventing substrate current and also helping reduce the amount of drain-source current when it is turned on with a 5V gate overdrive. This is important since the source of I2 is in the main signal path.

This scheme is implemented in both VGS generators in the drain coupled switch topology DC2. When P1 VBS exceeds the clamp voltage, the same mechanism is used to short out the gate and source of P2.

Cases 2a, 2b and 2c for fast falling slew are covered by the solutions for fast rising slew.

Table 6.2 summarizes conditions in which devices need protection when the drain coupled switch DC2 is off. The same conditions are considered as when the switch is on (table 6.1), with different expected results. When the switch is off, change in T1 voltage ideally would not affect T2. Fast rising and falling slew of T1 are thus considered.

Case 3 considers fast rising slew at T1 when the switch is off. The $V_{SG}$ of P1 could increase transiently, turning on P1 which could then carry large rush current and pull up the drain, which in turn pulls up T2. Ideally, with the switch off, T2 would be unaffected by changes in T1 voltage. Thus the gate of P1 should be pulled up as fast as T1 so that the $V_{SG}$ of P1 maintains the device in cutoff. A feed-forward capacitor from T1 to the gate pull up current helps speed up gate pull up during T1 rising slew.

To ensure that the shared drain, DP, stays at VM, despite rising slew of the input voltage at T1, a low voltage NMOS (MN4 in figure 6-2 below) is added to provide extra drain pull down current if the drain is pulled up when the switch is fully turned off. The comparator shown in figure 6-2 provides gate voltage to turn on MN4 when
<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
<th>Issue(s)</th>
<th>(Proposed) solution(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>T1 fast rising slew</td>
<td>$V_{SG}$ increase could turn switch on, pulling up drain and T2</td>
<td>Gate pull up feed-forward capacitor from T1. Extra drain pull down current during slew.</td>
</tr>
<tr>
<td>4</td>
<td>T1 fast falling slew</td>
<td>P1 and P2 $V_{SG}$ further reduced; P1, P2 stay off, T2 unaffected</td>
<td>Proposed minimum $V_{SG}$ clamp.</td>
</tr>
<tr>
<td>5</td>
<td>Turn off transient</td>
<td>Drain slew down to VM pulls down gate via $C_{gd}$, keeping switch on thus pulling T2 down as well.</td>
<td>Extra gate pull up current during drain slew. Delay drain slew until VGS generators of P1 and P2 completely off.</td>
</tr>
<tr>
<td>6</td>
<td>Turn on transient</td>
<td>Drain slew up affects T2 if VGS generators on during drain slew</td>
<td>Drain pull up before VGS generator turn on.</td>
</tr>
</tbody>
</table>

Table 6.2: Off-state protection cases in DC2

node voltage $v_{td}$ falls below 1V during the turn off drain pull down transient. The comparator also includes a latch at its output to prevent chatter.

Device MN4 needs to be off during initial drain turn off slew because it would otherwise cause an uncontrolled large drain pull down current, leading to fast drain pull down which in turn could cause strong pull down on the gate via $C_{gd}$, turning P1 and P2 back on.

However, if the terminal (and drain) voltage are already below 1V before switch turn off, the comparator will not trigger. Thus another feature was needed to trigger it a set time delay after switch turn off. Having chosen a drain pull down slew rate of $20V/\mu s$, the longest drain slew time would be $7.5\mu s$ and thus this was chosen for the delay.

As in case 4, if T1 voltage falls at high slew rate when the switch is off, the $V_{SG}$ of P1 could be further reduced, thus the drain and T2 should not be affected by T1, as is ideal for the switch in off condition.

The transients in cases 5 and 6 are controlled by the turn on and turn off sequences discussed in chapter five. Additionally, the extra gate pull up current shown in figure 6-2 kicks in during drain slew to ensure that the $V_{SG}$ of P1 and P2
6.2 Source coupled switch

Similar methods were used in the source coupled switch to protect P1 and P2 for each of the conditions considered for the drain coupled switch. Testing for all these conditions helped in tuning the clamps and maxer feed-forward capacitors to ensure the responses were fast enough.

Similarly to case 3 in the drain coupled topology, extra source pull up current was added to cater for T1 fast falling slew while the switch is off, preventing source pull down, as this would violate expected "off" behavior. As previously discussed, turn on and turn off sequences help ensure proper switch behavior during those transients.
Chapter 7

Tests and Comparison.

After completing the design of the necessary blocks for all four switch topologies, each was subjected to the same simulation-based tests to perform a fair comparison of their characteristics. The following sections present and discuss tests and results.

Identical symbols were made for each switch to ease test setup. The symbol is shown below.

![General switch symbol](image)

Figure 7-1: General switch symbol

T1 and T2 are the two terminals of the switch. VP and VM are the power supply rails for the switch, with VP=150V and VM connected to ground for the tests below. V5P is VP - 5V (145V) and V5M is VM + 5V (5V). ON is connected to the enable signal for the switch and is referenced to VM; VM + 5V to turn on the switch and VM to turn it off. IIN is a 5μA reference bias current.

ISUB1 and ISUB2 tap into the substrate current from the vertical PNP models in the switches, allowing for measurement of the total substrate current from P1 and P2 on the test bench level.
7.1 On resistance

Given that the main switch devices P1 and P2 have the same size in all topologies, it is expected that they will all have approximately the same on resistance.

The test for simulation of large signal on resistance is shown in figure 7-2 below.

The switch is turned on by applying 5V to the ON pin. T1 voltage was set between the two voltage rails at 75V, and the DC current drawn from the switch (IODC) swept from 0 to 30mA (30mA is the current limiting value set for the switches.) The on resistance was then calculated using the equation:

\[ R_{ON, \text{large signal}} = \frac{V(T2) - V(T1)}{IODC} \] (7.1)

The results are presented in figure 7-3 below.

From the figure, we see that at low current levels, the on resistance of all four switches is approximately the same at about 200\( \Omega \), as expected. As the current increases, the resistance of DC1 and SC1 is seen to reduce. This is due to the turn on of a vertical PNP in the main HVPMOS devices (P2 in DC1 and P1 in SC1) which leads to clamping of the \( V_{DS} \) of that device and thus the total impedance of the switch is reduced.

The resistance of DC1, DC2, and SC2 is seen to increase at even higher current levels, as the current limiting scheme kicks in.

From the results, we see that a constant on resistance is maintained for a wider range of current values in the switches with the maxer body tie, DC2 and SC2, as compared to those without a maxer, DC1 and SC1. Sharper current limiting, which is more desirable, is seen in SC2 than in DC2.
Figure 7-3: Large signal on resistance
The small signal on resistance was simulated as shown in figure 7-4. With a small output current of 1μA, the input voltage T1 was swept from VM to VP, and the test was performed at temperatures of -45°C, room temperature (25°C), 85°C, and 125°C.

![Figure 7-4: Small signal on resistance test.](image)

The results are shown in figure 7-5, from which it can be seen that all four topologies have approximately the same on resistance at all temperatures, but resistance increases significantly over temperature.

When T1 is at a voltage below 5V, the resistance goes up in all switch topologies because they only use PMOS devices and the $V_{SG}$ is forced to reduce since the gate voltage cannot go below 0V. This could be remedied by using NMOS devices in parallel with the PMOS devices, and the NMOS path would be able to stay on even with T1 at 0V.

The switch resistance is seen to increase at high terminal voltages as well, and this is due to lack of headroom for the current sources in the switch, especially in the $V_{GS}$ generators, leading to decreasing gate overdrive and thus higher on resistance.

### 7.2 Leakage current

Figure 7-6 below shows the test setup used to simulate leakage current.

For this test, the switches were turned on/off, and the current into pin T1 measured. T1 voltage was swept from VM to VP, and the test was performed at temperatures of -45°C, room temperature (25°C), 85°C, and 125°C.

The measured leakage current is expected to differ slightly from the previously discussed behavior in section 3.2 for switch topologies DC2 and SC2 due to the
Figure 7-5: Small signal on resistance over temperature test.
Figure 7-6: Off leakage current test setup.

Figure 7-7: On leakage diodes

addition of turn on pull up/down current sources, which add more reverse biased diodes to the picture.

7.2.1 On leakage

Figure 7-7 shows the updated picture of diodes that contribute to leakage current when the switches are on. The on leakage current is expected to differ slightly from that discussed in section 3.2.1 due to the changing voltage across the added diodes; D4 in DC2, and D6 in SC2. D4 is from the HVPMOS cascode device used in the pull up current for turn on of switch topology DC2, and D6 is from the pull down current at turn on of SC2.
For switch topology DC2, D1 and D2 leakage current is provided by the maxer. At low T1 (and DP) voltage, there is a large reverse bias on diode D4 and small voltage across D3. This leads to leakage current flowing out of T1. As T1 voltage increases, the reverse bias on D4 reduces and D3 leakage is provided by the terminals.

Similar behavior is expected in SC2 since the structure of diodes when the switch is on is very similar to that in switch topology DC2.

Results for the simulated on leakage are shown in figure 7-8 below.

The results show that the trends of the simulated on leakage current at room temperature are similar to what was expected. Leakage current is significantly higher at higher temperatures, where it can also be noted that SC1, DC2 and SC2 measured currents no longer cross the x-axis. SC1 current stays positive, suggesting that diode D5, from the HVPMOS cascode pull up current source, dominates over the body-substrate diodes D3 and D4 at high temperature. DC2 and SC2 simulated leakage current remains negative when hot, suggesting that the HVPMOS devices have higher leakage current than the HVNMOS devices at high temperature.

### 7.2.2 Off leakage

As shown in figure 7-9, the diodes added from turn on pull up/down are connected directly between VP and VM when the switch is off, and so the results are still expected to follow the behavior discussed in section 3.2.2.

The results in figure 7-10 show that as expected, at room temperature, the leakage current of switch topology DC2 is very low and fairly constant throughout the range of terminal voltages. It is also significantly lower than that simulated for all other switch topologies at all temperatures. Also as expected, the leakage currents of SC1 and SC2 are very similar.

### 7.3 Charge conservation

The test used to simulate the charge relationship with slew rate is shown in figure 7-11 below. At each slew rate, the input voltage T1 is ramped from VM to VP and, to
Figure 7-8: On leakage current over temperature test
calculate the input charge, the input current was copied using an LTSpice behavioral current source (B2 in fig. 7-11), and integrated over a capacitor. The capacitor voltage was then measured after the slew transient and the input charge calculated as:

\[ Q_{in} = C_{int} \times V(qin) \]  

(7.2)

After the measurement of input charge for the rising slew, the integrating capacitor was discharged through the resistor and switch, and then used to integrate the input charge over the falling slew. The output charge at the capacitive load, and the charge lost to the substrate from P1 and P2 vertical PNPs were calculated in the same manner.

From figure 7-13c, we see that up to 14% of input charge is lost to the substrate in switch topology SC1 during fast falling slew conditions. In both rising and falling slew, the versions with maxers are seen to have significantly less charge lost to the substrate than the versions without maxers.

Figure 7-12c shows that, in switch topology SC1, up to 54% of charge lost in the switch was lost to the substrate. Whereas with the maxer in topology SC2, a
Figure 7-10: Off leakage current over temperature test
maximum of 8% of charge loss is through the vertical PNPs of P1 and P2, in the range of slew rates covered in this document.

For the drain coupled switch topologies, the highest percentage of charge loss that is due to the vertical PNPs in P1 and P2 goes from 26% in DC1 to 0.4% in DC2 by adding the maxers.

DC2 shows the best charge conservation behavior over slew rate. However, it also has the highest input charge at low slew rate. This is due to the high capacitance of the switch. This topology has two maxers and because of the large capacitance of the two extended drains at node DP, large feed-forward capacitors were needed to support the source followers at the maxer inputs from the drain side. The use of two maxers is thus one of the main contributors to this topology's high switch capacitance. DC1 has the second highest capacitance, followed by SC2 and finally SC1 has the lowest switch capacitance due to its lack of maxers and its simple VGS generator design.

### 7.4 Charge vs step size

At a given slew rate, the amount of charge needed by a capacitor depends on the step size of the charging voltage source \( \Delta Q = C \times \Delta V \). Thus the amount of input charge is linear with step size for a capacitor. Measuring the input charge to the switch with changing step size tells us whether the switch has capacitive behavior, and the value...
(a) Input charge

(b) Vertical PNP charge

(c) Percentage charge lost to substrate

Figure 7-12: Charge conservation at rising slew
Figure 7-13: Charge conservation at falling slew
of the switch capacitance is given by the slope of the graph.

For this test, T2 was loaded with a small capacitor, and T1 voltage stepped. The setup is the same as that used for the charge conservation test, and uses the same integration method to measure input and substrate charge.

Figure 7-14 shows the results for switch input charge vs step size for each switch topology, for both rising and falling slew.

From these results, it can be observed that the switches all behave approximately linearly for both rising and falling slew. With the same load capacitance used for each switch in this test, the slopes are thus representative of each switch’s effective capacitance. $C_{sw} = \frac{\Delta Q_{in}}{\Delta V} - C_{load}$. DC2 thus has the highest capacitance, DC1 and SC2 have about the same, and finally SC1 has the lowest capacitance. This matches the results seen from the charge conservation plots.

### 7.5 Charge injection

As previously discussed, turn off charge injection is an important switch parameter and thus must be simulated. T2 is capacitively loaded, and the switch toggled from on to off. The voltage at T2 is measured before turn off, and then again after complete turn off. The turn off charge injection is then given by $Q_{inj} = C_{load} \times \Delta V T2$.

The plot in figure 7-15 below shows the measured charge injection at different T1 voltages.

From the results in figure 7-15, it can be seen that the drain coupled switch topologies have lower charge injection than the source coupled ones, as was discussed in chapter 5.

DC2 has low constant charge injection across the range of terminal voltages, due to the small constant reverse bias on the drain-body diodes in P1 and P2, created by the maxer. This behavior is also as expected.

DC1 charge injection is seen to cross the x-axis when the effect of drain pull down outweighs that of gate pull up at switch turn off.
Figure 7-14: Charge vs step size
7.6 Insertion loss

The insertion loss of the switch was simulated in LTSpice using an AC source at T1, and measuring the response at T2. Insertion loss is the attenuation in signal power resulting from insertion of a component into a circuit. It is calculated as:

\[ 20 \log \frac{V_{out \text{ with switch}}}{V_{out \text{ without switch}}} \]  

(7.3)

The test setup and results are shown in figure 7-16 below. 50Ω termination resistors were used.

From the plots, we see that DC2 has a significantly lower -3dB bandwidth (100MHz), which corresponds to its high switch capacitance. All other switches have -3dB points above 1GHz.

The -3dB bandwidth of the switches is affected by the switch capacitance, leading to lowest bandwidth (100MHz) in switch topology DC2, and highest bandwidth in SC1, in the same order as the capacitance derived from the charge conservation and charge vs. step size results.
7.7 Off Isolation

When the switch is off, it is desirable that any AC signal at one terminal does not couple to the other, allowing sufficient isolation between different circuits.

The test setup and results are shown in figure 7-17. With the switch turned off, an AC signal is applied at terminal T1 and the response at T2 measured.

DC2 shows the best isolation throughout the frequency range shown, with -60dB being its worst case. SC1 has the lowest low frequency isolation. Isolation decreases with frequency due to the influence of parasitic parallel capacitors.[2]
Figure 7-17: Isolation
7.8 Overall comparison

Table 7.1 shows a numeric comparison of the four switch topologies in terms of the characteristics discussed in this document.

<table>
<thead>
<tr>
<th></th>
<th>DC1</th>
<th>DC2</th>
<th>SC1</th>
<th>SC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ON}(\Omega)$ room temp, VT1=75</td>
<td>190.5</td>
<td>200.6</td>
<td>192.3</td>
<td>227.2</td>
</tr>
<tr>
<td>On leakage (pA), room temp, VT1=75</td>
<td>306.5</td>
<td>-141.4</td>
<td>-50.7</td>
<td>-117.0</td>
</tr>
<tr>
<td>Off leakage (pA), room temp, VT1=75</td>
<td>239.6</td>
<td>-6.9</td>
<td>-159.1</td>
<td>-157.6</td>
</tr>
<tr>
<td>Vertical PNP charge at 1000V/µs</td>
<td>391.2</td>
<td>18.6</td>
<td>366.8</td>
<td>146.7</td>
</tr>
<tr>
<td>Effective switch capacitance (pF)</td>
<td>9.2</td>
<td>34.4</td>
<td>1.7</td>
<td>9.1</td>
</tr>
<tr>
<td>Charge injection (pC), VT1=75</td>
<td>-14.8</td>
<td>14.1</td>
<td>191.8</td>
<td>185.4</td>
</tr>
<tr>
<td>Isolation at 10kHz (dB)</td>
<td>-207</td>
<td>-236</td>
<td>-147</td>
<td>-200</td>
</tr>
</tbody>
</table>

Table 7.1: Numeric comparison table.

7.9 Conclusion

Overall, the topologies are all good switch design options, each with its advantages and weak points. The drain coupled switch with maxer, DC2, shows great off leakage behavior, low charge injection, and very low vertical PNP charge loss. However, this came at the cost of increased switch capacitance. The source coupled switch with maxer, SC2, showed good current limiting behavior, and lower switch capacitance than DC2. From the simulation results presented, depending on the application a switch topology can be selected for further development, fabrication in silicon, and testing.

7.10 Future work

7.10.1 VGS generators

Since the drain coupled switch VGS generator depends on the voltage drop across a resistor, the current through the resistor needs to be well controlled. If this current increases with temperature, the main switch gate overdrive voltages will also
increase with temperature. This is undesirable as it would lead to a higher current limit at higher temperature, leading to possible thermal run-away issues. It would thus be desirable that the current that supplies the resistor has a negative temperature coefficient decreasing as temperature increases. For example, a current that is complimentary to absolute temperature (CTAT).

A CTAT current source can be achieved if a current that is proportional to absolute temperature (PTAT) is available. PTAT current sources are commonly generated in a bandgap circuit.

If IRTP is the desired current at room temperature, IPTAT is the PTAT current (equal to the desired current at room temperature), then the CTAT current can be achieved as shown in the equation below:

\[
ICTAT = 2 \cdot IRTP - IPTAT
\] (7.4)

Figure 7-18 shows one way this could be implemented, with the load resistor's current being complimentary to absolute temperature.

This method requires a lot of current and thus was not immediately implemented in the switch topologies. For future work, this idea would need to be improved, or a different method considered.

Additionally, current limiting would need to be implemented in the SCI VGS generator. And the current limit in switch topologies DC1 and SC1 should both be set to 7mA to prevent vertical PNP turn on.

7.10.2 Alternative slew boost

An alternative method for boosting the current in a source follower during slew is shown in figure 7-19. This method would use a feed-forward capacitor and resistor in series to create the \( V_{GS} \) needed to turn on a low voltage NMOS device, I19, which would then provide the extra current needed during rising slew of node VIN. This would prevent forward biasing of the protection diode I11 on the HVPMOS device U1, and provide current to maintain the \( V_{SG} \) of U1 during slew.
This method has the advantage of requiring a smaller capacitor than that needed in the simple capacitor feed-forward method used so far. This would help in reducing the total switch capacitance, which would in turn increase the bandwidth of the switches, and reduce the amount of charge required by the switches during slew.

The desired behavior is that the low voltage NMOS device, I19, is off in DC conditions, and otherwise sources current proportional to the slew rate of node VIN. However, since the device current is dependent on the square of the gate overdrive voltage, a directly proportional relationship between slew rate and current is not possible. Alternatively, a threshold slew rate could be set, such that I19 is off at lower slew rates, and turned fully on for slew rates higher than the threshold.

However, in order to implement this, a lot of care has to be taken with the choice of the resistor value, and especially with the biasing of the source of I19. At DC, the gate of I19 is at VP and thus its source should be at about one threshold voltage below VP so that the device is easily and quickly turned on. The low voltage PMOS
device, I16 is used to control the voltage at the source of I19.

This method was not used in the current switch designs because the device biasing is not easily implemented and would require care to ensure good device matching between the boost devices and the biasing devices, so that the slew boost circuit is not "on" in DC conditions, which would lead to increase in DC power dissipation. This method also does not scale with load capacitance as easily as the simple feed-forward capacitor method that was implemented. And given the large number of fast slewing nodes in each switch, this method would have to be used with many source followers, and a different bias set for each one, given the different load capacitances and current requirements.

7.10.3 Multiplexer

Having completed the improvements in the switch designs, one topology would be selected to be used in the design of a multiplexer. Break before make circuitry would
be added to control switch turn on and ensure that no two switches were on at the same time. Since switch turn on is controlled by low voltage signals, the break before make control would simply be implemented with digital logic gates, relying on a logic signal from the switches to indicate whether they were on or off.
Appendix A

Vertical PNP model

The available SPICE model for the HVPMOS device did not include a model for the vertical PNP device to the substrate. The first step in assessing the effect of the vertical PNP on charge conservation was to add a behavioral model that would show the effect of the vertical PNP on the switch behavior. This was accomplished using behavioral current sources in LTSpice to create a lookup table to match the drain to body voltage and give a substrate current equal to what is seen in the measured lab data.

An additional step in modeling the vertical PNP device was to de-embed the drain-body diode which came included in the HVPMOS device model. Since this diode is part of the vertical PNP, the diode and the base-emitter junction of vertical PNP would be in parallel if not de-embedded. Its model is copied to a new diode. The drain-body voltage is copied by an LTspice behavioral voltage source and applied to the terminals of the new diode. The current in the diode is then copied and injected back into the drain, essentially undoing the effect of the drain to body diode in the device model.

The figure below shows the circuit of behavioral components used to create this model for the vertical PNP device.

Due to the limited number of data points each behavioral current source can take, they were placed in parallel to include all the measured lab data. The substrate current was then measured in the resistor rsub1 and using the behavioral current
source SUB1, this current was scaled and sunk to the substrate.

Figure A-1: Vertical PNP behavioral model
Bibliography


