

Characterizing Dielectric Materials with a Feedback-Based Model

by

Michelle Rybak

Submitted to the Department of Electrical Engineering and Computer Science

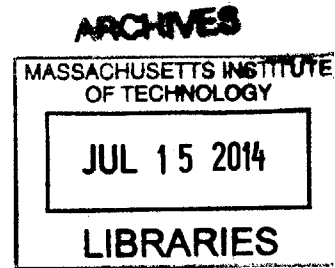
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**General Thesis Release Letter and Classification Review Letter
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Subject: Master of Engineering Thesis of Michelle Rybak

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Abstract

As signal frequencies continue to increase, conductor surface roughness losses of interconnects are becoming more prominent. There is currently no industry standard for separating the dielectric and conductor losses that appear in PCBs. As part of the thesis work, test vehicles composed of six different dielectric materials were fabricated with different trace widths, copper foil profiles, and oxide surface treatments. A Feedback-Based Model was used to simulate and extract the dielectric and conductor losses from measurements made with the different test vehicles. Simulation software such as MATLAB, Agilent ADS, and Polar Si9000 were utilized. Dielectric material Megtron 4 had the lowest Df of the materials of interest. The Feedback Based Model was able to fit the data well for either low frequencies and high frequencies, but not both. Further, the model was able to model the effects of changes in copper roughness well. Small variations were seen in the extracted Df associated with changes in width of the measurement traces.

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Contents

1	Introduction	9
1.1	Background	10
1.2	Motivations for Dielectric and Copper Roughness Loss Consideration	10
1.3	Objective	11
2	Theoretical Basis	12
2.1	Mechanisms of Dielectric and Conductor Loss	12
2.1.1	Skin Effect	12
2.1.2	Copper Roughness and Oxide Treatments	13
2.2	Dissipation Factor	14
2.3	Scattering Parameters	16
2.4	Calibration of the Vector Network Analyzer	19
2.5	Dielectric Characterization Methods	22
2.5.1	Comparison of Popular Methods	22
3	Technical Approach	25
3.1	Materials Considered	25
3.2	Feedback Based Method of Loss Characterization	27
3.2.1	Mathematical Approximation of Insertion Loss	27
3.2.2	Test Vehicle Design	28
4	Required Resources	36
4.1	Hardware Resources	36

4.2	Software Resources	36
4.3	Information Resources	37
5	Results	38
5.1	Insertion Loss Comparison	38
5.2	Extracted Dk and Df for Each Material	40
5.3	Modeling Copper Foil and Oxide Surface Treatment	44
5.4	Modeling Effects of Width Variation	47
6	Discussion and Future Work	50

List of Figures

1-1	Typical inner layer trace with surface roughness [6]	11
2-1	Illustration of the skin effect	13
2-2	Multilevel hemispherical model of surface roughness	14
2-3	2-Port Scattering Parameters	16
2-4	Sample 2-Port scattering parameters for 16" transmission line	17
2-5	Insertion loss plotted on a log-log scale with reference lines of slopes 1/2 and 1	18
2-6	Decomposing total insertion loss into dielectric loss and and conductor loss for FR-4 [10]	19
2-7	Plots for Calibration Verification with Through Trace	21
3-1	Cross section of general test vehicle stackup	30
3-2	Cross section of stackup sections	31
3-3	Signal layers of test vehicle	31
3-4	Panel Design	33
5-1	Insertion loss of materials examined for this thesis work	39
5-2	High Fit Modeling S_{21} and Dk_{eff} in Agilent ADS	40
5-3	Extracted Dk and Df for High Fit Modeling	41
5-4	Low Fit Modeling S_{21} and Dk_{eff} in Agilent ADS	42
5-5	Extracted Dk and Df for Low Fit Modeling	43
5-6	Effect of foil type on oxide induced losses from section 1 traces in I- Speed IS, RTF test vehicles and NPLDII, VLP test vehicles	44

5-7	Increasing R_q and increasing $Df(f)$ to model increase in roughness for NPG-170D	46
5-8	Extracted $Dk(f)$ and $Df(f)$ for each section	47

List of Tables

3.1	Df Values for Materials	26
3.2	Panel Identification	34
3.3	Roughness information provided from each vendor	35
5.1	Changes in roughness parameters for foil types of each material . . .	45
5.2	Widths of measurement traces in each section	47

Chapter 1

Introduction

As signal frequencies reach the 10+ GHz range, signal integrity problems are becoming more persistent in modern technologies. One such problem is signal loss. Signal loss is the decrease in power a signal undergoes as it travels through different components and interconnects. In printed circuit boards (PCBs), signal loss can be attributed to both resistive loss in the conductors as well as dielectric loss. In the past, differentiating between and accurately estimating these losses has not been crucial for maintaining signal fidelity. However, the combination of these losses observed in common and cheap PCB materials at high frequencies is now too large to ignore. The intent of my work is to determine for a variety of materials how to properly characterize and approximate the dielectric loss and differentiate it from conductor loss.

Chapter 1 will provide the objective and motivations for this thesis work. Chapter 2 will give a summary of the theoretical knowledge necessary to understand the topics discussed. Chapter 3 will discuss the technical approach taken to investigate the types of losses that arise at high frequencies. Chapter 4 outlines the resources used for this thesis work. Chapter 5 outlines the results and Chapter 6 discusses the results as well as potential future work.

1.1 Background

Not all dielectric materials are created equal and selecting an appropriate material can be a challenging task. High-speed digital designers must always consider the trade off between performance and cost. The performance of a dielectric can be characterized by the expected loss. Choosing a dielectric material which meets the performance specifications of an application requires an accurate understanding of the dielectric loss expected across a range of frequencies.

1.2 Motivations for Dielectric and Copper Roughness Loss Consideration

Material vendors will often provide values for dielectric loss, but these values have proven to be unreliable. Loss values are provided at single frequency points, when applications typically operate at a range of frequencies. Further, with clock frequencies constantly climbing, previous methods of modeling and extracting loss parameters are no longer accurate. This is largely due to the surface roughness of copper traces. Copper traces are intentionally not perfectly smooth, as seen in Figure 1-1. This serves to promote adhesion between the copper and the surrounding dielectric. Surface roughness will disturb the current flow in interconnects. This disturbance is enhanced at higher frequencies due to the skin effect. As a result of this phenomenon, the current density becomes larger closer to the surface as the frequency of the signal increases. The skin effect in smooth conductors is a well understood phenomenon and can be readily modeled. However, when the surface is roughened, the calculations for dielectric loss can be skewed as a result of the poorly understood effects of surface roughness.

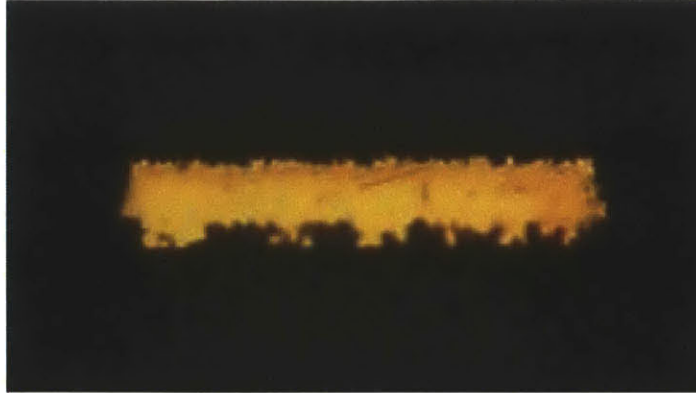


Figure 1-1: Typical inner layer trace with surface roughness [6]

There are many methods used in the industry to calculate dielectric loss. In the past it has been sufficient to assume the conductor is smooth, since frequencies were not high enough for roughness to affect the loss measurement. This assumption is no longer adequate; It is now imperative to find a new way to calculate dielectric and conductor losses.

1.3 Objective

The objective of this thesis is to select and implement an appropriate characterization method and use it to investigate the dielectric losses of several materials. As part of the thesis work, the different popular methods of calculating dielectric loss are explored and a feedback-based method is selected for analysis. In order to investigate the accuracy of the feedback-based model, the following factors are varied between test vehicles:

- trace width
- oxide surface treatment
- copper foil type

Moderately priced low loss materials are of particular interest for investigation. Six potential materials are chosen and their loss properties are extracted and compared.

Chapter 2

Theoretical Basis

As part of the thesis work it is imperative to understand the physical meaning of the many parameters used to characterize dielectric materials. Similarly, understanding how these parameters are calculated and related to each other is necessary to ultimately be able to extract and analyze the dielectric loss. Furthermore, it is important to understand the theory behind calibration of a vector network analyzer in order to properly dimension traces on test vehicles and perform the necessary measurement calibration. Finally, a summary of the current popular methods for dielectric characterization was provided.

2.1 Mechanisms of Dielectric and Conductor Loss

2.1.1 Skin Effect

Conductors have both a DC and an AC component to their resistance. The AC component is associated with skin effect losses. The skin effect describes the tendency of current density to be concentrated near the surface of the conductor as frequency increases. The width of the conductor through which the current flows is called the skin depth. This effect is illustrated in Figure 2-1 and described in Equation 2.1.

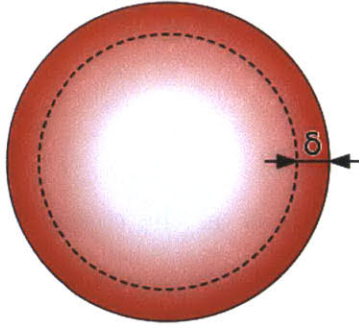


Figure 2-1: Illustration of the skin effect

$$\delta = \sqrt{\frac{2}{\sigma\mu\omega}} \quad (2.1)$$

δ is the skin depth in meters

σ is the conductivity of the conductor in $\frac{\Omega}{m}$

ω is the angular frequency of the current in the conductor in $\frac{rad}{s}$

2.1.2 Copper Roughness and Oxide Treatments

PCBs are composed of copper foil layers and dielectric layers. Copper foil is used for the interconnects, power, and ground planes, while dielectric layers provide insulation. The surface of the copper is roughened to ensure adhesion between the separate layers. This roughness often leads to increased conductor losses at high frequencies. Depending on the application, copper foils of different profiles will be used. High profile copper foils will have a larger roughness profile, allowing for better adhesion. Conversely, low profile copper will have smaller roughness profiles and will incur lower losses at high frequencies.

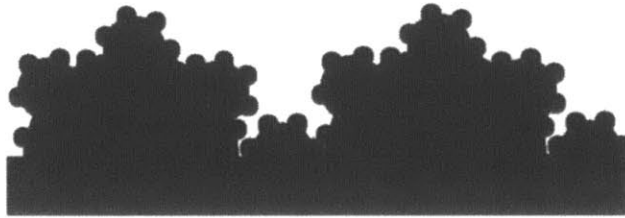
One method of promoting adhesion between the dielectric layers and the copper foil is surface treatment. The classic surface treatment is called "Reduced Oxide," and functions by introducing a thin layer of cupric oxide on the surface of the copper. However, because this method is hard to automate, the industry has turned to "Oxide Alternatives" in recent years. These function by selectively corroding the copper surface to create peaks and valleys. These peaks and valleys promote adhesion between

the foil and dielectric.

Copper Roughness Model

Accurate modeling of the roughness on the copper surface of the conductors is an active field of study. The copper roughness model used in this research is the Multi-level Hemispherical Model. The motivation for using levels of hemispheres to model the roughness comes from Scanning Electron Microscopy photos of rough copper that contain multiple levels of surface protrusions. The inputs to this model are the roughness amplitude, distance between peaks, and the size of the hemisphere base. All of these parameters are RMS values. The RMS amplitude of the roughness is typically provided by the vendor, while distance between peaks and base length require Scanning Electron Microscopy and Atomic Force Microscopy. [4]

Figure 2-2: Multilevel hemispherical model of surface roughness



2.2 Dissipation Factor

The most common method of quantifying dielectric loss is the Dissipation Factor (Df). The Df of a material is closely related to its complex electric permittivity. In general, the electric permittivity describes a material's ability to transmit, or permit, an electric field. The electric permittivity is a complex function of the frequency of the applied field and follows the form of Equation 2.2.

$$\epsilon(\omega) = \epsilon'(\omega) + j\epsilon''(\omega) \tag{2.2}$$

ϵ' is the real part of the permittivity and is related to the stored energy in the medium.

ϵ'' is the imaginary part of the permittivity and is related to the loss of energy in the medium. Df is then the ratio of the real and imaginary parts of the complex permittivity.

$$Df = \frac{\epsilon''(\omega)}{\epsilon'(\omega)} \quad (2.3)$$

Physically, this ratio is the resistive (lossy) component of the E-field to the reactive (lossless) component of the E-Field. This term describes a dielectric's inherent dissipation of electromagnetic energy.

Svensson Djordjevic Approximation of the Wideband Debye Model for Dielectric Loss

In this thesis work, both Dk and Df as a function of frequency were modeled using the Svensson-Djordjevic approximation. The equations that govern this model are presented in equations 2.4 and 2.5. [1]

$$Dk(f) = \epsilon'_{\infty} + \frac{\Delta\epsilon'}{\log f_2 - \log f_1} (\log f_2 - \log f) \quad (2.4)$$

$$Df(f) = \frac{-0.682}{Dk(f)} \frac{\Delta\epsilon'}{\log f_2 - \log f_1} \quad (2.5)$$

ϵ'_{∞} the real part of the relative electric permittivity at high frequencies

$\Delta\epsilon'$ the change in real part of the relative electric permittivity

f_1 minimum frequency for model

f_2 maximum frequency for model

ϵ'_{∞} and $\Delta\epsilon'$ are unknowns but they can be solved for if Dk and Df are known at a specific frequency. Material vendors will provide Dk and Df values at particular frequencies. However, these values are considered untrustworthy and are not used when simulating interconnects in this work.

2.3 Scattering Parameters

There are many methods of quantitatively characterizing interconnects. One such method is generating Scattering Parameters, or S-parameters. The 2x2 S-Parameter matrix for an interconnect describes the relationship between the incident power wave and the reflected power wave as shown in Figure 2-3 and Equation 2.6. [3]

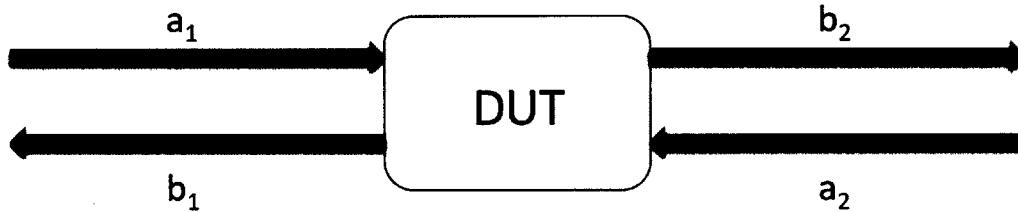


Figure 2-3: 2-Port Scattering Parameters

$$\begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \quad (2.6)$$

In an ideal conductor the S-parameters matrix can be simplified by invoking symmetry, namely, $S_{21} = S_{12}$. The term "Insertion Loss (IL)" is used to quantify the loss of signal power as the signal travels down the transmission line. IL is defined as follows:

$$\text{IL(dB)} = -20 \log_{10} |S_{21}| \text{ or } \text{IL(dB)} = -20 \log_{10} |S_{12}| \quad (2.7)$$

Sample 2 port S-parameters for a 16 inch 50Ω transmission line are displayed in Figure 2-4. S_{12} and S_{21} lie directly on top of one another as predicted by symmetry.

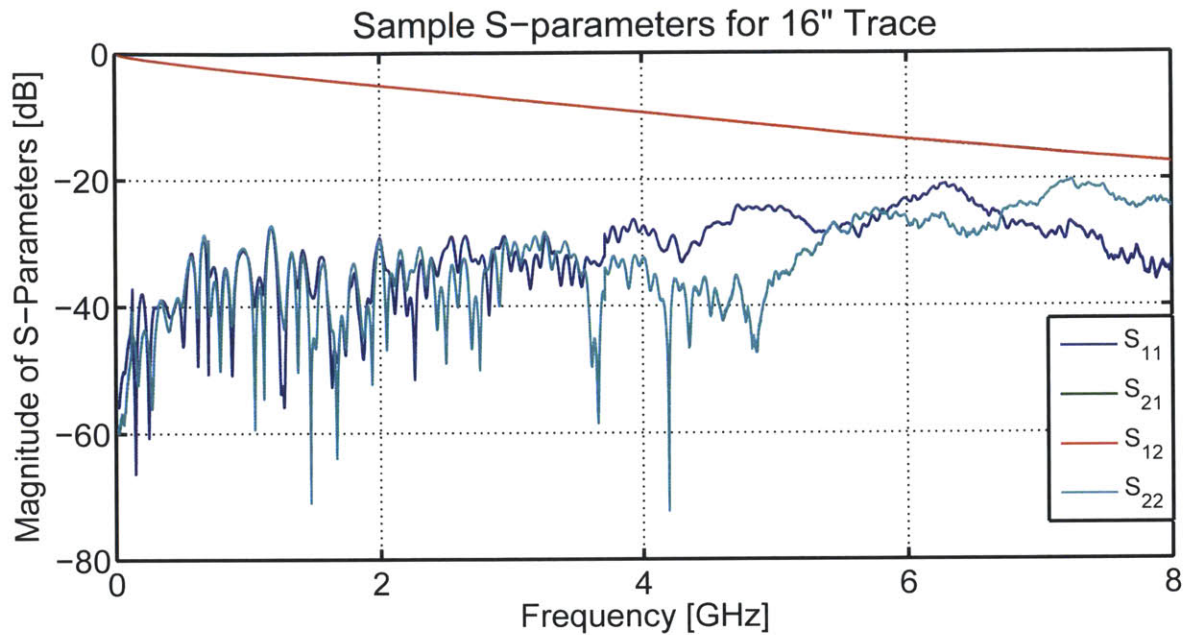


Figure 2-4: Sample 2-Port scattering parameters for 16" transmission line

An examination of the insertion loss can provide a preliminary understanding of a material's performance. One way to understand the insertion loss of an interconnect is to investigate the frequency dependence at low and high frequencies. At low frequencies, the insertion loss varies with the square root of frequency, while at high frequencies it varies linearly with frequency. This can be seen when insertion loss is plotted on a log-log scale as in Figure 2-5.

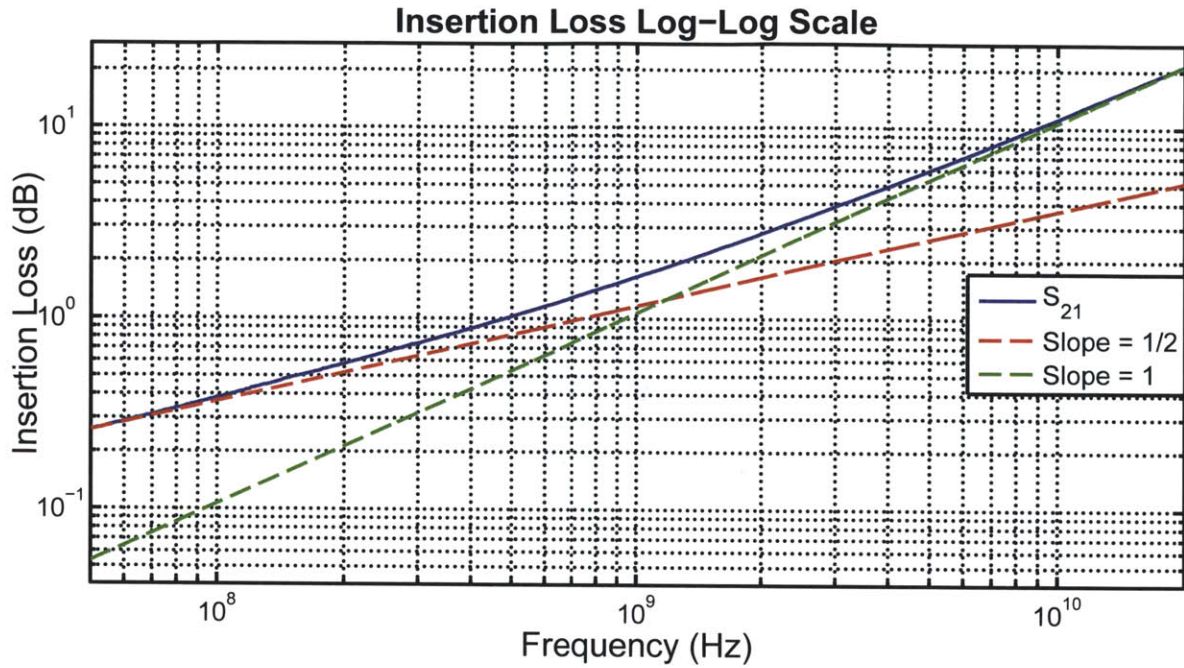


Figure 2-5: Insertion loss plotted on a log-log scale with reference lines of slopes 1/2 and 1

At low frequencies, the insertion loss is dominated by conductor losses due to the skin effect, which varies with the square root of frequency. At high frequencies, the insertion loss is dominated by dielectric losses due to imperfections in the dielectric materials.

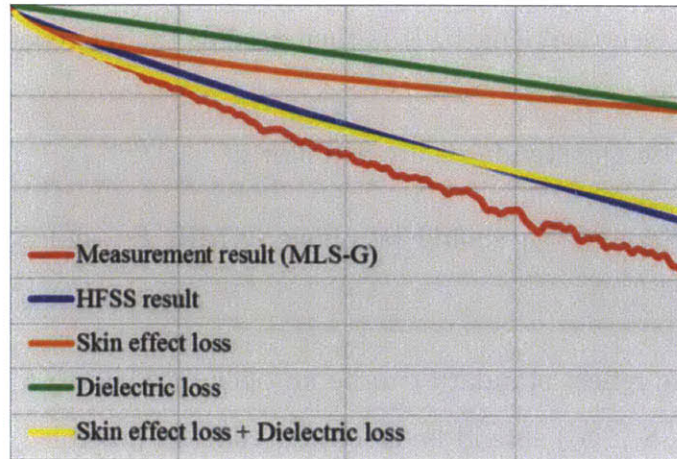


Figure 2-6: Decomposing total insertion loss into dielectric loss and and conductor loss for FR-4 [10]

The effect of the copper roughness on the traces can be seen in the insertion loss measurements in Figure 2-6. These measurements are from Taka-aki Okubo's Designcon 2014 presentation "Reducing Signal Transmission Loss by Low Surface Roughness". In this figure, the dielectric loss and conductor loss and the total loss are measured using ANSYS HFSS simulation software. Yet the simulated loss does not match the measured loss. The resulting difference is attributed to the losses that arise due to the roughness of the copper traces.

2.4 Calibration of the Vector Network Analyzer

S-Parameter measurements are taken with a Vector Network Analyzer (VNA). For most applications, standard calibration kits are available to achieve the necessary level of precision. However, in this thesis work, each test vehicle incorporated independent auxiliary calibration traces allowing for a more accurate calibration.

The calibration type implemented in this work is the Thru-Reflect-Line (TRL) calibration. Like other calibration methods, TRL calculates a 12-term error correction vector at each frequency point. To calculate these terms, standards for which the S-parameters are known are measured. These standards include a "Thru" standard, a "Reflect" standard, and four delay lines of varying length. By definition, the thru

standard has zero electrical length. It is then used as the reference length for each of the delay lines.

Requirements for the standards are as follows:

- Through - S_{12} and S_{21} should be above -0.1dB. S_{11} and S_{22} should be below -30dB.
- Reflect - The reflect standard can be an open or a short. S_{12} , S_{21} must be less than -30dB. S_{11} , S_{22} should be as close to 0dB as possible.
- Delay lines - The S_{12} differential phase of each delay line has to be from 20° - 160° with reference to the thru. The 20° and 160° points correspond to the frequency range for which that standard is defined. The frequency ranges for each line should overlap to ultimately cover the desired 50 MHz to 20GHz range.

The accuracy of the resulting TRL calibration for the test vehicle can be verified by assessing the S-parameters and the Smith Chart of the through and/or the reflect standards. The magnitude of the S-parameters should meet the requirements outlined above. A sample ideal calibration is presented in Figure 2-7. It should be noted that the calibration measurements are extremely sensitive. Slightly loose SMA connectors can cause large inaccuracies in a calibration. Similarly, delays of the four delay lines should not only be estimated but also measured before inputting into the calibration definition in order to ensure calibration accuracy. Since the calibration is very sensitive, it is very useful to have this check to ensure the quality of each measurement made.

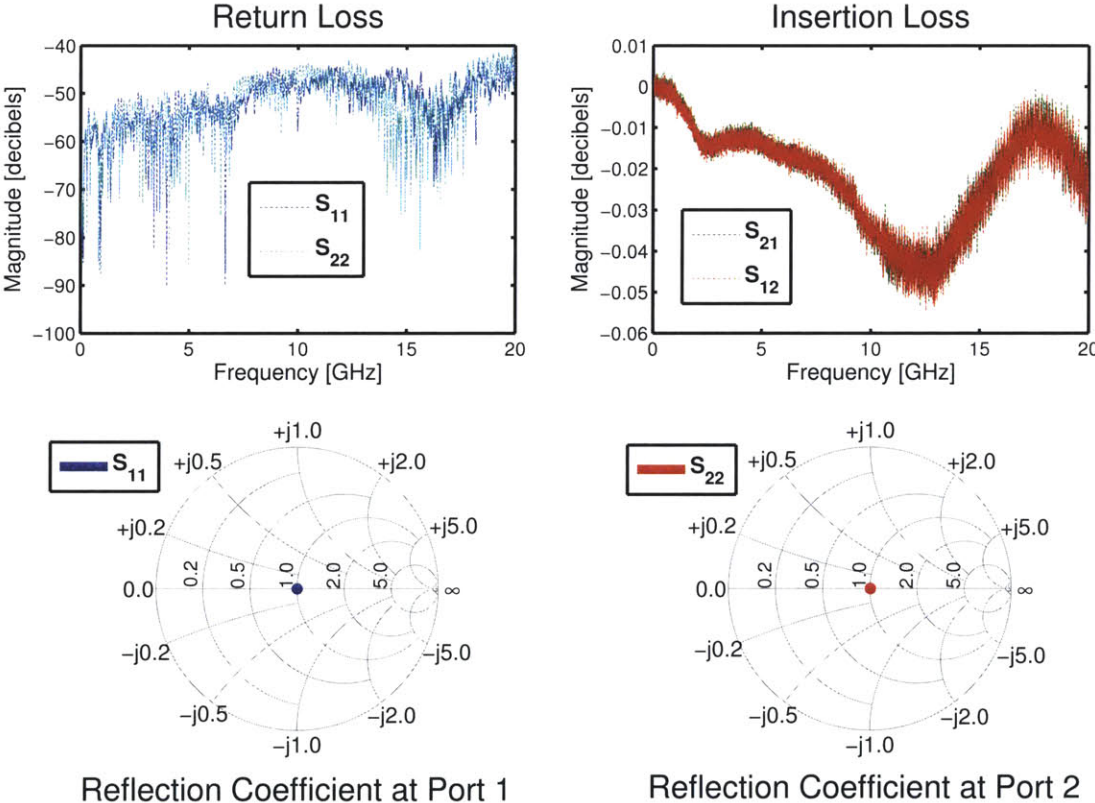


Figure 2-7: Plots for Calibration Verification with Through Trace

2.5 Dielectric Characterization Methods

Frequencies of high speed digital circuits have only recently become high enough to require surface roughness effects to be considered in the design process. Because of this, there is currently no single industry standard for a dielectric loss characterization method that takes into account the surface roughness. Below is a discussion of the methods currently popular in the industry.

2.5.1 Comparison of Popular Methods

Many characterization methods were taken into consideration before selecting chosen method in this thesis work. These methods include IPC standards such as IPC Stripline (IPC-2.5.5.5) and Split Cylinder Resonator (IPC 2.5.5.13). Other popular methods include Bereskin Stripline, SET2DIL, SPP, S3, and the Feedback Based Design Method. The pros and cons of each were considered and are discussed below.

Cavity Resonator Methods

IPC Stripline, Split Cylinder Resonator, and Bereskin Stripline all fall in the category of Cavity Resonator Methods. These function similarly by exciting and detecting fundamental resonant modes, and using the value of the resonant frequency to calculate the quality factor of the resonator. The dissipation factor can then be derived from the quality factor. The way these methods differ is how the method used to create resonance. In the Split Cylinder Resonator, a cylindrical cavity is split into 2 halves with a dielectric in the gap and the resonant modes are created by introducing a coupling loop. In the IPC Stripline method, a stripline resonator is created between the resonant element pattern cards and the ground planes. In the Bereskin Stripline method, a signal source is used to excite oscillations in an isolated stripline element. [2, 13, 12]

A limitation of these cavity resonator methods is that D_f can only be calculated at the discrete frequencies of the resonant modes. As a result, these cavity resonator methods do not provide D_f data over an entire range of frequencies. To get D_f

information for the entire range, the data is often interpolated between resonant frequencies. This introduces some uncertainty to the results.

In addition, the calculated dissipation factor does not necessarily correspond to those measured in actual PCB test data. In the IPC test method the following is stated: "...users are cautioned against assuming the method yields permittivity and loss tangent values that directly correspond to applications." [13] Df values produced by the Bereskin Stripline method have correlated closely with those produced from actual PCB test data. However Df values of the Split Cylinder Resonator method were 20-30% lower than those produced with the Bereskin Stripline method. This discrepancy indicates that the Split Cylinder Resonator method is less trustworthy. [11]

Another shortcoming of these cavity resonator methods is the effects of copper roughness are not factored into the Df calculations. An important step in the calculation of Df is differentiating between the loss due to the conductor and the loss due to the dielectric. In both these methods, conductor loss is calculated entirely from stripline geometry. This calculation would be accurate if the conductor was perfectly smooth. However, as previously discussed it is not. The contribution to the attenuation from the copper roughness is therefore factored in as dielectric loss, leading to a Df that is higher than the value reported on the vendor datasheet.

SET2DIL

Another popular method frequently used by material vendors is SET2DIL, which stands for Single Ended TDR/TDT to Differential Insertion Loss. As the name indicates, the method produces differential insertion loss measurements from simple test vehicles containing single ended transmission lines. The disadvantage of this method is that the product is insertion loss, which includes the loss of both the conductor and the dielectric. Therefore, this method provides information about the conductor and dielectric together, but does not attempt to separate conductor and dielectric losses. [9]

S3

A popular method which explicitly considers the conductor roughness effects is the Stripline S-Parameter Sweep, or S3, method. The S3 method features a test vehicle containing 16 inch 50Ω striplines between the dielectric material of interest. S-parameters of this stripline are measured and fed into the S3 algorithm. The algorithm uses transmission line theory to calculate the total attenuation from the S-parameters. Separately, α_c is calculated as the sum of the contribution from a smooth conductor and the contribution from the surface roughness. An appealing advantage to this method is that the surface roughness contribution can be calculated in a variety of ways depending on the capabilities of the user.

The main shortcoming of this method is that the loss contribution from the surface roughness must be approximated from micrographs or scanning electron microscopy (SEM) images of trace surfaces or cross-sections. [7] Practically speaking, this information is often inaccessible or too costly to obtain. Ideally, a dielectric characterization method would be able to simulate the performance of a material with the information and parameters readily available from material and PCB fabrication vendors.

Feedback Based Method

The method chosen for further exploration in this thesis is a feedback based method as proposed at DesignCon 2013 by Eric Bogatin, Don DeGroot, Paul Huray, and Yuriy Shlepnev. Rather than take measurements and extract the parameters, this method estimates a set of parameters which, when used as inputs to models for dielectric and conductor losses, matches the measured S-parameters.[8]

This method is attractive because it does not require complex analysis or approximation of the physical attributes of the roughness profile. Rather it only requires a simple test vehicle and information that the material vendor can provide.

Chapter 3

Technical Approach

The technical approach was focused on accomplishing the following two goals:

1. Gather a breadth of knowledge regarding the current low loss dielectric materials available in order to make an educated recommendation for a future data server product.
2. Study the Feedback Based Method of dielectric characterization and assess its efficacy in simulating interconnects over the frequency range of 50 MHz - 20 GHz

3.1 Materials Considered

The dielectric materials considered were chosen based on their loss properties and their cost. There exists dielectric materials with Df values so low that loss would no longer be a concern, however they are costly in comparison to those examined in this thesis work. The challenge is to find the material with the lowest Df that is cost competitive.

Six dielectric materials in total were chosen for this research. Five of the six materials met the cost requirement and were advertised as having low enough Df values for the target application. The sixth material, Megtron 6, is costly in comparison to the others, however it had better performance. It was therefore intriguing and deserved

closer inspection.

Table 3.1: Df Values for Materials

Material	Test Method	Typical Df	Resin Content	Frequency
NPLDII	-	0.006	-	1 GHz
NPLDII	S3	0.0112	50%	-
NPG-170D	-	0.005	-	1 GHz
Isola I-speed IS	Bereskin Stripline	0.006	56%	2 GHz
Isola I-speed IS	Bereskin Stripline	0.0071	56%	10 GHz
EM-888	IPC TM-650 2.5.5.9	0.006	50%	1 GHz
EM-888	Cavity Resonator	0.008	50%	10 GHz
Megtron 4	IPC TM-650 2.5.5.9	0.005	-	1 MHz
Megtron 4	IPC TM-650 2.5.5.9	0.005	-	1 GHz
Megtron 6	IPC TM-650 2.5.5.9	0.002	-	1 GHz
Megtron 6	*Note	0.004	-	12 GHz

Note - Method by H.Kawataba, Proceedings of the 36th European Microwave Conference, 388-391 (2006)

Table 3.1 illustrates the materials' Df values *as described by the material vendor*. These values were obtained from datasheets readily available on the internet. It should be noted that between vendors and test methods, the frequency points at which the Df value is reported as well as the resin content of the dielectric is inconsistent. For some materials, important information such as test method, resin content, and frequency point may not even be listed and to obtain this information the vendor needs to be contacted personally. Since the way Df values are reported is not standardized, it can be very hard to compare one material to another. Further, since there are so many test methods available, many high speed digital designers may not be familiar with the pros and cons of each one and will therefore not be able to interpret the data sheets properly. This thesis work aims to investigate whether the values in Table 3.1 are valid by examining the Df values over a frequency range rather than a single frequency point.

3.2 Feedback Based Method of Loss Characterization

The feedback-based method for loss characterization was chosen to analyze the above materials. The basic steps of this method as described in the DesignCon 2013 paper are included below [8]

1. Measure the S-parameters of the measurement traces on the test vehicle
2. Select a mathematical expression to be implemented for loss approximation of roughness profile
3. Fit the parameters of the mathematical expression to the measured data.
4. Evaluate quality of the mathematical fit
5. Extract parameters with best fit

3.2.1 Mathematical Approximation of Insertion Loss

The interconnect modeling was performed using Agilent ADS Software. The inputs to the modeling include $Dk(f)$, $Df(f)$, cross sectional parameters of width and thickness for dielectric and copper layers, copper conductivity, and RMS roughness profile parameters. $Dk(f)$ and $Df(f)$ are modeled with the Svensson-Djordjevic model and the roughness was modeled with the Multilevel Hemispherical Model, both of which are described in Chapter 2. The RMS amplitude of the roughness (R_q) is approximated from roughness values provided by the vendor. Although the Svensson-Djordjevic model only requires $Dk(f)$ and $Df(f)$ at a specific frequency, and this information is provided by the material vendor, it was determined that these values can not be trusted and needed to be fit to the measurements data. Finally, the cross sectional parameters are known for each material.

To analyze the data, first $Dk(f)$, $Df(f)$, and R_q are fit to the measurement and extracted from section 1 of test vehicles with no surface oxide treatment. The simulated S_{21} and effective Dk (Dk_{eff}) are compared to the measured S_{21} and Dk_{eff} to optimize the parameters in the model. Then, while only changing the width of

the conductor, the extracted parameters are as inputs to the simulation. Similarly, only changing the value of R_q , the extracted parameters are used as inputs to the simulation for test vehicles of the same material with surface oxide treatment and different copper profiles. If the resulting simulation is not a good fit, the parameters are changed to create a better fit.

3.2.2 Test Vehicle Design

Classic S3 Test Vehicle

The test vehicle used in this thesis is based on the test vehicle described in the S3 test method. The original test vehicle is a 6 layer PCB with test and TRL calibration traces. The calibration traces are dimensioned for 50Ω impedance and are located on layer 2. The lengths of these traces vary depending on the expected dielectric constant of the material. The lengths are determined by calibration breakpoint frequencies f_A , f_B , and f_C the minimum frequency of the calibration f_{min} , and the maximum frequency of the calibration f_{max} . [6]

$$f_A = \sqrt{f_{min}f_B} \quad f_B = \sqrt{f_A f_C} \quad f_C = \sqrt{f_B f_{max}} \quad (3.1)$$

Once the breakpoints are calculated, the lengths of the delay lines are calculated as follows

$$L_1 = \frac{T + 1.5 * 10^8}{\sqrt{Dk}(f_{min} + f_A)} \quad (3.2)$$

$$L_2 = \frac{T + 1.5 * 10^8}{\sqrt{Dk}(f_A + f_B)} \quad (3.3)$$

$$L_3 = \frac{T + 1.5 * 10^8}{\sqrt{Dk}(f_B + f_C)} \quad (3.4)$$

$$L_4 = \frac{T + 1.5 * 10^8}{\sqrt{Dk}(f_C + f_{max})} \quad (3.5)$$

T is the length of the thru trace

Dk is the nominal/estimated value of Dk , the Dielectric constant

Then, for each set of lengths, a corresponding set of frequency ranges can be calculated. This is required as input to the custom VNA calibration.

There are 3 single ended test traces also on layer 2. These test traces are dimensioned for impedances of 48Ω , 50Ω , and 52Ω . On layer 5 there are 3 differential test traces dimensioned for impedances of 96Ω , 100Ω , and 104Ω . Since impedance control is often imprecise during the fabrication process, varying the impedance of the test traces allows for boards to still be useful even if the measured impedances is slightly off from the intended 50Ω .

Test Vehicle Implementation

The final design for the test vehicle inherited many of its qualities from the classic test vehicle described above. A TRL calibration with traces dimensioned in the same manner as the classic S3 test vehicle is used. Test vehicles also include measurement traces of varying impedances.

The core and prepreg of each test vehicle are composed of the same standard construction (2116). However, the thickness, resin content, and as a result nominal dielectric constant vary for each material. It was therefore necessary to do precise impedance modeling for each material and change the trace widths to maintain 50Ω impedance.

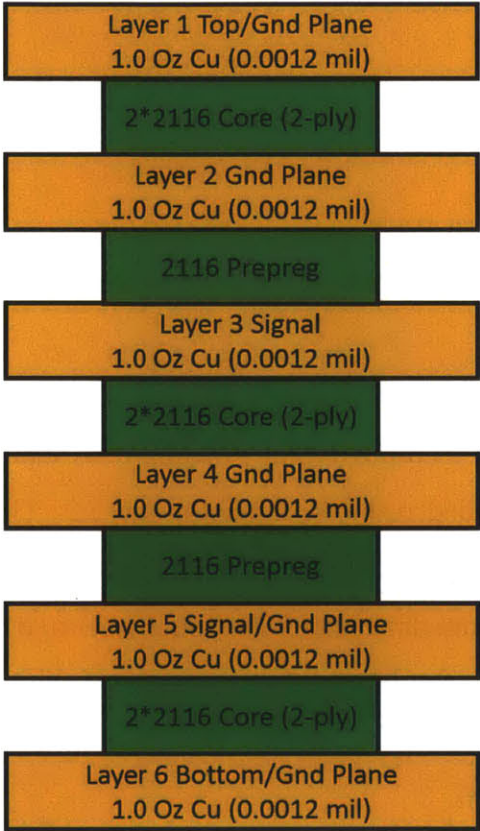


Figure 3-1: Cross section of general test vehicle stackup

The test vehicle is split into three sections. Each of these sections has a different cross section as illustrated in Figure 3-2 . The cross sections are generated by evacuating the copper foil from layers 2 and 4 accordingly. This allows for variation of the widths of the traces while maintaining a 50 Ω characteristic impedance. Traces of section 1 are designed to have width typical of that in a high performance backplane (~ 8.5 mil). Traces of sections 2 and 3 are designed to be considerably larger (~ 19.5 mils, ~ 14 mils respectively) in order to examine the effect of changing the width of a trace on the resulting optimal model parameters. Widths were calculated for each dielectric material using Polar Si9000 Software.

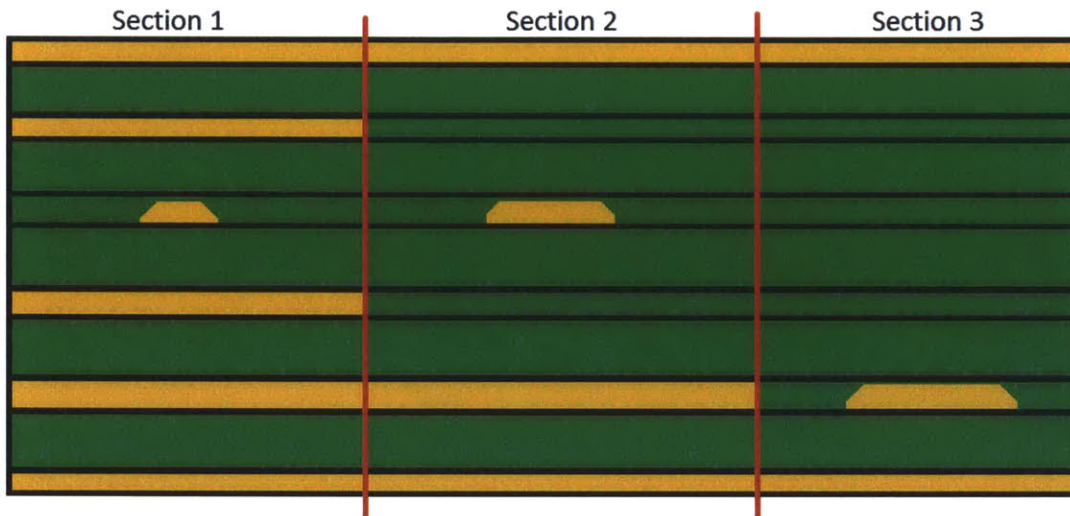


Figure 3-2: Cross section of stackup sections

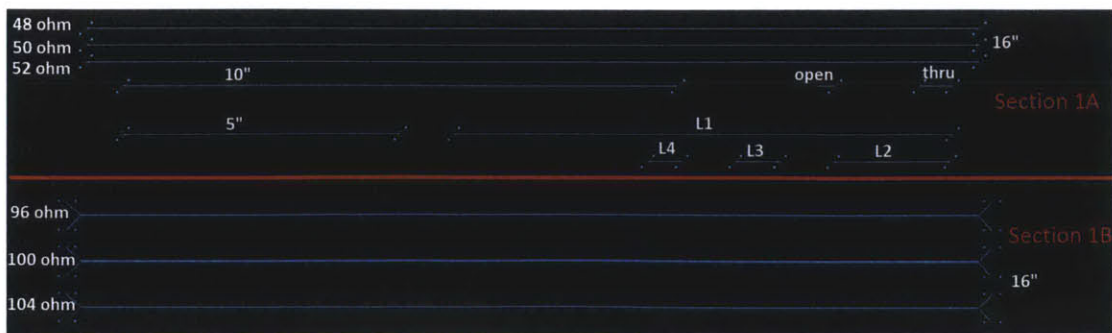


Figure 3-3: Signal layers of test vehicle

Sections 1 and 2 traces are on layer 3 of the stackup, section 3 is on layer 5 of the stackup.

The layout of the calibration and measurement in section 1 traces is pictured in Figure 3-3. The layouts of section 2 and 3 are identical to Section 1A in every aspect other than width. Each section contains the following:

- 3 Measurement traces
- Thru trace
- Open trace
- 4 delay lines
- 5" trace
- 10" trace

Section 1 also includes differential measurement traces. At the time of the test vehicle design it had not been determined whether or not the differential traces, 5" trace, and 10" trace would be used for measurement or calibration. However ultimately these traces were not used and are therefore not relevant to this thesis work.

Each panel is composed of the test vehicle as described previously with the addition of two copies of section 1A. Section 1A traces are of widths expected in a high performance backplane PCB. The insertion loss measurements of this section are therefore most pertinent to a data server application. Three copies of section 1A are included so the measurements could be averaged together and a more accurate calculation could be obtained.

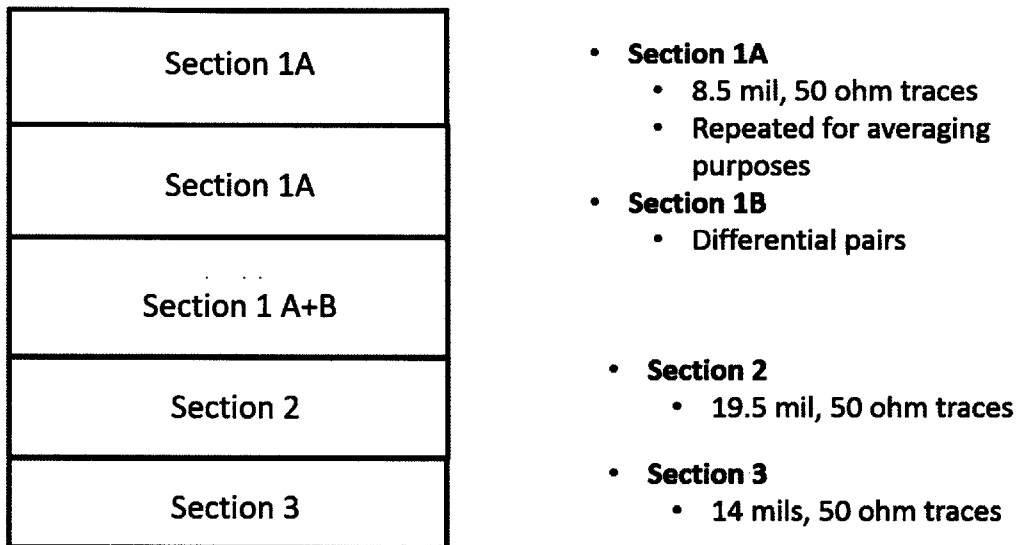


Figure 3-4: Panel Design

Each panel is composed of different combinations of dielectric material, copper foil type, and oxide treatment. This variation allows for the performance of the different dielectric types to be compared. This variation also allows for the robustness of the feedback-based method to be assessed with respect to trace width, oxide treatment, and copper foil type.

Table 3.2: Panel Identification

Panel Identification	Vendor	Material	Foil Type	Surface Treatment
N1a	Nanya	NPLDII	RTF	No Oxide
N1b	Nanya	NPLDII	RTF	AlphaPREP PC-7030
N2a	Nanya	NPLDII	VLP	No Oxide
N2b	Nanya	NPLDII	VLP	AlphaPREP PC-7030
N3a	Nanya	NPG-170D	RTF	No Oxide
N3b	Nanya	NPG-170D	RTF	AlphaPREP PC-7030
N4a	Nanya	NPG-170D	VLP	No Oxide
N4b	Nanya	NPG-170D	VLP	AlphaPREP PC-7030
I1a	Isola	I-Speed IS	RTF	No Oxide
I1b	Isola	I-Speed IS	RTF	AlphaPREP PC-7030
I2a	Isola	I-Speed IS	VLP-2	No Oxide
I2b	Isola	I-Speed IS	VLP-2	AlphaPREP PC-7030
M41a	Panasonic	Megtron 4	RTF	No Oxide
M41b	Panasonic	Megtron 4	RTF	AlphaPREP PC-7030
M61a	Panasonic	Megtron 6	RTF	No Oxide
M61b	Panasonic	Megtron 6	RTF	AlphaPREP PC-7030
M62a	Panasonic	Megtron 6	HVLP	No Oxide
M62b	Panasonic	Megtron 6	HVLP	AlphaPREP PC-7030
E1a	Elite Materials	EM-888	VSP	No Oxide
E1b	Elite Materials	EM-888	VSP	AlphaPREP PC-7030

The terminology used to describe the copper profiles is similar amongst vendors, however the dimensions of the associated roughness vary between vendors. Table 3.3 includes precise definitions of the copper profiles from each vendor. While many vendors use the same name for the copper foil profiles, i.e Very Low Profile (VLP), Reverse Treated Foil (RTF), the average roughness associated with the profiles differs from one material to the next.

Vendor	Foil Type	Shiny Side $R_a(\mu\text{m})$	Matte Side $R_z(\mu\text{m})$	$R_q(\mu\text{m})$
Nanya	RTF	0.5	5.5	-
Nanya	VLP	0.6	<2.2	-
Isola	RTF	0.8	5.13	-
Isola	VLP-2	0.45 (0.3-0.6)	1.6 (1.5-3.5)	0.27 (0.16-0.45)
Panasonic	RTF	5	3	-
Panasonic	HVLP	0.2	1.5	-
Elite Materials	VSP	0.25	3.0	-

Table 3.3: Roughness information provided from each vendor

R_a - The arithmetic average of the deviation from the mean amplitude line

R_z - Arithmetic average of the maximum height of the roughness profile

R_q - The root mean squared deviation from the mean amplitude line

Although R_q is the input to the model, it is not always provided by the vendor. Rather, R_a for the shiny side, which is the side facing the core, and R_z for the Matte side, which is the side facing the prepreg, is typically given. These values can provide an approximate idea of the value of R_q , however modeling needs to be done to select values that fit the data.

Chapter 4

Required Resources

The following software, hardware, and information resources were required for this thesis research:

4.1 Hardware Resources

- Vector Network Analyzer Model Agilent N5230C PNA-L 300KHz-20GHz - used to perform S-Parameter measurements
- Customized Test Vehicles - used to calculate Df differences with respect to width, foil type, and oxide treatment. These test vehicles include

4.2 Software Resources

- MATLAB - MATLAB is a high-level language and interactive environment for numerical computation, visualization, and programming from Mathworks. MATLAB was used to implement the S3 algorithm
- Agilent Advanced Design Software (ADS) - Electronic design automation software for RF, microwave, and high speed digital applications

- Polar Instruments Si9000 Transmission Line Field Solver - Used for impedance calculations. For more information: <http://www.polarinstruments.com/products/si/Si9000.html>

4.3 Information Resources

It is important to gain an understanding of signal integrity problems when approaching this thesis. Several books and articles were read to get an understanding of S-Parameters, copper roughness approximations, and dielectric material characterization.

Chapter 5

Results

5.1 Insertion Loss Comparison

To get a general idea of which material and foil combination performed best, the insertion loss data is plotted in Figure 5-1. Each of these measurements are from test vehicles with no oxide treatment with one exception: I-Speed IS. The data obtained for this material was faulty, likely due to an error in the calibration, and could not be used. Fortunately, as explained in Section 5.3, no oxide and oxide test vehicles have similar insertion loss data for low profile coppers. Therefore, I-Speed IS VLP test vehicles with oxide surface treatment are equally informative as those without. The lowest profile copper available for each material was selected and plotted.

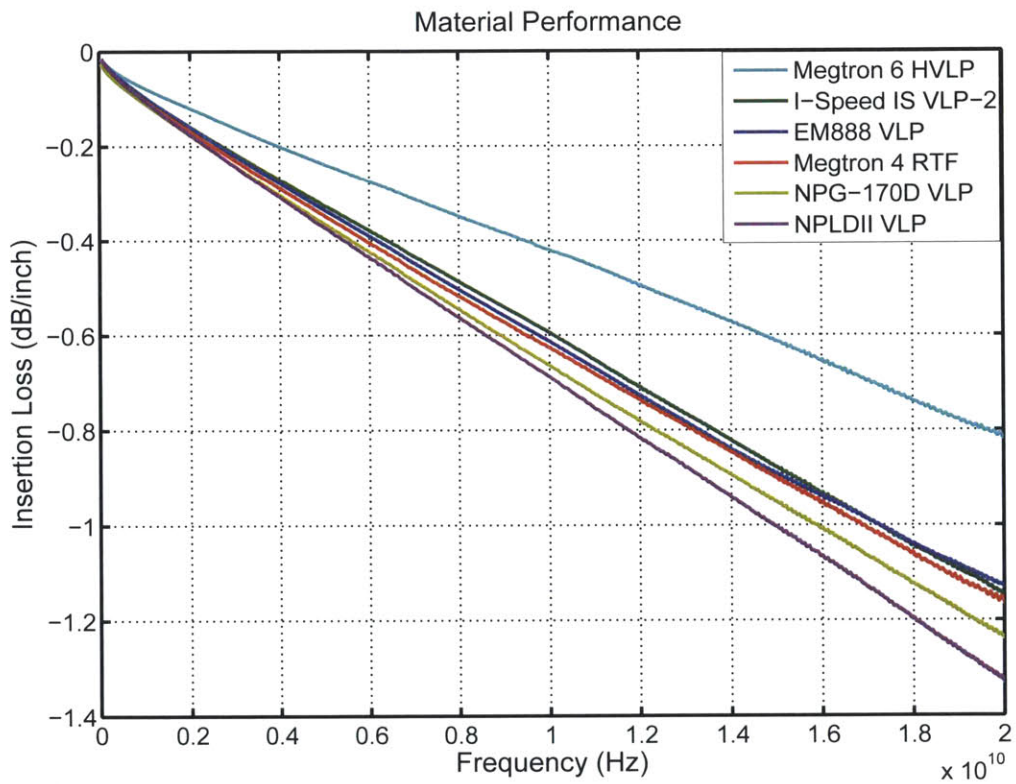


Figure 5-1: Insertion loss of materials examined for this thesis work

5.2 Extracted Dk and Df for Each Material

The input parameters $Dk(1\text{GHz})$, $Df(1\text{GHz})$, and R_q were varied to get the best possible fit of the simulated data to the measured data. The material and foil combinations considered were those with the lowest insertion loss. These are plotted in Figure 5-1. When constrained by the known parameters of the model, like the cross sectional parameters, copper conductivity, and approximate R_q values, getting a good fit was consistently a choice between overestimating at lower frequencies and fitting at higher frequencies, or fitting at lower frequencies and underestimating at higher frequencies. Let us name these two situations High Fit and Low Fit respectively. Figure 5-2 has two samples of the generated S_{21} and Dk_{eff} data compared to the measured data in the High Fit case. In both Figure 5-2 A and Figure 5-2 B the insertion loss is overestimated at lower frequencies with A corresponding to the largest overestimate in the data and B corresponding to the smallest.

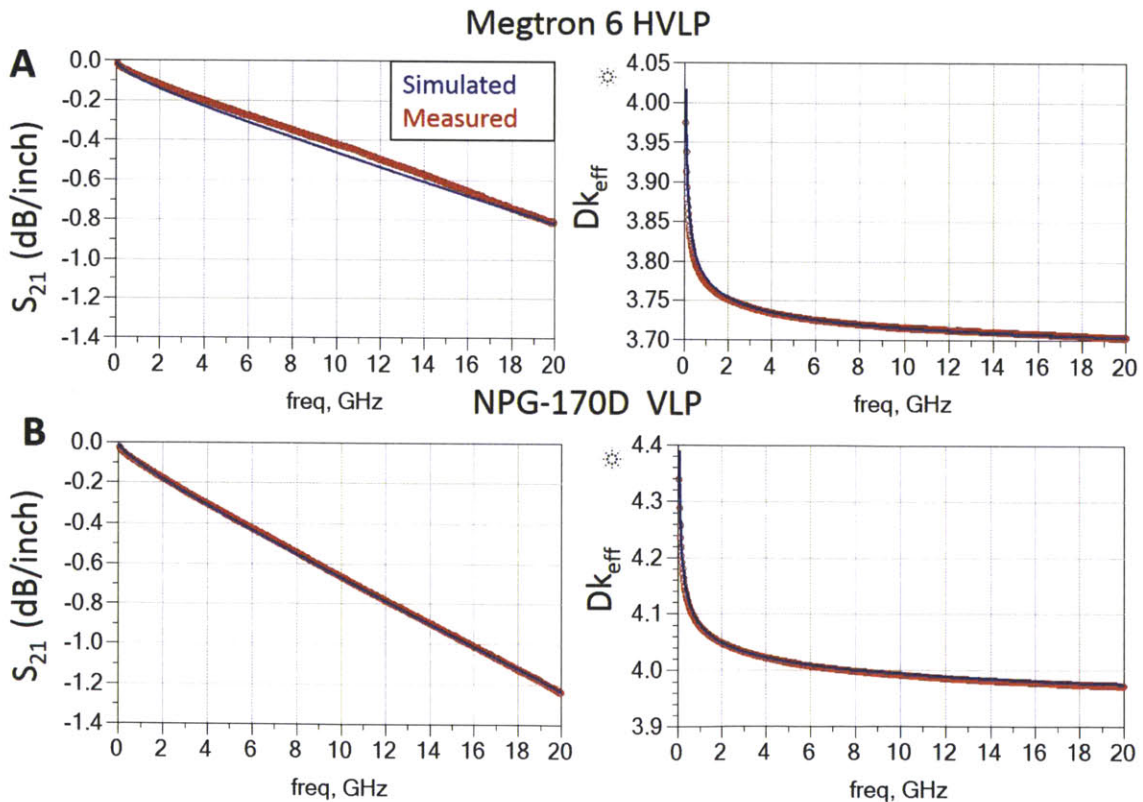


Figure 5-2: High Fit Modeling S_{21} and Dk_{eff} in Agilent ADS

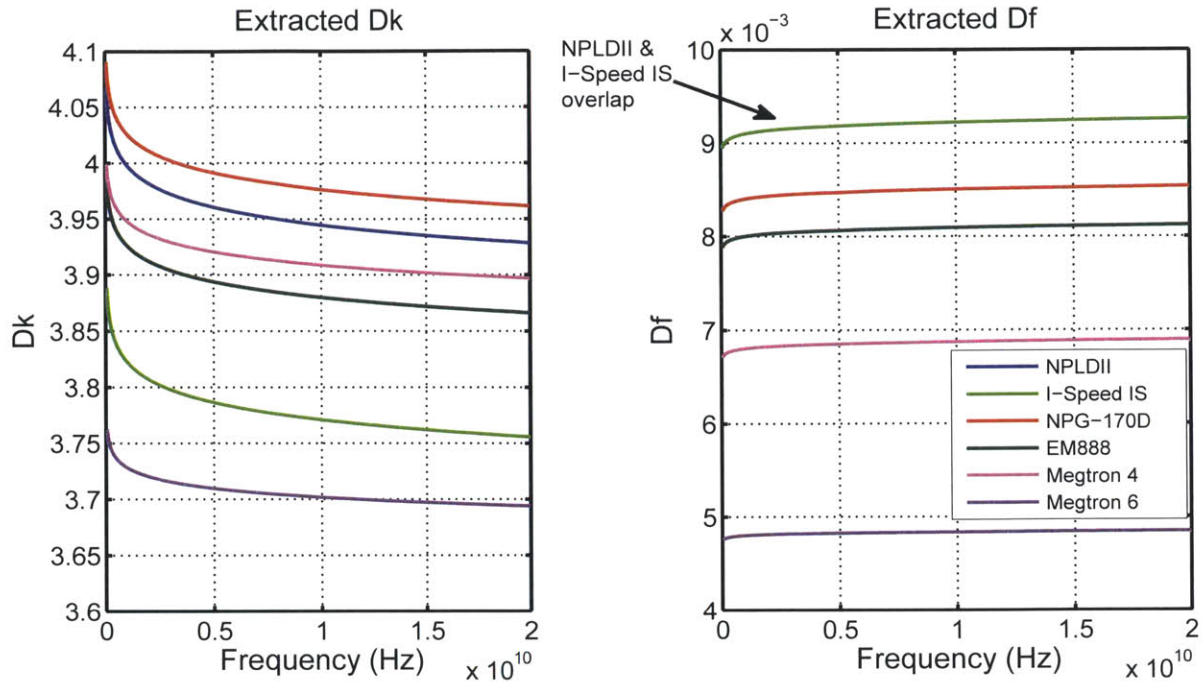


Figure 5-3: Extracted Dk and Df for High Fit Modeling

Extracted values for Dk(1GHz) and Df(1GHz) in the High Fit case were used to plot Dk(f) and Df(f) in MATLAB and are displayed in Figure 5-3.

Figure 5-4 has two samples of the generated S_{21} and Dk_{eff} data as compared to the measured data in the Low Fit case. In both Figure 5-4 A and Figure 5-4 B the insertion loss is underestimated at higher frequencies with A corresponding to the largest underestimate and B corresponding to the smallest.

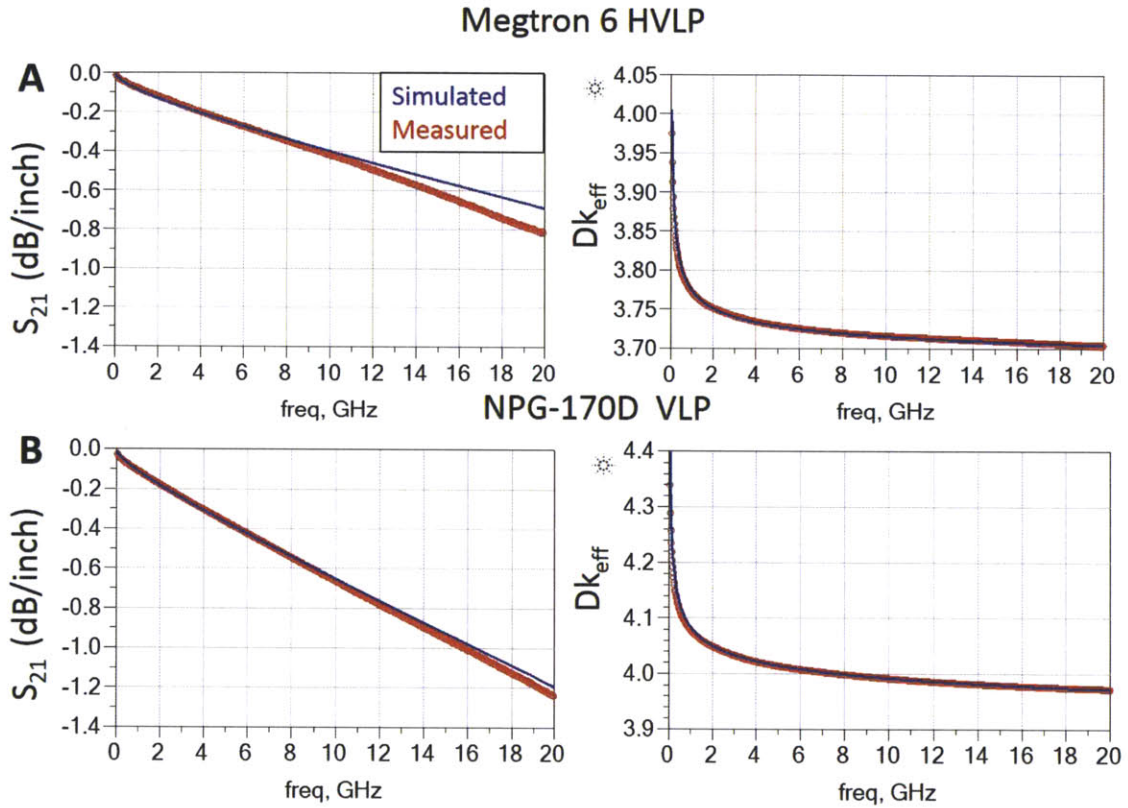


Figure 5-4: Low Fit Modeling S_{21} and Dk_{eff} in Agilent ADS

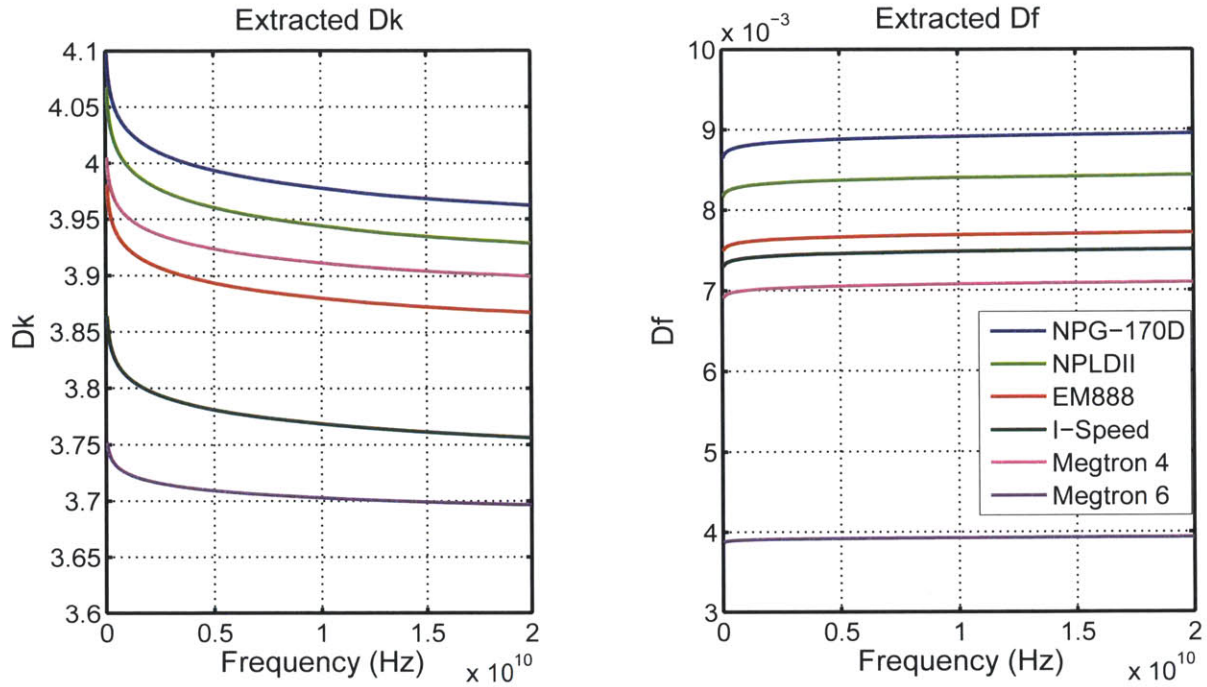


Figure 5-5: Extracted Dk and Df for Low Fit Modeling

Again, extracted values for Dk(1GHz) and Df(1GHz) were used to plot Dk(f) and Df(f) in MATLAB and are displayed above.

5.3 Modeling Copper Foil and Oxide Surface Treatment

Both changes in foil type and oxide type were modeled with a High Fit model, since these parameters tend to affect high frequency losses. Lower profile copper consistently produces lower losses at high frequency, as expected. However, for many of the measurements the oxide treatment did not have much of an effect on the insertion loss seen at high frequency.

The reason for this is likely due to the specific chemistry of the particular oxide, AlphaPREP PC-7030, used in this work. The small grain structure of the low-profile foils can inhibit the normal etching action of the oxide, creating a smaller roughness profile than typically seen with high-profile foils. For this reason the effect of oxide was not considered for test vehicles whose copper profile was unaffected by the oxide treatment. [6]

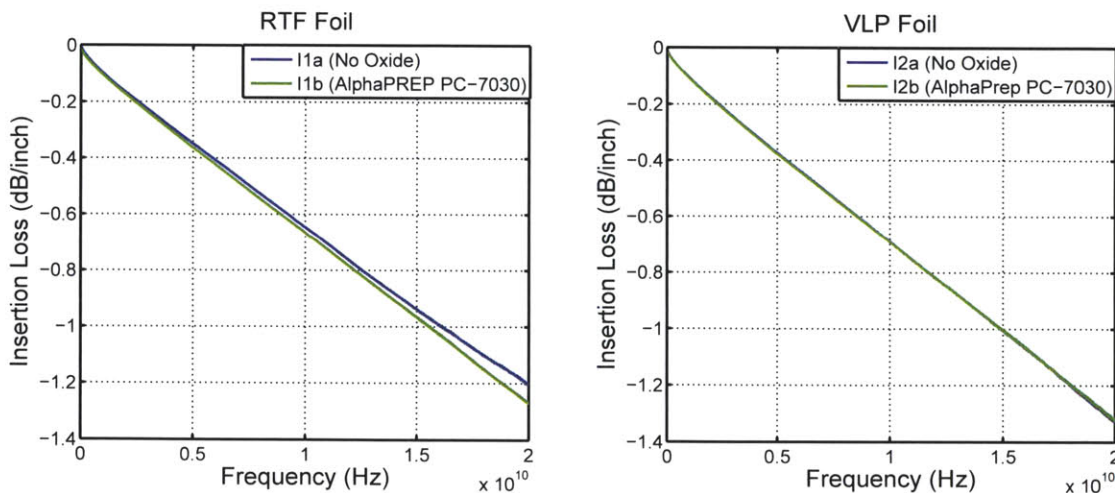


Figure 5-6: Effect of foil type on oxide induced losses from section 1 traces in I-Speed IS, RTF test vehicles and NPLDII, VLP test vehicles

The only material and foil combination that experienced a noticeable difference with and without the oxide treatment was I-Speed IS with RTF foil. The effects of oxide on this material were well modeled by an increase in R_q from $0.95\mu\text{m}$ to $2.05\mu\text{m}$ in the simulation parameters with $Dk(f)$ and $Df(f)$ unchanged.

The effects of the change in foil type were modeled by the Multilevel Hemispherical Model in Agilent ADS. Again, the data was fit in the High Fit regime, since roughness changes primarily effect high frequency insertion loss. Table 5.1 illustrates the changes in roughness associated with the changes in copper foil profile.

Material	Foil Type	Simulated R_q (μm)
I-speed IS	VLP-2	0.35
I-speed IS	RTF	0.45
Megtron 6	HVLP	0.3
Megtron 6	RTF	0.6
NPG-170D	VLP	0.25
NPG-170D	RTF	1.2
NPLDII	VLP	0.35
NPLDII	RTF	0.75

Table 5.1: Changes in roughness parameters for foil types of each material

Although the change in insertion loss seen with the change in foil type arises from an increase in the roughness amplitude, the losses can also be well fit by increasing $Df(f)$. Figure 5-7 displays results from both changing the roughness and changing $Df(f)$. Specifically 5-7(A) represents an increase in R_q from $0.25\mu\text{m}$ to $1.2\mu\text{m}$. 5-7(B) represents an increase in $Df(1\text{GHz})$ from 0.008 to 0.0087.

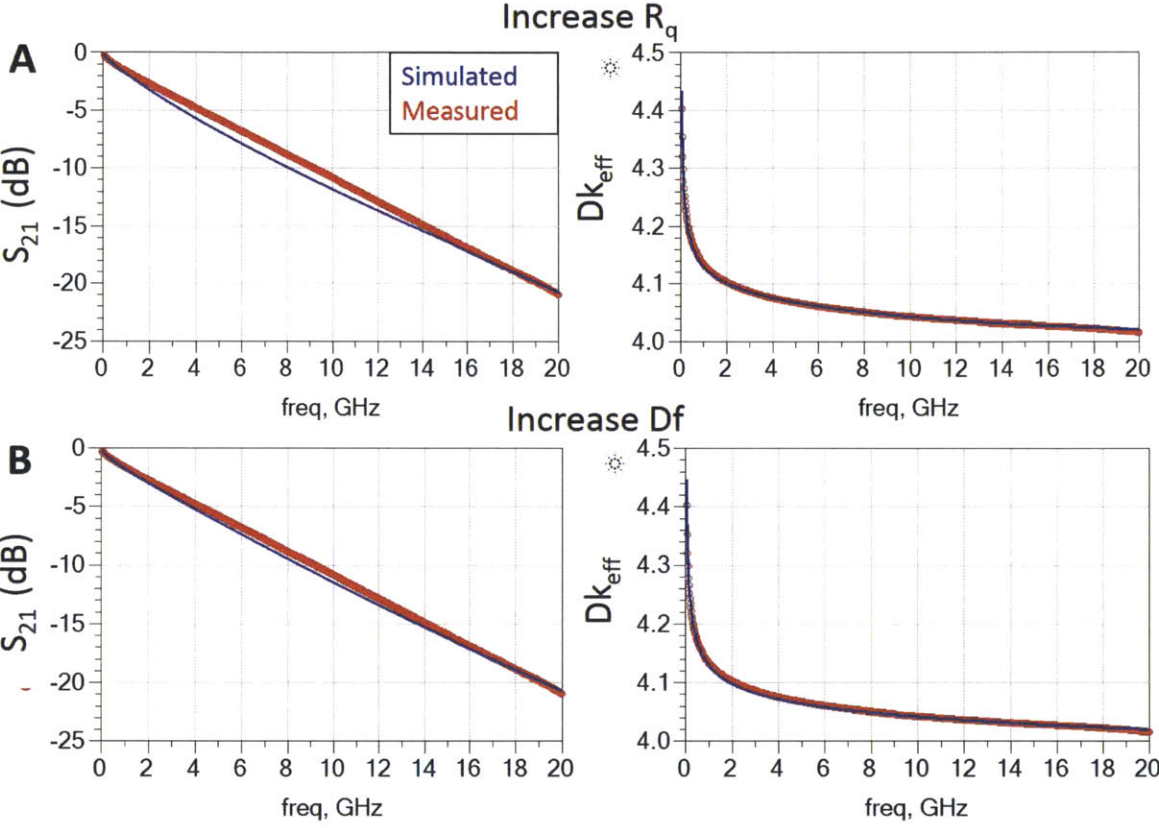


Figure 5-7: Increasing R_q and increasing $Df(f)$ to model increase in roughness for NPG-170D

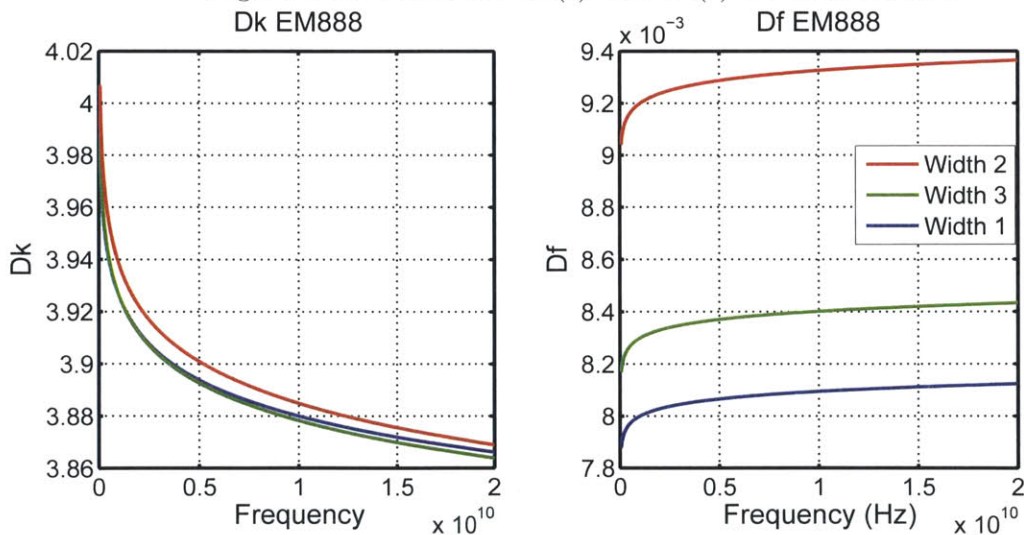
5.4 Modeling Effects of Width Variation

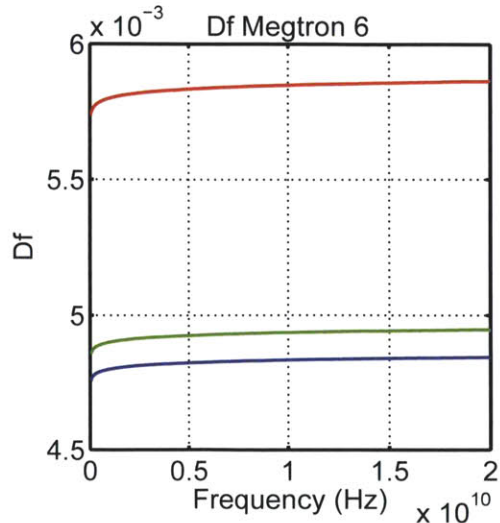
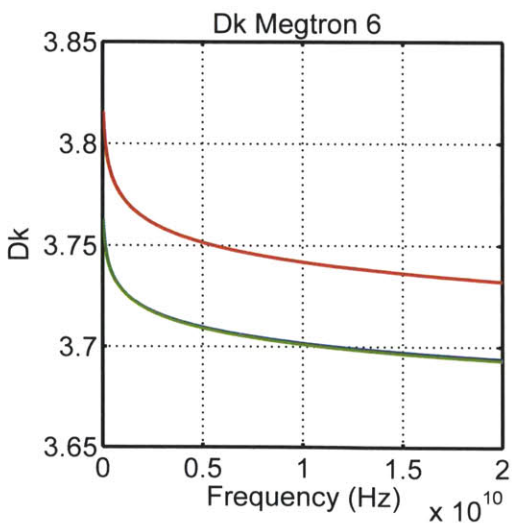
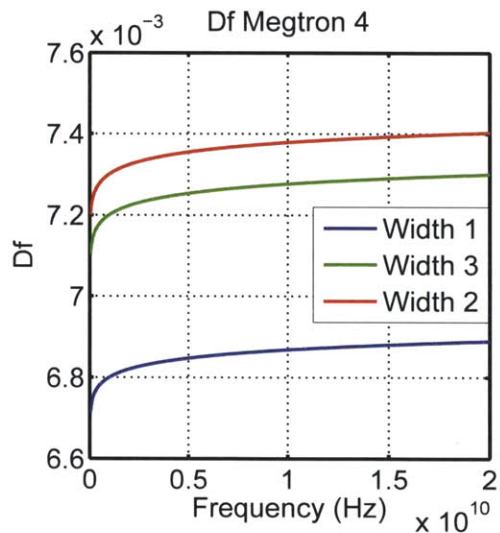
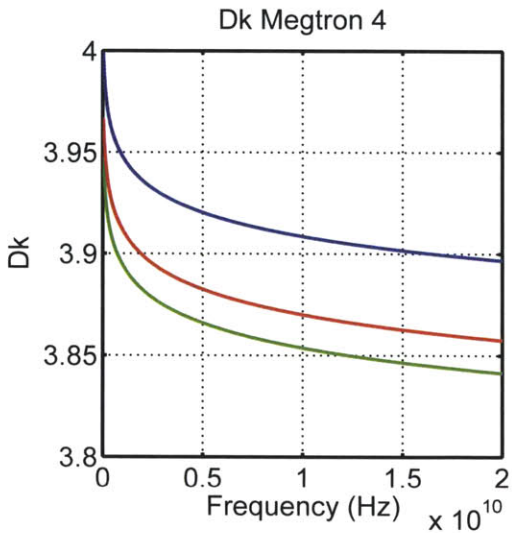
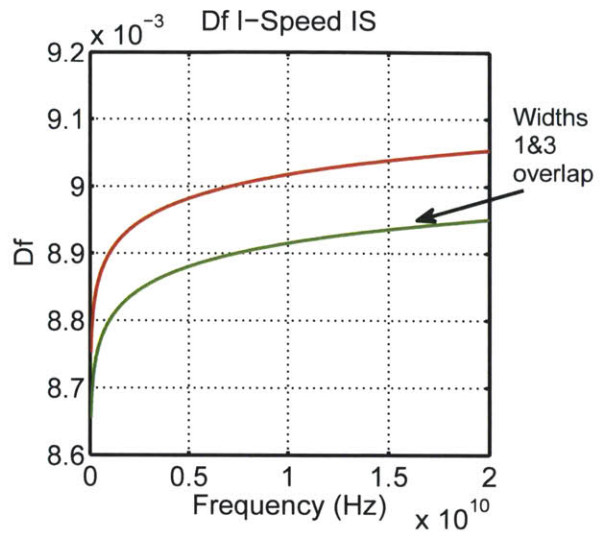
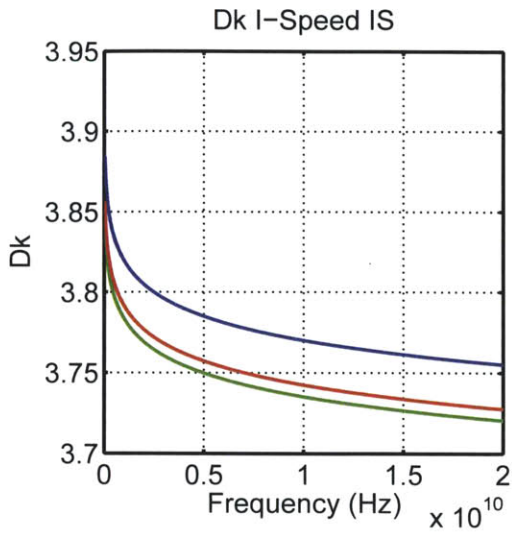
Dk(f) and Df(f) were extracted for each section and are displayed in Figure 5-8. Table 5.2 can be used for reference for widths in each section. Section 1 corresponds to Width 1, Section 2 corresponds to Width 3, and Section 3 corresponds to Width 2.

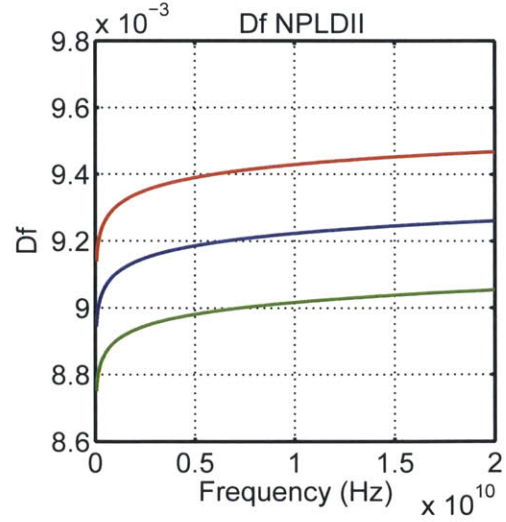
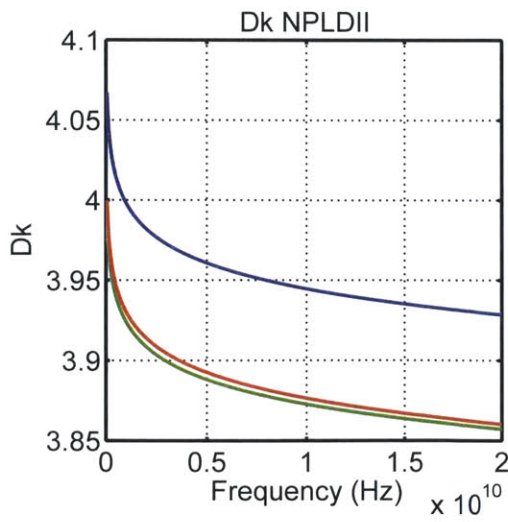
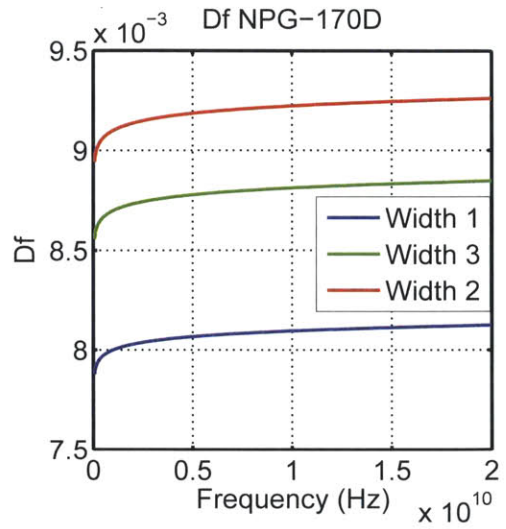
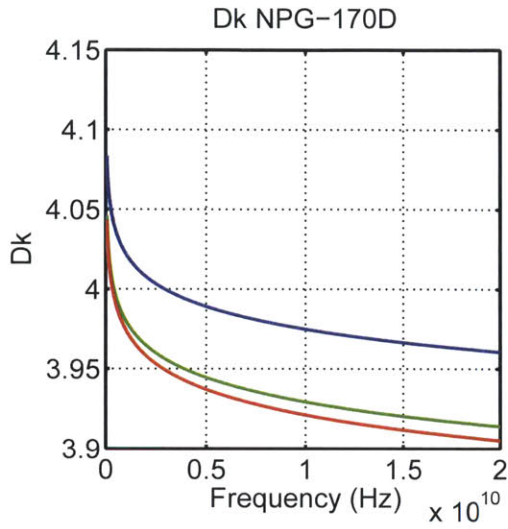
Material	Width 1 (μm)	Width 2 (μm)	Width 3 (mil)
EM888	8.7	15	20.5
I-Speed IS	9.7	16.5	21.5
Megtron 4	8.2	14	19.5
Megtron 6	8.7	14.	20.7
NPG-170D	9	14.5	20.7
NPLDII	9.2	14	19.5

Table 5.2: Widths of measurement traces in each section

Figure 5-8: Extracted Dk(f) and Df(f) for each section







Chapter 6

Discussion and Future Work

One goal of this thesis work was to assess which material had the lowest loss according to the Feedback-Based Model. In both the High Fit regime and the Low Fit regimes Megtron 6 had the lowest Df, with 0.0039 at 1GHz for the Low Fit and 0.0048 at 1GHz for the High Fit. Megtron 4 had the next lowest Df, with 0.0068 at 1GHz for the Low Fit and 0.007 at 1GHz for the High Fit. Extracted Df(f) in the Low Fit regime is much closer to the advertised values of Df by the material vendors, while extracted Df(f) in the High Fit regime is often 0.003-0.004 above that advertised by the vendor. This suggests that Df values advertised by vendors may only be trustworthy for lower frequencies, specifically up to about 8 GHz.

The second goal of this thesis work was to assess the efficacy of the Feedback-Based Model. For some materials accurately fitting the simulated data to both the low frequency insertion loss and the high frequency insertion loss posed a challenge. Specifically, when fitting the parameters to match the high frequency behavior, the low frequency insertion loss was overestimated. Conversely, when fitting the parameters to match the low frequency behavior, the high frequency insertion loss was underestimated.

There are a number of possible explanations for the inaccuracy of the model for the entire data range. The Svensson-Djordjevic model, used to calculate Dk(f) and Df(f), assumes a log dependence on frequency. However, this log dependence does not seem to be aligning well with the data collected for these materials. The

Svensson-Djordjevic model was developed for FR-4, a popular dielectric material with significantly higher loss than the materials examined in this work. It is possible that assumptions made for the frequency dependence of D_k and D_f in FR-4 do not apply and a different model needs to be used.

There are some limitations to this modeling. For one, R_q values are often provided as a range of values or are not specified whatsoever. A difference of $0.1\mu\text{m}$ for R_q has a significant effect on the simulated results. Furthermore, the dielectric layers in the stackup for sections 2 and 3 of the test vehicle is comprised of layers of core construction and prepreg. The dielectric constants of these layers is known to be similar but not exactly the same. In the model the combination of core construction and prepreg is modeled as one dielectric material, introducing some inaccuracy to the results.

One question investigated was whether the Feedback -Based Model could capture the effects of varying roughness. In the case of varying the oxide surface treatment, it was expected that changing the roughness parameters would accurately represent the changes seen in the insertion loss and effective D_k . Unfortunately, the specific type of oxide surface treatment used had no effect on a majority of the copper profiles used in this research and no conclusive results could be obtained.

In the case of the copper profile, the effect of going from a a low profile copper foil such as VLP or HVLP to a higher profile copper such as Reverse Treated Foil (RTF) could be fit well by increasing the R_q in the input to the simulation. The change in roughness has a small effect on the dispersion in the material, and therefore only slightly changes the simulated Dk_{eff} . The inputs $Dk(1\text{GHz})$ and $Df(1\text{GHz})$ did not need to change very much to accomodate the changing foil.

The change in profile type could also be fit well by instead increasing $Df(1\text{GHz})$, changing $DK(1\text{GHz})$, and holding R_q constant. In some cases this even created a better fit than an increase in R_q . This finding is supported by findings made by Gerald Gold and Klaus Helmreich in their Designcon 2014 paper entitled "Effective Conductivity Concept for Modeling Conductor Surface Roughness". This paper demonstrates that the effects of an increased R_q can be lumped into an effective con-

ductivity. This effective conductivity is defined as the conductivity of a material with an ideally smooth surface that would cause the same loss as the rough surface. The loss caused by the roughness that has been previously attributed to the dielectric has the same frequency dependence as the simulated losses due to an effective conductivity. Potential future work should involve varying the factors varied in this thesis, such as width, foil type, and oxide surface treatment, to see if they can be well modeled by an effective conductivity[5].

For most materials, VLP and RTF foils have very similar performance and consequently similar simulated RMS roughness amplitudes. Although not identical, these two foil types seem to be very similar in terms of high frequency copper roughness losses. In fact, both Panasonic and Elite Materials no longer provide both options because they perform so similarly. Rather, Elite Materilas has discontinued RTF and only provides VLP. Panasonic has discontinued VLP and only provides RTF and HVLP (Hyper Very Low Profile) copper. Higher profile coppers were initially pursued to create greater variation between foil types, however across the board the vendors only provided reverse treated and low profile copper foils. This reflects an industry trend of discontinuing production of copper foils that produce high losses at higher frequencies.

In the case of the width, it was expected that changing the width of the trace for each section would encompass all the changes seen in the measurements. There was slight variation seen in the extracted D_k and D_f of the different widths. Specifically in most materials the narrowest width, width 1, produced the lowest $D_f(f)$ while middle width, width 3, produced the highest $D_f(f)$. The exceptions are Isola's I-Speed IS and Nanya's NPLDII.

The dielectric layers of sections 1, 2, and 3 are composed of either core construction, prepreg, or both. Core construction and prepreg have similar, but not identical D_k s. The modeling imposes an identical dielectric on both, introducing some inaccuracy. This could contribute to the differences in extracted $D_k(f)$ and $D_f(f)$. Further work may include creating a more complicated model that could account for these slight changes, or developing test vehicles that keep the stackups identical, vary the

widths, and as a consequence vary the characteristic impedance of the interconnects.

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