A 120nW 18.5kHz RC Oscillator with Comparator Offset Cancellation for ±0.25% Temperature Stability

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Integrated low-frequency oscillators can replace crystal oscillators as sleep-mode timers to reduce the size and cost of wireless sensors [1]. Since the timer is one of the few continuously functioning circuits, minimizing its power consumption can greatly reduce sleep-mode power of highly-duty-cycled systems. Temperature stability of the oscillator is important in order to minimize timing uncertainty and guard time for the radars, and thus maximizing sleep time. The voltage-averaging feedback method described in [2] achieves high stability in the MHz frequencies, but when scaled to the kHz range, requires very large filters. On the other extreme, gate leakage-based timers have been designed for sub-nW power consumption, but operate in the sub-Hz frequencies [3]. In the past, high accuracy RC oscillators in the kHz range have been designed with feedforward correction [1] and self-chopped operation [4]. In this work, an offset cancellation architecture achieves long-term frequency stability and temperature stability while operating at lower power. The architecture of the proposed offset-cancelling oscillator is shown in Fig. 10.7.1. When phase φ=0, a current I passes through resistor R to generate a voltage V/R on node Vc. At the same time, a matched current source charges capacitor C1, such that node V1 crosses Vt at time RC. After I×t, corresponding to the delay of the comparator and subsequent buffers, φ changes to 1, which then resets the capacitor voltage. In addition, the role of the two comparator inputs is reversed, with V1 being the resistor voltage and V2 the voltage across capacitor C2. The period of the oscillator is thus nominally 2RC+2tmax. Two separate capacitors are used in the two phases so that the delay of capacitor discharge is not included in the period. This switching scheme also cancels comparator offset. For example, if the comparator has an offset Vos, as shown in Fig. 10.7.2, the duration of phase φ=0 increases by CVos/I, however the opposite phase φ=1 decreases by the same amount, thus the total period of oscillation is constant. This cancellation scheme allows significant power reduction in the oscillator by: (a) permitting low-swing oscillations since offset and temperature variations of the offsets do not proportionally affect frequency stability, (b) requiring only one comparator as opposed to two in traditional architectures, and (c) relaxing the specifications on the comparator offset, and allowing optimization of gain and bandwidth. The offset cancellation also attenuates the effect of flicker noise, improving long-term stability of the oscillator.

In this design R is chosen to be 5MΩ and C1 and C2 are 5pF for an RC time constant of 25μs. The charging current I is 30nA on each branch, for a swing of only 150mV. Simulations show that a 10mV offset change (~6% of the swing) can greatly reduce sleep-mode power of highly duty-cycled systems. Simulations show that a 10mV offset change (~6% of the swing) can greatly reduce sleep-mode power of highly duty-cycled systems. The offset-cancellation scheme helps reduce the flicker noise and its contribution to the Allan deviation, leaving a floor below 20ppm for intervals over 0.5s. This indicates the ability of the oscillator to measure long sleep times accurately. Fig. 10.7.6 summarizes this work and compares it with previously published RC oscillators operating in various frequencies. In conclusion, an offset cancellation scheme has been presented that helps achieve temperature stability of ±0.25%, ultra-low power operation at 120nW and long-term stability of better than 20ppm, advancing the state of fully-integrated timers for wireless sensors.

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References:
[1] T. Tokairin, et al., "A 280nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," Dig. Symp. VLSI Circuits, pp. 16-17, June 2012
Figure 10.7.1: Architecture of the proposed offset compensated RC oscillator. The switch state for phase $\phi=0$ is shown with off switches grayed out.

Figure 10.7.2: Timing diagram showing the operation of the offset-cancellation architecture for the case of positive comparator offset $V_{OS}$.

Figure 10.7.3: Implementation of the constant-BW comparator and the digital Schmitt trigger.

Figure 10.7.4: Temperature measurements for the oscillator showing the effect of varying charging current, total power consumption and effectiveness of the offset compensation scheme.

Figure 10.7.5: Allan Deviation measurement over 24 hours shows long-term stability of the oscillator.

Figure 10.7.6: Summary of measured results and comparison to previous work.
Figure 10.7.7: Die photo of the chip fabricated in 65nm CMOS.