Power Monitoring in Integrated Circuits

by

Anas Ibrahim Al Bastami

B.S., Texas A&M University at Qatar (2012)

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Author .....
Department of Electrical Engineering and Computer Science
August 29, 2014

Certified by .....
Steven B. Leeb
Professor
Thesis Supervisor

Certified by .....
Al-Thaddeus Avestruz
Doctoral Candidate
Thesis Supervisor

Accepted by .....
Leslie A. Kolodziejski
Chair, Department Committee on Graduate Students

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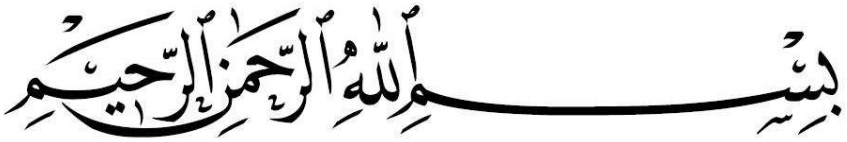
Abstract

Power monitoring is needed in most electrical systems, and is crucial for ensuring reliability in everything from industrial and telecom applications, to automotive and consumer electronics. Power monitoring of integrated circuits (ICs) is also essential, as today ICs exist in most electrical and electronic systems, in a vast range of applications. Many ICs, including power ICs, have functional blocks across the chip that are used for different purposes. Measuring circuit block currents in both analog and digital ICs is important in a wide range of applications, including power management as well as IC testing and fault detection and analysis. For example, the presence of different kinds of faults in IC circuit blocks during IC fabrication causes the currents flowing through these circuit blocks to change from the expected values. There has been general interest in monitoring currents through different circuit blocks in an attempt to identify the location and type of the faults. Previous works on nonintrusive load monitoring as well as on power-line communications (PLCs) provide motivation for the work presented here. The techniques are extended and used to develop a new method for power monitoring in ICs.

Most solutions to the challenge of measuring currents in different circuit blocks of the IC involve adding circuitry that is both costly and power consuming. In this work, a new method is proposed to enable individual measurement of current consumed in each circuit block within an IC while adding negligible area and power overhead. This method works by encoding the individual current signatures in the main supply current of the IC, which can then be sensed and sampled off-chip, and then disaggregated through signal processing. A demonstration of this power monitoring scheme is given on a modular discrete platform that is implemented based on the UC3842 current-mode controller IC, which can also be used for educational purposes.

Thesis Supervisor: Steven B. Leeb
Title: Professor

Thesis Supervisor: Al-Thaddeus Avestruz
Title: Doctoral Candidate



﴿ وَقُل رَّبِّ زِدْنِي عِلْمًا ﴾

And say, "My Lord, increase me in knowledge."

Quran [20:114]

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Chapter 1

Introduction

Power monitoring is needed in most electrical systems, and is crucial for ensuring reliability in everything from industrial and telecom applications, to automotive and consumer electronics. Power monitoring of integrated circuits (ICs) is also essential, as today ICs exist in most electrical and electronic systems, in a vast range of applications. Many ICs have functional blocks across the chip that are used for different purposes. Power ICs also have multiple circuit blocks, each performing their own function. An example of a typical power management IC is shown in Figure 1-1 [1]. Measuring circuit block currents in both analog and digital ICs is important in a wide range of applications, including power management as well as IC testing and fault detection and analysis.

1.1 Motivation

The motivation behind the proposed monitoring technique comes from three different ideas. Non-Intrusive Load Monitoring (NILM) has been shown to be useful in determining the power consumption of individual loads in a power distribution system [6, 7, 8, 9]. The major advantage of NILM is the ability to determine the load composition of household appliances through a single point of measurement at the main power feed [6]. The decomposition of the single point measurement is normally performed by using pattern matching and classification algorithms on a set of

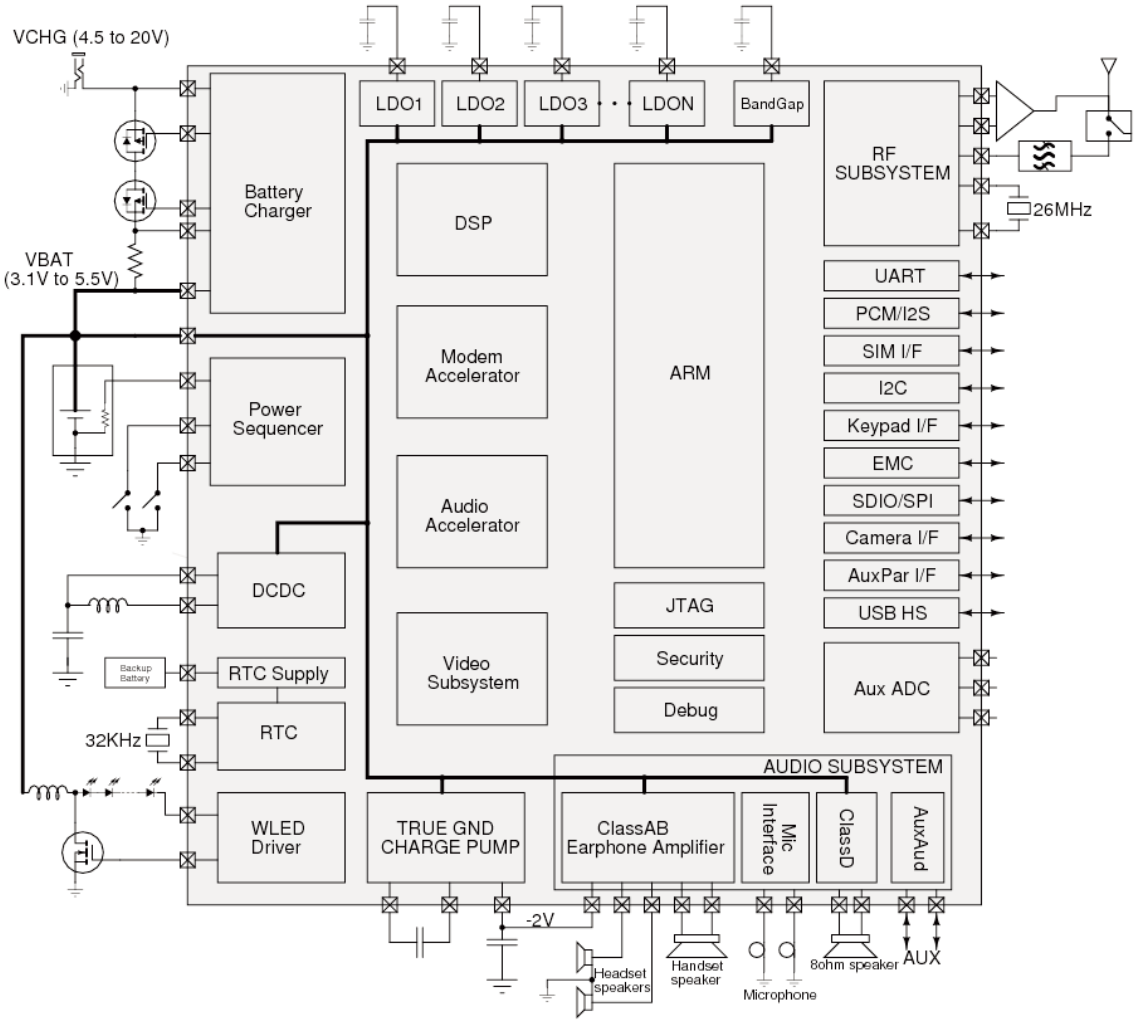


Figure 1-1: A typical power management IC block diagram showing the numerous circuit blocks present [1] (© 2011 IEEE).

pre-recorded transient or steady-state power signatures of the different loads. NILM has been implemented in a number of residential, commercial, as well as automotive applications [7], where the recorded signatures of the appliances were processed and matched with real-time power readings for individual load power consumption estimation. Once a signature has been identified, it is straightforward to tabulate the power consumption of that specific load.

Measuring power supply currents in both analog and digital ICs has proven to be crucial in IC testing and in fault detection and analysis. The presence of different kinds of faults in IC circuit blocks during IC fabrication causes the currents flowing

through these circuit blocks to change from the expected values. This effect is sketched in Figure 1-2. Therefore, there has been general interest in monitoring currents through different circuit blocks in an attempt to identify the location and type of the fault [10]. For digital CMOS VLSI circuits, the switching of the transistors in different circuit blocks cause specific current transients to appear on the power-line. It is important to monitor these transients in both time and frequency domains and compare them with the expected transients in order to identify any faults [2]. This technique of supply current monitoring, known as *IDDQ testing*, has been adopted by many in the semiconductor industry [2, 11, 12, 13, 14]. In fact, as electronic designs continue to grow in complexity, there is interest in having multiple monitoring blocks that track changes in temperature, voltage, and error data [15].

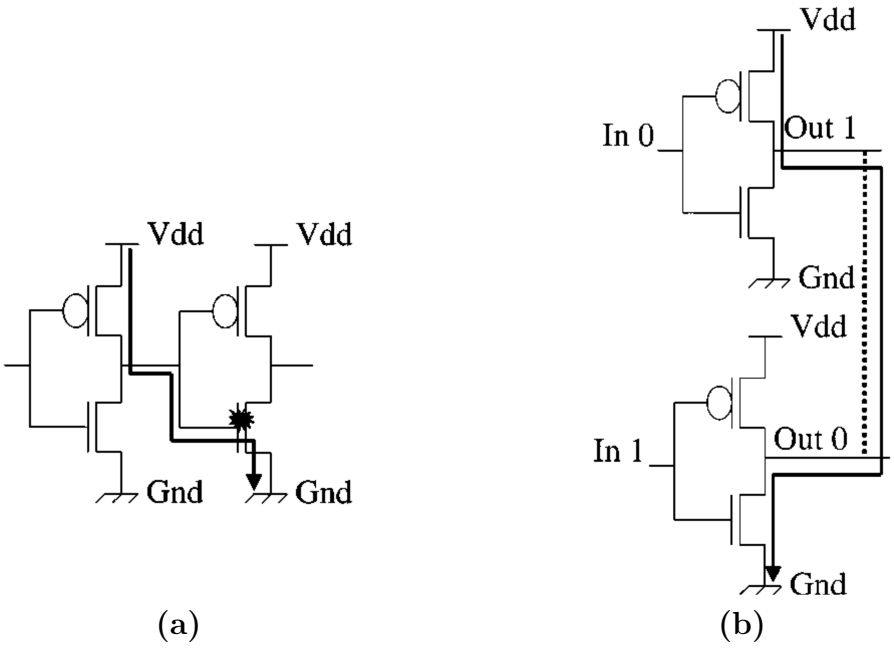


Figure 1-2: Formation of current paths in presence of: (a) gate-oxide short, and (b) metal bridging in CMOS circuits [2].

Another idea that motivated the development of the proposed current monitoring technique is the transmission of data over the power-line, referred to as *Power-Line Communications* (PLC) in the literature [16, 17, 18]. The use of the power-line as a medium through which system information can be transferred has been considered since the 1830's [16]. Nevertheless, application of this technique has been for many

years limited to low speed data communications such as power distribution automation and local area networks due to undesirable channel characteristics. For example, the PLC channel's characteristics, such as the frequency response and channel noise, vary depending on the electrical system's wiring structure, wire types, as well as the loads connected to the circuit [18]. In addition, the channel is time-varying and frequency-selective in nature, which makes the PLC channel a very hostile medium for data transmission [19]. To be able to understand, model, and simulate PLC channels, several approaches have been used. The communication approach in particular has been used very widely since it permits the use of classical communication methodologies to make the transmitted data less vulnerable to corruption [16]. Recent advances in modulation and coding schemes have enabled the use of the PLC channel as a medium for high speed data transmission. Spread spectrum, for example, has been considered as an effective solution for PLC due its robustness against interference and its ability for multiple access operation [16].

Combining these three concepts together yields a nonintrusive current monitoring technique that enables us to monitor the current (and thus power) consumption of different circuit blocks in an IC.

1.2 Method and Architecture

The proposed method involves modulating the current flowing through each individual circuit block by unique predetermined digital codes. In particular, the current through each circuit block is perturbed proportionally so that the value of the dc current is encoded on the ac amplitude of these perturbations. The timing of these perturbations is determined by known codes that are unique to each circuit block. Equivalently, this process represents amplitude modulation, where the perturbation signal acts as the carrier, and the value of the current acts as the information. Note that the perturbations are designed to be much smaller in magnitude (e.g. 5%) than the value of the current itself. This ensures that each circuit block operates normally, and prevents interference with the circuit operation. Since each circuit block has its

own unique carrier signal and all currents in the different circuit blocks add up on the power-line, the method resembles data transmission on a PLC channel. The IC power-line can be thought of as a communication channel, where each circuit block behaves as a "user", each sending modulated information that is uniquely encoded. The communications scheme is equivalent to that used in code division multiple access (CDMA) systems in wireless communications. With proper choice of codes, one can transfer individual circuit block information outside the chip through the power-line channel.

Among the various available circuit building blocks, current mirrors are among the most prevalent in almost every subsection of a chip, such as in the blocks shown in Figure 1-1. In addition to this, the structures of current mirrors allow for ease of perturbation of the quiescent current flowing through them. For these reasons, the power monitoring scheme will be demonstrated on circuit blocks that are biased by current sources that utilize the simple current mirror architecture. Figure 1-3 shows a sketch of the proposed method.

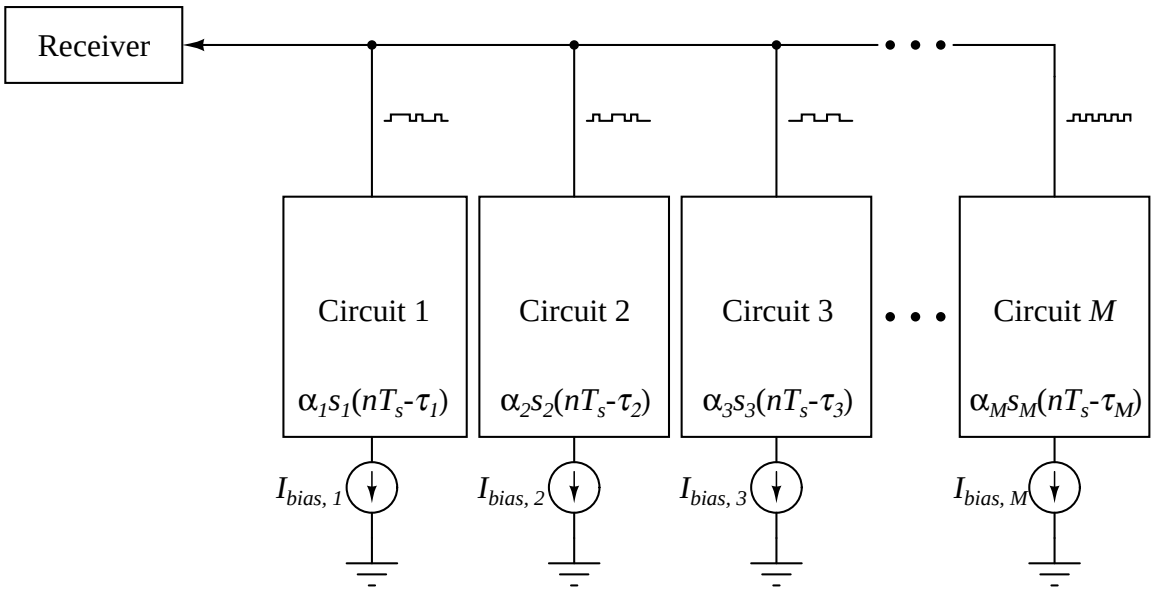


Figure 1-3: Sketch of the proposed current monitoring method.

Each circuit block sends a current signal of the form $\alpha_i s_i(nT_s - \tau_i)$, where α_i

denotes the current information that will be transmitted, $s_i(t)$ denotes the carrier signal associated with that circuit, τ_i denotes the delay, T_s denotes the sampling period, and n is the sample number. The fact that $t = nT_s$ is to emphasize that the data is sampled later on. Note also that the fact that each circuit has its own delay τ_i means that the perturbations of different circuit blocks are not synchronized with each other, which makes the method more realistic and practical. After the data is transferred outside the chip through the power-line, the total aggregate current is sensed and digitized for processing in MATLAB.

This power monitoring method is tested on different circuit blocks of a power electronic controller kit that is based on the UC3842 pulse width modulation (PWM) control chip [20]. This platform serves both as an educational tool to teach circuit design for power electronics, as well as a discrete experimental platform that provides circuits in which the proposed power monitoring method can be applied and tested. This thesis will cover the various aspects of the monitoring scheme and its experimental validation, and is structured as follows:

Chapter two presents some theoretical background on random spreading sequences and spread spectrum communications, which is needed in order to understand the nature and characteristics of the unique codes assigned to each user.

Chapter three discusses the criteria and tradeoffs in selecting the codes for the users, and presents circuits to generate and embed these codes in the current sources.

Chapter four illustrates both the design of the high side current sense amplifier circuit, corresponding to the receiver in Figure 1-3, as well as the experimental setup. The proposed nonintrusive monitoring method is experimentally tested and validated for different choices of codes.

Chapter five outlines the UC3842-based platform and its circuit blocks in full details, and serves as a teaching manual for instructors seeking to teach circuit design using this kit.

Chapter six discusses the usage of the various circuit blocks of the kit to teach modeling, control, and simulation, through a rigorous design strategy and thought process.

Finally, appendix A contains schematics and PCB designs of the circuits presented in this thesis.

Chapter 2

Random Spreading Sequences

As we described earlier, our system consists number of circuit blocks each sending information on the value of its current over a shared power-line. The information in each circuit block is encoded in a unique code. Since all circuit blocks are sending their information over the same power-line, this is analogous to different users transmitting information to the same base station in a mobile communications system. In order for the base station to be able to recover the individual information of each user from the aggregate received signal, techniques such as spread spectrum need to be employed.

Spread spectrum is a wireless communications technique that has been used for over half a century [21]. The main idea behind it is to spread the spectrum of the signal of interest to make it virtually indistinguishable from background noise. This is achieved by multiplying the signal of interest by special spreading codes/sequences that give this noise-like property to the spectrum of the result. These sequences are referred to as pseudo-random noise (PN) sequences for exactly this reason. Code division multiple access (CDMA) systems use spread spectrum techniques to serve multiple users on the same communications channel, whereby users are distinguished from one another at the receiver by each having a unique PN sequence. This mode of communications is known as *multi-user CDMA*.

This chapter will present and derive some of the basic properties of PN sequences, and will illustrate the basic operation of multi-user CDMA communications. This information will be useful for next chapter. The chapter is divided into two sections. In

section 1, the characteristics of PN sequences are stated, and their correlation properties derived. In section 2, basic principles of multi-user CDMA communications are illustrated. An important result [22] on the cross correlation properties of sequences, the Welch bound, is briefly discussed in section 3.

2.1 Properties of PN Sequences

In the scope of this thesis, only bipolar sequences are considered, i.e. sequences whose elements either be $+1$ or -1. It turns out that the effect of using bipolar waveforms is nearly the same as if purely Gaussian noise waveforms were used [21]. Consider a PN spreading sequence $c[i]$ of length N, where $0 \leq i \leq N-1$. PN sequences, which are ultimately deterministic, nearly satisfy the randomness properties of purely random spreading sequences. The properties can be readily found in the literature [21]. The ones relevant to our discussion are shown below:

- each $c[i]$ can be $+1$ or -1 with a probability of 0.5, where $0 \leq i \leq N-1$
- each $c[i]$ is independent of $c[j]$, where $0 \leq i \leq N-1$, $0 \leq j \leq N-1$, and $i \neq j$
- code family members are independent, i.e. if $c_0[i]$ and $c_1[i]$ are two random spreading sequences, then $c_0[i]$ is independent of $c_1[i]$.

The above properties lead to the following important result:

$$E\Big(c_0[i]\Big) = (+1)(0.5) + (-1)(0.5) = 0 \qquad \Longrightarrow \qquad E\Big(c_0[i]\Big) = 0, \tag{2.1}$$

where $E\Big(\ \Big)$ denotes the expectation value.

2.1.1 Autocorrelation Properties

Autocorrelation is a mathematical tool useful for finding repeating patterns in data. Examples include detecting the presence of a periodic signal obscured by noise, or identifying the missing fundamental frequency in a signal implied by its harmonic

frequencies. Essentially, it is a measure of the similarity between observations as a function of the time delay between them. Consider a random spreading sequence $c_0[i]$ of length N, where $0 \leq i \leq N-1$. The autocorrelation of the sequence, denoted by $r_{00}[k]$, is mathematically defined as follows:

$$r_{00}[k] = \frac{1}{N} \sum_{i=0}^{N-1} c_0[i] c_0[i+k] \tag{2.2}$$

It can be readily seen that $r_{00}[0]$ is 1, when $k = 0$, because $c_0^2[i] = 1$. If we evaluate the expected value of the autocorrelation for $k \neq 0$, we get:

$$E\Big(r_{00}[k]\Big) = E\left(\frac{1}{N} \sum_{i=0}^{N-1} c_0[i] c_0[i+k]\right) \tag{2.3}$$

Applying the fact that the expectation of a sum of random variables is equal to the sum of the expectations of the individual random variables, one obtains:

$$E\Big(r_{00}[k]\Big) = \frac{1}{N} \sum_{i=0}^{N-1} E\big(c_0[i] c_0[i+k]\big) \tag{2.4}$$

We also know that in the case of random sequences, $c_0[i]$ and $c_0[i+k]$ are independent (for $k \neq 0$), as was noted earlier. This means that the expectation of the product is the product of the expectations. Thus, we can write:

$$E\Big(r_{00}[k]\Big) = \frac{1}{N} \sum_{i=0}^{N-1} E\big(c_0[i]\big) \cdot E\big(c_0[i+k]\big) = 0 \tag{2.5}$$

The variance of the autocorrelation in this case is simply the square of the autocorrelation for $k \neq 0$, since the mean is zero. When $k = 0$, the variance is clearly zero. We find an expression for the variance as follows:

$$r_{00}^2[k] = \left(\frac{1}{N} \sum_{i=0}^{N-1} c_0[i] c_0[i+k]\right)^2 \tag{2.6}$$

Breaking up the product into two sums, we have:

$$r_{00}^2[k] = \left(\frac{1}{N}\sum_{i=0}^{N-1} c_0[i]c_0[i+k]\right) \cdot \left(\frac{1}{N}\sum_{j=0}^{N-1} c_0[j]c_0[j+k]\right) \tag{2.7}$$

Rearranging the product of the two sums into a double sum, one obtains the following expression:

$$r_{00}^2[k] = \frac{1}{N^2}\sum_{i=0}^{N-1}\sum_{j=0}^{N-1} c_0[i]c_0[i+k]c_0[j]c_0[j+k] \tag{2.8}$$

The expected value of the variance of the autocorrelation ($k \neq 0$) is computed as follows:

$$E\Big(r_{00}^2[k]\Big) = E\left(\frac{1}{N^2}\sum_{i=0}^{N-1}\sum_{j=0}^{N-1} c_0[i]c_0[i+k]c_0[j]c_0[j+k]\right) \tag{2.9}$$

Once again, the expectation of the sum is the sum of the expectations, therefore:

$$E\Big(r_{00}^2[k]\Big) = \frac{1}{N^2}\sum_{i=0}^{N-1}\sum_{j=0}^{N-1} E\big(c_0[i]c_0[i+k]c_0[j]c_0[j+k]\big) \tag{2.10}$$

Note that if $i \neq j$, then all the terms vanish after applying the independence of the expectation, since $E\Big(c_0[i]\Big) = E\Big(c_0[j]\Big) = 0$. Therefore, one has to deal only with the terms for which $i = j$, as follows:

$$E\Big(r_{00}^2[k]\Big) = \frac{1}{N^2}\sum_{i=0}^{N-1} E\big(c_0^2[i]c_0^2[i+k]\big) = \frac{1}{N}, \tag{2.11}$$

noting that $c_0^2[i] = c_0^2[i+k] = 1$.

One can note that as the number of bits in the sequence, i.e. the code length, increases, the expected value of the variance becomes closer and closer to zero.

2.1.2 Cross Correlation Properties

Cross correlation is a measure of the similarity of two waveforms as a function of the time delay between them. Instead of measuring the similarity of observations within one function (i.e. autocorrelation), cross correlation implies that the observations are from different functions. Consider two random spreading sequences $c_0[i]$ and $c_1[i]$, both of length N, where $0 \leq i \leq N-1$. The cross correlation between the two sequences, denoted by $r_{01}[k]$, is defined as follows:

$$r_{01}[k] = \frac{1}{N} \sum_{i=0}^{N-1} c_0[i] c_1[i+k] \tag{2.12}$$

In a similar manner to the autocorrelation derivations, one can find an expression for the expected value of the cross correlation:

$$E\Big(r_{01}[k]\Big) = E\left(\frac{1}{N} \sum_{i=0}^{N-1} c_0[i] c_1[i+k]\right) \tag{2.13}$$

Distributing the expectation operator into the sum:

$$E\Big(r_{01}[k]\Big) = \frac{1}{N} \sum_{i=0}^{N-1} E\big(c_0[i] c_1[i+k]\big) \tag{2.14}$$

Since random spreading sequences are independent of each other, i.e. $c_0[i]$ and $c_1[i]$ are independent, the expectation of their product is equal to the product of the expectations:

$$E\Big(r_{01}[k]\Big) = \frac{1}{N} \sum_{i=0}^{N-1} E\big(c_0[i]\big) \cdot E\big(c_1[i+k]\big) = 0 \tag{2.15}$$

Just as in the case of autocorrelation, the variance in this case is the square of the cross correlation. We compute the variance of the cross correlation as follows:

$$r_{01}^2[k] = \left(\frac{1}{N} \sum_{i=0}^{N-1} c_0[i] c_1[i+k]\right)^2 \tag{2.16}$$

Once again, breaking up the product into two sums, we get:

$$r_{01}^2[k] = \left(\frac{1}{N}\sum_{i=0}^{N-1} c_0[i]c_1[i+k]\right) \cdot \left(\frac{1}{N}\sum_{j=0}^{N-1} c_0[j]c_1[j+k]\right) \tag{2.17}$$

Rearranging into a double sum, we obtain:

$$r_{01}^2[k] = \frac{1}{N^2}\sum_{i=0}^{N-1}\sum_{j=0}^{N-1} c_0[i]c_1[i+k]c_0[j]c_1[j+k] \tag{2.18}$$

The expected value of the variance of the cross correlation is computed as follows:

$$E\Big(r_{01}^2[k]\Big) = E\left(\frac{1}{N^2}\sum_{i=0}^{N-1}\sum_{j=0}^{N-1} c_0[i]c_1[i+k]c_0[j]c_1[j+k]\right) \tag{2.19}$$

Distributing the expectation into the sum:

$$E\Big(r_{01}^2[k]\Big) = \frac{1}{N^2}\sum_{i=0}^{N-1}\sum_{j=0}^{N-1} E\big(c_0[i]c_1[i+k]c_0[j]c_1[j+k]\big) \tag{2.20}$$

Again, the expectation of the product is the product of the individual expectations. In addition, just like in the autocorrelation case, the terms for which $i \neq j$ vanish due to the fact that $E\Big(c_0[i]\Big) = E\Big(c_0[j]\Big) = 0$. Thus, we have:

$$E\Big(r_{01}^2[k]\Big) = \frac{1}{N^2}\sum_{i=0}^{N-1} E\big(c_0^2[i]\big) \cdot E\big(c_1^2[i+k]\big) = \frac{1}{N} \tag{2.21}$$

Table 2.1 summarizes the results obtained from the derivations of the expected autocorrelation and cross correlation as well as their variance.

2.2 Multi-user CDMA Systems

Consider a communications system that consists of two users, namely user 0 and user 1, sending information to a receiver. User 0 needs to send some number a_0 to the receiver, and user 1 needs to send some number a_1. Note that typically, CDMA

Table 2.1: Summary of correlation properties of random spreading sequences

Parameter	**Result**
$E\Big(r_{00}[k]\Big)$	0
$E\Big(r_{00}^2[k]\Big)$	$1/N$
$E\Big(r_{01}[k]\Big)$	0
$E\Big(r_{01}^2[k]\Big)$	$1/N$

systems are discussed in the contxt of digital communication techniques. Thus, a_0 and a_1 would be waveforms consisting of modulated digital information bits. In this thesis, we do not have this assumption, but the analysis remains the same. In CDMA communication systems, each user is assigned a unique code (a spreading sequence) that is known to the receiver. Let us denote the codes for user 0 and user 1 as $c_0[n]$ and $c_1[n]$, respectively, where each code has length N, and $0 \leq n \leq N-1$. In CDMA systems, users share the same channel and the same bandwidth. Thus, the transmitted signal is essentially a multiplexed signal containing information from both users:

$$\underbrace{x[n]}_{\substack{\text{transmitted}\\ \text{signal}}} = \underbrace{a_0 c_0[n] + a_1 c_1[n]}_{\text{multiplexed signal}} \tag{2.22}$$

In order to simplify the analysis, let us analyze the case where the only noise source to the channel is additive white Gaussian noise (AWGN). In this case, the received signal $y[n]$ has the following form:

$$y[n] = a_0 c_0[n] + a_1 c_1[n] + w[n], \tag{2.23}$$

where $w[n]$ is the term due to the AWGN.

Suppose the receiver needs to recover the information sent by user 0. The receiver will need to reverse the spreading that was done by $c_0[n]$. This is done by correlating the received signal with the spreading code of interest, $c_0[n]$ in this case. This is done as follows:

$$r_{y0} = \frac{1}{N}\sum_{n=0}^{N-1} y[n]c_0[n] \tag{2.24}$$

Substituting in the expression for $y[n]$ into the equation yields:

$$r_{y0} = \frac{1}{N}\sum_{n=0}^{N-1} a_0 c_0[n]c_0[n] + \frac{1}{N}\sum_{n=0}^{N-1} a_1 c_1[n]c_0[n] + \frac{1}{N}\sum_{n=0}^{N-1} w[n]c_0[n] \tag{2.25}$$

Taking the constants outside the sums and simplifying, one obtains:

$$r_{y0} = \frac{a_0}{N}\sum_{n=0}^{N-1} c_0^2[n] + a_1\left(\frac{1}{N}\sum_{n=0}^{N-1} c_1[n]c_0[n]\right) + \omega \tag{2.26}$$

We recognize that the sum in the second term is equal to the cross correlation between $c_0[n]$ and $c_1[n]$. Denoting the noise term on the right by ω and simplifying the expression further yields:

$$r_{y0} = \underbrace{a_0}_{\substack{\text{desired}\\ \text{information}}} + \underbrace{a_1 r_{01}[0]}_{\substack{\text{multi-user}\\ \text{interference}}} + \underbrace{\omega}_{\text{noise}} \tag{2.27}$$

We see that the result is a combination of three terms, which include the desired information a_0, a term due to interference from user 1, and a noise term due to the AWGN. Ideally, we desire the other two terms to be negligible compared to a_0.

An important figure of merit to consider here is the ratio of the signal power to the interference-plus-noise power, known as the *signal-to-interference-plus-noise ratio* (SINR). Let us look at the statistical means and variances of each of these terms and compute their power, in order to obtain an expression for SINR:

- ***Desired information:***

  This is a deterministic quantity, and thus $E(a_0) = a_0$, and $E(a_0^2) = a_0^2$.

- ***Multi-user interference:***

  The mean of this term can be found as follows:

$$E\Big(a_1 r_{01}[0]\Big) = a_1 E\Big(r_{01}[0]\Big) = 0 \tag{2.28}$$

  Computing the variance gives:

$$E\Big(a_1^2 r_{01}^2[0]\Big) = a_1^2 E\Big(r_{01}^2[0]\Big) = \frac{a_1^2}{N}. \tag{2.29}$$

- ***Noise:***

  We compute the mean of the noise term as follows:

$$E\left(\omega\right) = \frac{1}{N}\sum_{n=0}^{N-1} E\big(w[n]c_0[n]\big) = \frac{1}{N}\sum_{n=0}^{N-1} E\big(w[n]\big)\cdot E\big(c_0[n]\big) = 0 \tag{2.30}$$

  The variance of ω is computed using the following equation:

$$E\left(\omega^2\right) = E\left(\frac{1}{N^2}\sum_{n=0}^{N-1}\sum_{m=0}^{N-1} w[n]c_0[n]w[m]c_0[m]\right) \tag{2.31}$$

  The terms for which $n \neq m$ are all 0 because different white noise samples are independent. Thus, we have:

$$E\left(\omega^2\right) = \frac{1}{N^2}\sum_{n=0}^{N-1} E\big(w^2[n]\big)\cdot E\big(c_0^2[n]\big) = \frac{\sigma_w^2}{N}, \tag{2.32}$$

  where σ_w^2 denotes the variance of the noise.

Now we are ready to find the expression for the SINR as follows:

$$\text{SINR} = \frac{E\left(a_0^2\right)}{\frac{a_1^2}{N} + \frac{\sigma_w^2}{N}} = \frac{a_0^2}{a_1^2 + \sigma_w^2} \times N \tag{2.33}$$

In general, when k users are present, the expression can be generalized as follows:

$$\text{SINR} = \frac{p_0}{\sigma_w^2 + \sum_{i=1}^{k} p_i} \times N, \tag{2.34}$$

where p_i denotes the signal power of the i-th user. The code length N is referred to as the *spreading gain*. An important thing to notice here is that as code length increases, the multi-user interference term decreases as well as the AWGN term:

$$\lim_{N\to\infty} \frac{p_i}{N} = \lim_{N\to\infty} \frac{\sigma_w^2}{N} = 0 \tag{2.35}$$

Therefore, the SINR can be made arbitrarily large by increasing the code length.

2.3 The Welch Bound

If we look back at equation (2.27), we notice that the interference term depends on the information signal of the other user as well as on the cross correlation between the spreading code of that user with that of the user of interest, namely user 0. The result is similar in the case of more than two users. Therefore, if one can design spreading sequences whose cross correlation values are zero, then one can completely eliminate the interference from other users. Codes that are strictly orthogonal, i.e. that have zero cross correlations between each other, generally need to be synchronized with each other. However, many CDMA systems, such as the ones used in mobile communications, have no synchronization between the users and the base station. This means that the spreading codes need to have zero cross correlations between each other for any arbitrary phase shift. Unfortunately, it is not possible to design such codes for most practical applications when several users need to communicate.

The reason for this is the existence of the Welch bound. Given a set of M sequences (which in the proof are complex), each of length N, and norm of 1, it can be shown that when $M > N$, there is a lower bound on the maximum value of the inner product

of any two sequences in the set [22]:

$$c_{\max} \geq \sqrt{\frac{M-N}{N(M-1)}} \tag{2.36}$$

The process of taking the correlation between two sequences is similar to taking the inner product. Each correlation value is the inner product of the shifted sequence and the other sequence.

We will show in the next chapter that for a very small number of users, one can simply use square waves whose fundamental frequencies are even multiples of each other. Such square waves exhibit the property of being shift orthogonal, i.e. they have zero inner product/correlation for any arbitrary phase shift between the two sequences due to their symmetry.

Chapter 3

Selection and Generation of Codes

In an ideal situation, we require that the multi-user interference terms which appear during the process of recovering the currents from individual users (i.e. circuit blocks), and which happen to be equal to the cross correlations between the codes, to be exactly zero. It was shown in chapter 2 that random sequences exhibit this property in a statistical sense (the expectation of the cross correlations was found to be 0). In practice, we seek to use pseudo-random noise (PN) sequences, which imitate the characteristics of random sequences, as was mentioned in the previous chapter. These PN sequences can be used to both encode the value of the current flowing in a circuit block, as well as spread the spectrum of this information in frequency-domain. This method allows us to employ the techniques of CDMA communications systems to recover the individual circuit block currents with minimal interference from the other blocks.

The choice of the type of sequences to be used for encoding will significantly affect the performance of the power monitoring method. Different codes have different correlation properties, and this will directly manifest as an error in the recovered data.

Section 1 of this chapter presents a criterion for the selection of codes, discusses two possible choices of codes that can be used, namely square wave signals and Gold sequences, and presents some of their key properties. Section 2 presents the hardware techniques required to implement the sequences. A circuit that generates Gold

sequences in hardware is also presented, along with the simulation and experimental results.

3.1 Code Selection

Figure 3-1 shows a general scenario where M circuit blocks need to send current information over the same power-line. The i-th circuit block sends its value of the current α_i, and is assigned a unique code $s_i(t)$. The transmitted data from each user is of the form $\alpha_i s_i(t-\tau_i)$, where τ_i is the time delay specific to that circuit block. The fact that each block has its own delay τ_i means that the perturbations of different circuit blocks are not synchronized with each other, which makes the method more realistic.

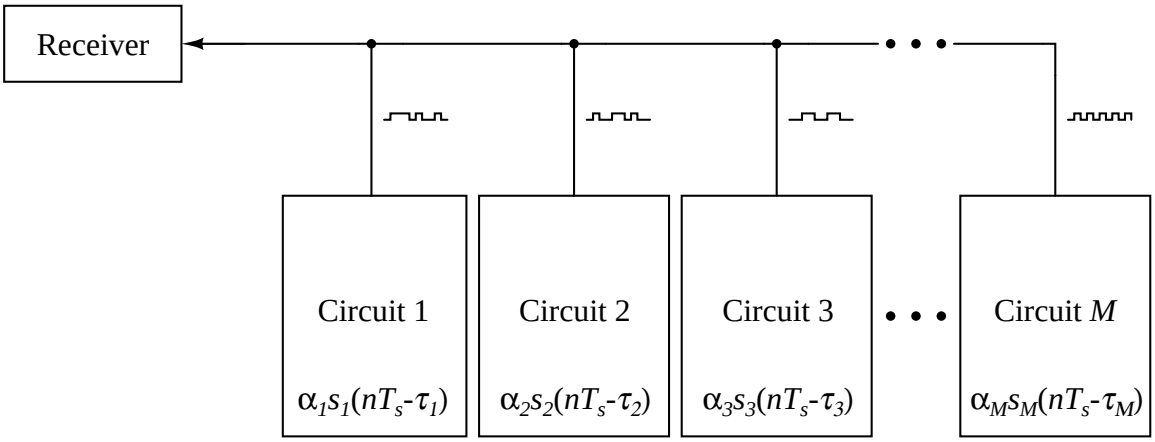


Figure 3-1: A schematic drawing of the different users transmitting their data over the power-line.

If we denote the received and sampled data by $r[n]$, we have:

$$r[n] = \sum_{i=1}^{M} \alpha_i s_i(nT_s - \tau_i), \tag{3.1}$$

where n denotes the sample number, and T_s denotes the sampling period. Suppose we need to extract α_j from the received data samples $r[n]$. Just as was done in equation (2.24) in chapter 2, we correlate $r[n]$ with $s_j[n]$, which is a sampled and synchronized version of $s_i(t)$. Phase synchronization can be performed through signal processing

by sweeping the circular phase shift and picking the one that yields the maximum correlation. This assumes that the power of the signal of interest is larger than the noise and interference power. If we ignore the noise term and consider only the effect of interference from the other blocks, we obtain:

$$r_{rj} = \alpha_j r_{jj} + \sum_{i \neq j}^{M} \alpha_i r_{ij} \tag{3.2}$$

If the selected codes have zero cross correlations with $s_j[n]$, then we have:

$$\alpha_j = \frac{r_{rj}}{r_{jj}}, \tag{3.3}$$

which is the data point we needed to extract.

If the code sequences used are bipolar, i.e. their values can be either $+1$ or -1, then the autocorrelation term r_{jj} is 1, and therefore:

$$\alpha_j = r_{rj} \tag{3.4}$$

3.1.1 Criterion for Code Selection

In practice, it is not possible to find a family of codes whose cross correlations vanish for all arbitrary phase shifts τ_i and that can accommodate a large number of users. It was shown in chapter 2 that for a set of M sequences each of length N, there is a lower bound on the maximum possible cross correlation when $M > N$. Thus, in practice, the non-zero cross correlation terms appear as noise on the value of the current to be recovered, known as multiple access interference (MAI).

However, if one relaxes the requirement of zero cross correlations, and allows for some percentage error K, then one can form a useful criterion for choosing codes that are appropriate for the application. Thus, we can write:

$$r_{rj} = \underbrace{\alpha_j r_{jj}}_{\text{detect}} + \underbrace{\sum_{i \neq j}^{M} \alpha_i r_{ij}}_{\text{error}} \tag{3.5}$$

If we require the term to be detected $\alpha_j r_{jj}$ to be A times larger than the error term, where A is some positive number, then we have:

$$\alpha_j r_{jj} = A \sum_{i \neq j}^{M} \alpha_i r_{ij} \tag{3.6}$$

This will result in the following expression for r_{rj}:

$$r_{rj} = \left(1 + \frac{1}{A}\right) \alpha_j r_{jj} \tag{3.7}$$

Rearranging the equation to solve for α_j, we have:

$$\alpha_j = \left(\frac{1}{1 + 1/A}\right) \cdot \frac{r_{rj}}{r_{jj}} \tag{3.8}$$

If A is large, and we define K to be $1/A$, then we see that the non-zero cross correlation terms result in some percentage error K during the recovery of α_j:

$$\alpha_j \approx \left(1 - \frac{1}{A}\right) \cdot \frac{r_{rj}}{r_{jj}} = (1 - K) \cdot \frac{r_{rj}}{r_{jj}} \tag{3.9}$$

From this analysis, and from equation (3.6) in particular, we deduce the following condition on the cross correlation of the codes, which will result in an error of at most K percent:

$$\alpha_{j,min} r_{jj} \geq A \sum_{i \neq j}^{M} \alpha_{i,max} r_{ij} \tag{3.10}$$

In other words, we require that the minimum value of the term to be detected $\alpha_{j,min} r_{jj}$ be at least A times larger than the largest possible value of the error term. Rearranging the equation, and substituting K for $1/A$, we obtain the following criterion:

$$\sum_{i \neq j}^{M} \frac{\alpha_{i,max}}{\alpha_{j,min}} \cdot \frac{r_{ij}}{r_{jj}} \leq K \tag{3.11}$$

Note that the K error factor can also take into account the contributions of other

noise sources as well.

3.1.2 Square Wave Signals as Codes

Square wave signals are not random signals, and they do not possess the properties of PN sequences discussed earlier. However, a class of square wave signals exhibit the powerful property of being shift orthogonal, which makes them ideal for our application.

Consider two signals $s_1(t)$ and $s_2(t)$ that are square waves with amplitudes of 1, and fundamental frequencies ω_0 and $M\omega_0$, respectively, where M is some real number. We would like to show that under certain conditions on M, the cross correlation between the two signals is zero for any arbitrary phase shift between them.

We start by noting that the cross correlation between the two continuous-time signals $s_1(t)$ and $s_2(t)$ is given by:

$$r_{s_1,s_2}(t) = \int_{-\infty}^{\infty} s_1(\tau) s_2(t+\tau)\, d\tau \tag{3.12}$$

It should also be noted that this is equivalent to the linear convolution between $s_1(-t)$ and $s_2(t)$:

$$r_{s_1,s_2}(t) = \int_{-\infty}^{\infty} s_1(-\tau) s_2(t-\tau)\, d\tau = s_1(-t) \star s_2(t) \tag{3.13}$$

This result is useful, as now we can resort to frequency-domain analysis to find an expression to the cross correlation, and then use the inverse Fourier transform to obtain the time-domain expression if needed. Let us assume that there is some delay t_0 on $s_2(t)$ relative to $s_1(t)$. The square waves can be expanded in a Fourier series as follows:

$$s_1(t) = \sum_{\substack{n \\ \text{odd}}} \frac{4}{n\pi} \sin(n\omega_0 t) \tag{3.14}$$

$$s_2(t) = \sum_{\substack{k \\ \text{odd}}} \frac{4}{k\pi} \sin\Big(kM\omega_0 (t - t_0)\Big) \tag{3.15}$$

We need to evaluate the convolution given in equation (3.13) in frequency-domain. It is well-known in signal processing that the Fourier transform of the convolution of two functions, $s_1(-t)$ and $s_2(t)$ in this case, is the product of the Fourier transforms of the functions $s_1(-t)$ and $s_2(t)$ [23]. We use the Fourier series expressions obtained above to compute the Fourier transforms of the signals $s_1(-t)$ and $s_2(t)$. Denoting the Fourier transform operator by $\mathcal{F}$, we have:

$$s_1(-t) = -\sum_{\substack{n \\ \text{odd}}} \frac{4}{n\pi} \sin(n\omega_0 t) \qquad \xrightarrow{\mathcal{F}} \qquad -\sum_{\substack{n \\ \text{odd}}} j\frac{4}{n}\Big[\delta(\omega + n\omega_0) - \delta(\omega - n\omega_0)\Big] \tag{3.16}$$

$$s_2(t) = \sum_{\substack{k \\ \text{odd}}} \frac{4}{k\pi} \sin\Big(kM\omega_0(t - t_0)\Big) \qquad \xrightarrow{\mathcal{F}} \qquad \sum_{\substack{k \\ \text{odd}}} j\frac{4}{k}\Big[\delta(\omega + kM\omega_0) - \delta(\omega - kM\omega_0)\Big]e^{-j\omega t_0} \tag{3.17}$$

The product of the Fourier transforms is given as follows:

$$\sum_{\substack{n \\ \text{odd}}}\sum_{\substack{k \\ \text{odd}}} \frac{16}{nk}\Big[\delta(\omega + n\omega_0) - \delta(\omega - n\omega_0)\Big]\Big[\delta(\omega + kM\omega_0) - \delta(\omega - kM\omega_0)\Big]e^{-j\omega t_0} \tag{3.18}$$

The terms will all be zero unless the arguments of the delta functions are equal, which occurs when $M = \pm n/k$. Therefore, when this condition is not satisfied, all the terms in the product of the Fourier transforms are zero, and the two square wave signals $s_1(t)$ and $s_2(t)$ are orthogonal for any arbitrary phase shift/time delay t_0 between them. Thus, the condition for $s_1(t)$ and $s_2(t)$ to be shift orthogonal is given by:

$$M \neq \pm\left(\frac{n}{k}\right), \qquad \text{(for any odd } n \text{ and } k) \tag{3.19}$$

An example is given below, where this condition is tested on a 400 Hz and a 1 kHz signal. In this case, $M = 2.5 = 5/2$. Since M is not a ratio of two odd integers, the condition for shift orthogonality given in equation (3.19) is satisfied, and we expect the cross correlation to be 0 for any shifts in the sequences. Figure 3-2 shows a plot of the cross correlation value versus the shift. The shift orthogonality condition is

clearly satisfied.

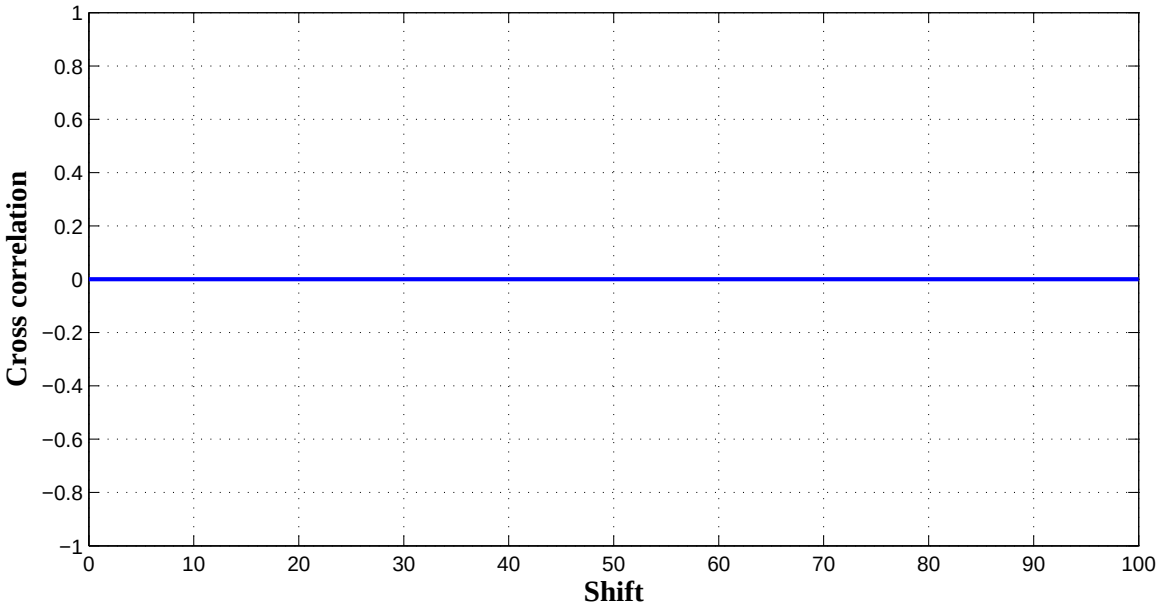


Figure 3-2: Cross correlation between a 400 Hz signal and a 1 kHz square wave signal.

We also expect the product of the frequency spectra of both signals to be zero. In other words, the individual frequency components should never overlap. The result is shown in Figure 3-3, and it is clear that none of the harmonics overlap.

3.1.3 Gold Sequences

An important and widely used family of PN sequences are Gold sequences [24], which form a large class of sequences with relatively low and bounded cross correlations between the sequences.

The Gold sequences have the property that the cross-correlation between any two sequences of the family takes on one of three values, regardless of the phase shift between them [25]. Gold sequences of length $N = 2^n - 1$ are defined by a pair of sequences known as *preferred pairs*, and the only three possible correlation values r_{ij}

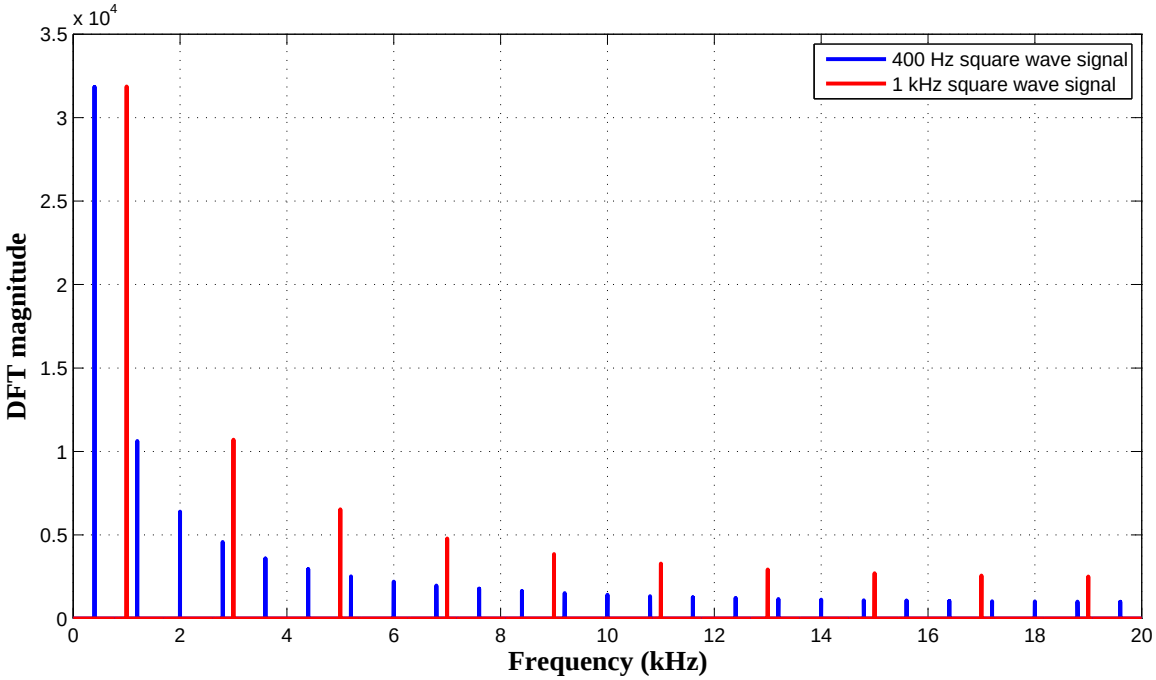


Figure 3-3: Frequency spectra of a 400 Hz signal and a 1 kHz square wave signal.

between any two Gold sequences can be shown to be [1]:

$$r_{ij} = \{-t(n),\ -1,\ t(n) - 2\}, \tag{3.20}$$

where $t(n)$ is given by:

$$t(n) = \begin{cases} 1 + 2^{(n+1)/2} & \text{if } n \text{ is odd} \\ 1 + 2^{(n+2)/2} & \text{if } n \text{ is even} \end{cases}$$

An example showing the 3-valued cross correlation property between two 31-length Gold sequences is shown in Figure 3-4. Since $N = 31$, and thus $n = 5$, the three values of the cross correlation according to the above equation are -9, -1, and 7. This can be observed in the plot.

[1]Note that the correlation values shown here are not normalized by N as in the definitions used in this thesis. However, this un-normalized definition is still used in order to be consistent with the literature on Gold sequences.

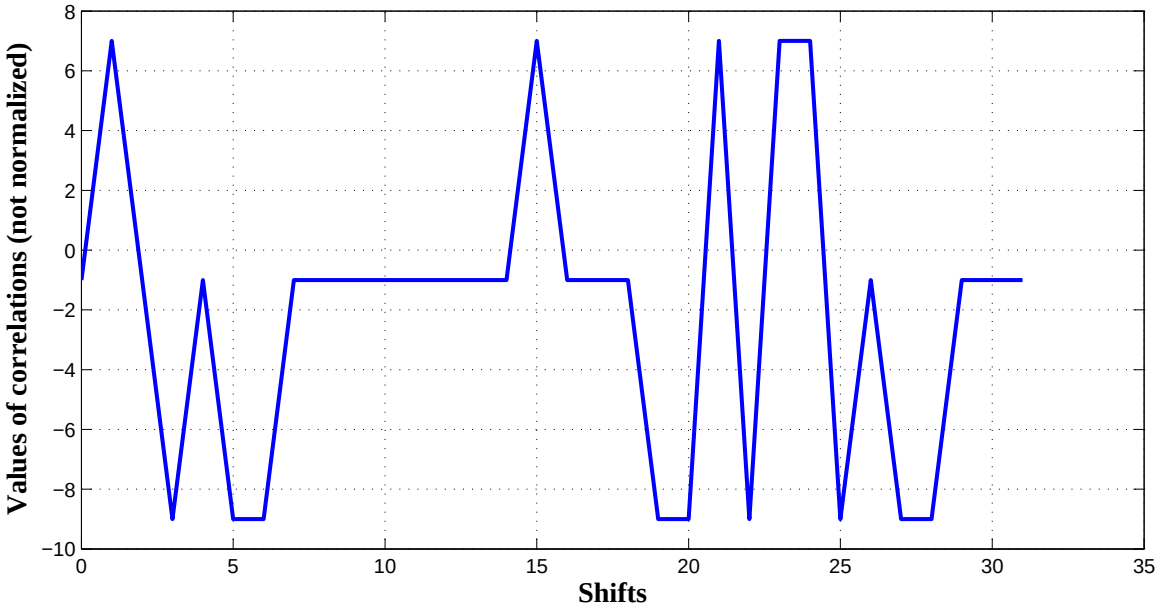


Figure 3-4: Plot of the cross correlation values of two 31-length Gold sequences.

3.2 Code Generation

As mentioned earlier, the Gold codes are defined by a preferred pair of sequences. To be able to encode and spread the information, circuitry that generates the codes needs to be designed and implemented.

3.2.1 M-sequence Generation

Numerous long sequences can be generated using shift registers with feedback connections through XOR gates. These are known as linear feedback shift registers (LFSR). It can be shown [21] that sequences generated using LFSR are periodic with a period P of at most $2^n - 1$. Thus,

$$P \leq 2^n - 1 \tag{3.21}$$

A special class of these LFSR sequences achieves the maximum possible period of $2^n - 1$, corresponding to equality in the above equation. These sequences are known as *maximal length sequences* (m-sequences), and are characterized by what is known as *characteristic polynomials*. The properties and the mathematical theory behind

these sequences are beyond the scope of this thesis; references such as [21] can be consulted for further details. However, it suffices to know that the preferred pair of sequences used to produce the Gold sequence belongs to the class of m-sequences. Once an m-sequence is given, its characteristic polynomial is well-known, and the coefficients of that polynomial can be used to construct a circuit to generate this m-sequence. An example of an m-sequence generator circuit is shown in Figure 3-5.

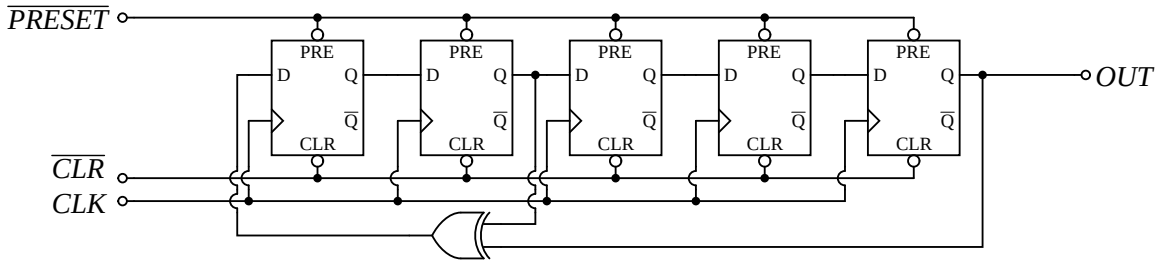


Figure 3-5: Circuit schematic of the m-sequence generator using linear feedback shift registers.

3.2.2 Gold Sequence Generation

Given two m-sequences of length N (i.e. periodic with period N) that form a preferred pair, then $(N+2)$ Gold sequences can be generated by performing an XOR operation on the outputs of the m-sequence generators. Different Gold sequences can be generated by circularly shifting one of the m-sequences with respect to the other, and so each phase lag between the two m-sequences generates a Gold sequence. If we denote the preferred sequences by u and v, then the generated Gold sequences are defined by:

$$G(u,v) = \{u, v, u \oplus v, u \oplus Tv, u \oplus T^2v, \cdots, u \oplus T^{N-1}v\}, \tag{3.22}$$

where $\oplus$ denotes the XOR operator, and T denotes a a left circular shift by 1. The phase shift can be performed using feedforward terms. Figure 3-6 illustrates this concept. The top five shift registers can be seen to have the same connections as the ones in Figure 3-5; they generates the first m-sequence in the preferred pair. The bottom registers generate the second m-sequence in the preferred pair. Changing the

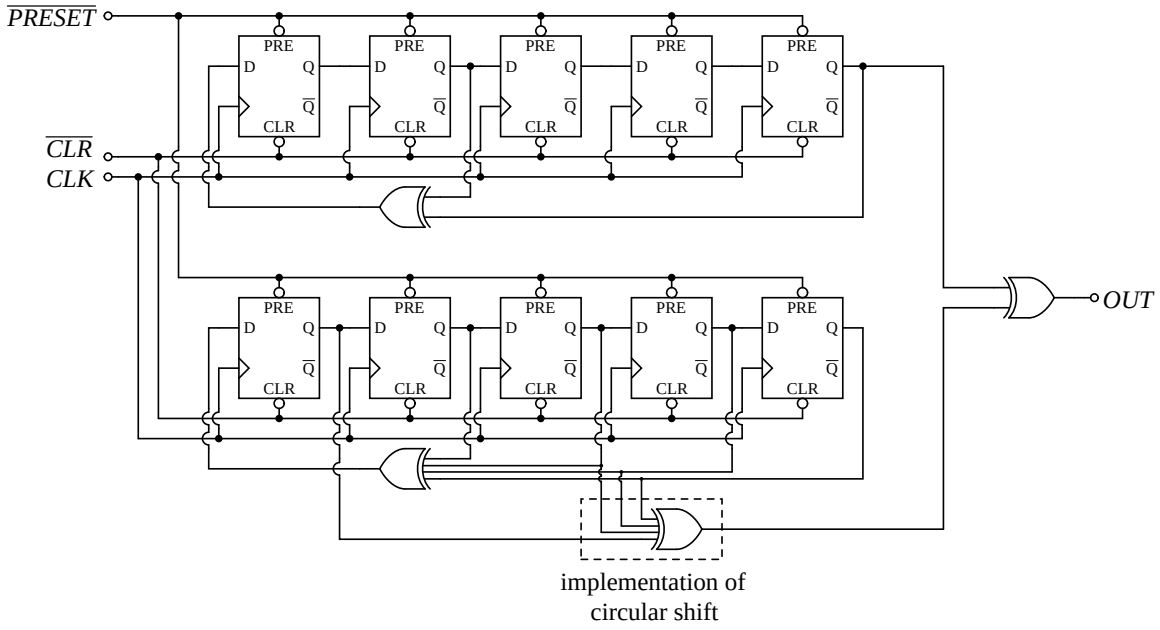


Figure 3-6: Circuit schematic of the Gold code generator. The bottom m-sequence generator produces a circularly shifted m-sequence, which results in a Gold sequence when XOR'ed with the top m-sequence.

feedforward connections to the bottom XOR gate changes the phase shift between the top and bottom m-sequences. The outputs of both m-sequence generators are fed to the output XOR gate on the right to produce the Gold codes.

Note that if the initial values of the registers are all zero, then the circuit is stable in the trivial zero state, and no sequences will be generated. For this reason, at least one of the registers needs to be initialized with a nonzero value for the circuit to be useful. Different initial values can generate different m-sequences. In this case, the $\overline{PRESET}$ signal can be used to initialize all the registers to 1 before the sequences are generated.

A SPICE transient simulation was performed on the circuit, and the result is shown in Figure 3-7.

A prototype was also built to illustrate the generation of this specific Gold sequence. The result is shown in Figure 3-8. Notice that in all the sequence generators, the clock signal CLK plays an important role in the overall system performance, since it directly affects the spectral content of the sequences. All our analysis in this thesis assumes no frequency errors in the clocks at the users' side, which means that

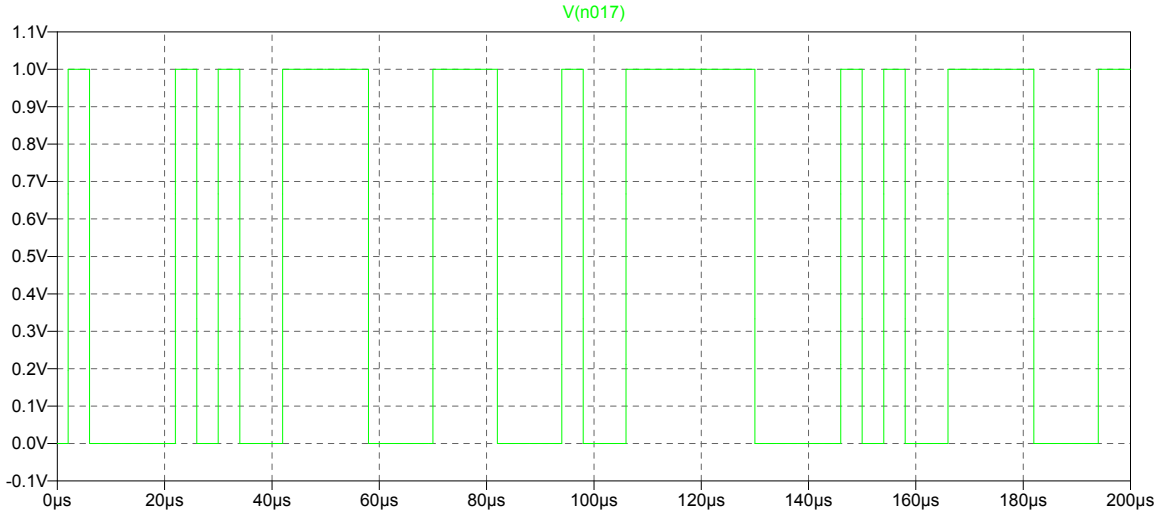


Figure 3-7: Result of a SPICE simulation showing the generation of a Gold sequence.

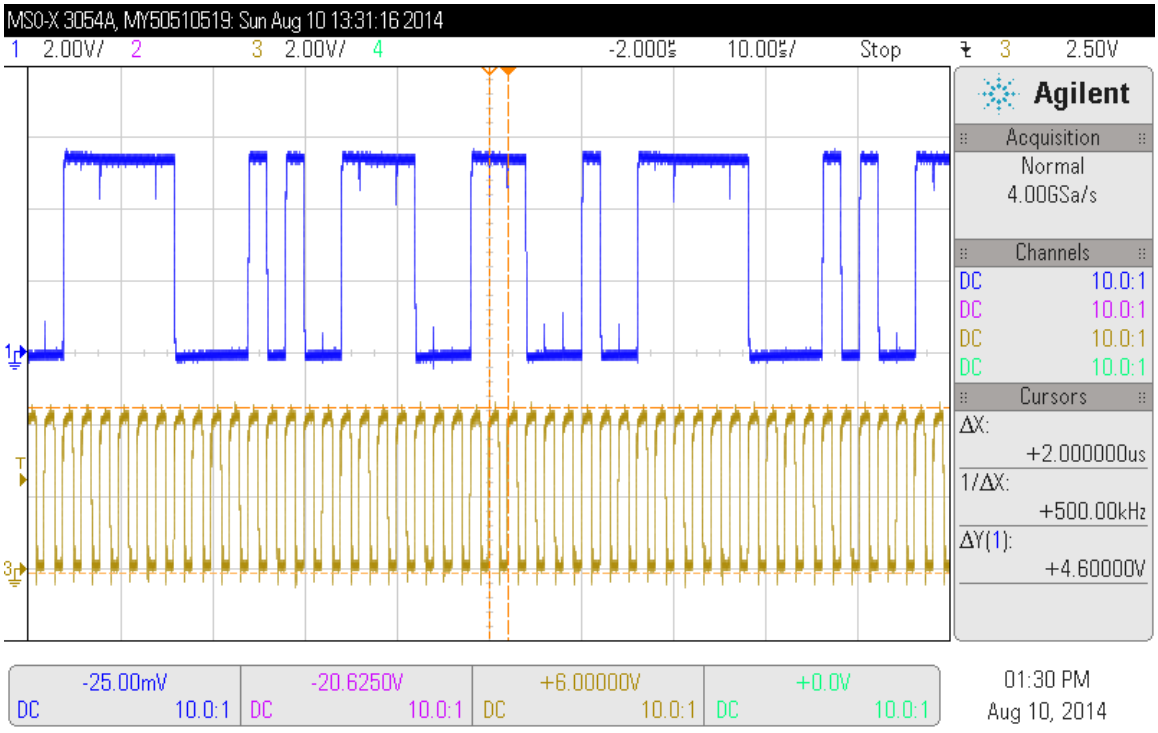


Figure 3-8: Experimental result showing a Gold sequence generated at the output of the circuit.

the autocorrelation of the sequence of interest is precisely the expected value. In our prototype, the clock was implemented using a ring oscillator composed of inverters connected in a feedback configuration, with the RC time constants of the resistors and capacitors setting the clock frequency.

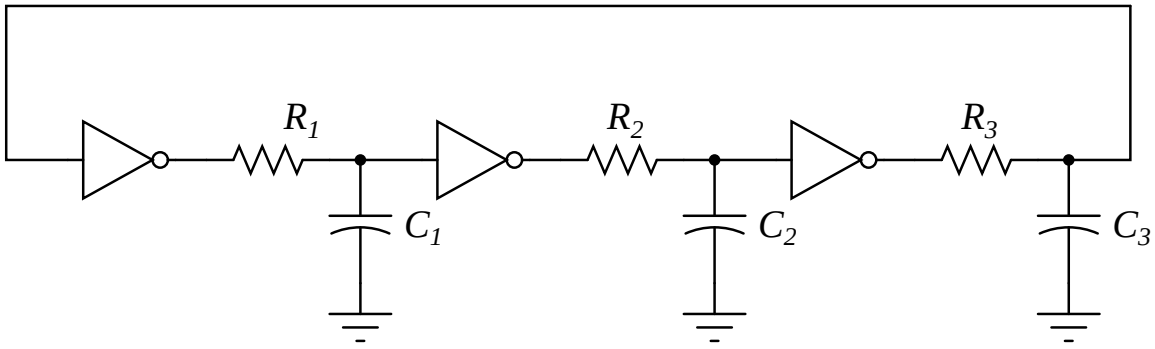


Figure 3-9: Generation of a clock signal using a ring oscillator circuit.

Figure 3-10 shows the effect of a frequency error on the values of autocorrelation for four different Gold sequences, normalized to the case when there is no error. It can be seen that the autocorrelation value is in fact sensitive to an error in the clock frequency. The clock needs to be accurate to within ±1.5% for the autocorrelation to be off by about 20%.

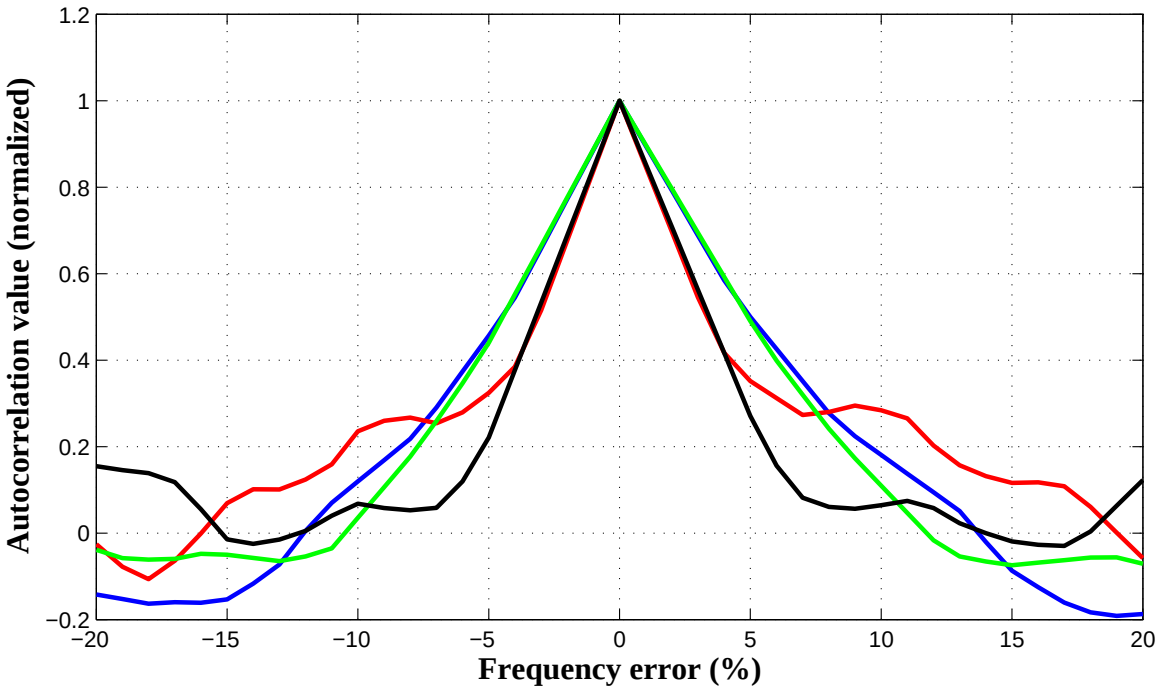


Figure 3-10: The effect of clock frequency error on the autocorrelation values of different 31-length Gold codes. The values are normalized with respect to the case with no error.

Chapter 4

Experimental Demonstration and Results

So far we have presented the types of sequences that will be used to encode the information of the different users, as well as circuits to generate these sequences. Now, we wish to test the current monitoring method by having actual users, i.e. circuit blocks that are running and performing their own tasks, current encoders that perturb the currents using the codes, as well as a receiver circuit through which the power-line signal flows. We seek to monitor the quiescent currents flowing through the circuit blocks by perturbing their currents using the code generators presented in the previous chapter. The circuit blocks are chosen to be modules from a discrete version of the UC3842 current-mode power electronic controller [5, 20]. Figures 4-1 and 4-2 show a high level schematic drawing of the controller and a an overview of its modules, respectively.

The details of the circuits in this discrete platform are presented in the next chapter. Here, we seek to use circuit blocks from the platform as users, to test the monitoring strategy.

Section 1 presents the designs of the current encoder circuit and the receiver circuit. Section 2 presents the experimental setup and results obtained when square wave signals were used as the codes for the users. Section 3 presents the setup and the results when Gold sequences were used. Finally, section 4 suggests some ideas for

future work on this topic.

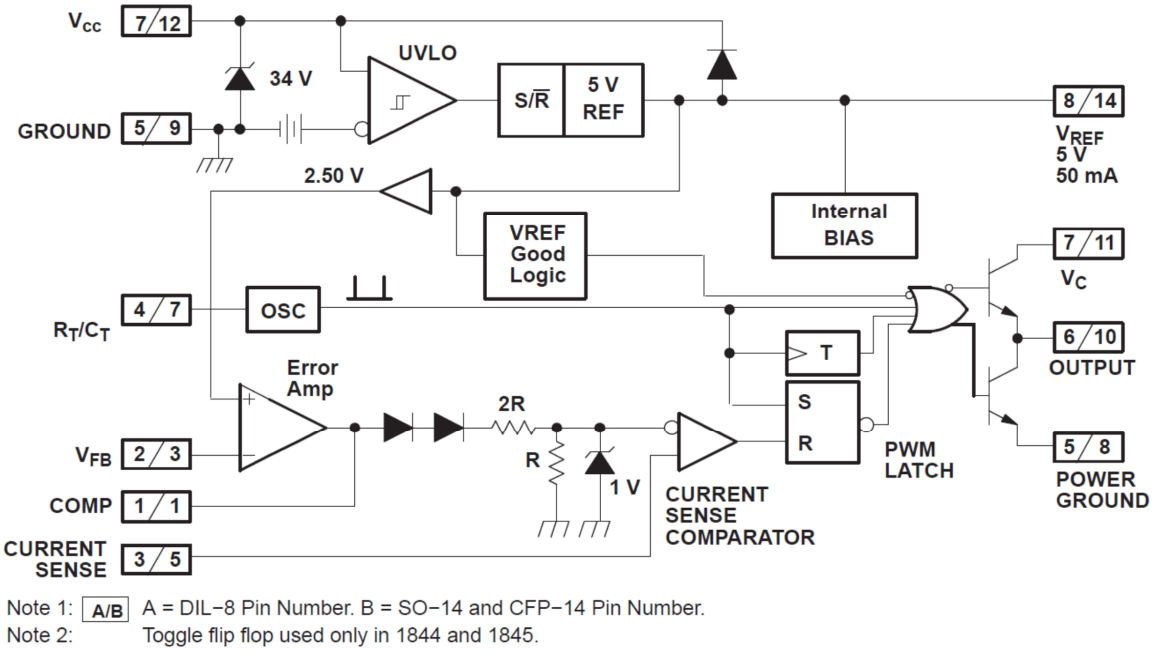


Figure 4-1: High level schematic drawing of the controller.

4.1 Encoder and Receiver

We need to encode the value of the quiescent current on the ac amplitude of the perturbations. This means that the ac current perturbations i_{ac} need to be a function of the bias current I_{bias}, i.e. $i_{ac} = f(I_{bias})$. The encoder circuit presented here results in a linear function between the two currents.

The total ac perturbations from the different users need to be sensed on the power-line bus, amplified to a reasonable level beyond the signal-to-noise ratio, and then sampled for signal processing.

4.1.1 Current Encoder

One implementation of the current encoding method can be integrated into already-existing current mirrors in the circuit blocks, as shown in Figure 4-3. When the switch is closed, both sides of the current mirror have equal degeneration resistors, assuming

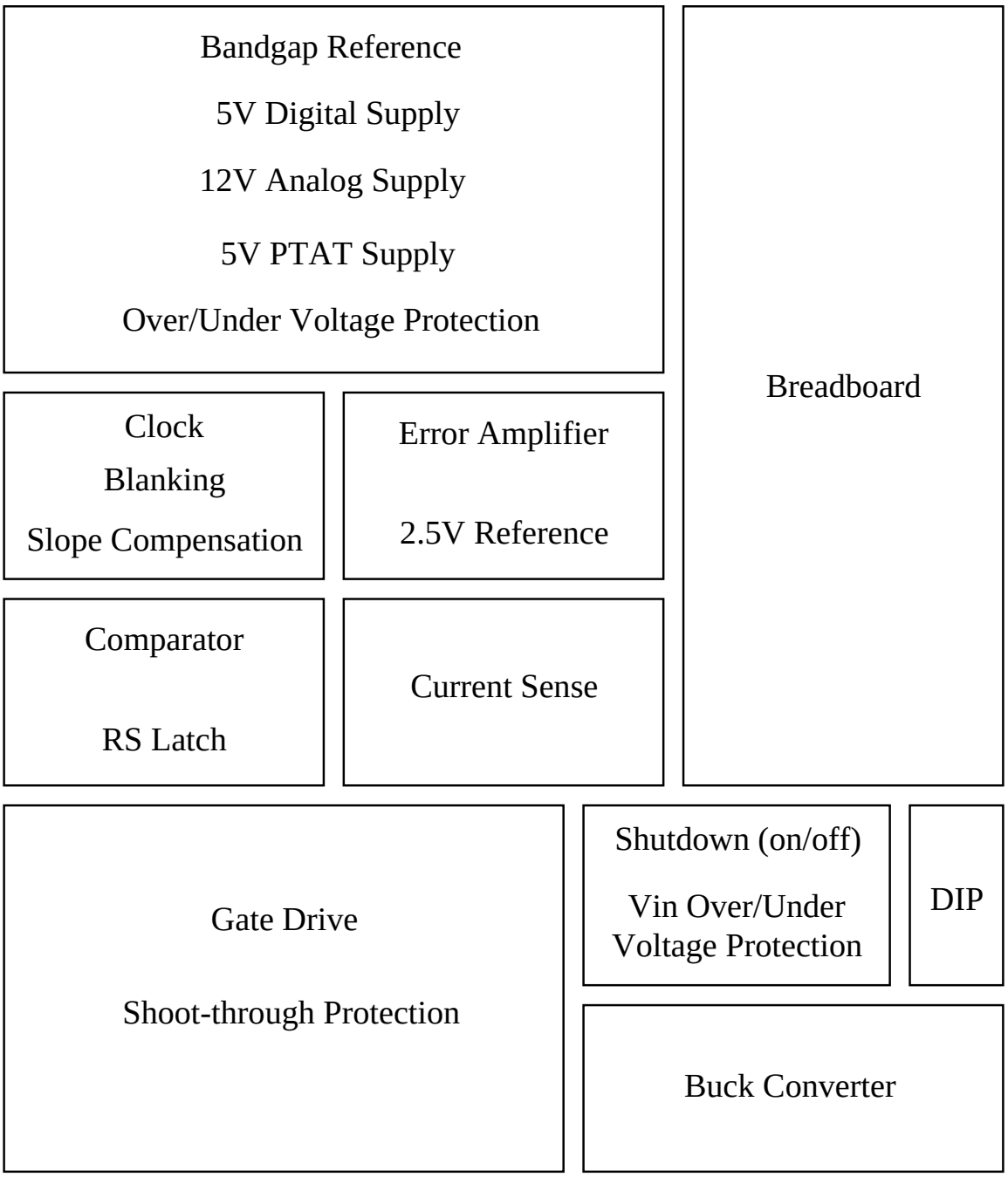


Figure 4-2: Various modules of the controller.

negligible switch on-resistance. Thus, the currents on both sides are equal to the bias current flowing during normal operation of the circuit. Therefore, denoting the current flowing through the circuit block when the switch is closed by I_{closed}, we have:

$$I_{closed} = I_{bias} \tag{4.1}$$

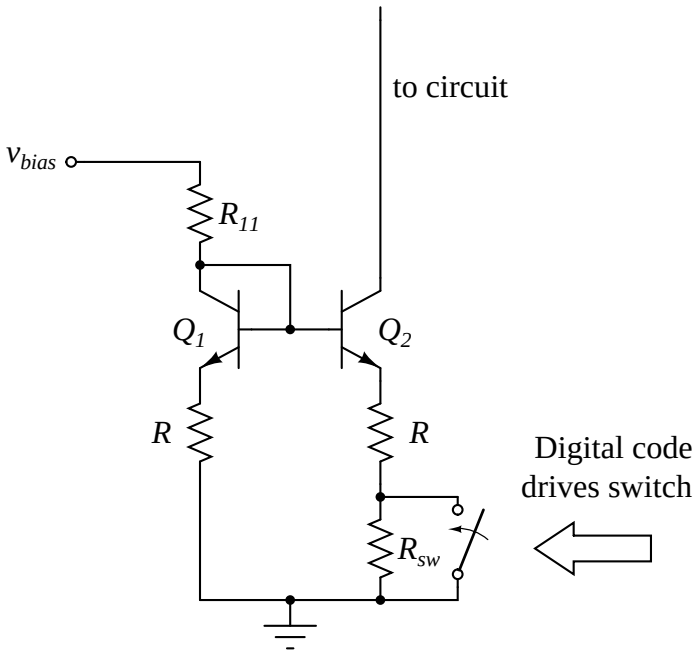


Figure 4-3: Current encoder circuit. The timings of the current perturbations are controlled by the digital sequence driving the switch.

When the switch is open, the right leg of the current source has a resistance $R + R_{sw}$. The current on the left leg is still I_{bias}, but the current on the right I_{open} is no longer equal. Noting that the base-emitter voltage of both transistors is around 0.6 V, and applying Kirchhhoff's voltage law (KVL) on the bottom loop, we have:

$$I_{bias}R = I_{open}\left(R + R_{sw}\right) \tag{4.2}$$

Rearranging the equation to solved for I_{open}, we obtain:

$$I_{open} = \left(\frac{R}{R + R_{sw}}\right) I_{bias} \tag{4.3}$$

This action creates ac perturbations on the quiescent current flowing through the circuit block. The peak-to-peak value of this current i_{ac} is simply equal to the difference between I_{closed} and I_{open}:

$$i_{ac} = I_{closed} - I_{open} = I_{bias} - \left(\frac{R}{R + R_{sw}}\right) I_{bias} \tag{4.4}$$

Simplifying, we get:

$$i_{ac} = \left(\frac{R_{sw}}{R + R_{sw}} \right) I_{bias} \tag{4.5}$$

This means that the ac perturbations are linearly proportional to the quiescent bias current flowing through the circuit block. The constant of proportionality is solely determined by the resistor being switched R_{sw} and the degeneration resistor R. The magnitude of the ac perturbations needs to be much smaller than the magnitude of the current I_{bias}, and the ratio of the resistors can be used to control that magnitude, depending on how much variation in bias current the circuit block can tolerate. Thus, typically, $R_{sw} \ll R$.

It is important to note that the use of resistors in degeneration in circuit blocks is assumed due to the fact that the experimental work is being done on a discrete platform of the UC3842 chip, which will be explained in the next chapter. In practical integrated circuits, resistors are not typically used for transistor matching. Instead, the dimensions of the transistors are matched appropriately to provide the mirroring ratio. In that case, the same principle can be applied, and another transistor that is relatively smaller in dimension can be switched on and off in parallel. The constant of proportionality between i_{ac} and I_{bias} is therefore determined by the ratios of the transistor dimensions.

4.1.2 High Side Current Sensor

Figure 4-4 shows the high side current sensor circuit. It consists of a sense resistor R_{sense} placed in series with the power-line bus feeding the circuit blocks, followed by two gain stages. Thus, the full current going to the blocks also flows through the sense resistor. For this reason, the sense resistor needs to be as small as possible, in order to minimize the power dissipation as well as the voltage drop across it. However, since the small ac current perturbations, which appear as an ac voltage across R_{sense}, need to be amplified for processing, the size of the resistor needs to be large enough. The choice of the value of R_{sense} is application dependent. For example, in applications

where the voltage drop across the resistor can be tolerated, the size of R_{sense} can be increased to amplify the ac voltage across it.

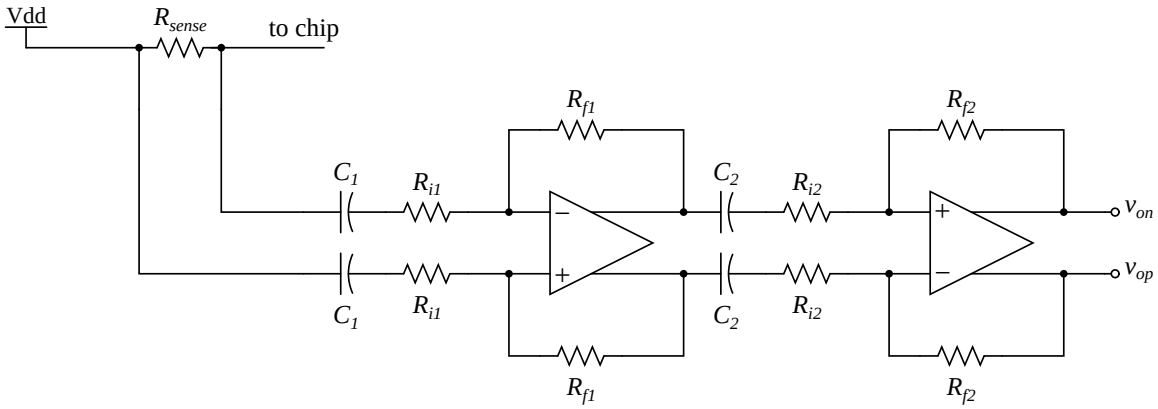


Figure 4-4: High side current sense circuit.

The gain stages need to amplify the ac voltage at the proper bandwidth. The dc voltage across R_{sense} should not be amplified, since it is the ac voltage that we intend to measure. In addition, the dc voltage is relatively larger than the ac component because it results from the total current flowing through R_{sense}. For this reason, a high pass characteristic is selected. The differential output $v_{o,d} = v_{op} - v_{on}$ is given by:

$$\frac{v_{o,d}}{v_{sense}} = \frac{s^2 R_{f1} R_{f2} C_1 C_2}{(sR_{i1}C_1 + 1)(sR_{i2}C_2 + 1)} \tag{4.6}$$

where v_{sense} is the voltage across the sense resistor R_{sense}. It can be seen that this configuration results in two zeros at the origin. In addition, the frequencies of the two poles are given by:

$$f_{pole,1} = \frac{1}{2\pi R_{i1} C_1}, \qquad f_{pole,2} = \frac{1}{2\pi R_{i2} C_2} \tag{4.7}$$

The ac component of v_{sense} that needs to be amplified is given by:

$$v_{sense,ac} = R_{sense} i_{ac} = R_{sense} \left(\frac{R_{sw}}{R + R_{sw}} \right) I_{bias} \tag{4.8}$$

If R_{sense} is chosen to be $0.1\,\Omega$, and if the resistor ratios result in a factor of 0.1

Table 4.1: Summary of component values used in the high side current sensor design

Component	**Value**
R_{sense}	$0.1\,\Omega$
R_{i1}	$10\,\Omega$
R_{i2}	$1\,k\Omega$
R_{f1}	$10\,k\Omega$
R_{f2}	$10\,k\Omega$
C_1	$1\,\mu\,\mathrm{F}$
C_2	$0.01\,\mu\,\mathrm{F}$

(resulting in a 10% perturbation), then a 1 mA bias current would be encoded as a $10\,\mu$V ac voltage. The gain of the amplifier needs to be large enough to get the voltage to a level that can be sampled and processed. We chose this gain to be 10,000. This gain is split into two stages, the first providing a gain of 1000, and the second providing a gain of 10.

If we place both poles at around 16 kHz, we get a wideband amplifier that provides 80 dB amplification within the passband. The values that are chosen are given in Table 4.1.

Figure 4-5 shows the result of a SPICE simulation of the current sense circuit. Beyond about 9 MHz, the poles of the amplifier circuit start to show up and reduce the gain.

The current sense circuit was built as shown in Figure 4-6. The ISL55210 chip was used to implement the amplifier. The result of the bandpass characteristic was verified experimentally. The gain of the circuit was measured for a wide range of frequencies, and is shown in Figure 4-7. Note that the input referred noise of the circuit under this configuration is close to 12 μV. This sets the minimum value of the smallest detectable ac voltage $v_{sense,ac}$.

The amplifier, however, suffers from a problem with the common-mode input voltage. If there is a common-mode step at the inputs of the amplifier beyond about 25 mV, the amplifier saturates and goes unstable, and takes time to settle back to

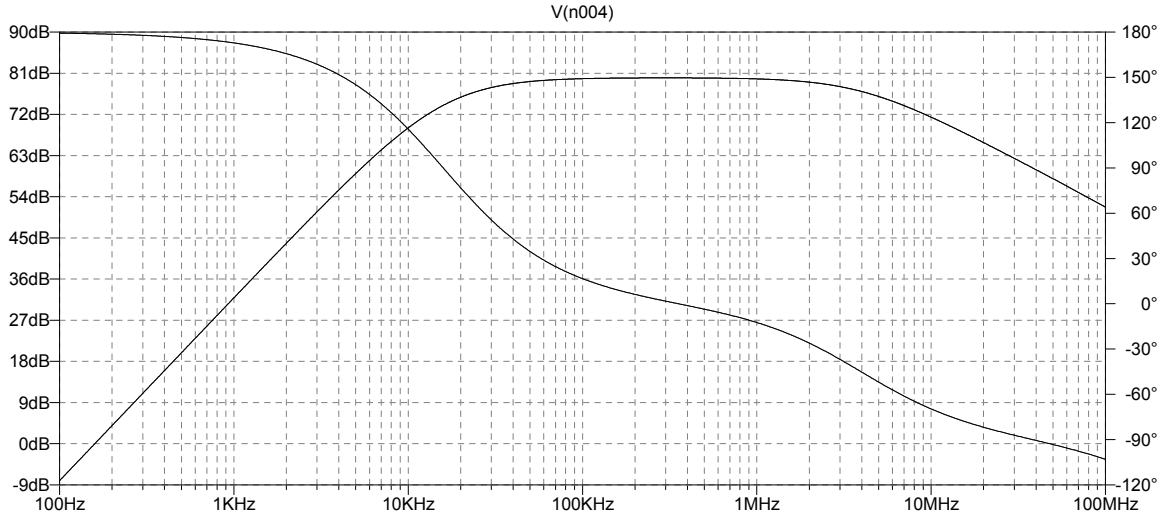


Figure 4-5: Simulation showing the frequency response of the high side current sensor.

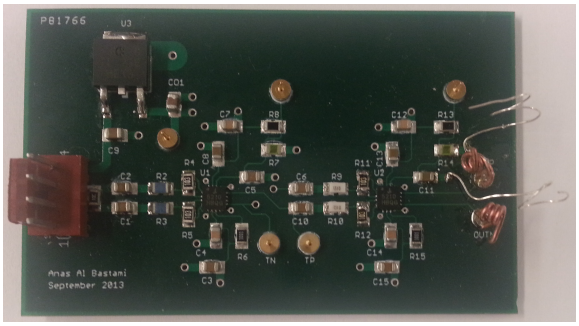


Figure 4-6: High side current sense board.

its normal mode of operation. We suspect that the problem is due to a narrow input common-mode range. In Figure 4-8, the result of a common-mode step up of about 50 mV is shown. It can be seen that it takes the output about 1.4 ms to recover back from saturation. The higher the magnitude of the common-mode step-up, the longer it takes for the amplifier to recover from saturation. This effect will show up in the results of section 4.3, when circuit blocks are instantly shut down.

4.2 Experiment with Square Waves as Codes

Now that the infrastructure for our current monitoring method is available, i.e. code generators, circuit blocks, current encoders, and a current sensor, we can start experimenting with data transmission over the power-line bus. The first experiment was

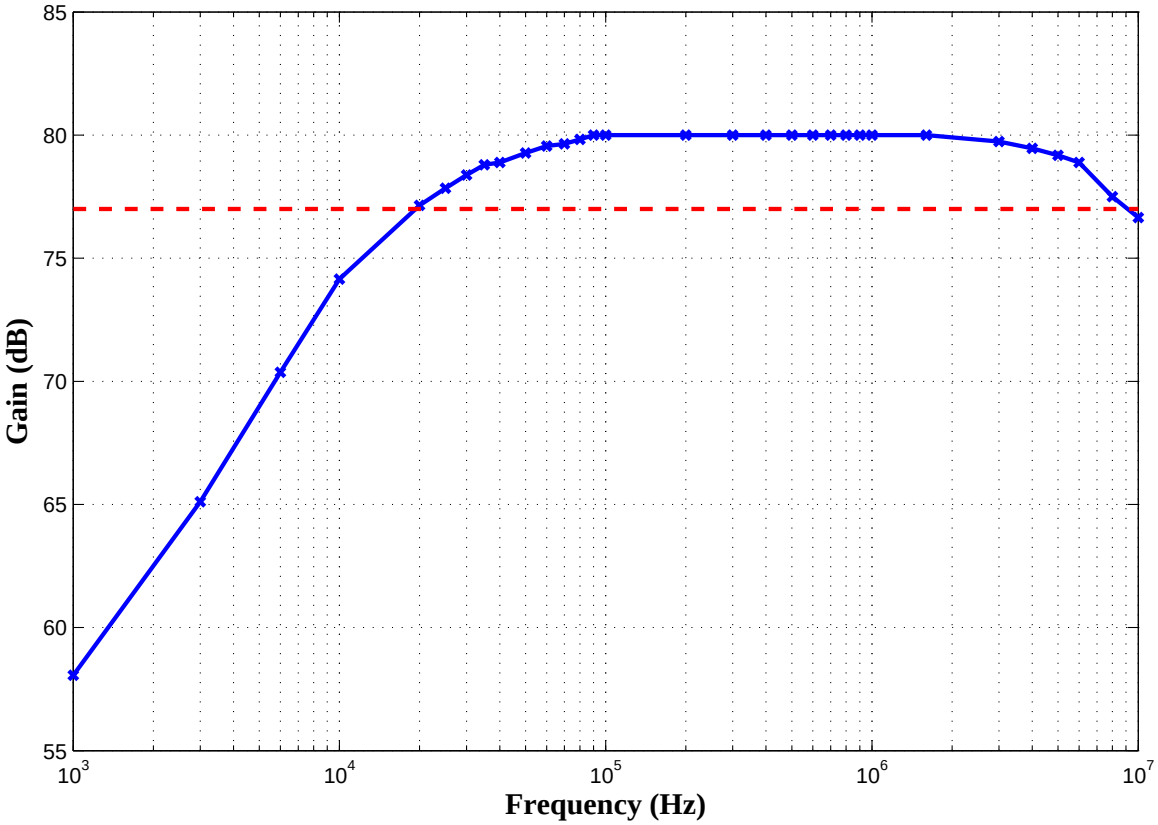


Figure 4-7: Bandpass characteristic of the high side current sense receiver circuit.

carried out using square wave signals as the unique sequences assigned to the users.

4.2.1 Experimental Setup

Recall from the previous chapter that when the fundamental frequencies of the square wave signals are chosen appropriately, one can obtain signals that have zero cross correlations for any arbitrary phase shifts between them. This is important, since it will result in no interference between the two users.

We chose 250 kHz and 500 kHz square wave signals to encode the data from the users. The square wave signals were generated using an FPGA module through an easy-to-use programmable interface shown in Figure 4-9, and the current encoder which was illustrated in Figure 4-3 was implemented on the breadboard. The switch was implemented using a simple 2N7000 signal level N-MOSFET. Figure 4-10 shows the full experimental setup.

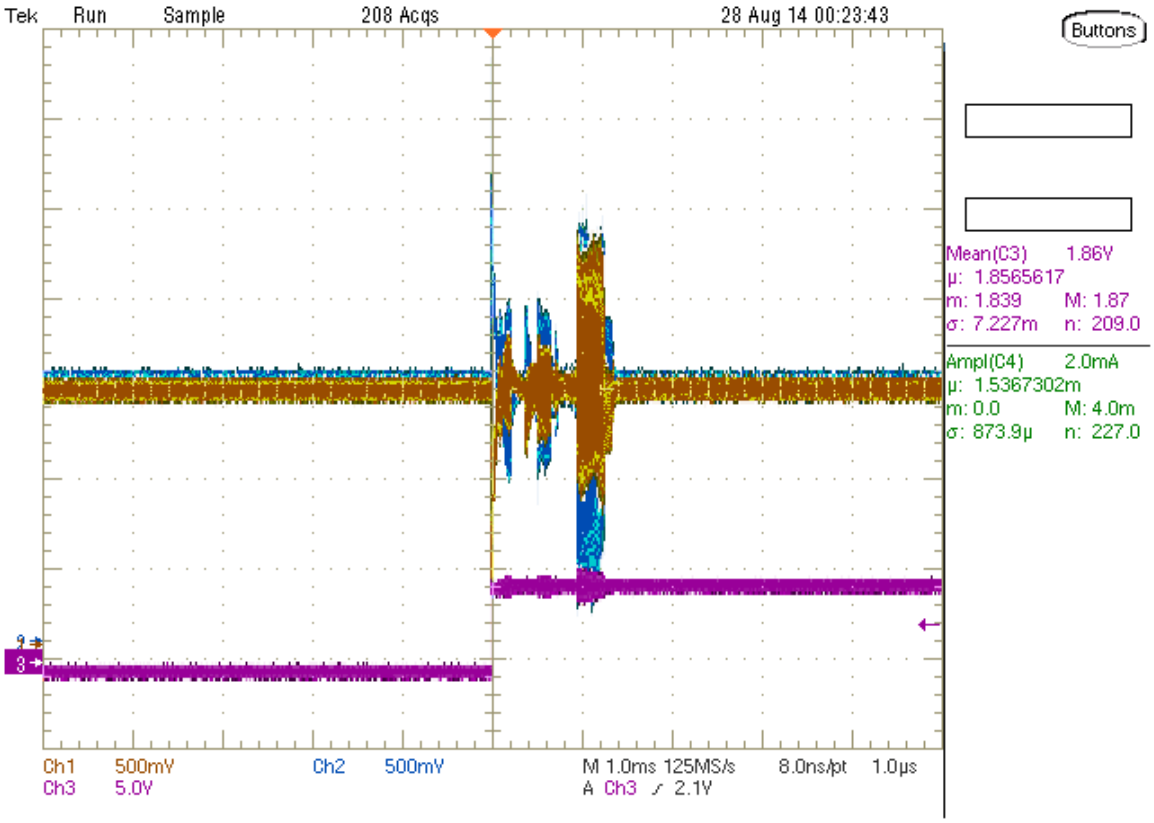


Figure 4-8: Result of a 50 mV step up in the common-mode voltage. The output takes about 1.4 ms to recover from saturation.

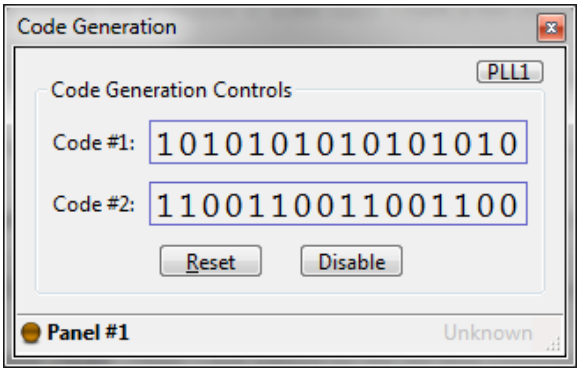


Figure 4-9: FPGA code generation interface.

In order to demonstrate the viability of the monitoring method, the bias currents in both circuit blocks were made to vary in a controllable way. This was done by driving the bias voltages of the current sources using a signal generator, thereby causing the bias currents to vary accordingly. One of the circuit blocks was biased with a 200 Hz sinusoidal current, and the second block was biased with a 200 Hz

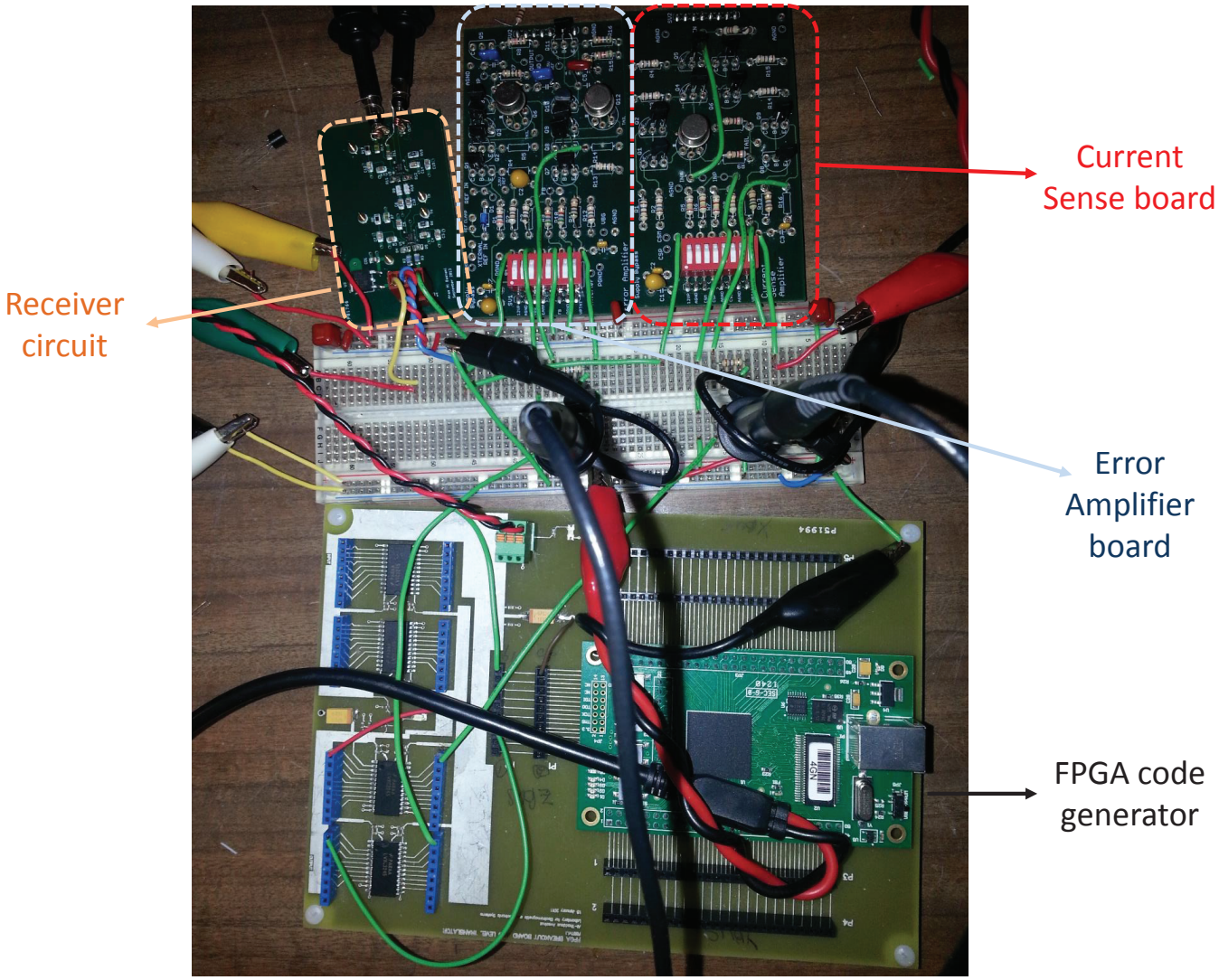


Figure 4-10: Full experimental setup showing two circuit blocks, the code generator, and the receiver circuit.

burst signal current.

4.2.2 Results

The output of the receiver circuit was observed on the oscilloscope, and was sampled using the scope's internal analog to digital converter. The highest-frequency signal in this experiment was the 500 kHz square wave signal. Thus, to ensure that enough samples are available for signal processing, the sampling rate was set to 25 MSamples/second.

After the data was collected, it was loaded onto MATLAB for processing. Since the sampling frequency was 25 MSamples/second, this means that there are 100 samples in each period of the 250 kHz square wave signal, and 50 samples in each period of the 500 kHz signal. After these signals are synthesized in MATLAB, the received data is organized into overlapping sets of 100 samples, i.e. 1-100, 2-101, 3-102, etc. Each of these sets is correlated with both of the synthesized square signals, and the maximum correlation value for every 100 sets is stored. The result is shown in Figure 4-11.

It can be seen that the method is able to recover the individual currents of the circuit blocks by only measuring the total current flowing through the power-line bus.

4.3 Experiment with Gold Sequences as Codes

The next experiment was performed using Gold sequences as the unique codes assigned to each user. The circuits used to generate these sequences were illustrated in the previous chapter.

Before carrying out the experiment, a SPICE simulation with four circuit blocks was performed as a first pass test to the use of Gold sequences for power monitoring. In a similar manner as the experimental setup when square wave signals were used, each bias current was made to vary in a certain pattern, and the total current was sampled and exported to MATLAB for processing. After the correlations were performed, the results are shown in Figure 4-12. Random arbitrary phase shifts between the different Gold codes were introduced. The results indicate that the recovered currents track the actual currents flowing through the circuit blocks. It can be seen that the phase shifts in the codes can directly affect the accuracy of the results; this is a direct result of the non-zero cross correlations. In this simulation, the result from code 1 shows an offset between the expected and recovered currents.

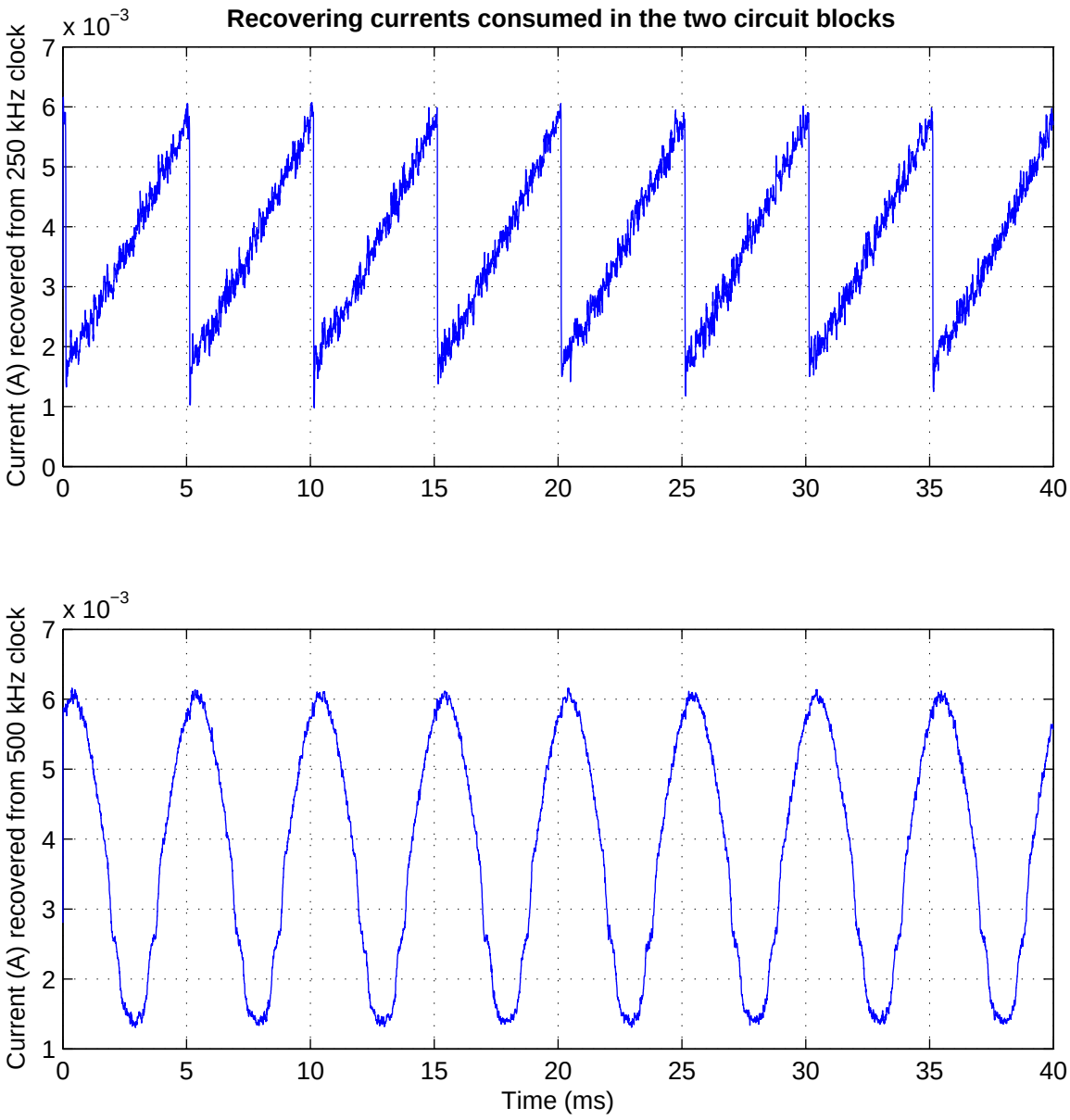


Figure 4-11: Result showing the recovered currents in the two circuit blocks.

4.3.1 Experimental Setup

Now, we wish to demonstrate the ability of the current monitoring method to detect transients in the quiescent currents, such as a turn-on or a turn-off transient. Integrated circuits can sometimes have a "shutdown" mode of operation, in which certain circuit blocks are disabled. Therefore, this experiment involves a turn on or a turn off being enforced on one or more circuit blocks. 31-length Gold sequences were used to encode the values of the currents. For purposes of this experiment, and

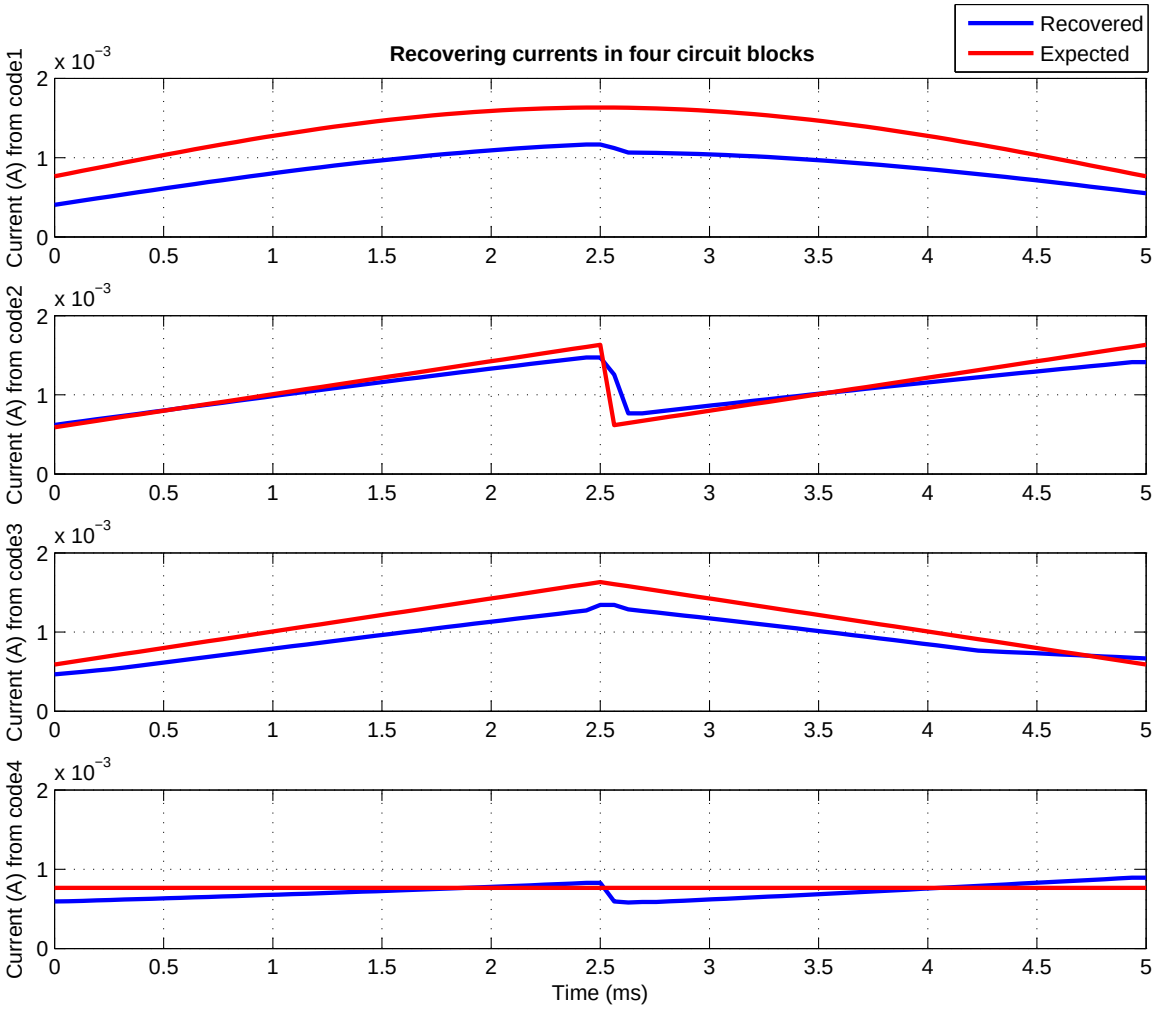


Figure 4-12: A first pass test simulation result showing currents recovered from four circuit blocks with Gold sequences as the codes. The currents clearly match to within an offset that results due to interference.

for easy embedding into the current sources of the circuit blocks to be monitored, a microcontroller was used to generate the Gold sequences. The bit frequency was set to 1 MHz to ensure that the spectral components of the sequences are within the passband of the receiver amplifier given in Figure 4-7. The Gold sequences used were selected from the four codes whose spectra are shown in Figure 4-13.

We first start with the simplest case, when a shutdown is enforced on a single circuit block, which was chosen to be the low side gate drive block from the UC3842 discrete platform (see next chapter). In the normal mode of operation, the circuit

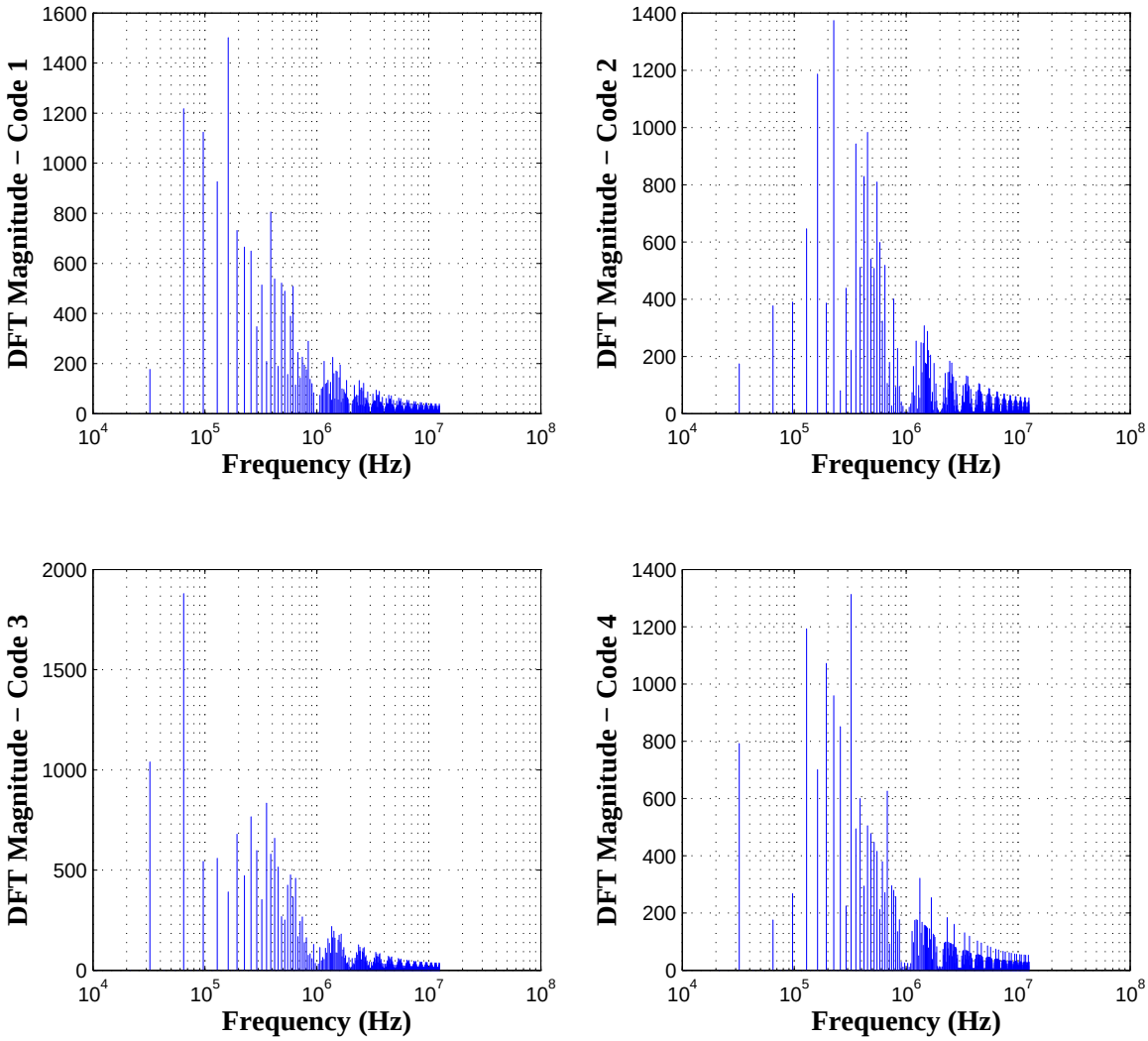


Figure 4-13: Spectral content of several Gold sequences. The first three are selected for the experiment.

block runs with a 5 mA quiescent current. When the circuit is in shutdown mode, we expect the current to drop to zero.

The next stage of the experiment involves repeating the same shutdown procedure, but this time two other circuit blocks are added. In this case, a current of about 5 mA flows through the block that will be shut down, and the other two blocks also carry a current of 5 mA each. We expect the nonzero cross correlations to cause interference between the different recovered currents. The effect this has on the detection of shutdown will be shown.

Next, we again repeat the same procedure, but we introduce several turn on and

turn off events in the low gate drive circuit block, instead of just a single shutdown.

In order for the current monitoring method to be valid, we expect that a turn on or a turn off event in one block must not affect the recovered current of the other blocks. To verify this, we introduce a turn on and a turn off event in one block, along with a turn on and a turn off event in another block. We time the events in the two blocks such that they do not overlap with each other, and we observe the recovered currents. The last case we investigate is when one of the events in the two blocks occurs during another event in the other block, i.e. for example, a circuit block is turned off a little after the other block is turned off. The third circuit block is kept on in all of these cases.

4.3.2 Results

Figure 4-14 shows the result of the experiment when a single circuit block sends its current information, encoded with a Gold sequence, over the power-line. Note that the process of recovering the current using the correlation method does not assume any knowledge of the timing of the sequence. The blue plot shows the result using this method. In this particular experiment, the synchronized sequence was also stored, and the current was recalculated (the red plot) using this synchronized sequence, so that we can compare the current resulting from the correlation method to the value of the current that we should expect. We can see that the two currents are almost identical. As expected, the current is around 5 mA before the shutdown is enforced. The current drops to zero after the shutdown. The step in current resulting from an instantaneous shutdown causes the high side current amplifier, i.e. receiver circuit, to saturate, resulting in the first peak shown at around 20 ms. However, another peak is observed about 2 ms after the shutdown. This results from the amplifier circuit recovering from saturation due to the common-mode step, so it takes 2 ms for the amplifier to return back to its normal mode of operation, as was illustrated in Figure 4-8.

Since we already know that the amplifier is in saturation between the peaks, we can use a median filter to observe the true step in the value of the current. Figure

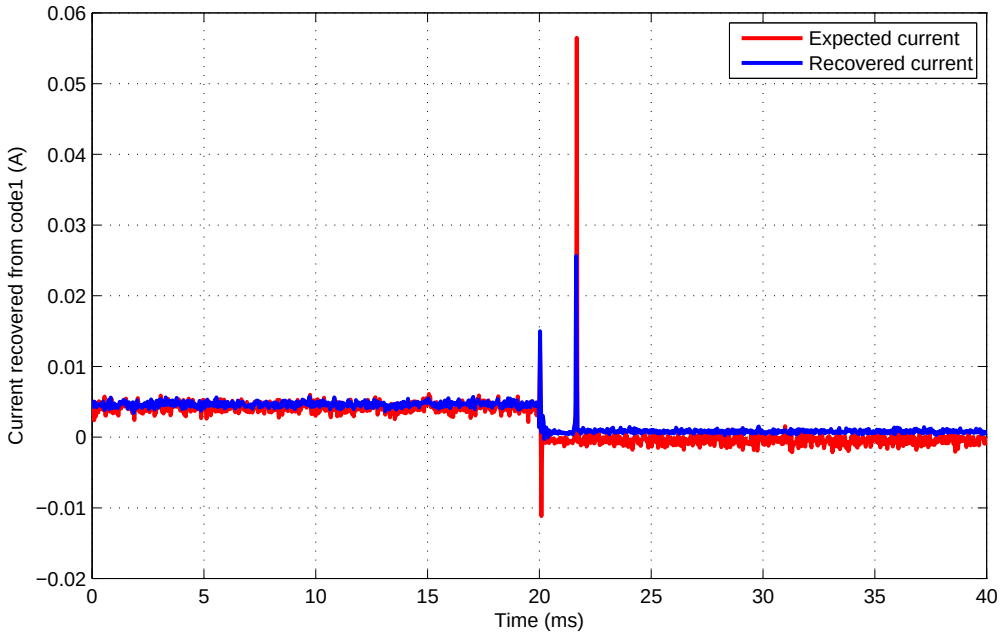


Figure 4-14: Result showing the decoded current value during a shutdown event.

4-15 shows the filtered waveform.

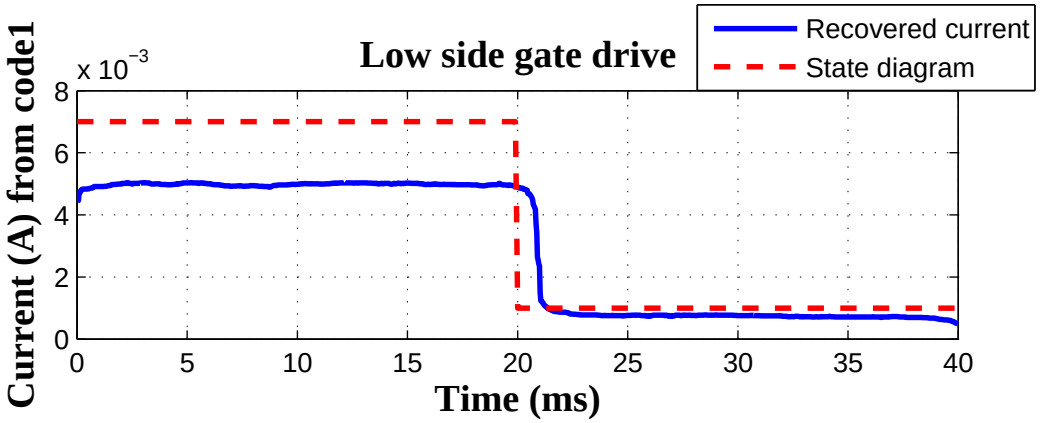


Figure 4-15: Result showing the decoded current value during a shutdown event after a median filter has been applied. The state diagram indicates when the block is on (high) or off (low).

One can observe from Figure 4-15 that there is an offset close to 0.8 mA even though the circuit block is turned off as indicated by the state diagram. This is a consequence of the decoding algorithm used to recover the currents, which is similar in principle to that explained in section 4.2. Since there is no synchronization between

the code generating circuits and the receiver, the algorithm correlates the received data with locally generated Gold sequences in MATLAB, and picks the maximum correlation values. When the circuit block is in shutdown mode, the only data that is being measured is noise. The algorithm will therefore pick the maximum values of the cross correlations of noise with the Gold sequence, which result in the offset shown in Figure 4-15.

When the low side gate drive was off, the root-mean-square (rms) noise was measured to be around 67 mV. The noise bandwidth is around 9 MHz, as can be deduced from the bandpass characteristic of the amplifier, which was shown in Figure 4-7. Since the Gold sequence bit frequency is 1 MHz, and the length of the sequence is 31 bits, the bandwidth of the recovered data is (1/31) MHz (because the algorithm computes an average every one period of the sequence). This means that the noise bandwidth after the algorithm is applied reduces by a factor given by:

$$\text{Noise bandwidth reduction factor} = \sqrt{\frac{(1/31)\,\text{MHz}}{9\,\text{MHz}}}, \tag{4.9}$$

noting that the noise is proportional to the square root of the bandwidth. Multiplying the 67 mV rms noise by this reduction factor yields about 4 mV. The rms of the signal before shutdown is about 146 mV, and thus we expect the noise to result in a 2.7% deviation from its mean value, which is expected to be very close to zero. However, as stated earlier, due to the lack of synchronization, the algorithm picks the maximum values of the correlation results between the noise and the Gold sequence, which results in a nonzero mean in the decoded current. In order to illustrate this, an artificial white Gaussian noise signal comparable to the one observed when the circuit block is turned off was created. The noise signal was correlated with the Gold sequence using the algorithm, and after accounting for the proper factors, the result of the correlations is shown in the blue plot in Figure 4-16. The mean of this signal was measured to be around 1.35×10^{-7} V, which is negligible as expected. When the maximum correlation values are picked, as shown by the red circles, the result is a signal with a nonzero mean value. This accounts for the nonzero offset

that is observed even though the circuit block is turned off. In addition, this offset in fact increases when more circuit blocks are running, since the algorithm would correlate the sequence with noise as well as the interference from the other users. A more accurate synchronization method beyond the scope of this thesis needs to be investigated to eliminate this offset.

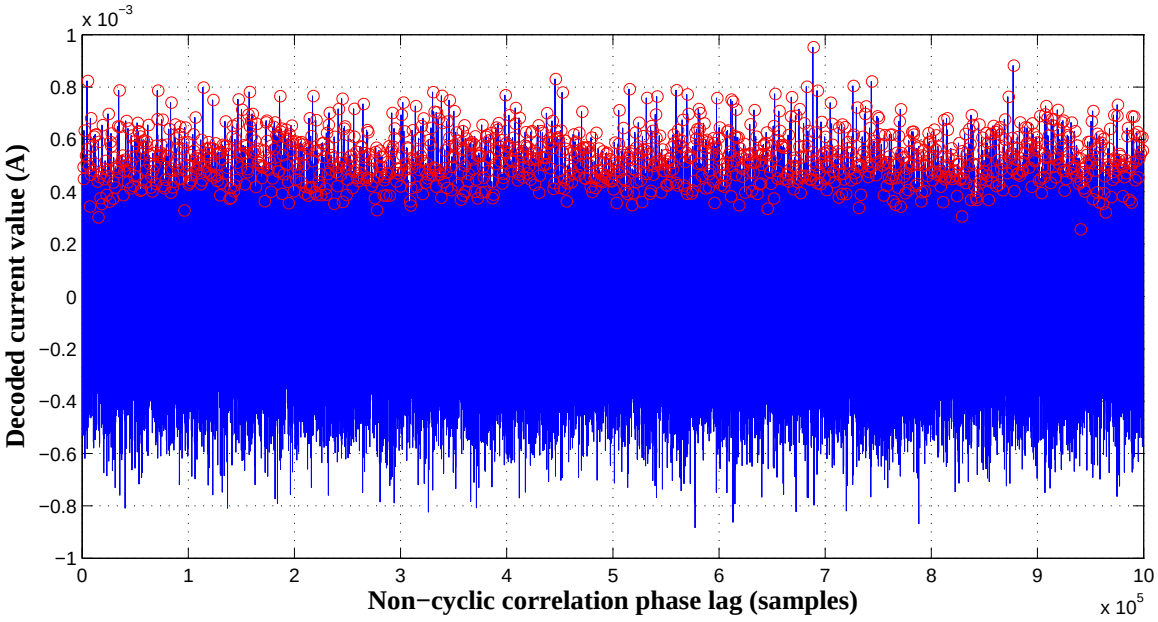


Figure 4-16: Result of all the correlation values of the noise signal with the Gold sequence computed by the algorithm for all the phase lags after accounting for the gain factors. The red circles are the maximum values that are picked by the algorithm to estimate the value of the current.

Next, Figure 4-17 shows the result of the experiment performed, where two other circuit blocks are added. The plot in red shows the state diagram of the block. When the value is high, the block is on, and when the value is low, the block is off.

The effect of the multi-user interference is apparent. However, since the expected value of the multi-user interference is zero, the averaged value of the recovered current over a period of time should equal the actual current. This result can be observed in Figure 4-17. In addition, one can still clearly notice the shutdown transient on the user whose current is encoded with code 1. One can filter the resulting waveforms to get rid of the spikes due to the amplifier saturation as well as the fluctuations due to the cross correlations. The filtered data is shown in Figure 4-18.

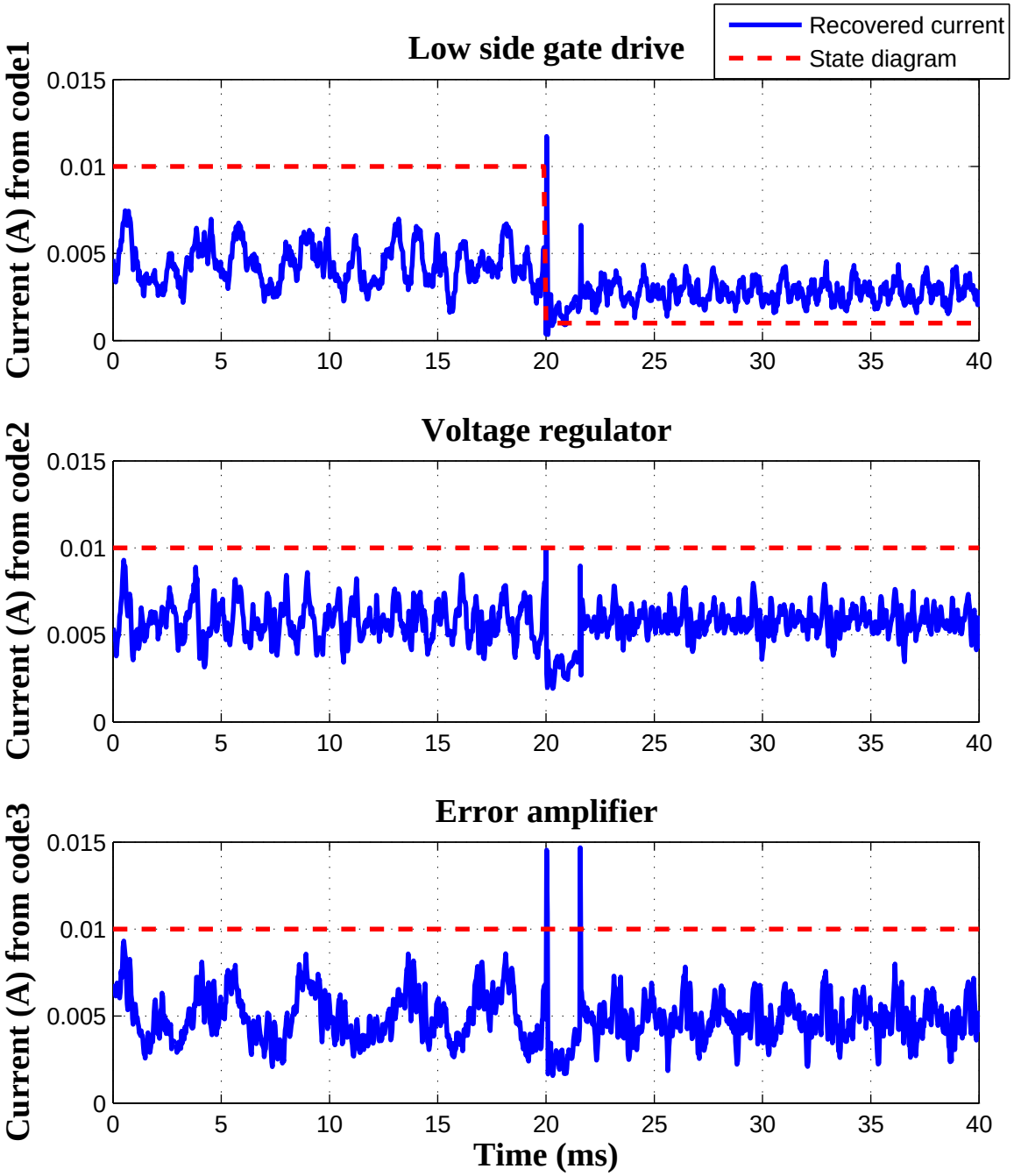


Figure 4-17: Result showing the decoded current value during a shutdown event in the low side gate drive block. The red plot shows the state of each block. In this case, the top block undergoes a shutdown event, while the other two are always on.

Next, Figure 4-19 shows the results of having multiple turn on and turn off events on the low side gate drive block. The filtered waveforms are shown in Figure 4-20.

The next case that we present is when two blocks undergo a turn on and a turn off

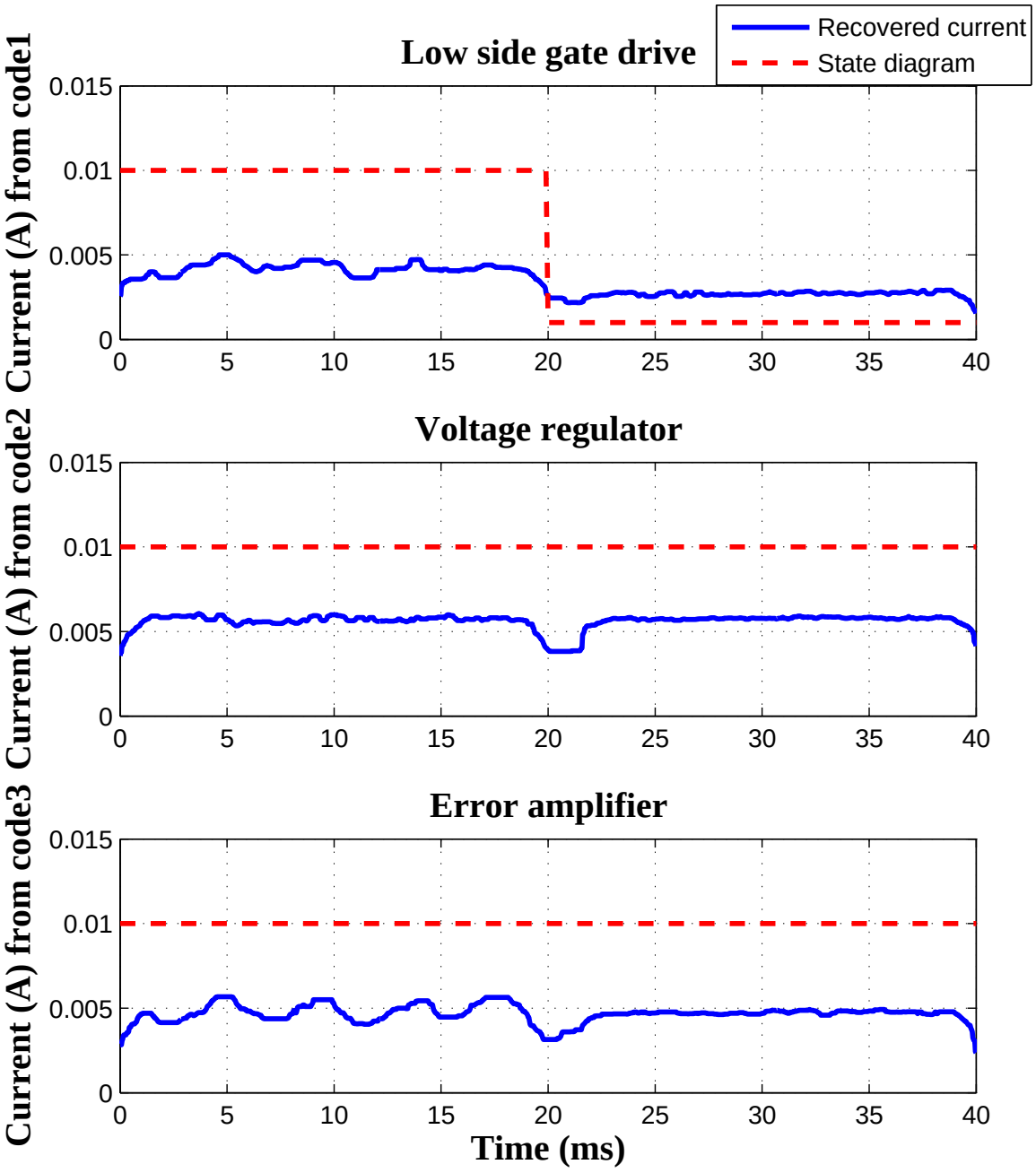


Figure 4-18: Result of the decoded currents after applying a median filter.

event. These events are timed such that they do not overlap with each other. Figures 4-21 and 4-22 show the decoded currents before and after filtering, respectively.

Finally, Figures 4-23 and 4-24 show the results of the case when the turn on and turn off events in the low side gate drive and the voltage regulator overlap with each other.

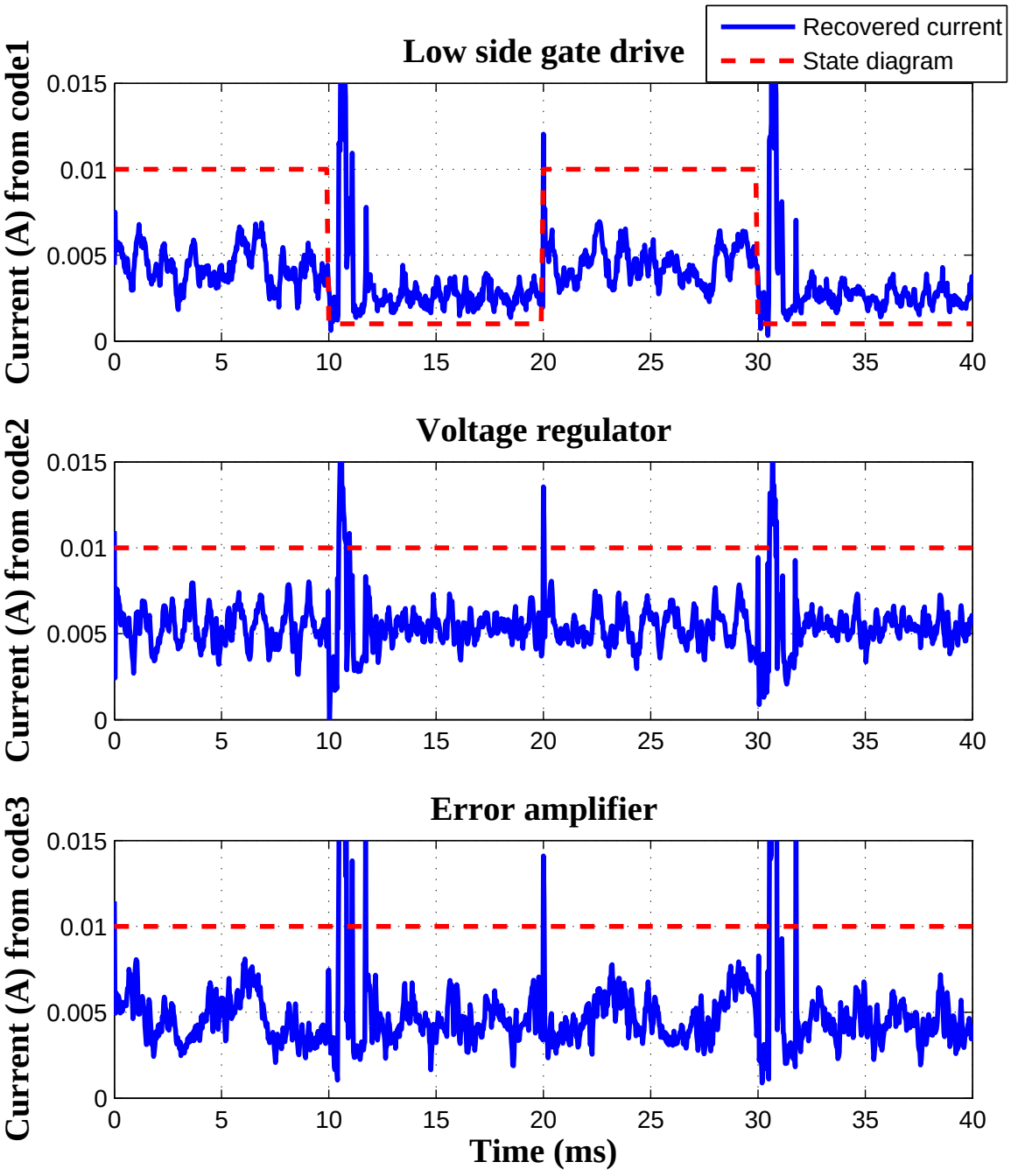


Figure 4-19: Result of the decoded currents when the low side gate drive undergoes multiple turn on and turn off events.

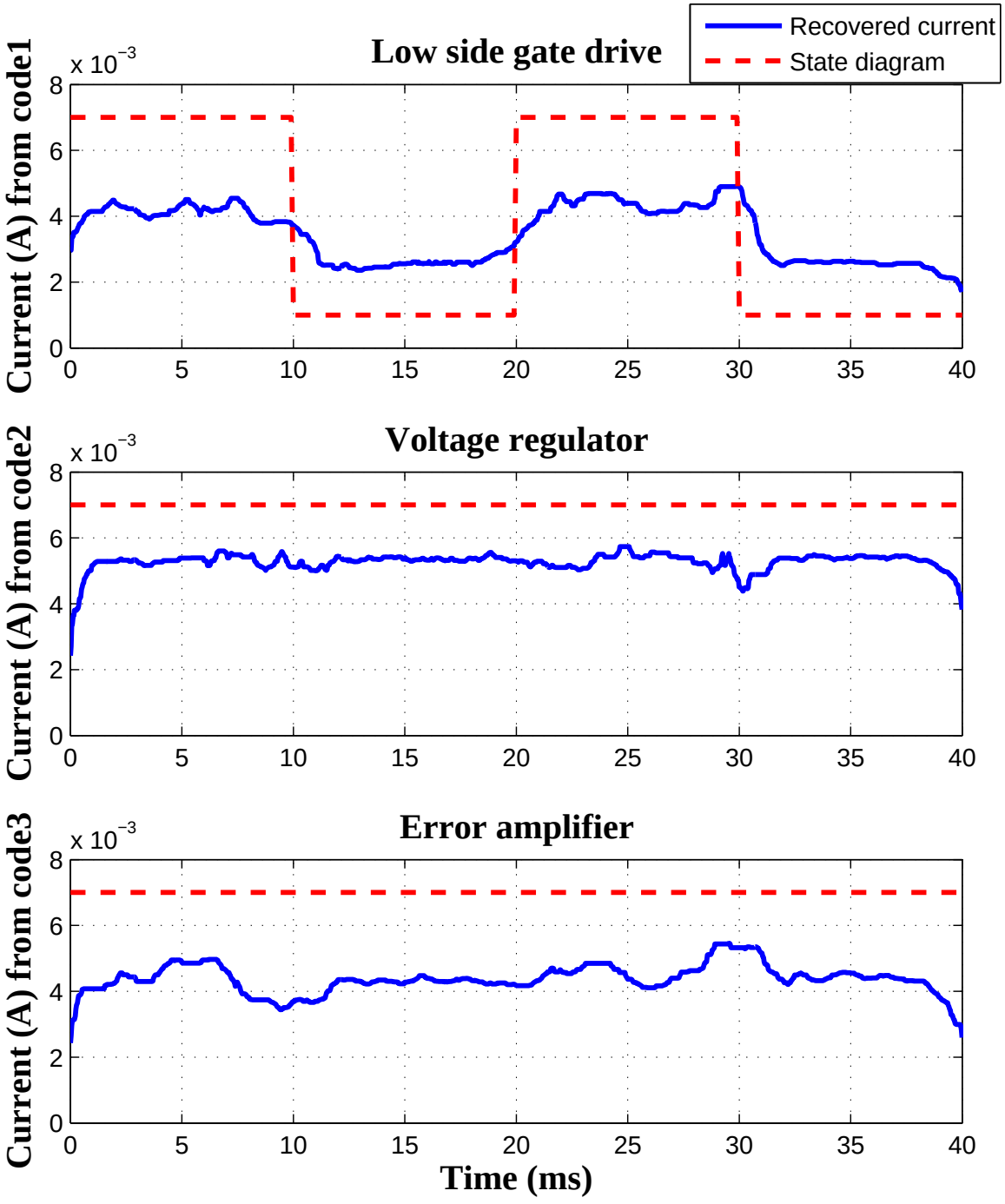


Figure 4-20: Result of the median-filtered decoded currents when the low side gate drive undergoes multiple turn on and turn off events.

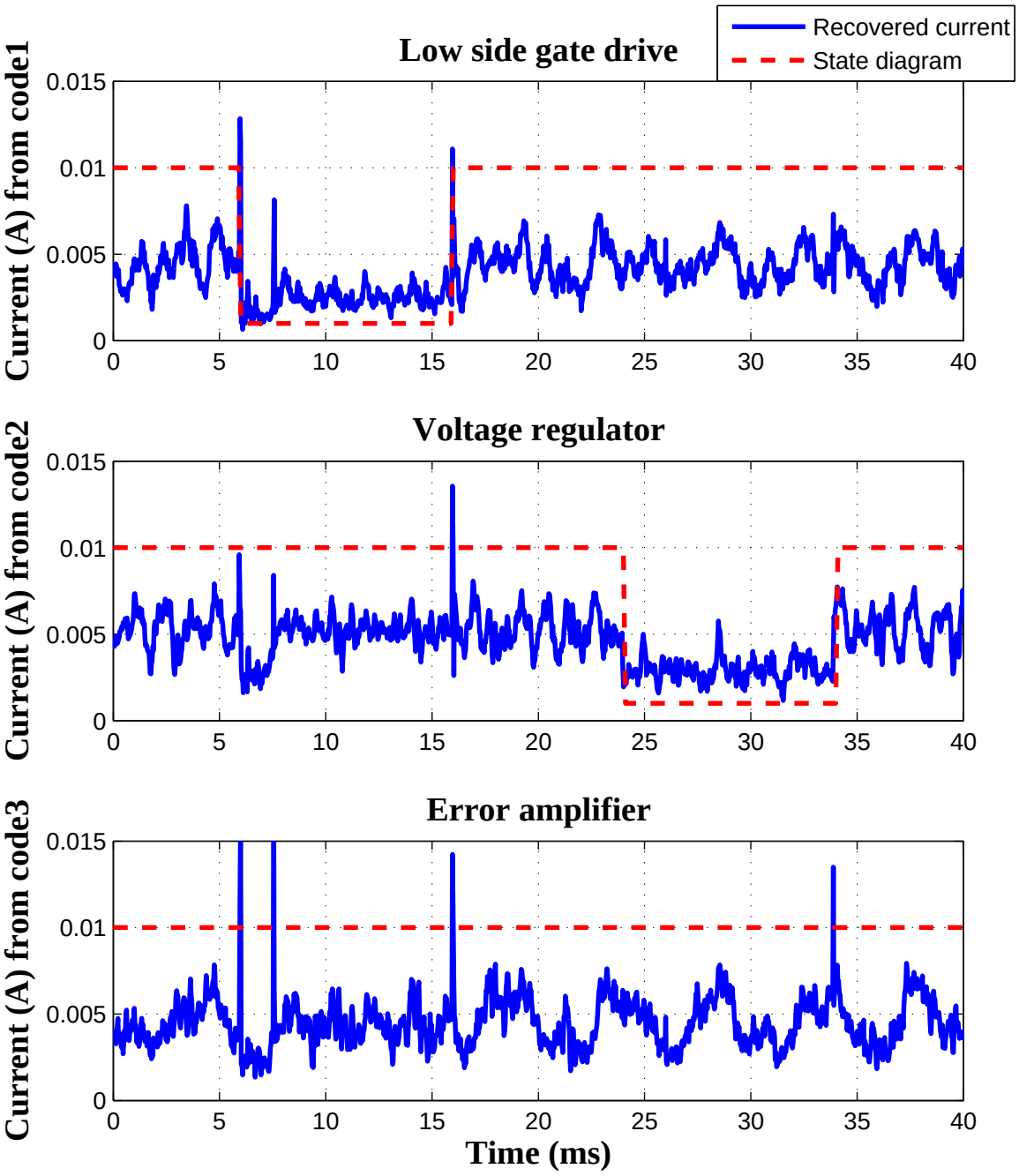


Figure 4-21: Result of the decoded currents when a turn on and a turn off event occur in the low side gate drive block as well as the voltage regulator block. The events do not overlap in this case.

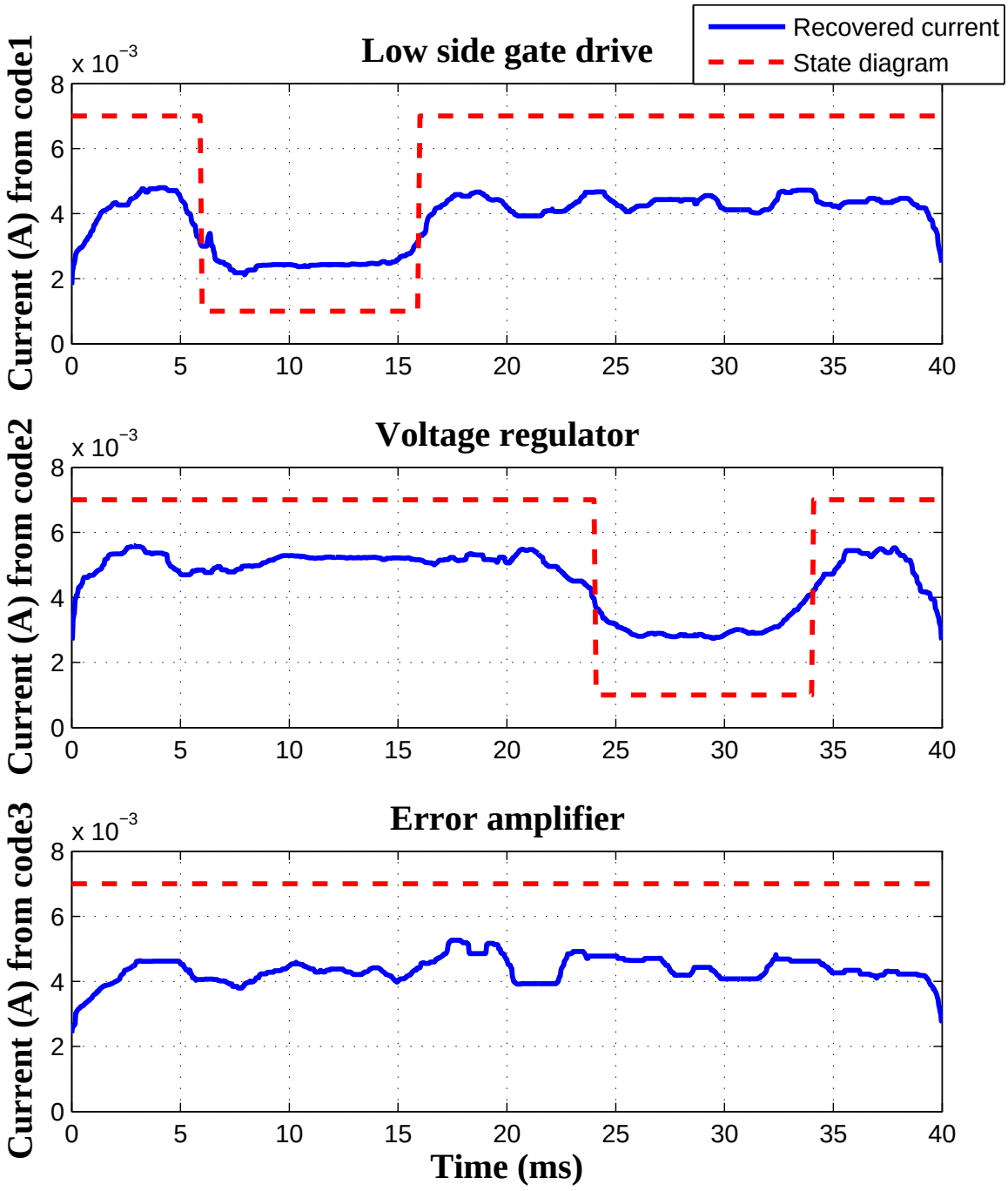


Figure 4-22: Median-filtered decoded currents for the case with non-overlapping turn on and turn off events.

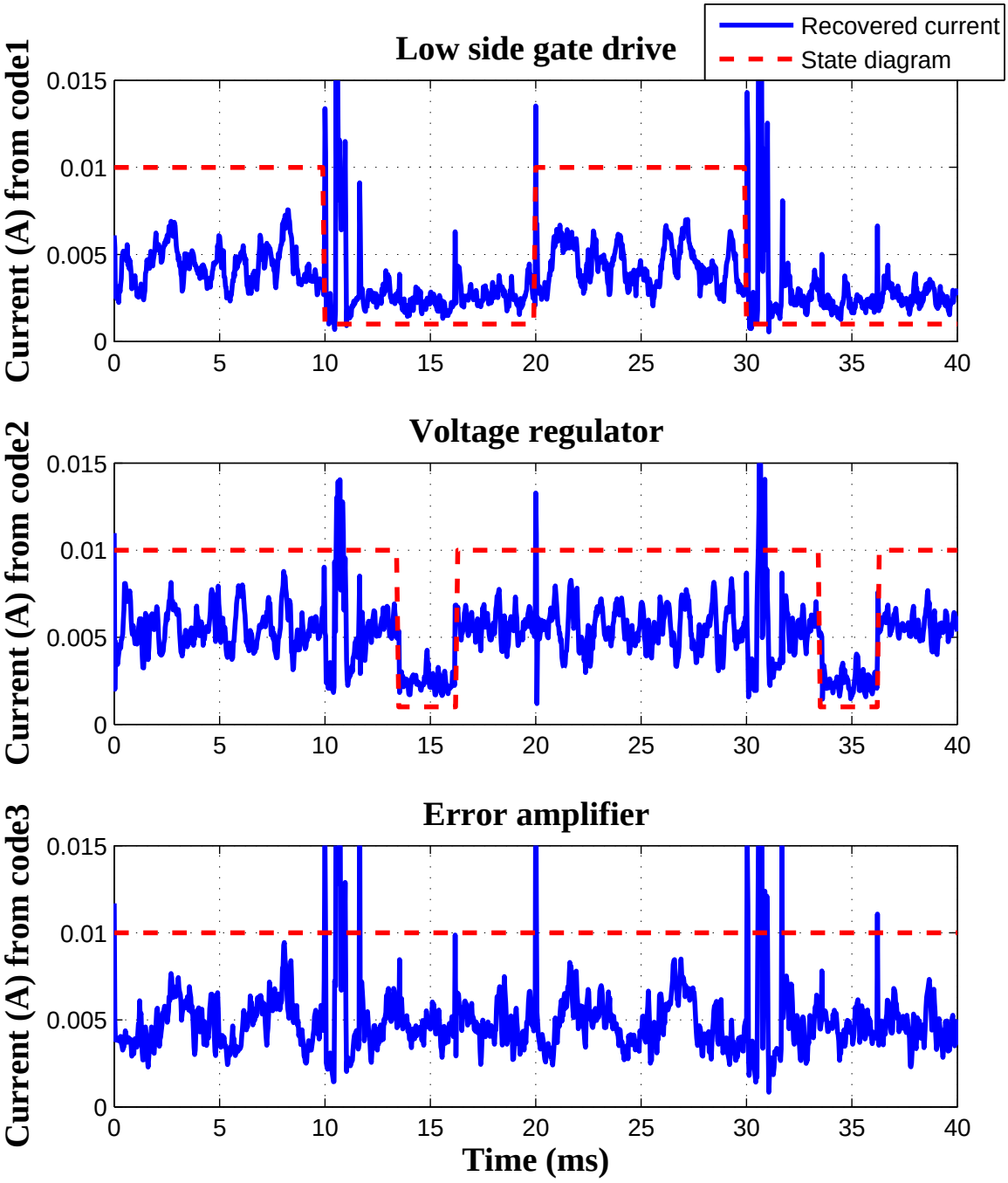


Figure 4-23: Result of the decoded currents when a turn on and a turn off event occur in the low side gate drive block as well as the voltage regulator block. The events overlap with each other in this case.

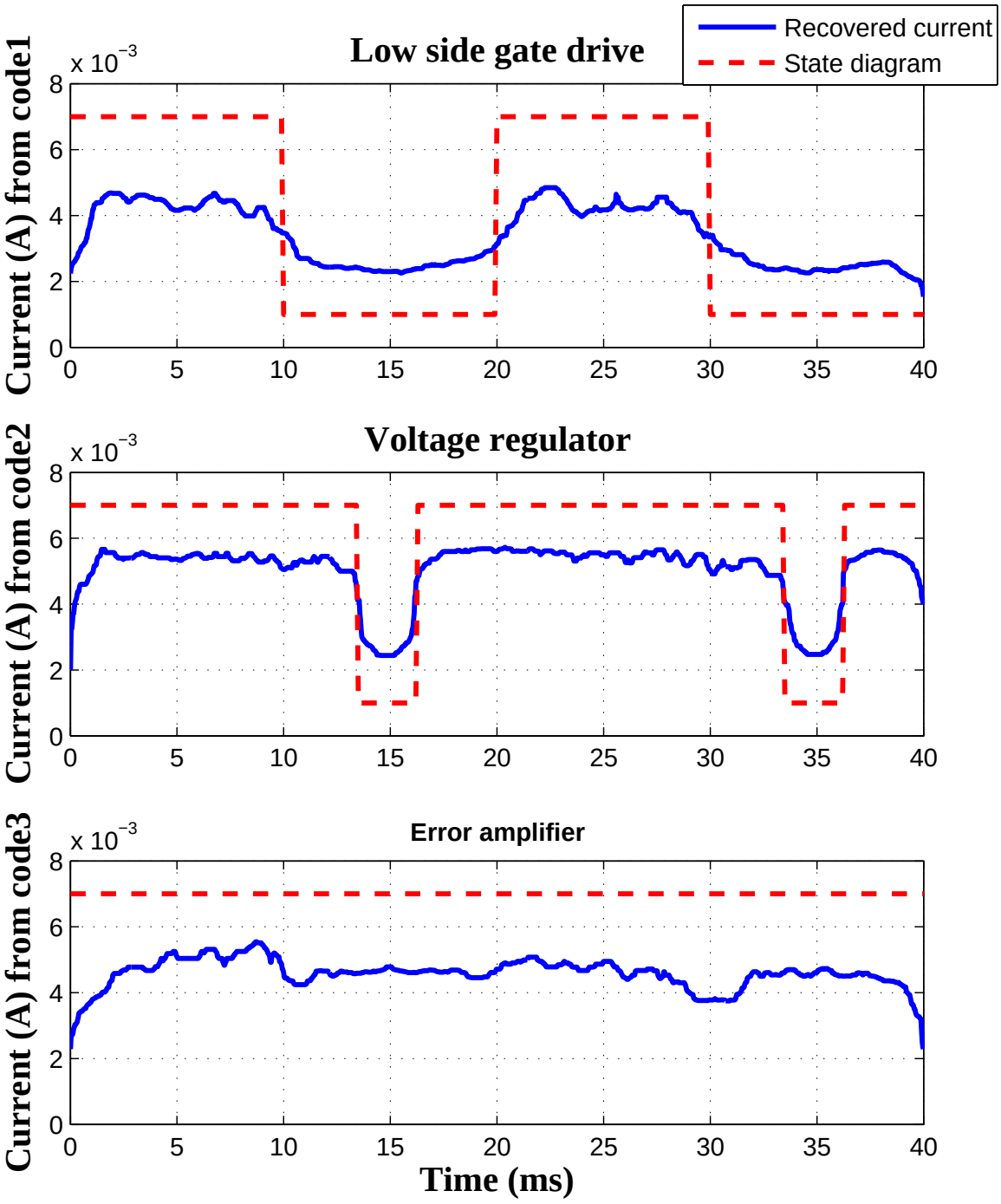


Figure 4-24: Median-filtered decoded currents for the case when the turn on and turn off events in the two blocks overlap with each other.

The signal-to-interference-plus-noise-ratio (SINR) at the input of the receiver circuit can be deduced from equation (2.34) in chapter 2 to be:

$$\text{SINR} = \frac{R_{sense}^2 \alpha_j^2}{R_{sense}^2 \sum_{i \neq j}^{M} \alpha_i^2 + B n_d^2} \times N, \tag{4.10}$$

where α_j is the encoded current of a circuit block that needs to be recovered, α_i's are the rest of the encoded currents from the other blocks, N is the length of the Gold sequence, B is the noise bandwidth and n_d^2 is the rms noise density. This relation implies that the longer the codes, the higher the SINR, and the lower the interference can be made. This is equivalent to noting that the variance of the multi-user interference terms diminishes with a larger code length N.

It is important to keep in mind an issue that can have a significant effect on the accuracy of the recovered currents if not taken into account. In most, if not all circuits, bypass capacitors are added on the power-line to maintain a fixed supply voltage and attenuate any fluctuations. Figure 4-25 shows the effect as well as the small-signal circuit model.

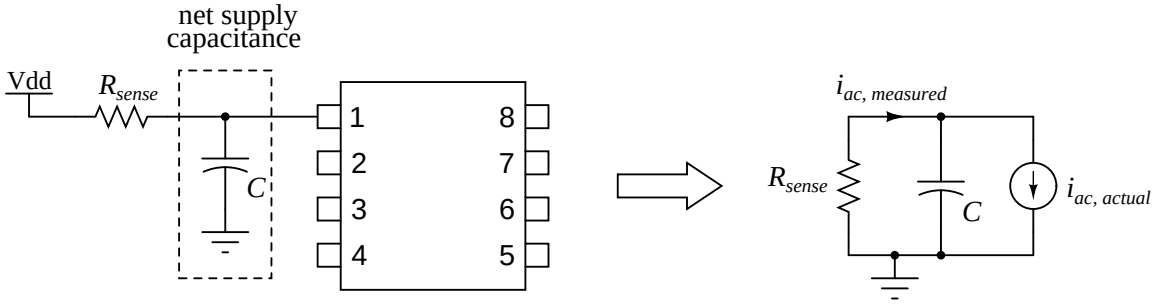


Figure 4-25: A schematic drawing showing the effect of bypass capacitance on the magnitude of the measured current. The small-signal model is shown on the right.

If C denotes the net capacitance on the power-line bus, then the measured ac current is given by a simple current divider:

$$i_{ac,\,measured} = \left(\frac{1}{sR_{sense}C + 1} \right) i_{ac,\,actual} \tag{4.11}$$

If we consider only the magnitudes of both sides of the equation, and solve for $i_{ac,\,actual}$,

we have:

$$i_{ac,\,actual} = \sqrt{1 + (2\pi f R_{sense} C)^2}\, i_{ac,\,measured}, \tag{4.12}$$

where f denotes the frequency of the ac signal.

In the experiments presented here, the gain error factor was corrected for by manually accounting for the factor in the square root during the recovery of the currents. In practice, this factor needs to be determined by measuring the attenuation of a well-known signal before recovering the circuit block currents.

Chapter 5

Discrete Power Controller Platform

We mentioned in the previous chapter that the circuit blocks used for the experiments were actual modules of a discrete version of the UC3842 power controller IC. This discrete implementation of the IC serves not only as an experimental platform to validate the proposed power monitoring method, but also as an educational kit to teach circuit design for power electronics. The platform contains all the control circuitry needed to operate a buck converter with current-mode control strategy.

Section 1 of this chapter provides some background on basic building blocks of analog circuits. Section 2 consists of a full description of all the platform's functional blocks, and can serve as a teaching manual for instructors seeking to use this kit. It includes circuit schematics, functional descriptions, design equations, sample component values, as well as SPICE simulations and experimental results. Appendix A contains the printed circuit board (PCB) designs.

5.1 Analog BJT circuits: a quick review

The control circuit consists of a number of functional blocks that perform a certain task, such as sensing current, amplifying an error, and providing voltage references. These functional blocks are each made up of basic analog building blocks that are

interconnected to form a larger circuit. This section presents some of the most frequently used analog building blocks. These basic blocks are crucial, and most of them will appear several times in multiple functional blocks of the full control circuit.

The bipolar junction transistor (BJT) is a nonlinear device, whose behavior is accurately modeled by the following relation:

$$i_c = I_S \, e^{v_{BE}/V_T} \left(1 + \frac{V_{CE}}{V_A}\right), \tag{5.1}$$

where I_S is the saturation current, V_{BE} is the base-emitter voltage, V_{CE} is the collector-emitter voltage, V_A is the early voltage (due to the "Early Effect"), and $V_T = kT/q$ is the thermal voltage. The reader is encouraged to refer to a reference such as [3] for details on transistor operation. In general, designers are interested in operating the transistor in its linear mode of operation, about a well-defined fixed operating point. Once this fixed operating point is achieved through proper transistor biasing techniques, the nonlinear model can be simplified into an incremental small-signal linear model, which is used to derive simple design equations that are easy to comprehend.

Before presenting the circuit blocks, the small-signal model, also known as the *hybrid-pi* model of the BJT is introduced. This model, shown in Figure 5-1, can be used to derive design equations for various useful design parameters, such as small-signal gain, input and output impedance, as well as the bandwidth of the basic analog blocks.

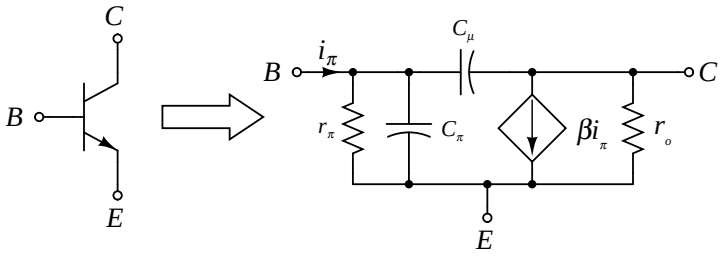


Figure 5-1: Hybrid-pi model of BJT.

It is necessary to differentiate between small-signal parameters (denoted by lower-case letters with lower-case subscripts), and fixed dc parameters (denoted by capital

letters with capital subscripts). Among the most important BJT parameters for the small-signal model are the following:

- ***Transconductance:***

  This parameter models the change in collector current for a change in the base-emitter voltage.

$$g_m = \frac{\partial i_C}{\partial v_{BE}} = \frac{I_C}{V_T} \tag{5.2}$$

- ***Current gain:***

  This parameter models the change in collector current for a change in the base current.

$$\beta = \frac{\partial i_C}{\partial i_B} \tag{5.3}$$

- ***Input resistance:***

$$r_\pi = \frac{\partial v_{BE}}{\partial i_B} = \frac{\beta}{g_m} \tag{5.4}$$

- ***Output resistance:***

$$r_o = \frac{\partial v_{CE}}{\partial i_C} = \frac{V_A}{I_C} \tag{5.5}$$

C_π and C_μ are used to model the dynamics of the BJT in the small-signal model, and can usually be estimated from the device datasheet. One can use them to model the frequency response of circuits involving BJTs.

5.1.1 Single Transistor Amplifiers

Common Emitter

Figure 5-2 shows the configuration of the common emitter amplifier. When viewed as a two-port circuit, the BJT has its emitter shared between the input and output, thus the name "common emitter."

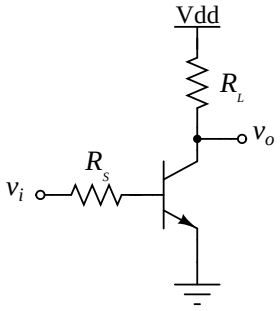


Figure 5-2: Common Emitter Amplifier.

The small-signal gain $a_v = v_o/v_i$ of this circuit can be found by analyzing the small-signal circuit, and applying KVL and KCL. The result is, noting that $r_o \gg R_L$, and assuming a source resistance R_S:

$$a_v = -\frac{\beta R_L}{r_\pi + R_S} \tag{5.6}$$

The input and output resistances, i.e. the ratio of an input (or output) voltage signal to the input (or output) current, of this configuration are:

$$R_{\text{in}} = r_\pi \tag{5.7}$$

$$R_{\text{out}} = r_o \parallel R_L \approx R_L \tag{5.8}$$

Common Base

Figure 5-3 shows the common base configuration. In this case, the base is the shared terminal in the small-signal circuit (the base voltage is a fixed dc bias voltage, and

its small-signal model is a short).

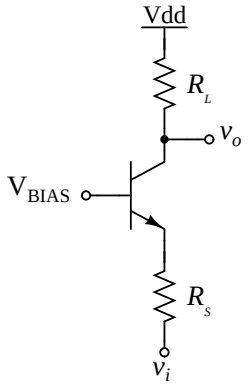


Figure 5-3: Common Base Amplifier.

The gain a_v of this circuit is found to be:

$$a_v = \frac{\beta R_L}{r_\pi + (\beta + 1)R_S} \tag{5.9}$$

Furthermore:

$$R_{\text{in}} = \frac{r_\pi}{\beta + 1} \approx \frac{1}{g_m} \tag{5.10}$$

$$R_{\text{out}} \approx R_L \tag{5.11}$$

Emitter-Follower

Figure 5-4 shows another very important configuration, which is the common-collector, or emitter-follower, circuit. In this topology, the output voltage node is at the emitter of the BJT, unlike the previous two topologies.

The gain of this circuit is:

$$a_v = \frac{(\beta + 1)R_E}{r_\pi + R_S + (\beta + 1)R_E} \approx 1 \tag{5.12}$$

Therefore, the small-signal output v_o at the emitter of this circuit "follows" the input v_i, thus the name "emitter-follower." This circuit makes use as a voltage buffer, which copies the same voltage from its input to its output, but with a low output

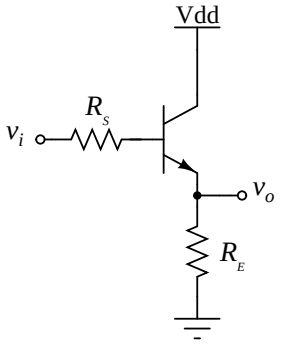


Figure 5-4: Emitter-Follower Configuration.

resistance.

$$R_{\text{in}} = r_\pi + (\beta + 1)R_E \tag{5.13}$$

$$R_{\text{out}} = R_E \parallel \frac{r_\pi + R_S}{\beta + 1} \tag{5.14}$$

5.1.2 Current Mirrors

A very useful topology that appears in most analog electronic circuits is the simple current mirror, shown in Figure 5-5. Assuming matched transistors, this circuit copies current from one terminal to another.

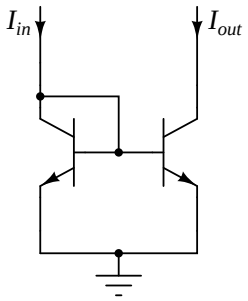


Figure 5-5: Simple Current Mirror.

Since the two transistors are matched, they have the same base-emitter voltage, and thus must have the same collector currents. This fact, along with KCL at the input node, yields:

$$I_{out} = \left(\frac{\beta}{\beta + 2}\right) I_{in} \approx I_{in} \tag{5.15}$$

There are other current mirror topologies that employ more transistors, and give better accuracy and larger output resistance. Ideally, the output resistance is infinite, and the mirror is perfectly accurate. For the specific mirror shown, the output resistance is $R_{\text{out}} = r_o$.

5.1.3 Differential Pairs

Differential pairs are crucial building blocks that appear in many practical analog amplifiers. They amplify the difference between the two input voltages, and they are among the fastest (high bandwidth) amplifiers.

Resistively Loaded Pairs

In this configuration, shown in Figure 5-6, the loads are simple resistors. Consider applying a differential voltage $v_d = v_{ip} - v_{in}$. Assuming the transistors are identical (matched), symmetry demands that $v_{ip} = v_d/2$, and $v_{in} = -v_d/2$. Thus, the differential gain $a_v = v_o/v_d$ can be found from the small-signal model to be:

$$a_v = -\frac{1}{2} g_m R_L \tag{5.16}$$

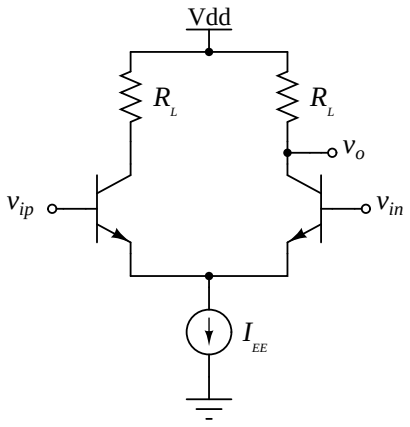


Figure 5-6: Differential Pair with Resistive Loads.

In practice, R_L needs to be large for the gain to be high. In integrated circuits, it

is impractical to have large resistors, as they consume a lot of area.

Actively Loaded Pairs

An alternative way to achieve high gain is to load the differential pair with a current mirror, as shown in Figure 5-7. Again, $v_{ip} = v_d/2$, and $v_{in} = -v_d/2$. Thus, the small-signal current is $g_m v_d/2$ on the collector of the BJT on the left, and $-g_m v_d/2$ on that of the BJT on the right. The current mirror copies current from left to right, resulting in an output current:

$$i_{\text{out}} = \frac{1}{2} g_m v_d - (-\frac{1}{2} g_m v_d) = g_m v_d \tag{5.17}$$

Noting that $v_o = i_{\text{out}} R_{\text{out}}$, we obtain the gain of the circuit:

$$a_v = g_m v_d (r_{o,\ \text{pnp}} \parallel r_{o,\ \text{npn}}) \tag{5.18}$$

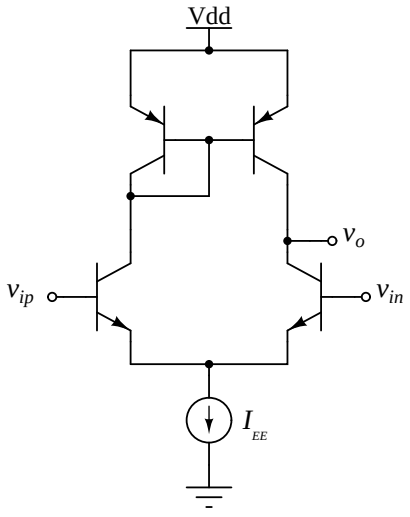


Figure 5-7: Differential Pair with Active Loads.

5.1.4 Emitter Degeneration

As was mentioned earlier, the current-voltage relationship for a BJT (which arises from a semiconductor physics analysis) is highly nonlinear. In order for the linear model to be valid, variations in base-emitter voltage need to be on the order of the thermal voltage, around 26 mV. In certain applications, this narrow allowable range of base-emitter voltage variations might not be acceptable, and one may desire a wider range of input voltage variation.

In order to increase the linear range, a resistor can be added at the emitter, as shown in Figure 5-8. In this case, the input voltage needs to be in the order of $V_T + I_C R_E$ to stay in the linear range. The addition of the emitter degeneration resistor prevents thermal runaway, and increases the linear range by a factor of n, where:

$$n = \frac{I_C R_E}{V_T} \tag{5.19}$$

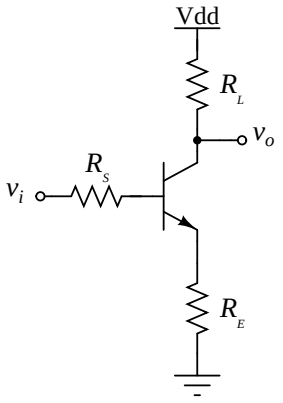


Figure 5-8: Amplifier with emitter degeneration.

It can be shown that the addition of the emitter resistor causes a reduction in the gain by a factor of about $1 + g_m R_E$, compared to the case when there is no emitter resistor. However, the bandwidth can be shown to increase by approximately the same amount.

5.1.5 Operational Amplifiers

Brief Overview

Operational Amplifiers (op amps) are one of the most prevalent and crucial building blocks of analog circuits. They have numerous applications, from general-purpose amplifiers, to comparators, to the implementation of transfer functions for control purposes. The op amp takes in a differential input voltage, and produces an output given by:

$$v_o = a_v(v_{ip} - v_{in}) \tag{5.20}$$

Ideally, op amps have an infinite open-loop gain a_v. The common-mode voltage v_{cm}, defined by

$$v_{cm} = \frac{v_{ip} + v_{in}}{2}, \tag{5.21}$$

is perfectly rejected by an ideal op amp. In other words, the common-mode gain for an ideal op amp, defined by

$$a_{cm} = \frac{v_o}{v_{cm}}, \tag{5.22}$$

is zero. The metric used to measure common-mode rejection is the common-mode rejection ratio (CMRR), measured in decibels (dB), and defined by:

$$\text{CMRR} = 20\log_{10}\left(\frac{a_v}{a_{cm}}\right) \tag{5.23}$$

Real op amps are of course non-ideal, and thus have a finite gain and a finite CMRR. Moreover, real op amps suffer from other non-idealities such as finite bandwidth, noise, saturation, and slew rate limitations. Typically, we operate the op amp so that these non-idealities have no considerable effect on the circuit performance.

Op amps are usually designed to operate under negative feedback. The use of negative feedback is the reason for the op amp's wide use as a stable amplifier whose

gain can be easily set and adjusted with external components. This allows the op amp to be used to implement transfer functions, and thus makes it very useful in filtering and control applications. Figure 5-9 shows a typical op amp configuration being used as an inverting amplifier.

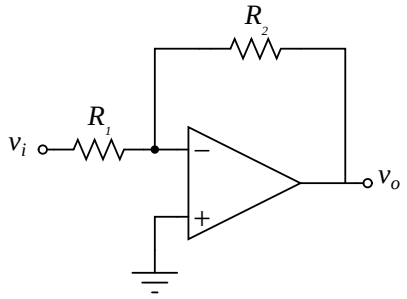


Figure 5-9: Op amp in the inverting configuration.

Operational Amplifier Design Stages

Depending on how the op amp is going to be used, the design may vary for different purposes. For example, a comparator does not typically have all the stages that are present in general-purpose op amps. In this section, a brief overview of the design of op amps is given. Figure 5-10 shows the general design strategy.

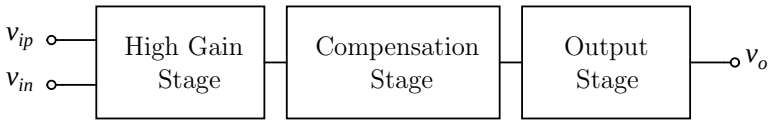


Figure 5-10: Typical stages in general-purpose op amps.

- **High Gain Stage**

  This stage is typically made up of a differential amplifier, very similar to the one shown in Figure 5-7. The input is taken in the form of a differential voltage, and is amplified and passed to the next stage.

- **Compensation Stage**

  The full op amp circuit contains a number of parasitic capacitors to ground at different nodes. This results in a number of parasitic poles that severely degrade the performance by reducing the phase margin. If these are ignored, the op amp will be unstable (as the phase will reach -180° before crossover). Therefore, the op amp has to be compensated in order to force early crossover, such that there is enough phase margin. This is typically done through dominant pole compensation; a low-frequency pole is added, which forces roll-off at that frequency.

- **Output Stage**

  This stage is needed to interface the op amp with the load. It acts as a voltage buffer, and results in the op amp's low output impedance. Typically, some form of an emitter-follower stage (similar to the one in Figure 5-4) is used.

5.2 Platform Circuit Blocks

5.2.1 Bandgap and References

The bandgap and references board contains four circuits that provide several voltage sources as well as protection to the rest of the controller circuit. The only voltage source available to the power controller is the standard 15 V supply. The outputs of these circuits in this board provide the rest of the controller access to 12 V and 5 V references, as well as to a temperature-independent bandgap voltage V_{BG} (whose value is about 1.2 V), and a proportional-to-absolute-temperature (PTAT) voltage V_{PTAT} whose value is about 5 V at room temperature.

The way the bandgap voltage is created is illustrated in Figure 5-11. The temperature coefficient of the base-emitter voltage V_{BE} of a BJT is about -2 mV/°C, and that of the thermal voltage V_T is around +0.085 mV/°C. Thus, if a circuit can

be designed to create a voltage $V_{BE} + KV_T$, where K is around $2/0.085 \approx 23.5$, the resulting voltage will have a temperature coefficient very close to zero. The resulting voltage value will be $V_{BE} + KV_T \approx 1.2$ V.

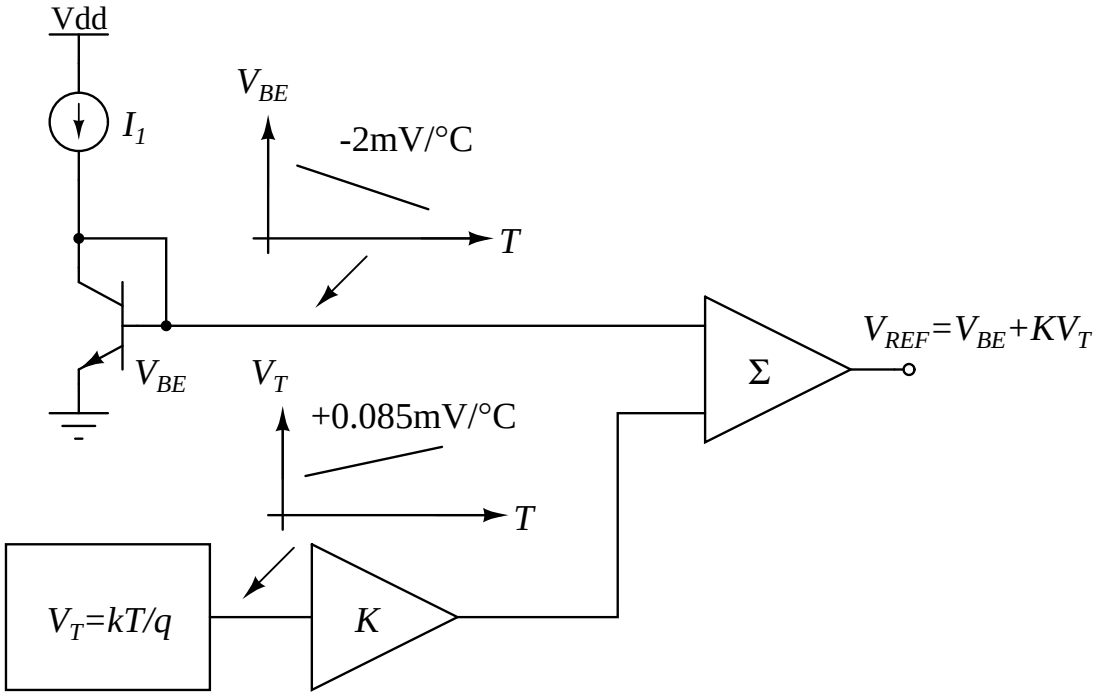


Figure 5-11: Illustation of bandgap voltage creation [3].

Circuits Description

- Bandgap Circuit

Figure 5-12 shows the schematic of the bandgap voltage generator. This circuit contains a number of features that should be individually analyzed. A simplified diagram of the core of the circuit used here to create the bandgap voltage is shown in Figure 5-13.

The feedback of the operational amplifier forces its input nodes to be practically equal. Since the top node V_{BG} is the for both R_1 and R_2, the voltage drop across them is equal. Thus:

$$I_1 R_1 = I_2 R_2, \tag{5.24}$$

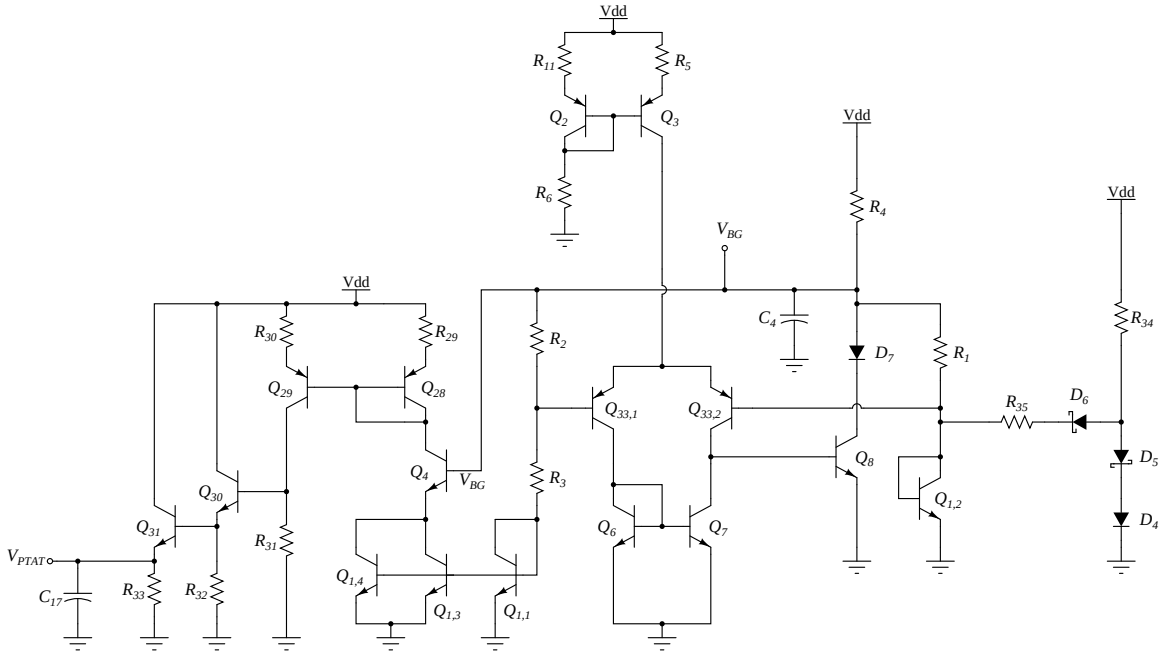


Figure 5-12: Circuit schematic of the bandgap circuit

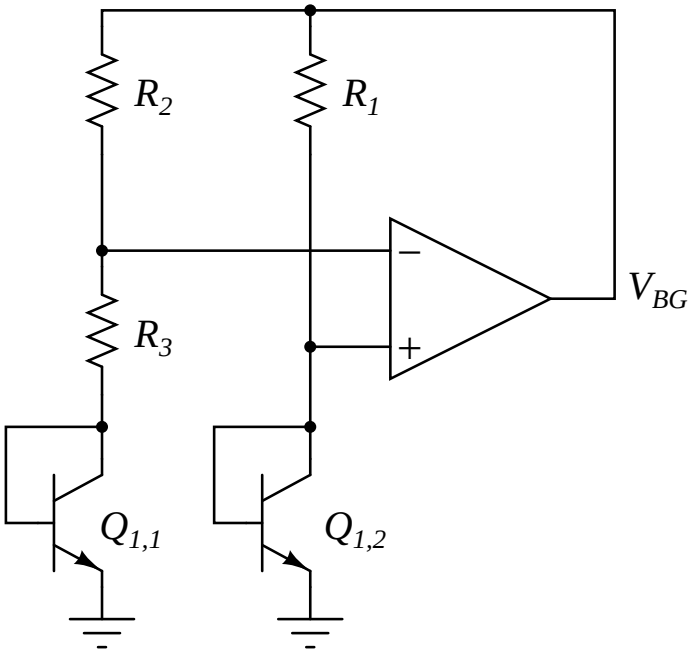


Figure 5-13: A simplified circuit model of the bandgap voltage circuit block.

where I_1 and I_2 are the currents flowing through R_1 and R_2, respectively. This also dictates the voltage drop across R_3, so we can compute the current through it as

follows:

$$\begin{aligned} I_2 &= \frac{V_{BE2} - V_{BE1}}{R_3} = \frac{V_T \ln(I_1/I_S) - V_T \ln(I_2/I_S)}{R_3} \\ &= \frac{V_T}{R_3} \ln\left(\frac{I_1}{I_2}\right) = \frac{V_T}{R_3} \ln\left(\frac{R_2}{R_1}\right) \end{aligned} \tag{5.25}$$

Note that this assumes that the transistors are well-matched, and thus I_S is the same for both (Q_1 is implemented using a matched quad NPN part). The last equality comes from the fact that $I_1/I_2 = R_2/R_1$ as was noted above.

The output voltage V_{BG} can now be found as follows:

$$\begin{aligned} V_{BG} &= V_{BE2} + I_1 R_1 = V_{BE2} + I_2 R_2 \\ &= V_{BE2} + \left[\frac{R_2}{R_3} \ln\left(\frac{R_2}{R_1}\right)\right] V_T \end{aligned} \tag{5.26}$$

This expression is clearly analogous to the desired voltage reference $V_{BE} + KV_T$ shown above, and K is the term in the brackets. Now, the fact that $K = 23.5$ sets a condition on this term. The designer can set conditions on I_1 and I_2 in order to uniquely determine the resistor values. A possible combination can be as follows:

$$R_1 = 910\,\Omega \tag{5.27}$$

$$R_2 = 11\,k\Omega \tag{5.28}$$

$$R_3 = 1.2\,k\Omega \tag{5.29}$$

The differential pair formed by the super-matched pair Q_{33} in Figure 5-12, along with transistor Q_8 is an implementation of the op amp in Figure 5-13. The differential pair is actively loaded with the current mirror formed by Q_6 and Q_7, and biased by the current source formed by Q_2, Q_3, R_5, R_6, and R_{11}. This bias current I_{bias}, given by the equation below, is chosen to be around 0.5 mA. Note that $R_5 = R_{11}$ in order for the currents through both sides of the mirror to be equal. Also, C_4 is a 0.1 μF bypass

capacitor and provides dominant-pole compensation to the op amp.

$$I_{bias} = \frac{15 - 0.6}{R_6 + R_{11}} \approx 0.5\,\text{mA} \tag{5.30}$$

Thus, a possible choice for the resistors is as follows:

$$R_5 = 620\,\Omega \tag{5.31}$$

$$R_6 = 27\,k\Omega \tag{5.32}$$

$$R_{11} = 620\,\Omega \tag{5.33}$$

The next important feature of the circuit is the creation of V_{PTAT}. One can realize from equation (5.25) that I_2 is a PTAT current. This current can be mirrored by $Q_{1,3}$ and $Q_{1,4}$, Q_{28} and Q_{29}, and passed through resistor R_{31} to create a PTAT voltage. The two transistors $Q_{1,3}$ and $Q_{1,4}$ are paralleled in order to double the current, so that R_{31} can be made smaller. This is needed to avoid any loading by Q_{29} on the node at the top of R_{31}. Q_4 simply acts as a level shift.

However, one should note that V_{PTAT} is feeding a number of circuits in other boards, and is thus vulnerable to inter-stage loading. To avoid this, two emitter-follower stages are added using Q_{30} and Q_{31}, which result in a relatively low output impedance at the V_{PTAT} node. Also, the two emitter-follower stages increase the amount of current than can be sourced to other circuits. R_{31} is chosen to be $60\,k\Omega$ such that its voltage is around 6.2 V at room temperature. C_{17} is a 0.1 μF bypass capacitor.

$$2I_2R_{31} = 6.2\,\text{V} \qquad \Longrightarrow \qquad V_{PTAT} = 5\,\text{V} \tag{5.34}$$

The last feature of this circuit deals with the issue of start-up. An inherent problem with most self-biased circuits [3] is the existence of more than one operating point, in which another stable operating point could be the zero current state, i.e. when zero current flows through sections of the circuit. This is prevented by ensuring that a small but non-zero current flows at all times. This is achieved by adding the

sections at the right of Figure 5-12 using D_4, D_5, D_6, D_7, R_4, R_{34}, and R_{35}.

- Supply Voltage Protection Circuit

This is a protection circuit that prevents any damage to the other circuits on the bandgap and references board in case the supply voltage goes outside the allowable range. Nominally, the supply voltage should be 15 V. We choose the allowable range to be approximately between 14 V and 16 V. The circuit is shown in Figure 5-14. D_1

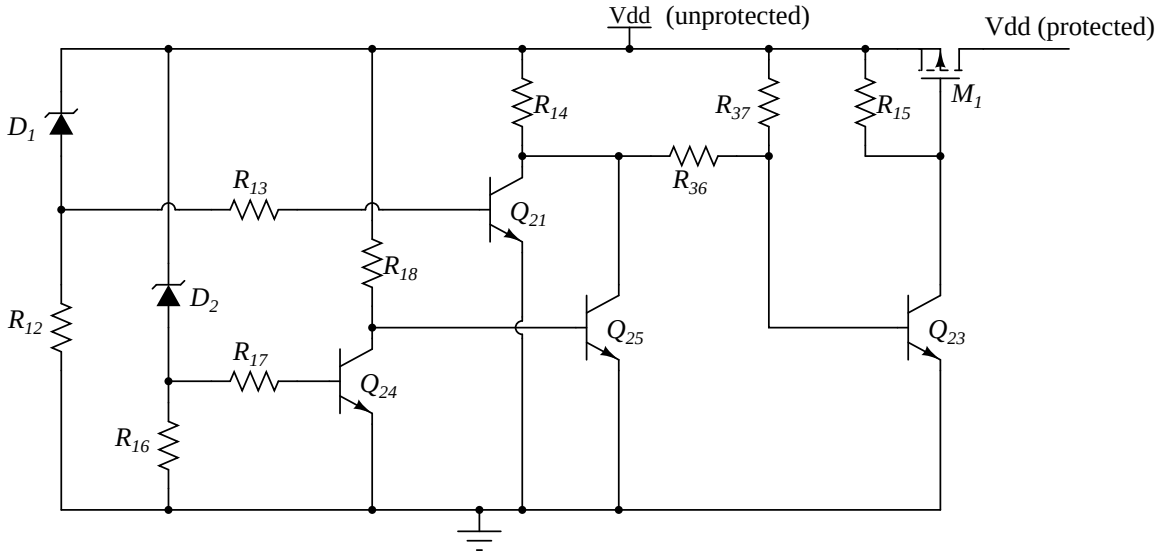


Figure 5-14: Circuit schematic of the supply protection circuit

is a 16 V zener diode, and D_2 is a 14.3 V zener. When the supply voltage is lower than 14.3 V, both zeners are off, and thus both Q_{21} and Q_{24} are off. Q_{25} turns on since R_{18} pulls its base voltage up, and so Q_{23} turns off. Therefore, M_1 is off and the supply voltage is disabled.

When the supply voltage is between about 14.6 V and 16.3 V (i.e. within the allowable range), D_2 is on, so the collector of Q_{24} is pulled down, turning Q_{25} off. Q_{21} is also off since D_1 is off. In this case, the base of Q_{23} is pulled up by R_{37} and $R_{14} + R_{36}$, thus pulling $M1$'s gate low, turning it on and activating the supply.

When the supply voltage exceeds 16.3 V, both D_1 and D_2 are on, turning on Q_{24} (so Q_{25} is off) and Q_{21}. Thus, Q_{23} turns off, which means M_1 is off again, and the supply voltage is disabled.

Resistors R_{14}, R_{15}, R_{18}, and R_{37} are pull-up resistors, and chosen to be 10 $k\Omega$.

R_{13}, R_{17}, and R_{36} are base protection resistors, chosen to be 160 Ω. R_{12} and R_{16} are pull-down resistors, chosen to be 5.1 $k\Omega$.

- 5 V and 12 V References

These two circuits provide the 5 V and 12 V voltages needed for the operation of the circuits in the other boards. Their design procedure is identical, and will therefore be analyzed together here. Figure 5-15 shows the circuit of the 5 V reference.

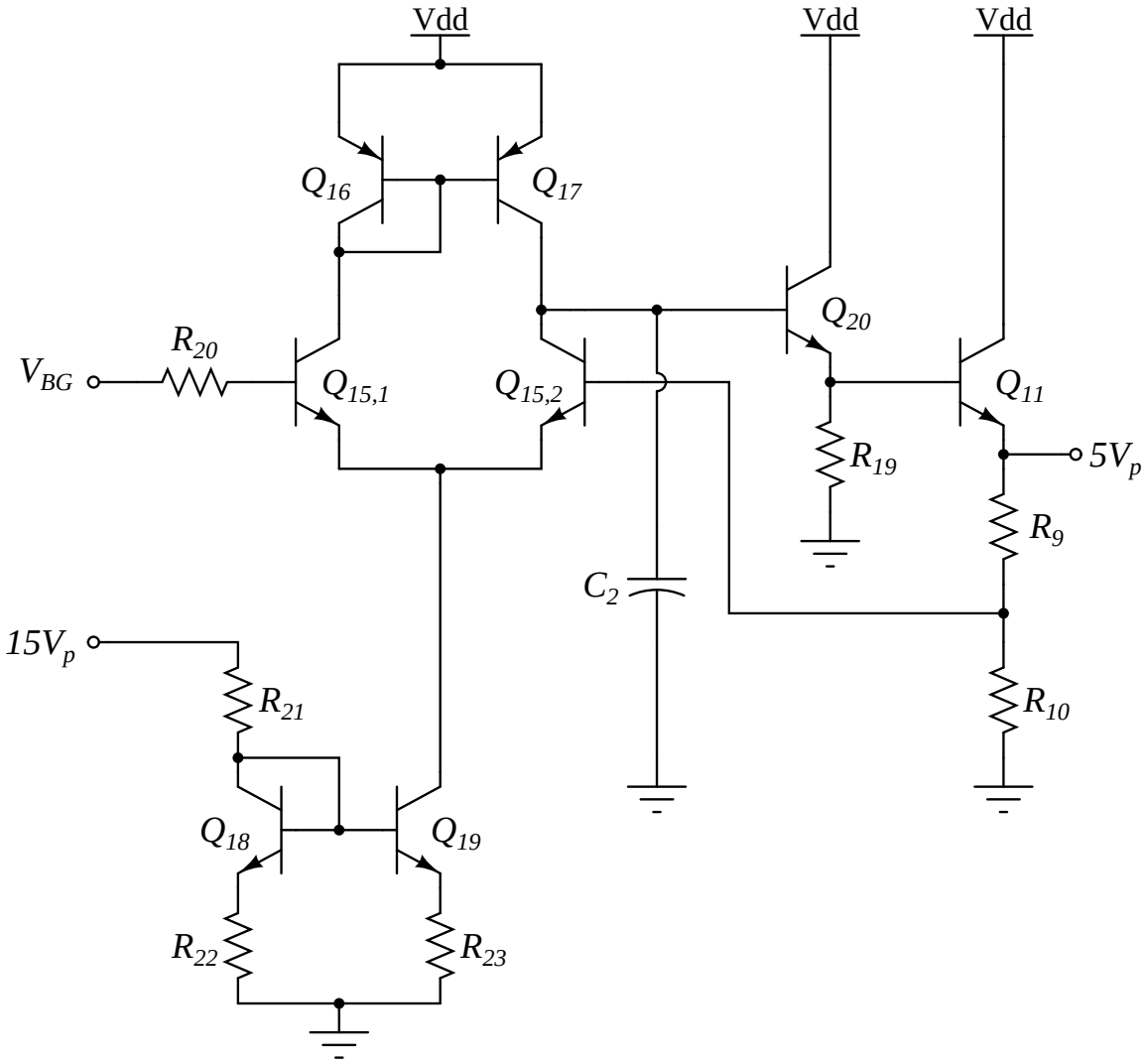


Figure 5-15: Circuit schematic of the 5 V supply

The circuit is an op amp connected in negative feedback, with the bandgap voltage V_{bg} as the reference voltage, and with feedback resistors R_9 and R_{10} to set the required reference voltage of 5 V. Just like in the case of the output stages needed

to generate V_{PTAT}, Q_{11} and Q_{20} form two emitter-follower stages to provide a low output resistance, as well as increase the current driving capability. C_2 is chosen to be HEREHERE in order to provide dominant-pole compensation to the op amp. The tail bias current is chosen to be around 2 mA, which results in a g_m of about 40 m$\mho$ for each input transistor in the pair Q_{15}. The bias current is generated from the 15 V protected supply:

$$I_{bias} = \frac{15 - 0.6}{R_{21} + R_{22}} = 2\,\text{mA} \tag{5.35}$$

A possible choice of resistor values can be $R_{21} = 6.8\,k\Omega$ and $R_{22} = 150\,\Omega$. Moreover, the mirror ratio is $1:1$, so $R_{23} = R_{22} = 150\,\Omega$.

The voltage across R_{10} is equal to the bandgap voltage V_{BG} due to the op amp in feedback. Thus:

$$\left(1 + \frac{R_9}{R_{10}}\right) V_{BG} = 5\,\text{V}, \tag{5.36}$$

and so one can choose $R_9 = 10\,k\Omega$ and $R_{10} = 3\,k\Omega$ (using $V_{BG} = 1.16\,\text{V}$).

The 12 V supply has an identical design, but the resistor ratio in equation (5.36) is designed to give 12 V on the right hand side of the equation instead of 5 V. Thus, if one chooses $R_9 = 12\,k\Omega$ and $R_{10} = 1.3\,k\Omega$, the resulting output voltage would be 12 V.

Table 5.1 below shows a summary of the chosen component values.

SPICE Simulations

Figure 5-16 shows a temperature sweep simulation of the bandgap and PTAT voltage references. It can be observed that the bandgap voltage maintains its value over the temperature range of interest, while the PTAT voltage linearly increases. Note that the nominal value of V_{PTAT} at room temperature is around 5 V. Next, Figure 5-17 shows the result of the supply voltage protection circuit simulation. It can be seen that the protected output voltage is 0 outside the allowable range.

Table 5.1: Summary of component values used in the sample design of the bandgap and references board

Component	**Value**	**Component**	**Value**
R_1	$910\,\Omega$	R_{23}	$150\,\Omega$
R_2	$11\,k\Omega$	R_{24}	$160\,\Omega$
R_3	$1.2\,k\Omega$	R_{25}	$6.8\,k\Omega$
R_4	$10\,k\Omega$	R_{26}	$150\,\Omega$
R_5	$620\,\Omega$	R_{27}	$150\,\Omega$
R_6	$27\,k\Omega$	R_{28}	$10\,k\Omega$
R_7	$12\,k\Omega$	R_{29}	$5.1\,k\Omega$
R_8	$1.3\,k\Omega$	R_{30}	$5.1\,k\Omega$
R_9	$10\,k\Omega$	R_{31}	$60\,k\Omega$
R_{10}	$3\,k\Omega$	R_{32}	$51\,k\Omega$
R_{11}	$620\,\Omega$	R_{33}	$10\,k\Omega$
R_{12}	$5.1\,k\Omega$	R_{34}	$100\,k\Omega$
R_{13}	$160\,\Omega$	R_{35}	$160\,\Omega$
R_{14}	$10\,k\Omega$	R_{36}	$160\,\Omega$
R_{15}	$10\,k\Omega$	R_{37}	$10\,k\Omega$
R_{16}	$5.1\,k\Omega$	C_1	$10\ \mu$F
R_{17}	$160\,\Omega$	C_2	$10\ \mu$F
R_{18}	$10\,k\Omega$	C_3	0.1μF
R_{19}	$10\,k\Omega$	C_4	$0.1\ \mu$F
R_{20}	$160\,\Omega$	C_5	$0.1\ \mu$F
R_{21}	$6.8\,k\Omega$	C_6	$220\ \mu$F
R_{22}	$150\,\Omega$	C_7	$0.1\ \mu$F
C_9	$220\ \mu$F	C_{10}	$0.1\ \mu$F
C_{11}	$220\ \mu$F	C_{13}	$0.1\ \mu$F
C_{14}	$0.1\ \mu$F	C_{16}	$220\ \mu$F
C_{17}	$0.1\ \mu$F	C_{18}	$10\ \mu$F
C_{19}	$10\ \mu$F	C_{20}	$10\ \mu$F
C_{21}	$10\ \mu$F		

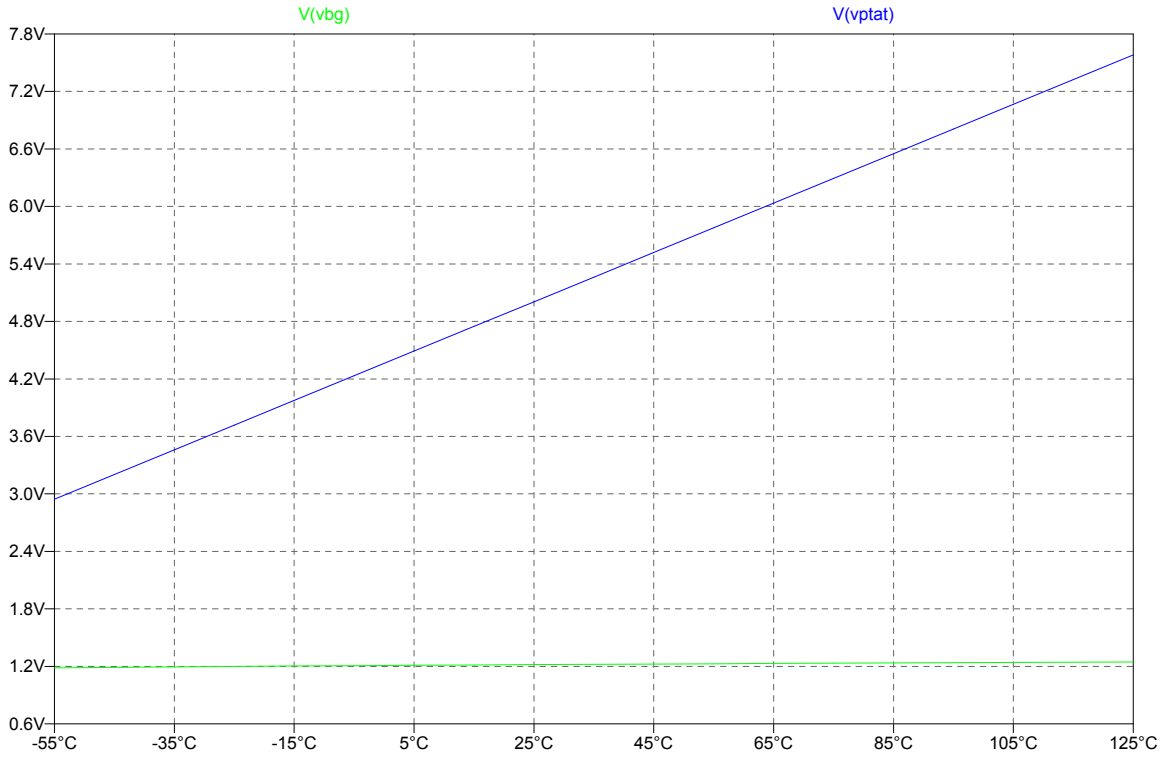


Figure 5-16: Temperature sweep simulation of the bandgap circuit

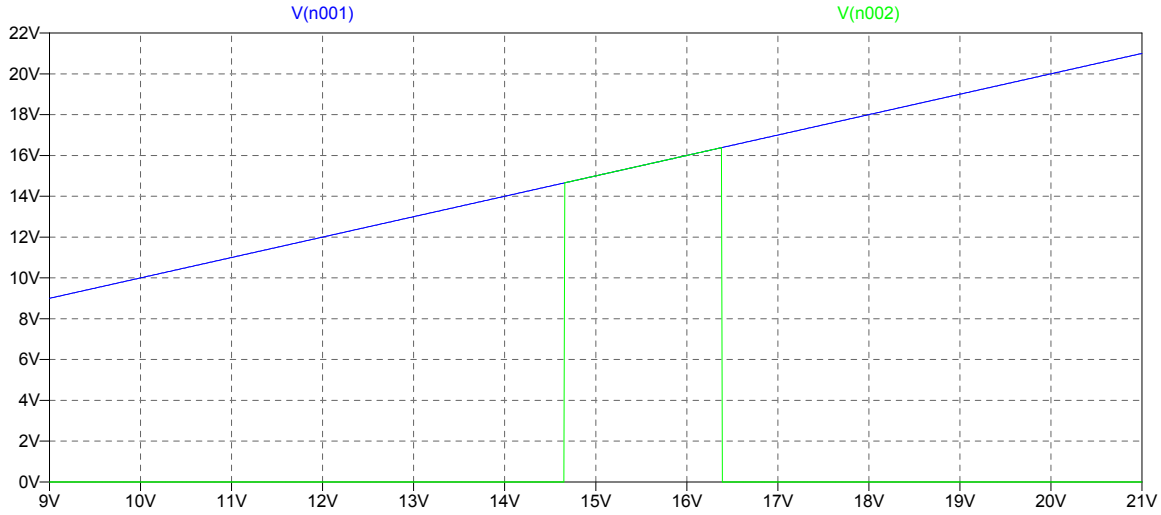


Figure 5-17: Simulation of the supply voltage protection circuit

Experimental Result

Figure 5-18 below shows the experimental result of the bandgap and voltage references circuits.

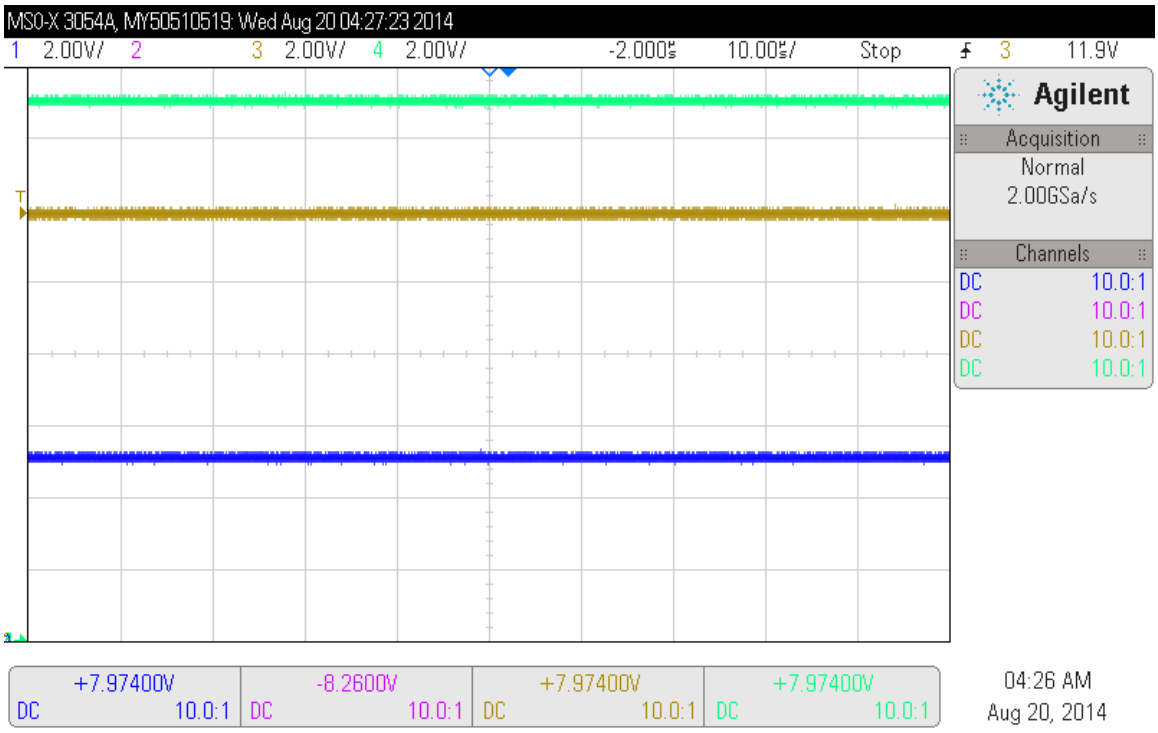


Figure 5-18: Experimental result showing the voltage levels of the bandgap and references circuits.

5.2.2 Error Amplifier and 2.5 V Reference

The error amplifier board consists of two functional circuit blocks that are crucial to the design of the power controller circuit: the voltage regulator, and the error amplifier.

Circuits Description

- Voltage Regulator

The voltage regulator, shown in Figure 5-19, provides a constant stable 2.5 V reference to be used by the error amplifier. This voltage should be constant regardless of the operating conditions of the board, and thus must also be independent of temperature.

For this reason, the bandgap voltage V_{BG}, generated in the bandgap and references board, is used. V_{BG} has a value around 1.2 V and is independent of temperature for

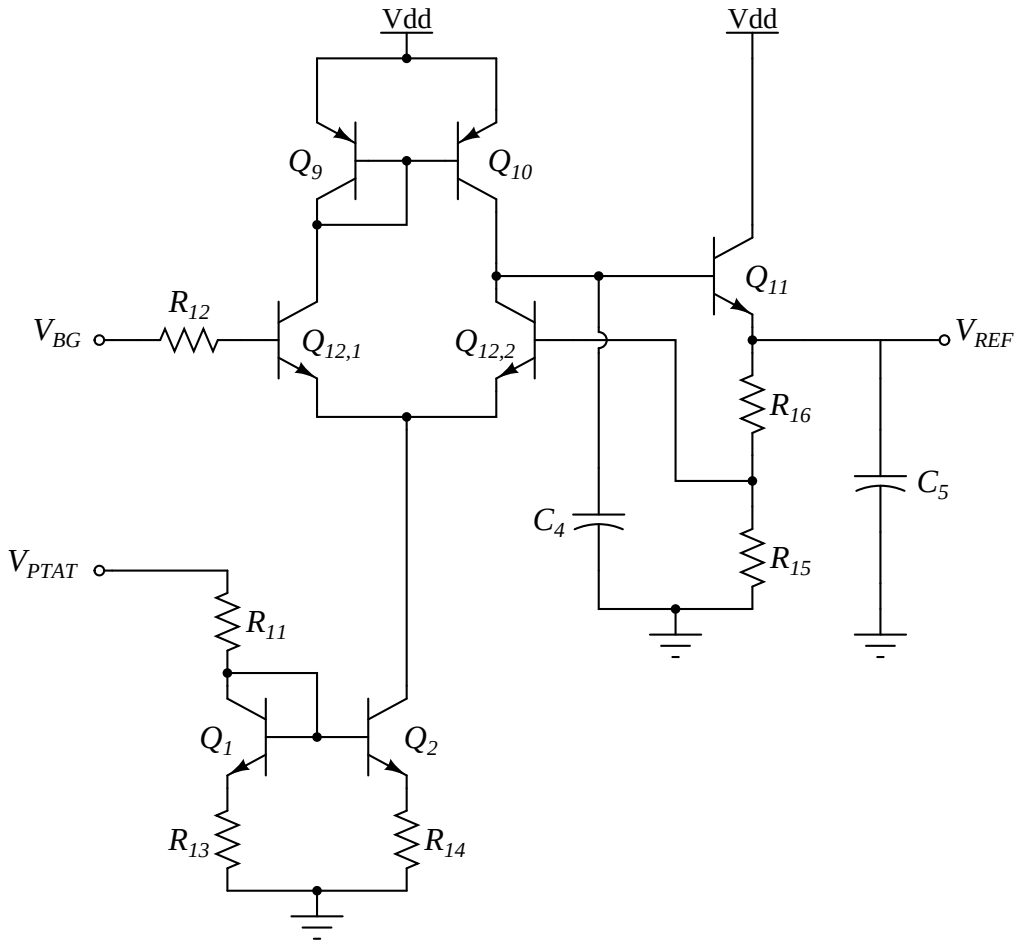


Figure 5-19: Circuit schematic of the voltage regulator.

a wide temperature range, as was discussed earlier. The circuit is simply an op amp connected in negative feedback, with the feedback resistors setting the required reference voltage. The design is similar to the 5 V and 12 V references in the bandgap board, but we wish to analyze the circuit here in more details. The open-loop dc gain of the circuit is:

$$A = g_{m12}\{r_{o12,2} \parallel r_{o10} \parallel [r_{\pi 11} + (\beta + 1)(R_{15} + R_{16})]\} \tag{5.37}$$

The exact closed-loop gain of the circuit then becomes:

$$V_{REF} = \frac{A}{1 + \frac{R_{15}}{R_{15}+R_{16}}A} V_{BG} \tag{5.38}$$

For practical design purposes, it is not necessary to analyze the exact gain equation. The simplified schematic is shown in Figure 5-20. An op amp connected in feedback forces the input voltages to be approximately equal. Therefore:

$$\begin{aligned} V_{BG} &= \frac{R_{15}}{R_{15}+R_{16}} V_{REF} \\ V_{REF} &= \left(1+\frac{R_{16}}{R_{15}}\right) V_{BG} \end{aligned} \tag{5.39}$$

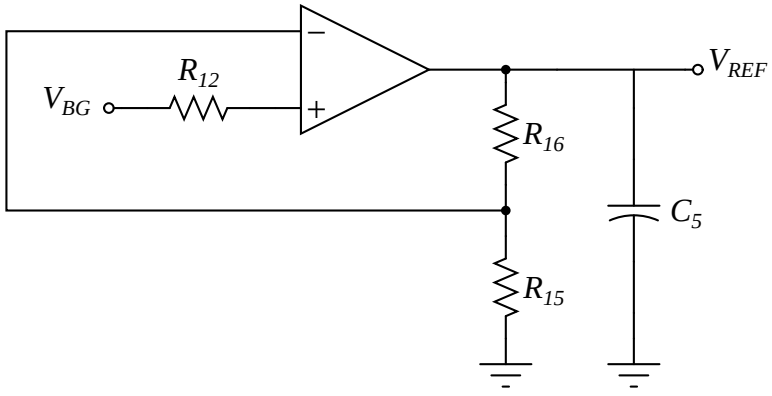


Figure 5-20: Simplified voltage regulator diagram.

This is the same result obtained in equation (5.38), with A taken to be very large [1]. V_{BG} is approximately 1.2 V, so a reasonable choice for R_{15} and R_{16} is $5.1\,k\Omega$ and $5.6\,k\Omega$, respectively, which results in a reference voltage V_{REF} of about 2.5 V.

R_{12} is chosen to be 160 Ω, to prevent any ringing to the base of $Q_{12,1}$. The purpose of C_4 is to provide dominant-pole compensation to the amplifier for stability considerations. It provides a low frequency pole that forces the magnitude of the frequency response of the amplifier to crossover before the phase reaches 180°. Therefore, it provides enough phase margin to ensure the stability of the amplifier. The value of C_4 is chosen to provide the necessary phase margin. In this case, a 22 nF results in a phase margin of approximately 40°, as will be shown in the simulation, but this is acceptable in this case because the output is slew-rate limited. Noting from equation (5.37) that the resistance seen at the node on top of C_4 is A/g_{m12}, it can be seen that

[1] One can easily verify that A is at least three orders of magnitude larger than 1, and since R_{15} and R_{16} have the same order of magnitude, the term $\frac{R_{15}}{R_{15}+R_{16}} A \gg 1$ dominates the denominator.

the dominant pole occurs at:

$$f_{dominant} = \frac{g_{m12}}{2\pi A C_4} \approx 57\,\text{Hz} \tag{5.40}$$

C_5 acts as a bypass capacitor, and thus ensures a steady noiseless voltage reference. It results in a pole that is the second most dominant pole in this circuit. Noting that the resistance at this node near the pole frequency is around $1/g_{m12}$, this pole occurs at:

$$f_{C_5} = \frac{g_{m12}}{2\pi C_5} \approx 53\,k\text{Hz} \tag{5.41}$$

The last but important feature of this circuit is the tail bias current. The tail current is generated by the PTAT voltage V_{PTAT}, which is generated in the bandgap and references board, and R_{11}. This results in a PTAT tail current. This current is then mirrored through Q_1 and Q_2 to form a PTAT tail current source I_{EE} for the differential pair. This results in g_{m12} to be independent of temperature. Assuming $I_{EE} = \gamma T$:

$$g_{m12} = \frac{I_{EE}}{2V_T} = \frac{qI_{EE}}{2kT} = \frac{q\gamma}{2k} \tag{5.42}$$

R_{13} and R_{14} are chosen to be $150\,\Omega$, and serve as degeneration resistors to improve the matching of Q_1 and Q_2. A possible choice for the tail current would be 0.8 mA. Writing KVL in the bias circuit:

$$V_{PTAT} - R_{11}I_{EE} - 0.6 - 150I_{EE} = 0 \tag{5.43}$$

$$R_{11} = \frac{V_{PTAT} - 0.6 - 150I_{EE}}{I_{EE}} \approx 5.6\,k\Omega \tag{5.44}$$

- Error Amplifier

The error amplifier circuit is shown in Figure 5-21. The purpose of this circuit is to compare the output voltage of the buck converter v_{FB} with a pre-chosen reference

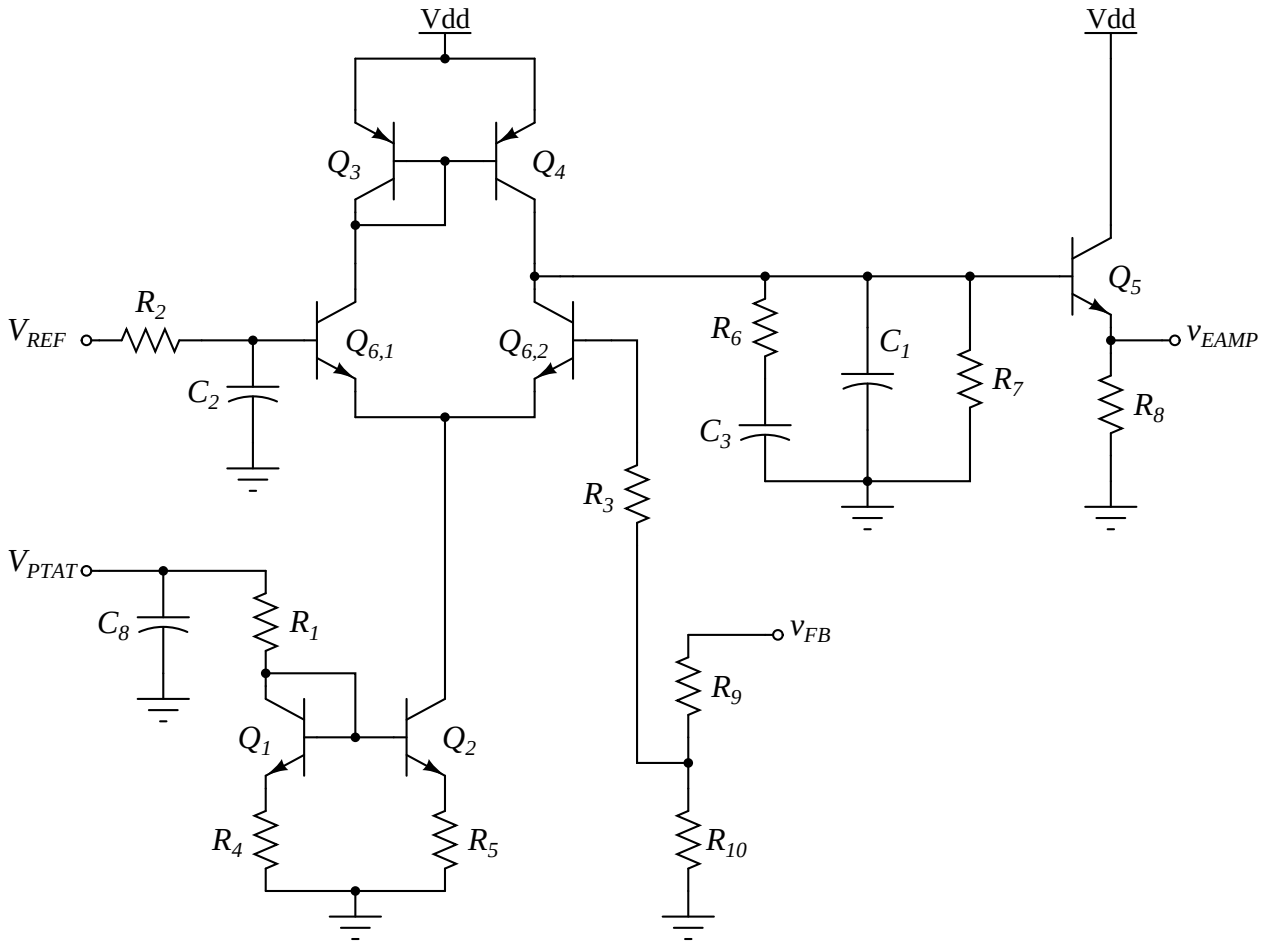


Figure 5-21: Circuit schematic of the error amplifier.

voltage V_{REF}, and to amplify and compensate the difference between them to give an output voltage v_{eamp}. This voltage sets the maximum high-side switch current (thus inductor current) during which this switch is on. In other words, it dynamically sets the peak inductor current for the current-mode controller. This circuit is thus the heart of the buck converter controller, since it implements the actual control transfer function.

A regulated voltage of 5 V is needed at the output of the buck converter. The reference used in this circuit is the 2.5 V reference provided by the voltage regulator. Therefore, v_{FB} is passed through the resistive divider R_9 and R_{10}, which divides the voltage by 2. Both R_9 and R_{10} are chosen to be $5.6\,k\Omega$. R_2 and R_3, chosen to be $160\,\Omega$, and serve to protect the bases of the matched transistor pair Q_6 from any

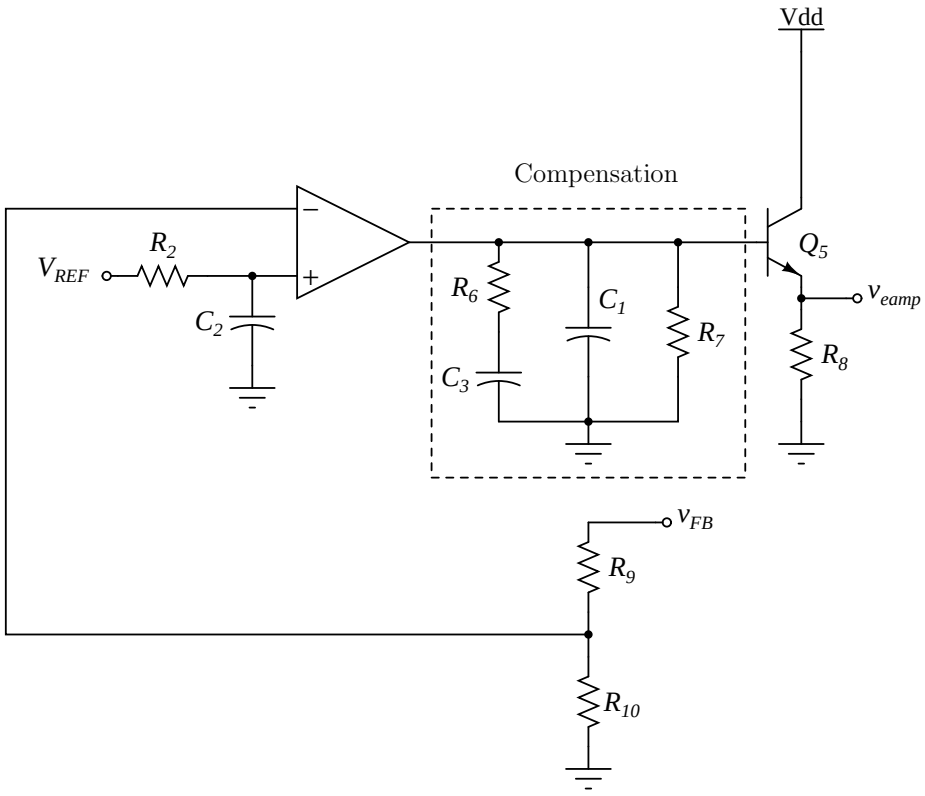


Figure 5-22: Simplified error amplifier diagram.

possible ringing. C_2, along with R_2, forms a low-pass filter to ensure a steady ripple-free voltage reference; a reasonable choice of C_2 would be $1\,\mu$F. The 2.5 V reference and $v_{FB}/2$ are the two inputs to a differential pair amplifier, whose output is then connected to a compensation network and terminated by an emitter-follower output stage.

The compensation network implements the control transfer function. Figure 5-22 shows a simplified diagram of the error amplifier, in which the compensation network is clearly labeled. R_7 is designed to have a relatively very large value (1 $M\Omega$), and will be treated as an open circuit. It causes the transfer function to have a very large but finite gain at frequencies close to dc. Defining the error voltage v_{err} to be

$V_{REF} - v_{FB}/2$, we get the transfer function:

$$\begin{aligned} \frac{v_{eamp}}{v_{err}} &= g_{m6}\left[\left(R_6 + \frac{1}{sC_3}\right) \parallel \frac{1}{sC_1}\right] \\ &= \frac{R_6C_3s+1}{s\left(R_6\frac{C_1C_3}{C_1+C_3}s+1\right)} \cdot \frac{g_{m6}}{C_1+C_3} \end{aligned} \tag{5.45}$$

The transfer function in equation (5.45) gives the flexibility of implementing more than one type of controller. Without C_1, the transfer function implements a Proportional-Integral (PI) controller. With the addition of C_1, an extra pole is added for additional flexibility in the controller design. The transfer function in equation (5.45) has one pole at 0 Hz [2], and one other pole and zero, the location of which can be set by R_6, C_1, and C_3. If one chooses R_6 to be $510\,\Omega$, and both C_1 and C_3 to be $0.47\,\mu$F, then the pole and zero locations occur at:

$$f_{pole} = \frac{1}{2\pi R_6\frac{C_1C_3}{C_1+C_3}} \approx 1.3\,k\text{Hz} \tag{5.46}$$

$$f_{zero} = \frac{1}{2\pi R_6C_3} \approx 664\,\text{Hz} \tag{5.47}$$

The tail bias current circuit is almost identical to that of the voltage regulator. The PTAT voltage is bypassed with C_8, which is chosen to be $0.1\,\mu F$, since V_{PTAT} is created in the bandgap and references board. Note that since the error amplifier and regulator are on the same board, one bypass can be enough (thus no bypass in the regulator current bias circuit). Just like in the regulator circuit, degeneration resistors R_4 and R_5 are $150\,\Omega$, used to improve transistor matching. The tail current I_{EE} is chosen to be 1.2 mA. Following the procedure in equation (5.43):

$$R_1 = \frac{V_{PTAT} - 0.6 - 150I_{EE}}{I_{EE}} \approx 3.6\,k\Omega \tag{5.48}$$

Finally, R_8 is chosen to be $10\,k\Omega$, which limits the maximum current at the output stage to 1.2 mA. Even though the circuit appears to be open-loop, its output goes

[2]The effect of a finite R_7 causes the pole to be very close to 0 Hz, but not exactly at 0 Hz.

Table 5.2: Summary of component values used in the sample design of the error amplifier and 2.5 V reference board

Component	**Value**	**Component**	**Value**
R_1	$3.6\,k\Omega$	C_1	$0.47\,\mu$F
R_2	$160\,\Omega$	C_2	$10\,\mu$F
R_3	$160\,\Omega$	C_3	$0.47\,\mu$F
R_4	$160\,\Omega$	C_4	22 nF
R_5	$160\,\Omega$	C_5	$0.1\,\mu$F
R_6	$510\,\Omega$	C_6	$10\,\mu$F
R_7	$1\,\text{M}\Omega$	C_7	$0.1\,\mu$F
R_8	$10\,k\Omega$	C_8	$0.1\,\mu$F
R_9	$5.6\,k\Omega$	R_{13}	$150\,\Omega$
R_{10}	$5.6\,k\Omega$	R_{14}	$150\,\Omega$
R_{11}	$5.6\,k\Omega$	R_{15}	$5.1\,k\Omega$
R_{12}	$160\,\Omega$	R_{16}	$5.6\,k\Omega$

to the comparator, which eventually drives the switches of the buck power stage, the output of which is connected to the input of the error amplifier circuit. Thus, the overall system is closed-loop, and the dc operating points automatically get adjusted.

Table 5.2 shows a summary of the component values used in the error amplifier and 2.5 V reference circuits.

SPICE Simulations

Figure 5-23 below shows the frequency response of the open-loop voltage regulator circuit. The effect of the dominant pole can be easily seen from the graph, and its location can be clearly seen to occur very close to 57 Hz. The cursors on the phase plot show that the phase at the unity gain frequency is about $-140°$, thus giving a phase margin of 40°. The closed-loop frequency response is shown in Figure 5-24.

Figure 5-25 shows the step response of the closed-loop voltage regulator. The input step voltage resembles applying the bandgap voltage in the form of a step function, i.e. $V_{BG}u(t)$. It can be seen that the output settles to the correct 2.5 V

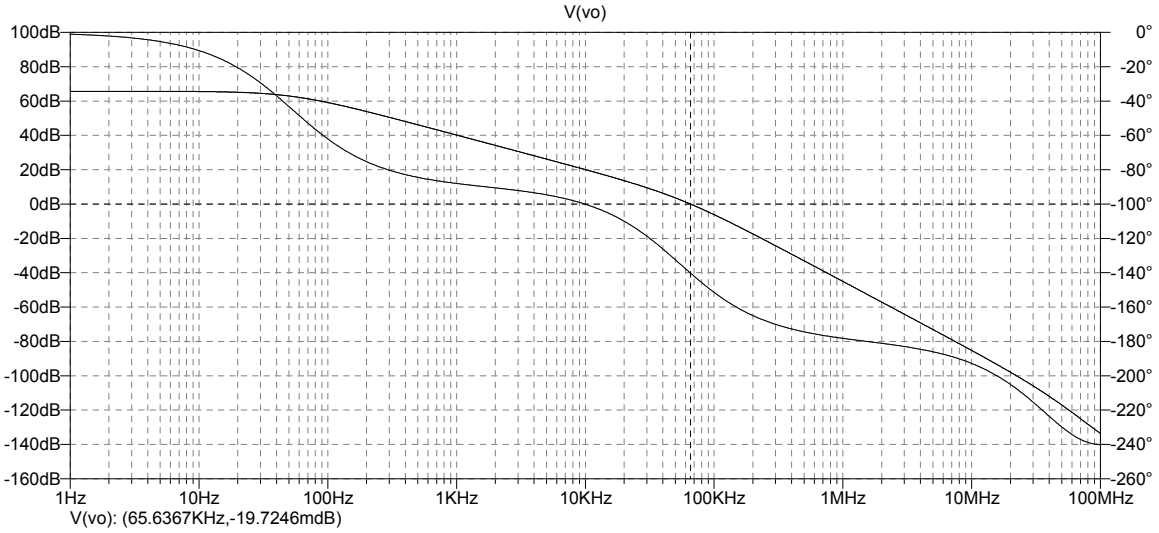


Figure 5-23: Simulation showing the frequency response of the voltage regulator in open-loop.

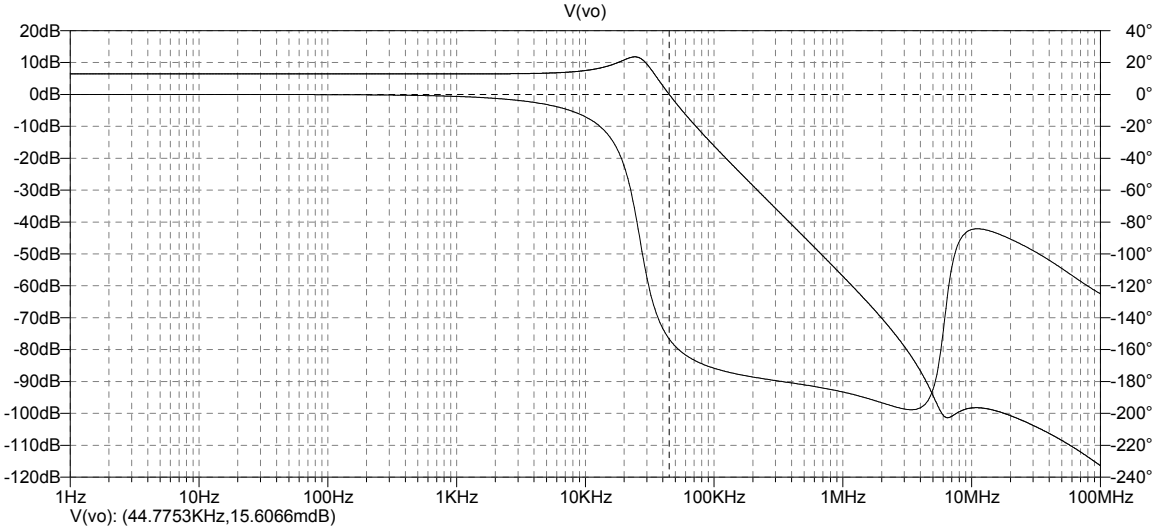


Figure 5-24: Simulation showing the frequency response of the closed-loop voltage regulator.

value in less than 0.2 ms. Also, the effect of slew-rate limiting is evident.

Figure 5-26 shows the frequency response of the error amplifier circuit. The two poles and the zero can be seen on the plot. The "bump" shape in the phase comes from the fact that there is a pole that is very close to the zero, as was shown in equations (5.46) and (5.47).

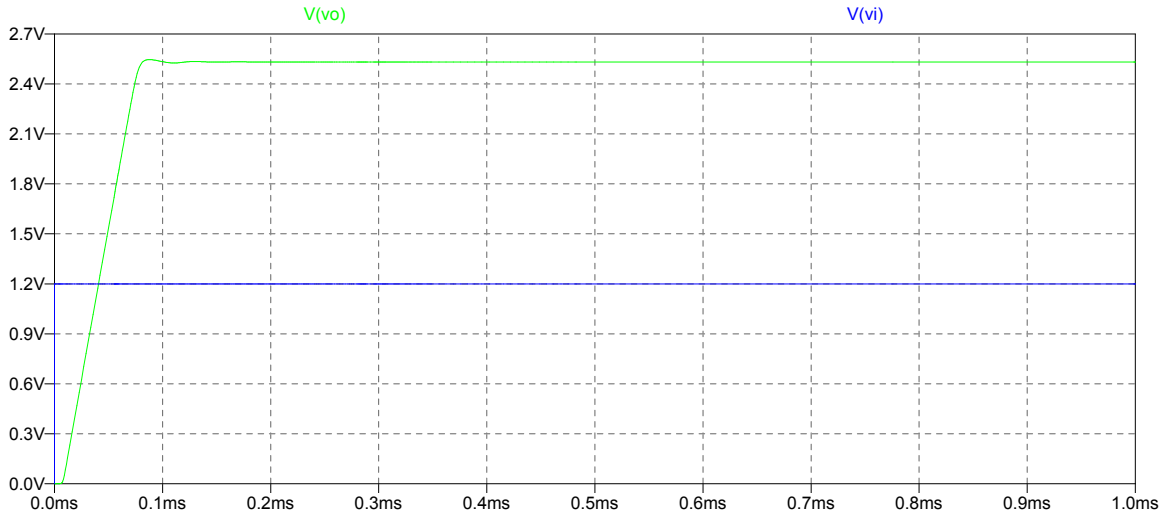


Figure 5-25: Simulation showing the step response of the voltage regulator.

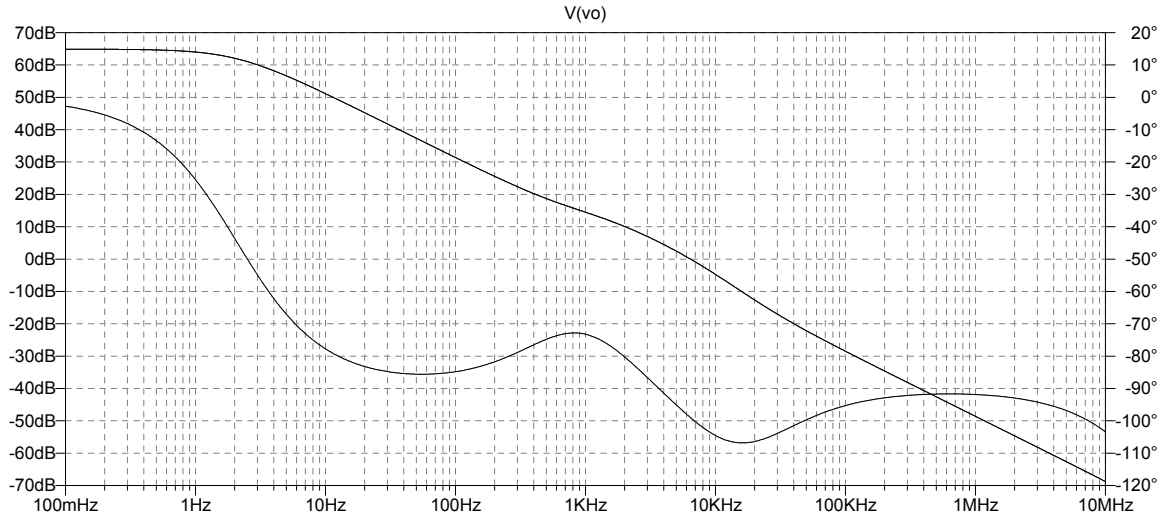


Figure 5-26: Simulation showing the frequency response of the error amplifier.

Experimental Result

Figure 5-27 shows the experimental result of a step applied to the reference voltage of the error amplifier circuit. The compensation values used result in no peak overshoot, at the expense of a slower settling time.

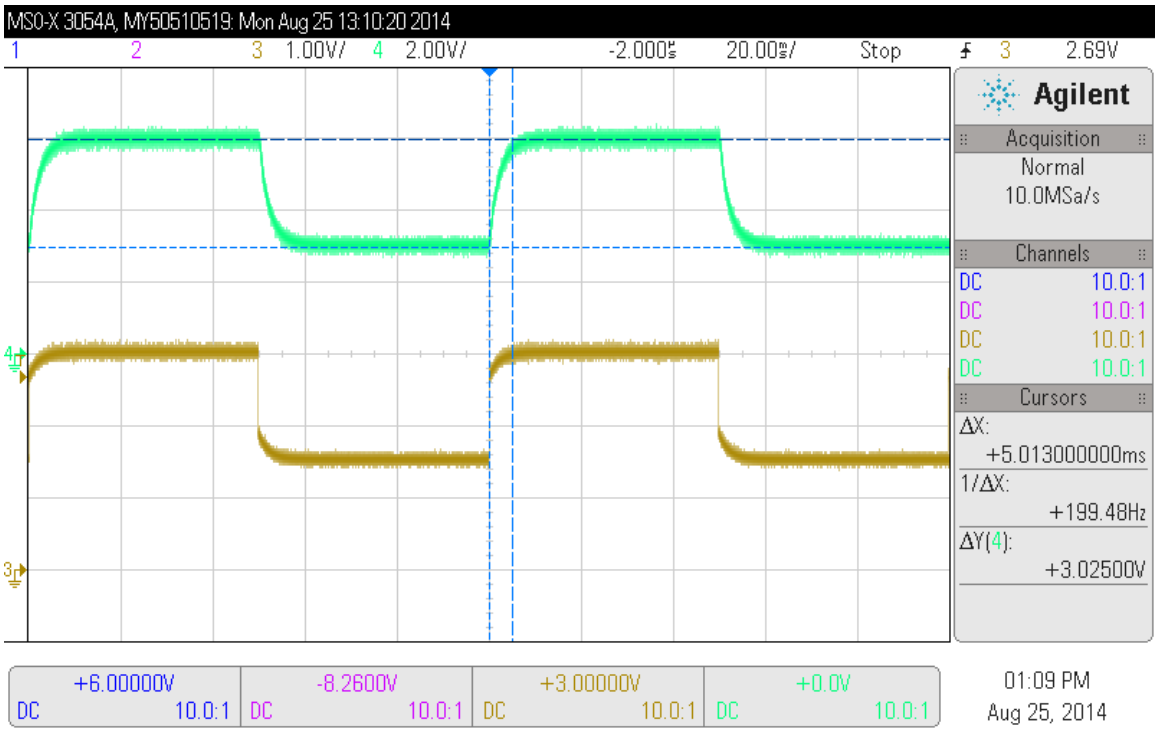


Figure 5-27: Experimental result showing the response of the output of the buck power stage to a step in the reference in the error amplifier circuit.

5.2.3 Comparator and Latch

The comparator and latch board contains the circuit block that is responsible for performing the comparison between the high side switch current and the maximum allowable inductor current commanded by the controller. The result of this comparison is used to generate appropriate PWM signals that control the operation of the gate drive circuit and thus the switches of the buck power stage.

Circuit Description

- Comparator

Figure 5-28 shows the comparator circuit. The comparator is a mixed-signal module that takes in two analog inputs and produces a digital logic output. The circuit is composed of a differential pair stage formed by Q_3 and Q_4. However, as opposed to the normal operation of the differential pair, this pair operates in large-signal mode, so the full bias current flows through only one of the two transistors. When the output

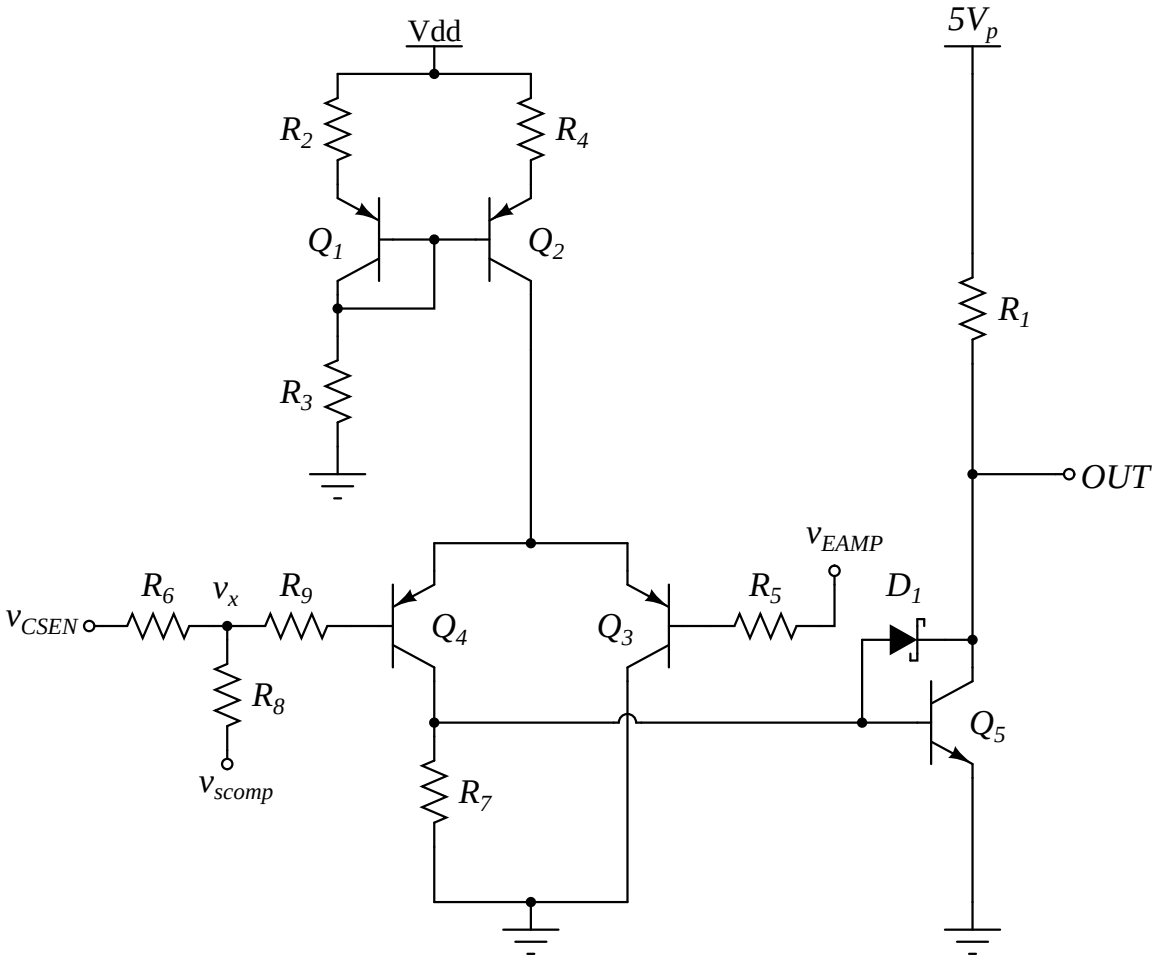


Figure 5-28: Transistor-level implementation of the comparator

of the error amplifier circuit v_{EAMP} is larger than the voltage v_x, Q_4 is on, turning on Q_5, thereby pulling the output voltage OUT low. When v_x exceeds v_{EAMP}, Q_3 is on, which pulls the bas of Q_5 low, turning it off. The output is then pulled up to the 5 V rail.

The node v_x is the output of the current sense amplifier, with an added slope compensating ramp. The reason for this is that in current-mode control, the converter is unstable for duty ratios larger than 0.5. Node v_x is given by:

$$v_x = \left(\frac{R_8}{R_6 + R_8}\right) v_{CSEN} + \left(\frac{R_6}{R_6 + R_8}\right) v_{scomp} \tag{5.49}$$

If the slope of the rising current of the inductor is m_L, then the slope of the current sense voltage v_{CSEN} is given by $R_{sense}Gm_L$, where G is the gain of the current sense

amplifier. If the slope of the slope compensating ramp is denoted by m_{scomp}, then the slope of v_x, denoted by m_x, is found to be:

$$m_x = \underbrace{\left(\frac{R_8}{R_6+R_8}\right) R_{sense} G m_L}_{\substack{\text{current sense} \\ \text{term}}} + \underbrace{\left(\frac{R_6}{R_6+R_8}\right) m_{scomp}}_{\substack{\text{compensation} \\ \text{term}}} \tag{5.50}$$

Typically, we require the compensation term to be some percentage M of the current sense term, usually greater than 0.5. This yields the following relation between the resistor values:

$$\frac{R_6}{R_8} = \left(\frac{m_L}{m_{scomp}}\right) M R_{sense} G \tag{5.51}$$

For our sample demonstration, we chose R_6 and R_8 to be $270\,\Omega$ and $270\,k\Omega$, respectively. If we bias the top current source formed by Q_1 and Q_2 to source 2 mA, then the current source resistors can be chosen as follows:

$$R_2 = R_4 = 150\,\Omega \tag{5.52}$$

$$R_3 = 5.6\,k\Omega \tag{5.53}$$

R_5 and R_9 are base protection resistors, chosen to be $160\,\Omega$. R_1 is a $1\,k\Omega$ pull-up resistor. R_7 needs to have a voltage higher than 0.6 V when the 2 mA bias current is flowing through it. A $510\,\Omega$ resistor is chosen.D_1 is a Schottky diode to prevent Q_5 from saturating.

- Latch

The comparator circuit is followed by a latch and some digital logic gates that generate the PWM signals needed by the gate drive circuits. Figure 5-29 shows the full block diagram.

When the $PWM0$ signal is high, the low side switch should turn on, and the high side switch should turn off. The comparator output and the inverted blank signal and fed to an AND gate (implemented as a NAND with an inverter). The output of this is a blanked signal, which acts as the "reset" input to the RS latch implemented

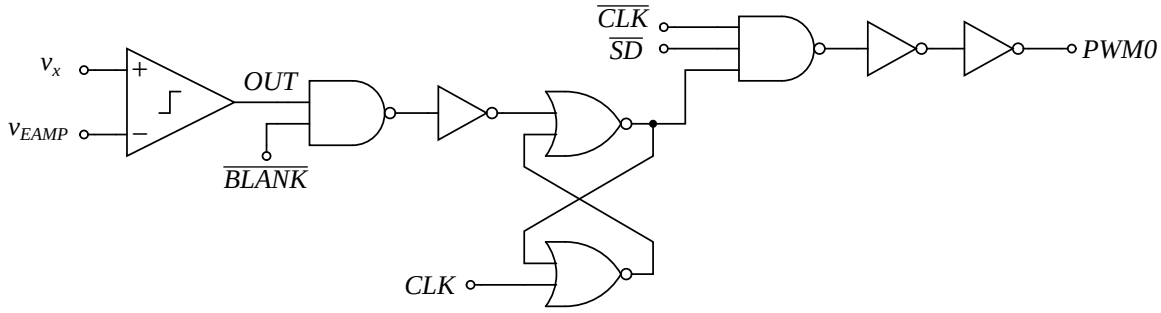


Figure 5-29: Block diagram of the comparator and latch circuit

by the two NOR gates. The other NOR gate has the clock pulse signal CLK as its "set" input. The RS latch is followed by a 3-input NAND gate. When any of its inputs is low, the output of the gate will be high, resulting in a high $PWM0$ signal. The last two inverters act as buffers to the output signal. Buffers are used in the logic portions of the boards to cancel the effect of ground bounce. Therefore, when the output of the comparator is high, it commands the low side switch to turn on, and turns off the high side switch, resulting in the current sense voltage (and thus v_x) to drop to zero, which in turn causes the output of the comparator to go back low.

The logic gates were implemented using transistor-level CMOS logic circuits, as shown in Figures 5-30, 5-31, 5-32, and 5-33.

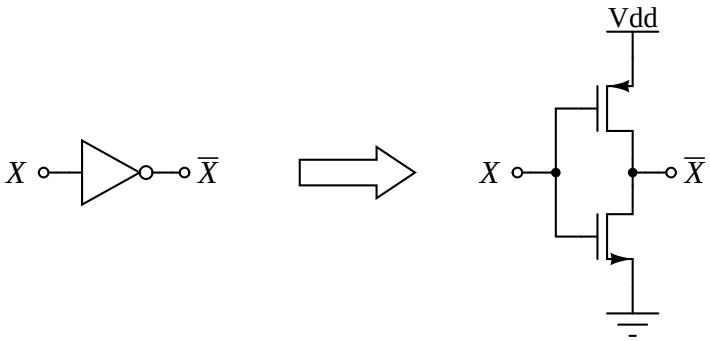


Figure 5-30: NOT gate

Table 5.3 shows a summary of the component values used for the comparator and latch board.

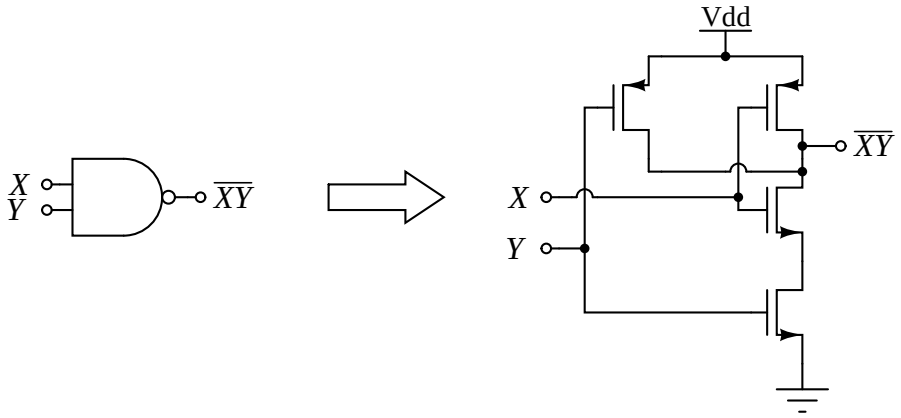


Figure 5-31: NAND gate (with two inputs)

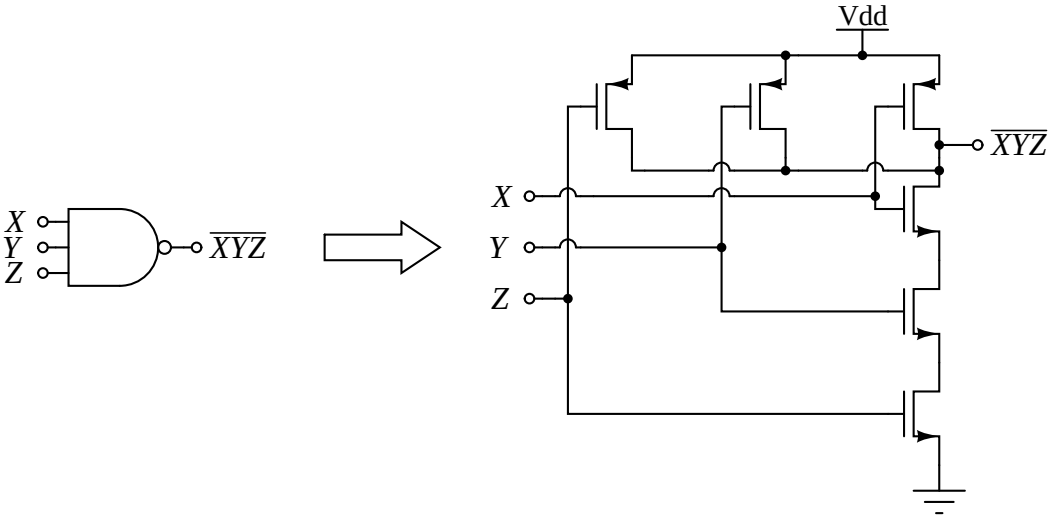


Figure 5-32: NAND gate (with three inputs)

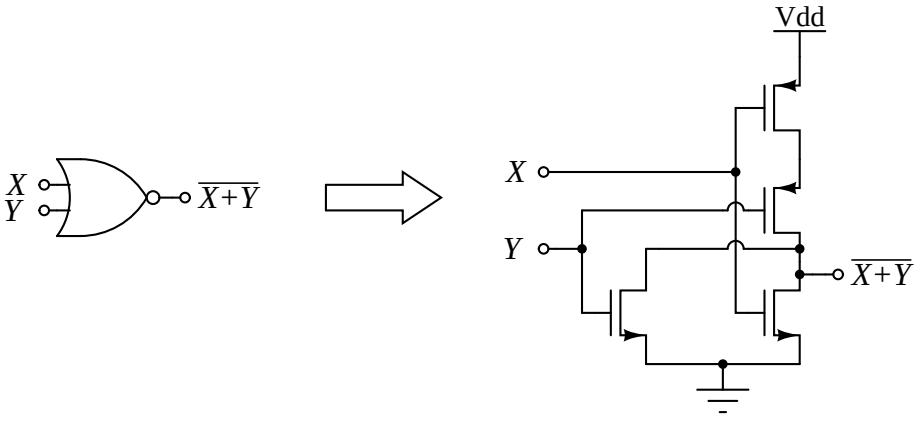


Figure 5-33: NOR gate

Table 5.3: Summary of component values used in the sample design of the comparator and latch board

Component	Value	Component	Value
R_1	$1\,k\Omega$	C_1	$0.1\,\mu$F
R_2	$150\,\Omega$	C_2	$10\,\mu$F
R_3	$5.6\,k\Omega$	C_3	$10\,\mu$F
R_4	$150\,\Omega$	C_4	$0.1\,\mu$F
R_5	$160\,\Omega$		
R_6	$270\,\Omega$		
R_7	$510\,\Omega$		
R_8	$270\,k\Omega$		
R_9	$160\,\Omega$		

Simulation Result

Figure 5-34 shows the result of simulating the comparator circuit. The current sense signal was emulated in SPICE, and the output can be seen to be high when the current sense voltage exceeds the error amplifier voltage.

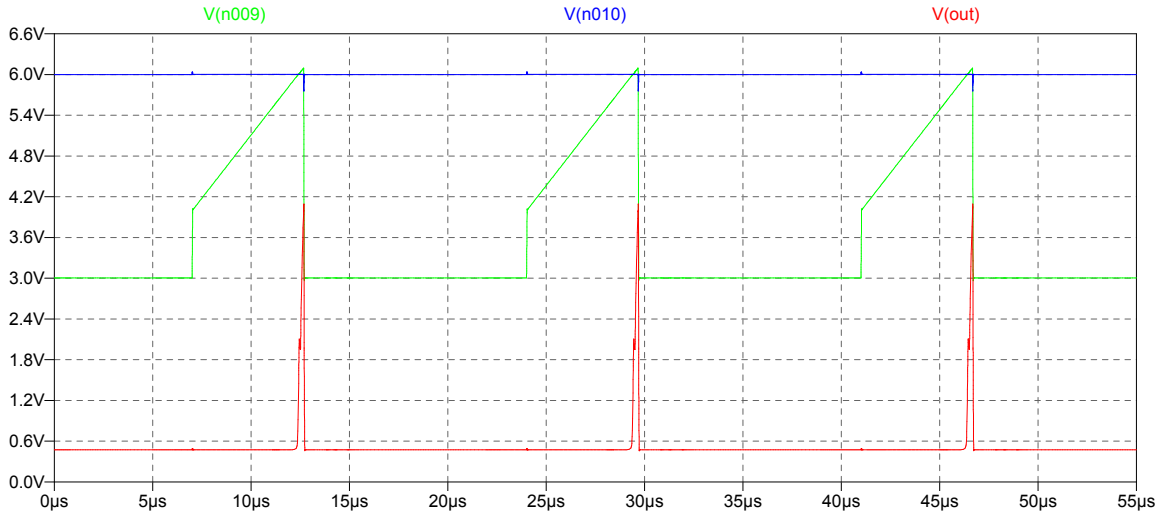


Figure 5-34: Simulation showing the output of the comparator relative to its two inputs.

Experimental Result

Figure 5-35 shows the experimental result of the comparator circuit during the operation of the converter. As expected, as soon as the high side current sense signal just exceeds the error amplifier signal, the comparator output goes high. It goes low after that when the current sense voltage drops.

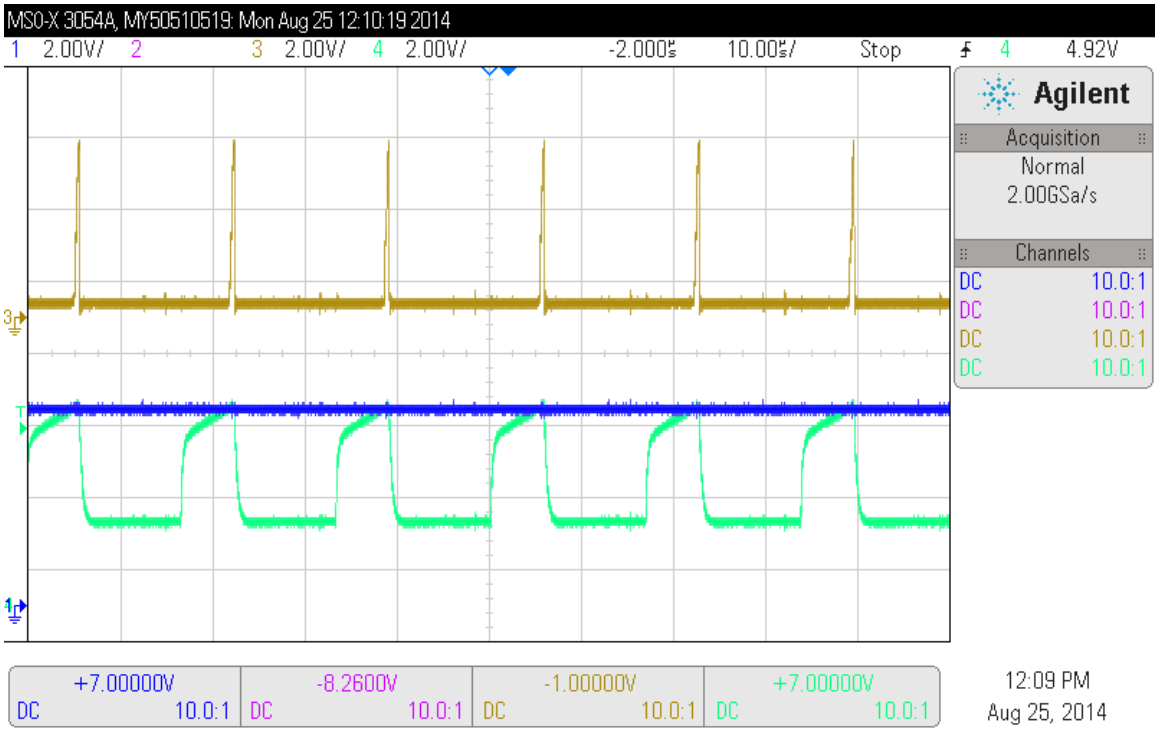


Figure 5-35: Experimental result showing the output of the comparator circuit relative to its inputs, which are the current sense signal and the error amplifier output.

5.2.4 High Side Current Sense

This circuit measures and amplifies the voltage across a current sense resistor, which is placed in series with the high-side switch of the buck converter. The current sense amplifier provides a measure of the inductor current to the controller while the high-side switch is on. This will be needed by the controller in order to decide whether or not the inductor current has reached the maximum peak value.

Circuit Description

Figure 5-36 shows the circuit schematic of the current sense amplifier. The circuit can be recognized as an open-loop trans-conductance amplifier. This implementation has a much faster response than a closed-loop op amp.

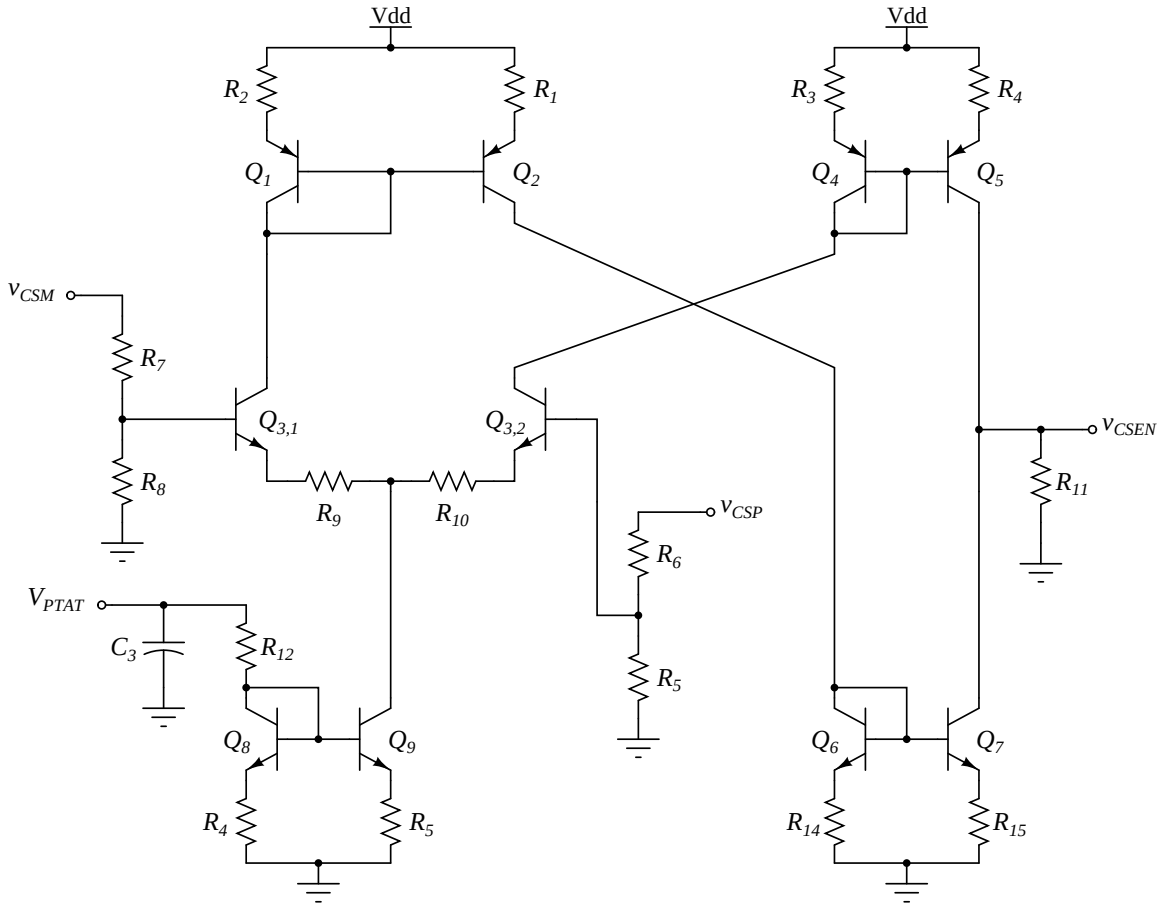


Figure 5-36: Circuit schematic of the current sense amplifier.

The differential pair circuit (with matched transistors) takes the differential voltage $v_{INP} - v_{INM}$ as an input, and outputs a current which, when passed through the output resistance R_{11}, generates an output voltage given by:

$$v_{CSEN} = i_{CSEN} R_{11} = g_{m3}(v_{INP} - v_{INM}) R_{11} \tag{5.54}$$

The problem with this result is that the output current (and voltage) is dependent on temperature, since $g_{m3} = qI_C/kT$. Thus, V_{PTAT} is used to drive the current

source implemented by transistors Q_8 and Q_9. This causes the collector currents to be also PTAT, and therefore the output current (and thus voltage) is independent from temperature.

The two emitter resistors are placed in the differential pair in order to increase the linear range by a factor of about 5. This way, the amplifier still behaves linearly up to a differential input voltage $v_{INP} - v_{INM} \approx 125\,\mathrm{mV}$.

$$\begin{aligned} \frac{I_{EE}R_E}{2V_T} &= 5 \\ R_E &= \frac{10V_T}{I_{EE}} \approx 62\,\Omega \end{aligned} \tag{5.55}$$

since I_{EE} is chosen to be about 4 mA. The design equations for the I_{EE} current source are as follows:

$$I_{EE} = \frac{V_{PTAT} - 0.6}{R_{12} + R_{13}} \tag{5.56}$$

$$R_{13} = R_{16} \tag{5.57}$$

The mirror degeneration resistors are chosen to be $R_{13} = R_{16} = 75\,\Omega$, and finally R_{12} is then chosen to be $1.1\,k\Omega$.

However, emitter degeneration due to R_9 and R_{10} reduces the gain by the same factor as the increase in linearity, namely 5. Therefore, since the final desired gain of the circuit is 48, the value of R_{11} is chosen such that the gain becomes $48 \times 5 = 240$. The collector current is $I_{EE}/2 = 2\,\mathrm{mA}$, and thus:

$$g_m = \frac{I_C}{V_T} = 0.08\,\mho \tag{5.58}$$

$$a_{vd} = \frac{v_{CSEN}}{v_{INP} - v_{INM}} = g_m R_{11} = 240 \tag{5.59}$$

$$R_{11} = \frac{240}{0.08} = 3\,k\Omega \tag{5.60}$$

The common mode gain of the circuit is zero, since no current flows through the

output at common mode, assuming no mismatch between the current mirrors:

$$a_{vc} = 0 \tag{5.61}$$

The mirror ratios of the current mirror formed by Q_1 and Q_2, and that formed by Q_6 and Q_7, are both $1:1$. The mirror degeneration resistors are thus chosen to be $R_1 = R_2 = R_{14} = R_{15} = 150\,\Omega$.

The biasing of the output stage of this circuit is important. If the mirror ratio of the current mirror formed by Q_4 and Q_5 is also $1:1$, then under the quiescent bias condition (i.e. when there is no differential input voltage), the output currents balance out and no current flows through R_{11}, resulting in $v_{CSEN} = 0$. One can realize why this is an inappropriate dc bias point, since this will saturate Q_7. This means that under bias conditions, Q_7 is not operating in the forward active regime, and will prevent the amplifier from behaving normally. To solve this problem, R_3 is chosen to be $150\,\Omega$ just as the other resistors, but R_4 is chosen to be $R_4 = R_3/2 = 75\,\Omega$. This will double the current through Q_5, resulting in a net current flowing through R_{11}. If everything is balanced, this net current will be close to $I_{EE}/2$. With the resistor values chosen above, this current is close to 1.85 mA, resulting in an output dc bias voltage close to 5 V.

The inputs of the transconductance amplifier (INP and INM) cannot be directly placed across the current sense resistor, because the common mode input voltage is usually very close to the supply voltage, which can reach up to 20 V. The control circuit is operating at 12 V, and therefore a 20 V common mode input would saturate the transistors in the circuit. The resistive voltage dividers at the inputs in Figure 5-36 divide the common mode input voltage by 2, thus preventing v_{INP} and v_{INM} from exceeding 12 V.

$$v_{INP} = \left(\frac{R_5}{R_5 + R_6}\right) v_{CSP} = \frac{v_{CSP}}{2} \tag{5.62}$$

$$v_{INM} = \left(\frac{R_8}{R_7 + R_8}\right) v_{CSM} = \frac{v_{CSM}}{2} \tag{5.63}$$

Table 5.4: Summary of component values used in the sample design of the current sense board

Component	Value	Component	Value
R_1	$150\,\Omega$	R_{12}	$1.1\,k\Omega$
R_2	$150\,\Omega$	R_{13}	$75\,\Omega$
R_3	$150\,\Omega$	R_{14}	$150\,\Omega$
R_4	$75\,\Omega$	R_{15}	$150\,\Omega$
R_5	$2.5\,k\Omega$	R_{16}	$75\,\Omega$
R_6	$2.5\,k\Omega$	C_1	$10\,\mu$F
R_7	$2.5\,k\Omega$	C_2	$0.1\,\mu$F
R_8	$2.5\,k\Omega$	C_3	$0.1\,\mu$F
R_9	$62\,\Omega$		
R_{10}	$62\,\Omega$		
R_{11}	$3\,k\Omega$		

SPICE Simulation

Figure 5-37 shows the simulation result of the current sense amplifier circuit. The result clearly shows how the output of the current sense circuit tracks the current flowing through the sense resistor. The sense resistor used has a value of $0.33\,\Omega$, and the current ramps up between 340 mA and 360 mA. Notice also how the output dc voltage is close to 5 V when no current is flowing through the sense resistor.

Experimental Result

Figure 5-38 shows the result of the current sense amplifier circuit. A current probe was used to measure the inductor current so that the two waveforms can be compared. The output of the current sense amplifier clearly tracks the inductor current when the high side switch is on.

5.2.5 Clock

This circuit generates the clock pulse that will periodically command the buck high-side switch to turn on. Since the converter control is current-mode, it is unstable

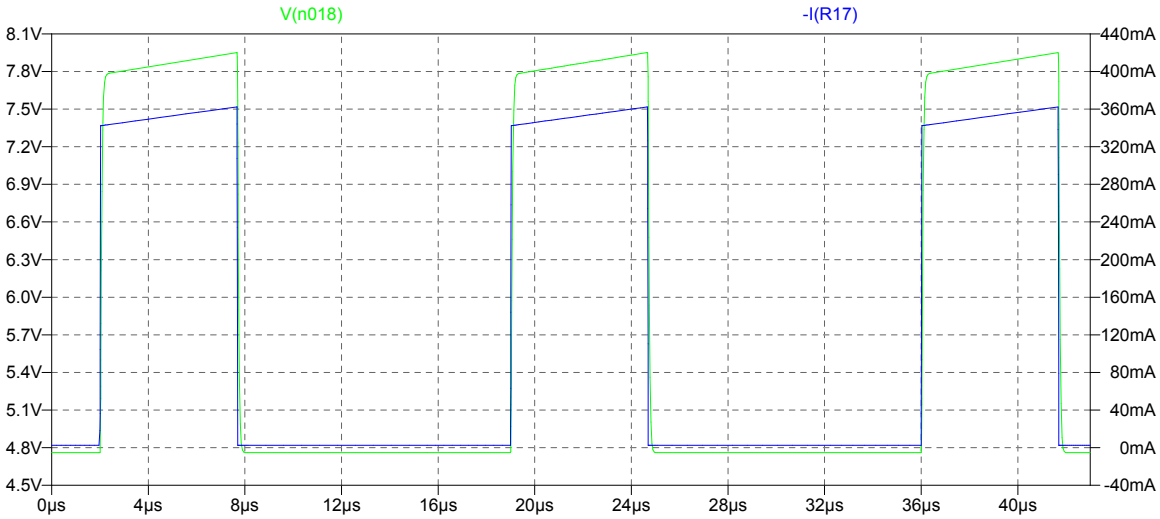


Figure 5-37: Simulation showing the output of the current sense amplifier. The current through the sense resistor emulates that of the high-side switch of the buck converter.

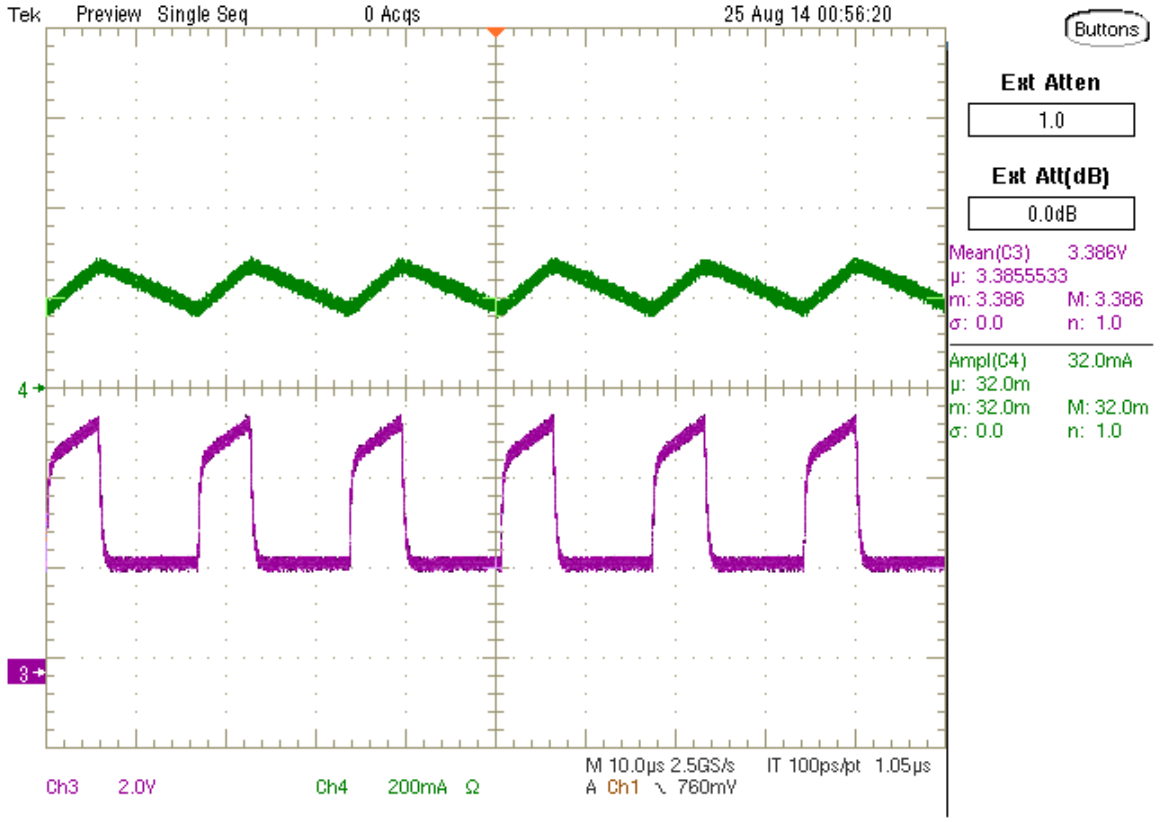


Figure 5-38: Experimental result showing the output of the current sense amplifier and the inductor current. The circuit clearly tracks the inductor current when the high side switch is on.

for duty ratios higher than 0.5 [26]. Thus, this circuit also generates the ramp signal needed for slope compensation. The circuit also implements leading-edge blanking, which prevents the controller from turning the high-side switch off due to the initial current spike at turn on (since that spike exceeds the maximum inductor current set by the control loop).

Circuit Description

Figure 5-39 shows the circuit. The clock pulse is generated using a single input

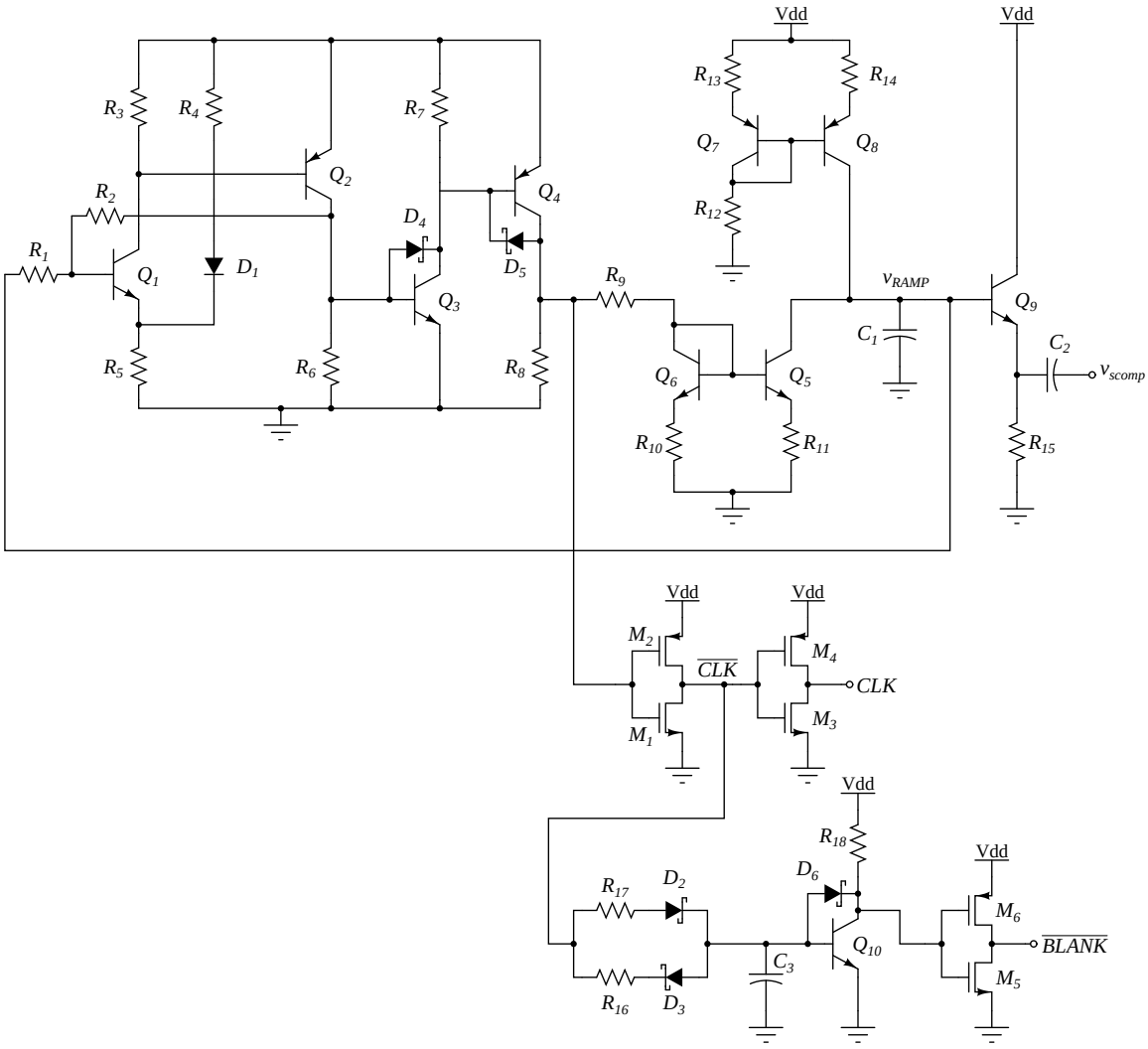


Figure 5-39: Clock circuit schematic.

Schmitt trigger circuit with positive feedback. The basic operation is illustrated

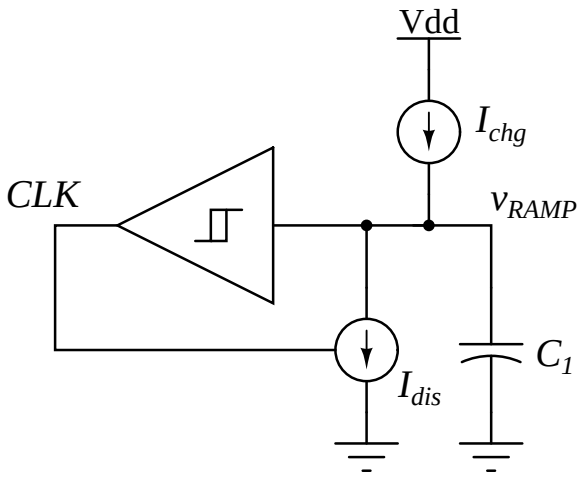


Figure 5-40: A simplified view of the clock circuit.

in Figure 5-40. When the output of the Schmitt trigger is low, the upper current source I_{chg} slowly charges capacitor C_1. When the voltage rises to a threshold voltage determined by the Schmitt trigger, the output of the trigger is high, and this turns on the lower current source I_{dis} (which by design is larger than I_{chg}). This causes the capacitor voltage to quickly ramp down until it reaches the lower threshold voltage level, after which I_{dis} is turned off and the process repeats. This results in a ramp voltage across C_1, and a clock pulse at the Schmitt trigger output.

The Schmitt trigger action is implemented by the first two stages using Q_1 and Q_2. When the collector of Q_2, which is the output of the Schmitt trigger, is low, both Q_1 and Q_2 are off, and R_4, R_5 and D_1 set the voltage at the emitter of Q_1 to be $(5 - 0.6)R_3/(R_3 + R_4)$. Note that R_3, R_4, and R_5 are chosen to be $11\,k\Omega$, and thus this voltage is around 2.2 V. Therefore, the base of Q_1 needs to reach about 2.8 V for it to turn on. Thus, we can calculate the first threshold voltage $V_{th,H}$ as follows:

$$\begin{aligned} 2.8 &= \left(\frac{R_2}{R_1 + R_2}\right) V_{th,H} \\ V_{th,H} &= \frac{2.8}{1 + R_1/R_2} \end{aligned} \tag{5.64}$$

The second threshold is calculated by considering the case when the collector of Q_2 is pulled up to 0.6 V, i.e. when Q_1 and Q_2 are on. The threshold for Q_1 to turn

off is approximately given by solving the following equation for $V_{th,L}$:

$$\left(\frac{R_2}{R_1+R_2}\right)V_{th,L}+\left(\frac{R_1}{R_1+R_2}\right)(0.6)=2.8 \tag{5.65}$$

R_1 and R_2 need to be relatively large such that the current that flows through them is negligible compared to the currents charging and discharging C_1. However, if they are too large, they will slow down the circuit operation. A reasonable tradeoff has to be made. A possible choice is $R_1 = 100\,k\Omega$ and $R_2 = 390\,k\Omega$. This results in thresholds of about 3.36 V and 3.52 V.

The next two stages at the output of the Schmitt trigger are simply buffering stages, and the Schottky diodes prevent saturation of the transistors. Also, MOSFETS $M1$-$M4$ form two CMOS inverters, which serve to buffer the output of Q_4 and result in a sharp well-behaved clock pulse CLK.

It can be seen that v_{RAMP} ramps up and down between $V_{th,L}$ and $V_{th,H}$, but so far no information was given on the duration of the ramp-up or ramp-down. The ramp-up duration corresponds to when the clock is low, and the ramp-down corresponds to the clock pulse duration.

I_{chg} charges up C_1 at a rate equal to $m_r = I_{chg}/C_1$. When CLK is high, the bottom current source is on, and the capacitor voltage discharges at a rate $m_f = (I_{dis}-I_{chg})/C_1$, i.e. the slope of the voltage is $-m_f$. From this information, the times t_r and t_f taken for the capacitor voltage to rise from $V_{th,L}$ to $V_{th,H}$ or fall from $V_{th,H}$ to $V_{th,L}$, respectively, can be calculated as follows:

$$t_r = \frac{V_{th,H}-V_{th,L}}{m_r}=\frac{C_1(V_{th,H}-V_{th,L})}{I_{chg}} \tag{5.66}$$

$$t_f = \frac{V_{th,L}-V_{th,H}}{-m_f}=\frac{C_1(V_{th,L}-V_{th,H})}{I_{chg}-I_{dis}} \tag{5.67}$$

It can be seen that I_{chg} and I_{dis} are the design handles that set both the duration of the clock pulse as well as the clock frequency, f_{sw}, which is given by:

$$\frac{1}{f_{sw}}=\frac{C_1(V_{th,H}-V_{th,L})}{I_{chg}}+\frac{C_1(V_{th,L}-V_{th,H})}{I_{chg}-I_{dis}} \tag{5.68}$$

A possible choice of the currents can be:

$$I_{chg} = 94.6\,\mu\text{A} \tag{5.69}$$

$$I_{dis} = 620\,\mu\text{A}, \tag{5.70}$$

which are found to produce a clock of frequency $f_{sw} \approx 60k\,\text{Hz}$. Resistors R_9-R_{11} are designed to implement I_{dis}, and R_{12}-R_{14} implement I_{chg}. Note that we will observe in the results section that there is a discrepancy between the simulation and experimental result due to the slow turn off of Q_1 relative to the falling ramp of v_{RAMP}. This effect will be explained later.

The last feature of this circuit is the leading-edge blanking. The blanking needs to be done for about 200 ns after the high-side switch of the buck converter turns on, which happens at the falling edge of the clock. The turn-on of a BJT is sharper and more precisely controllable than turn-off. Controlling the turn-on time can be achieved by controlling the time it takes a capacitor placed at the base to charge up to 0.6 V, as is done at the bottom section of Figure 5-39. One can charge C_3 using $\overline{CLK}$, where the time constant is controlled by R_{17} and C_3. The base voltage of Q_{10} is given by:

$$v_B = 5\left(1 - e^{-t/R_{17}C_3}\right) \tag{5.71}$$

Solving for the time taken t to raise the base voltage to 0.6 V yields:

$$t = -R_{17}C_3 \ln\left(1 - \frac{0.6}{5}\right) \tag{5.72}$$

Choosing $R_{17} = 1.9\,k\Omega$ and C_3 of 1 nF yields about 200 ns of time delay.

Table 5.5 shows a summary of the values of the components used in the clock board.

SPICE Simulation

The result of simulating the clock circuit is shown in Figure 5-41.

Table 5.5: Summary of component values used in the sample design of the clock board

Component	Value	Component	Value
R_1	$100\,k\Omega$	R_{13}	$7.5\,k\Omega$
R_2	$390\,k\Omega$	R_{14}	$7.5\,k\Omega$
R_3	$11\,k\Omega$	R_{15}	$10\,k\Omega$
R_4	$11\,k\Omega$	R_{16}	$5.1\,\Omega$
R_5	$11\,k\Omega$	R_{17}	$1.9\,k\Omega$
R_6	$20\,k\Omega$	R_{18}	$1\,k\Omega$
R_7	$1.2\,k\Omega$	C_1	$2.2\,\text{nF}$
R_8	$1.2\,k\Omega$	C_2	$1\,\text{nF}$
R_9	$510\,\Omega$	C_3	$1\,\text{nF}$
R_{10}	$75\,\Omega$	C_4	$10\,\mu\text{F}$
R_{11}	$910\,\Omega$	C_5	$0.1\,\mu\text{F}$
R_{12}	$39\,k\Omega$		

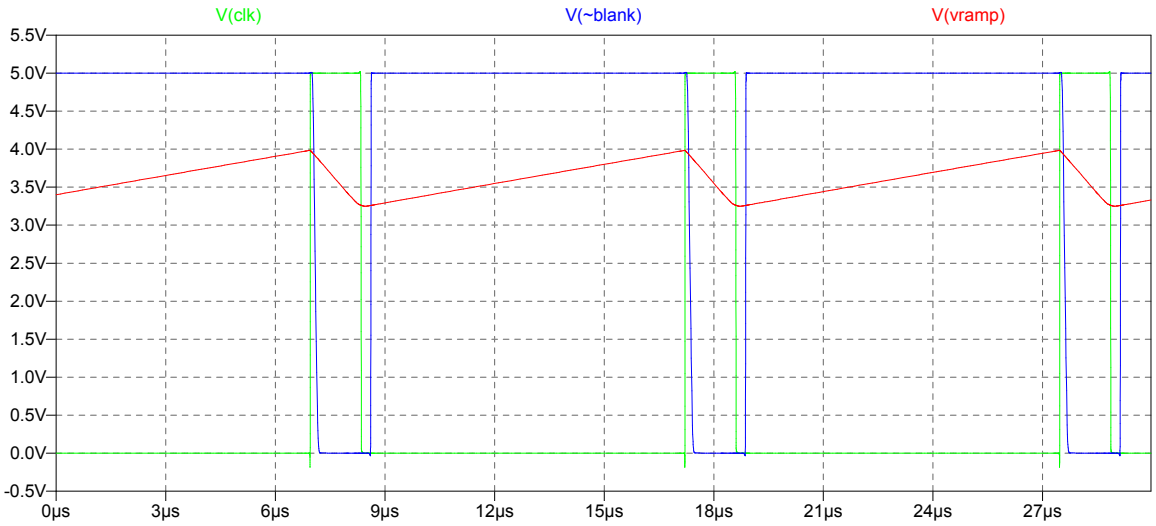


Figure 5-41: Simulation showing the clock pulse, the blanking, and the ramp signals.

Experimental Result

Figure 5-42 below shows the experimental result of the clock and the compensation ramp. Figure 5-43 shows the result of the leading-edge blanking. The reason for the difference in clock frequencies between the simulation and the experiment is elaborated on in the next chapter.

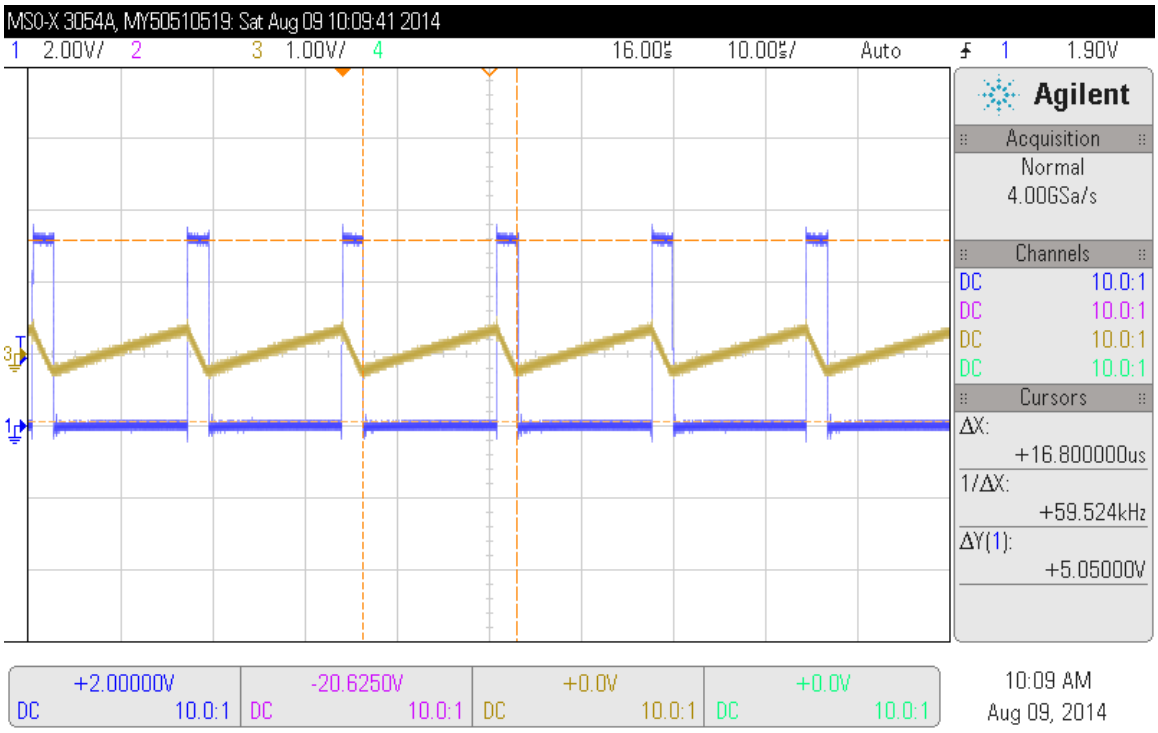


Figure 5-42: Experimental result showing the clock pulse and the ramp signal.

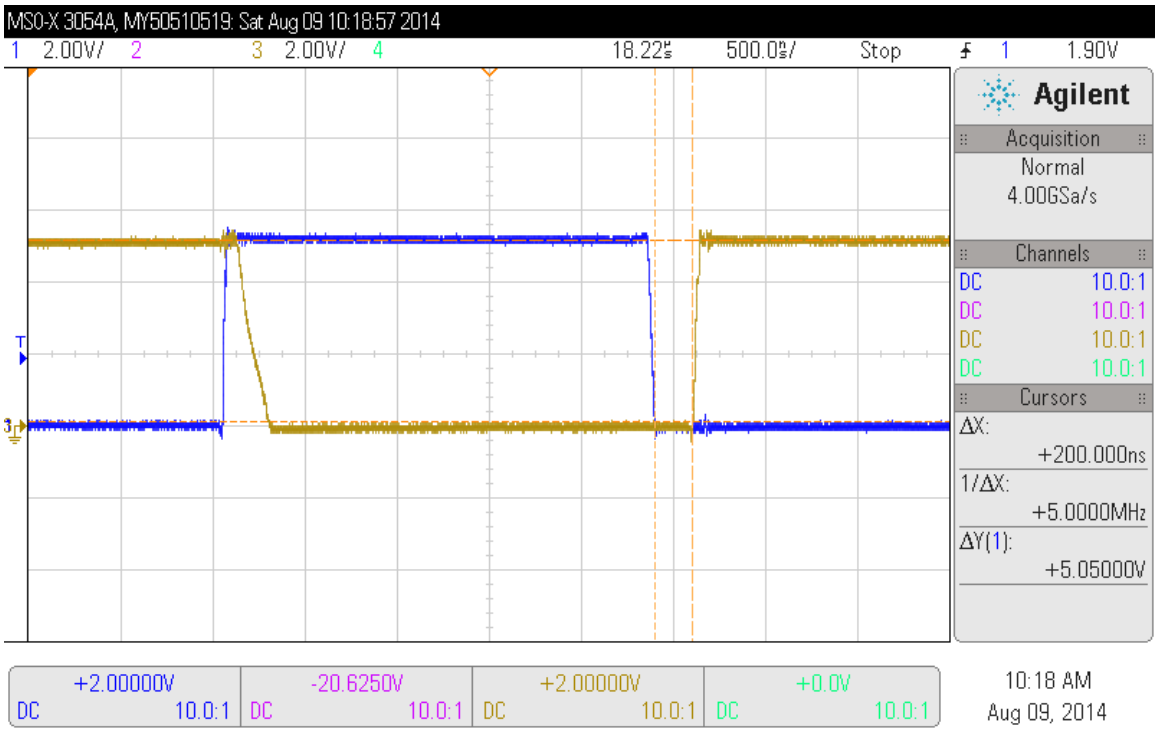


Figure 5-43: Experimental result showing the leading-edge blanking signal $\overline{BLANK}$.

5.2.6 Shutdown

The shutdown board contains protection circuitry that detects under-voltage or over-voltage on the input of the buck power stage, and sets a shutdown signal high or low accordingly. This shutdown signal is used by the comparator and latch as well as the gate drive boards to determine the mode of operation of the converter.

Circuit Description

Figure 5-44 shows the schematic of the shutdown circuit. The board uses an AND gate (NAND followed by an inverter) to produce the inverted shutdown signal SD . It can be seen that the output SD can go low if (a) the over-voltage signal is low, or (b) the under-voltage signal is low, or (c) a user-controlled switch is manually turned off. The manual switch sets the input of M_3 and M_7 high or low. This action is implemented using CMOS logic through transistors $M_1 - M_8$.

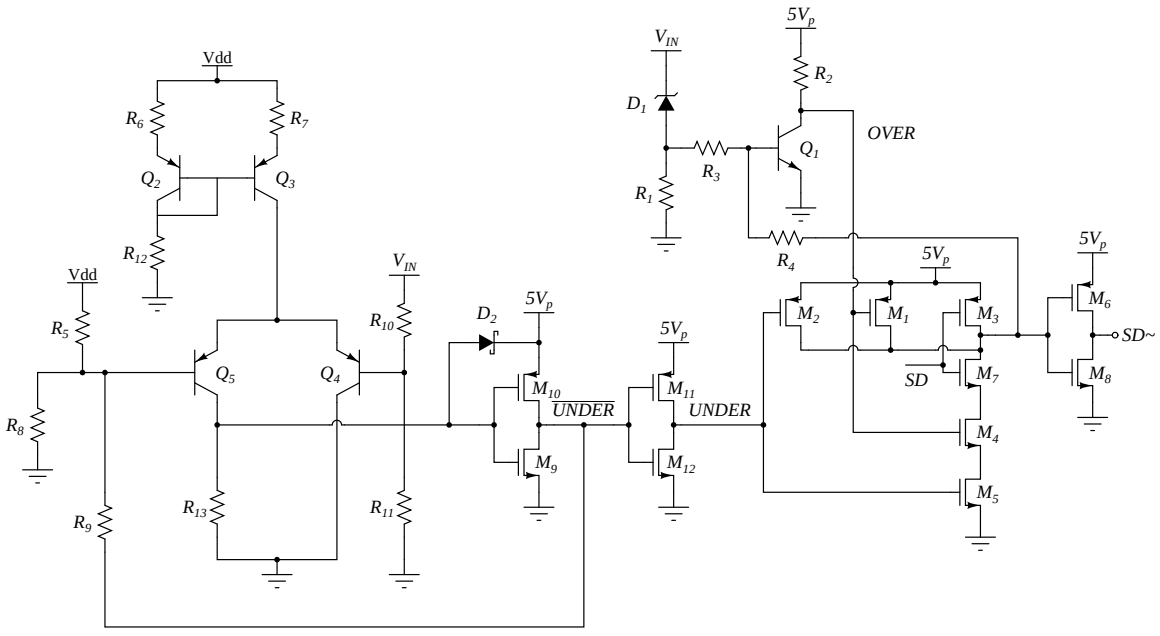


Figure 5-44: Shutdown circuit schematic.

Over-voltage

We require the converter to go into shutdown mode if its input voltage is beyond approximately 22 V. D_1 is a 22 V zener diode. When the input voltage to the buck

power stage increases a little beyond 22 V, Q_1 turns on, pulling the $OVER$ signal low. Thus, the shutdown signal is asserted high (or SD is low). R_1 and R_2 are pull-down and pull-up resistors, respectively, chosen to be $1\,k\Omega$ and $5.1\,k\Omega$. R_3 is a $160\,\Omega$ base protection resistor. R_4 is an optional resistor if hysteresis is needed. We chose a value of $100\,k\Omega$, so negligible hysteresis is used.

Under-voltage

The left section of the circuit in Figure 5-44 is used to detect an under-voltage condition. It consists of a comparator (similar to the one in the comparator and latch board) that runs from a supply Vdd of 15 V, with a positive feedback connection through resistor R_9. The comparator is implemented using a differential pair formed by Q_4 and Q_5, and biased by the top current source. This current source produces about 2 mA, and so the resistors R_6, R_7 and R_{12} were chosen to be $270\,\Omega$, $270\,\Omega$, and $6.8\,k\Omega$, respectively. Resistor R_{13} is chosen to be around $3.3\,k\Omega$, so that it can produces a high voltage to drive the inverter when current is passing through it.

When the input voltage is rising, we need the threshold voltage beyond which the converter leaves the under-voltage mode to be around 10 V. When the input voltage falls down, we need the threshold to be around 7 V. The positive feedback creates this hysteresis effect, resulting in one threshold voltage being higher than the other.

R_{10} and R_{11} are chosen to be $3.6\,k\Omega$ each to form a voltage divider that divides the input voltage V_{IN} by two. The divided voltage is the inverting input of the comparator.

When the output voltage of the comparator $\overline{UNDER}$ is 0, the threshold at the base of Q_5 is given by:

$$V_{th,L} = 15\left(\frac{R_8 \parallel R_9}{R_5 + R_8 \parallel R_9}\right) \tag{5.73}$$

When the comparator output is 5 V (high), the threshold is:

$$V_{th,H} = 15\left(\frac{R_8 \parallel R_9}{R_5 + R_8 \parallel R_9}\right) + 5\left(\frac{R_5 \parallel R_8}{R_9 + R_5 \parallel R_8}\right) \tag{5.74}$$

Table 5.6: Summary of component values used in the sample design of the shutdown board

Component	**Value**	**Component**	**Value**
R_1	$1\,k\Omega$	R_{10}	$3.6\,k\Omega$
R_2	$5.1\,k\Omega$	R_{11}	$3.6\,k\Omega$
R_3	$160\,\Omega$	R_{12}	$6.8\,k\Omega$
R_4	$100\,k\Omega$	R_{13}	$3.3\,k\Omega$
R_5	$24\,k\Omega$	C_1	$10\,\mu$F
R_6	$270\,\Omega$	C_2	$0.1\,\mu$F
R_7	$270\,\Omega$	C_3	$0.1\,\mu$F
R_8	$12\,k\Omega$	C_4	$10\,\mu$F
R_9	$20\,k\Omega$		

If we pick the resistor values of R_5, R_8 and R_9 to be $24\,k\Omega$, $12\,k\Omega$, and $20\,k\Omega$, then the thresholds are:

$$V_{th,L} \approx 3.57\,\text{V} \tag{5.75}$$

$$V_{th,H} \approx 5.24\,\text{V} \tag{5.76}$$

This corresponds to thresholds on V_{IN} of about 7 V and 10.4 V as needed. Thus, when the input voltage is rising up from a low value, the comparator output is high, and the threshold to leave the under-voltage mode is 10 V. When V_{IN} is falling from a high value, the comparator output is low, and the threshold is 7 V. Finally, D_2 is placed for the protection of M_9 and M_{10}.

Table 5.6 shows a summary of the component values used in this board. Refer to the appendix for a view of the full board.

Simulation Results

Figures 5-45 and 5-46 show the simulation results of the shutdown circuit. The results show the inverted shutdown signal versus the input voltage to the buck power stage. The cases when the voltage is rising or falling are simulated separately.

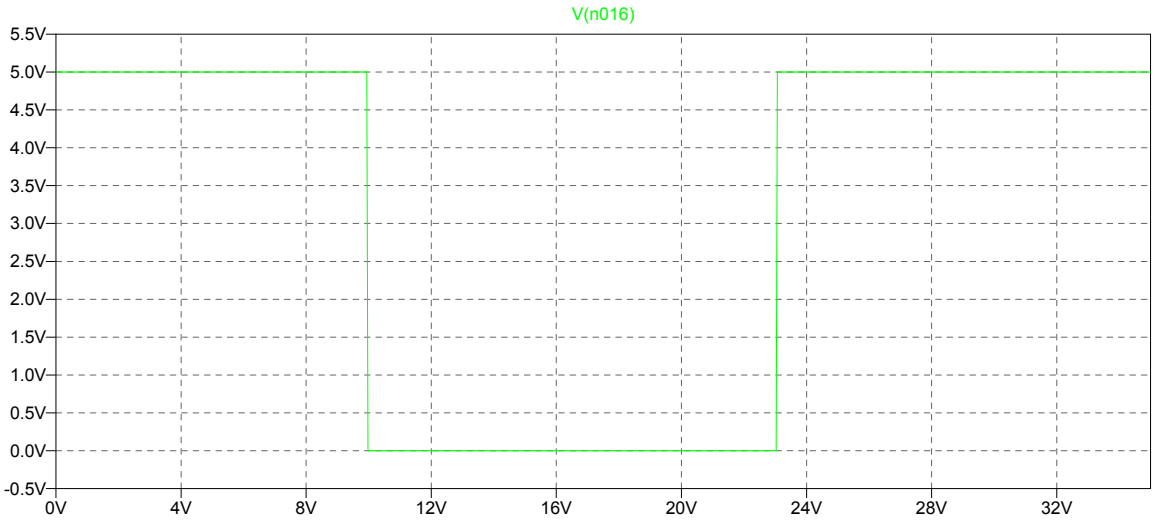


Figure 5-45: Simulation showing the inverted shutdown signal versus a sweep in the input voltage from low to high values.

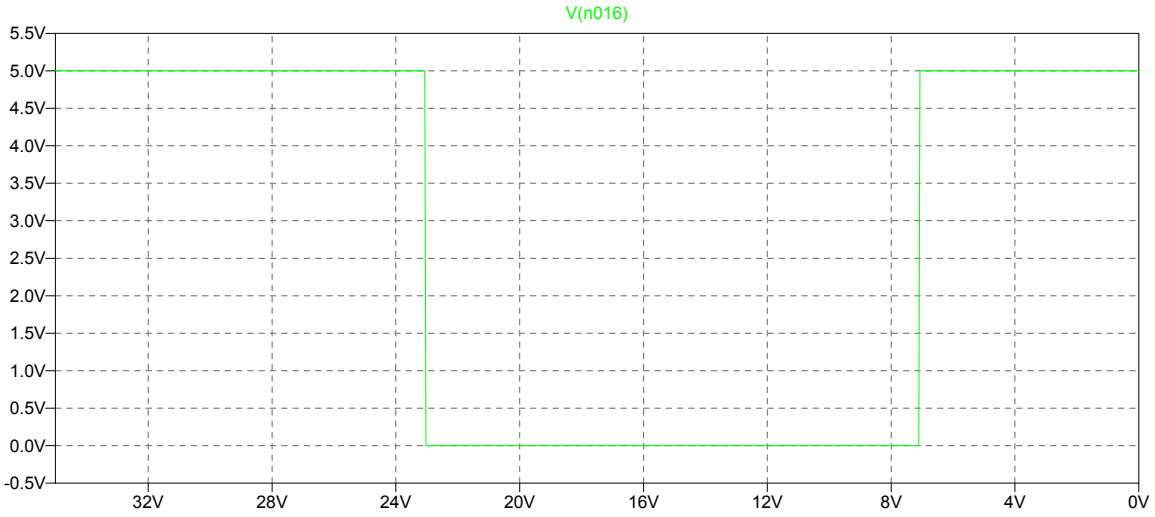


Figure 5-46: Simulation showing the inverted shutdown signal versus a sweep in the input voltage from high to low values.

Experimental Result

Figure 5-47 shows the experimental result of the shutdown circuit. The scope was set to "XY mode", and the result shows the thresholds as expected.

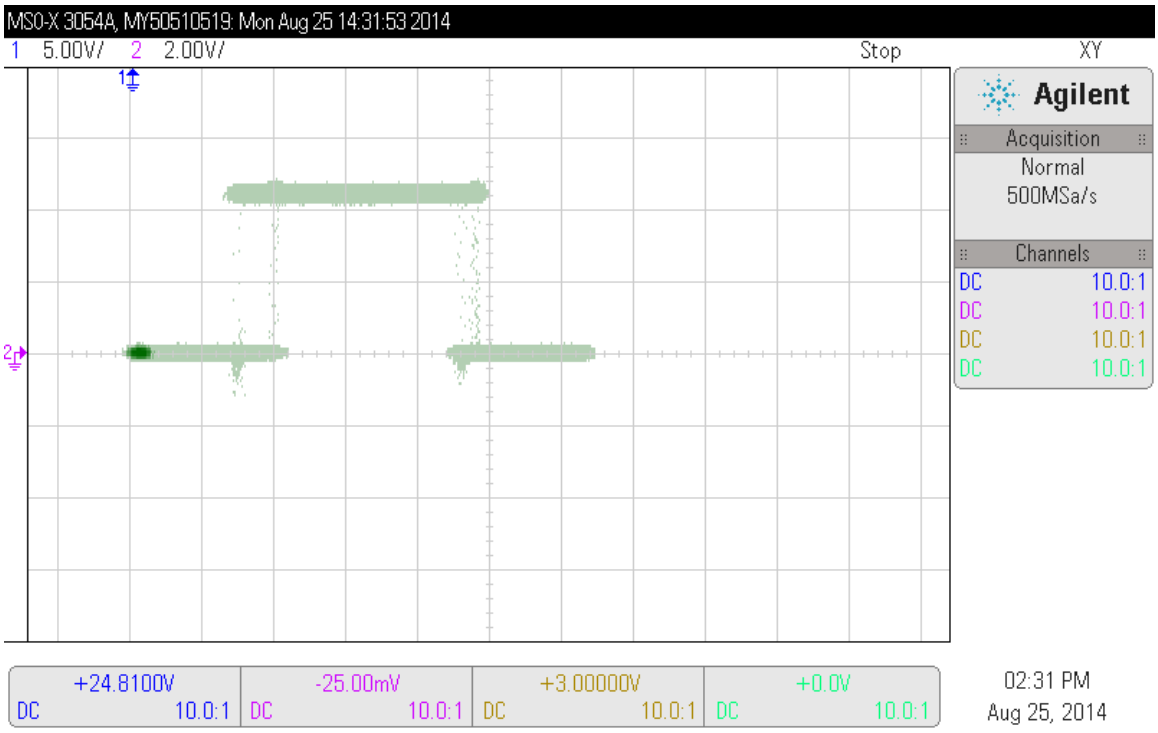


Figure 5-47: Experimental result showing the value of the shutdown signal for a sweep in the input voltage of the buck power stage.

5.2.7 Gate Drive

The gate drive board contains a number of circuits that are needed to properly switch the power MOSFETs on and off. The digital logic signals from the comparator and latch board do not carry enough current to handle the switching of the power MOSFETs. Therefore, the gate drivers provide the right voltage levels to turn both switches on and off at the right times. The timings should be accurately controlled to prevent the switches from turning on both at the same time, resulting in a shoot-through current. In addition, this board contains a safety feature that ensures that both power switches are off in case no PWM signal is applied to the board from the RS latch.

Circuits Description

- Low Side Gate Drive

Figure 5-48 shows the circuit schematic of the low side gate driver, which is used to

drive the low side switch of the buck power stage. This circuit operates from the 15 V supply rail. The structure of the first stage is a differential pair formed by Q_{15} and Q_{16}. Similar to the comparator circuit, this stage operate in large-signal mode, and thus the tail current source is fully switched to the right or left side. The current source is biased using the 5 V digital supply to produce a current of about 1.9 mA. The resistor values R_{31}, R_{32}, R_{38}, and R_{39} are thus chosen to be $1\,k\Omega$, $1\,k\Omega$, $270\,\Omega$, and $270\,\Omega$, respectively, since $I_{bias} = (5 - 0.6)/(R_{31} + R_{32} + R_{38})$ and $R_{38} = R_{39}$. A $0.1\,\mu$F capacitor C_9 is placed as a low pass filter to attenuate high frequency components in the 5 V supply.

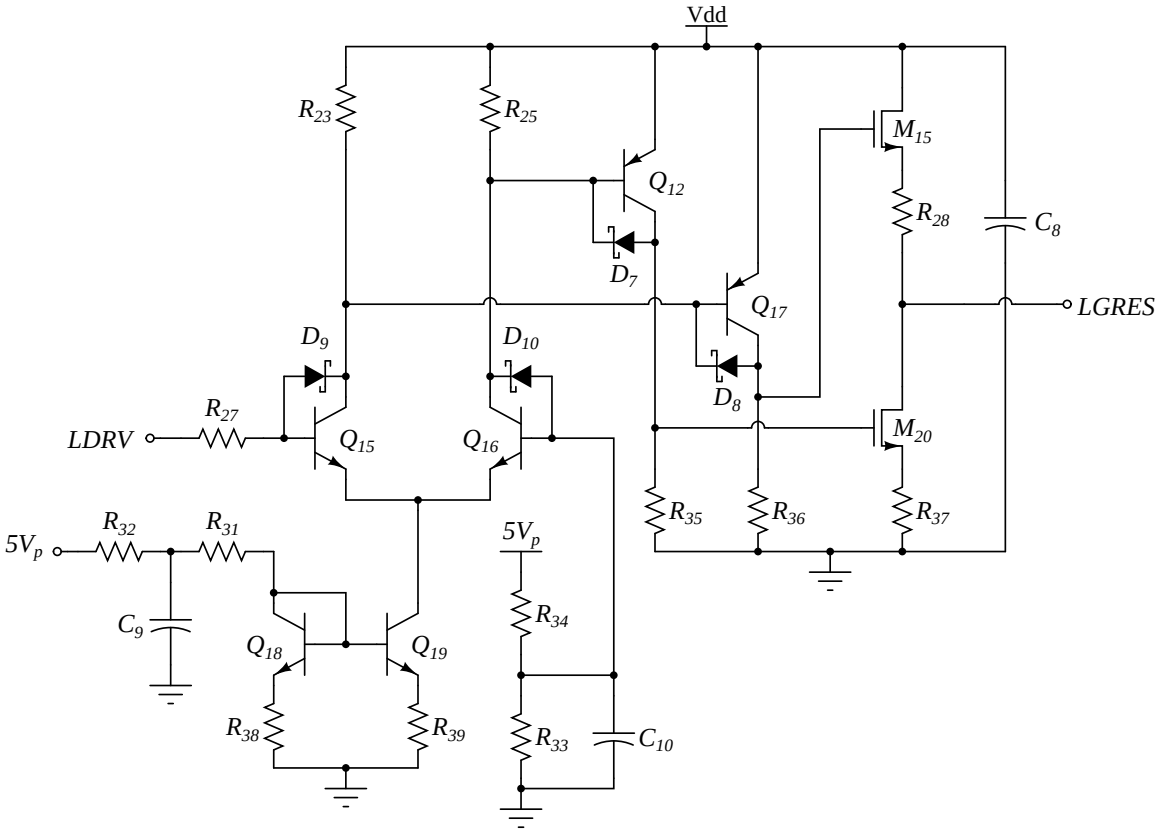


Figure 5-48: Circuit schematic of the low side gate drive.

D_7, D_8, D_9 and D_{10} are anti-saturation diodes. R_{33}, chosen to be $5.1\,k\Omega$, C_{10} ($0.1\,\mu$F) and R_{34} ($10\,k\Omega$) provide a fixed threshold of about 1.7 V at the gate of Q_{16}. Q_{12} and Q_{17} act as level shifts, and their collectors are connected to M_{20} and M_{15}, respectively. R_{28} and R_{37} are current-limiting resistors that prevent any over-currents

in the totem-pole output stage formed by M_{15} and M_{20}. When $LDRV$ is high, Q_{15} is on, which turns on Q_{17} and M_{15}, thereby pulling up $LGRES$ close to 15 V. When $LDRV$ is low, the opposite happens, and M_{20} turns on, pulling the output down to 0. R_{23} and R_{25} were chosen to be $510\,\Omega$, such that when the 1.9 mA bias current flows through each, the voltage across them fully turns on Q_{12} or Q_{17}. Finally, C_8 is a $1\,\mu$F bypass capacitor.

- High Side Gate Drive

The advantage of the low side driver is that the source of the power MOSFET is ground connected. We would like to have the same gate drive functionality to turn the high side switch on and off. However, the source of that switch is the drain of the low side switch, which is pulled to ground when the low switch is on, but is equal to the input voltage V_{IN} when the high side switch is on. Thus, the gate voltage must be equal to $(V_{IN} + 15)$ during this time. This is a classical issue with high side gate drive circuits, and there are several ways the level shift can be implemented. Figure 5-49 shows the high side drive circuit. The circuit is very similar to the low side drive, and has the same component values. However, the two notable differences are the additional diode D_2 and the $HSRC$ node. This node is the source of the high side switch, which is also the drain of the low side switch. When the low switch is on, D_2 is on, and the circuit is identical to the low side drive. The voltage across C_1 is equal to the 15 V supply. Now when the low switch turns off, and the $HDRV$ signal is high, $HSRC$ hold the full input voltage V_{IN}, and D_2 turns off. The right section of the circuit is thus supplied by C_1, known as the *bootstrap capacitor*, and $HGRES$ gets pulled up by M_3 close to a voltage of $(V_{IN} + 15)$, where 15 V is the voltage across the capacitor. This ensures that the gate-to-source voltage of the high side switch is close to 15 V. C_1 needs to be large enough to maintain its voltage with low ripple during the time the high switch is on. Note that in this case, the level shift is performed by Q_7 and Q_8 as they hold an additional voltage V_{IN} compared to what they would hold in the low side drive.

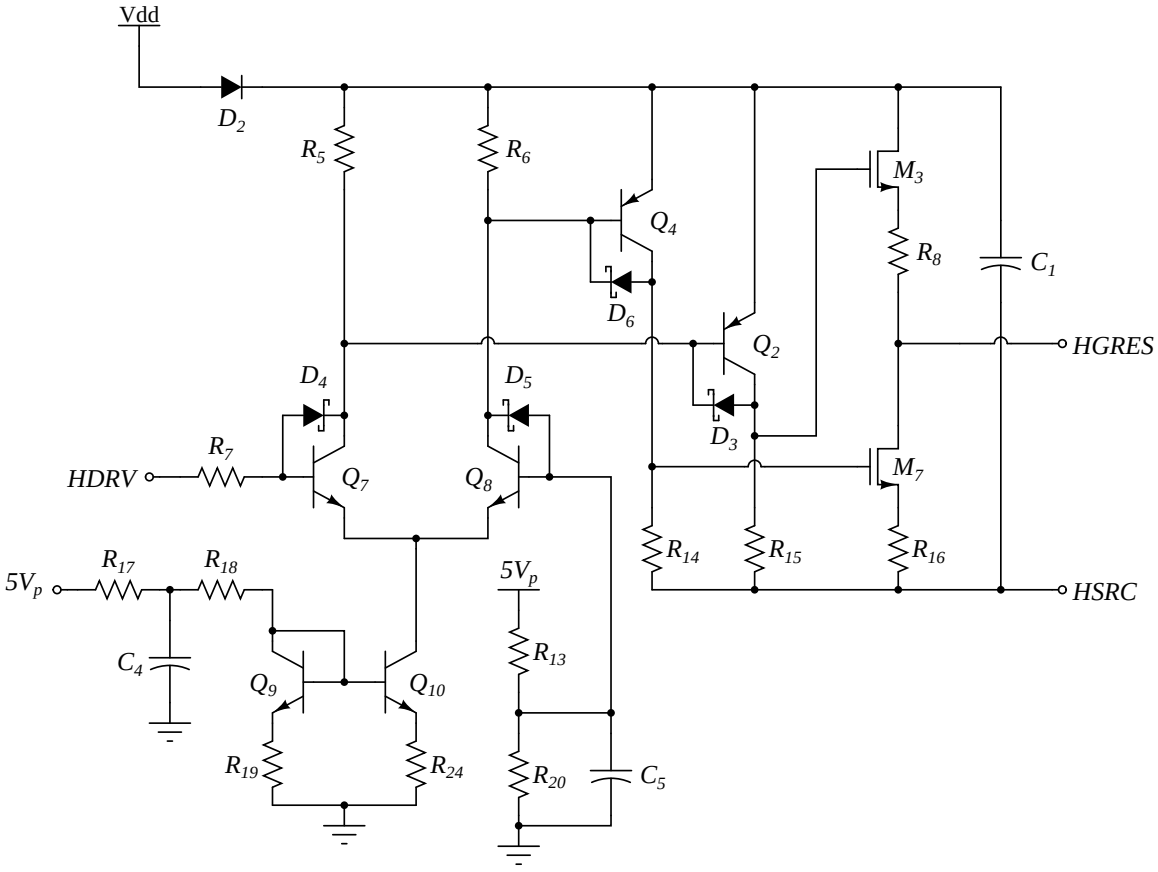


Figure 5-49: Circuit schematic of the high side gate drive.

The size of the bootstrap capacitor is determined by the following relation:

$$C_1 = C_{boot} \geq \frac{I_Q D_{max}}{f_{sw} \Delta V} + \frac{Q_g}{\Delta V}, \tag{5.77}$$

where D_{max} is the maximum duty ratio the converter operates in (ideally 1), f_{sw} is the switching frequency, Q_q is the gate charge of the power switch, ΔV is the allowable ripple, and I_Q is the quiescent current flowing through the gate drive. In this case, C_1 is chosen to be $1\,\mu$F.

- V_{GS} Sense Circuitry

The purpose of this circuit, shown in Figure 5-50, is to provide shoot-through protection. The base-emitter voltage of Q_5 measures the gate-to-source voltage of the low side switch. If V_{GS} is low, indicating that the low side switch if off, Q_5 turns off and

Q_6 turns on. This results in the output $HSEN$ being low. This enables that high side gate drive circuit. Similarly, Q_{11} measures the gate-to-source voltage of the high side switch. When the high side switch is off, Q_{11} turns off, thereby turning Q_{13} off and Q_{14} on, and pulling the inverted low side enable signal $LSEN$ low. R_3, R_4, R_{21}, and R_{22} are $10\,k\Omega$ pull-up resistors. R_{12} and R_{29} are $160\,\Omega$ base protection resistors. R_{26}, chosen to be $51\,k\Omega$ helps to limit the current drawn from the gate of the high side switch, and R_{30} is a $2.7\,k\Omega$ pull-down resistor.

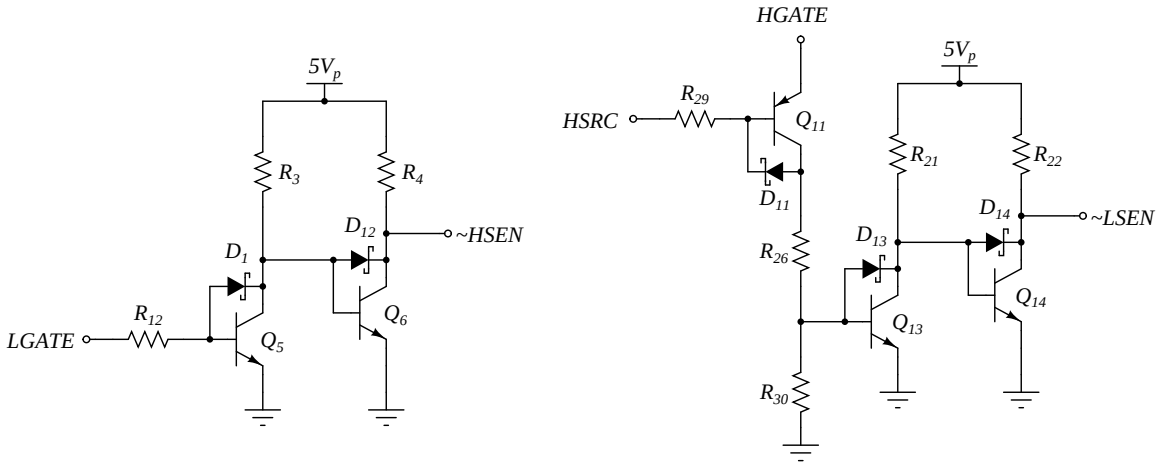


Figure 5-50: Shoot-through protection circuitry that provides the enable signal to the high side and low side gate drives.

- Gate Drive Logic

Figure 5-51 shows the basic digital logic required for the gate drive operation. The $PWM0$ signal is buffered through an inverter formed by M_4 and M_8 to create the signal PWM. This PWM output is the high side drive logic signal. M_5 and M_9 form an inverter to generate the PWM signal, used as the low side drive logic signal. Basically, the two logic structures shown on the right side of the circuit are 3-input NOR gates, and have the shutdown signal SD, the corresponding inverted enable signal, and the appropriate PWM signal as their inputs. If any of the inputs are high, the drive signal is pulled low.

- Safety Feature

Figure 5-52 shows an additional safety feature available in the gate drive board. In

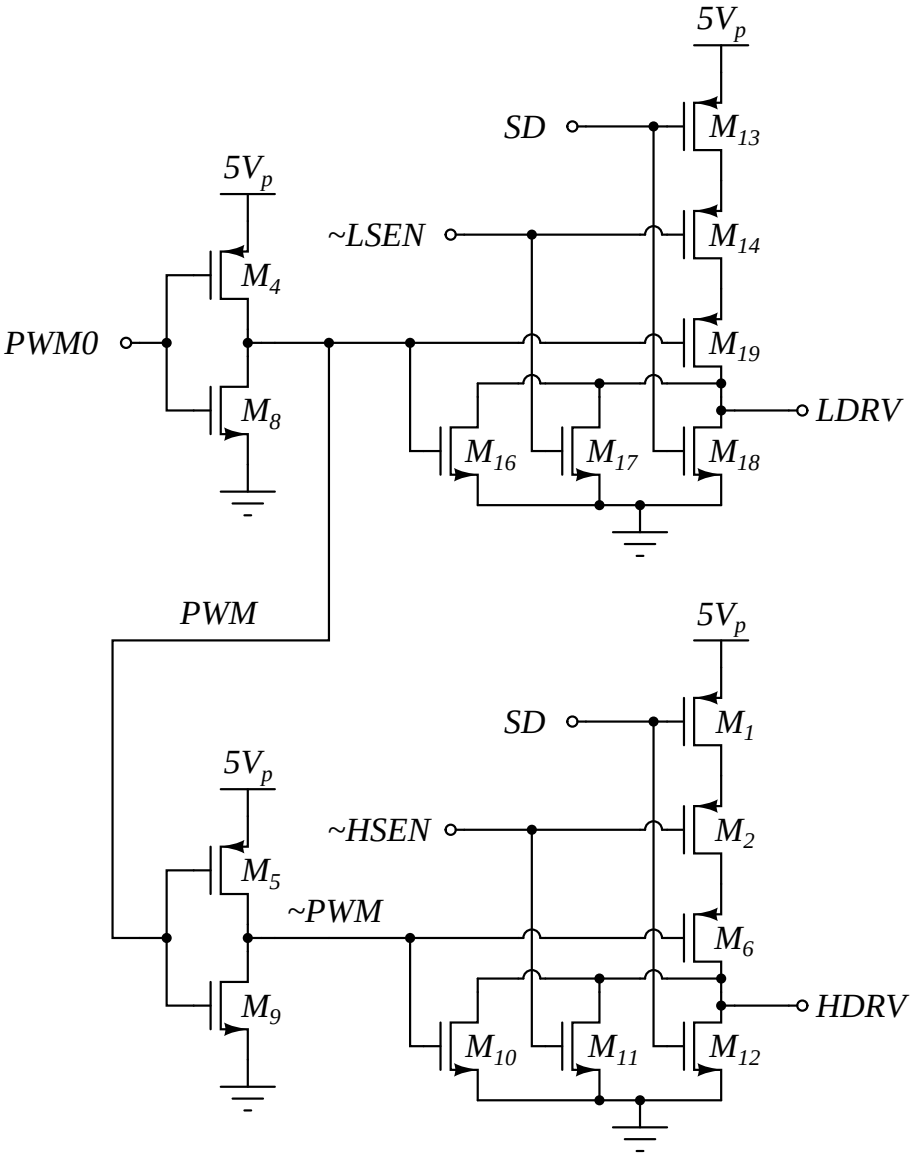


Figure 5-51: Digital logic for gate drive operation.

case the PWM0 signal is floating, R_1 and R_9 cause Q_1 to turn off, and Q_3 also turns off, resulting in a shutdown signal. This results in both drive signal being low. R_9 is a $1\,\mathrm{M}\Omega$ resistor (to limit the base current of Q_1), and R_{11} is a $160\,\Omega$ base protection resistor. R_1, R_2, and R_{10} are the usual $10\,k\Omega$ pull-up or pull-down resistors. Noting that Vdd is 15 V, we can see that when $PWM0$ is either 0 or 5 V, the SD signal is low and the operation is unaffected.

Table 5.7 shows a summary of all the values of the components used in this board.

Table 5.7: Summary of component values used in the sample design of the gate drive board

Component	**Value**	**Component**	**Value**
R_1	$10\,k\Omega$	R_{25}	$510\,\Omega$
R_2	$10\,k\Omega$	R_{26}	$51\,k\Omega$
R_3	$10\,k\Omega$	R_{27}	$160\,\Omega$
R_4	$10\,k\Omega$	R_{28}	$5\,\Omega$
R_5	$510\,\Omega$	R_{29}	$160\,\Omega$
R_6	$510\,\Omega$	R_{30}	$2.7\,k\Omega$
R_7	$160\,\Omega$	R_{31}	$1\,k\Omega$
R_8	$5\,\Omega$	R_{32}	$1\,k\Omega$
R_9	$1\,\mathrm{M}\Omega$	R_{33}	$5.1\,k\Omega$
R_{10}	$10\,k\Omega$	R_{34}	$10\,k\Omega$
R_{11}	$160\,\Omega$	R_{35}	$1\,k\Omega$
R_{12}	$160\,\Omega$	R_{36}	$1\,k\Omega$
R_{13}	$10\,k\Omega$	R_{37}	$5\,\Omega$
R_{14}	$1\,k\Omega$	R_{38}	$270\,\Omega$
R_{15}	$1\,k\Omega$	R_{39}	$270\,\Omega$
R_{16}	$5\,\Omega$	C_1	$1\,\mu\mathrm{F}$
R_{17}	$1\,k\Omega$	C_2	$10\,\mu\mathrm{F}$
R_{18}	$1\,k\Omega$	C_3	$0.1\,\mu\mathrm{F}$
R_{19}	$270\,\Omega$	C_4	$0.1\,\mu\mathrm{F}$
R_{20}	$5.1\,k\Omega$	C_5	$0.1\,\mu\mathrm{F}$
R_{21}	$10\,k\Omega$	C_6	$0.1\,\mu\mathrm{F}$
R_{22}	$10\,k\Omega$	C_7	$10\,\mu\mathrm{F}$
R_{23}	$510\,\Omega$	C_8	$1\,\mu\mathrm{F}$
R_{24}	$270\,\Omega$	C_9	$0.1\,\mu\mathrm{F}$
C_{10}	$0.1\,\mu\mathrm{F}$		

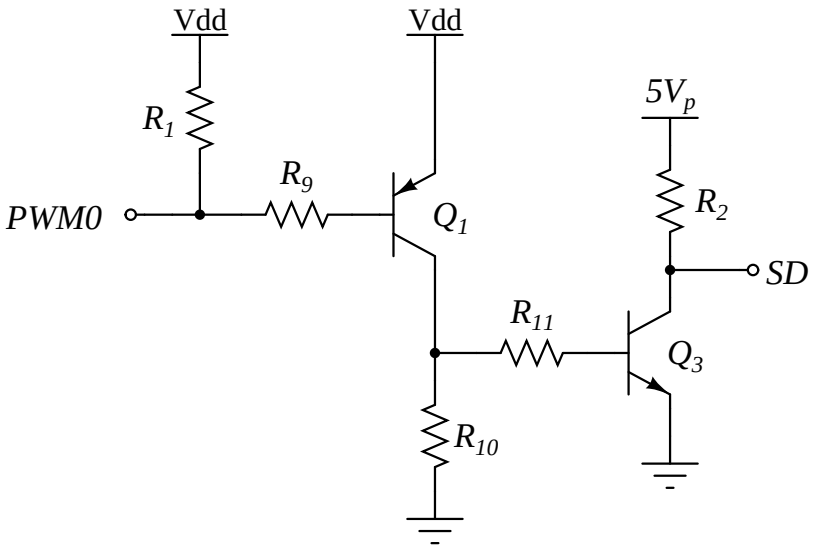


Figure 5-52: Circuit that provides a safety lockout feature in case there is no PWM signal.

Simulation Result

Figure 5-53 shows the result of simulating the gate drive circuits. The results show correct drive signals at both the high and low side switches as expected.

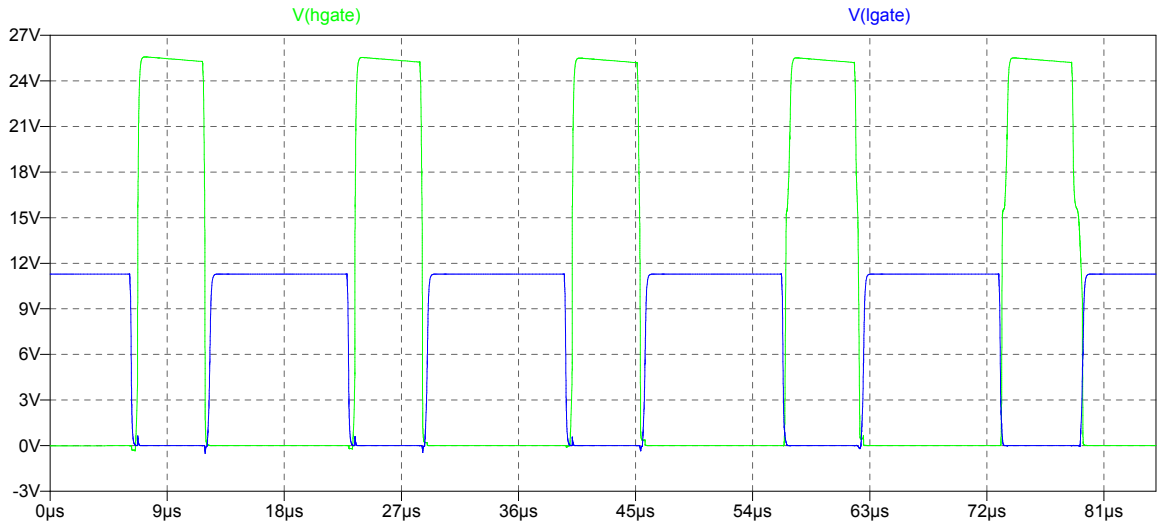


Figure 5-53: Simulation result showing the high and low side gate drive signals.

Experimental Result

The experimental result of the gate drive circuits when the converter is operating in closed loop configuration is shown in Figure 5-54.

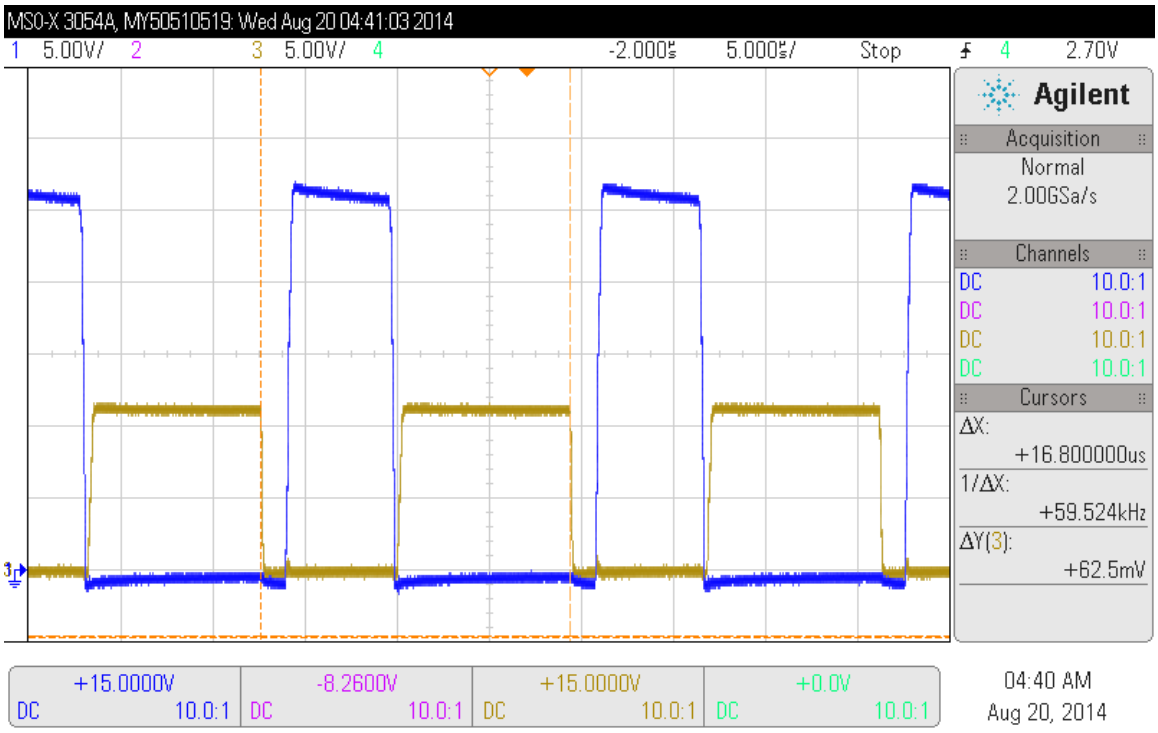


Figure 5-54: Experimental result showing the gate drive signals when the converter operates in closed loop configuration.

5.2.8 Buck Power Stage

The buck power stage consists of the main power circuit that has the high and low side power switches. The buck power circuit is shown in Figure 5-55. M_1 and M_2 are the high side and low side switches, respectively. R_1 is a $0.33\,\Omega$ sense resistor used by the current sense amplifier circuit. R_2 and R_8 are $10\,\Omega$ gate resistors, used to protect the gates of the power MOSFETs from any possible ringing. R_4 and R_7 are $10\,k\Omega$ pull-down resistors, used to keep the gate-to-source voltages at zero whenever they are floating. R_6 is a $15\,\Omega$ power resistor and is the load of the circuit. R_3 and R_5 are optional resistors, and are not used in out design example. The combination of L_1, C_4, and C_5 form the output filter of the buck converter. Given a current

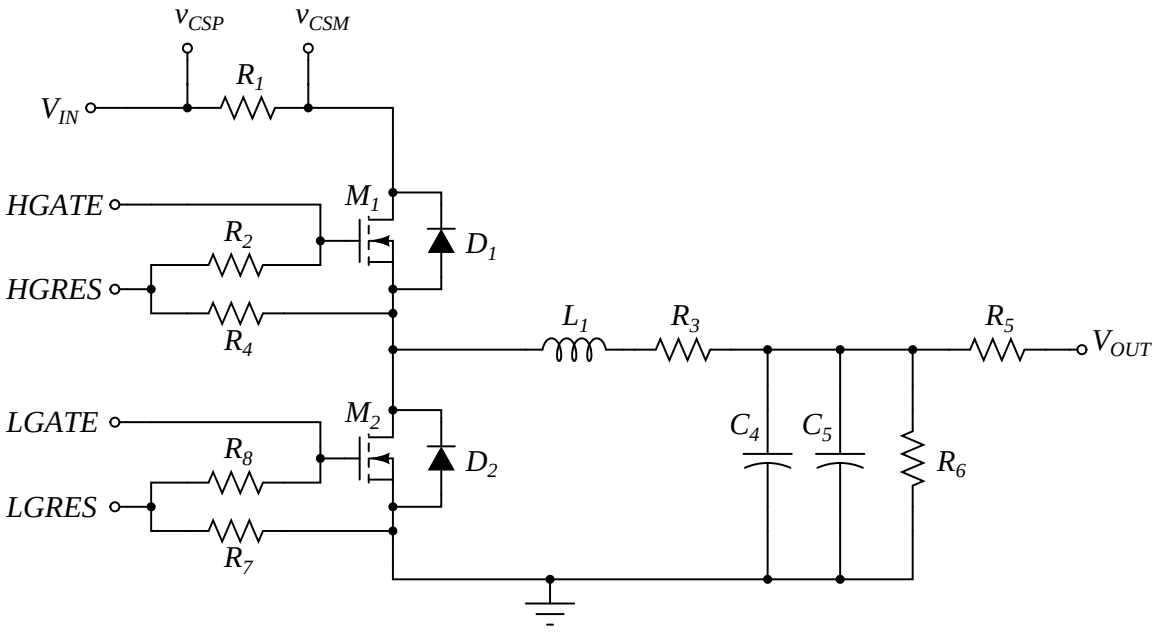


Figure 5-55: Buck power stage circuit.

ripple specification Δi_L, we design the inductor such that the resulting ripple current doesn't exceed the specification. Thus, we have:

$$L_1 \geq \frac{(V_{IN} - V_{OUT})DT}{\Delta i_L} \tag{5.78}$$

Similarly, given a capacitor voltage ripple specification Δv_C, we design the output capacitance to be:

$$C \geq \frac{\Delta i_L T}{8\Delta v_C}, \tag{5.79}$$

where C in our case is $C_4 + C_5$.

Figure 5-56 shows the inductor voltage plotted over time. The converter's high side switch is on for a portion DT of the switching period, where D is the duty ratio. Since the average inductor voltage is zero, the areas have to be equal:

$$(V_{IN} - V_{OUT})\, DT = V_{OUT}\,(1 - D)\, T \tag{5.80}$$

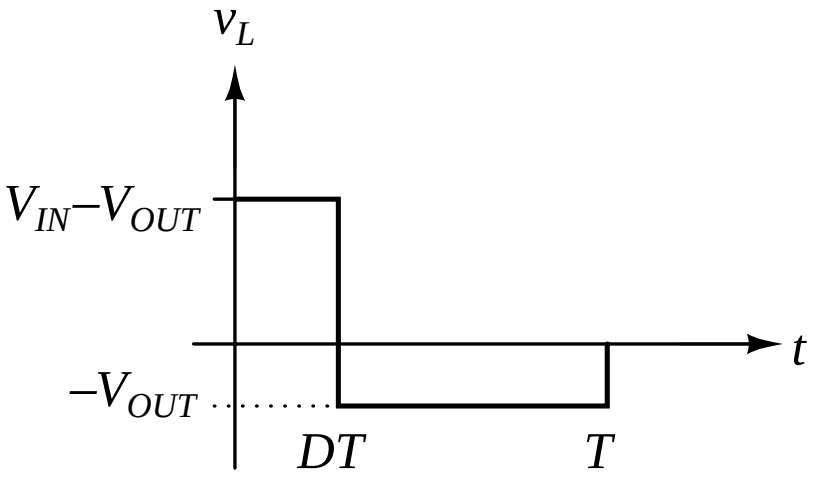


Figure 5-56: A plot of the inductor voltage v_L with time.

Table 5.8: Summary of component values used in the sample design of the buck power circuit board

Component	**Value**	**Component**	**Value**
R_1	$0.33\,\Omega$	R_8	$10\,\Omega$
R_2	$10\,\Omega$	C_1	$220\,\mu$F
R_3	$0\,\Omega$	C_2	$10\,\mu$F
R_4	$10\,k\Omega$	C_3	$0.1\,\mu$F
R_5	$0\,\Omega$	C_4	$33\,\mu$F
R_6	$15\,\Omega$	C_5	$0.1\,\mu$F
R_7	$10\,k\Omega$	L_1	$330\,\mu$H

Solving for V_{OUT} yields:

$$V_{OUT} = DV_{IN} \tag{5.81}$$

We designed the converter to run at around 60 kHz from a 15 V supply, with a duty ratio of 1/3, to give a steady output voltage of 5 V. Table 5.8 shows the values of the components used.

Simulation Result

Figures 5-57 and 5-58 show the simulation results of the converter circuit block.

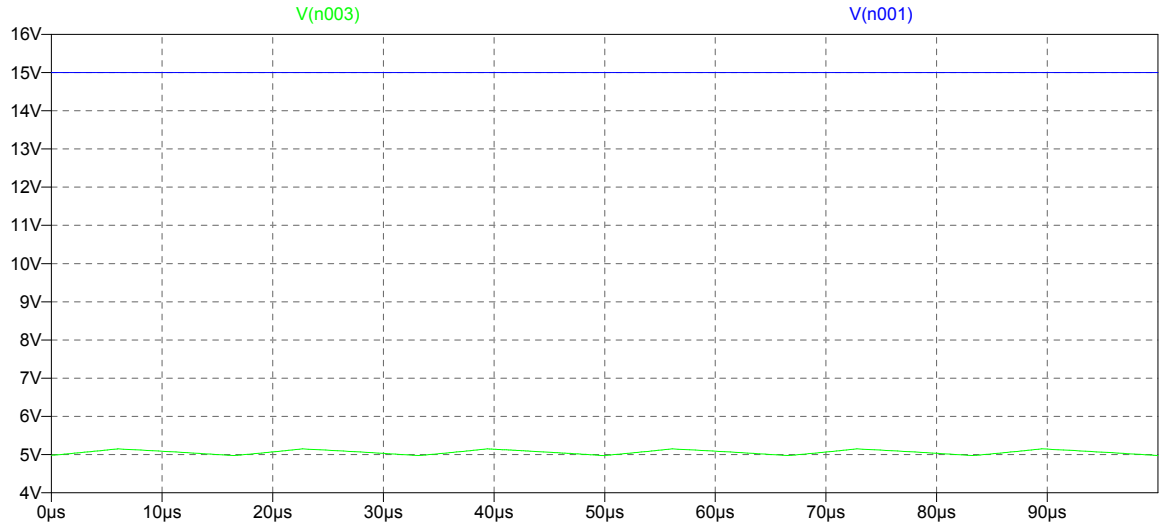


Figure 5-57: Simulation showing the steady-state output voltage of the converter.

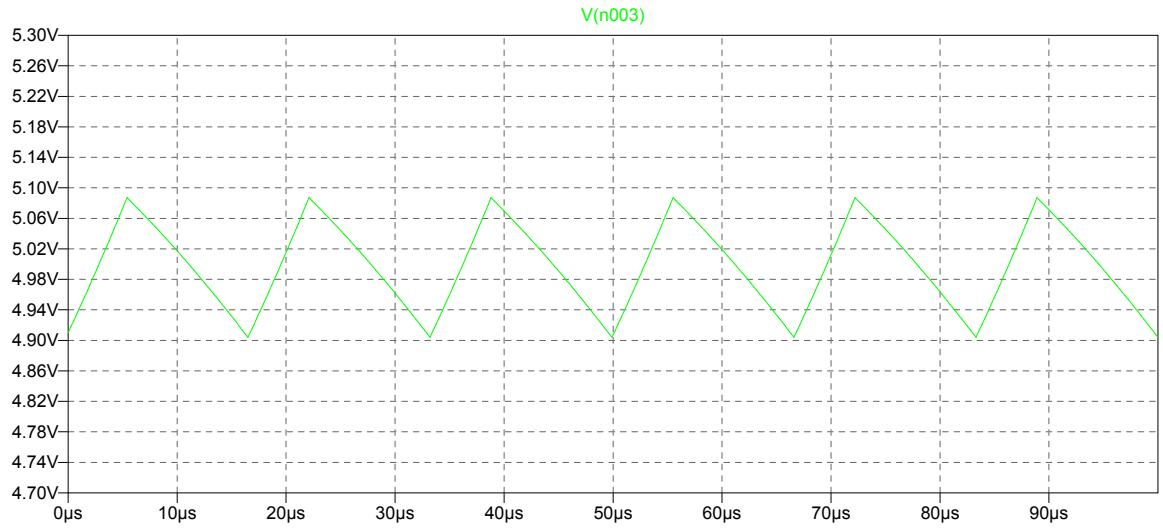


Figure 5-58: Simulation showing the output voltage ripple.

Experimental Results

Figures 5-59 and 5-60 show the experimental results from the buck power stage circuit.

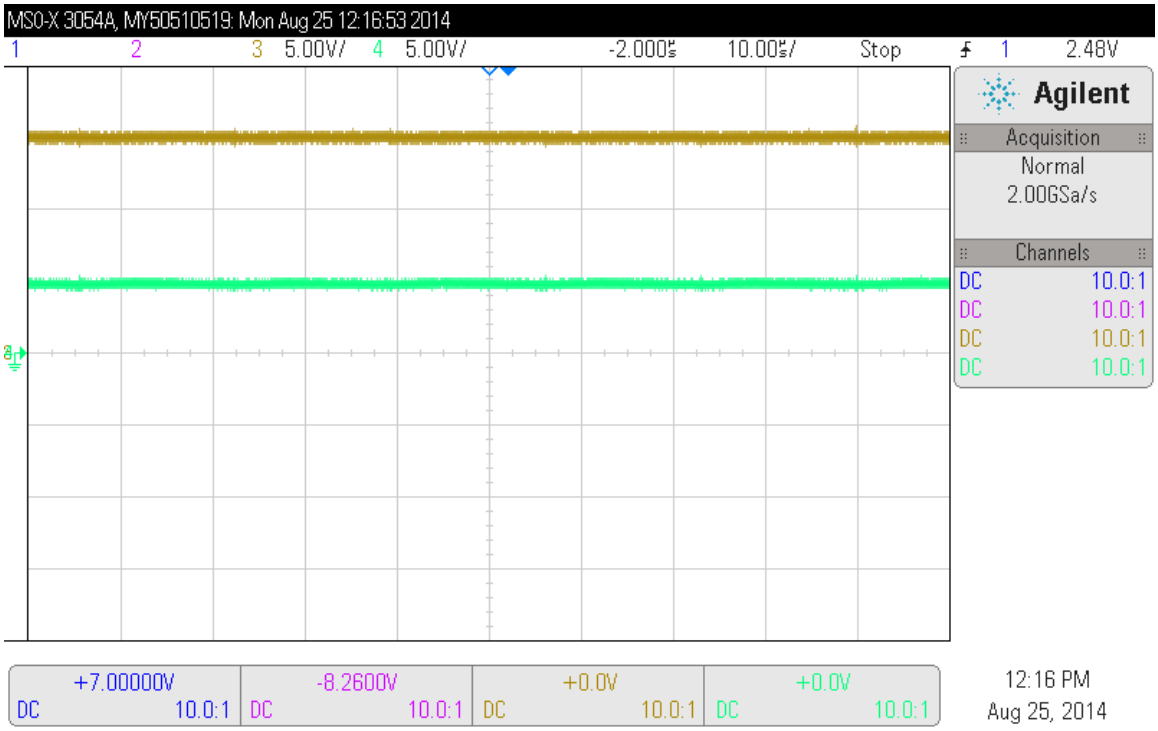


Figure 5-59: Experimental result showing steady-state operation of the buck power stage. The output is a constant 5 V.

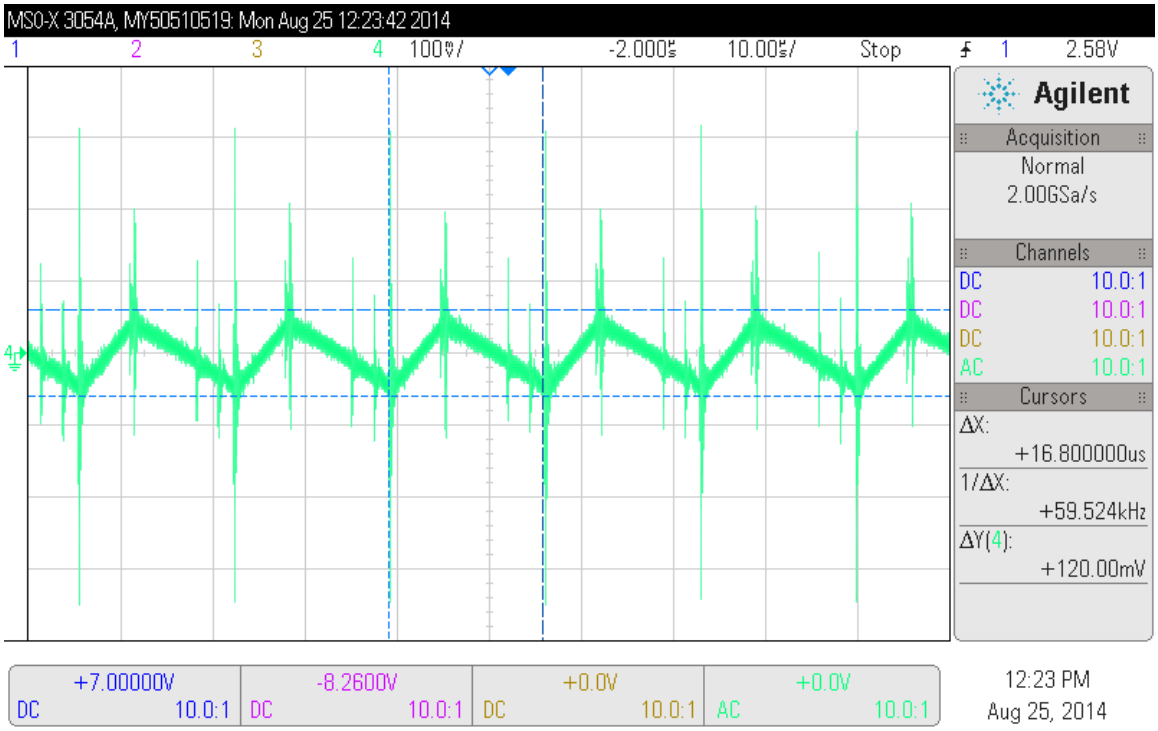


Figure 5-60: Experimental result showing ac ripple magnitude on the output voltage of the buck power stage.

Chapter 6

Teaching Modeling, Control, and Simulation through the Platform

This chapter is based on the work in [27], where we introduce an educational kit to teach modeling, control, and simulation through power electronics. This hands-on kit consists of a power converter and controller, and is built using discrete electronic devices. Our proposed strategy in this work is to use the kit to help guide students in system modeling by dividing the process into different levels of model abstraction: system-level, control-level, behavioral-level, and device-level. This strategy is illustrated through design examples utilizing circuit blocks from the kit.

6.1 Introduction

System modeling and design is fundamental in engineering, especially power electronics. We have developed an educational kit that serves as an experimental platform to help teach modeling, control, and simulation in power electronics within a robust system design strategy. Much of today's engineering education focuses on ensuring that students understand numerous technical concepts, and perhaps apply these concepts in course projects or laboratories to build systems that perform some function. However, little or no attention is generally given to the iterations the students perform in the system design process. As a result, many new engineering graduates enter

industry lacking a proper system design methodology. For example, it is common for electrical engineering undergraduates to learn about basic circuit design techniques and topologies, and implement some circuits with discrete components. However, the fact that a proper modeling and system design approach is often not emphasized as a teaching objective leads students to various undesirable engineering practices, such as repeatedly "tweaking" component values and iterating on simulations, attempting to simulate the entire system all at once, which in large projects is intractable. This work's approach to modeling and design in the context of a teaching kit aims to promote better system design.

Along with teaching modeling and simulation, the educational kit, which is inspired by the UC3842 power electronic controller shown in Figure 6-1, provides an invaluable hands-on experience. The actual building within the platform and the modularity of the circuit blocks gives significant insight on interconnections, board parasitics, current flow, grounding and layout, device variations and nonidealities, among others. These aspects will not be elaborated further in this work, as the focus will be on the proper incorporation of modeling and simulation in the design of large complicated systems.

It is without a doubt that simulation has taken a major role in modern system design not only in circuit design and power electronics, but also in most, if not all, other engineering disciplines. The advancements in computing power have made computer simulation a very powerful tool; its speed and ease can make it a pedagogical crutch to learning, and of great value to industry [4]. At the same time, systems continue to grow in complexity, and especially at the forefront of technology, system complexity tends to outpace the power of simulation. Moreover, simulations are based on mathematical models of different physical processes, which themselves contain many assumptions and limitations. Students should therefore keep in mind that simulation by itself is not enough, and can arguably waste significant time if it is not incorporated within a proper system design methodology.

It is crucial that instructors help students understand the role of simulation in the design process by keeping it as a teaching goal. Students should know, for in-

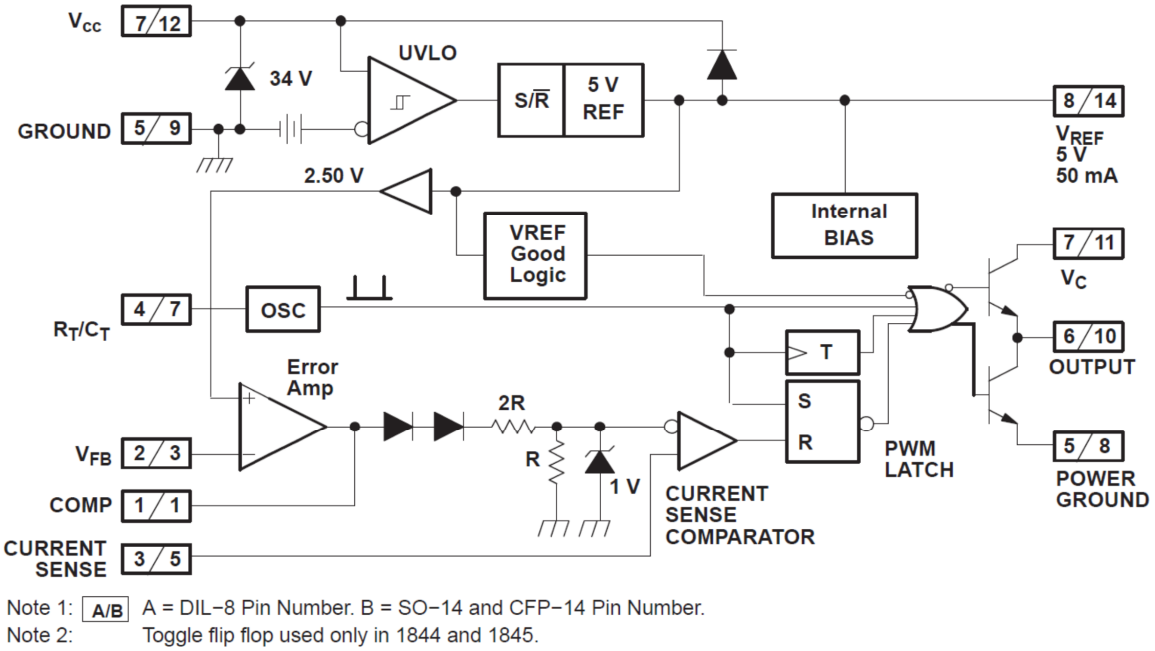


Figure 6-1: The venerable Unitrode UC3842 provides the inspiration. The UC3842 has been used as a controller building block for many classically controlled power converters [4, 5].

stance, that hand calculations serve as a first order model of the system, whether this is achieved by performing linearizations about fixed operating points through small-signal analysis, or by idealized functions, such as in translinear circuits. Computer simulations provide extra levels of model complexity, depending on the device models used, which leads to the inherent tradeoff between simulation time and model accuracy. With that in mind, students would be mindful that running the whole controller as in Figure 6-1, for example, through a time-domain transient simulation is not wise. Simulation, with all its power in computation and algorithms, requires a degree of sophistication in system-level thinking and problem partitioning.

The strategy that we propose in this work is to use the kit to help guide the students in system design, modeling, and simulation by dividing the process into different levels of model abstraction: system-level, control-level, behavioral-level, and device-level. The final objective of the syllabus is to have a fully functional power electronic controller that is built using only discrete electronic devices: transistors, capacitors, and resistors. Without a proper design process, this is unattainable be-

cause of a naive preoccupation of a simultaneity of design details. With the proposed design strategy, students analyze the power electronic controller kit at each model level and identify the parts of interest and their functionality at that model level. This emphasizes the need for a *top-down* approach when defining and organizing the whole system and its requirements, as well as a *bottom-up* approach when analyzing technological capabilities (i.e. what is possible) and specific functionality.

The use of hands-on kits and platforms on which educational experiments are conducted has been continually evolving over the recent years [28, 29, 30, 31, 32, 33]. Examples vary from a buck converter to drive an electric motor of a solar model car [30], to a reconfigurable educational platform for fast experimentation with different power converter topologies [29], to an educational system for controlling power electronics systems with digital signal controllers (DSCs) [34], among others. Hands-on projects reinforce the concepts given in lecture, and provide more insight on various design issues that may not be obvious in theory. There is generally a great demand in the industry for the skills acquired from these educational platforms [28, 30].

The fact that power electronics is a multidisciplinary field makes the power electronic controller kit a platform for teaching not only classical concepts in power electronics, but also integrated circuit (IC) design [4], as well as classical control theory.

This chapter is divided into five sections. Section 2 provides a description of the kit and the circuit blocks. Section 3 lays out the proposed system design methodology, and section 4 provides three design examples on how this methodology can be educational. A conclusion is given in section 5.

6.2 Kit Description

It can be seen from Figure 6-1 that the UC3842 current-mode controller consists of several subcircuits that perform different functions. These different functions, along with additional ones, were realized in different circuit boards in the kit, each carrying

out a specific function. Figure 6-2 shows an overall view of the power controller kit. A wooden case houses the motherboard on which the controller blocks are mounted. The motherboard has female pin connectors to which the circuit blocks plug. Pin sockets are used for all components not only to minimize soldering, but also to provide design flexibility and ease in replacing components. Figure 6-3 shows a sketch of the different circuit blocks in the kit.

Figure 6-2: An overall view of the power electronic controller kit. The wooden box houses the motherboard, on which the various controller circuit blocks are mounted. The box also has a place for storing the kit components (courtesy of Mark Avestruz, 2012).

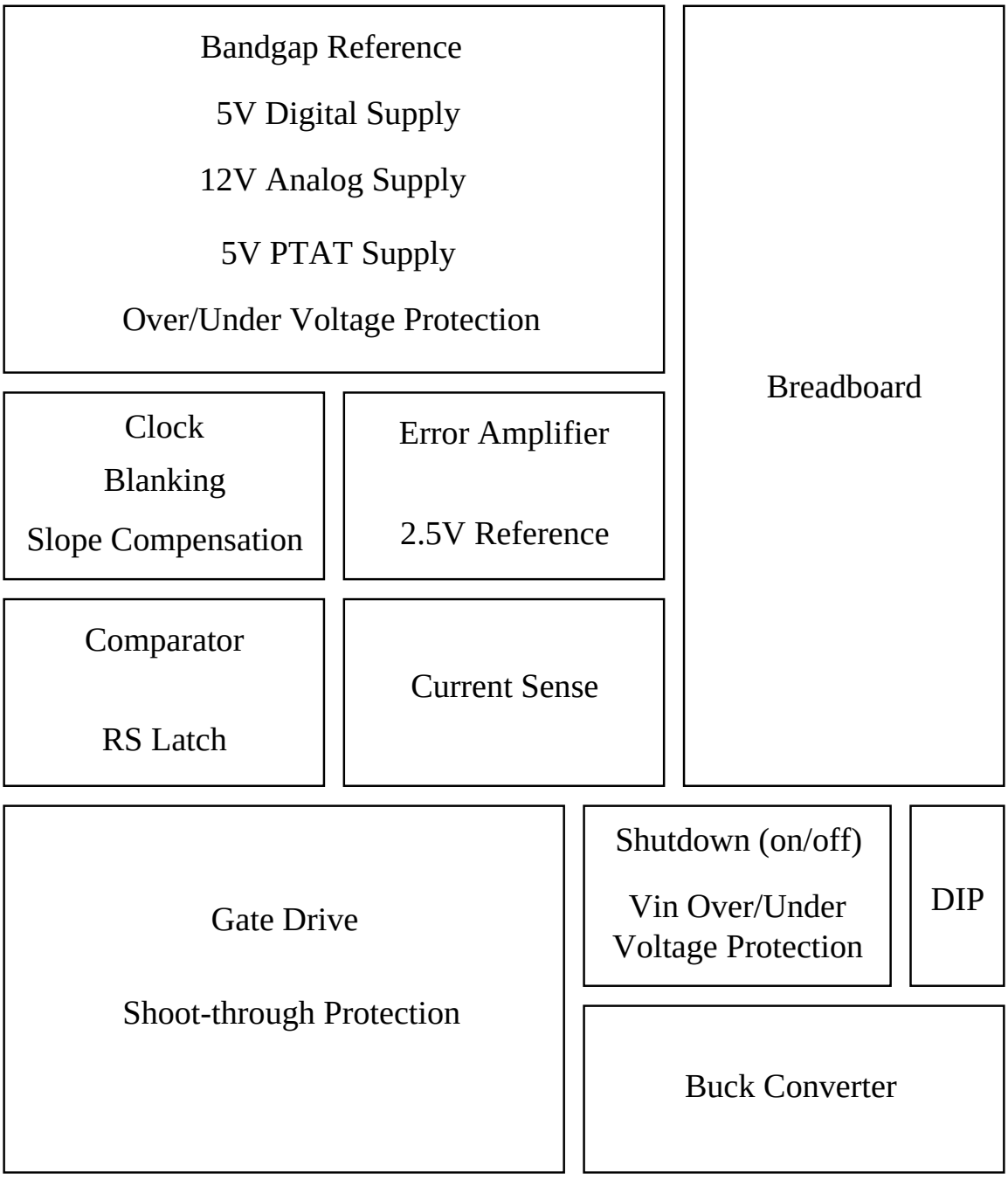


Figure 6-3: Power electronic controller modules [4]. This clearly shows how the controller functionality is organized into different circuit blocks, each performing a specific function. The modularity in the kit design is clearly noticed.

The modularity in the kit design is easily noticed. Each module can be isolated and tested independently. Individual modules can be easily replaced if they are damaged, or if the board is updated. In addition, the fact that pin sockets are used for component placement makes the modules reusable, thereby significantly reducing the operating costs in the long run. All the designs are created using common discrete electronic devices, which are readily available and inexpensive. These include the well-known and characterized 2N3904 and 2N3906 NPN and PNP bipolar junction transistors (BJTs), respectively, and 2N7000 N-MOSFETs, among others. This gives substantial insight on deeper transistor-level circuit operation, making the kit a great tool for teaching IC design [4]. Test points to which instrumentation and oscilloscope probes may be clipped are available on most of the nodes, thus providing access to and insight on almost every part of the controller circuit. The grounds and other connections of the different modules are also fully configurable, allowing many possibilities for testing. Furthermore, the kit contains a breadboard for optional external circuitry to interface with the controller circuit blocks.

The controller is used to operate a buck converter, as shown in Figure 6-3, and consists of the following modules:

- ***Bandgap and voltage references***: this block provides the different voltage levels necessary for the operation of the other controller circuit blocks. It provides a 5V supply for the digital blocks, a 12V supply for the analog blocks, and a 5V proportional to absolute temperature (PTAT) supply to generate PTAT current sources in other circuit blocks.

- ***Clock, leading-edge blanking, and slope compensation***: this block generates the clock pulses necessary for commanding the gate drive circuit and for setting the switching frequency of the power converter switches. It also provides leading-edge blanking to prevent false turn off of the high-side switch of the converter due to an initial current impulse [5], and generates the ramp voltage needed for slope compensation, which is crucial in current-mode control with duty cycles over 50% [26].

- ***Current sense amplifier***: this block provides a measure of the high-side switch current by amplifying the voltage across a sense resistor. Thus, it also provides the controller with a measure of the instantaneous inductor current while the high-side switch is on.

- ***Error amplifier***: this block implements the controller transfer function, and dictates the maximum inductor current value allowed before the high-side switch turns off, i.e. it provides inductor current command to the power stage. For example, this module can implement a proportional-integral (PI) controller, or perhaps some other controller, depending on the compensation network configuration used.

- ***Comparator and RS latch***: this block is responsible for deciding which state the converter must be in, i.e. whether the high-side or low-side switch should be on. The comparator toggles as soon as the measured inductor current reaches the maximum current dictated by the controller, thus turning the high-side switch off. The RS latch holds the state of the converter until the next clock pulse, at which the converter state changes back, turning the high-side switch back on.

- ***Gate drive circuitry***: this block receives the current state of the converter from the comparator and latch board, and provides the gate voltages required to turn the power switches on or off. The block also includes shoot-through protection circuitry to prevent the two switches from turning on at the same time. Moreover, the gate drive board checks whether the shutdown signal is asserted by the shutdown board, in which case the gate driver turns off both power switches.

- ***Shutdown and protection circuitry***: this block ensures that the input of the power converter is within the allowable limits. If the input voltage is too low or high, the shutdown signal is asserted, and the gate drive turns off both power switches. The shutdown board also includes the option of asserting the

shutdown signal through a mechanical switch.

- ***Buck converter***: this block contains the power stage with the power switches and filtering needed to meet given output current and voltage ripple specifications. This block is where signals such as the inductor current and output voltage are fetched from.

Although the focus of this work is on teaching modeling, control, and simulation through the power controller kit, it is important to highlight the importance of the hands-on aspect of the kit. The learning outcomes acquired from applying theoretical concepts in power electronics and control theory to actual circuits, and experiencing the system design process starting with back-of-the-envelope calculations and ending in a fully functioning system cannot be paralleled by those that result from most other teaching methods. The whole process engraves various skills in the hands and minds of the students, which otherwise would not have been possible without the hands-on aspect. It develops intuition and a feel of why and how different parts of the system behave the way they do, and this proves to be invaluable in the engineering industry. This is one of the main reasons why teaching engineering system design methodology within the context of power electronic control can be of great benefit.

6.3 Model Abstraction Levels

The system modeling strategy that we propose is to divide the process into different levels of model abstraction: system-level, control-level, behavioral-level, and device-level. This essentially structures the way students think about and analyze the given system. If properly applied, these model abstraction levels should prevent students from "getting stuck" in dealing with details of the design that are impertinent at the early stages of the system design process.

6.3.1 System-Level Model

The first level of model abstraction that students should understand is the system-level model. At this point, students have a high-level overview of the whole system. Students at this model level are encouraged to ask themselves fundamental questions such as, "What does the system consist of?" Or, "What does this system do?"

When the kit is presented at the system-level, students identify the buck power stage and the controller as the two subsystems that comprise the entire system. At this point, students should understand the basic functionality of each system, and how its role fits in the operation of the entire system.

For the power stage subsystem, students can be exposed to the topology of the converter. In addition, depending on the requirements, students can set their own specifications or understand the specifications provided to them. For example, the kit's buck converter is supposed to work with a 10-20V input voltage, and must deliver a steady output voltage of 5V. Students are free to set reasonable requirements for the output current and voltage ripples, as well as the switching frequency of the converter switches. However, it is important to note that at this stage, students should not be concerned about *how* these specifications are met, or any further implementation details. The emphasis in the system-level model is on understanding the fundamentals of the system, identifying its main subsystems, and understanding its specifications and main functionality.

As for the controller subsystem, students can observe that it is a peak current-mode controller, and should understand that it controls the generation of pulse width modulation (PWM) signals, thereby controlling how often the converter switches turn on and off. Students can use this as an opportunity to think about the options available for controlling the converter, i.e. current-mode or voltage-mode control, but without yet being concerned about the peculiarities of the dynamics.

It is important to also understand how the roles of the individual subsystems are related to each other and how they all fit into the operation of the whole converter. The controller subsystem cannot function properly without obtaining information

on inductor current, output voltage, and switch turn on/off timings from the power stage. Similarly, the power stage will not deliver power to the output without the PWM signals and the gate driver in the controller subsystem. This is an example of why a combination of a *top-down* and a *bottom-up* approach to system design is necessary. Figure 6-4 illustrates the system-level model.

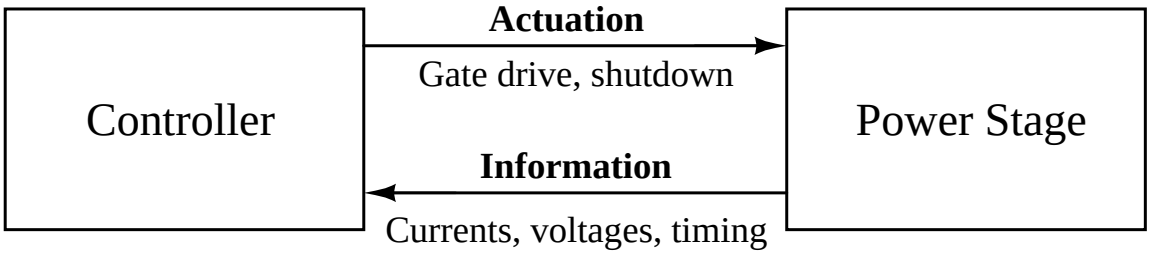


Figure 6-4: System-level description of the power controller kit. The subsystems are identified, and the information flow between them is understood.

6.3.2 Control-Level Model

After gaining understanding of what the system is and what it should do, students move on to the next model level, namely the control-level. At this level, students analyze each subsystem identified in the system-level model from a controls perspective. This is done by identifying the subsystem's main constituents (plant and controllers) and their interconnections in the form of block diagrams, each having inputs, a transfer function, and outputs [35]. Students identify the control structure and the relevant state variables. This could be an opportunity for students to not only learn about averaged power converter models and their transfer functions, but also explore differences in the dynamics of voltage-mode control (v.m.c.) and current-mode control (c.m.c.) [26, 36].

For example, students should be able to identify the kit's buck power stage as the plant to be controlled, and must understand the difference in the relevant states in

v.m.c. and c.m.c., and the effect this has on the buck power stage transfer function:

$$P(s) = \begin{cases} v_o(s)/i'_L(s) & \text{in c.m.c.} \\ v_o(s)/d(s) & \text{in v.m.c.} \end{cases}$$

Students see at this point how current-mode control simplifies the buck transfer function to first-order, as opposed to second-order in the case of v.m.c. Students should be to come up with a control-level model similar to the one shown in Figure 6-5.

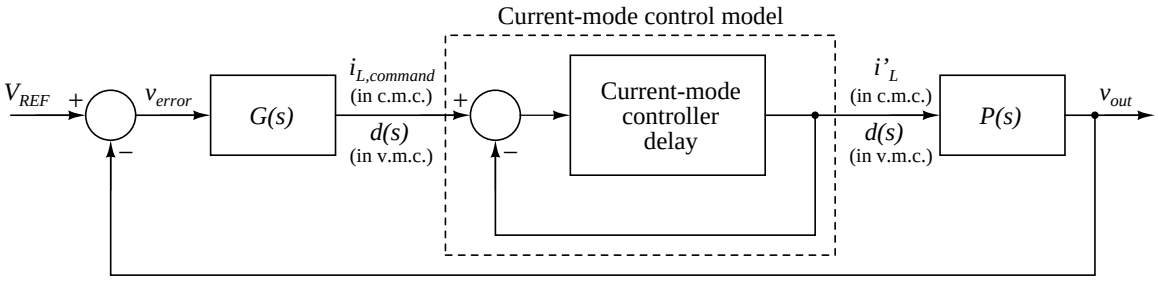


Figure 6-5: Control-level model of the power controller kit. $G(s)$ corresponds to the controller which commands the maximum inductor current in c.m.c. or duty ratio in v.m.c.

After identifying the plant and controller blocks, as well as the relevant state variables, and after deriving the relevant transfer functions, students should analyze the assess the different options for the design of the controller. One of the most critical teaching objectives at this model level is understanding design for stability and performance. Students understand that there is a trade off between the two, and proper design should be a compromise between stability and performance, depending on the system requirements [35]. Bode plots are introduced as tools to help visualize system response characteristics in frequency domain, and the step response is introduced as a means to observe the time domain system response to a step in the input.

Students are encouraged to study the effect of parameter variation on the various response characteristics of the system. Phase margin should be identified as a metric for relative stability, and students should be able to easily read it off the Bode phase response plot. Moreover, students should also note the effect of parameter variations

on the performance metrics, such as over-shoot, settling time, and steady-state error. Based on these metrics, students should be able to come up with controller parameters that fit the design's stability and performance requirements. Figure 6-6 shows an example of how variation in certain parameters can affect the phase margin (PM), causing significant ringing.

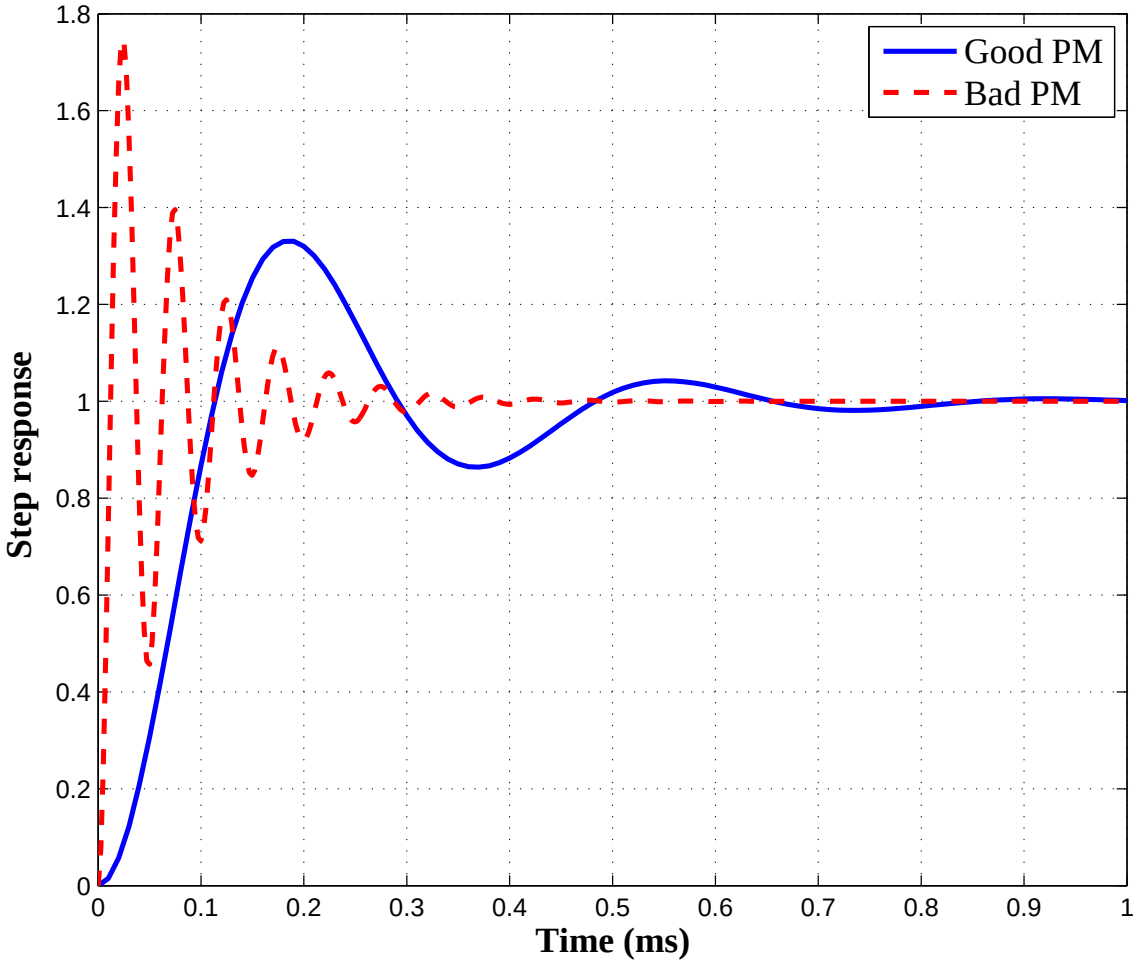


Figure 6-6: An example of a closed-loop transfer function plot of a controller design with good phase margin, and one with poor phase margin.

A possible controller to use for the kit is a PI controller, with an additional pole to attenuate higher frequency components and thus provide lead compensation in addition to the PI controller. Bode plots of the loop transmission of the model in Figure 6-5 are shown in Figure 6-7. The controller, which corresponds to $G(s)$ shown

in Figure 6-5, commands inductor current. In this model, the controller commands the peak inductor current allowed, beyond which the high-side switch of the buck power stage is turned off. The variation in the inductor current, denoted by i'_L in Figure 6-5 is estimated by measuring the current of the high-side switch.

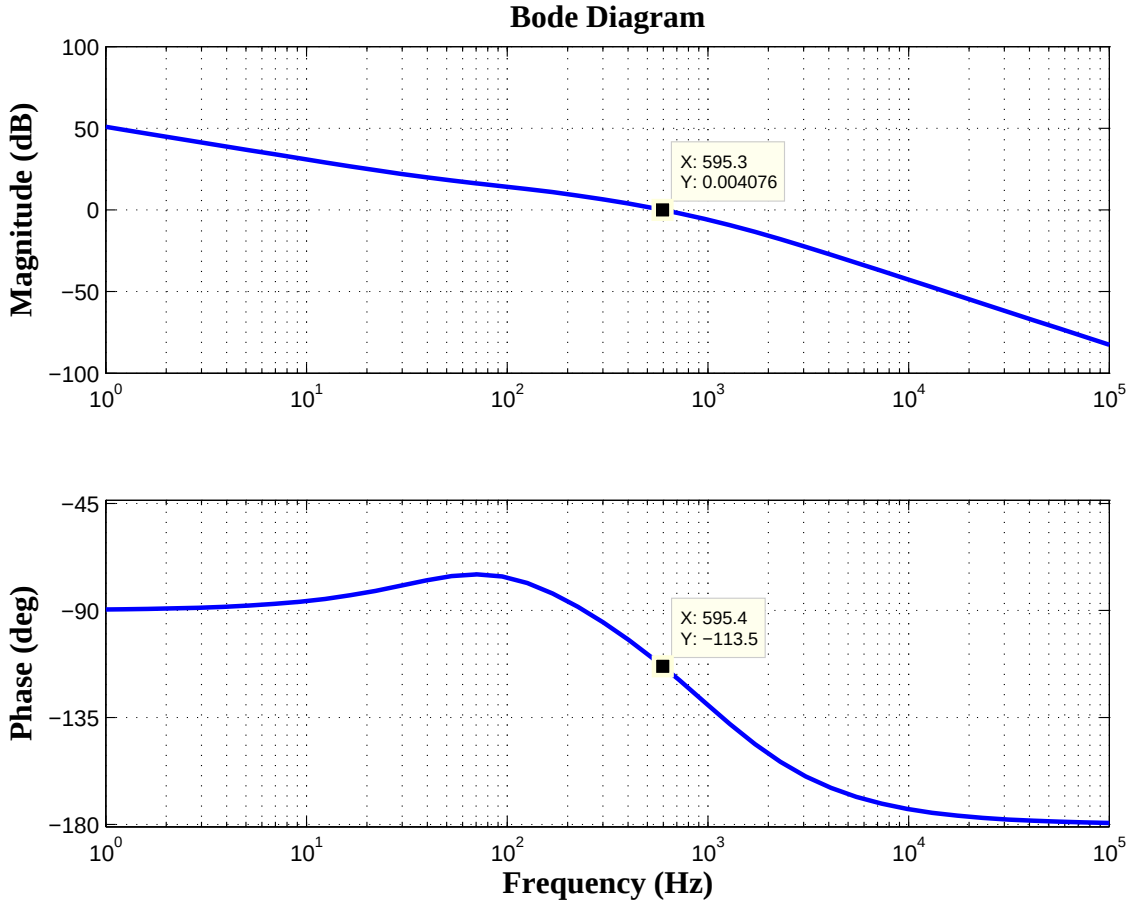


Figure 6-7: Bode magnitude and phase plots of the control loop transmission. The phase margin can be easily read off the Bode phase plot as the difference between the phase at unity gain and -180°. In this case, there is 66.5° of phase margin.

Note that other circuit blocks, such as the voltage regulator and the bandgap reference, also utilize local feedback. Similar analysis can also be performed so that proper stability and performance is ensured.

6.3.3 Behavioral-Level Model

After the analysis of the control aspect of the system through the control-level model is completed, the next step is to devise circuit implementations of the subsystems. At this level, students translate the blocks whose dynamics have been analyzed into circuit blocks that are readily available in SPICE libraries (e.g. LTSpice), such as operational amplifiers, comparators, idealized switches, clock generators, and digital logic. The detailed transistor-level implementation of these blocks are irrelevant in this model level. The objective at this stage is to design circuits whose dynamics match the expected behavior that was analyzed at the control-level model.

A possible behavioral-level model of the power controller kit is shown in Figure 6-8. This model uses operational amplifiers, a comparator, and some digital logic, as a first pass behavioral design to implement the controller.

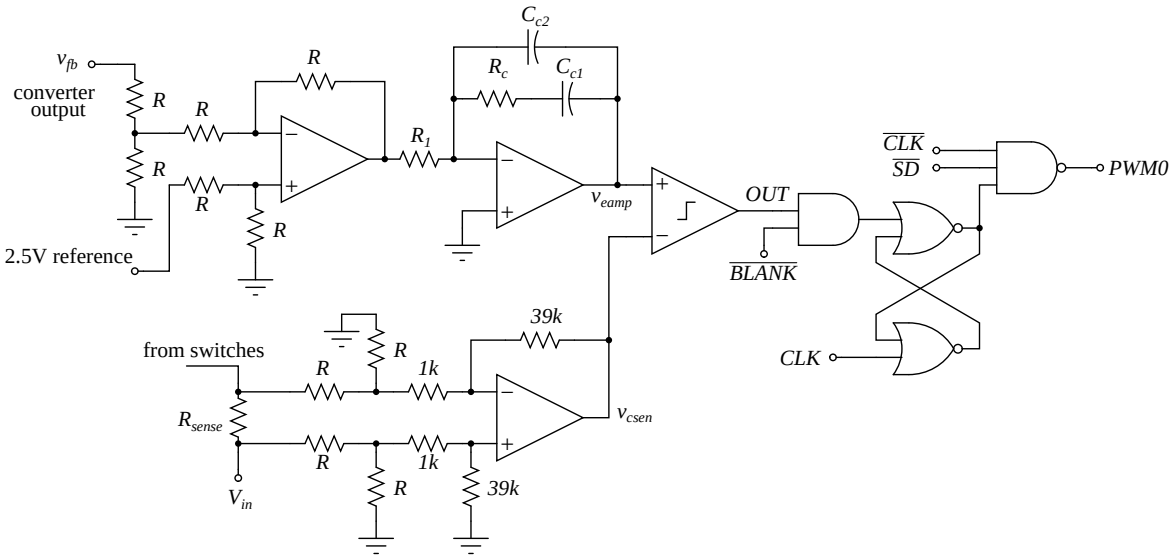


Figure 6-8: Behavioral model of the controller kit. The control functionality is implemented using idealized blocks as a first pass behavioral design.

The functionality of the controller can be demonstrated using SPICE simulations. Students are encouraged to perform both time-domain and frequency-domain simulations on the various portions of the behavioral model using transient and ac analysis. Important teaching objectives can be established during simulations at the behavioral-level model. Students need to design test circuits in order to be able to

run a successful simulation with meaningful results.

Students should note, for example, that if there are circuit blocks that are implemented in open-loop configuration, then closing the loop around that block for testing purposes is necessary. Otherwise, students may end up with erroneous frequency response characteristics and wrong gain values due to the saturation of the amplifier. In addition to this, it is crucial that students devise test circuits that have proper conditions for providing a well defined dc operating point. This is important not only in dc bias point simulations, but also in ac small-signal analysis, where a fixed dc operating point is needed.

A possible test circuit for the error amplifier block, which is part of the behavioral-level diagram in Figure 6-8, is shown in Figure 6-9. The fact that there is a pole at the origin means that the gain is undefined at dc, and thus the dc operating point is ill-conditioned. A large feedback resistor can be added to keep a finite dc gain. However, the offset voltage of the operational amplifier can saturate the amplifier if it is not accounted for. One solution is to place a large capacitor in series with R_1, as shown. One can also correct the offset by adding a voltage source at one of the operational amplifier inputs, and tweaking its value. At the behavioral-level model, students should be able to characterize the various circuit blocks using simulations.

6.3.4 Device-Level Model

The last model abstraction level is the device-level. As mentioned earlier, one of the outcomes of having the hands-on kit is that students can learn circuit design through the different and diverse circuit blocks available. At this model level, all the circuit blocks such as operational amplifiers, comparators, clocks, and other blocks are implemented using transistors and passive components. No integrated circuits or any built-in blocks were used in the design of the power controller kit's circuit blocks. Students use devices that are readily available, such as 2N3904 and 2N3906 NPN and PNP BJTs, respectively, as well as 2N7000 N-MOSFETs and ZVP3306A P-MOSFETs.

After the device-level circuits are designed, it is important to verify that the

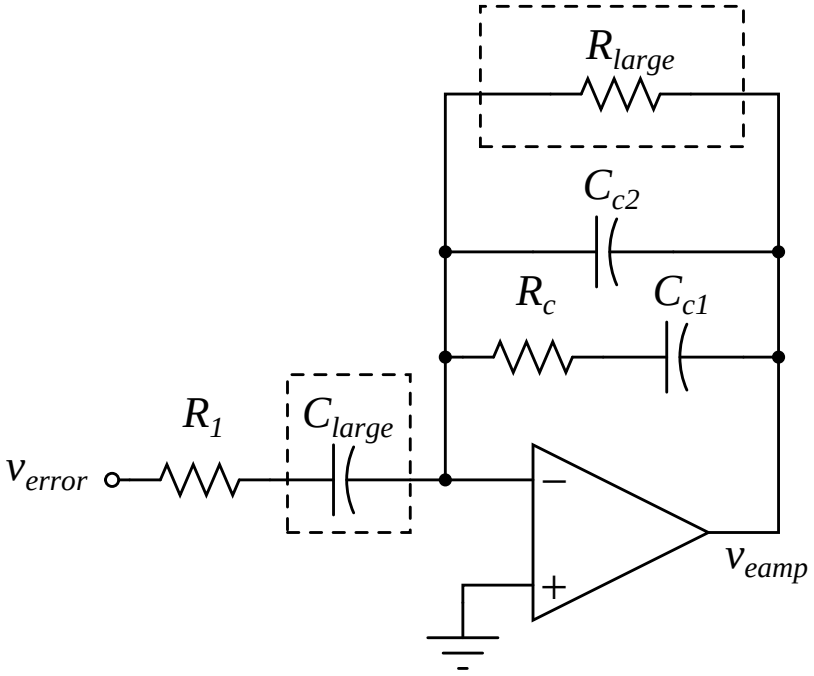


Figure 6-9: A possible test circuit for the error amplifier implementation in Figure 6-8. The components shown in the dashed boxes ensure a stable dc operating point.

functionality of the transistor-level circuits match that of the circuit blocks analyzed in the behavioral-level modeling stage. Once again, students should perform transient and ac analyses, and compare the time-domain and frequency-domain simulation results between those at the behavioral-level and device-level.

As part of the learning process, it is also equally important to compare the simulation results against the expected ones from hand calculations. Back-of-the-envelope calculations provide reasonable intuition on how and which components influence certain metrics and specifications, but students have to be aware of the approximations and linearizations that are assumed. Simulations provide nonlinear and more complex device modeling, but should agree, to a first order, with what students expect from their hand calculations.

One of the most important skills circuit designers possess is their knowledge of device parasitics and how they can impact the design. The device-level modeling stage can be an opportunity for instructors to shed light on this topic, and illustrate examples of how certain parasitics can severely affect the circuit behavior. These

parasitics, in fact, become only apparent at the device-level model. For example, a behavioral-level model of the buck power stage would use ideal switches, and these switches do not capture the actual power device parasitics, such as gate capacitance as well as rise and fall times.

Students should always keep the previous model levels in the back of their minds. Due to the iterative nature of design, students are expected to continually go back and forth between the different model levels. Moreover, it is also important to keep in mind that all models, at all model levels, have their limitations; the more accurate the model is, the more time it takes for it to produce the results. There is an inherent tradeoff between model fidelity and simulation time that students should keep in mind.

6.4 Design Examples

The following section contains examples that not only present interesting teaching goals which can be achieved through some of the kit's circuit blocks, such as the voltage regulator, but also point out some of the issues that students may encounter while applying the proposed design methodology. For example, it is important to note that it is not necessary that every circuit appears in all model levels. Utility circuits such as the bandgap and voltage references circuit block form a significant block that is needed for the operation of almost all other blocks, but in terms of dynamics, does not pertinently show up at the control-level model of the power controller. In addition to this, it is emphasized that sometimes certain differences between experimental and SPICE-simulated results can and will occur. Students need to be able to account for and explain the reasons why the experiment differs from their model, whether it is due to differences in device parameters, PCB layout issues, or some other reason. The clock circuit serves as an example of how and why this can happen.

6.4.1 Voltage Regulator

The voltage regulator circuit is a simple and illustrative way to use operational amplifiers. It involves one of the most basic control strategies that can be taught to students, namely dominant pole compensation [35]. This can be an opportunity for instructors to use this block to teach and experiment with various control methods. Furthermore, from a circuit design perspective, the voltage regulator introduces prevalent circuit blocks, including current sources and differential pairs. Concepts of feedback, compensation, and loading can be introduced and analyzed using this circuit block.

In addition to this, more advanced concepts such as the analysis and modeling of the regulator when a step in the load is applied can also be illustrated here. Instead of using the regulator response to a step in the bandgap voltage as the performance metric, the regulator's response to a load step is used. Students can learn how this can be modeled as a constant current perturbation for the system to remain linear and time invariant. This can be illustrated in a control-level model, as shown in Figure 6-10.

Next, a behavioral-level as well as a device-level model can be created. Figure 6-11 shows these models (R_L denotes the load resistance). These models can all be simulated and have their results compared with each other. The result of the device-level load step simulation is shown in Figure 6-12.

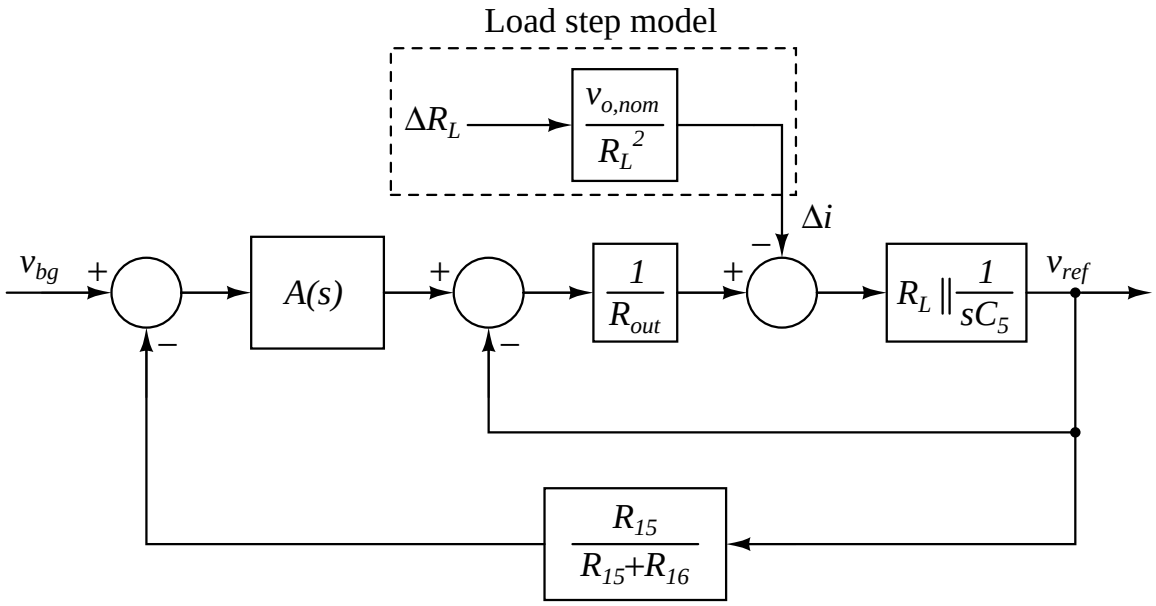


Figure 6-10: Control-level model of the voltage regulator circuit, with load step modeled as a current perturbation. R_L is the output load. ΔR_L is placed instantaneously in series with R_L to create a step in the load. R_{out} is the output impedance of the operational amplifier.

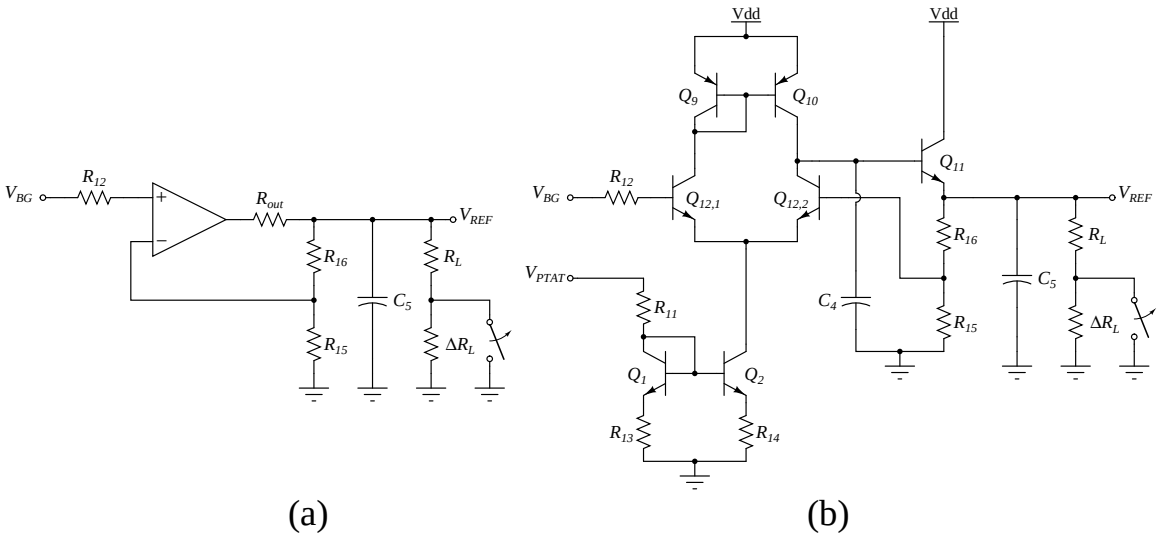


Figure 6-11: (a) Behavioral-level model of the voltage regulator, and (b) its corresponding device-level model.

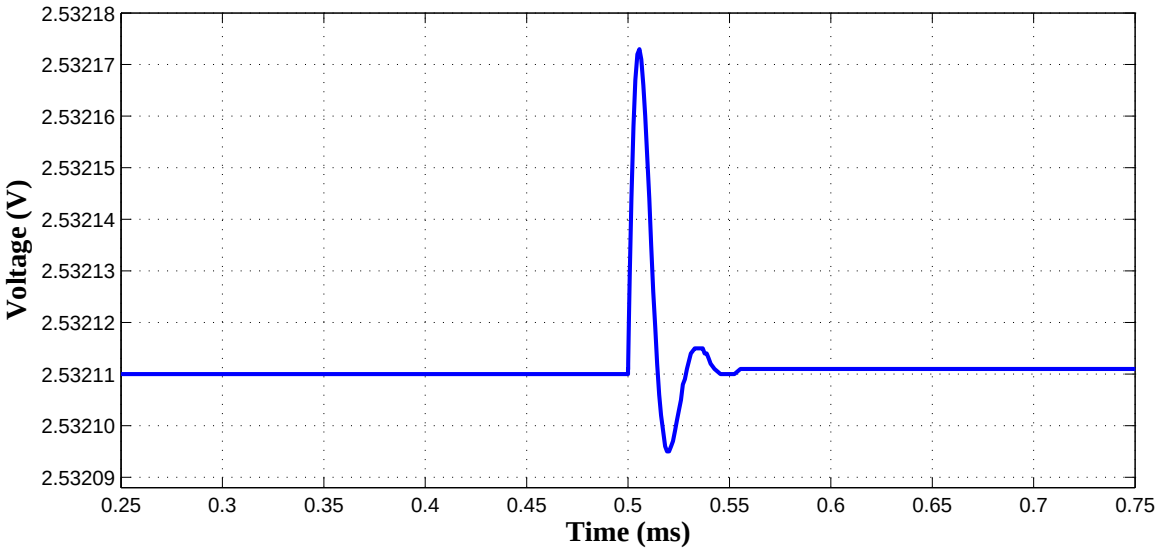


Figure 6-12: Simulation of the voltage regulator response to a step in its load.

6.4.2 Bandgap Reference

Another interesting example is the bandgap reference circuit. As mentioned earlier, the bandgap circuit does not result directly from the control-level model, and can be used as a circuit block to convey this aspect to students. This circuit block suffers from a start-up issue, i.e. the circuit has a stable operating point at 0V. This aspect might be exposed at the device-level model, but definitely not at the behavioral-level model. In fact, this aspect portrays one of those less obvious issues encountered in circuit design, which may not even be detected from simulations. This stresses the fact that building the actual circuit after modeling it is an invaluable exercise.

Figure 6-13 [3] illustrates the concept behind the bandgap voltage, and can serve as a system-level model of the circuit block. It reflects the drift in the base-to-emitter voltage of a BJT with temperature, and how the thermal voltage V_T can be used to compensate for the drift. This leads to the generic implementation, i.e. the behavioral-level model, in Figure 6-14.

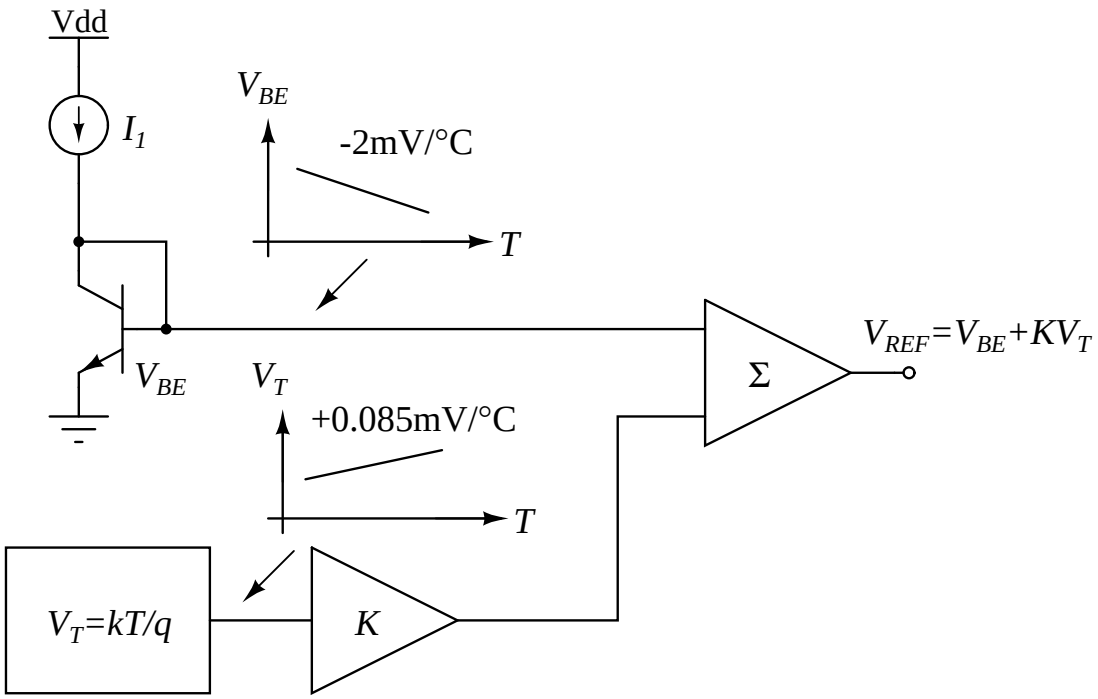


Figure 6-13: Illustation of bandgap voltage creation [3].

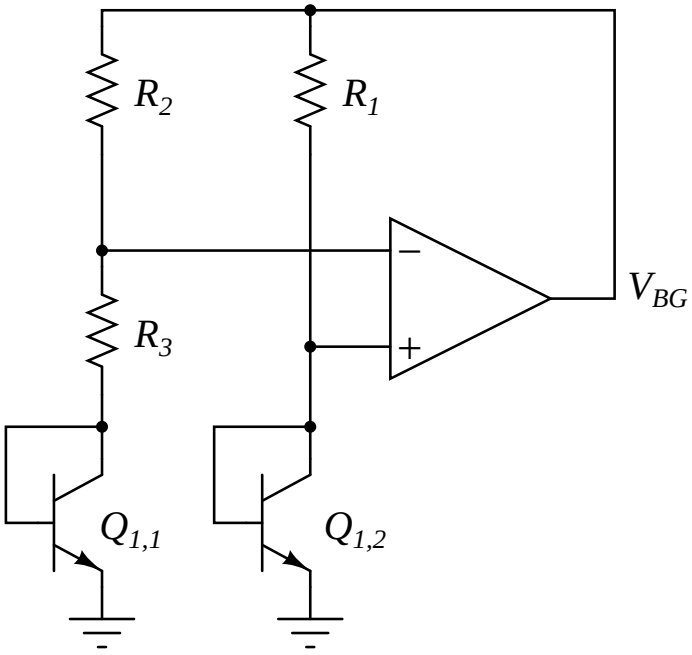


Figure 6-14: Behavioral level model of the bandgap voltage circuit block.

It can be observed that there is no indication of any start-up issue with this model. The device-level circuit is shown in Figure 6-15. At this level, start-up circuitry can be incorporated to prevent the circuit from settling at the 0 V trivial state. From this model, students should point out that the current through $Q_{1,1}$ is PTAT, and can thus utilize it, with the use of current mirrors, to create a PTAT voltage source to be used in other circuit blocks of the power controller. This is shown in the left half of Figure 6-15. An interesting teaching point here is performing a temperature sweep simulation, and observing the variation of the bandgap and the PTAT voltages. The result is shown in Figure 6-16, which matches our expectations.

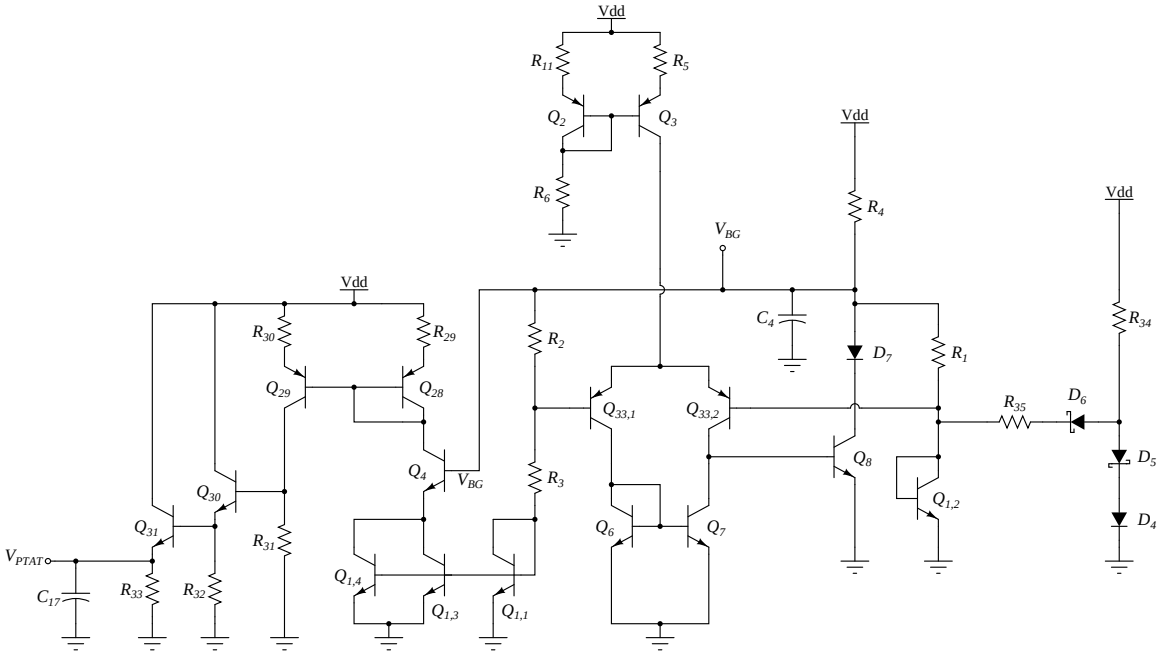


Figure 6-15: Device-level bandgap voltage circuit block. Students can mirror the PTAT current through $Q_{1,1}$ to create a PTAT voltage source.

6.4.3 Clock

The third design example that illustrates the teaching benefits of the power controller kit is the clock circuit block. An important teaching objective here is to provide a hands-on experience on how variations in certain device parameters can severely impact the response characteristics. Robust design that is independent of the device

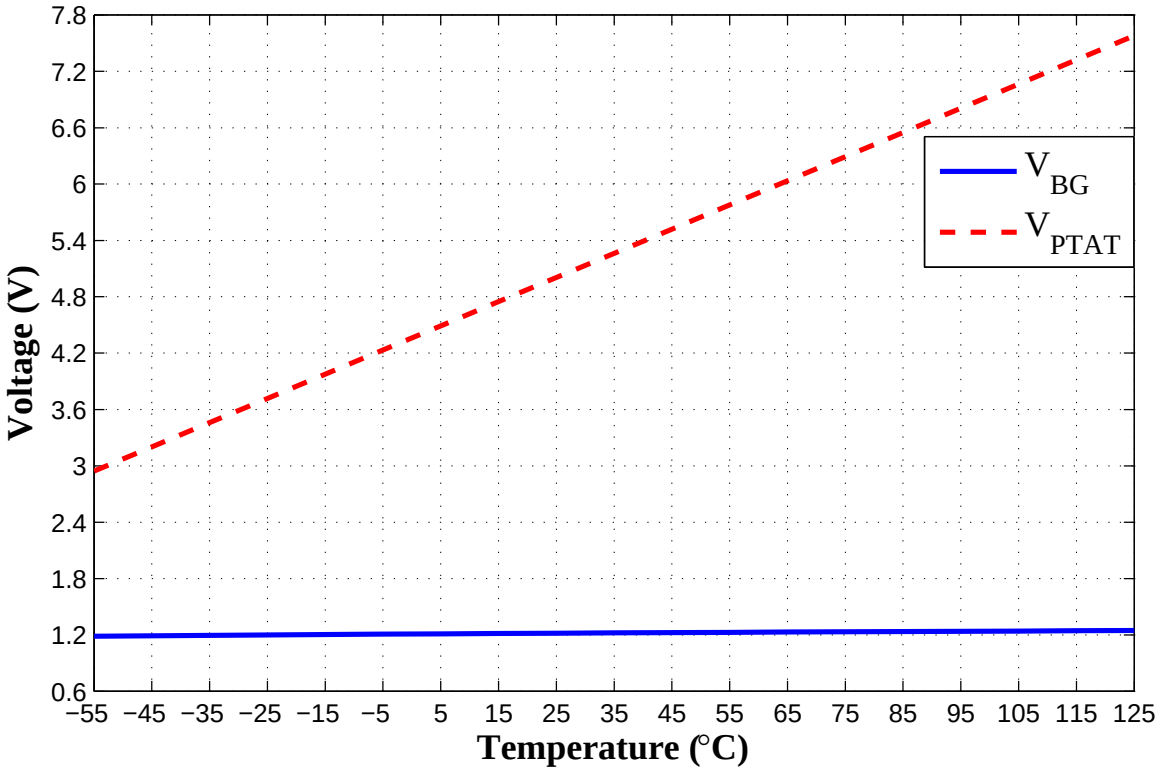


Figure 6-16: Temperature sweep simulation showing the variation of PTAT and the bandgap voltages with temperature.

nonidealities and variations in the manufacturing process is thus promoted and encouraged. The clock circuit also illustrates how the design process follows a spiral trajectory, whereby students iterate through the different model levels until the design objectives are met. It is an example of how simulation by itself does not guarantee identical operation in practice. However, when proper hand calculations are made, and when the design process is followed correctly, debugging becomes easier, and the number of iterations is low. Moreover, explaining the differences between simulation and experiment becomes much easier.

Figure 6-17 shows a behavioral-level model of the clock used in this kit. It consists of a single-input Schmitt trigger, which toggles at fixed high and low threshold voltages. When the Schmitt trigger output is low, the bottom current source I_{dis} is off, and I_{chg} charges up C_2 at a rate equal to $m_r = I_{chg}/C_2$. When CLK is high, the bottom current source is on, and the capacitor voltage discharges at a rate $m_f = (I_{dis} - I_{chg})/C_2$, i.e. the slope of the voltage is $-m_f$. From this information,

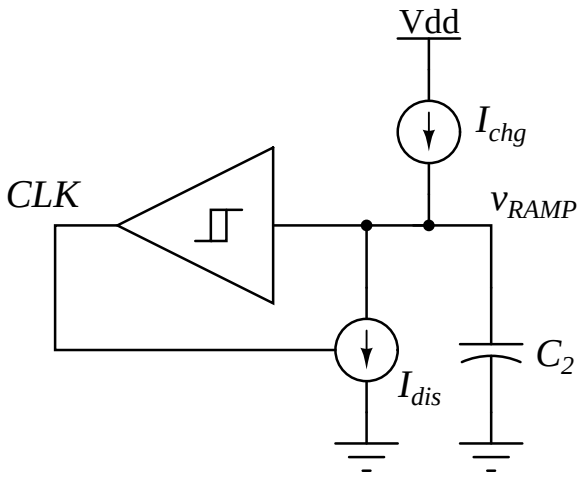


Figure 6-17: Clock behavioral-level model. The clock pulse is the output of the Schmitt trigger, CLK. I_{chg} and I_{dis} control the pulse duration and the clock switching frequency.

the times t_r and t_f taken for the capacitor voltage to rise from V_{th1} to V_{th2} or fall from V_{th2} to V_{th1}, respectively, can be calculated as follows:

$$t_r = \frac{V_{th2} - V_{th1}}{m_r} = \frac{C_2(V_{th2} - V_{th1})}{I_{chg}} \tag{6.1}$$

$$t_f = \frac{V_{th1} - V_{th2}}{-m_f} = \frac{C_2(V_{th1} - V_{th2})}{I_{chg} - I_{dis}} \tag{6.2}$$

Therefore, it can be seen that I_{chg} and I_{dis} are the design handles that set both the duration of the clock pulse as well as the clock frequency, f_{sw}, which is given by:

$$\frac{1}{f_{sw}} = \frac{C_2(V_{th2} - V_{th1})}{I_{chg}} + \frac{C_2(V_{th1} - V_{th2})}{I_{chg} - I_{dis}} \tag{6.3}$$

Figure 6-18 shows the device-level clock circuit. Notice how Q_1 and Q_2 perform the function of a single-input Schmitt trigger, with the resistors R_1 and R_2 configured in positive feedback to set the thresholds V_{th1} and V_{th2}.

Consider the case when, for example, the top current source in Figure 6-18 is configured to provide a current $I_{chg} \approx 95\mu$A, and the bottom current source is configured such that $I_{dis} \approx 620\mu$A. The simulation result of the clock circuit is shown in Figure 6-19, and the experimental result is shown in Figure 6-20. Notice how the

clock frequencies are different; the simulation gives a 97.4kHz clock pulse, while the experiment results in a 60kHz clock pulse.

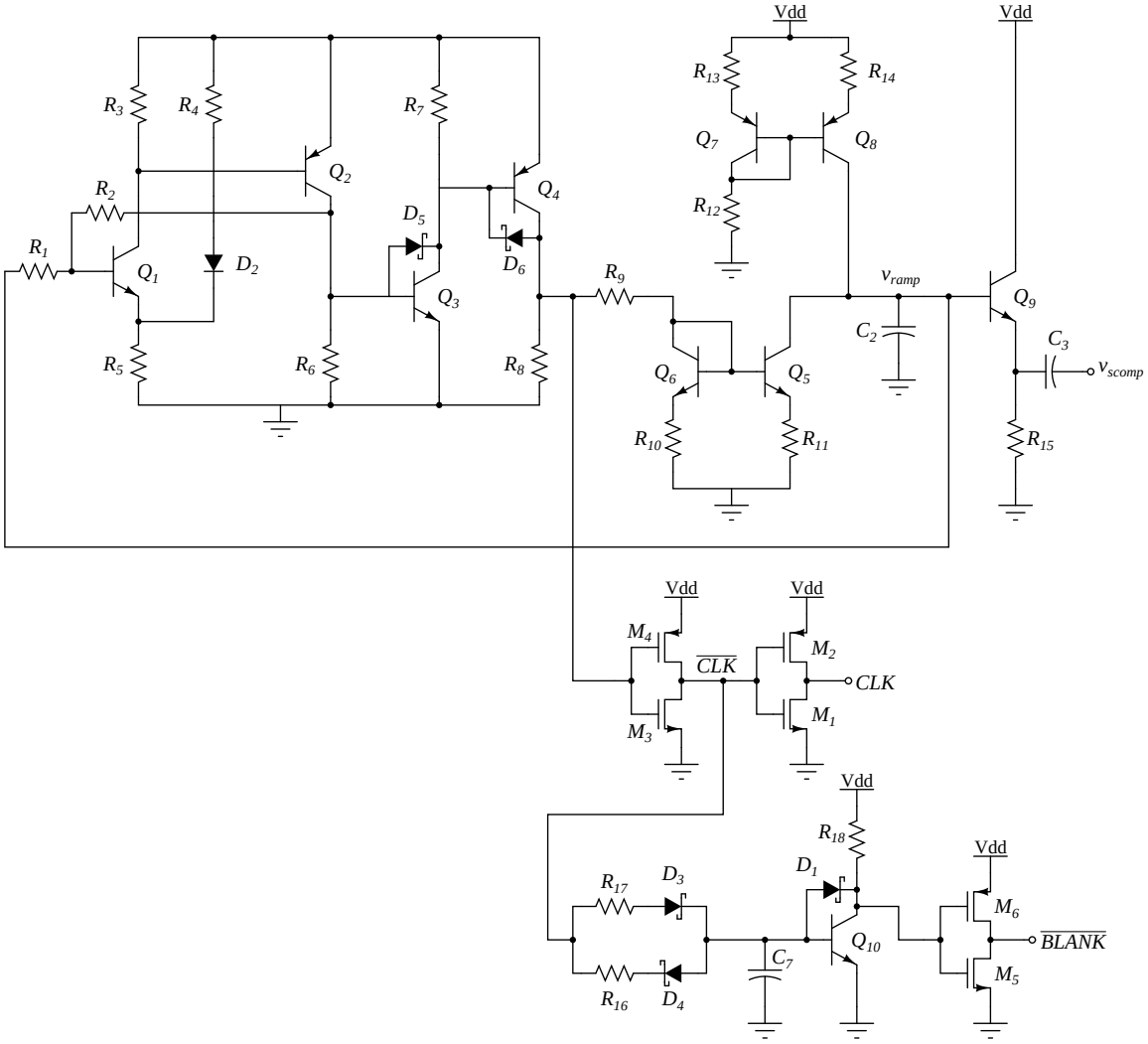


Figure 6-18: Device-level model of the clock. This circuit block generates a clock pulse, a ramp, as well as a blank signal, all of which are needed in the complete controller implementation.

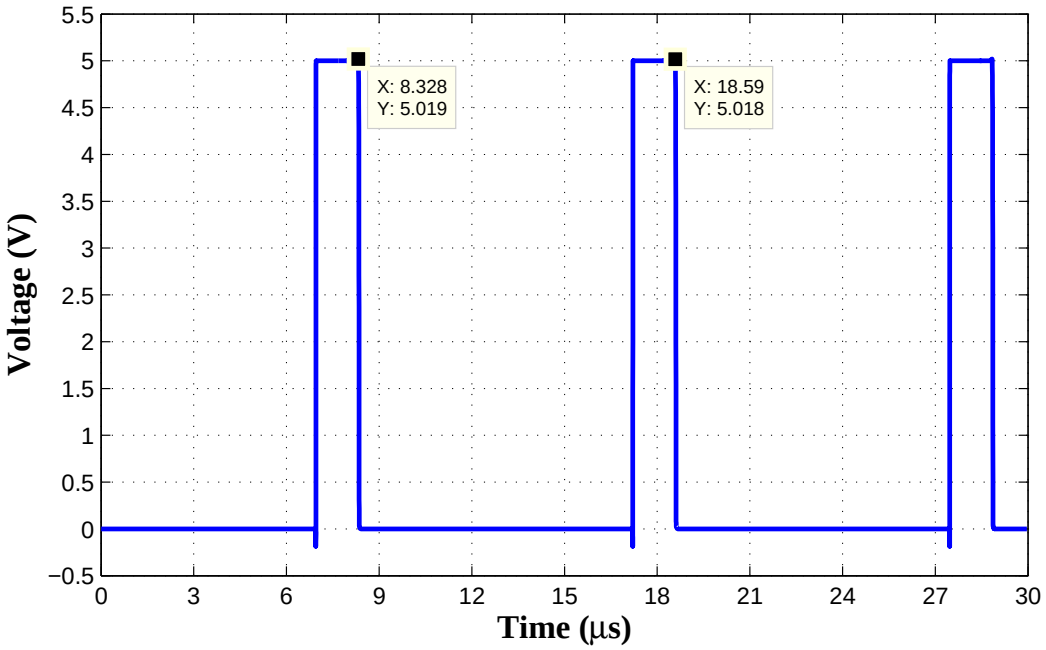


Figure 6-19: Result from a SPICE simulation of the clock circuit. The clock period is about 10.3μs, which corresponds to a clock frequency of 97.4kHz.

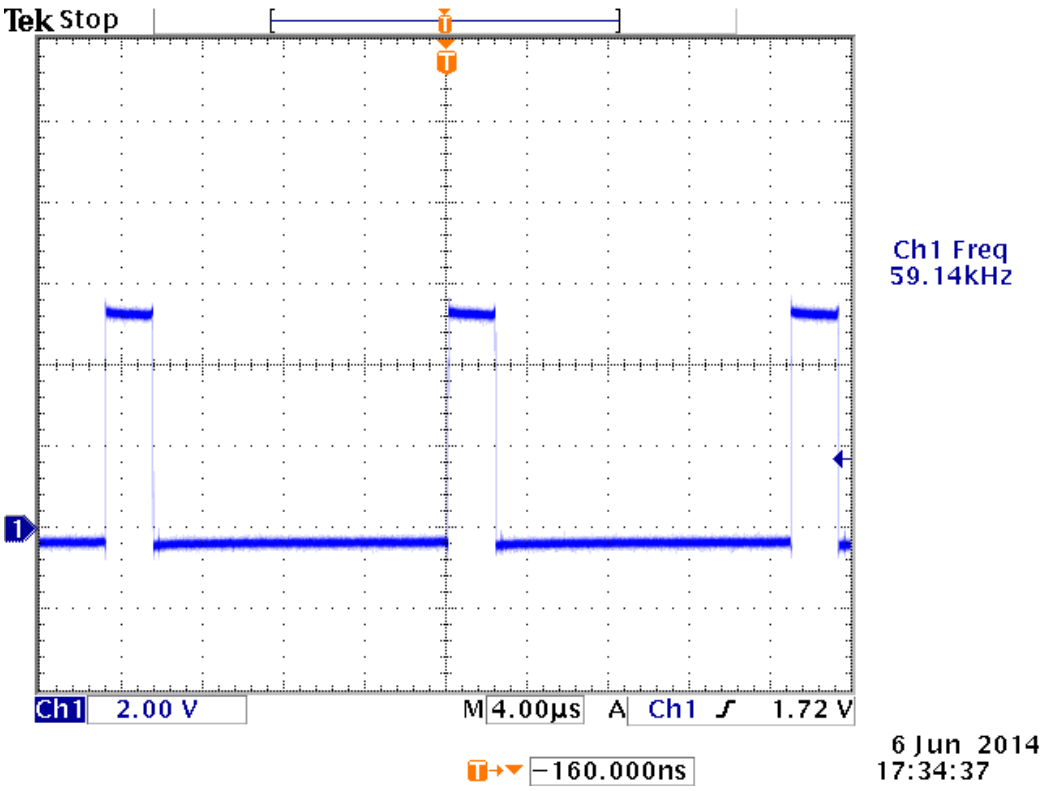


Figure 6-20: Clock experimental result. The scope shows a clock frequency close to 60kHz, as opposed to the 97.4kHz observed in the simulation.

The reason behind the discrepancy between the simulation and the experiment lies in the actual device-level implementation of the Schmitt trigger. Specifically, the turn-off times of transistors Q_1 and Q_2 have a significant effect on the frequency of the clock. A small error in modeling this parameter in SPICE for both Q_1 and Q_2 can result in a large change in the rise time of the ramp signal, and in turn result in a large change in the clock frequency. This comes from the fact that the falling edge of the ramp has a much steeper slope than that of the rising edge. This is needed because the clock pulse occurs during the falling edge of the ramp; the narrower the clock pulse, the higher is the maximum converter duty ratio the controller can sustain. Figure 6-21 illustrates the effect. It can be readily shown from the sketch that the errors in rise and fall times are related by the ratio of the slopes, as follows:

$$\Delta t_r = \left(\frac{m_f}{m_r}\right) \Delta t_f \tag{6.4}$$

Thus, the fact that we need $m_f \gg m_r$, i.e. $(m_f/m_r) \gg 1$, means that Δt_r is very sensitive to changes in Δt_f.

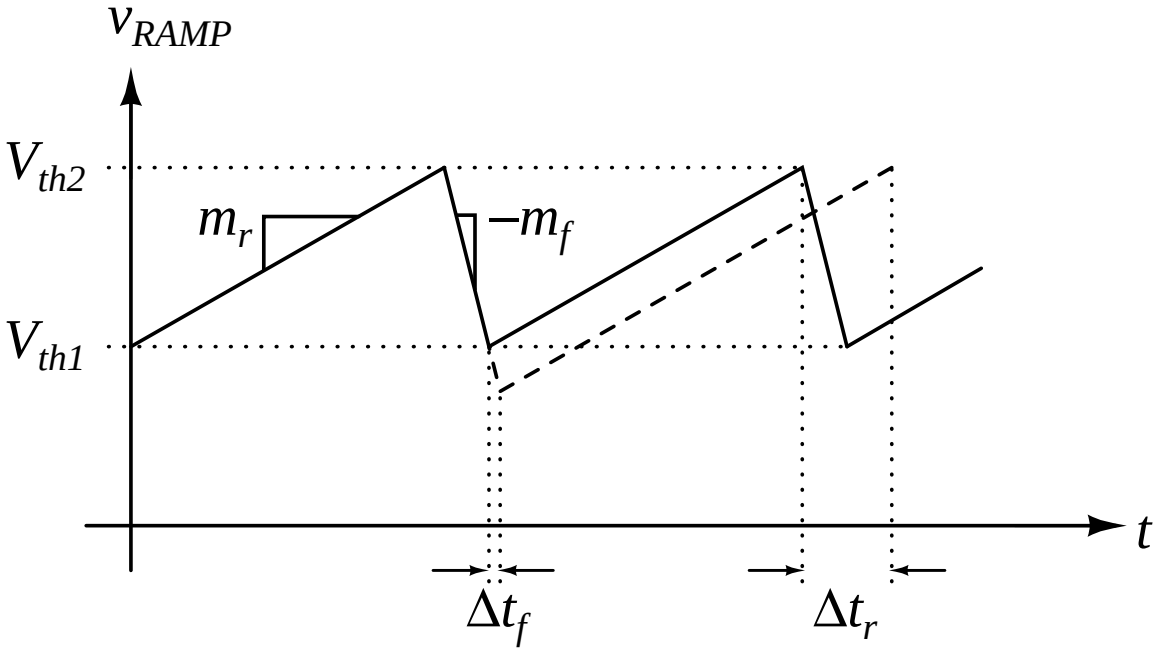


Figure 6-21: Clock model error illustration. When $m_f \gg m_r$, a small change Δt_f in the ramp fall time causes a much larger effect on the ramp rise time Δt_r.

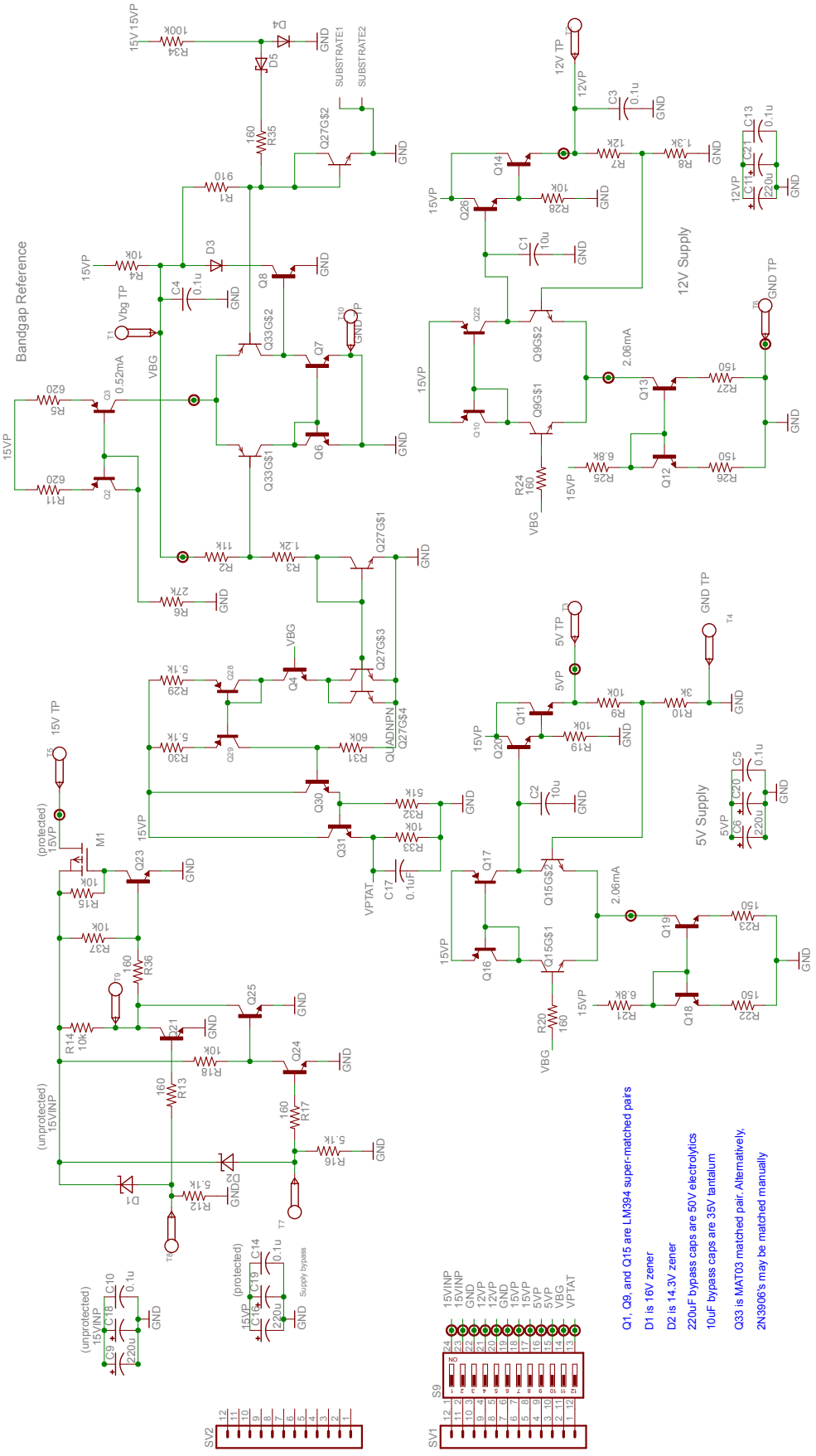
6.5 Conclusion

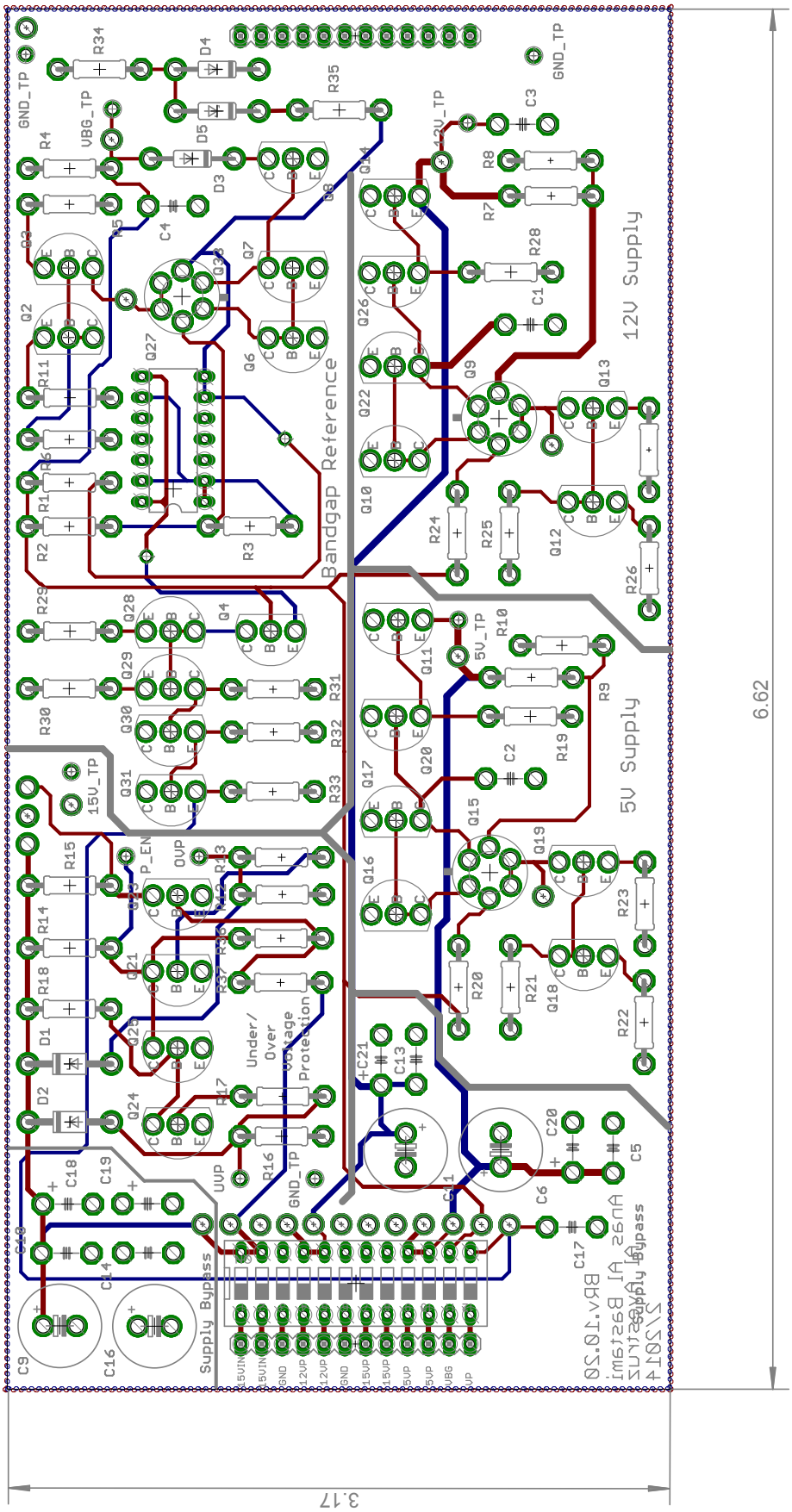
An educational power electronic controller kit was presented as an experimental platform for teaching modeling, control, and simulation in power electronics. A description of the kit's circuit blocks and their functionality was given. A methodology for proper system design that aims to eliminate poor engineering practices, such as running the whole controller through a time-domain device-level simulation, was illustrated. Going through the different model levels not only results in a full rigorous understanding of each subsystem and circuit block of the power converter and controller, but also significantly reduces the chances of students facing problems when building each circuit block. The different model levels also prevent prolonged hours of extensive simulation iterations and tweaking of component values. Various teaching objectives were proposed and explained at the different model levels. Three design examples, taken directly from the kit's circuit blocks, were also presented, and a number of important aspects of system design were pointed out and elaborated on. This system design methodology is applicable not only in the field of circuit design and power electronics, but can also be extended to all fields of engineering involving system design.

Appendix A

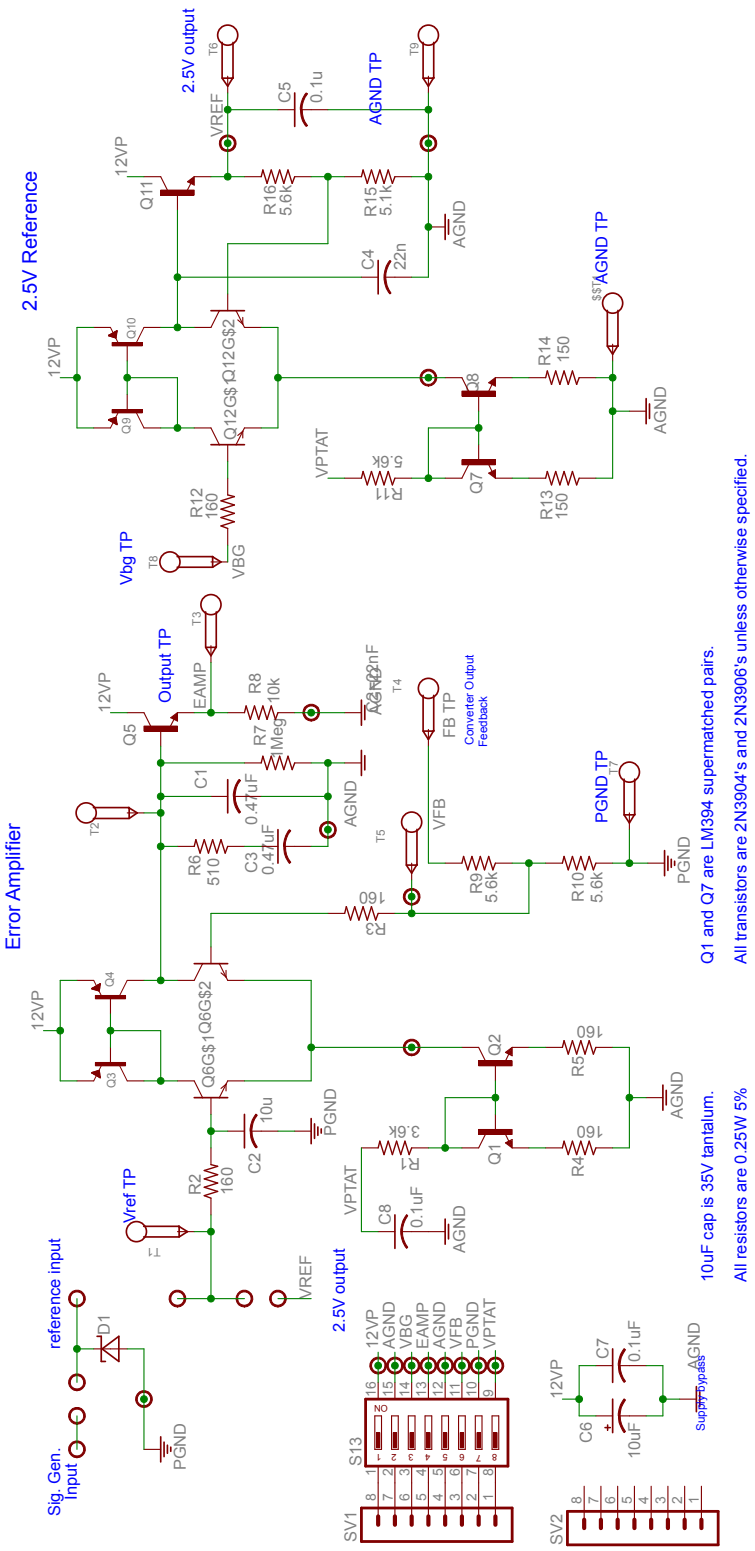
Schematics and PCB Designs

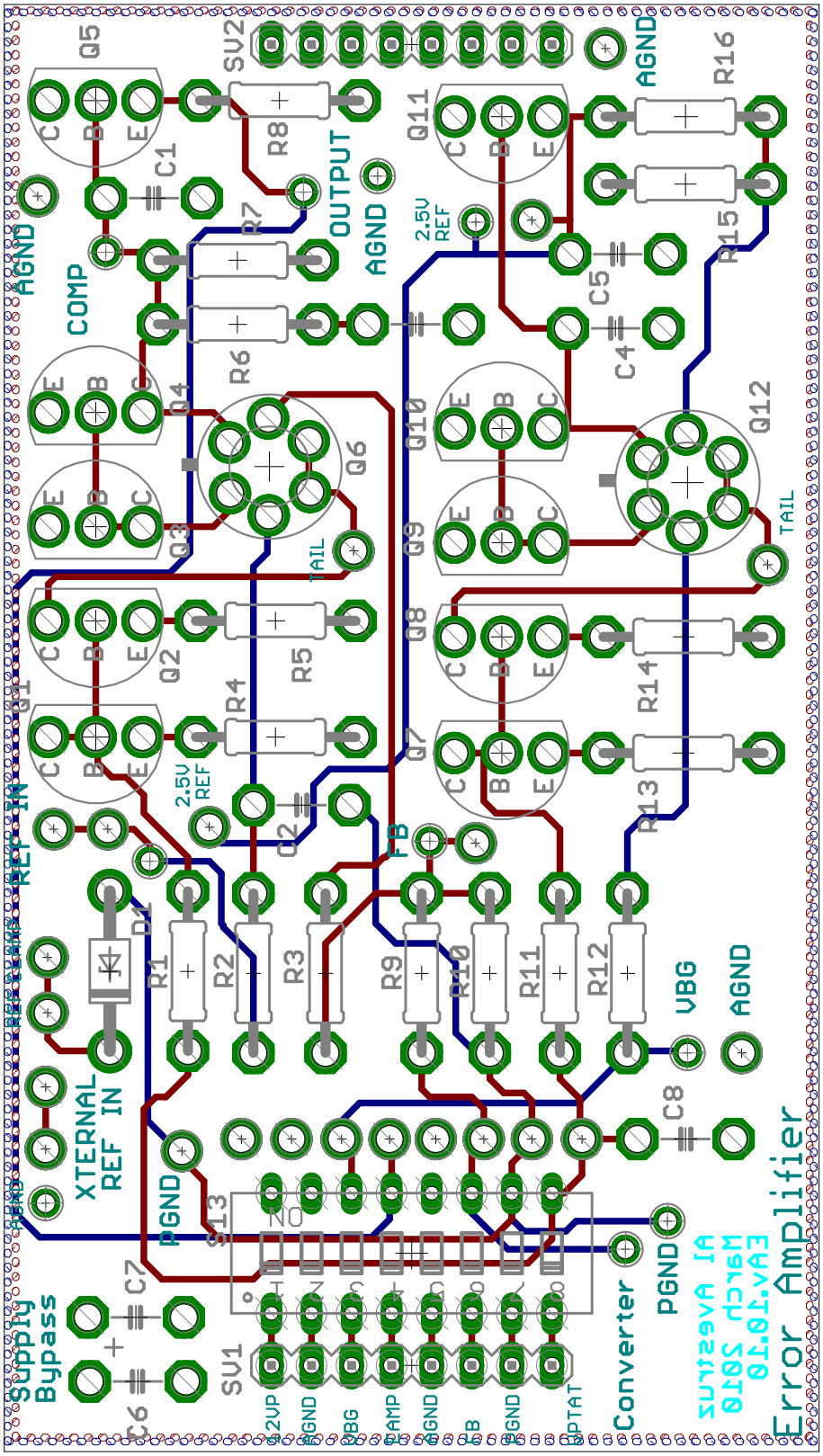
A.1 Bandgap and references schematic and PCB


Bandgap Reference
12V Supply
5V Supply
Q1, Q9, and Q15 are LM394 super-matched pairs
D1 is 16V zener
D2 is 14.3V zener
220uF bypass caps are 50V electrolytics
10uF bypass caps are 35V tantalum
Q33 is MAT03 matched pair. Alternatively,
2N3906's may be matched manually

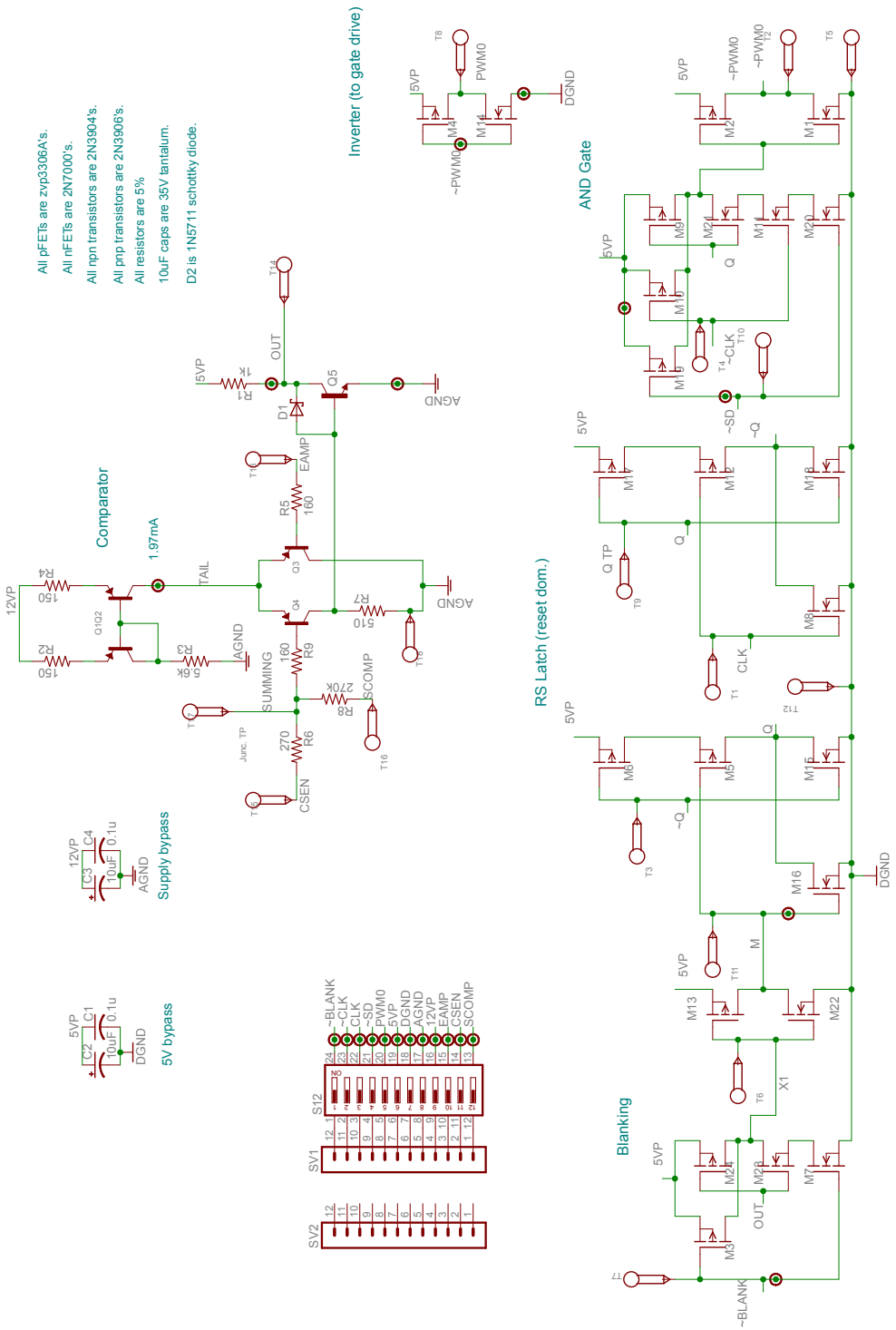

Bandgap Reference
12V Supply
5V Supply
Under/ Over Voltage Protection
Supply Bypass
6.62
3.17

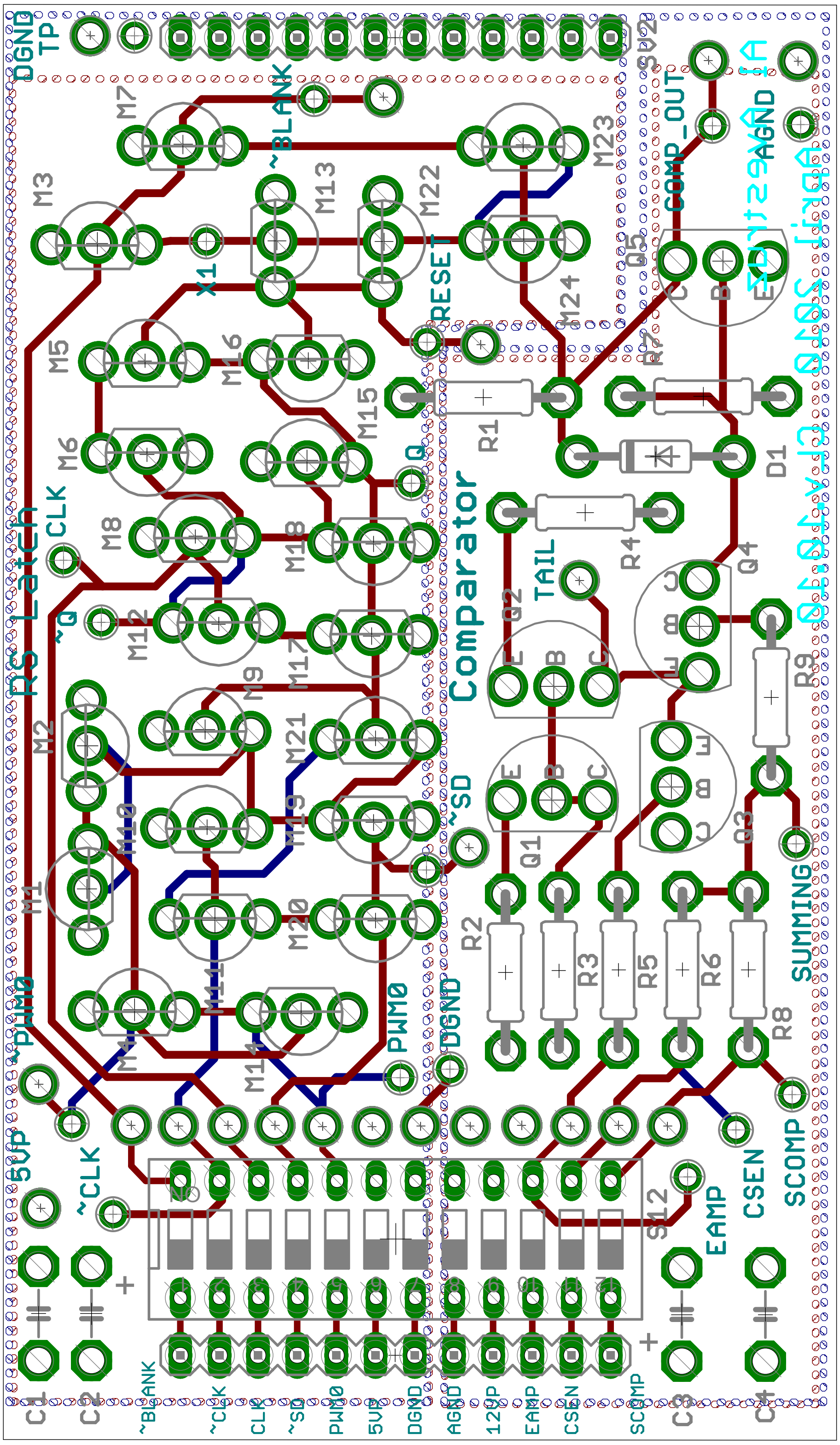
A.2 Error amplifier schematic and PCB



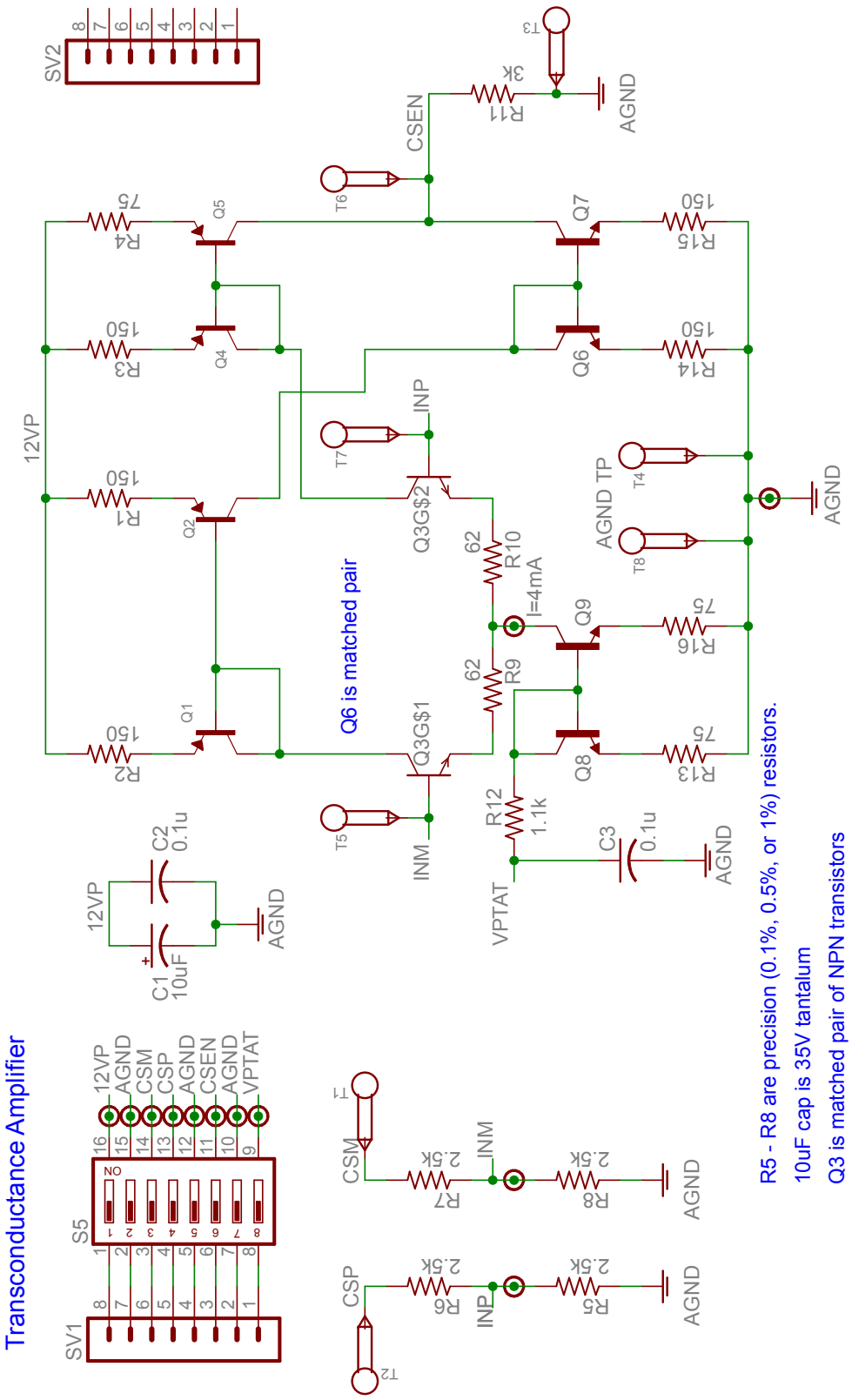

Error Amplifier
Supply Bypass
XTERNAL REF IN
COMP
OUTPUT
AGND
PGND
VBG
TAIL
FB
2.5V REF
Converter
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
C1
C2
C4
C5
C6
C7
C8
D1
SW1
SW2
SW3

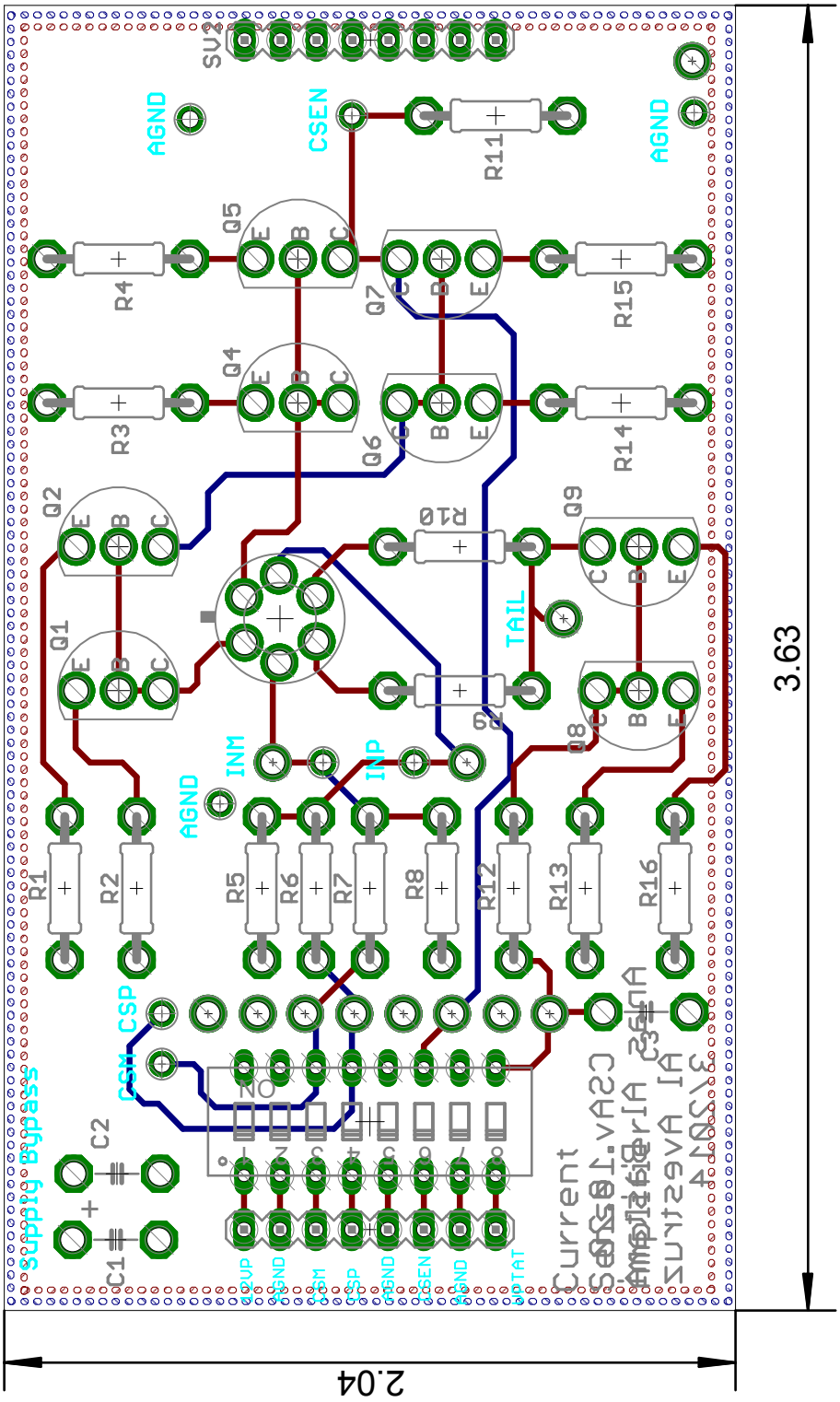
A.3 Comparator and latch schematic and PCB



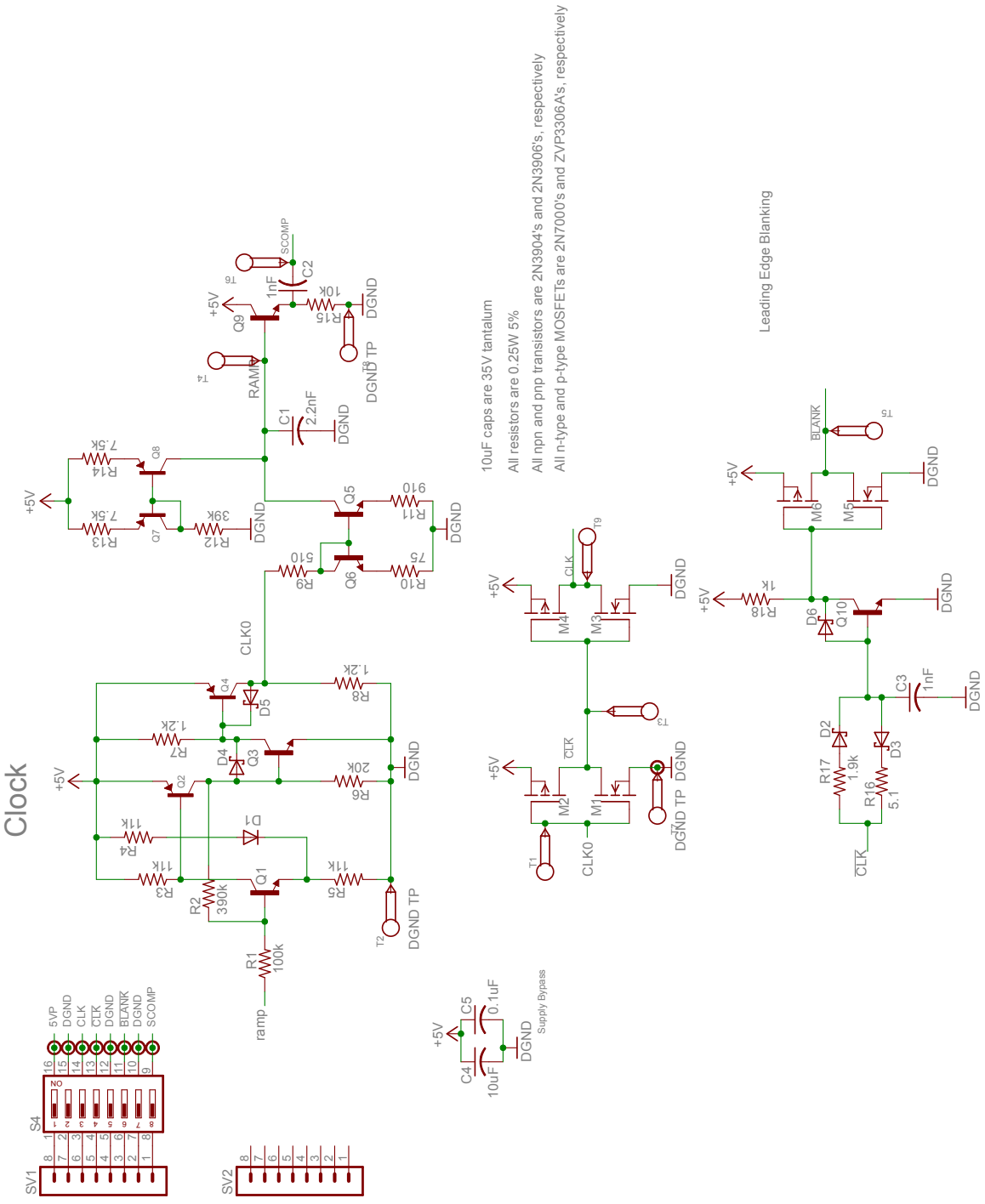

RS Latch
Comparator
DGND
TP
SV2
COMP_OUT
AGND
RESET
~BLANK
TAIL
SUMMING
SCOMP
CSEN
EAMP
~CLK
CLK
~Q
Q
~SD
PWM0
~PWM0
5VP

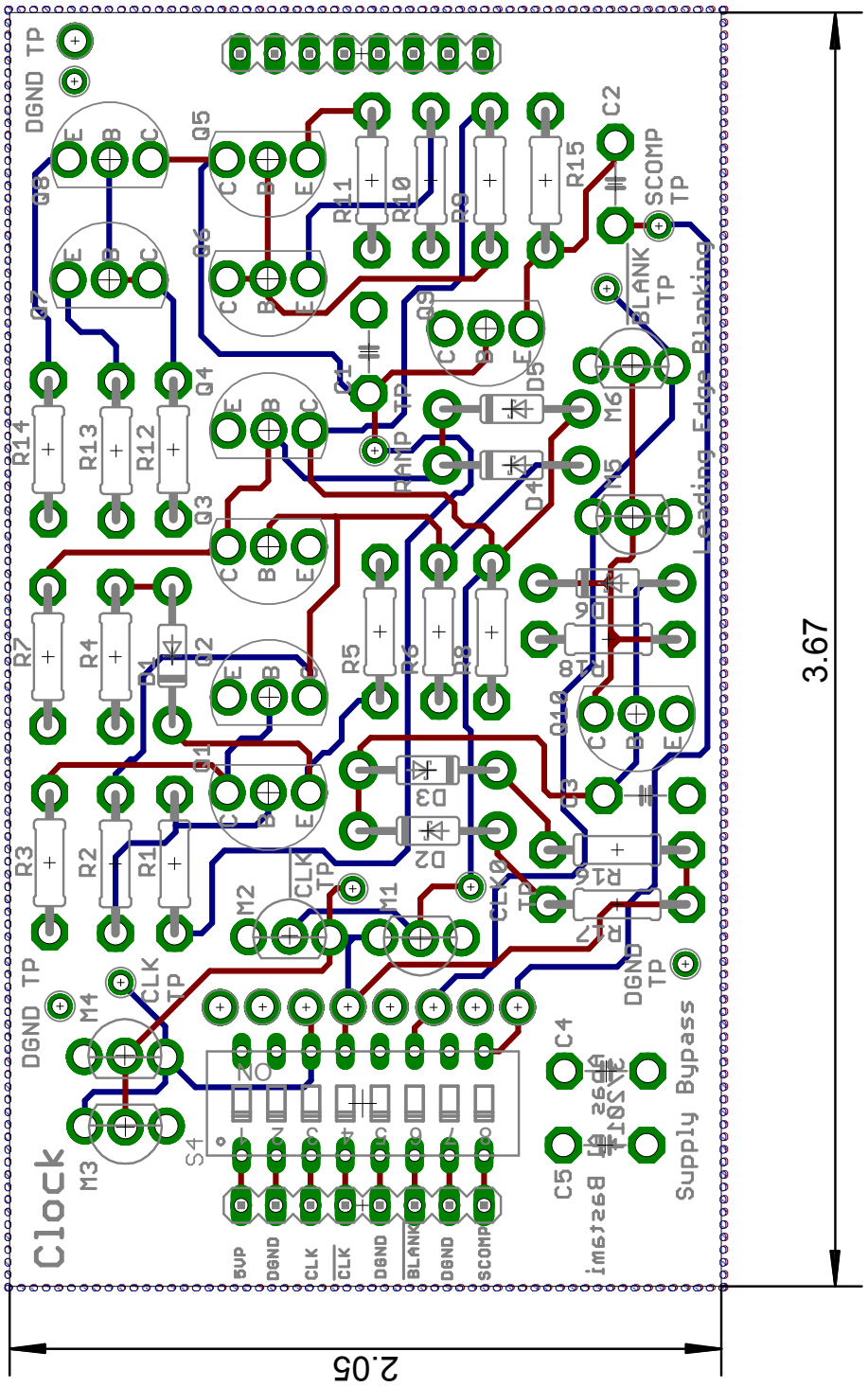
A.4 Current sense schematic and PCB



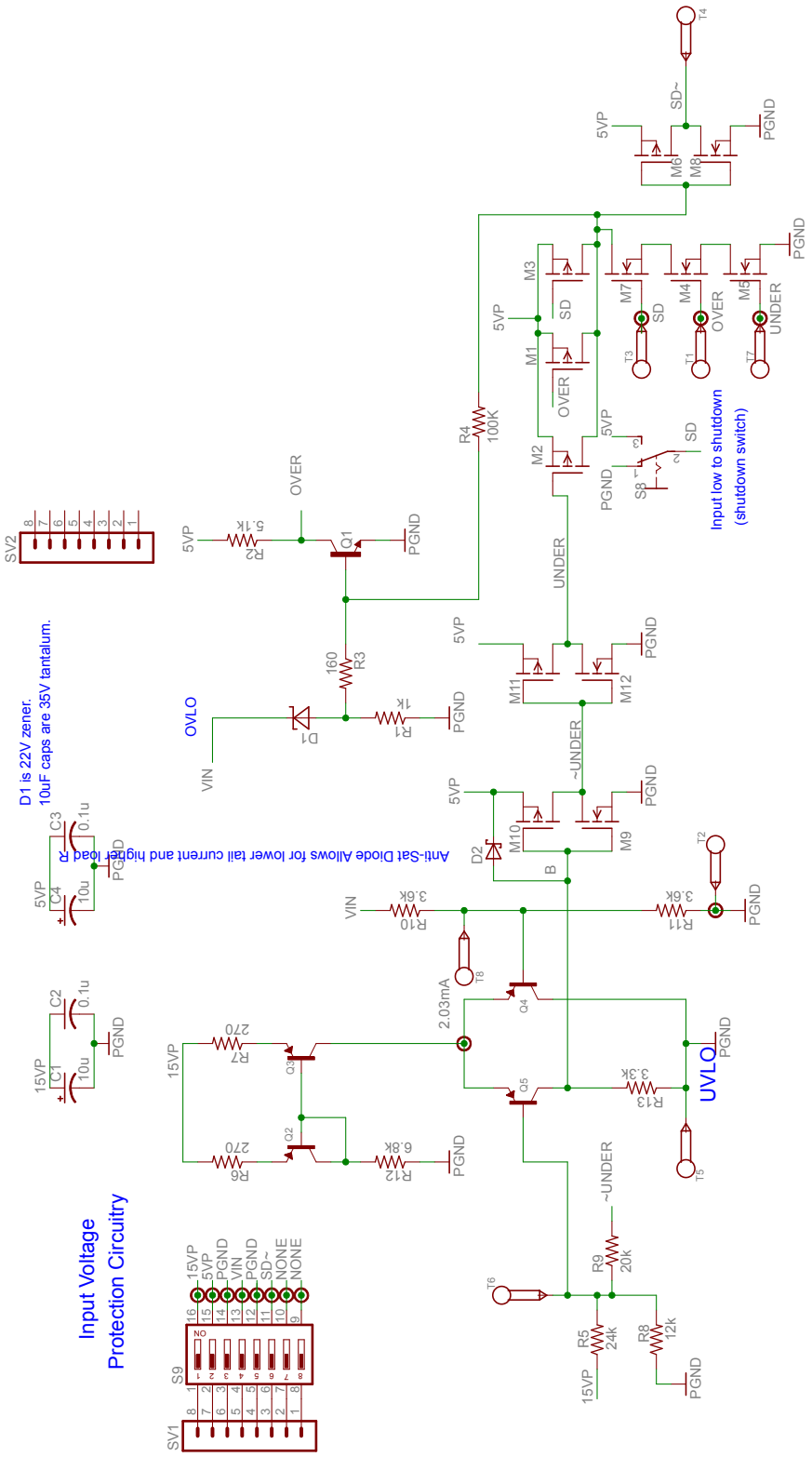

3.63
2.04
AGND
CSEN
INM
INP
TAIL
CSP
CSM
Supply Bypass
Current Sensor

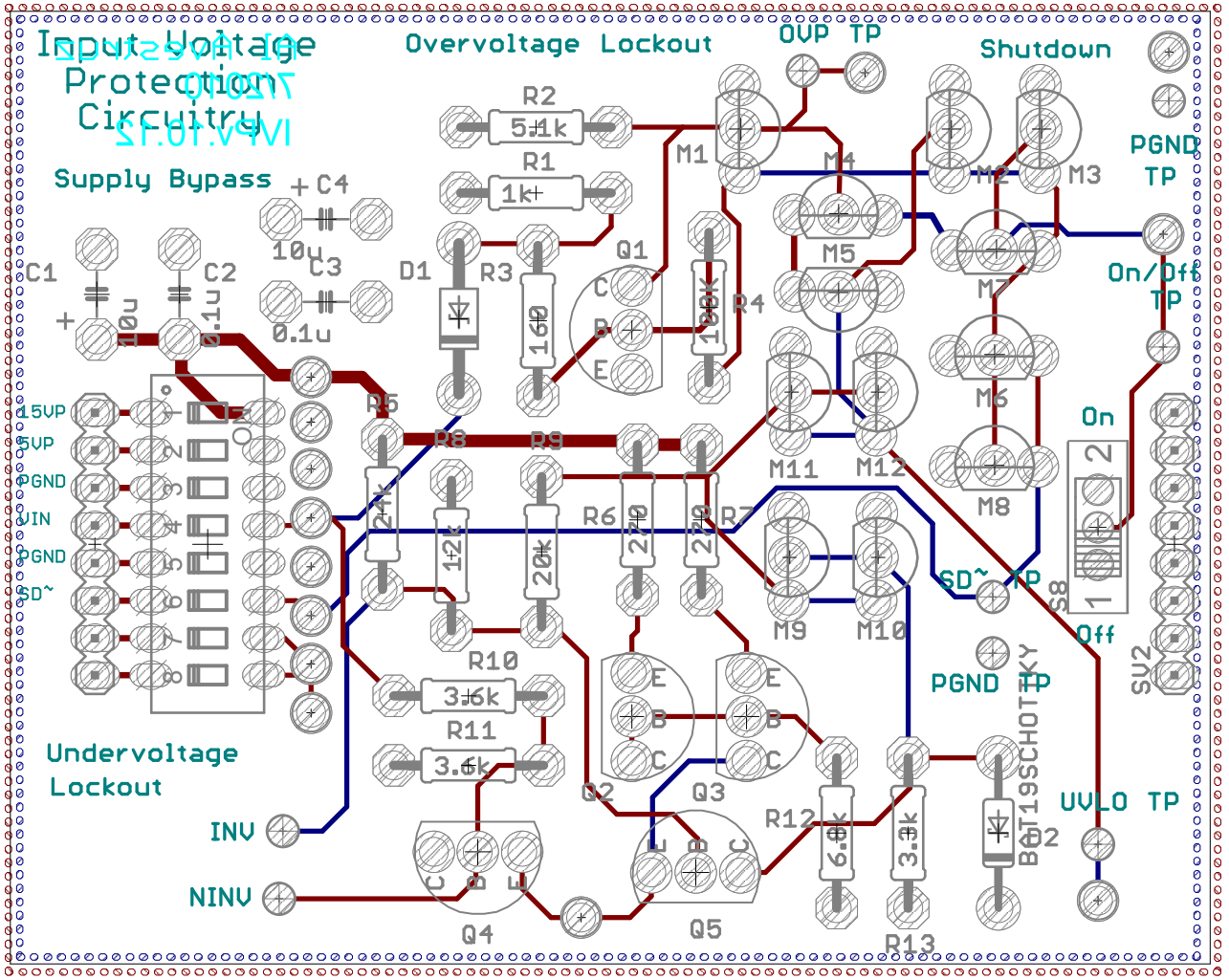
A.5 Clock schematic and PCB



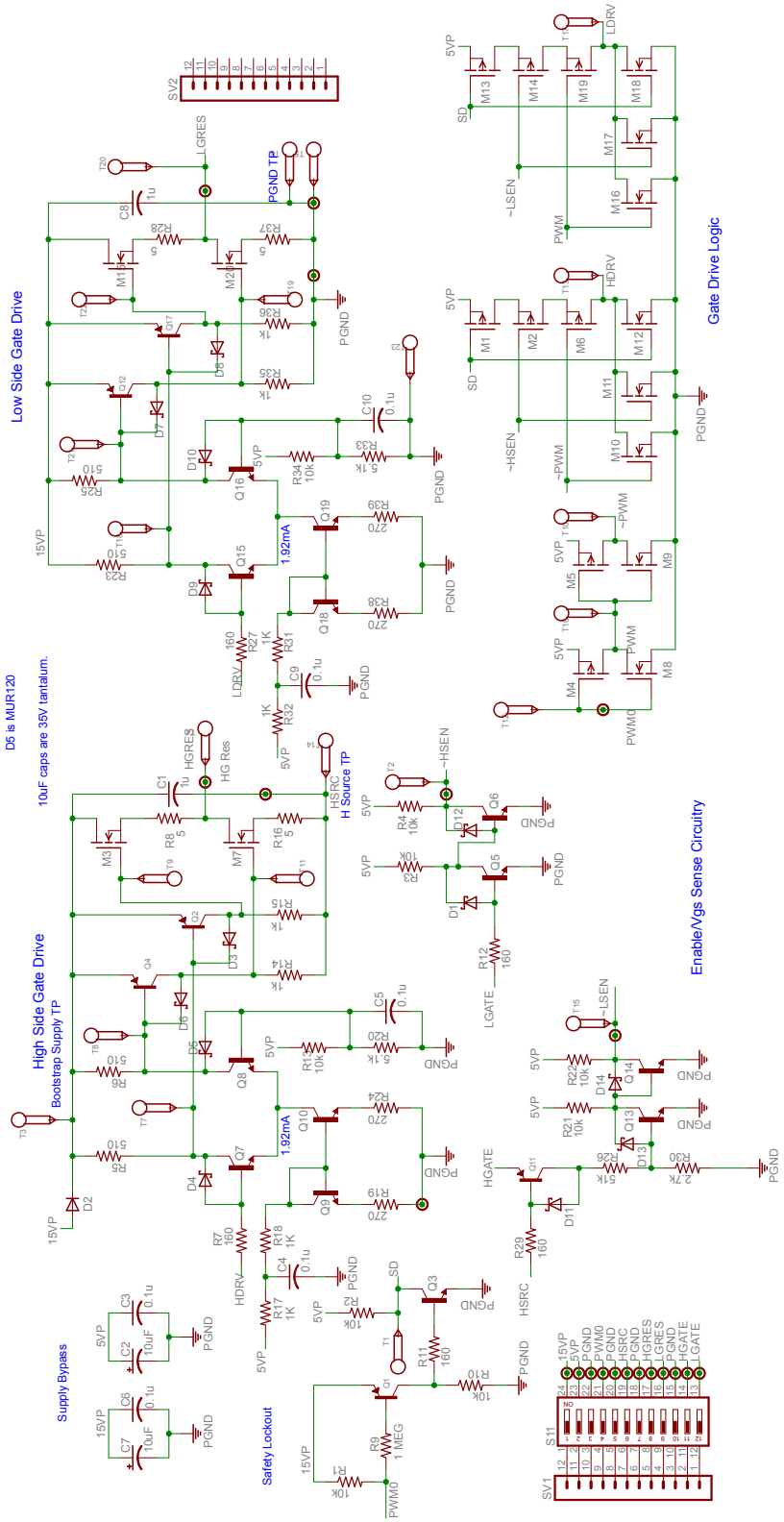

Clock
Supply Bypass
Leading Edge Blanking
DGND TP
SCOMP TP
BLANK TP
CLK TP
3.67
2.05

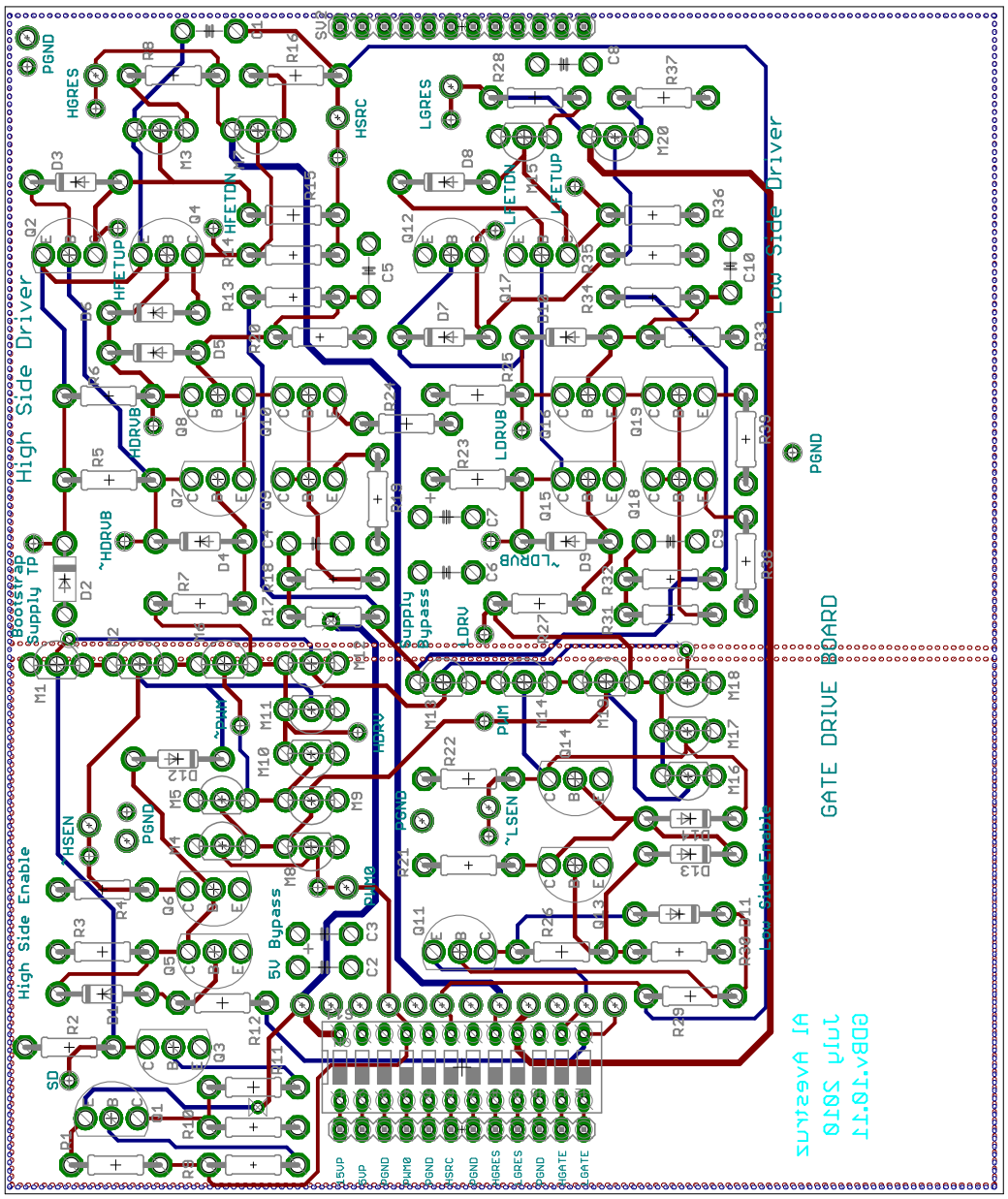
A.6 Shutdown schematic and PCB



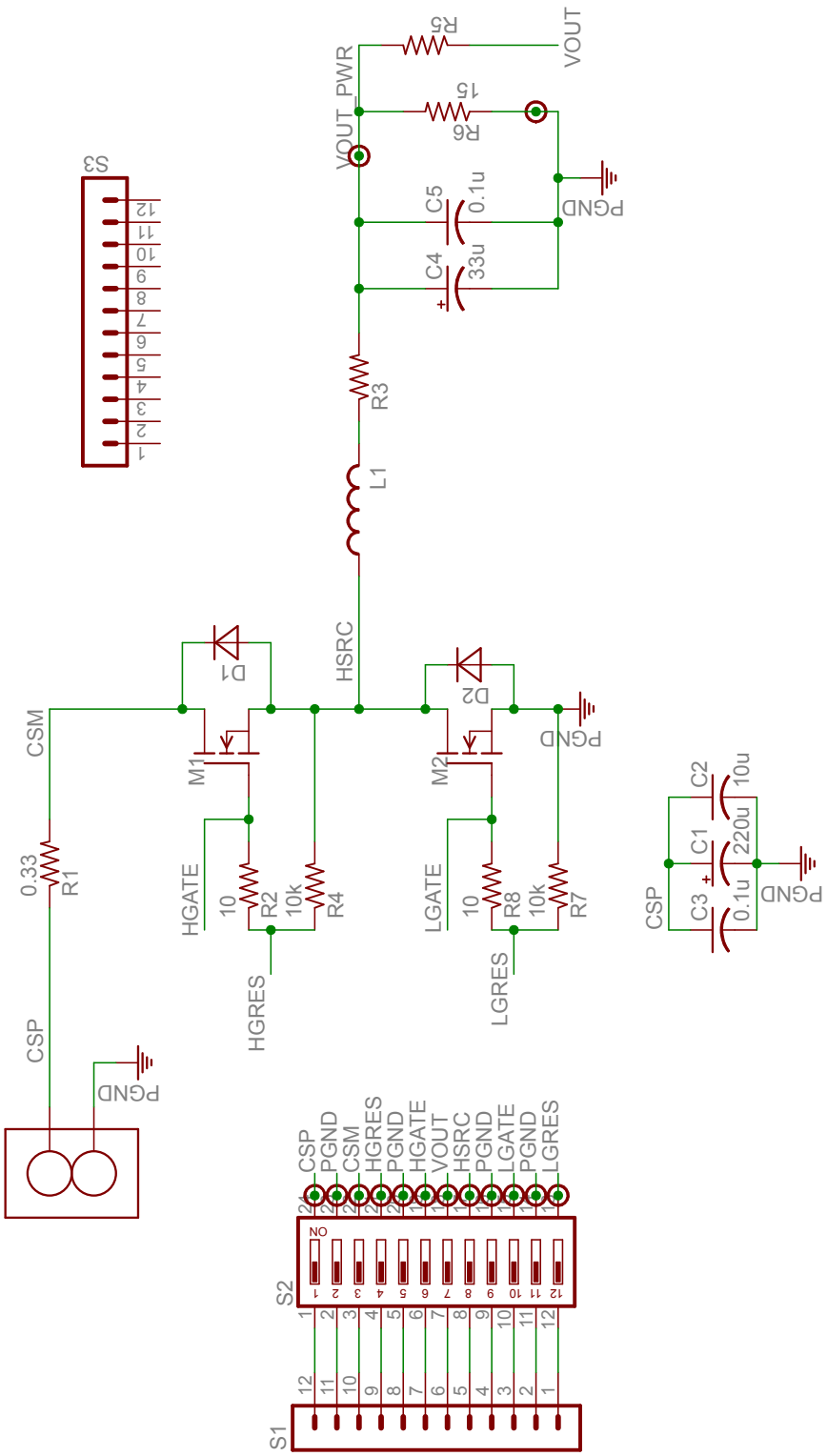

Input Voltage
Protection
Circuitry
Supply Bypass
Overvoltage Lockout
Undervoltage
Lockout
Shutdown
OVP TP
PGND
TP
On/Off
TP
On
Off
SD~ TP
PGND TP
UVLO TP
15VP
5VP
PGND
VIN
PGND
SD~
INV
NINV
C1
C2
C3
C4
10u
0.1u
0.1u
D1
R1
1k
R2
5.1k
R3
16Ω
Q1
R4
100k
R5
24k
R6
20k
R7
270
R8
12k
R9
270
R10
3.6k
R11
3.6k
Q2
Q3
Q4
Q5
R12
6.8k
R13
3.3k
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
D2
BAT19SCHOTTKY
S8
SV2

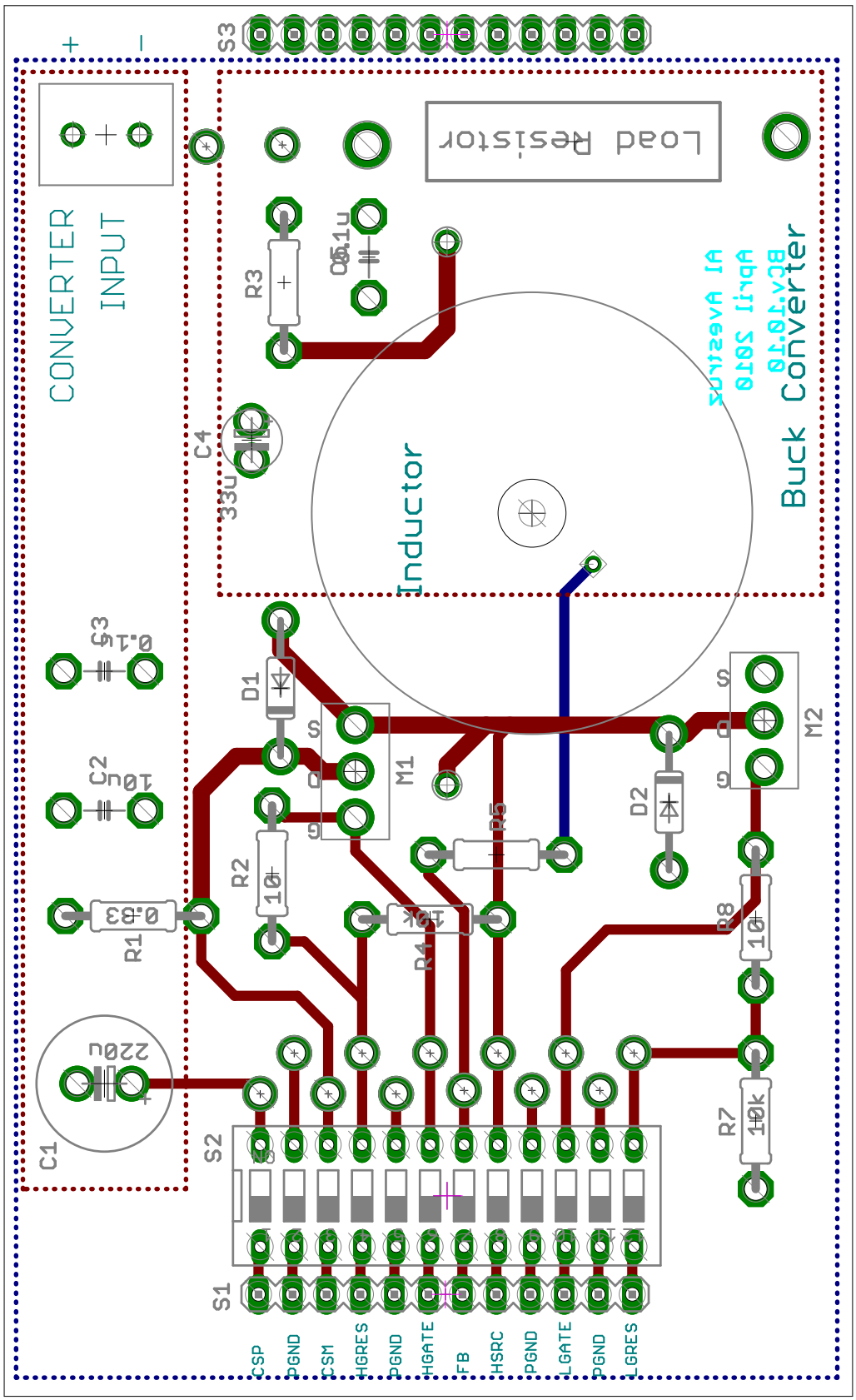
A.7 Gate Drive schematic and PCB



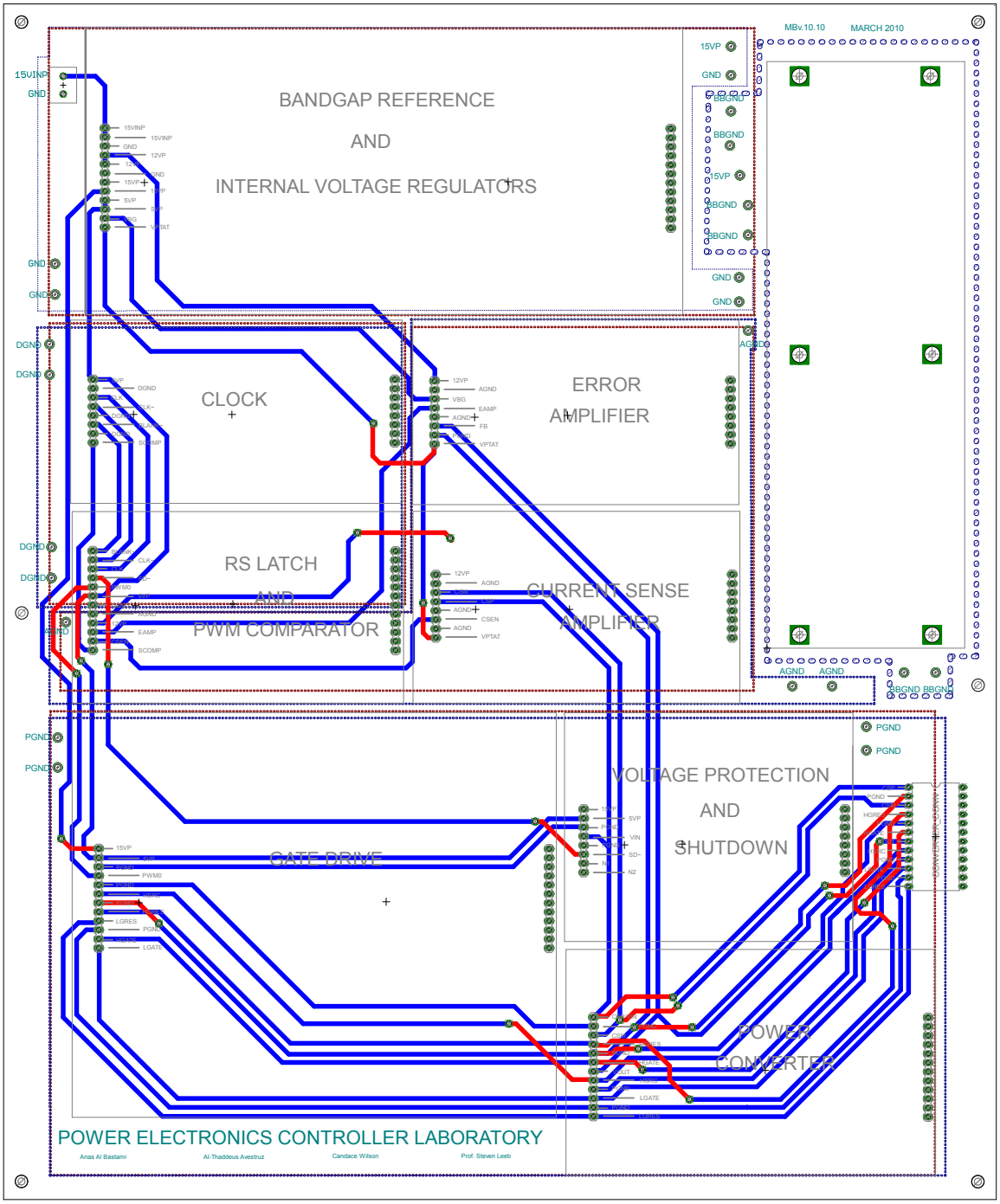

GATE DRIVE BOARD
High Side Driver
Low Side Driver
Bootstrap Supply TP
High Side Enable
Low Side Enable
5V Bypass
Supply Bypass
PGND
HSEN
HGRES
LGRES
HSRC
HFETON
HFETUP
LFETON
LFETUP
HDRVB
~HDRVB
LDRVB
~LDRVB
HDRV
LDRV
PWM
~PWM
~LSEN
SD
VBUP
VUP
PGND
PWM
HSRC
HGRES
LGRES
HGATE
LGATE

A.8 Buck power stage schematic and PCB




CONVERTER
INPUT
+
-
S3
Load Resistor
Inductor
Buck converter
Ayesha Iqra
April 2010
BCA-10.10
C4
33u
R3
0.1u
D1
D2
M1
M2
R1
0.83
R2
10
R4
10k
R5
R7
10k
R8
10
C1
220u
C2
10u
C3
0.1u
S1
S2
CSP
PGND
CSM
HGRES
PGND
HGATE
FB
HSRC
PGND
LGATE
PGND
LGRES

A.9 Motherboard PCB



Bibliography

[1] A. D'Souza *et al.*, "A fully integrated power-management solution for a 65nm CMOS cellular handset chip," in *2011 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2011, pp. 382–384.

[2] R. Rajsuman, "Iddq testing for CMOS VLSI," *Proceedings of the IEEE*, vol. 88, no. 4, pp. 544–568, 2000.

[3] A. Grebene, *Bipolar and MOS Analog Integrated Circuit Design.* John Wiley & Sons, 1984.

[4] A. Avestruz, C. Wilson, R. Cox, S. Campbell, and S. Leeb, "A hands-on approach to advanced undergraduate instruction in control and circuitry in power electronics." in *Proc. IEEE Power Electronics Education Workshop*, June 2007.

[5] (2007) Current mode PWM controller. Texas Instruments. [Online]. Available: http://www.ti.com/lit/ds/symlink/uc3842.pdf

[6] G. Hart, "Nonintrusive appliance load monitoring," *Proceedings of the IEEE*, vol. 80, no. 12, pp. 1870–1891, 1992.

[7] S. Shaw, S. Leeb, L. Norford, and R. Cox, "Nonintrusive load monitoring and diagnostics in power systems," *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 7, pp. 1445–1454, 2008.

[8] S. Shaw, C. Abler, R. Lepard, D. Luo, S. Leeb, and L. Norford, "Instrumentation for high performance nonintrusive electrical load monitoring," *ASME J. Solar Energy Eng.*, vol. 120, no. 3, pp. 224–229, 1998.

[9] S. Leeb, S. Shaw, and J. Kirtley Jr., "Transient event detection in spectral envelope estimates for nonintrusive load monitoring," *IEEE Transactions on Power Delivery*, vol. 10, no. 3, pp. 1200–1210, 1995.

[10] S. Yellampalli and A. Srivastava, "A comparator-based IDDQ testing of CMOS analog and mixed-signal integrated circuits," in *48th Midwest Symposium on Circuits and Systems*, 2005, pp. 179–182 Vol. 1.

[11] A. Miller, "Iddq testing in deep submicron integrated circuits," in *Proc. of the International Test Conference*, 1999, pp. 724–729.

[12] S. Maltabas, O. Ekekon, K. Kulovic, A. Meixner, and M. Margala, "An iddq bist approach to characterize phase-locked loop parameters," in *2013 IEEE 31st VLSI Test Symposium (VTS)*, April 2013, pp. 1–6.

[13] A. Srivastava and R. Soundararajan, "Testing of trusted cmos data converters," in *2012 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Aug 2012, pp. 350–355.

[14] C.-W. Lin, M.-T. Chao, and C.-C. Hsu, "Novel circuit-level model for gate oxide short and its testing method in srams," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 6, pp. 1294–1307, June 2014.

[15] S. Rahimipour, W. Flayyih, I. El-Azhary, S. Shafie, and F. Rokhani, "A survey of on-chip monitors," in *IEEE International Conference on Circuits and Systems (ICCAS)*, 2012, pp. 243–248.

[16] N. Pavlidou, A. Vinck, J. Yazdani, and B. Honary, "Power line communications: state of the art and future trends," *IEEE Communications Magazine*, vol. 41, no. 4, pp. 34–40, 2003.

[17] F.-N. Pavlidou, H. A. Latchman, A. J. H. Vinck, and R. E. Newman, "Powerline communications and applications," *International Journal of Communication Systems*, vol. 16, no. 5, pp. 357–361, 2003. [Online]. Available: http://dx.doi.org/10.1002/dac.594

[18] T. Esmailian, F. R. Kschischang, and P. Glenn Gulak, "In-building power lines as high-speed communication channels: channel characterization and a test channel ensemble," *International Journal of Communication Systems*, vol. 16, no. 5, pp. 381–400, 2003. [Online]. Available: http://dx.doi.org/10.1002/dac.596

[19] E. Biglieri, "Coding and modulation for a horrible channel," *IEEE Communications Magazine*, vol. 41, no. 5, pp. 92–98, 2003.

[20] C. Wilson, "Development of a laboratory course in power electronic control circuitry based on a PWM buck controller," Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, 2006.

[21] A. Viterbi, *CDMA : Principles of Spread Spectrum Communication.* Addison-Wesley Publishing Company, 1995.

[22] L. Welch, "Lower bounds on the maximum cross correlation of signals," *IEEE Transactions on Information Theory*, vol. 20, no. 3, pp. 397–399, May 1974.

[23] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, 3rd ed. Pearson, 2010.

[24] R. Gold, "Optimal binary sequences for spread spectrum multiplexing," *IEEE Transactions on Information Theory*, vol. 13, no. 4, pp. 619–621, October 1967.

[25] ——, "Maximal recursive sequences with 3-valued recursive cross-correlation functions," *IEEE Transactions on Information Theory*, vol. 14, no. 1, pp. 154–156, Jan 1968.

[26] J. Kassakian, M. Schlecht, and G. Verghese, *Principles of Power Electronics*. Prentice Hall, 1991.

[27] A. Al Bastami, A.-T. Avestruz, and S. B. Leeb, "Teaching modeling, control, and simulation in a modular kit for power electronics," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2014, pp. 1–10.

[28] E. Ortiz-Rivera and M. Castro-Sitiriche, "Work in progress - integration of hands-on-laboratory experience of power electronics and renewable energy applications," in *39th IEEE Frontiers in Education Conference*, Oct 2009, pp. 1–2.

[29] O. Lucía, J. Burdío, D. Navarro, and J. Acero, "Educational reconfigurable platform for courses on power electronics," in *4th IEEE International Conference on E-Learning in Industrial Electronics (ICELIE)*, Nov 2010, pp. 19–23.

[30] A. Bousbaine and M. Eljarh, "A practical project approach for teaching experimental power electronics," in *46th International Universities' Power Engineering Conference (UPEC)*, Sept 2011, pp. 1–6.

[31] J. Hudgins, A. Monti, and R. Dougal, "Control system laboratory: a power electronics teaching experience," in *Proc. IEEE Workshop on Computers in Power Electronics*, June 2002, pp. 112–116.

[32] D. Perez, J. Balcells, M. Lamich, N. Berbel, J. Zaragoza, and J. Mon, "Training kit for power electronics teaching," in *34th Annual Conference of IEEE Industrial Electronics*, Nov 2008, pp. 3541–3545.

[33] N. Mohan, W. Robbins, P. Imbertson, T. Undeland, R. Panaitescu, A. Jain, P. Jose, and T. Begalke, "Restructuring of first courses in power electronics and electric drives that integrates digital control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 429–437, Jan 2003.

[34] F. Batista, C. Petry, E. Santos, and B. Almeida, "Didactic system for digital control of power electronics applications," in *Brazilian Power Electronics Conference*, Sept 2009, pp. 1093–1098.

[35] J. Roberge, *Operational Amplifiers: Theory and Practice*. John Wiley & Sons, 1975.

[36] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. John Wiley & Sons, 2002.