Contact-Type Mechanical Interfaces for High Speed Digital Interconnects

by

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ABSTRACT

The objective of this work was to determine the feasibility of Ball Grid Array (BGA) planarization and to investigate the effects of mechanical contacts on signal integrity for high-speed digital signals. As devices become smaller and clock frequencies increase, new technologies for contacting devices are being developed, especially in the field of semiconductor test. These contactors will be incorporated into a socket or an interconnect used in testing devices or printed circuit boards.

The heights of the solder ball leads on BGA packages have a high degree of co-planarity. As BGA pitches become tighter, the requirement for improved co-planarity persists. This thesis shows that through diamond turning techniques, the co-planarity of the solder ball leads can be improved. Planarization of solder balls enables the use and development of rigid interconnects. Interconnections generally have a built in compliance to them to accommodate for co-planarity. Reducing co-planarity eliminates the need for compliant interconnects. Contact mechanics identifies the conical shaped tip as the optimal tip shape, providing the best mechanical connection. The intent of the tip shape investigation is to correlate indentation theory with signal integrity.

The electrical performance of the contactor tip is evaluated using the industry standard pogo pin. Mechanical parameters are varied to observe the effect on the signal integrity. At high frequencies, the interconnect provides a vulnerable location for signal losses to occur. A new interconnect design to address the electrical performance of existing designs is introduced. The cantilevered interconnect consists of a coplanar waveguide cross-section. The interconnect is both mechanically and electrically sound.

This thesis presents aspects of mechanical contact interfaces for electrical signal testing purposes. It focuses on device interfacing, contactor tip shape, signal integrity and new interconnect designs.
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Chapter 1

Introduction

Many issues in the world of semiconductor testing have driven the industry to look at how to interconnect with devices under test (DUT) and interface boards more effectively. The main issue is one of size for the devices, especially Ball Grid Array devices, shown in Figure 1.1. Ball Grid Array devices, commonly known as BGA, allow designers to pack more input/output contacts into a smaller area by occupying the backside of a device with the contacts. They are placed on the planar face of the device as opposed to the periphery, thus enabling the devices to become smaller. Therefore, BGA devices are becoming increasingly popular.

![Ball Grid Array Device](image)

**Figure 1.1: Ball Grid Array Device**

The Input/Outputs of the BGA device are solder balls. In final assembly, these balls mate with a solder pattern on a printed circuit (PC) board and are reflowed through an oven to secure the electrical connection. As the semiconductor industry attempts to make products smaller and more efficient, so too is the size of the devices decreasing. The standard spacing for BGA devices is a 1.27" pitch. However, Tessera has recently developed a newer BGA device with a pitch of .50" called the μBGA™. These devices are also known as fine-pitch BGA packages.
The testing industry generally develops test sockets to contact devices under test, however designing and manufacturing a socket and contactors for the $\mu$BGA$^{\text{TM}}$ proved to be challenging. The challenge is primarily due to the fact that the variation in solder ball heights of the devices becomes more difficult to contact as the spacing of the solder balls decrease. All semiconductor devices are tested 100% to ensure the highest standards of reliability and quality are upheld. The contactors are used to create a temporal, high-integrity electrical contact with the fine pitch BGA devices. Planarizing BGA and $\mu$BGA$^{\text{TM}}$ devices could greatly simplify the world of testing. The advantage of planarization is that it minimizes the variation in height of the solder balls, reducing the problems in the testing phase and perhaps in the assembly phase as well. It also opens the door to designing simpler contactors to improve the electrical performance at test. Because the top of the solder balls lie in the same plane after the planarization, contactors in the test sockets do not need to have as much compliance as before. The compliance in contactors such as pogo pins and other spring loaded contactors is mainly to account for co-planarity in the device I/O’s. The first phase of this project is a study that measures BGA and $\mu$BGA$^{\text{TM}}$ height variation before and after planarization. It is also an investigation to determine if planarization is feasible. This work is described in Chapters 2-5.

The second phase will investigate contactor tip design, interconnect designs and the electrical signal integrity of these designs. Planarization of the devices allows for rigid interconnects to be used as test probes. In addition, the contactor tip shape becomes important because this is the critical transition area for the signal to travel from one medium to another. When contacting the solder ball leads of the BGA or $\mu$BGA$^{\text{TM}}$ devices, a contactor tip will plastically deform the solder. Because solder is such a ductile material, it almost immediately undergoes plastic deformation. Both the spherical and conical tip shapes are considered as the contactor tips. It is suggested that perhaps a greater indentation into the surface may improve the signal integrity of the interconnection and provide a much more reliable contact. In addition, the optimal tip shape will be identified. Hertzian contact and elastic-plastic indentation mechanics assist in identifying the relationship between applied force at the tip and indentation depth. The study on contactor tip shapes is discussed in Chapter 6.
The next phase discusses the signal integrity of electrical contacts. The signal integrity investigation was performed on pogo pins which is a type of interconnect commonly used in the semiconductor industry. Although pogo pins were the means of contact, various tip shapes were used at the end of the pogo pin including the conical and spherical tip shapes. Mechanical parameters such as location on the launch, pogo compression and tip shape of the pogo pins were varied to determine the effect on signal integrity. These tests were all done at high clock frequencies. This discussion can be found in Chapter 7.

The final phase of the project is to propose a possible interconnect design utilizing the indentation theory and the knowledge gained from the signal integrity section. The interconnect design includes the possible use of rigid contactor tips as test probes for the devices. A primary goal of the interconnect design is to design one with minimal contact force requirements. The interconnect must be impedance matched to the printed circuit board or the interface board to which it is mating. This will allow for maximum energy transfer through the interconnection and improve the electrical performance. The newly designed interconnect is a cantilever beam that has a coplanar waveguide geometry. This work is presented in the final chapter.
Chapter 2

Planarization of BGA and $\mu$BGA™ devices

An initial study of the solder ball height variations has been done on the present BGA device. Twelve devices were measured. Two completely different measurement techniques were used to measure the heights; the raster and continuous trace methods. Due to potential tilt in the measurement, the heights were normalized. Normalizing the values allows for comparison between the results of the two methods of measurement; the raster and the continuous trace methods. The main purpose of two measurement methods was to qualify the raster method because it is more feasible and simple. The raster method was qualified and was then used through the remainder of the study. The deviation in heights prior to planarizing them was in the range of 0.0012 to 0.0022 inches.

The investigation was performed in conjunction with Polaroid Corporation’s Optical Engineering Division. They have the specialized diamond turning machine and the measurement equipment used to planarize and measure the heights of the solder balls.

2.1 Statistical Analysis

One of the initial steps preempting the planarization investigation was a statistical analysis on the solder ball height variation. Twelve $\mu$BGA™ memory chips were given to the Optical Engineering Division of the Polaroid Corporation to be measure for height. Each chip had a 5x8 array of solder balls uniformly spaced as shown in the Figure 2.1.
Figure 2.1: Ball Grid Array Chip

With a fine pitch of 0.03” (0.76 mm), this chip can be categorized as a μBGA™. The first task was to determine the height variation of each of the solder balls. Two height measurement methods were investigated; continuous trace and raster. The machine used to make these measurements was a three-axis profilometer. This machine has proven 1 ppm accuracy.

2.2 Continuous Trace Method

The first method was a scanning method in which the measurement probe of 0.5mm diameter was aligned with the x-axis, and was setup to traverse along it. The origin is located at the lower right hand corner of the array as shown in Figure 2.2. The probe was lowered to the substrate at the right hand side of the array at y=0.00” and made to traverse in the negative x-direction. Height measurements were recorded every 0.002” (0.051 mm) across the x-axis. This produced 201 data points per row. After scanning the first row, the probe returned to the right side of the array and indexed up by one row (now at the y=0.03”). It then traveled along the second row, recording data in the same manner. In this way, height data for all of the rows were recorded. Next, the maximum height in an approximate 0.03” interval was determined for each ball, yielding 40 ball heights per chip.

Figure 2.2: Continuous Trace Axes Orientation
2.3 Raster Method

The second method of measurement was noted as the raster method. The raster method is more of an indexing type measurement. The probe of 1mm diameter begins at the origin on the axis defined in Figure 2.3, and is programmed to index along the positive x-axis in 0.03” increments. At each 0.03” increment, the probe records the height of the solder ball at that point. The probe applies approximately 0.8 grams of pressure at contact. At the last ball in the first row, the probe then indexes up one row and returns back in the negative x-direction taking measurements at every solder ball. After all the measurements are recorded, there will be 40 height data points per chip for this particular 5x8 configuration. This method proved to be less time consuming than the continuous trace method.

![Figure 2.3: Raster Method Axes Orientation](image)

In the first trial, there were twelve chips in total, however all twelve were not measured using both methods. Only chips 1 and 10-12 were measured using the continuous trace method, whereas all the twelve were measured using the raster method. This was done in order to compare and qualify the two methods. The raster method was ultimately chosen because it was less labor intensive and time consuming.

2.4 Measurement Error

A valid concern with measuring using either of these methods is the possibility of a horizontal offset error. That is to say that if the bottom center of the probe does not meet the top center of the solder ball, it will result in an error in the height measurement as shown in Figure 2.4.
\[
\delta = (r_1 + r_2) - \sqrt{(r_1 + r_2)^2 - \Delta^2}
\] (2.1)

where \( r_1 = 0.5 \text{mm} \) for the raster probe
\( r_1 = 0.25 \text{mm} \) for the continuous trace probe
\( r_2 = 0.762 \text{mm} \) for the solder ball (approximation)

\[
\frac{\partial \delta}{\partial \Delta} = -\frac{\Delta}{\sqrt{(r_1 + r_2)^2 - \Delta^2}}
\] (2.2)

The radius of the probes for the two different measuring methods, continuous trace and raster, are 0.25mm and 0.50mm respectively. The radius of the solder ball was taken to be 0.125mm. Using equations 2.1 and 2.2, the relative vertical error as well as the sensitivity to that error was plotted for each method as shown in Figure 2.5 and Figure 2.6.
Figure 2.5: Horizontal Offset Error for both methods

Figure 2.6: Sensitivity of Vertical Offset with respect to the Horizontal Offset
The results of these graphs indicate that a horizontal offset will definitely result in a vertical offset, however the effect is not extremely significant. The raster method is less sensitive to vertical error than the continuous trace method because it has a probe diameter double in size. This larger probe diameter minimizes the relative vertical height error seen between the two contacting points. The saving grace of the continuous trace method is the relatively small step size of 0.002” by which it indexes; therefore it will not have a horizontal offset greater than 0.002”. As a result, the vertical offset error is reduced to 0.00016”. It is well noted that each method has its advantages as well as disadvantages.

2.5 Measurement Comparison Study

After measuring all twelve chips using the raster method and chips 1, 10 – 12 using the continuous trace method, a comparison between the two methods was done. However, prior to comparing the data directly, a few key issues needed to be addressed. When measuring at this kind of accuracy, there is a certain degree of tilt that can be a factor in the absolute height of the solder balls. Therefore, this tilt must be accounted for and normalized by subtracting the best-fit plane through the measured heights from the actual measured heights. Figure 2.7 shows the tilt of the chip. The main reason for this is probably the relative flatness of the back of the chip, and how it is mounted to the fixture.

![Graph showing raw height data using the raster method.](image)

**Figure 2.7: Raw Height Data using the Raster Method**

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The best-fit plane through these points can be found by using linear regression analysis in three dimensions. The error is given by

\[ e = b - Ax \]  \hspace{1cm} (2.3)

where \( b \) = the actual values which the plane passes through
\( A \) = a matrix of coefficients describing the plane
\( x \) = the unknown values which are the “best fit” in the plane
\( e \) = the error difference between the actual and calculate values

The best plane is that which makes \( e \) as small as possible. To minimize \( e \) is to minimize

\[ \|Ax-b\|^2 = (Ax-b)^T(Ax-b) \]  \hspace{1cm} (2.4)

The vector that minimizes \( \|Ax-b\|^2 \) is given by the least squares solution to \( Ax=b \):

\[ x = (A^TA)^{-1}A^tb \]  \hspace{1cm} (2.5)

The least square solution outputs 3 values which are used as coefficients \( A, B \) and \( C \) in Equation 2.5.

\[ z = A + Bx + Cy \]  \hspace{1cm} (2.6)

In this way, the best-fit plane through each array of heights was calculated. The difference between those actual values and the “best-fit” heights was taken as the error.

\[ z_{\text{norm}} = (z_{\text{raw}} - z_{\text{fit}}) \]  \hspace{1cm} (2.7)

Because some of the differences were negative and others were positive, the values were normalized by subtracting the most negative number from each of them. This simply shifts the x-axis down through the most negative point, and results in a true representation of the height deviations amongst the solder balls in each array. The least squares method can be used to fit to functions other than the equation of a plane. The matrix \( A \) changes depending on how many unknown coefficients exist.
Table 2.1: Unmached Data for Both Measurement Methods

Table 2.1 shows that after the numbers are normalized, the two methods compare quite nicely. The most interesting value to notice is the peak to valley number. These show the values by which the heights deviate from one another. With the raster method, the maximum peak to valley value is 0.001193” (30.3 μm) while the maximum peak to valley value for the continuous trace method is 0.001515” (38.5 μm). Although these values are not identical, they do compare relatively well. The other two chips that were measured using both methods compare quite well also as shown in Table 2.2.

Table 2.2: Comparison of Maximum Peak to Valley for Both Methods

Finally, this qualifies the raster method for further use. This is a desirable outcome because the raster method is less time consuming and less complex than the continuous trace method.

2.6 Conclusions

This chapter explores the testing and measuring of the solder ball heights of BGA and μBGA™ devices. It also offers a method of interpreting the data from the different measurements so that all the data is comparable. Both the continuous trace and raster methods of measurement were
attempted on the devices. Through a small study, it was found that the raster method is a sufficient and simple way to measure the heights of the solder balls. In order to characterize the heights of all the balls with one equation, the least squares method was employed. This mathematical linear regression analysis delivered an equation of a plane that best fit the heights of the balls. The difference between the actual heights and the best-fit heights has become known as the peak to valley or co-planarity value for the device. The range of co-planarity values for the unmachined devices measured were .00119 - .00181 inches (30.25 - 45.97 μm). The next chapters will focus on the planarization and its feasibility.
Chapter 3

Machining

After taking the initial solder ball height measurements, the BGA and µBGA™ devices were then planarized. The tops of the balls were all machined down into a flat plane parallel to the back of the chip. After measuring the heights of the solder balls on each chip, compliance in the substrate of the chip was noticed. The technician expressed some hesitation in doing this because he felt that the compliance of the substrate would cause some of the solder balls to tear off, therefore adversely effecting the machining process. Machining them was nevertheless attempted, and proved to be successful. Approximately a quarter of the nominal chip height was removed. Two different tools were attempted for machining. For comparison with surface roughness, both diamond machining and CNC turning were attempted. Eight of the twelve chips were machined with a carbide tool on a lathe, while the remaining three were diamond turned on a diamond turning machine.

3.1 CNC Machining

The chips were mounted onto a fixture using double-sided adhesive. At all times the chips were assumed to be functional therefore, grounding straps were used when handling the chips to ensure that no static charge could affect the chip. A ground wire was also connected from the spindle to a known ground. The tool traversed laterally while the fixture was spinning, and the tool began to remove material in passes. The depth of cut per pass was 0.0005”, and the operation took 4 passes to complete removing about 0.002” in total. As expected, machining with a carbide tool produced a rougher surface than diamond machining.
Figure 3.1: Surface of Solder Balls after Turning with a Carbide Tool (50X)

Tooling marks were very noticeable in Figure 3.1 because of the carbide tool used. Because of the particular roughness, it was possible that slight corrosion would occur and an oxide layer would form on top each ball. The next step in the investigation was to take a cross-section of the solder ball and look at the oxide layer more carefully. A question of particular importance is one such as: What minimum contacting force is necessary to break through this oxide layer, and if that oxide layer can be overcome, will the roughness of the surface be an advantage in terms of electrical performance at testing?

3.2 Diamond Machining

Diamond machining the solder balls was the original intent because of the excellent surface finish and the attainable precision associated with diamond turning. The diamond turning machine used was a 5-nanometer resolution with excellent precision. Similar to the previous machining process, these chips were mounted to a fixture with double-sided adhesive and all machined at the same time. It was a dry cutting process and it exhibited no sticking to the tool. The feed rate was 0.040 inch/sec and the depth of cut was again 0.0002”. The radius of the diamond tool used was 0.030”. Unlike the other machining process, the resulting surface roughness using diamond machining is smooth and produces an almost mirror-like surface as shown in Figure 3.2 and Figure 3.3.
When comparing Figure 3.1 and Figure 3.3 it can be seen that the diamond machining produced a much smoother surface finish than the turning operation. Figure 3.2 shows the entire BGA after it had been machined. It is worth noting that the technician noticed that a small oxide layer had formed on the diamond-machined surface as well after several days. It was looked at under a microscope just after machining and there was no noticeable oxide layer, however after a few days, the solder balls were reexamined and an oxide layer had formed. Once again, cross-section of the diamond turned solder ball must be examined, and then the oxide layer can be better understood. Of particular interests the possible further investigation of the oxide layer thickness.
Chapter 4

Re-Measurement

Following the planarization of the BGA and μBGA™ devices, the heights of the solder balls were re-measured using the qualified raster method. The procedure was identical to the one described in Chapter 2, where the probe was indexed 0.03” through the array, recording the height at every solder ball. Planarization using the diamond turning machine decreased the variability in the height by one order of magnitude, as expected. Figure 4.1 shows the small variation in height, and the tilt of the planarized surface.

Figure 4.1: Surface Flatness and Tilt after Diamond Machining
4.1 Diamond Turning Versus Traditional Turning with Carbide Tool

Because both diamond turning and traditional turning using a CNC lathe were attempted, the resultant height measurements of the two machining types were compiled and compared. Table 4.1 and Table 4.2 show the maximum peak to valley data for the two types.

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>raw</th>
<th>fit</th>
<th>(raw-fit)</th>
<th>Peak to Valley</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>0.00</td>
<td>-0.000006</td>
<td>0.00E+00</td>
<td>-6.00E-06</td>
<td>-6.00E-06</td>
</tr>
<tr>
<td>0.03</td>
<td>0.00</td>
<td>0.000001</td>
<td>0.00E+00</td>
<td>1.00E-06</td>
<td>1.00E-06</td>
</tr>
<tr>
<td>0.06</td>
<td>0.00</td>
<td>-0.000016</td>
<td>0.00E+00</td>
<td>-1.60E-05</td>
<td>-1.60E-05</td>
</tr>
<tr>
<td>0.09</td>
<td>0.00</td>
<td>0.000013</td>
<td>0.00E+00</td>
<td>1.30E-05</td>
<td>1.30E-05</td>
</tr>
<tr>
<td>0.12</td>
<td>0.00</td>
<td>0.000005</td>
<td>0.00E+00</td>
<td>5.00E-06</td>
<td>5.00E-06</td>
</tr>
<tr>
<td>0.15</td>
<td>0.00</td>
<td>-0.000019</td>
<td>0.00E+00</td>
<td>-1.90E-05</td>
<td>-1.90E-05</td>
</tr>
<tr>
<td>0.18</td>
<td>0.00</td>
<td>-0.000017</td>
<td>0.00E+00</td>
<td>-1.70E-05</td>
<td>-1.70E-05</td>
</tr>
<tr>
<td>0.21</td>
<td>0.00</td>
<td>0.000009</td>
<td>0.00E+00</td>
<td>9.00E-06</td>
<td>9.00E-06</td>
</tr>
<tr>
<td></td>
<td>0.12</td>
<td>-0.000313</td>
<td>-0.000248</td>
<td>-0.000065</td>
<td>7E-06</td>
</tr>
</tbody>
</table>

Note: All Values are in Inches

Max 0.000188

Table 4.1: Post-Machining (CNC Lathe) Data for Chip 9

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>raw</th>
<th>fit</th>
<th>(raw-fit)</th>
<th>Peak to Valley</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0.000028</td>
<td>0.0001</td>
<td>-7.2E-05</td>
<td>0</td>
</tr>
<tr>
<td>0.03</td>
<td>0</td>
<td>-3.4E-05</td>
<td>0.000016</td>
<td>-0.00005</td>
<td>0.000022</td>
</tr>
<tr>
<td>0.06</td>
<td>0</td>
<td>-0.0001</td>
<td>-6.8E-05</td>
<td>-3.6E-05</td>
<td>0.000036</td>
</tr>
<tr>
<td>0.09</td>
<td>0</td>
<td>-0.00018</td>
<td>-0.00015</td>
<td>-2.8E-05</td>
<td>0.000044</td>
</tr>
<tr>
<td>0.12</td>
<td>0</td>
<td>-0.00026</td>
<td>-0.00024</td>
<td>-2.3E-05</td>
<td>0.000049</td>
</tr>
<tr>
<td>0.15</td>
<td>0</td>
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<td>-0.00032</td>
<td>2E-06</td>
<td>0.000074</td>
</tr>
<tr>
<td>0.18</td>
<td>0</td>
<td>-0.00042</td>
<td>-0.0004</td>
<td>-1.3E-05</td>
<td>0.000059</td>
</tr>
<tr>
<td></td>
<td>0.12</td>
<td>-0.00031</td>
<td>-0.00025</td>
<td>-6.5E-05</td>
<td>7E-06</td>
</tr>
</tbody>
</table>

Note: All Values are in Inches

Max 0.000074

Table 4.2: Post Machining (Diamond Turning) Data for Chip 10

The maximum peak to valley (max PV) is significantly smaller in this case at 0.000074” than the max PV of the solder balls at 0.000188” using the CNC lathe tool. The diamond turning produced variations that were less than half of the variation seen in the CNC turning machine. This is definitely the expected result because diamond turning is a more precise technique. The comparison measurements can be seen in Table 4.3.
<table>
<thead>
<tr>
<th>Chip Number</th>
<th>Carbide Tool</th>
<th>Diamond Tool</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.000224</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0.000147</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0.000239</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.000161</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0.000198</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>0.000145</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.000188</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>N/A</td>
<td>0.000074</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>0.000138</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>0.000106</td>
</tr>
</tbody>
</table>

Table 4.3: Maximum Peak to Valley of Normalized Heights After Diamond and Carbide Tooling

4.2 Surface Roughness

In addition to measuring the heights of the planarized surfaces, a surface roughness trace was measured on an individual solder ball on the array for both the CNC lathed and the diamond turned chips. A ball profile was also obtained by the surface profilometer. This instrument is a Tencor® Profilometer that uses a stylus of 2μm radius as the measurement tool. The stylus was dragged across the surface of the planarized solder ball at a specified starting point and a specified distance of travel.

![Figure 4.2: Tencor Trace of CNC-Turned Surface](image_url)
Figure 4.3: Tencor Trace of Diamond-Turned Surface

Figure 4.3 and Figure 4.4 show a surface profile of a single solder ball surface. As expected, the CNC-turned surface has a larger variation in height than the diamond turned surface. The height deviation for the CNC-turned surface was ± 0.4 μm whereas the diamond turned deviation was only about ± 0.15 μm. Again, this is due to the precision of the diamond turning machine. Figure 4.4 and Figure 4.5 show the profile of three consecutive solder balls from the CNC Lathe and the diamond turning machine, respectively. These traces give a good estimate of the solder ball heights, and how much material was removed from the original surface.

Figure 4.4: Solder Ball Profile After Planarization with CNC Lathe
Figure 4.5: Solder Ball Profile After Planarization with Diamond Turning Machine

Figure 4.6 shows an actual image of a cross-sectioned single solder ball from the diamond turned chip. Assuming the solder ball is completely spherical, the height removal is approximately 85 μm or 33.35 mils. This is about 35% of the original height.

Figure 4.6: Cross-Sectioned View of a Single Diamond-Turned Solder Ball

The next phase of the investigation was a case study for Rambus, a major producer of high speed memory devices using the μBGA™. Rambus was interested in the prospect of planarizing the μBGA™ devices because co-planarity was a major issue for testing.
The raster measurement method was used to obtain deviations in the solder ball heights. The resulting height deviations were in the range of 0.000145-0.000224 inches (3.68-5.69 μm) for the rougher cut machining, and 0.000074 – 0.000138 inches (1.88-3.51 μm) for the diamond turning. In addition, the diamond turned surface roughness was an order of magnitude better. Therefore, it was seen that the diamond turning produced a more planar surface than the CNC lathing technique. To date, the study has supported the hypothesis that planarizing the BGA and μBGA™ chips can minimize the deflection of a contactor while improving the electrical performance during testing of the chip.
Chapter 5

Rambus Case Study

The objective of this investigation for Rambus was to determine the feasibility of planarizing BGA and μBGA™ using a diamond turning machine. The initial study explained in Chapter 3 was done to see if the prospect of planarization was possible. The initial study also compared two machining options: Carbide-Tooled Lathe or the Diamond Turning Machine. This investigation further explores the option of planarization with the diamond turning machine as a case study for Rambus. In conjunction with this investigation, machining parameters were also tweaked to get the best looking cut and surface finish possible, therefore providing more depth into the results. Five BGA devices and 11 μBGA™ devices were planarized using only the diamond turning machine.

5.1 Cutting Process

The first few BGAs were used to set-up the procedure and converge on machine parameters such as feed rate, depth of cut and spindle speed. The first chip was initially machined with a feed rate of 0.0025"/sec, depth of cut of 0.002", and a spindle speed of 1200rpm. After the first pass, the surface finish of the cut was inspected under the microscope and was found to have visible cutting lines. In previous trials, the surface finish from diamond machining was very smooth producing mirror-like surfaces. Because of the poor surface finish, the feed rate was decreased to 0.001"/sec, depth of cut was decreased to 0.0005", and the spindle speed was increased to 1450rpm. The diamond tool radius at this point was 0.059". The surface finish was inspected again for improvement, however it appeared to be the same as before. In order to alleviate the surface finish problem, the operator changed the diamond tool to one of a smaller radius of 0.020" to cut the remaining samples. Table 5.1 describes the number of passes, the feed rate, the depth of cut and the spindle speed for each. Diamond turning was preferred because it creates
varied velocities across the chip. This enables us to determine the best velocity so we can set the diamond turning machine to that speed.

<table>
<thead>
<tr>
<th>Number of Passes</th>
<th>Feed Rate (inch/sec)</th>
<th>Depth of Cut (inches)</th>
<th>Spindle Speed (rpm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip #2</td>
<td>7</td>
<td>0.005</td>
<td>0.001</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.001</td>
<td>0.0005</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.001</td>
<td>0.0002</td>
</tr>
<tr>
<td>Chip #3</td>
<td>7</td>
<td>0.005</td>
<td>0.001</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.001</td>
<td>0.0005</td>
</tr>
<tr>
<td>Chip #4</td>
<td>7</td>
<td>0.005</td>
<td>0.001</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.001</td>
<td>0.0005</td>
</tr>
<tr>
<td>Chip #5</td>
<td>7</td>
<td>0.005</td>
<td>0.001</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.001</td>
<td>0.0005</td>
</tr>
</tbody>
</table>

Table 5.1: Description of Cutting Process for Chips 2-5

Upon inspection, the surface quality of chip 2 was similar to that of chip 1. The solder balls at the center of the chip had much more burring than the solder balls on the periphery. The changes in feed rate and depth of cut must have helped moderately because the surface finish on the periphery of this chip was better than the first one. The reason for such the poor surface finish at the center is the speed at which the solder balls in the center are spinning is less than those balls on the periphery. In production, this clearly indicates that turning at a constant speed is required. Chips 3-5 were machined in a similar fashion with the same radius tool of 0.020". Table 5.1 describes the parameters used to planarize them. The surface finish of these remaining chips resembled chips 1 and 2. However, those chips cut with a higher spindle speed tended to have less burring. After changing various machine parameters in order to improve the surface quality of the planarized solder balls, it was concluded that the solder must be of a softer nature with the possibility of high lead content. Rambus confirmed this hypothesis for the μBGA™ devices, however indicated that the BGAs were made from harder (less lead) solder. The chips were mounted on an aluminum platform and attached using double-sided tape. They were removed
using a small amount of alcohol. During the removal, two of the \( \mu \text{BGAs}^{\text{TM}} \) were broken from the specimen platform. These two chips were not measured for planarity.

### 5.2 Visual Results

The surface finish was of considerable concern after viewing the solder balls under the microscope. Figure 5.1 shows burring and buildup of solder after planarization. Figure 5.2 shows smearing of the solder into 3 different planes. This is the result of machining "soft solder". Planarizing BGAs with soft solder causes buildup on the tool as well as slightly greater ball height variations. In addition to these pictures, a surface profile was done to quantify the actual roughness of the cut. Figure 5.3 shows a surface trace of a single solder ball on the BGA chip.

![Solder Build-up](image)

**Figure 5.1:** Single Solder Ball from a BGA After Planarization – 50X
The trace was done with a Tencor\textsuperscript{\textregistered} surface profilometer. The trace shows a variation of $\pm 1 \ \mu m$ across the surface of a single planarized solder ball. Figure 5.4 shows the surface roughness of a solder ball for a $\mu$BGA\textsuperscript{TM} chip. The variation in height across one solder ball on a BGA ($\pm 1 \ \mu m$) was larger than across the $\mu$BGA\textsuperscript{TM} ($\pm .4 \ \mu m$).
The initial diamond turning trials were done on \(\mu\text{BGA}^\text{TM}\) chips with a 5x8 grid array. As stated earlier, the surface finish was much cleaner and shinier than the chips from this trial. The surface profilometer traces support this observation. The variation for the initially diamond flycut samples was ± .2 \(\mu\text{m}\).

### 5.3 Ball Height Measurement

A raster method was employed to measure the solder ball heights after planarization of the chips. The raster method is an indexing type measurement. The probe of 4mm diameter for the BGAs and 1mm diameter for the \(\mu\text{BGAs}^\text{TM}\) begins at the origin, and is programmed to index along the positive x-axis in 0.03" – 0.035" increments, depending on the pitch. At each increment, the probe takes a measurement. The probe applies approximately 0.8 grams of pressure at contact. At the last ball in the first row, the probe then indexes up one row and returns back in the negative x-direction taking measurements at every solder ball. After all the measurements were recorded, there were 676 data points per chip for the BGAs and 119 data points for the \(\mu\text{BGAs}^\text{TM}\). There were two trials of measurements recorded.
5.3.1 Trial 1 Data

Using the linear regression analysis for a best-fit plane, the ball height variations of the BGAs and μBGAs™ were calculated for trial 1 data. Figure 5.5 shows a graph of the actual height of the balls measured for BGA 3 without the drop-off. "Drop-off" refers to the probe running off the solder balls because the alignment between the chip and the linear probe track was not accurate enough. This problem will be further explained in the "interpretation of data" section. Figure 5.6 shows a graph of the actual height of the balls measured for the first 8 rows of μBGA™ 8.

![Graph of normalized ball height variation for BGA Chip 3]

Figure 5.5: Normalized Ball Height Variation for the BGA Chip 3
Figure 5.6: Ball Height Variation for the First 8 rows of $\mu$BGA™ 3

Figure 5.7: Surface Plot of Normalized Data for the First 8 rows of $\mu$BGA™ 3

The purpose of using the linear regression analysis is to account for the tilt like that shown in Figure 5.6. This tilt can be due to a number of factors including solder buildup on the ball,
substrate compliance, machine alignment, and probe misalignment. The difference between the best-fit plane and the actual values is calculated for each data point. The data is then normalized against the minimum difference within the array resulting in a peak to valley value. The maximum peak to valley value is then found for each array in the case of the BGAs and each of the first 4-8 rows in the case of the µBGAs™. This value has particular importance because it serves as a comparison gauge between the data sets. The maximum peak-to-valley value also serves as the upper limit of deviation from a perfectly planar surface. Figure 5.7 shows the normalized ball height variation for the first 8 rows of the µBGA™ 3 seen in Figure 5.6. Figure 5.8 shows the maximum peak-to-valley values for each of the BGAs. Figure 5.9 shows the maximum peak to valley for the first 4-8 rows of the 10 µBGAs™.

Figure 5.8: Maximum Peak-to-Valley Values for all BGAs
Figure 5.9: Maximum Peak-to-Valley for each $\mu$BGA™ across the First 8 rows of the Chip

5.3.2 Trial 2 Data

Because of the drop-off in data, one more attempt at measuring the heights was done. Subsequently, the problem from the first trial was discovered. It was believed that the pitch on the BGAs and $\mu$BGAs™ was 0.03", however after careful re-measurement, the pitch was found to be 0.0315". The "drop-off" issue was then resolved however a new issue revealed itself. There appeared to be a curvature in the raw data. One modification was made to the testing apparatus. The fixture upon which the chips were measured had been modified with vacuum ports. This ensured that the chips would be held flush against the 90° edge and it minimized any gap between the fixture and the back of the chip. This issue is discussed further in the "interpretation of data" section below. Table 2 shows the type of fit done for each chip measured in trial 2. Figure 5.10 gives an example of the curvature in a $\mu$BGA™. In this case, the best-fit polynomial curve was fit, and the difference between the raw and the fit data was recorded. Figure 5.11 shows the normalized data. Figure 5.12 and Figure 5.13 give the maximum peak-to-valley values for the $\mu$BGAs™ and BGAs respectively.
<table>
<thead>
<tr>
<th>Type of fit</th>
<th>Max Variation (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>μBGA™ 1</td>
<td>1.65</td>
</tr>
<tr>
<td>μBGA™ 2</td>
<td>3.66</td>
</tr>
<tr>
<td>μBGA™ 3</td>
<td>6.65</td>
</tr>
<tr>
<td>μBGA™ 4</td>
<td>3.25</td>
</tr>
<tr>
<td>μBGA™ 5</td>
<td>2.72</td>
</tr>
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<td>μBGA™ 6</td>
<td>2.72</td>
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<td>4.67</td>
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<td>1.90</td>
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<td>μBGA™ 9</td>
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<tr>
<td>BGA3</td>
<td>16.95</td>
</tr>
<tr>
<td>BGA4</td>
<td>16.80</td>
</tr>
</tbody>
</table>

Table 5.2: Maximum Variation and Type of Normalization for Trial 2

Figure 5.10: Ball Height Measurements for μBGA™ 4 – Raw Data
Figure 5.11: Normalized Ball Height Variation for µBGA™ 4

Figure 5.12: Maximum Peak-to-Valley Height Variation of the µBGA™ Devices
Figure 5.13: Maximum Peak-to-Valley Height Variation of the BGA Devices

5.3.3 Interpretation of Data

Figure 5.8 shows the maximum peak-to-valley values for the 5 BGA chips after the drop-off data was removed. Correspondingly, Figure 5.9 show the maximum peak-to-valley values for the 10 μBGA™ chips. Only the first 4-8 rows of the μBGA™ chips were analyzed because an error was discovered after the measurements were complete. The platform upon which the chips were set for measurements was not perfectly aligned with the machine. Therefore the initial rows were measured correctly, however the measurement probe dropped off and onto the substrate for the subsequent rows. This was discovered after looking at the μBGAs™ more closely. Under the microscope, the linear trace along which the measurement was taken was visible on the planarized solder balls. The points at which the trace dropped off to the substrate could also be seen under the microscope. Figure 5.3 shows the linear probe trace on the single solder ball running parallel to the length of the page. Consequently, Figure 5.6 shows the first 8 rows of the 17-row chip whereas Figure 5.7 shows the actual data for the entire chip. It is very apparent that
the data drops off after \(x=0.21\). This is the sole reason that the first 8 rows of each chip were analyzed.

The maximum peak-to-valley values for the BGA chips are much larger than those values for the \(\mu\text{BGAs}^\text{TM}\) rows. These chips were measured with a larger probe to account for any vertical offset, especially considering the high volume of points to be measured. In addition, there was some solder buildup on the probe. This may account for the misleading maximum peak-to-valley values calculated for these 5 BGAs. Initially, the best-fit analysis was done without accounting for the drop-off points where the probe fell off the solder balls. The values did not agree with what was seen in the initial trials, and the surface of the BGAs was investigated. Sure enough, the similar issue with the misalignment of the measurement platform was seen on the BGAs as well. To gain a better understanding of the actual heights, the drop off data was omitted and the analysis was redone. Figure 8 shows the maximum peak-to-valley values without the drop-off data.

Due to the problem of the probe dropping off, the chips were remeasured in trial 2. As earlier mentioned, a new platform with a more accurate 90° ridge for the chip to align itself against was machined. This ensured measurement alignment, and reduced the chances of the probe dropping off. A portion of the raw data from trial 2 indicated a degree of curvature to the measurements. Therefore, instead of fitting a plane to this curved data, a second order polynomial was fit to normalize the data. A speculative reason for the curvature could be the new vacuum fixture that the chips were now tested on. The cause of the curvature is not certain, nonetheless it was removed using the normalization techniques. The remaining data sets were flat but tilted, so a best-fit plane was used for normalization. Figure 5.11 shows the normalized data. There is a distinguishable peak in the Figure 5.11, however it is not considered to be an outlier. The data has been reexamined for an error and it appears to be correct. This is not of large concern because the outlier value is an expected low of 3.25\(\mu\text{m}\).

Figure 5.12 and Figure 5.13 give the actual maximum peak-to-valley values for the \(\mu\text{BGAs}^\text{TM}\) and the BGAs respectively. The \(\mu\text{BGA}^\text{TM}\) values are quite low ranging from 1-7 \(\mu\text{m}\). The BGA values appear to be higher in the 10-17 \(\mu\text{m}\) range. The reason for this disparity has still not been
determined. The same trend was also observed in trial 1 where the range of values was along the same order as trial 2. Nevertheless, the results from both trials give a good sampling of the achievable planarity from diamond turning. In general, various factors have affected the measurement process. Possible factors include the vacuum fixture, and solder buildup on the probe.

In addition to the data taken from the coordinate measuring machine, the same devices were examined using a 3-D non-contact surface metrology system. Only two or three devices were measured, but the result correlate well with the results from the CMM. Figure 5.14 and Figure 5.15

![Surface Statistics and Setup Parameters]

**Surface Statistics:**
- Ra: 33.02 um
- Rq: 48.17 um
- Rz: 228.42 um
- Rt: 253.10 um

**Set-up Parameters:**
- Size: 1158 X 742
- Sampling: 6.36 um

**Processed Options:**
- Terms Removed: Tilt
- Filtering: Low Pass

---

**Figure 5.14: 3-D Surface Plots of a μBGA™ device**
5.4 Conclusions

The Rambus case study was another opportunity, beyond the initial planarization investigation, to examine the feasibility of flattening the tops of the BGA and µBGA™ devices. Although the study produced some unexpected results such as the polynomial curvature of the planarized surface, after some calculations and further investigation, the technique proved to be successful. To recap the Rambus case study, it was found that the µBGA™ devices were planarized within a range of 1-7 µm and the BGA devices within 10-17 µm. Compared to the results of the height measurements prior to planarization, this is nearly an order of magnitude better. A comparison plot can be seen in Figure 5.16.
Figure 5.16: Improvement from Pre to Post - Machining of μBGAs™

This improvement enables more robust interconnects to be built for testing the BGA and μBGA™ devices.
Chapter 6

Testing Socket for BGA with focus on "Tip shape"

The main purpose of planarization is to enable rigid contactors to be used as part of the testing devices. Rigid contactors versus a flexible connector, such as a pogo pin, provide a shorter path length for the signal to travel as well as a more robust mechanism. The robustness improves the cycling and thermal fatigue that the contactor undergoes in the test socket. The rigid contactor also eliminates the need for introducing compliance in the contactor if the surface to be contacted is planarized within a micron range of co-planarity. The following sections explore the geometry of the contactor and how this geometry relates to the indentation the contactor makes into the material. When contacting the solder balls of BGA and μBGA™ devices, the contactor will plastically deform the contacted surface because solder is extremely soft and compliant. On the other hand, when contacting launches on printed circuit boards, the contacted surface is much harder because it is a gold plated nickel surface.

The intent of this tip shape investigation is to correlate indentation theory with signal integrity. These contactors will be incorporated into a socket or an interconnect used in testing devices, or printed circuit boards.

6.1 Hertz Theory

Hertz studied the influence of elastic deformation at the surface of two objects touching, and the stresses between them. He also tried to give a definition of the hardness of a solid in terms of the contact pressure to initial the onset of plastic yielding by two bodies pressed against each other. The assumptions of the Hertz theory are based on the following points:

i. surfaces are continuous and non conforming

ii. strains are small
iii. each solid can be considered as an elastic half space
iv. surfaces are frictionless

These four points become the basis for stating the elasticity problem. This gives rise to the empirical solutions of the hertzian problem of contact stresses for different contactor tip styles.

### 6.2 Closed form solution of indentation calculations for two standard tip shapes

One question that arises when dealing with rigid contactors is what tip shape should be used? Because solder is a relatively soft material, it will most likely undergo permanent deformation when contacted. An empirical study was done to determine the deformation effects of using different tip shapes on the contactor tip. For simplicity, only two tip shapes, round and conical were evaluated empirically. There are trade-offs between the round and conical shaped contactors.

#### 6.2.1 Round Tip Shape

For contacts of two solids of revolution, the maximum stress occurs on the axis of symmetry beneath the surface. Both the von Mises criterion and the Tresca criterion for the onset of yield give the maximum contact pressure between the two surfaces as:

\[ P_o = 1.6Y \quad (6.1) \]

where \( P_o \) is the maximum contact pressure
\( Y \) is the flow stress

The load to initiate yielding is then related to the maximum contact pressure. This equation is given by:

\[ P_Y = \frac{\pi^3 R^2}{6E^*} (P_o)^3 \quad (6.2) \]

where \( R \) is the radius of the contactor
\( E^* \) is the resolved Elastic Modulus
\( P_o \) is the maximum contact pressure

The resolved elastic modulus is given by:
\[ E^* = \left( \frac{1 - \nu_{\text{BeCu}}^2}{E_{\text{BeCu}}} + \frac{1 - \nu_{\text{SnPb}}^2}{E_{\text{SnPb}}} \right)^{-1} \] (6.3)

where \( \nu \) is Poisson’s ratio

\( E_{\text{material}} \) is the Elastic Modulus of the indenter or the indented material. It is denoted by the subscript.

From Equation 7.2 it can be seen that to carry a high load without yielding it is desirable to combine a high yield strength or hardness with a low elastic modulus. This considers the modulus of both the indented material and the indenter. Once the indenter has reached the fully plastic regime, the depth of penetration is given by:

\[ \delta = \left( \frac{9P^2}{16R(E^*)^2} \right)^{\frac{1}{3}} = \frac{a^2}{R} \] (6.4)

where \( P \) is the load applied

\( R \) is the radius of the indenter

\( E^* \) is the resolved elastic modulus

\( a \) is the horizontal distance between the centerline of the indenter and the surface of the indentation as seen in Figure 6.1

**Figure 6.1: Cross-Section of Spherical Indenter**

Figure 6. and Figure 6. are both based on Equation 6.4. Figure 6. shows a plot of the load applied versus the indentation depth for a given indenter radius. This is an empirical result, and the friction between the indenter and the indented material may affect experimental results. Figure 6. is calculated at the elastic-plastic line, where boundary conditions must satisfy both elasticity and plasticity laws. Therefore it represents the Hertzian contact deformations which
are in the elastic regime. On the other hand, Figure 6. is beyond the elastic-plastic limit in a nearly fully plastic regime. It shows the indentation depth versus indenter radii for a given load of 1.36N.

Figure 6.2: Indentation versus Force graph for a given Indenter Radius
Figure 6.3: Indentation Depth versus Radius for a load of 1.36N

Keeping these results in mind, a similar analysis will be done for the conical tip shape.

6.2.2 Conical Tip Shape

Evaluating a conically shaped tip is slightly different than that of the round tip because Hertz contact theory is restricted to smooth, continuous profiles. Those indenters having a sharp edge or corner create an infinite pressure at the apex of the cone or wedge. The danger with the pointed tips is that they are likely to wear more quickly than a smoother, gradual tip shape. Another drawback is that the manufacturing process for these tips is more involved and costly because they require machining and cannot be formed. However, certain surfaces that are contacted are known to oxidize. Although gold does not oxidize as much as solder does, it is still necessary to break through whatever the oxide layer and contaminants may exist on the gold plated surface. The thickness of the oxidation layer is environment dependent, and is affected by temperature and moisture.
6.2.2.1 Elastic to Plastic Regime of the Indentation

There are three distinct stages to the indentation process in the elastic-plastic regime. There is the point when the yield point first exceeds the plastic zone. This zone is small and the plastic strains are of the same magnitude as the surrounding elastic strains. Next, there is a region of elastic-plastic, where the plastic zone is expanding into the elastic zone encompassing it, but also pushing it a little further if strain hardening exists. Finally, there is the regime where the plastic zone has completely dominated the elastic zone and it no longer remains. This process is described well in Figure 6.4. This diagram depicts the elastic-plastic regime.

![Figure 6.4: Conical Tip Shape](image-url)
Assuming that the elastic modulus of the indenter is much greater than that of the indented material it is not necessary to consider the modulus in this analysis. This is because solder, the indented material, is an elastic-perfectly plastic material that will continue to strain beyond its yield stress. Making a general estimation of the stresses occurring at the boundary between the indenter and the surface, the following equation is used:

\[ \sigma = \frac{F}{\pi a^2} \]  

(6.5)

where \( F \) is the applied load
\( a \) is the indentation radius
\( \sigma \) is the yield stress of the material

Prescribing the load and the yield stress of the material, the indentation radius, \( a \) can be calculated. Having calculated the value of \( a \) and prescribing the angle \( \alpha \), equation 6.6 can determine the indentation depth. Through geometry, the indentation depth is defined as:

\[ \delta = \frac{a}{\tan\left(\frac{\alpha}{2}\right)} \]  

(6.6)

Figure 6.5 shows a snapshot of the spreadsheet used to calculate the indentation depth.

<table>
<thead>
<tr>
<th>Applied Load</th>
<th>3.00E-02 lbs</th>
<th>1.36 N</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yield Stress of Solder</td>
<td>10000 psi</td>
<td>68.60 MPa</td>
</tr>
<tr>
<td>Indentation Radius</td>
<td>9.77E-04 inches</td>
<td>24.82 ( \mu )m</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>30 degrees</td>
<td></td>
</tr>
<tr>
<td>( \tan \alpha )</td>
<td>0.58</td>
<td></td>
</tr>
<tr>
<td>Indentation Depth</td>
<td>3.65E-03 inches</td>
<td>92.63 ( \mu )m</td>
</tr>
</tbody>
</table>

Figure 6.5: Parameters for Conical Indenter

Using Equations 6.5 and 6.6, the indentation depth based on a given loading, geometry and material properties can be obtained.
6.3 Conclusions

This chapter focuses mainly on the determination of indentation depth of two different shaped contactor tips for interconnection purposes. Both the spherical and the conical tip shapes were evaluated. Comparing the two tip shapes, at about 1.36N of force, the indentation depth of the conical tip shape is higher than that for the spherical tip shape. The depth for the conical is about 93 μm whereas the spherical is about 2-5 μm depending on the radius size. This result indicates that the conical tip shape would penetrate slightly more into the indented material at the same load. This however, is a very preliminary and empirical result. It does not consider the friction that occurs between the indenter and the indented material. Friction consumes energy that could otherwise be used to indent the material further. Further investigation into the plasticity of this indentation mechanics must be done. The intent of this and the following chapter was to test these contactor tips for signal integrity.
Chapter 7

Signal Integrity

Once the mechanical design of the contacts has been established, the next phase is to examine the electrical testing aspect of the devices. On a very general level, the mechanical reliability and mechanical contact have a significant effect on the signal integrity in electrical testing. This section focuses more on the electrical signal integrity of contacts on gold plated pad for printed circuit boards rather than to the solder on a ball grid array package. However this area within electrical testing is ultra-critical. Unfortunately, the tips could not be tested for signal integrity in the plastic domain, only in the elastic domain.

7.1 Introduction

Degradation of signals at high frequencies is an obstacle faced in the design of future Automated Test Equipment (ATE) systems. Some places that this degradation occurs are at the launch and through the trace on the printed circuit (PC) board. Of most concern in this chapter is the blind mate interconnection between the pogo block and the Device Interface Board (DIB). To generalize further, we can say that we are searching for a better solution to launch high frequency signals perpendicular to the device interface board. Signal speeds are increasing rapidly in electrical applications. As speeds increase, the interconnections become the resultant loss of signal speed capability. The higher the frequency, the more significant a short electrical discontinuity becomes. Therefore, interconnections become a very important part of the system at such high frequencies. In order to improve the quality of a signal as it travels through the pogo block, we must first characterize the existing block that is used in the current test systems. Only after better understanding our current system, can we make the necessary improvements to enhance signal delivery.
7.2 Current Interface Method

A study presented in this report is a step towards characterizing the existing pogo blocks as a baseline. The current brass block has a total of 8 signal pins surrounded by ground pins. The signal pins themselves are specially designed; longer than the manufacturer's stock items. These receptacles themselves are rated for 2/3 travel, which is about .08". The total possible travel is .125" for each pin. Each block mates with the Device Interface Board (DIB) on which there is a 9x2 array of 60mil diameter gold pads. The tip of the pin is shaped to a point to allow for more radial misalignment. The manufacturer also claims that the tips are pointed in order to break through any contaminants or oxide layers that exist.

![Current Pogo Block](image)

**Figure 7.1 Current Pogo Block**

7.3 Testing

7.3.1 Testing Apparatus

The testing was done on a test fixture especially built for the pogo block and DIB board. It comprises of a 3-axis stage with 1" travel in each direction. The stages are actuated using a micrometer for each stage. The capability for pogo cycle testing to be done is currently being built into the apparatus. A DC motor for the z-axis control has been acquired and a controller has been built for the purpose of cycle testing. The motor interchanges with the micrometer for easy attachment. Figure 7.2 shows the apparatus used in the testing. The printed circuit board used is the actual device interface board (DIB) used in the test systems.
Figure 7.2: Three axis stage, bracket and pogo pin assembly

The fixture is capable of moving the block radially (x-y) for pin to pad location testing and in the z-direction for compression testing.

7.3.2 Testing Equipment

Time domain reflectometry (TDR) and Network Analyzer measurements were taken for the existing block. TDR uses a step generator and an oscilloscope, and investigates a fast edge signal being launched into a transmission line. At a particular point on the line, the oscilloscope monitors the incident and reflected voltage waves. The characteristic impedance of a line is defined by its resistance, capacitance, inductance and conductance. After the step generator produces the positive-going incident wave, the step travels down the line at the velocity of propagation of the line. If the load impedance is equal to the characteristic impedance of the line, no wave is reflected. If an impedance mismatch exists at the load, part of the incident wave is reflected. Generally, designers make both transmission lines and boards to have a characteristic impedance of 50 ohms. A useful characterization in evaluating the transmission
line is by examining the rise time of the signal in the time domain. The rise time of a signal is defined as the time required for the step response to rise from 10% to 90% of its final value. We used the rise time of the signal as a means of comparison between different pogo pins. Figure 7.3 gives an example of how the rise time of a signal looks on the display of the oscilloscope. The picture was captured from the screen of the oscilloscope.

![Signal rise time at interconnection](image)

**Figure 7.3: Sample Rise time of a pogo pin interconnect**

Network Analyzer measurements are taken in the frequency domain and give insertion loss measurements for a range of frequencies. Figure 7.4 is the network analyzer used for testing.
Similar to the TDR, a signal generator produces a sinusoid whose frequency is swept to stimulate the device under test (DUT). The network analyzer measures both the reflected and transmitted signals from the DUT. The data is delivered in terms of scattering parameters or s-parameters. S-parameters are a useful network representation to characterize terminations at high frequencies. Other network parameters exist that evaluate open and short circuits, however as we move in higher frequency, the effectiveness of these other parameters declines. S-parameters return a direct physical interpretation of what the system is doing. Typically, the boards are made to be used in a 50 ohm terminated environment. In an ideal situation, all the energy sent down a path will be absorbed by the termination and reflections will not result. This would translate into 0 dB loss over the full tested range of frequencies. A loss of 3 dB corresponds to a 50% loss in power transmitted through the line. Figure 7.5 gives a good representation of how a network analyzer works.
7.4 Results

7.4.1 Pogo Compression Testing

The first test that was done was a pogo pin compression test using the TDR. The pogo pin was aligned to the center of the pad and incremented down to the maximum travel position in .1mm increments, where each rise time measurement was recorded. Compression tests were also done at the side (offset from the center) of the pad, as well as near the edge. Table 7.1 shows the amount of compression of the pogo pin for interesting test points.

<table>
<thead>
<tr>
<th>Interesting testing locations</th>
<th>Amount of Travel mm – (inches)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/3 of total travel</td>
<td>1.06 (.04”)]</td>
</tr>
<tr>
<td>2/3 of total travel (rated travel)</td>
<td>2.04 (.08”)</td>
</tr>
<tr>
<td>Maximum travel</td>
<td>3.175 (.125”)</td>
</tr>
</tbody>
</table>

Table 7.1: Pogo pin compression chart

The 2/3 travel or ‘rated’ travel is what the manufacturer specifies as the recommend working travel. Spring forces and stresses are calculated at this point and thus overstroking the probe or traveling beyond the 2/3 limit could decrease mechanical life. Consequently, testing at
maximum travel can possibly damage the plunger tip or the device interface board (DIB) by permanently deforming the plunger tip or the gold pads. Figure 7. shows the rise time versus pogo compression when testing at the center of the pad.

![Risetime vs. Pogo pin Compression @ Center of Pad](image)

**Figure 7.6: Center of Pad, Rise time versus Pogo Compression**

The rise time varies significantly below the 1/3 of total travel, however as the compression increases, the rise time variations stabilize. At the touchdown area, the rise time is relatively high, because there is little force holding the pin down at this point. The reason for the decreasing rise time with increased compression is the unshielded characteristic length through which the signal must travel becomes smaller. The unshielded length acts a spurious inductance in the transmission line and causes parasitic losses through the line. One key in designing high frequency interconnects is to keep all of them as short as possible. This minimizes delay times, clock skew and signal integrity problems.

The same type of pogo compression data was taken using the network analyzer. Using the network analyzer, the amount of loss or degradation the signal sees through the entire system in
the frequency domain is captured. The loop consists of the cable from Network analyzer to coax junction through the coaxial cable to the pogo pin, from the pogo pin to the launch pad on the board. On the board the signal must then travel through microstrip or stripline to the SMA connector that is connected by a network analyzer cable back to the Network Analyzer. Hence, the data for the network analyzer includes the interconnection as other portions of the system. Figure 7.7 shows a graph of insertion loss at different stages in pogo compression. It is worth mentioning that touchdown is when the pin barely makes contact with the pad, therefore the robustness of the contact is minimal. As compression increases, the interface between the pogo pin and the pad becomes more stable, and the characteristic length of the interconnect becomes shorter.

![Insertion Loss Measurements vs. Frequency at different compression Stages](image)

**Figure 7.7: Transmission data at various stages in compression**

A loss in 3dB corresponds to a 50% decrease in power transmission across the line. Figure 7.8 shows the pogo compression data taken at 2/3 travel (rated travel) for pogo pins with a spear tip
shape. From Figure 7.8, it is evident that the problem with signal degradation is at frequencies beyond the 4 GHz range.

![Insertion Loss Measurements for Spear Tip, FR4 Board](image)

**Figure 7.8: Pogo Compression, Transmission of Signal versus Frequency**

### 7.4.2 Pogo Placement Study

Another study was done to see the effects of pogo placement on the pad correlated to the signal rise time. The pogo was compressed to the rated travel at each of the locations (1-4). Figure 7. shows that the variation around the pad causes only a minimal effect on the rise time, if any. The only conclusion to deduce from Figure 7. is that the rise time of the signal is independent of path location. This is expected because the location of the pin on the pad does not effect the unshielded length of the pogo pin. Therefore, the inductance remains the same.
Figure 7.9: Pogo placement, Rise time versus Pogo Compression

7.4.3 Pogo Pin Tip Shape Testing

Another characteristic of the pogo pin that may affect the signal is the shape of the tip on the end of the pin. The tip is the contactor for the pin, therefore its characteristics could perhaps influence the integrity of the signal. It is proposed that if the pad, which the tip is contacting, can be permanently deformed, and the contact area increased, then the integrity of the signal will improve. The primary objectives for contact materials are low contact resistance and high corrosion resistance. These tips are either gold plated over nickel or Beryllium copper. Although soft, gold is a good corrosion resistant material and nickel gives the tip good hardness properties. Beryllium copper has been an industry standard for years because of its low resistance and adequate hardness.
Currently, Teradyne mostly uses a 30° spear point tip in their test systems. This shape is shown in Figure 7.10. This is the tip shape that was used in Figure 7.7, 1.7 and 1.8. It was chosen because it can allow for less stringent tolerances and it is a more cost-effective option.

![Diagram of 30° Spear Point Tip]

**Figure 7.10: IDI Spear Point Tip of 30° (diameter = 0.020")**

The objective of this investigation is the correlate mechanical variations in tip shape and contact area to signal integrity. The oxide layer is of some consideration when choosing a tip shape. Pointed tips are said to break through existing oxide layers thereby effectively reducing the contact resistance and providing good intermetallic contact. The pads on the PC boards are gold plated nickel. A layer of nickel is placed underneath the soft gold to give the pad robustness. Nickel has low interdiffusion rates with copper and gold, thus preventing the migration of copper to the surface where it will corrode. The use of nickel allows the use of thinner topcoat coatings such as gold. Gold is used as a topcoat because it has a low contact resistance. This is due to a combination of its low modulus and its corrosion resistance. However, gold has poor wear resistance. Thus, the nickel undercoat improves the wear resistance of the gold topcoats. In addition, the primary disadvantage of gold is high cost. Therefore, only thin topcoat layers are used.

The manufacturers create different tips for various uses. For example, some tips are made to mate to via holes, as shown in Figure 7.11. This would require tighter mechanical tolerances within the system. Theoretically this may be a very good option for signal integrity because the contact area is much larger than that of a spear tip. Figure 7.12 shows the chisel tip shape, which is a widely used option for mating to via holes.
The rise time of the signal was measured using this chisel tip shape. As a means of comparison, all the tests were performed against incremental compression of the pogo pin. Figure 7. shows the rise time measurements using a chisel tip mated to a via. The FR4 in the graph title indicates the board material used. The next section will describe the results of using two different board materials and the effect in both the time and frequency domain.
Figure 7.13: Rise time versus Pogo Compression for a Chisel shaped tip

Figure 7. shows that the testing done was not 100% reliable. Four of the 6 trials have data that compares well. The 2 trials that do not agree with the other is because the pogo pin we used is not a standard size, so the tips were not manufactured specifically for our brass block. They were instead put on to the standard pin by hand. The procedure is neither reliable nor robust. The connection between the tip and the plunger of the pogo pin is noticeably weak on the modified pins. Another contributor could be the test setup itself. The location for each trial could be moderately inaccurate for the different trials. Also, the rise time seems to jump down after a 1 mm of compression. One interpretation could be that the inductance in the spring contact of the barrel is not stable until more compression is applied.

In addition to the spear and chisel tip shapes, a cleaver and round tip shape were investigated. Figure 7.14 and Figure 7.15 show the cleaver and round tip shapes, respectively. The manufacturer recommends the cleaver tip shape because it has 9 points of contact. The presumption is that more points of contact will result in less contact resistance and hence better
signal integrity. A rounded tip shape may have the advantage of more contact area touching the
pad, therefore resulting in better signal integrity.

Figure 7.14: Cleaver Tip Shape

Figure 7.15: Rounded Tip Shape

Figure 7.16 compares the results of the TDR measurements for the 4 different tip shapes. Notice
that the chisel and the rounded tip appear to have the lowest rise times in this case, but the
differences between all 4 are minor. For rise times, ± 20 ps is reasonably accurate. The trend
that the rise time improves as compression increases is a reasonable conclusion from Figure 7.16.
It should be mentioned that the confidence level in these results is not very sound. It is believed
that they give a decent general impression of how the tips compare, but the repeatability of these
results can be questioned. Appendices A-1 and A-2 contain more results from the TDR and
Network analyzer pogo compression tests.
7.4.4 Coaxial Probes

Coaxial probes are another type of pogo pin available from Interconnect Devices Incorporated (IDI). They were tested using both the network analyzer and the oscilloscope.

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Figure 7.16: Rise Time Comparison Chart between various tip shapes

Figure 7.17: Coaxial Pogo Pin
Figure 7.17 shows the coaxial probe. The unique feature about these probes is a concentric ground shell that surrounds the signal pin. The purpose of the ground is to shield the pin through the life of the signal until it reaches the board. The shielding plunger is also spring loaded like the signal pin. Its edges are serrated to break through any oxide layers. Between the signal and the ground shield, there is a dielectric acting as an insulator. In theory, this connector should allow interconnection with the least amount of signal deterioration while providing the same simple connect/disconnect features seen in traditional pogo pins. Thus far, experimentation of these pins has proven inconclusive.

A special board was made to test these pins because of the concentric ground configuration. There are two types of signal pad launches. Figure 7.18 shows both of them. One is suitable for a spear tip plunger and the other for a chisel tip plunger mating to a via. Using the test fixture, the coaxial pogo was aligned to the board and compressed against the pad. The TDR was the best indication that the connection existed because it was difficult to see the signal pin.

![Figure 7.18: Coaxial Pogo Launch](image)

Figure 7.19 gives the results form the TDR measurements for the spear tip signal pin. The data is consistent through the entire compression of the pogo pin. In other words, compression does not effect the performance of the pin as it does for the traditional pins. The primary reason is the signal is constantly being shielded at any compression. Therefore, spurious inductances causing the signal to degrade do not result from the interconnection. This data is also consistent with that from the traditional configuration.
In addition to the TDR, network analyzer measurements were taken for the coaxial pogo pins. The measurements indicated that the signal degradation using the coaxial pogo pins was extremely high compared to the other tip shapes. This, however, is inconsistent with the data from the TDR.
Figure 7.20: Insertion Loss Comparison Chart between various tip shapes

Figure 7.20 shows the comparison between the different tip shapes and the coaxial probes. There is a gradual degradation as the signal frequency increases for all the pogo pins. However, the coaxial pogo pins are unique because the insertion loss jumps down at 4 GHz whereas the others remain on a gradual decline. This graph also indicates that mating to a via with a chisel tip gives the best signal integrity of them all. This is perhaps because of the line contact the chisel tip makes with the via. Also, mating to a via eliminates any capacitance induced by the gold pad. The round and spear tip results are nearly identical. This suggests that the point contact made at the center of the pad is the same for both tip shapes.

Of the tests done, the data from the Network analyzer and the TDR measurements propose that the chisel tip mated to a via is the best interconnect solution to signal degradation problem at higher frequencies. An encouraging point is that the pogo pins currently being used in the test heads today fall within a range very close to that of the chisel tip mating to via.
7.4.5 Printed Circuit Board Material

The last variable that was investigated to improve signal integrity was the material used in printed circuit boards (PCBs). Traditionally, Teradyne has been using FR4 as their board material. Some other PC board materials include Teflon, Polyimide, Cyanate Ester, and Arlon 25N. With many layers of ground relief and signal traces, the boards are generally .250” in thickness. Dielectric loss in the board substrate material is one of the components of insertion loss in all PCBs. While dielectric loss may not be the critical loss component along the transmission line, it definitely contributes to some of the loss. The dielectric constants of FR4 and Arlon are 4.6 and 3.28, respectively. Theoretically, this means that insertion loss should drop off more quickly with boards made of FR4 than those made of Arlon. Another key point is that dielectric loss varies linearly with frequency.

An insertion loss comparison study was done between the FR4 and Arlon. Two boards of the same footprint were made of the two different materials. All the tests in sections 7.4.1, 7.4.2, 7.4.3, and 7.4.4 of this report were done on the FR4 board. Pogo compression tests using the network analyzer only were done for the various tip shapes. In general, the data shows that using Arlon as a board material results in less insertion loss. Figure 7.21 shows data to support this.
Cost is often a main factor when selecting the board material. The cost of making an Arlon board is approximately 1.75 – 2.00 times that of FR4. Results from a previous investigation shows that FR4 is the standard when dealing with signal frequencies up to 1.5 GHz. Beyond this range, Arlon, Teflon or some of the other aforementioned materials will suffice.
7.5 Conclusions

There are a few key conclusions that can be drawn from this pogo pin study:

- Pogo pin compression does effect the rise time of a signal. As the pogo pin becomes more compressed, the rise time decreases.

- Beyond half the compression of a pogo, the rise times do not change significantly.

- The location of contact on a gold pad does not effect signal integrity. However, it has been shown that mating to a via results in better signal integrity because the capacitance of the gold pad has been eliminated.

- The results from the coaxial pogo pin investigation showed them to be invariant of pogo pin compression. This is because the shielded ground ring eliminates any spurious inductance produced by an unshielded signal.

- The four different tip shapes that were investigated were the spear tip, round tip, chisel tip and cleaver tip. The shape of the pogo pin tip does have an effect on the integrity of the signal as seen by the insertion loss measurements. However, the rise time measurements were not as consistent. The rise time measurements give a good indication of approximate values. The differences between the different tip shape rise times is not significant enough to conclude that one tip shape is superior to another.

- The network analyzer measurements show the cleaver tip mated to a via on an Arlon board to be the configuration resulting in the least signal degradation of 2.8 dB at 4.5 GHz.

- The comparison study between printed circuit board materials found the board made of Arlon to perform better at higher frequencies than the board made of FR4. Arlon is nearly 1.5 – 2 times more costly than FR4, but produces better results at higher frequencies.
Chapter 8

Novel Interconnect Design

In the verification study of the pogo pin interconnects, an opportunity for better contactor or interconnect design presented itself. At high frequencies, the interconnect provides a vulnerable location for signal losses to occur. More ground shielding would reduce the cross talk exhibited by the interconnect, and the signal would then be allowed to travel along the transmission line with less loss. In addition to this, contacting 90 degrees to a surface gives rise to more losses than a smooth, transitional contact. It is also necessary to consider the density of the contacts and to pack more interconnects into a smaller area. This interconnect could be used in BGA or μBGA™ sockets, or could also be used within automated testers when providing contact at higher frequencies between the device interface board and the electronics.

8.1 Design of a New Interconnect

The design requirements for the proposed interconnect are shown in Table 8.1. Firstly, the interconnect has a requirement of at least .02" vertical displacement. This can be accomplished using a cantilever beam geometry. Another possibility for the design could be variations of a spring-loaded contactor. The next functional requirement indicates that this interconnect must be able to provide good signal integrity at high frequencies. This can be accomplished by shielding the signal as much as possible and ensuring matched impedances along the line. This is seen as a major limitation with existing interconnects. The low force functional requirement is driven by the density of the interconnects. In the automated testing equipment (ATE) industry, testers will soon contain over 1000 interconnects and this number is increasing every year. Because of this high density, it is necessary that the interconnects have a low contacting force. If the contacting force is low, the total compression force of the test head at the point of docking will also be low. Note that currently these values are upwards of 2000 lbs. As the number of interconnects
increase, the docking compression force becomes a limitation in the design of the test head. In
general, the low force requirement and the deflection requirement are the constraints, and the
physics dictates that the geometry be adjusted to meet the two requirements. The next functional
requirement addresses the density issue again. It is important that the interconnects can be
nested or packed on a footprint close together. This again depends on the geometry or shape of
the interconnect. The limitation in nesting or packing the interconnects close together is
electrical crosstalk. Because high frequency signals travel on the outer surface of the
transmission line, there often exists electromagnetic radiation. The radiation of one interconnect
interacts with the radiation of a neighboring interconnect, and the result is crosstalk. This is an
especially challenging problem at high frequencies. The final functional requirement is
manufacturability of the interconnect. Pogo pins are widely used in the ATE industry because
they allow high density, are fairly low in cost and offer a desirable option of easy maintenance.
There must be a tip at the contact point of each interconnect. Methods of manufacturing this tip
could include sheet metal forming, machining or grinding. Sheet metal forming such as
stamping provides a cost-effective means to manufacturing the tips. The high level physics
behind stamping is that the post-process contact stress of the material must be lower than yield
stress of the material. If the contact stress exceeds the yield stress, cracking or tearing of the
material can occur. Therefore, a round tip shape may be more viable than a conical tip shape
when stamping the contact tip.
<table>
<thead>
<tr>
<th>Functional Requirements</th>
<th>Design Parameters</th>
<th>Physics</th>
</tr>
</thead>
<tbody>
<tr>
<td>.02” of Vertical Travel</td>
<td>Cantilever Beam</td>
<td>[ \delta_{\text{required}} = \frac{FL^3}{3EI} ]</td>
</tr>
<tr>
<td></td>
<td>Spring Loaded Contactor</td>
<td>[ \delta_{\text{required}} = \frac{F}{k} ]</td>
</tr>
<tr>
<td>Shield Signal for high speeds &gt;1GHz</td>
<td>Coplanar Waveguide Geometry</td>
<td>See section 8.2.1</td>
</tr>
<tr>
<td></td>
<td>Concentric Ground Shield</td>
<td>Electromagnetic Field Equations</td>
</tr>
<tr>
<td></td>
<td>Surrounding interconnect with ground lines</td>
<td>Electromagnetic Field Equations</td>
</tr>
<tr>
<td>Low force &lt;1.8 oz per connector</td>
<td>Material</td>
<td>[ \sigma_{\text{actual}} &lt; \sigma_{\text{yield}} ]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[ \sigma_{\text{actual}} = \frac{M \cdot c}{I_{\text{composite}}} ]</td>
</tr>
<tr>
<td></td>
<td>Geometry (for cantilever beam)</td>
<td>[ \delta_{\text{required}} = \frac{L^3}{F_{\text{prescribed}} 3EI} ]</td>
</tr>
<tr>
<td></td>
<td>Geometry for spring loading</td>
<td>[ \delta_{\text{required}} = \frac{1}{F_{\text{prescribed}} k} ]</td>
</tr>
<tr>
<td>Pack many connectors in small area (Increase density = more connectors per board)</td>
<td>Shape of connectors in nesting configuration</td>
<td>Electrical Crosstalk Equations</td>
</tr>
<tr>
<td>Manufacturability</td>
<td>Shape of tip</td>
<td>[ \sigma_{\text{contact}} &lt; \sigma_{\text{yield}} ]</td>
</tr>
</tbody>
</table>

**Table 8.1: Design Table for New Interconnect**

### 8.2 Concepts

Some concepts which meet the criteria of Table 8.1 could include existing, commercial interconnect technologies such as pogo pins, Fuzz Buttons™ and the IBM “C” contactor. Pogo pins are described in detail in chapter 7. In addition, a pogo pin is also schematically described in Figure 8.1. Fuzz Buttons™ are another type of interconnect which is based on the spring contact principle. A description of this can be seen in Figure 8.2. Another concept that has been marketed is a C-shaped interconnect by IBM. It is essentially a spring loaded interconnect, however the spring is a C-spring rather than a traditional helical spring. A diagram of this can be
found in Figure 8.3. A new concept for a viable interconnect was also introduced. It is a shielded cantilever beam that has the capability to be nested for density purposes, and shielded to meet the demands of higher frequencies. This interconnect will be called the coplanar waveguide (CPWG) interconnect. A coplanar waveguide is a type of transmission line that enables ground shielding of the signals from virtually all sides. A concept design of this is shown in Figure 8.4. The contact tip is shown as a spherical contactor.

![Diagram of Spring Contact Probe]

Figure 8.1: Pogo Pin Interconnect

![Diagram of Fuzz Button]

Figure 8.2: Fuzz Button™ Interconnect
Figure 8.3: IBM C-Spring Interconnect

Figure 8.4: CPWG Interconnect

These four different concepts, both new and old, will be evaluated and ranked using a Pugh chart.

8.3 Pugh Chart

To evaluate these concepts, a Pugh chart was employed. The functional requirements are listed in the rows of the chart. Each design is assigned pluses and minuses depending on how well the design addresses the functional requirement.
<table>
<thead>
<tr>
<th>Functional Requirements</th>
<th>Pogo Pin</th>
<th>Fuzz Button</th>
<th>C-Spring – IBM</th>
<th>CPWG</th>
</tr>
</thead>
<tbody>
<tr>
<td>.02” of Vertical Travel</td>
<td>+</td>
<td>0</td>
<td>0</td>
<td>+</td>
</tr>
<tr>
<td>Shield Signal for high speeds</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Low force per interconnect</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Increase density of interconnects</td>
<td>+</td>
<td>0</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Manufacturability</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>0</td>
</tr>
<tr>
<td>Totals</td>
<td>0</td>
<td>0</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>

**Table 8.2: Pugh Chart for Interconnect Designs**

Through evaluating each design for its ability to satisfy each functional requirement, the CPWG design was chosen as the final concept. It has a major advantage of shielding the signals at higher frequencies. In addition, this design has the capability of nesting and experiencing even more shielding benefits. The detailed design will be described in the following sections.

### 8.4 Detail of CPWG concept

The coplanar waveguide is a type of transmission line. The most common type of transmission line is the coaxial cable, which is used at lower frequencies. However at frequencies beyond 1 GHz, waveguide transmission lines become more useful. Examples of these are microstrip lines, stripline, and coplanar waveguides.

#### 8.4.1 Transmission Line Losses

As signal frequencies increase, transmission line losses increase as well. These losses include conductor losses, dielectric losses, radiation losses and leakage losses. The conductor losses are associated with the skin effect resistance. The skin depth is closely correlated to the frequency of the signal. At very high frequencies (i.e. those above 1 GHz) the signal travels on the skin of
the transmission line and the skin depth is very low. The dielectric losses are obviously
associated with the dielectric that is being used in the transmission line. Air is the most desirable
dielectric to use, however, often times for structural purposes, the use of air is not possible.
Because the signal travels from one medium to another (i.e. PC Board to interconnect), it is
desired to have impedance controlled structures. Impedance controlled structures minimize
losses due to crosstalk, impedance mismatch and dielectric materials. Some examples of such
structures are a coaxial cable, microstrip, stripline and the coplanar waveguide.

All transmission lines have a characteristic impedance, \( Z_0 \). This impedance is defined as a ratio
of voltage to current for a wave moving along that particular transmission line. It is important to
“match” the load on a line to the characteristic impedance because then total energy transfer of a
signal will occur. If the lines are not perfectly matched, it will result in a reflected wave of
opposite polarity and loss of energy in the line. In addition to mismatched lines, dielectrics also
provide some loss at higher frequencies. Therefore minimizing cross talk through better ground
shielding and matching the impedance between the interconnect and the board is essential when
improving signal integrity.

### 8.4.2 Impedance Matched Coplanar Waveguide

In the case of the electrical path through which these interconnects will be used, the impedance
of the structure is controlled at 50 \( \Omega \). Therefore interconnects must be made to match the 50 \( \Omega \)
characteristic impedance. The pogo pin interconnects discussed in Chapter 7 all have a
characteristic impedance of 50 \( \Omega \). The coplanar waveguide configuration was chosen because it
is a well-shielded structure. Similar to the coaxial pogo pin introduced in section 7.44, the
coplanar waveguide is surround with grounds to provide shielding from crosstalk and density
issues. The coplanar waveguide with a ground plane underneath is shown in Figure 8.5.
Figure 8.5: Cross Section of a Coplanar Waveguide Transmission Line

Figure 8.5 shows a ground plane underneath the coplanar waveguide. This provides even more shielding to the signal. The characteristic impedance of the coplanar waveguide is determined by the gap between the conductor and ground, the height of the dielectric, the dielectric constant and the width of the conductor. These dimensions are shown in Figure 8.5.

8.4.3 Characteristic Impedance of a Coplanar Waveguide Structure

The following equations can be used to determine the characteristic impedance of a coplanar waveguide structure. The inputs are based on the widths and thicknesses shown in Figure 8.5.

\[
Z_o = \frac{60.0\pi}{\sqrt{\varepsilon_{eff}}} \frac{1.0}{K(k) + K(k_1)}
\]

(8.1)

\[
k = \frac{2a}{b-a}
\]

(8.2)

\[
k' = \sqrt{1.0-k^2}
\]

(8.3)

\[
k_1' = \sqrt{1.0-k_1^2}
\]

(8.4)
\[ k_1 = \frac{\tanh\left( \frac{\pi a}{4.0h} \right)}{\tanh\left( \frac{\pi(b - a)}{6.0h} \right)} \]  

(8.5)

\[ \varepsilon_{\text{eff}} = \frac{1.0 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_1')}{K(k_1)}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1')}{K(k_1)}} \]  

(8.6)

A Hewlett Packard software package program, named APPCAD, was used to determine the characteristic impedance of the various cross-sections of the coplanar waveguides. APPCAD is based on with the above formulae (Equations 8.1-8.6). The software was developed by Hewlett Packard in 1990. Inputting the critical geometric values (as shown in Figure 8.5), the desired frequency and the dielectric constant would returned the characteristic impedance and the effective electrical length to the user. APPCAD becomes useful when iterating between the 50 \Omega characteristic impedance requirement and the mechanical requirements in order to converge upon a viable interconnect design.

### 8.4.4 Contactor Tip

It is proposed in the design to have a contactor tip that is connected to the signal and ground traces. This tip is the essential part of the interconnect. Both the conical and spherical shaped tips were modeled. The spherical tip is easier to manufacture through sheet metal forming. The drawback is that a spherical shape may not break through an oxide layer that has formed on the contact surface and therefore the conical shape is better suited. From the experiments done in Chapter 7, it is shown that a spherical tip shape on the pogo pin performed just as well as the pointed (conical) tip shaped. Therefore, the spherical tip shape was designed in as the contactor of choice for the CPWG interconnect.

### 8.4.5 Material Selection and Properties

The material used for the conductor and the ground shield is half-hard Beryllium Copper (BeCu). It is a standard conductor material used in the semiconductor industry for interconnections. The
The dielectric chosen is Kapton® made by DuPont. Kapton® is a polyamide film that exhibits good thermal and electrical properties suitable for an insulator. The dielectric constant of Kapton® is 3.95. It varies slightly with thickness. This value is essential in the characteristic impedance calculations. The following table gives the material properties for the interconnect.

<table>
<thead>
<tr>
<th>Material Properties</th>
<th>Kapton®</th>
<th>Beryllium Copper</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elastic Modulus</td>
<td>500 ksi</td>
<td>18000 ksi</td>
</tr>
<tr>
<td>Poisson’s Ratio</td>
<td>.4</td>
<td>.3</td>
</tr>
<tr>
<td>Yield Stress</td>
<td>3000 psi</td>
<td>120 ksi</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>3.95</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Figure 8.6: Material Properties of Interconnect

The limiting stress of the interconnect is 120 ksi. Therefore, using a factor of safety of 1.5, the interconnect was designed not to exceed 80 ksi.

8.4.6 Design Iterations

There are two aspects of this design that must be considered; the electrical and the mechanical aspects. Because a major intent of the design is to build an interconnect that can withstand high frequencies signals, the electrical parameters are of the utmost importance. Based on the design table shown in Table 8.1, the mechanical requirements for low force and moderate deflection are dependent on the geometry of the interconnect. Similarly, the 50 Ω characteristic impedance is also based on the geometry of the interconnect as described previously. A parametric model for the interconnect was created in SolidWorks®. The model was driven by its critical dimensions. The iteration process began with the electrical parameters, namely APPCAD. The gap width, conductor width and dielectric thicknesses were all adjusted to ensure the 50 Ω characteristic impedance. Once the thicknesses and widths were determined, the parametric model was adjusted accordingly. A finite element analysis of the interconnect model was then done to determine the maximum deflection and stress. One end was fixed and the other was loaded at the contact tips on the ground and signal traces. This is shown in Figure 8.7.
8.4.7 Results

The iterative design process continued until the functional requirements of maximum deflection, minimal force and matched impedance were met. A few different options were arrived upon. An example of one of the iterations is shown. This design was of the standard CPWG cross section as shown in Figure 8.8. The tip shape was spherical and was attached to both the signal and ground lines. A plated through hole, or via, was routed between the side and back ground planes. This allows the ground for all three parts to be connected to the same earth ground.
The APPCAD input parameters for this iteration are shown in Table 8.3

<table>
<thead>
<tr>
<th>GEOMETRIC AND LOAD INPUTS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Gap Width (inches)</td>
<td>.01”</td>
</tr>
<tr>
<td>Conductor Width (inches)</td>
<td>.01”</td>
</tr>
<tr>
<td>Dielectric Thickness (inches)</td>
<td>.005”</td>
</tr>
<tr>
<td>Frequency (GHz)</td>
<td>12 GHz</td>
</tr>
<tr>
<td>Load Applied at each Tip</td>
<td>.03 lbs</td>
</tr>
<tr>
<td>Back-ground Thickness</td>
<td>.002”</td>
</tr>
<tr>
<td>Top Signal and Ground Thickness</td>
<td>.003”</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OUTPUT VALUES</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Characteristic Impedance</td>
<td>51.92 Ω</td>
</tr>
<tr>
<td>Displacement at Tip</td>
<td>.012”</td>
</tr>
<tr>
<td>Maximum Stress</td>
<td>52.1 ksi</td>
</tr>
</tbody>
</table>

**Table 8.3: Iteration Inputs and Outputs**

The corresponding finite element plots are also included. A side view of the displacement plot is shown in Figure 8.9. The maximum stress areas are in the regions of tight bending near the fixed end. However, in this particular case, the stress of 52.1 ksi is much less than the limiting yield stress of 120 ksi. Another iteration was done to get more displacement from the interconnect. There are some trade-offs in the design of the interconnect. A smaller thickness of each layer will cause the stress to increase, but it will also allow for more deflection. The width of each layer is also a factor, but does not have as much effect as the height. This is because displacement and stress are dependent on the moment of inertia of the cross-section. Each layer is a rectangular cross-section and the moment of inertia is given by the following equation 8.7.
\[ I = \frac{bh^3}{12} \]  

where \( b \) is the base width  
\( h \) is the height

The height effects the moment of inertia as a cube, whereas the base only effects it in a 1:1 ratio.

**Figure 8.9: Resultant Displacement of Interconnect**
Figure 8.10: Stress Results for Interconnect

Many design iterations for this interconnect were done. For most of the finite element iterations, the applied force was 0.09 lbs (1.6 oz). Because there are three contact points, the force was divided evenly between them at 0.03 lbs each. Iteration 3 was a slightly smaller applied load at 0.075 lbs. (1.25 oz) total.
<table>
<thead>
<tr>
<th></th>
<th>Gap Width (inches)</th>
<th>Conductor Width (inches)</th>
<th>Dielectric Thickness (inches)</th>
<th>Characteristic Impedance (Ω)</th>
<th>Load Applied (lbs)</th>
<th>Max Stress (ksi)</th>
<th>Max Displacement (inches)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>.01</td>
<td>.01</td>
<td>.003</td>
<td>38.09</td>
<td>.09</td>
<td>64</td>
<td>.02</td>
</tr>
<tr>
<td>2</td>
<td>.01</td>
<td>.02</td>
<td>.004</td>
<td>45.60</td>
<td>.09</td>
<td>140</td>
<td>.042</td>
</tr>
<tr>
<td>3</td>
<td>.0115</td>
<td>.007</td>
<td>.003</td>
<td>48.78</td>
<td>.075</td>
<td>43.34</td>
<td>.0147</td>
</tr>
<tr>
<td>4</td>
<td>.0115</td>
<td>.007</td>
<td>.003</td>
<td>48.78</td>
<td>.09</td>
<td>52.0</td>
<td>.017</td>
</tr>
<tr>
<td>5*</td>
<td>.0115</td>
<td>.007</td>
<td>.003</td>
<td>48.78</td>
<td>.09</td>
<td>67</td>
<td>.020</td>
</tr>
<tr>
<td>6</td>
<td>.01</td>
<td>.01</td>
<td>.005</td>
<td>51.92</td>
<td>.09</td>
<td>52.1</td>
<td>.012</td>
</tr>
</tbody>
</table>

Iteration 5 appears to be the exact same geometry as iteration 4, however the actual length and height values of the interconnect itself were varied. Both the length and the vertical height were shortened by .01". From the iterations, it can be concluded that to be within the limiting yield stress, the maximum displacement of an impedance matched coplanar waveguide is .02".

It would be optimal to taper the cantilever beam because it gives the most displacement for the least amount of applied load. However, this option is not possible if the interconnect is to be impedance matched. Another concern with this design is that because the three points of contact are in along a line, there is a risk that all three may not contact the pad or solder ball. This risk could perhaps be abated by gradually separating the 3 signal and ground lines from the kapton® near the tip. This would then allow the 3 contacting lines to free float slightly.

### 8.5 Conclusions

Using standard design principles an interconnect was developed for use in automated testers or device sockets at high frequencies. High frequency signals limit the ability of current interconnect technology because the electromagnetic fields that form around the interconnect interferes with neighboring inter-connet fields. Existing technologies such as pogo pins, Fuzz Buttons™ and IBM’s C-spring contactor were compared against a new novel interconnect called the CPWG interconnect. This design, which has a coplanar waveguide geometry cross-section, allows for good shielding of the high frequency signals. The CPWG has a certain characteristic impedance associated with it and this impedance must match the impedance of the devices on either end of the interconnect or it will result in signal degradation. In conjunction with this
electrical requirement, the interconnect must comply with mechanical stress and displacement requirements. The yield stress of the material must not be exceeded. Through iterations between the mechanical and electrical parameters of the interconnect, a final design was chosen. When loaded at 0.09 lbs of force, the interconnect displaced .02". This displacement may be sufficient in socket devices, however it is insufficient for the ATE industry. The requirement of the ATE industry is at least 0.10" displacement.
Chapter 9

Conclusions and Future Work

This chapter briefly outlines and recaps the 4 major phases of this thesis and how they are interrelated. These four phases include, the planarization study, the tip shape analysis, the signal integrity investigation and the design of a new interconnect. In addition, suggestions for future work in contact interfaces will be discussed.

9.1 Thesis Conclusions

The testing industry has struggled for years with the co-planarity of bent leads, and now new ways of approaching this for BGA and fine-pitch BGA devices with solder ball leads has been explored. First, a method for optimal testing of solder ball heights was introduced. It was then showed that planarization of solder balls improves the co-planarity of the device by an order of magnitude. More specifically the improvement was from about 0.00150" (38.1 µm) of co-planarity to 0.000106 (2.69 µm). With some difficulty, such as tool wear, solder buildup and compliance in the substrates, it was proven that planarization is an effective way of improving co-planarity. It is also a viable option for companies that are considering using fine-pitch BGA devices, such as µBGA™.

In the next phase of the project, closed-form solutions for both tip shapes were presented. Planarization enables rigid contactors or at least interconnects with much less travel to be used. The contactors presented were both the spherical and conical indenters. Using hertzian contact mechanics and elastic-plastic solutions, the indentation depth for both types of tips were calculated for a given load of 1.36N. It was found that the conical tip indented deeper than spherical tip. The plastic deformation of the indented material could produce a more robust electrical contact.
The effect of tip shape on electrical signal integrity was investigated in this project phase. The interconnect employed for the tip shape study was the pogo pin because it the standard interface the Automated Testing Equipment (ATE) Industry. The study describes the effects that tip shape and other mechanical contact parameters have on signal integrity. In particular, it was shown that both the spherical and conical tips resulted in the same level of electrical performance. Therefore, based on this study, both tip shapes appear to have the same effect. Another important conclusion of this section is that the line contact of the pogo pin tip to a plated through hole on a printed circuit board improved the signal integrity.

The integrity of the signal through the interconnect is a vulnerable area for signal losses to occur. Because of this, the final phase of the project introduces a new type of interconnect that addresses signal integrity. This new interconnect combines mechanical cantilever beam theory for compliance, and signal theory to create a better shielded signal structure. The interconnect is a coplanar waveguide that allows for better signal shielding when speeds are about 1 GHz. This structure is formed into a type of cantilever beam that can be nested for high density. The designed interconnect travels about 0.02" at 0.1 lbs of force. This amount of travel is sufficient for the interconnect to be used in testing sockets for devices. Because the signal integrity study determined that tip shape was irrelevant to signal integrity for elastic hertzian contact, the spherical tip shape was used because it is a more manufacturable tip.

All four phases contributed to better understanding how contact interfaces affect the semiconductor world, especially in the world of testing. Interconnects are critical in any electrical system. The increase in clock frequencies and the shrinking size of devices will continue to drive the industry to develop newer technologies for interconnects.

**9.2 Future Work**

A few key parts of this project require further investigation. The particular study would have proven very useful when relating tip shape and indentation depth to signal integrity. The contactor tip shape was only attempted for elastic deformation of the indenter surface, but it was not performed for plastic. Testing the actual BGA and μBGA™ devices for signal integrity is necessary for this work to be fully completed. Therefore, the plastically deformed solder by both
spherical and conical tip shapes while evaluating the signal integrity of the interconnect still needs to be done.

Additionally, the interconnect designed in Chapter 8 should be made and tested. Further design work could be done with sophisticated finite element packages to determine the electric and magnetic fields surrounding the interconnect. This interconnect has the potential to address concerns of the high speed test market, but additional investigation into the feasibility of this structure must be explored.
Chapter 10

Bibliography


Appendix A

Appendix A – 1: Additional Rise Time Data

Rise time Measurements, Coaxial Pin with Spear Tip, FR4 Board, A1 Pad

![Graph showing rise time measurements for different pogo compression levels.](image)
Rise time Measurements, Mate to Via with Chisel Tip, Arlon Board

Rise time (ps)

Pogo Compression (mm)

Trial 1  Trial 2  Trial 3  Average
APPENDIX A-2: Additional Insertion Loss Data

Insertion Loss Measurements for Coaxial Pogopin, Chisel tip, Arlon

Frequency (GHz)

---

Insertion Loss Measurements for Coaxial Pogo, Chisel Tip, FR4

Frequency (GHz)
Insertion Loss Measurements for Cleaver tip, Arlon Board

Frequency (GHz)

- Trial 1  - Trial 2  - Trial 3  - Average

Insertion Loss Measurement for Cleaver Tip, FR4 Board

Frequency (GHz)

- Trial 1  - Trial 2  - Trial 3  - Average
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