Growth and Characterization of High Quality Relaxed Graded Silicon Germanium Layers for Integrated Photodetectors

By

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Growth and Characterization of High Quality Relaxed Graded Silicon Germanium Layers for Integrated Photodetectors

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ABSTRACT

Silicon germanium layers on silicon substrates (SiGe/Si) are useful for a variety of microelectronics applications. The most successful technique for growing low defect density relaxed SiGe/Si layers is relaxed compositional grading. However, with increasing Ge content in the graded SiGe layers, the following materials concerns need to be addressed—(i) a high surface roughness, (ii) the formation of dislocation pile-ups, (iii) an increase in the threading dislocation density, (iv) tensile strains and micro-cracking due to thermal mismatch, and (v) particulate contamination from germane gas phase nucleation.

We have grown relaxed graded SiGe/Si layers using ultra-high vacuum chemical vapor deposition (UHVCVD) at growth temperatures ranging between 500°-900° C and pressures between 30-500 millitorr. The SiGe growth rates at different temperature and Ge content regimes agree with previously proposed theories.

By applying both a dislocation blocking criterion and surface roughness effects to graded SiGe/Si structures, we have proposed a model to explain and predict the formation of dislocation pile-ups in graded structures.

We have discovered that there is a substantial improvement in the surface roughness and dislocation pile-up density in graded SiGe layers by growing on miscut Si(001) substrates. It was found that the array of 60° dislocations that usually forms to relieve the misfit stress could transform into a novel lower energy hexagonal dislocation network consisting of all edge dislocations. High resolution X-ray diffraction measurements indicate that there is a decrease in the rate of epilayer tilting in the Ge-rich layers of the graded buffer in agreement with the observed dislocation structure.

We have designed an optimized relaxed buffer (ORB) process that allows us to grow high quality Ge layers on Si substrates. By employing a chemical mechanical polishing (CMP) and regrowth step within the epitaxial structure, we have minimized the formation of dislocation pile-ups. Compressive strain has been incorporated into the graded layers to overcome the thermal mismatch problem. The ORB process eliminates
dislocation pile-ups, decreases gas-phase nucleation of particles, and eliminates the increase in threading dislocation density.

Germanium $p$-$n$ photodiodes were fabricated to assess the electronic quality and prove the feasibility of a high quality infrared detector on a Si substrate. The dark current in the diodes was at least two orders of magnitude lower than any previously reported value for Ge photodiodes on Si substrates. Capacitance measurements indicate that the devices are capable of high speed operation.

Dislocation filtering experiments were conducted to reduce threading dislocation densities on patterned mesas. It was found that at the strain levels from small compressive mismatch, dislocation nucleation from the mesa edges dominates over dislocation filtering.

Thesis Supervisor: Eugene A. Fitzgerald
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1. Introduction and Background

1.1. Semiconductor heterostructures

Elemental semiconductors like silicon (Si) and germanium (Ge) and compound semiconductors like gallium arsenide (GaAs), indium phosphide (InP), etc. have been well studied and their properties and applications have been exhaustively explored. Over the last three decades Si-based microelectronics and GaAs-based optoelectronics have matured significantly and account for over 99% of the worldwide semiconductor electronics industry. New semiconductor systems and devices have also been invented. High quality Si and GaAs substrates and the economics in combining device and materials technologies have driven the efforts to develop the new systems and devices on the aforementioned substrates. In addition, strain from lattice mismatch between thin semiconductor films and substrates has been utilized successfully to engineer the bandstructure, film growth mode, etc. and create new device structures.

Heterostructures generally refer to epitaxially grown thin films on dissimilar substrates. Semiconductor heterostructures are extremely useful in providing added functionality to existing systems and creating new systems. For example, high quality heteroepitaxial growth of III-V compounds on Si substrates can potentially combine optoelectronics or high frequency electronics with conventional Si-based microelectronics. Good quality germanium (Ge) or silicon-germanium (SiGe) layers on Si can be used to build high speed field effect transistors (FETs), heterojunction bipolar transistors (HBTs)
and photodetectors which have enhanced performance. The potential advantages in creating high quality semiconductor heterostructures have spurred intense research in this area in the last couple of decades. In many cases of semiconductor heteroepitaxy, the incompatibilities due to differences in lattice constants, crystal structures, surface energies, etc. pose problems in achieving single crystalline thin films with good electronic properties. In semiconductor heteroepitaxy several issues pertaining to good quality growth and point, line, and surface defect behavior are still unresolved.

1.1.1. Growth modes

There are primarily two growth modes in thin film semiconductor heteroepitaxy. If the lattice mismatch between the film and the substrate is small (<1%) and the surface energies are not too different, the film growth is two-dimensional and strained. The lattice planes in the film match those of the substrate, resulting in tetragonal distortion of the film unit cells (Figure 1.1). Such growth is referred to as pseudomorphic. As the film thickness increases, so does the strain energy stored in the film. Beyond a certain thickness referred to as the critical thickness, it becomes energetically favorable to form misfit dislocations at the film-substrate interface to accommodate the lattice mismatch (Figure 1.2). By definition, dislocations cannot terminate abruptly within the single crystalline film. If they are not eliminated by reactions with dislocations of opposite Burgers vector, they terminate at the surface of the film, forming a threading dislocation. Alternately, under amenable conditions, threading dislocations can glide long distances to exit from the wafer edge.
Figure 1.1  Schematic of pseudomorphic strained thin film heteroepitaxy. Note the tetragonal distortion in the epilayer unit cells.

When the mismatch between the film and the substrate is large (≥2%), the film forms strained coherent three-dimensional islands. As the growth continues the film relaxes, forming misfit dislocations (usually edge type) at the island edges. Eventually the islands coalesce to form a uniform film with a network of edge dislocations at the interface and a high density of threading dislocations through the bulk of the film. Thus, in lattice mismatched heteroepitaxy, uniform film growth beyond the critical thickness results in a high threading dislocation density and poor material quality (Figure 1.3).
1.1.2. Dislocation geometries

The commonly used semiconductors have either diamond cubic (Si, Ge, etc.) or Zinc Blende (GaAs, InP, etc.) crystal structures. In low-mismatched (<2%) heteroepitaxy
on (001) type diamond cubic substrates the majority of the misfit dislocations that form are 60° type, that is, the angle between the Burgers vector the dislocation line direction is 60°. The dislocations, with Burgers vectors of the type <101> or <011>, lie on one of the four {111} slip planes that intersect the (001) surface. Two of the four {111} planes intersect the (001) surface along each of two orthogonal in-plane <110> directions. The misfit dislocations form on the {111} planes and glide down under the mismatch induced stress ($\sigma_x=\sigma_y=\sigma_m$) to the (001) interface. In plan-view one normally observes an orthogonal misfit network of 60° dislocations lying along the two perpendicular <110> directions at the hetero-interface. The threading segments at the ends of the misfit dislocations are generally screw or edge type.

The Burgers vector of a 60° dislocation can be resolved into edge ($b//\parallel$), screw ($b_\parallel$), and tilt ($b_\perp$) components. For example, a misfit dislocation lying along the [110] direction in a (001) plane with a Burgers vector $b=a/2<011>$ is made up of $b//\parallel=a/4[-110]$, $b_\parallel=a/2[001]$ and $b_\perp=a/4[110]$. The in-plane edge component of the Burgers vector is responsible for misfit relief. Thus, a 60° misfit dislocation is only 50% efficient in relieving misfit since its edge component is $b/2$ ($b//\parallel=b\cdot\cos 45°\cdot\cos 45°=b/2$). A more efficient dislocation for misfit relief is an edge dislocation with an in-plane <110> type Burgers vector. However, the 60° dislocations are glissile and can slide into the heteroepitaxial system using the primary slip system. Hence they are more commonly observed in low-mismatched heteroepitaxy. The $b=a/2<110>$ type pure edge misfit dislocations have been observed under larger mismatch such as Si$_{0.5}$Ge$_{0.5}$/Si$^2$. Since the
(001) plane is not a glide plane, they must form through glide reactions between appropriate 60° type dislocations or directly introduced through climb. When high mismatch leads to island growth, the edge dislocation is introduced through climb, whereas reaction of 60° dislocations is observed in low-mismatched planar growth relaxed to a great degree.

1.1.3. Dislocation sources in heteroepitaxy

It is important to understand the origin of dislocations in thin films in order to try to minimize or eliminate them. There are two major categories of dislocations—pre-existing substrate dislocations and those that nucleate during the epilayer growth. In compound semiconductor substrates like GaAs, the substrate dislocation density is generally between $10^3$-$10^5$/cm$^2$, whereas in high quality Si substrates the density is usually between 0-50/cm$^2$. The substrate dislocations thread into the epilayer and, upon growth beyond the critical thickness, can glide and lay down misfit segments in their wake at the film/substrate interface relieving mismatch strain. However, the substrate dislocations alone cannot explain the observed dislocation densities and the rates of relaxation in semiconductor heteroepitaxy.

The dislocations that form during heteroepitaxy arise through homogeneous or heterogeneous nucleation. A commonly invoked model for homogeneous dislocation nucleation is that of a half loop at the surface that can expand radially downwards to the mismatched interface and form a misfit segment with two threading ends. Energy calculations show that the activation energy for homogeneous nucleation is much higher
than the available thermal energy, suggesting true homogeneous nucleation is unlikely except at very high strain levels ($\approx 4\%$)\textsuperscript{5,6}. However, there are several perturbations such as surface topographic features\textsuperscript{7}, random variations in local alloy composition\textsuperscript{8}, substrate imperfections\textsuperscript{9} and particulate contamination from the growth chamber that can produce local stress concentrations that substantially reduce the surface half-loop nucleation barrier. Nucleation from such heterogeneous sources is probably the dominant mechanism of dislocation formation in heteroepitaxy. However, it is difficult to model or observe heterogeneous dislocation nucleation and hence the process is not well understood.

Other sources of dislocations are through dislocation interactions–reactions and multiplication. Dislocation reactions are favored if $\Sigma b^2$ of the products is less than the $\Sigma b^2$ of the reactants. This is referred to as the $b^2$ criterion\textsuperscript{10}. Two $60^\circ$ dislocations can undergo an energetically favorable reaction to form a misfit edge dislocation with in-plane Burgers vector (Eq. 1). Alternately, a $60^\circ$ dislocation might dissociate into partial dislocations to lower its energy (Eq. 2).

\[
\frac{a}{2}[01\bar{1}] + \frac{a}{2}[101] \rightarrow \frac{a}{2}[110] \tag{1.1}
\]

\[
\frac{a}{2}[110] \rightarrow \frac{a}{6}[121] + \frac{a}{6}[21\bar{1}] \tag{1.2}
\]

The best known dislocation multiplication mechanism, although now considered unlikely in most systems, is the Hagen-Strunk mechanism\textsuperscript{11}. In Ge/GaAs growth, it was speculated that when two dislocations with identical Burgers vectors and orthogonal line directions intersect, two L-shaped nodes are formed, one of which may cross-slip to the
surface creating two mobile segments. Stacking fault-related structures have also been observed to introduce misfit dislocations in several situations. The first of these to be identified was the diamond defect, which consists of a 1/6<114> faulted loop\textsuperscript{12}. The diamond defect (a heterogeneous nucleation source, now believed to be due to Al contamination) was shown to be capable of producing multiple 1/2<110> glissile dislocations with at least two different Burgers vectors. The modified Frank-Reed mechanism is another dislocation multiplication source that has been proposed to explain relaxation in graded SiGe/Si heterostructures\textsuperscript{13}. It was proposed that intersections of misfit dislocations lying in perpendicular <110> directions act as Frank-Reed sources for dislocation multiplication, forming characteristic pile-ups several microns deep in the Si substrate. Such a mechanism, however, has not been widely observed suggesting that it probably occurs under very specific growth conditions.

1.1.4. Critical thickness

Frank and Van der Merwe were among the first to come up with theories for describing lattice mismatched crystalline heteroepitaxial systems\textsuperscript{14,15}. The theories were basically mathematically rigorous energy expressions for misfit interfacial energies which were found to be considerably valid for high-mismatched bcc metal systems, but could not explain heteroepitaxy in diamond cubic and sphalerite structures very well\textsuperscript{4,16}. The first widely accepted theory to explain formation of misfit dislocations in strained semiconductor heterostructures was the one proposed by Matthews and Blakeslee\textsuperscript{17,18,19}.

The Matthews and Blakeslee model for critical thickness estimation is as follows. Pre-existing dislocations in the substrate thread through the epilayer as growth
progresses. There are two opposing forces, $F_g$ and $F_l$, acting on a threading dislocation. $F_g$ is a glide force due to the mismatch stress, which necessitates laying down a misfit dislocation at the mismatched interface. $F_l$, also referred to as the line tension, is an opposing force that arises from the self-energy of the misfit dislocation. As the film thickness, $h$, increases, so does the force $F_g$ on the threading arm. When $h$ exceeds $h_c$, a critical value, $F_g$ becomes greater than $F_l$ and the threading dislocation glides, forming a misfit dislocation. From an energy consideration, when $h>h_c$, a misfit dislocation forms since the strain energy relief from the dislocation introduction exceeds the self-energy of its formation. Figure 1.4 is a schematic depicting the Matthews-Blakeslee (MB) model.

![Figure 1.4](image)

**Figure 1.4** A schematic depicting the Matthews-Blakeslee model for critical thickness estimation. $F_g$ is the glide force from the mismatch and $F_l$ is the dislocation line tension.

The expression for critical thickness is as follows. For details regarding the solution for $h_c$ please refer to Appendix 1.
\[ h_c = \frac{D(1 - \nu \cos^2 \theta)(b / b_{af})[\ln(\alpha h_c / b) + 1]}{2Yf} \]  

In the above expression, \( D \) is the average shear modulus of the interface, \( \nu \) is Poisson's ratio, \( \theta \) is the angle between the Burgers vector and dislocation line direction, \( b_{af} \) is the in-plane component of the Burgers vector, \( \alpha \) is the dislocation core parameter, \( Y \) is Young's modulus under biaxial stress and \( f \) is the mismatch between the film and substrate. Inaccuracies in knowledge of the dislocation geometry, estimation of the core parameter and the elastic constants can result in differing final expressions. For an explicit and lucid description of critical thickness calculations please see Ref. 5.

The MB criterion is conceptually correct in estimating when the first misfit dislocation should appear and has been experimentally verified for several mismatched systems. Apparent deviations from the MB criterion have been observed for SiGe/Si\textsuperscript{20,21,22} and InGaAs/GaAs\textsuperscript{23,24} heterostructures. In most cases the experimentally determined critical thickness was found to be larger than the MB prediction. This has been attributed to metastable growth and incomplete relaxation due to low growth temperatures, as well as uncertainty in the technique used for detecting relaxation\textsuperscript{25}.

1.1.5. Effect of dislocations on electronic properties

Dislocations are deleterious for electronic device applications. They are known to be carrier recombination sites resulting in loss of carriers. They scatter carriers and hence reduce carrier mobilities. The dislocation cores are regions of fast diffusion for dopants. When they lie across an electronic junction, they can increase leakage current\textsuperscript{22} or act as shorts when present in sufficient numbers or when they are contaminated. They adversely
affect long-term reliability and are usually nucleation sites for dark-line defects (DLDs) leading to failures in light emitting diodes and lasers. One way to avoid threading dislocations completely is to grow films below the critical thickness determined by the lattice mismatch. However, many applications do require SiGe layers of greater thickness than that imposed by the critical thickness limit. Hence, a variety of techniques have been attempted to circumvent the threading dislocation problem.

1.2. Techniques for reducing defects in heterostructures

Semiconductor heterostructures open up avenues for innovative technologies and device structures and help add value to existing systems. Success in any semiconductor hetero-system relies on the ability to grow strain-relaxed layers with low defect densities. Although debatable, the generally accepted limits on threading dislocation densities are of the order of $10^6$/$\text{cm}^2$ for majority carrier devices and some minority carrier devices like common LEDs and certain photovoltaics, $10^3$/$\text{cm}^2$ for lasers and avalanche photodetectors (APDs). The effect of dislocations on Si complementary metal oxide semiconductor (CMOS) technology has not been determined since Si CMOS was developed from low dislocation density Si bipolar technology. Early silicon-on-insulator (SOI) works seems to indicate that Si CMOS can tolerate dislocation densities up to $10^6$/$\text{cm}^2$. Metastable growth at low temperatures, in principle, can give partially relaxed layers with low defect densities. However, subsequent device processing should have time-temperature cycles less than or equal to the original growth temperature, which imposes severe restrictions on the processing routes. This section outlines the common strategies employed to reduce misfit and threading dislocation densities in semiconductor
heterostructures during growth. Other common materials issues associated with heterostructures such as the surface roughness, dislocation pile-ups, etc. which are equally important in practical device integration have received limited attention in the literature.

1.2.1. Thick buffers and annealing

Two threading dislocations with opposite Burgers vectors can mutually attract and annihilate. In the case of a strained interface, dislocations traveling in orthogonal <110> directions can react, leaving behind an L-shaped misfit dislocation at the interface. Two dislocations traveling in parallel or anti-parallel <110> directions in a strained interface and having the same line direction will not have opposite Burgers vectors. If they have opposing Burgers vectors then they need to have opposing line directions too, to provide similar strain relief (compressive or tensile) at the interface. Hence threading dislocations traveling along parallel or anti-parallel directions cannot annihilate. In a material with high dislocation density, the meandering of threading dislocations up through the structure can lead to annihilation. Any process that can increase threading dislocation interaction, such that they have an encounter within an interaction radius, $r_i$ (500-5000 Å)$^{27}$ of each other, will promote annihilations and reduce the overall dislocation density. This is the premise in the growth of thick constant composition layers and post-growth annealing. In growth of thick uniform layers on (001) substrates, 60° dislocations lie along <110> directions, ensuring that they move towards each other as the film thickness is increased. The process of annihilation is effective when the threading dislocation is high ($10^9$-$10^{10}$/cm$^2$), but as the density drops, so does the probability of interaction and the
rate of dislocation reduction slows down. Decrease in threading dislocation density with increasing film thickness has been well documented for several systems. A few recent examples include GaAs/Si\textsuperscript{28,29}, CdTe/GaAs\textsuperscript{30,31}, ZnSe/GaAs\textsuperscript{32}, InP/GaAs\textsuperscript{33} and Ge\textsubscript{x}Si\textsubscript{1-x}/Si\textsuperscript{34}. In many studies decrease in the full width at half maximum (FWHM) of double crystal X-ray rocking curves was used as an indicator to estimate the decrease in threading dislocation density, which might not have been very accurate. The decrease in threading dislocation density, $\rho(h)$, with thickness, $h$, is generally observed to have the following empirical dependence with an adjustable parameter $D$\textsuperscript{35,36,37}.

$$\rho(h) = \frac{D}{h - h_0}$$  \hspace{1cm} (1.4)

Similar reduction in threading dislocation density in high-mismatch systems was observed through post-growth annealing\textsuperscript{38,39}. Ayers et al.\textsuperscript{28} showed that both as-grown and annealed GaAs/Si samples obeyed Eq. 1. 4, with a lower $D$ parameter.

A major challenge in layers with widely different coefficients of thermal expansion (as in GaAs/Si, Ge$\textsubscript{x}$Si$_{1-x}$/Si) is to avoid film cracking due to tensile thermal mismatch. The minimum threading dislocation density generally observed in thick layers is of the order of $10^7$-$10^9$/cm$^2$, depending on the system, for practical film thicknesses (10 $\mu$m or less).

\subsection{1.2.2. Strained layer superlattice}

A strained layer superlattice (SLS) basically consists of alternating strained layers of differing composition on a relaxed buffer. Individual layer thicknesses below $h_c$ and slightly above $h_c$ have been investigated, with varying results in different systems. There
is no one clear model in the literature that can explain the majority of the observations. In the beginning, the SLS was designed to strain the threading dislocations at the multiple interfaces and force them to the edges of the wafer. Such a process involving dislocation motion of several centimeters is probably impossible since it would require a high strain level and no dislocation interaction events en route. Another theory suggests that the difference in elastic moduli causes the interfaces to act as barriers to dislocation propagation since the dislocations would have a lower self-energy if they resided in the softer material. On the basis of this, dislocation multiplication sources such as the Frank-Reed source, etc. could not be operative within a SLS since they would have difficulty in traversing the interfaces. The effect of modulus on defect density is questionable. SLS filtering most probably works on the basis that the probability of dislocation interaction and subsequent annihilation increases substantially when they are forced to move in definite directions at multiple strained interfaces. In GaAs/Si, SLS filtering using alternate In$_x$Ga$_{1-x}$As/GaAs$_{y}$P$_{1-y}$ layers (such that the average lattice constant is that of GaAs) and GaAs$_{y}$P$_{1-y}$/GaAs layers with each layer slightly above $h_c$ has been shown to work successfully. In the Ge$_x$Si$_{1-x}$/Si system however, SLSs grown on top of Ge$_{0.5}$Si$_{0.5}$ relaxed buffers seemed to nucleate many threading dislocations. SLS filtering has been used in many different heteroepitaxial systems with varying degrees of success. An incomplete understanding of its operation makes it an unpredictable technique. In systems where the SLS filtering has been successful, the reduction in threading dislocation density is an order of magnitude or less.
1.2.3. Limited area growth

Heteroepitaxy on mesas patterned on substrates has been shown to reduce misfit densities in InGaAs/GaAs\textsuperscript{47,48,49} and Ge\textsubscript{x}Si\textsubscript{1-x}/Si\textsuperscript{50}. If the strain in the epilayer is low enough to prevent homogenous dislocation nucleation or nucleation on the mesa sidewalls, the misfit dislocations form from substrate sources alone. Hence, by reducing the growth area or reducing the areal density of heterogeneous sources, the density of misfit dislocations can be reduced\textsuperscript{5}. Moreover, since the misfit dislocations need only travel short distances before they terminate at the mesa edges (rather than at the wafer edge), the probability of dislocation interaction and multiplication is reduced. Both of these effects lead to substantially fewer misfit dislocations on the mesa compared to wafer scale growth. Fig.1. 5 is a schematic illustrating the principle behind limited area growth. Theoretically, mesa growth should also lead to a reduced threading dislocation density if the strain in the system is high enough to force the threading segments to the edge of the mesa. It has been calculated that 1\% strain on a 1 cm\textsuperscript{2} mesa can filter out as many as 2 \times 10\textsuperscript{6} dislocations\textsuperscript{5}.

The biggest disadvantage of mesa growth is the limited area and non-planar geometry, which might be incompatible with certain device processing steps. To provide connectivity across the entire wafer and at the same time limit dislocation propagation lengths, other reasonably successful substrate patterning techniques, such as a two-dimensional array of oxide dots, have been tried\textsuperscript{51}. Selective epitaxy of SiGe in oxide windows, like growth on mesas, has also been shown to improve the misfit density and
hence diode characteristics. Advances in via filling and planarization, due to back-end Si CMOS advances, should generally allow implementation of any patterned geometry.

Figure 1.5 A schematic diagram illustrating the principle behind misfit reduction in limited area growth. Fewer sources on the smaller area translate into fewer misfits.

1.2.4. Relaxed graded buffers

Currently, one of the more successful and widely accepted techniques for reducing defect densities in semiconductor heteroepitaxy is the growth of relaxed graded buffer layers. It involves slow compositional grading of the epilayer such that the system is never in a high strain state. The low strain minimizes dislocation nucleation and high growth temperatures promote dislocation glide to ensure complete strain relaxation. At each interface pre-existing threading dislocations from the previous layer glide to relieve the strain and hence each dislocation is most efficiently utilized. The relatively long distances traversed by the threading dislocations also improve the probability of finding a
complementary dislocation to self-annihilate. Another advantage of compositional grading is that the low strain ensures that the dislocations introduced are glissile 60° type (as opposed to sessile edge type) allowing for possible dislocation filtering by subsequent layer growth on patterned areas\textsuperscript{5}. By distributing the lattice mismatch across several low-mismatched interfaces the misfit dislocations now have an extra degree of freedom to glide past each other and avoid pinning events\textsuperscript{53}. All these effects result in long misfit lengths and a low threading dislocation at the top of the relaxed graded structure. Figure 1.6 shows a transmission electron microscope image of a relaxed graded SiGe/Si buffer in cross-section. Reductions in threading dislocation density of the order of 10\textsuperscript{7}/cm\textsuperscript{2} or more, compared to constant composition layers, are common in relaxed graded buffers.

![Image of transmission electron microscope image](image.png)

**Figure 1.6** A cross-section transmission electron microscope negative image of a relaxed graded SiGe buffer with a Si\textsubscript{1-x}Ge\textsubscript{x} cap layer. Note the long misfit lengths at the multiple interfaces and the absence of any threading dislocations in the uniform cap layer.
Relaxed graded buffers were first utilized in hydride vapor phase epitaxy of GaAs$_{1-x}$P$_x$/GaAs and GaAs$_x$P$_{1-x}$/GaP layers in 1969 by Abrahams et al.\textsuperscript{54}. The grading rates used in these studies were very slow ($7 \times 10^{-5}/\mu$m strain rate) resulting in buffer layers several tens of microns thick. This process was, subsequently, commercially used to make GaAs$_{1-x}$P$_x$/GaP light emitting diodes. The relaxed grading technique failed to attract the attention of the heterostructure community for quite some time afterwards. The interest in graded buffers was renewed in the late 80s with the growth of InAs$_x$Sb$_{1-x}$/InSb\textsuperscript{55,56}. In the Ge$_x$Si$_{1-x}$/Si system, completely relaxed buffers at relatively high grading rates ($4 \times 10^{-3}/\mu$m strain rate) and very low defect densities were first grown by Fitzgerald et al.\textsuperscript{53,57}. An important aspect of these experiments was the high temperature growth ($900^\circ$C) to ensure complete relaxation of the graded buffer. Ge$_x$Si$_{1-x}$/Si films of similar material quality were also claimed using conventional growth temperatures ($500$-$550^\circ$C) and much higher grading rates ($10^{-2}/\mu$m strain rate)\textsuperscript{13}. Relaxed graded SiGe buffers have also been studied by other groups with varying degrees of success\textsuperscript{58,59,60}. In the InGaAs/GaAs system too, relaxed graded buffers have been successfully used to grow low defect density layers\textsuperscript{61,62,63}.

1.3. Characterization techniques

This section outlines the common materials and electrical characterization techniques used to assess thin film semiconductor heterostructures.
1.3.1. Bulk defects

Transmission electron microscopy (TEM) is a versatile technique that can image two and three-dimensional defects in the bulk of a thin film semiconductor. It requires a sample that has been thinned to electron transparency using repeated mechanical polishing and ion milling. Using a plan-view sample one can obtain images of the misfit dislocation structure at the semiconductor hetero-interface. The areas imaged in TEM are typically of the order of a few tens of square microns. Hence one should consider the statistical inaccuracy when using TEM to estimate material quality parameters like threading dislocation density. Incorrect claims of threading dislocation densities, measured using plan-view TEM, are often made, especially at low densities when the dislocations are far apart. If statistically large and representative areas are imaged in plan-view TEM, one can obtain precise threading dislocation densities when the density is greater than $10^5$ cm$^{-2}$. When heterostructures are imaged in cross-section one can one get information about the interface quality, epilayer growth mode, film thickness, etc.

In TEM, diffraction contrast is used to identify defect characteristics. For example, when a dislocation is imaged using electron beams diffracted off specific lattice planes, it is possible to isolate its Burgers vector from the image contrasts. The basic conditions for zero dislocation image contrast are as follows.

$$g \cdot b \times u = 0 \quad \text{(edge dislocation)} \quad (1.5)$$

$$g \cdot b = 0 \quad \text{(screw dislocation)} \quad (1.6)$$

$g$ is the normal to diffracting plane, $b$ is the Burgers vector and $u$ is the normal to the plane that the dislocation lies on. If we identify two reflections, say $g_1$ and $g_2$, for which
$g \cdot b = 0$, then $b$ is parallel to $g_1 \times g_2$. Knowing the possible Burgers vectors possible, one can identify the right one. It should be noted that dislocations usually appear to be out of contrast when $g \cdot b < 1/3$. Similarly, some dislocations are not invisible when $g \cdot b = 0$, since $g \cdot b \times u$ is not. For a detailed discussion and other exceptions to the above rules, please refer to books on practical electron microscopy by D. B. Williams and J. W. Edington.

1.3.2. Surface characterization

Optical microscopy in the differential interference contrast (Nomarski) mode is commonly used to qualitatively image surface morphology and large features. This technique is limited by its resolution ($\sim 1 \mu m$), poor depth of field and focus, and the lack of quantitative information. Scanning electron microscopy (SEM) overcomes these drawbacks. When semiconductor heterostructures are imaged in cross-section, one can also obtain quick estimates of epilayer thickness in SEM, provided there is sufficient atomic number contrast between the film and the substrate. Atomic force microscopy (AFM) in the tapping mode is routinely used to characterize surface roughness. AFM has very high areal resolution and can be used to image atomic steps. However, one should be careful in analyzing the images since the scanning tip can easily introduce artifacts. It is considered a good practice to scan a known surface with the tip before scanning the experimental sample to ensure tip integrity.

1.3.3. Strain, tilt and composition

High resolution X-ray diffractometry can be used to measure the strain, composition, epilayer tilt and the degree of relaxation in heterostructures. Most high
resolution X-ray diffractometers have a beam conditioner that consists of a channel-cut collimator crystal and a monochromator crystal in the path of the incoming beam. This results in a beam that has an axial divergence, $\Delta \Theta$ of few tens of arc seconds and wavelength dispersion, $\Delta \lambda$ of the order of $10^{-5}$. The beam conditioner axis is also referred to as the first axis, the specimen axis being the second. In a double axis system the detector integrates scattered intensity from the sample from all angles allowed by its aperture. Hence, it cannot distinguish very small angular variations in the diffracted beam that might occur from small strains, small changes in composition or lattice plane tilts. In a triple axis diffraction (TAD) set-up an analyzer crystal is mounted in front of the detector. This is referred to as the third axis, which can be manipulated independently ensuring that the diffracted intensity from the sample is truly a function of angle. The enhanced resolution can be used to determine absolute lattice constants up to 5 significant figures and hence strains of the order of $10^{-5}$ routinely. Figure 1.7 is a schematic of the TAD set-up.

![Diagram](image)

**Figure 1.7** A schematic of the triple crystal X-ray diffraction set-up.
In a perfect heterostructure the lattice planes of the substrate and the epilayer are exactly parallel to each other. For growth on a miscut substrate it is known that the epilayer planes tilt away from the substrate normal. Secondly, the presence of misfit dislocations and other imperfections can locally misorient the lattice planes (also referred to as the mosaic tilt). Both these factors result in a distribution of Bragg angles locally, that can be mapped out as variations of the parallel (in-plane) and perpendicular (out of the plane) local lattice constants. It is convenient to plot the angular variations in reciprocal space. Reciprocal space maps (RSMs) can provide information about the mosaic spread, epilayer tilt, parallel and perpendicular lattice constants and hence strain, degree of relaxation and composition (assuming Vegard’s law). See Appendix 2 for equations to determine the heterostructure parameters from RSMs. TAD is a trade-off between resolution and intensity. Therefore typical RSMs take 7-12 hours even when a high intensity rotating anode X-ray source is used.

Epilayer composition can also be determined using energy dispersive analysis of X-rays (EDAX) in an SEM or TEM. To determine composition of alloy epilayers such as InGaAs or SiGe, EDAX requires standards of the pure elements or compounds created at conditions similar to the analysis. Even with a good set of standards, the composition determined using EDAX is only accurate to within 5%. The volume resolution in EDAX is \( \approx 1 \, \mu m^3 \) and so a reasonably thick epilayer is required to obtain a good composition estimate. Rutherford Backscattering (RBS) with a good data fitting software can also be used for thickness and compositional analysis. Secondary ion mass spectroscopy (SIMS),
with its low detection limits is very useful for estimating trace impurity levels such as oxygen, carbon, etc. in semiconductor heterostructures.

1.3.4. Large area defect density measurements

To estimate low defect densities it is essential to use a technique that can analyze large areas to obtain statistically accurate information. One such technique is electron beam induced current (EBIC). It requires a built-in p-n junction in the heterostructure. When an electron beam strikes the sample, it creates electron-hole pairs that drift in opposite directions across the depletion region. Some of the carriers are lost if there is a defect that acts as a recombination center for carriers. By monitoring the current through the sample across the junction, one can detect the presence of defects. If the current is used to form an image in SEM, the defects show up as dark regions of carrier recombination. When the defect density is low ($10^6$/cm$^2$ or lower) EBIC gives clear images. The resolution limit of EBIC is $\sim 1\mu$m; hence it cannot distinguish between defects if they are close or grouped in pile-ups. Dislocation pile-ups appear as dark bands in EBIC images. The pile-up density (in #/cm) can be estimated by counting the average length per unit area imaged.

A quick and accurate method to measure threading dislocation densities is to count etch pits formed from selective chemical etching. A number of defect selective etchants for semiconductor crystals are known$^{70}$. For SiGe based heterostructures a dilute Schimmel etch$^{71}$ (5 parts of 0.2 M Cr$_2$O$_3$ and 4 parts of 49% hydrofluoric acid) is commonly used to reveal threading dislocations in the epilayer. The etching rate is a function of the Ge content and doping concentration in the film. The defect structure is
best revealed for lightly n-doped or intrinsic SiGe films. Typical etch time for a 
$Ge_{0.3}Si_{0.7}/Si$ film is 1 minute, with longer times for higher Ge contents. The etch pits can 
be easily imaged using an optical microscope in the Nomarski mode and counted to get 
an estimate of threading dislocation density. Figure 1.8 shows a typical image used for 
etch pit density (EPD) measurements. The etching responds to underlying misfit 
dislocation strain fields and accentuates the surface roughness. This enhanced roughness 
can obscure the etch pits in some cases. Hence, samples that already have considerable 
surface roughness (for example as-grown SiGe samples with $\geq 35\%$ Ge) need to be 
polished before they are etched.

![Etch Pit Image](image)

20$\mu$m

**Figure 1.8** A 50%Ge graded buffer etched using the Schimmel etchant for 1 
minute. The bright spots are contrast from pits formed from selective 
etching at threading dislocation sites.
1.3.5. *Electrical measurements*

The ultimate test of semiconductor material quality lies in the material performance in the desired device and application. Diode ideality factor (n) and dark current or the current gain (β) of a bipolar transistor are parameters often used to characterize material quality. Both require fabrication of actual devices using the material before any information is revealed. In direct bandgap materials cathodoluminescence (CL)\(^7\) is commonly used to map out defects. Photoluminescence (PL) studies have also been used to estimate defect densities in heterostructures like SiGe/Si\(^7\)\(^3\)\(^7\)\(^4\). Deep level transient spectroscopy (DLTS)\(^7\)\(^5\) and Raman scattering\(^7\)\(^6\) are other techniques used to characterize defects in semiconductor heterostructures.

1.4. *Growth of SiGe/Si layers*

Silicon and germanium both have a diamond cubic crystal structure and form an isomorphous system, completely miscible in each other at all compositions in the liquid and solid phases. Ge has a larger lattice constant (5.65Å) than Si (5.43Å) resulting in a compressive lattice mismatch of \(\approx 4\%\) for Ge films grown on Si substrates. Different applications require different SiGe alloy compositions and the lattice mismatch depends on the Ge composition of the film.

The growth of SiGe/Si has been achieved using several different growth techniques such as liquid phase epitaxy (LPE)\(^7\)\(^7\), very low pressure chemical vapor deposition (VLPCVD)\(^7\)\(^8\), molecular beam epitaxy (MBE)\(^7\)\(^9\)\(^,\)\(^8\)\(^0\) and limited reaction processing (LRP)\(^8\)\(^1\) and ultra-high vacuum chemical vapor deposition (UHVCVD)\(^5\)\(^7\)\(^,\)\(^8\)\(^2\)\(^,\)\(^8\)\(^3\).
1.4.1. Applications of SiGe/Si thin films

Most of the III-V compound semiconductor materials used to fabricate opto-electronic circuits have a larger lattice constant than Si. Since Ge has a larger lattice constant than Si, relaxed SiGe/Si graded to high Ge concentrations can provide a pseudo-substrate for III-V/SiGe/Si hetero-integration. This opens up possibilities of light emitting diodes (LEDs), lasers and high efficiency solar cells on inexpensive Si substrates. The feasibility of such a process has been demonstrated by the fabrication of InGaP based red light emitting diodes on Si substrates\(^{57}\).

Ge has a smaller bandgap and higher carrier mobilities than Si. This fact is utilized in the fabrication of SiGe graded base hetero-junction bipolar transistor (HBT). The Si emitter has a larger band-gap than the SiGe base; hence the injection efficiency can be made high even if the base is doped heavily. Doping the SiGe base region of the transistor heavily reduces the base resistance and the transit time of minority carriers across the base\(^{84}\). This short transit time substantially increases the speed \(f_{\text{max}}\) substantially, at which the transistors can be operated. Several groups have successfully fabricated high performance and high speed SiGe transistors for communications applications\(^{85,86,87}\).

Since the valence band in strained SiGe/Si layers is always higher than in Si, by sandwiching a strained SiGe layer between two Si layers it is possible to create a two-dimensional hole gas structure that exhibits enhanced hole mobilities\(^{88}\). Similarly, by growing a tensile strained Si layer between two SiGe layers, it is possible to create a high electron mobility channel\(^{89,90,91}\). Schaffler has written a good review article on electron
and hole mobility measurements in the SiGe/Si system\textsuperscript{92}. Such structures and their variations are being researched to create high speed SiGe complementary metal oxide semiconductor (CMOS) structures that can perform faster than the existing Si CMOS technology at similar gate lengths\textsuperscript{93,94}.

Polycrystalline SiGe used as a gate material in CMOS technology reduces the gate work function and dopant activation temperature allowing for superior optimization of transistors\textsuperscript{95}.

\subsection{1.4.2. SiGe/Si based photodetectors}

Fiber optical communication requires photodetectors in the 1.3-1.55 $\mu$m wavelength range. Si with a bandgap of 1.12eV has its absorption cut-off edge at $\lambda \approx 1.1$ $\mu$m. The lower bandgap of Ge and the compatibility of SiGe alloys with Si based processing has been the motivation for research on SiGe based photodetectors. The first 1.3 $\mu$m detector on a Si substrate developed by Luryi et al.\textsuperscript{96} was a $p-i-n$ Ge detector grown on graded SiGe layers. The material, however, was highly defective so the dark current and the noise factor of the photodetector were high. Since then different structures such as strained SiGe/Si multi-quantum wells\textsuperscript{97}, silicide/SiGe Schottky barrier type\textsuperscript{98}, SiGe/Si internal photoemission type\textsuperscript{99} and SiGe/Si double hetero-junction diode\textsuperscript{100} have been investigated to build SiGe based photodetectors for optical communication and infrared detection applications. SiGe based detectors will also prove extremely useful for optoelectronics applications on Si substrates.
1.5. Motivation and organization of thesis

A summary of the various motivating areas of research that inspired this thesis is outlined in the next few paragraphs.

For III-V/SiGe/Si integration and Ge based photodetector applications relaxed graded SiGe buffers with high Ge concentrations are required. Relaxed graded SiGe films with low Ge concentrations have been successfully grown by several groups. Very few groups, however, have attempted to grow Ge rich SiGe relaxed graded layers. Growth to high Ge presents several materials challenges that have either not been addressed or are not well understood yet. There is an increase in surface roughness with increasing Ge content in graded SiGe buffers. There is also an increase in the overall threading dislocation density that is not predicted by the equilibrium theory of grading (Figure 1.9). The threading dislocation density in structures graded to pure Ge can be as high as 5 x $10^7$/cm$^2$. It is essential to control the monotonic increase in threading dislocation density in high Ge buffers for device applications.

Growth of III-V compounds on diamond cubic substrates requires miscut substrates to produce double atom steps to avoid formation of inversion domain boundaries (also referred to as anti-phase boundaries). The effect of substrate miscut on the materials characteristics and the dislocation structure of the graded buffer is not known.

Many aspects of the graded buffer relaxation process like dislocation nucleation, dislocation annihilation and filtering, etc. are difficult to observe and hence only a limited knowledge base exists.
Figure 1.9  Increase in threading dislocation density with increasing Ge content in the graded buffer.

A high quality Ge photodetector integrated on a Si substrate will be useful for optical communications and Si-based optoelectronics. It will also serve as a practical device to examine materials quality improvements that are implemented in the graded buffer.

During the course of this thesis we have investigated the effect of miscut substrates on the defect structure in graded SiGe/Si layers. A model to explain the formation of dislocation pile-ups and the concomitant increase in threading dislocation densities has been proposed and verified. We have implemented a novel optimized relaxed graded buffer process that allows us to grow very high quality Ge layers on Si substrates. Using these Ge layers we have fabricated a high quality photodetector with record low dark currents.
The second chapter discusses the ultra-high vacuum chemical vapor deposition (UHVCVD) of SiGe layers for different applications. The third and the fourth chapters deal with the formation of dislocation pile-ups and the effect of substrate miscut respectively. Improvements in the graded buffer for optimized strain relaxation are reviewed in the fifth chapter. The fabrication and characterization of a high quality Ge photodetector is the basis for the sixth chapter. Experiments in dislocation filtering are discussed in the seventh chapter. The last chapter summarizes the thesis.
2. Ultra-High Vacuum Chemical Vapor Deposition of SiGe/Si

Several groups have successfully grown good quality SiGe/Si heterostructures using ultra-high vacuum chemical vapor deposition (UHVCVD)\textsuperscript{57,101,102,103,104,105}. This chapter outlines the details of our unique UHVCVD reactor and the growth calibration data at different temperatures and pressures. The temperature dependence of growth rate and Ge incorporation in the film are seen to follow previously published models.

2.1. UHVCVD reactor

The reactor is a hot wall vacuum load-locked system which is capable of a base pressure better than 9 \times 10^{-10} \text{ Torr} at 750\textdegree C. The load lock can be pumped down to the 10^{-8} \text{ Torr} range before the quartz boat containing the wafers is transferred to the growth chamber using a transfer rod. This ensures minimal water vapor and oxygen contamination of the reactor. Both the growth chamber and the load lock are pumped by separate turbo pumps that are backed by a two mechanical pump system. The quartz reactor tube is seated on a stainless steel flange and sealed using dual set of o-rings. A unique design allows for evacuation of the area between the o-rings using a smaller turbo pump. This results in an intermediate pressure drop to 4 \times 10^{-3} \text{ Torr} between the o-rings, allowing the inner o-ring to maintain a UHV seal inside the growth chamber. The top of the quartz reactor has a glass to metal seal that needs to be cooled to below 300\textdegree C. The
reactant gases flow from the top of the reactor and react on the hot wafer surface. Figure 2.1 is a schematic of the UHVCVD reactor. There is a manual gate valve above the process turbo pump that can be partially closed to decrease the pumping efficiency and hence increase the growth pressure in the reactor. Before each growth, the gate valve is manually adjusted to give the required growth pressure in the reactor while flowing Ar at flow rate similar to the reactant flow during growth.

Figure 2.1  Schematic of the UHVCVD reactor showing the primary components.
2.2. SiGe/Si growth calibrations

The UHVCVD reactor has been calibrated to grow SiGe/Si at temperatures ranging between 550° C and 900° C and growth pressures ranging from 30 mT to 500 mT. The high growth pressures resulting from large flow rates of reactant gases in our system ensure that the CVD process is not mass-transfer-limited for most growth conditions. Hence, the growth rate is relatively insensitive to small variations in growth pressure. The growth rates are, however, significantly temperature dependent. In general, with all other factors remaining constant, increasing temperature results in increased growth rates. For growth of graded SiGe buffers, a grading rate of 5%Ge/μm or 10%Ge/μm was used. This implies that grading to high final Ge concentrations requires fairly thick graded buffers. Silane (SiH₄) and germane (GeH₄) were used as the Si and Ge source gases respectively. The p dopant was diborane (B₂H₆) and the n dopant was phosphine (PH₃). For growth of SiGe layers with <50% Ge, the SiH₄ flow rate was fixed at 100 standard cubic centimeters per minute (sccm) and the GeH₄ flow rate progressively increased from 0 to 50 sccm. The Ge rich SiGe layers were grown by retaining the GeH₄ flow rate constant at 50 sccm and decreasing the SiH₄ flow rate from 100 to 0 sccm.

Prior to epitaxial growth, the Si wafers, from a clean-room sealed box, were typically cleaned in a “piranha” solution (3 parts of H₂SO₄ + 1 part H₂O₂) for ten minutes. Following which, the wafers were rinsed in de-ionized water and dipped in dilute HF solution (10:1::H₂O:HF) for one minute to form a hydrophobic hydrogen terminated surface. The wafers were left under low pressure in the load lock for about 5-7 hours before being transferred to the reactor. Typically the first step in the growth process was a
150-200° C bake to desorb organic contaminants and water vapor followed by a high temperature (850° C) oxide desorption step. It was found to be beneficial to grow a Si buffer layer at high temperature after the oxide desorption step. Subsequently the temperature was brought down to the desired growth temperature. A second Si buffer was grown at the growth temperature before growing the final structure.

Figures 2.2 and 2.3 are SiGe growth calibration curves at 750° C and 250 mT growth pressure. The film thicknesses were measured using cross section SEM or TEM. Figures 2.4 and 2.5 show the incorporation of Ge in the film as a function of source gas flow under the same growth conditions. The film composition was determined through EDAX. Similar data were also compiled for growth at 550° C and 30mT growth pressure. The higher temperature and higher pressure calibration data was typically used to grow SiGe buffers graded to Ge contents below 50%. For growth of thin layers for device structures, the lower temperature growths are preferred. The oxygen and carbon contamination in the SiGe films determined through secondary ion mass spectroscopy (SIMS) was found to be <10^{18} atoms/cm^3 and <4 \times 10^{17} atoms/cm^3 respectively, indicating the high quality of the growth process.

It is known that there are two primary regimes of SiGe growth when using SiH\textsubscript{4} and GeH\textsubscript{4} as the reactant gases. The first regime is hydrogen desorption limited and the second is limited by dissociative adsorption of SiH\textsubscript{4} and GeH\textsubscript{4}\textsuperscript{101,102}. At low temperatures (<600° C) and low Ge concentrations (<25%), the surface sites are primarily occupied by hydrogen. With increasing Ge fraction in the film, the hydrogen desorption rate becomes higher due to the weaker Ge-H bond. This leads to an increased number of free surface
sites so the film growth rate increases with increasing Ge fraction\textsuperscript{106}. At higher temperatures and higher Ge fractions, most of the surface sites are free of hydrogen and a competing effect is observed. There is a reduction in the sticking coefficients of SiH\textsubscript{4} and GeH\textsubscript{4} with increase in Ge fraction in the film\textsuperscript{101,107}. This causes the film growth rate to decrease with increasing Ge fraction in the SiGe film at higher temperatures. There is sufficient experimental evidence in the literature to support both these theories.

Figure 2.6 shows the effect of temperature on the SiGe film growth rate at 250 mT. At 650\textdegree\ C there is an increase in growth rate with increase in Ge fraction, whereas at 750\textdegree\, a monotonic decrease in growth rate in observed. This implies that the transition between the two competing effects, just discussed, lies between 650\textdegree\ C and 750\textdegree\ C for growths at 250 mT.

![Graph showing the effect of GeH4 flow on growth rate](image.png)

**Figure 2.2** Growth rate calibration of Si-rich SiGe layers grown at 750\textdegree\ C and 250 mT growth pressure.
Figure 2.3  Growth rate calibration of Ge-rich SiGe layers grown at 750° C and 250 mT growth pressure.

Figure 2.4  A graph showing the incorporation of Ge in the Si-rich SiGe film with GeH₄ flow rate.
Figure 2.5  A graph showing Ge incorporation in a Ge-rich SiGe film with SiH₄ flow rate.

Figure 2.6  Effect of temperature on the growth rate of SiGe films grown at 250 mT growth pressure.
Figure 2.7  Effect of temperature on Ge incorporation at 250 mT.

We have also noticed that, other factors remaining constant, with increasing temperature there is a decrease in Ge incorporation in the film. Figure 2.7 shows GeH₄ flow rate and Ge fraction in film data for growth at 650° C and 750° C. Such an effect has also been observed by others¹⁰⁷,¹⁰⁸ and has been attributed to variations in sticking probabilities of SiH₄ and GeH₄ with temperature.
3. Dislocation Pile-up Formation in Graded SiGe/Si Structures

There is an increase in threading dislocation density with increasing Ge fraction in the graded buffer as shown in Figure 1.9. This cannot be explained from the theory of graded buffers. Researchers have seen dislocation pile-ups in graded structures the origin of which is not clearly understood\textsuperscript{109}. There is also an associated increase in surface roughness with increasing Ge fraction in the graded buffer. This chapter reviews the topic of surface roughness in graded SiGe structures and uses an existing dislocation blocking idea to propose a model that explains and predicts the formation of dislocation pile-ups in graded structures. The formation of pile-ups is primarily responsible for the puzzling increase in threading dislocation density.

3.1. Surface roughness in graded structures

Surface morphology and defect structure are key issues in utilizing relaxed graded SiGe/Si structures for electronic and opto-electronic applications. The strain fields associated with the misfit dislocations lead to the characteristic cross hatch pattern on the epilayer surface in lattice mismatched heteroepitaxy\textsuperscript{57}. The strain fields associated with threading dislocations also change the surface morphology\textsuperscript{110}. Lattice mismatch strain itself, without the presence of dislocations, can roughen the surface if the growth temperature, sign and magnitude of the strain are adequate\textsuperscript{111}. The unifying theme is that any event capable of producing lattice strain will induce surface roughening if the
temperature is high enough to allow enough surface diffusion to approach thermodynamic equilibrium. The surface roughness due to the cross hatch pattern in graded SiGe structures is primarily due to strain fields arising from inhomogeneous distribution of misfit dislocations at each grading step interface. The growing surface incorporates undulations (to minimize strain energy) in response to local strain field variations. The strain field variations from an array of misfit dislocations at each heterointerface extend well beyond each Ge grading step. Thus, the cross hatch pattern at any instant during growth is the response of the surface to multiple overlapping strain fields. The formation of the cross hatch pattern exposes higher index planes along the trenches. Anisotropic CVD growth rates along different lattice planes subsequently accentuates the surface roughness even further.

It has been suggested that the cross hatch pattern is primarily due to formation of surface steps produced by gliding 60° dislocations\textsuperscript{112,113}. This proposition alone, however, does not explain the increase in rms roughness of the cross hatch pattern with increase in grading rate for equally relaxed graded SiGe structures\textsuperscript{57,110}. Nor can it explain differences in cross hatch morphology (long-wavelength surface undulations) due to growth temperature. Also, the surface roughness anisotropy along the two \textit{<110>} directions (for growth on miscut substrates) cannot be explained by the surface step argument, since dislocations are introduced in equal numbers along both \textit{<110>} directions. Surface step formation by gliding dislocations could affect the cross hatch appearance in the early stages of stress relaxation in partially relaxed graded SiGe films\textsuperscript{114}. If surface diffusion is limited, for example at low growth temperatures, the steps produced by the dislocations
will not migrate the distances necessary to achieve the equilibrium surface. In completely relaxed graded SiGe/Si structures grown at higher temperatures where the equilibrium surface can be achieved, strain field effects from underlying misfit dislocations coupled with anisotropic growth kinetics are predominantly responsible for cross hatch formation.

For (001) epitaxy, the cross hatch pattern occurs in the form of trenches and ridges aligned along the two in-plane <110> directions. The cross hatch pattern has been observed in graded SiGe/Si\textsuperscript{110,114}, and other lattice-mismatched systems such as In\textsubscript{x}Ga\textsubscript{1-x}\textsubscript{As}/GaAs\textsuperscript{112,115}, GaAsP/GaAs\textsuperscript{116}, GaAs/Si\textsuperscript{117} and Ge\textsubscript{x}Si\textsubscript{1-x}/Si\textsuperscript{113}.

We note here that this cross hatch pattern is very different from the <100> oriented "surface ripples" that are observed\textsuperscript{118,119} in thin elastically strained SiGe/Si(001) epitaxial films. Under typical growth conditions, the surface ripples generally have a much shorter wavelength and originate from a thermodynamic equilibrium between surface roughness and misfit-induced elastic strain\textsuperscript{120}. In slowly graded SiGe structures grown at fairly high temperatures, such as the samples discussed in this study, the epilayers relax easily forming misfit dislocations at the interface and hence the <100> oriented surface ripples are not observed.

Figure 3.1 shows the effect of increasing final Ge content of the graded layer on the rms roughness of the top surface in Ge\textsubscript{x}Si\textsubscript{1-x}/Si films. Since all the graded layers were grown at 10% Ge/μm, different final Ge contents indicate that the graded regions in each structure have different thicknesses as well. With the increase in Ge content of the graded region, the rms roughness increases. In all low-mismatched heterostructures, the cross hatch pattern contributes to an increase in surface roughness.
In layers graded gradually to higher Ge concentrations (>30%), an additional feature appears in CVD grown material. Occasional, deep trenches are observed on the surface that account for increased rms roughness of the samples (Figure 3.2). Since they are absent in 10% Ge/μm graded layers grown to lower Ge contents (<30%), they must be related to a rare degenerative phenomenon in the relaxed graded region that occurs more frequently with increased final Ge concentration.

![Graph showing the relationship between rms roughness and final Ge% in the graded buffer.](image)

**Figure 3.1** Increase in root mean square surface roughness with increasing Ge content in the graded buffer.

3.2. **Freund's dislocation blocking criterion**

Work hardening occurs in heavily dislocated materials; in this case the graded region may experience work hardening if the dislocation density becomes very high. The
microscopic origin of such work hardening is dislocation interaction. In mismatched interfaces, Freund has shown that a threading dislocation can be blocked by a perpendicular interface misfit dislocation\textsuperscript{121}, since in a single heterostructure they are confined to a single plane. When a threading dislocation approaches an orthogonal

![AFM image](image)

**Figure 3.2** An AFM image of the surface of a SiGe buffer graded to pure Ge showing the cross-hatch pattern and the occasional deep trenches.

misfit dislocation, the effective force (from mismatch stress, in this case) moving the threading dislocation is reduced by the stress field of the orthogonal misfit
dislocation\textsuperscript{121,122}. The stress field from the misfit dislocation decays as $\approx 1/r$ where $r$ is the distance from the misfit dislocation. Thus, there is some area above the misfit dislocation where the orthogonal misfit stress field completely negates the glide stress such that the force on the threading dislocation cannot sustain glide. This happens only over a finite region of the glide plane beyond which the orthogonal misfit dislocation stress decays to low values. This implies that a threading dislocation segment must pass through a restricted channel, $h^*$, formed between the film surface and the decay of the misfit stress field from the interface. Figure 3.3 is plot of normalized channel width, $h^*/h$ as a function of $(h/b)e^*$, where $h$ is the height of the film and $e^*$ is the background strain\textsuperscript{122}. Referring to the plots in Figure 3.3, for a background strain of $e^*$ in a film thickness $h$, $h^*$ is the channel width through which a threading segment must pass to overcome the stress field of the orthogonal dislocation.

The first SiGe buffers used in this study were grown at 900° C and graded at 10% Ge/μm. Under these conditions, the equilibrium critical thickness is $\approx 375$ nm\textsuperscript{57}. This implies that during growth of the graded layer, there is $\approx 375$nm of graded Ge\textsubscript{x}Si\textsubscript{1-x} at the surface that is elastically strained at all times. In these growth experiments the grading rate of 10% Ge/μm was achieved by increasing the Ge content by $\approx 3.33\%$ Ge in steps of $\approx 333$ nm. Hence, each step in Ge is completely strained until the next step in concentration occurs, and a threading dislocation experiences approximately the same force as in a single heterostructure which is 333 nm in thickness. The critical thickness for a graded layer is a strong function of the Ge grading rate and nearly independent of the final Ge% of the graded layer.
Figure 3.3  A graph from Gillard et al.\textsuperscript{122} showing a plot of $h/h^*$ versus $(h/b)e^*$, used to calculate $h^*/h$ ratio for graded SiGe/Si layers. The different curves are for different dislocation combinations. For the strains in our SiGe graded buffers $h^*/h$ always tends to 1, irrespective of the dislocation combination chosen.

Hence, the same critical thickness approximation can be applied to films graded to different final Ge\% (at the same grading rate) in these experiments. The background strain $e^*$ that causes the threading dislocation glide during graded layer growth is, hence, $\approx 0.13\%$ corresponding to the 3.33\%Ge increase per step. Referring to Figure 3.3, the $h^*/h$ ratio in Freund’s blocking model approaches unity under these conditions. Since the channel width, $h^*$, is almost as thick as the epilayer, $h$, the gliding threading segment can easily overcome the strain field and blocking effect of any orthogonal misfit dislocation. However, dislocation pile-ups do form in graded SiGe structures and have been observed. The blocking criterion of a single perpendicular dislocation alone cannot explain the formation of dislocation pile-ups in graded Ge\textsubscript{x}Si\textsubscript{1-x}/Si structures. From this analysis, one
can conclude that the blocking effect of orthogonal misfit dislocations is not large enough to counter the background strain in reasonably thick and/or moderately lattice-mismatched cases. To explain the formation of dislocation pile-ups in these graded structures, some other mechanism of dislocation blocking needs to be invoked.

Figure 3.4  A schematic showing the gliding dislocations interacting with existing dislocations and getting blocked at the trench side-walls.

3.3.  Surface-dislocation interaction model

Initially, some of the deeper regions in the cross hatch pattern can contribute to the blocking action of the gliding threading dislocation segments. Figure 3.4 shows a schematic that explains the possible mechanism of dislocation blocking and subsequent dislocation pile-up formation in graded Ge<sub>x</sub>Si<sub>1-x</sub>/Si structures. Figure 3.4 shows a threading segment of a gliding dislocation interacting and being blocked by the stress
fields of pre-existing groups of orthogonal misfit dislocations. Such groups are known to exist in mismatched structures due to repeated operation of heterogeneous dislocation nucleation sources. The strain fields from such a group create a deeper trough in the cross hatch pattern. With this local decrease in thickness, threading dislocations get blocked since the channel width, $h^*$, can decrease to zero from both the depression in the surface morphology and the stress fields from the orthogonal dislocations. Other gliding segments traveling on the same or parallel $\{111\}$ planes could also be blocked, and previous blocked threading dislocations also aid in subsequent blocking. Such an event can lead to a dislocation pile-up along a depression in the cross hatch pattern.

We note here that very pronounced deep ripple troughs\textsuperscript{118}, surface cusps\textsuperscript{120}, and surface depressions\textsuperscript{123} have been identified as regions with reduced kinetic barriers to dislocation nucleation. Such events occur when the layers are heavily elastically strained (>1\%) as mentioned previously. Recent TEM studies\textsuperscript{124} have revealed that there is a direct correlation between the position of troughs and individual dislocations injected to relieve misfit in InGaAs/GaAs system. However, in slowly graded structures such sharp dislocation sources are not present initially, and the strain is nearly completely relaxed except for a small equilibrium strain at the surface. Thus, dislocation nucleation can not be initially producing the pile-up structures. At higher growth temperatures and continued roughening due to CVD growth, it is not inconceivable that such large surface features contribute to dislocation nucleation. However, it is unlikely that all of the surface trenches that could lead to nucleation would be deeper than the channel width $h^*$. Thus the blocking events must be responsible for dislocation pile-up formation. Using this
hypothesis of dislocation blocking, we can make estimates of when blocking should occur.

![Graph showing the variation of maximum trench depth of surface cross-hatch pattern with increase in final Ge% in the graded layer. Shown also is h* for 10% Ge/µm grading rate. Whenever the maximum trench depth is greater than h*, there is a high probability of dislocation pile-up formation.](image)

Figure 3.5  A graph showing the variation of maximum trench depth of surface cross-hatch pattern with increase in final Ge% in the graded layer. Shown also is h* for 10% Ge/µm grading rate. Whenever the maximum trench depth is greater than h*, there is a high probability of dislocation pile-up formation.

3.4. Predicting dislocation pile-up formation

The experimental data shows that depth of the deepest surface trench from the cross hatch pattern increases with increase in final Ge% of the graded region as shown in
Figure 3.5. The thickness of the channel available for the threading dislocation, $h^*$, is also plotted on the same graph. Note that $h^*$ is a function of grading rate only and not of the final Ge% of the graded region. In cases where the maximum trench depth is greater than $h^*$, dislocation pile-ups can be expected. The farther the "maximum trench depth" point is above the $h^*$ line, the more trenches can block dislocations; hence we expect a higher density of dislocation pile-ups. For each Ge grading rate, a plot such as Figure 3.5 can be constructed. Such plots would allow one to predict the likelihood of dislocation pile-up formation in graded structures. The above analysis, though demonstrated for graded SiGe structures, is applicable to any graded lattice-mismatched heteroepitaxial system.

![Diagram]

Figure 3.6 A schematic diagram illustrating the degenerate nature of interactions between surface morphology and dislocation pile-ups.

The dislocation pile-up formation contributes to further degradation of the surface morphology. Threading segments of gliding dislocations terminate at or near the trench associated with the dislocation pile-up. The surface sites where the dislocations terminate are energetically unfavorable sites for adatoms diffusing on the growth surface. The
growth rate at or near the trench is thereby further reduced. Such an effect increases the trench depths, making more gliding dislocations prone to blockage. The degenerate nature of the interactions of the surface morphology and dislocation pile-up formation is summed up in Figure 3.6. A correlation between rms roughness and dislocation pile-up density for Ge/Ge$_{x}$Si$_{1-x}$/Si(001) samples along the two in-plane <110> directions (to be discussed in the next chapter) agrees with the above analysis.
4. Effect of Miscut Substrates

The integration of III-V/Ge/SiGe/Si requires miscut Si substrates to avoid formation of anti-phase domain boundaries (APBs) in the III-V layer. It was observed that the SiGe graded buffers grown on miscut substrates had a different surface morphology than those grown on on-axis wafers. The reason for this was not known. This chapter reveals the effect of substrate miscut on surface morphology and dislocation pile-up formation\textsuperscript{125}. The substrate miscut aids dislocation interactions and causes the epilayers to tilt. Details of a novel hexagonal dislocation network that was discovered and its effect on epilayer tilt are also discussed in this chapter\textsuperscript{126}.

4.1. Experimental procedure

The samples used in this study were grown by T. Sorsch and E. A. Fitzgerald at Bell Laboratories. Epitaxial films of Ge/SiGe/Si were grown on (001) and (001) 6° off-cut (towards in-plane <110>) n-Si substrates using UHVCVD at 900° C. The films were graded at a constant grading rate of 10% Ge/μm. The grading rate of 10% Ge/μm was achieved by increasing the Ge content by ≈3.33% Ge in steps of ≈0.33 μm. A 2 μm uniform cap layer of pure Ge was grown above the graded region. The top 0.1 μm of the uniform cap layer was p-doped to create a p-i-n structure suitable for EBIC characterization.
The surface morphology of the heterostructures was characterized using SEM and AFM. The rms roughness data was obtained from a number of 100μm x 100μm surface scans using contact mode AFM (Nanoscope III, Digital Instruments Inc.). In miscut samples, the roughness along the two in-plane <110> directions was also characterized. The data were obtained by performing the section analysis routine on several lines along the specific <110> direction on the sample. The dislocation structures were characterized primarily through (001) plan view TEM. The samples for observation were prepared by mechanical polishing from the Si substrate side to about 20 μm followed by argon ion beam milling. For observing the dislocation networks near the top of the graded SiGe region (Ge-rich), the sample was ion-milled primarily from the substrate side until electron transparency was obtained. For characterizing the Si-rich regions of the graded SiGe structure, the sample was milled from both the substrate side and the epilayer side, so that the electron transparent regions would lie in the bottom of the graded SiGe buffer.

EBIC was used to observe electrically active dislocations threading up through the uniform cap layer. As discussed in the previous chapter, dislocation pile-ups can form along deep trenches in the cross-hatch pattern. These pile-ups were good recombination sites for charge carriers and showed a dark contrast along the trenches. The dislocation pile-ups are planar defects and their densities were characterized by the number of intersections per unit length of the sample surface. The density (number/cm) was determined by calculating the number of intersections of the dark contrast lines with random straight lines drawn on the EBIC micrographs.
4.2. Effect on surface roughness

Figure 4.1 is a graph showing the rms roughness for SiGe samples graded to different Ge concentrations. The data includes samples grown on on-axis substrates as well as miscut substrates. There is clear evidence that the substrate miscut drastically reduces rms roughness of the graded buffer at any Ge concentration. For example the rms roughness for the 100% Ge sample grown on an on-axis Si(001) substrate is 210nm. It drops to 50nm when a 6° off-cut Si(001) substrate is used. There are two major effects for growths on miscut substrates that result in reduced surface roughness of the graded buffers.

![Graph showing rms roughness vs Ge concentration]

Figure 4.1 A chart showing the rms roughness of SiGe buffers graded to different final Ge concentrations. Data for both on-axis as well as miscut (001) substrates is shown. The samples are graded to different final Ge concentrations and hence have different thicknesses.

It is known that on miscut substrates, 60° dislocations (that normally lie along the two orthogonal in-plane <110> directions) do not lie exactly along the in-plane <110>
directions. It was observed by Kightley et al.\textsuperscript{127} that in InGaAs layers grown on (001) off-cut (2° towards (010)) GaAs substrates, two 60° misfit dislocations with the same line direction but gliding on different \{111\} planes intersect each other due to the substrate miscut. Figure 4.2 shows a schematic sketch from their paper that depicts the glide of 60° dislocations along a miscut <110> direction. Viewed in plan view the 60° dislocations that normally lie along parallel <110> directions, lie along intersecting lines along the miscut <110> direction as shown in Figure 4.2. We have also observed this in graded SiGe/Si films grown on miscut substrates. Figure 4.3 is a photo-montage of plan-view TEM micrographs depicting a 60° dislocation network in a graded SiGe on an off-cut Si(001) substrate. It is seen that 60° dislocations gliding along the miscut [110] direction tend to have intersecting paths whereas the dislocations gliding along the [\bar{1}10] direction lie parallel to each other. Since the 60° dislocations are not parallel, a nucleation source cannot create long lines of parallel dislocations with the same Burgers vector. Without close, parallel misfit dislocations, the strain fields at any given point above the misfit interface are less than those in the on-axis sample. Hence, rms roughness is reduced for the miscut sample.

In our growth experiments, the above proposition would be true only along one of the two <110> directions, since the miscut was towards a <110> direction. This hypothesis explains the anisotropy in rms roughness along the two <110> directions on the miscut samples (Figure 4.4). The 60° dislocations at each mismatched interface intersect along the miscut <110> direction. Hence, the strain fields along the non-miscut
orthogonal <110> directions are reduced. This translates into lower rms roughness along the non-miscut <110> direction.

![Plan view diagram](image)

**Figure 4.2** The left part of the figure is a schematic sketch from Kightley et al.\textsuperscript{127} showing the glide of 60° dislocations along a miscut <110> direction. The right part of the figure is a schematic of the plan-view depicting intersecting 60° dislocations along the miscut <110> direction.

It was shown by L. Csepregi et al.\textsuperscript{128} that the growth rate for Si surfaces is highest for {001}, lowest for {111} and intermediate for {110}. The cross hatch pattern leads to the formation of planes tilted away from (001) growth surface, as described in the previous section. The surfaces oriented off the (001) have slower growth rates; thus a large differential in growth rates encourages even greater changes in growth rate, forming facets on the surface. Growth on a substrate that is miscut towards <110> implies that the difference in the growth rates along the trench side-walls and the average growth surface
is less compared to growth on an exact (001) surface. Over prolonged growth, the miscut wafer case translates into reduced rms roughness of the growth surface.

Figure 4.3 A photo-montage of plan-view TEM micrographs showing intersecting 60° dislocations along the miscut <110> direction in a SiGe graded buffer grown on an off-cut Si(001) substrate.

A secondary effect that also contributes to the reduced rms roughness in the off-cut samples is the ease of formation of the edge dislocations with in-plane Burgers vector. Such dislocations do not produce as severe strain field inhomogeneties at the growth surface as the mixed 60° dislocations. In addition, if only edge type dislocations are present in a regular array, the strain fields from the neighboring dislocations will quickly
annihilate, thus creating fewer residual strain fields at the surface of the growing epilayer. As will be discussed in a subsequent section, the substrate miscut promotes dislocation interactions that can lead to energetically favorable dislocation reactions forming edge dislocations.

![Graph showing rms roughness and pile-up density](image)

**Figure 4.4** A plot of rms roughness and dislocation pile-up density along the two in-plane <110> directions for Ge/SiGe/Si samples grown on-axis (001) and 6° off-cut (001) substrates.
4.3. Effect on dislocation pile-ups

Intersection of 60° dislocations at the mismatched interfaces as seen in Figure 4.3 implies that it is difficult to form a long wall of blocking stress fields along the miscut <110> direction. Hence a dislocation gliding along the non-miscut <110> direction is less likely to be blocked by stress fields of orthogonal misfit dislocations as discussed in the previous chapter. In addition, the reduced surface roughness due to the same effect means that there will be fewer deep trenches (greater than h*) that are capable of blocking gliding threading dislocations. Figures 4.5a and 4.5b are plan-view EBIC images of 100% Ge graded samples grown on Si(001) and Si(001) off-cut substrates respectively. The dark bands are regions of heavy recombination activity caused by closely spaced threading dislocations trapped in a pile-up. The dark spots are individual threading dislocations. Comparing the EBIC images with SEM images clearly shows that the pile-ups form along deep trenches as predicted by our dislocation pile-up formation model. There is a substantial reduction in dislocation pile-up density in the 100% Ge sample grown on the off-cut substrate, as expected from the previous discussion. As shown in Figure 4.5, there is also clear anisotropy in the dislocation pile-up density along the two in-plane <110> directions for the sample grown on the off-cut substrate. The anisotropy in dislocation pile-up density follows the anisotropy of rms roughness. Reduced pile-up density also reduces surface roughness since some of the spatially inhomogeneous strain fields are eliminated.
Figure 4.5  Plan-view EBIC images from Ge/SiGe/Si samples grown on (a) on-axis and (b) off-cut Si(001) samples.
4.4. Novel dislocation structure

It is well-known that low-mismatch, graded SiGe/Si(001) structures typically relax by the formation of 60° dislocations that glide down the various {111} planes to the (001) interface. The straight misfit segments of the 60° dislocations that relieve misfit lie along the two in-plane <110> directions at the (001) interface. Figure 4.6a shows one such array of 60° dislocations existing in a (001) interface in the Si-rich region of the graded SiGe structure. Figure 4.6b shows a similar TEM micrograph taken from the Ge-rich region of the graded structure grown on a (001) off-cut substrate. A hexagonal network of dislocations was observed. Several bright field TEM images obtained under different "two-beam" conditions were used to perform a \( \mathbf{g} \cdot \mathbf{b} \) analysis of the network. By analyzing the dislocation contrast in images formed using different \( \mathbf{g} \) beams and guessing the possible reactions at dislocation nodes we were able to isolate the different Burgers vectors that make up the network. Figures 4.7(a-d) are bright field TEM micrographs of a region with the hexagonal dislocation network imaged using different diffracted beams. The analysis revealed that the network was made up of dislocations of the type \( \frac{1}{2}<110> \), \( \frac{1}{2}<\bar{1}0> \) and \( <100> \), all with in-plane Burgers vectors. Each node in the hexagonal network was formed by a \( <100> \) edge type dislocation and two reacting \( \frac{1}{2}<110> \) edges.

Such dislocation networks have also been observed by Hedges et al.\textsuperscript{129} and Amelinckx\textsuperscript{130} in silver bromide (AgBr) and potassium chloride (KCl) crystals respectively in the 1950's. To our knowledge, this is the first time that such a dislocation structure has been observed in heteroepitaxial diamond cubic thin film growth. The reaction sequence that causes the 60° dislocation network to transform into this hexagonal edge network is
probably as follows. Two 60° dislocations with Burgers vectors of the type \( \frac{1}{2}<101> \) and \( \frac{1}{2}<011> \) can glide out of the (001) interface and react to form an edge dislocation of the type \( \frac{1}{2}<110> \). Such reactions are favored since there is a large reduction in strain energy due the \( b^2 \) criterion. The \( \frac{1}{2}<110> \) type edge dislocation that forms now lies in the (001) plane which is not a glide plane for the diamond cubic system. The dislocation is sessile and can only move through a climb process or under extremely high stresses. The former is more probable, since the stress levels from slow grading (5-20% Ge/\( \mu \)m) are fairly low (\( \approx 0.01 \)). As the Ge content of the graded layer increases, the melting point of the Ge\(_x\)Si\(_{1-x}\) alloy decreases (\( T_{m, Ge}\approx 1425^\circ \) C, \( T_{m, Ge}\approx 940^\circ \) C, Ge and Si form a isomorphous system). Since the growth temperature is constant, the layer approaches the melting point as the SiGe buffer is graded to pure Ge. Vacancy diffusion increases as the growth temperature approaches the melting point of the alloy and climb mechanisms, which occur through vacancy diffusion, become activated. Thus the sessile edge dislocations can climb out of the (001) interface more easily as the Ge content of the graded layer increases. Edge dislocations of the type \( \frac{1}{2}<110> \) (formed by reactions between 60° dislocations) can now further react as shown:

\[
\frac{1}{2}[110] + \frac{1}{2}[\bar{1}0] \rightarrow [010]
\]  
(4.1)

\[
\frac{1}{2}[110] + \frac{1}{2}[\bar{1}0] \rightarrow [100]
\]  
(4.2)
Figure 4.6  Plan view TEM micrographs of (a) Si-rich region of the graded structure showing an orthogonal array of 60° dislocations, (b) Ge-rich region of the graded structure showing a hexagonal network of edge dislocations.
Figure 4.7 A series of plan view TEM micrographs of the same region as in Figure 4.6b, taken using different g beams for Burgers vector analysis of the hexagonal network. (a) g=040, (b) g=400, (c)g=220, (d) g=−220.

Such reactions, though energetically neutral using the elasticity theory ($b^2$ criterion), are favored since it leads to energy lowering due to the sharing of atomic misfit in the dislocation cores. Amelinckx claims that very little external driving force is required for such reactions to proceed. In a Ge-rich SiGe alloy grown at an average temperature of $0.8T_m$, it is not difficult to imagine that such reactions are feasible. From an orthogonal
dislocation grid made up of edge dislocations of the kind $\frac{1}{2}<110>$ and $\frac{1}{2}<\bar{1}10>$, reactions such as (4. 1) and (4. 2) can lead to a hexagonal network as observed in Figure 4.6b. Figure 4.8 shows a schematic of the sequence of dislocation reactions that form the hexagonal dislocation network. In the high Si regions of the graded SiGe structure, the difference in the growth temperature and the melting point of the alloy is large (the average growth temperature is $\approx 0.5 T_m$) and therefore dislocation climb is minimal. In this case, the 60° network that originally forms is unable to overcome the kinetic barrier to climb (Figure 4.6a).

TEM observations of the graded regions for the samples grown on exact (001) orientation revealed that the hexagonal network of dislocations do not form easily. In off-cut substrates, two 60° dislocations gliding on different {111} planes would intersect since their line directions in the (001) plane were off the exact $<110>$ direction. Such intersections of 60° dislocations are favorable in their reaction to form an edge type dislocations. The off-cut of the substrate increases the probability that a 60° dislocation would find the right 60° to react with. Thus, for samples on the off-cut substrates it would be easier for the $\frac{1}{2}<110>$ type edge dislocations to form. The presence of more $\frac{1}{2}<110>$ type edge dislocations implies that more reactions could occur and it is easier to form the low energy hexagonal network of dislocations. For samples grown on the (001) exact substrate, the formation of $\frac{1}{2}<110>$ type edges is more difficult and hence the formation of $<100>$ dislocations is more difficult.
Figure 4.8 A schematic showing the sequence of probable dislocation reactions that result in the formation of the hexagonal dislocation network.

Since all the Burgers vectors of the network lie in the (001) plane, they are 100% efficient in relieving the misfit strain unlike the 60° dislocations which are only 50% as efficient. Such a dislocation network is probably the lowest energy configuration possible at a mismatched (001) interface in diamond cubic materials. The new dislocation structure offers new degrees of freedom in designing relaxation processes. 60° dislocations are advantageous, since their introduction can be controlled at relatively low temperatures. However, this work suggests that the subsequent elimination of the "extra" Burgers vector components is possible by forming the hexagonal dislocation network.
4.4.1. **Dislocation network energy calculations**

We have modeled the energetics of formation of the hexagonal network from a square \(1/2<110>\) edge network, which in turn forms from a 60° orthogonal dislocation array. The reactions of 60° dislocations to form \(1/2<110>\) type edge dislocations is energetically favored from the \(b^2\) criterion. However, the energy of the reacting \(1/2<110>\) edges is equal to the <100> type product using this rule. We have estimated the line energies and dislocation node energies for the different configurations. Our calculations indicate that the hexagonal network forms to convert the high energy four-fold nodes of the orthogonal network into three-fold nodes of the hexagonal network. Figure 4.9 is a plot of the total network energy per unit area for the three dislocation network configurations as a function of plastic strain \((\varepsilon=b\cdot\rho_m\text{, where }\rho_m\text{ is the misfit dislocation density})\). It is seen that the hexagonal dislocation network has the lowest energy at \(\varepsilon=0.0012\), the strain from a single-step increase in Ge concentration during the graded buffer growth (3.33% Ge jump every 0.33μm). Appendix 3 contains the details of the dislocation network energy calculations.

4.5. **Epilayer tilt study**

To study the epilayer tilt in graded SiGe/Si the Ge/SiGe/Si samples were characterized using triple crystal X-ray diffraction. Figure 4.10a shows a (004) reciprocal space map (RSM) of a Ge/SiGe/Si(001) 6° off-cut sample with the diffraction plane perpendicular to the miscut [110] direction. The y-axis of the RSM, \(q_{\text{<001>}}\), is proportional
to the reciprocal lattice constant along the [001] direction. The x-axis, $q_{<110>}$, represents
the in-plane reciprocal lattice constant along a $<110>$ direction. When the epilayer does

![Graph showing dislocation network energy vs. plastic strain relieved](image)

**Figure 4.9** A plot of total dislocation network energy as a function of plastic strain relief for the three configurations.

not tilt with respect to the substrate, the substrate peak and the epilayer peak line up along
the same $q_{<110>}$ value. In Figure 4.10a it is seen that the substrate Si peak and the epilayer
Ge have approximately same $q_{<110>}$ value indicating that there is no epilayer tilt about the
miscut [110] direction. This observation is confirmed by the (224) RSM of the same
sample under a similar diffraction configuration.
Figure 4.10  Reciprocal space maps of Ge/SiGe/Si(001) 6° miscut sample. In (a) the diffraction plane is perpendicular to the miscut [110] direction. In (b) the diffraction plane is parallel to the miscut [110] direction.
Measurement of $a_l$ and $a_\perp$ of the Ge peak using the (224) RSM indicates that the graded layers are almost completely relaxed. Figure 4.10b shows a (004) RSM of the same sample as in Figure 4.10a, with the diffraction plane parallel to the miscut [110] direction. It is seen that the graded layer is tilted away from the Si(001) 6° off-cut peak in such a way that it reduces the epilayer miscut. The net tilt of the graded SiGe layer with respect to the Si substrate is $\approx 1.6^\circ$. Similar measurements were made on Ge/SiGe/Si samples grown on an on-axis Si(001) substrate. The RSMs along both the $<110>$ directions were similar to the RSM on the miscut substrate with the diffraction plane along the non-miscut direction. There was no epilayer tilt along either of the $<110>$ directions for the on-axis samples, as expected.

We determined the epilayer tilt as a function of the graded layer composition for the Ge/SiGe/Si sample grown on the miscut substrate. Figure 4.11 is a plot of the epilayer tilt as a function of Ge concentration in the graded buffer. The rate of epilayer tilting is more or less uniform until about 71% Ge, where it decreases from $\approx 0.017^\circ/\%$Ge to $\approx 0.011^\circ/\%$Ge.

The component of the Burgers vector of the 60° dislocation perpendicular to the interface, $b_z$, is responsible for the epilayer tilt and therefore a change in the tilting corresponds to a change in the Burgers vector population. The 60° dislocation that generally forms to reduce misfit in low mismatch systems has $b_z$ oriented either "up" or "down" depending up on its inclination to the (001) growth surface. In an on-axis sample there are equal number of 60° dislocations with opposite tilt components such that the epilayer does not have a net tilt. An asymmetric population of dislocations with opposite
tilt components causes the epilayer to tilt away from the substrate orientation. If it is assumed that the graded layers are relaxed entirely by $60^\circ$ dislocations, one can determine the number of dislocations with either orientation of $b_2$ as a fraction of the total number of dislocations, knowing the rate of epilayer tilt. In the sample graded up to 100%Ge we find that 78% of dislocations are "tilt-up" below 71%Ge and above 71%Ge, 65% are "tilt-up". This indicates that there must be a variation in the Burgers vector population arising from a change in the dislocation structure in the higher Ge regions of the graded structure.

![Graph](image)

**Figure 4.11** A plot of the epilayer tilt as a function of Ge in the graded buffer for a Ge/SiGe/Si sample grown on a $6^\circ$ miscut substrate. The RSM, from which this data was obtained was created with the diffraction plane parallel to the miscut <110> direction.
The novel hexagonal dislocation network that we observe in the Ge-rich regions of the graded buffer might be responsible for this tilt behavior. All the dislocations in the hexagonal network have in-plane Burgers vectors, with no tilt component. Hence, they do not contribute to the tilt of the epilayer. The hexagonal network occurs only in those areas of the interface where the right kind of \( \frac{1}{2}<110> \) dislocations are found. This explains why there is a decrease in the tilt rate on average without the tilt rate going to zero, which would be the case if the hexagonal network were to form everywhere. This explains the reduction in the tilting rate of the epilayers rich in Ge (\( \geq 70\% \)) observed in Figure 4.11.
5. Optimized Relaxed Graded Buffers

5.1. Motivation

III-V/SiGe/Si integration requires high quality SiGe layers with high Ge contents and pure Ge layers. For example direct band-gap InGaP which can be used to fabricate LEDs and lasers luminescent in the yellow-orange color regime is lattice-matched with Ge$_{0.7}$Si$_{0.3}$. Pure Ge is closely lattice-matched to GaAs, which can be used to fabricate high efficiency solar cells, AlGaAs-GaAs red lasers and LEDs and high speed MESFETs. Finally Ge layers can be used to fabricate photodetectors sensitive in the 1-1.7 μm wavelength regime. All of these applications require Ge-rich SiGe layers with low threading dislocation densities.

As seen in Chapters 3 and 4, growth of graded buffers to high Ge concentrations leads to an increase in surface roughness and concomitant formation of dislocation pile-ups. To compensate for the dislocations trapped in pile-ups new dislocations nucleate, leading to an overall increase in threading dislocation density. The monotonic increase in threading dislocation density with increasing Ge concentration in the graded buffer is attributed to this effect. The surface roughness needs to be maintained at a low value to prevent deep trenches and dislocation pile-ups from forming. One way to achieve this could be through an intermediate planarization step. There are other materials challenges too, in grading SiGe buffers to high Ge concentrations. The difference in the coefficients of thermal expansion for Si and Ge results in tensile thermal mismatch when cooling the
structure from the growth temperature to room temperature. This can cause residual tensile stresses or even micro-cracking in the epilayers. Most III-V compounds have larger coefficients of thermal expansion than Si or Ge. Hence the growth of III-V compounds on SiGe or Ge layers intensifies the thermal mismatch problem. The Ge source gas, GeH₄, can dissociate in the gas phase under high partial pressures and growth temperatures, creating particles that are incorporated in the epilayer. The particulate contamination is a more serious issue when the GeH₄ partial pressure is higher than the SiH₄ partial pressure, which is the case when Ge-rich SiGe layers are grown. The optimized relaxed graded buffers were designed to address these different materials challenges in the growth of Ge-rich SiGe buffer layers.³³⁶

![Figure 5.1](image)

*Figure 5.1*  A schematic of the optimized relaxed graded buffer structure.
5.2. **Growth of optimized relaxed graded buffers**

Our first attempts to grow high quality Ge layers on graded SiGe buffers were experiments in varying the obvious process variables—growth temperature, growth pressure and grading rate. The first high quality graded SiGe/Si buffers, grown by Fitzgerald et al., were generally grown at 900° C, 500mT growth pressure and 10%Ge/μm grading rate. The Ge/SiGe/Si samples grown under these conditions (the subject of the study in chapter 4), will henceforth be referred to as Sample A. As a first experiment, we reduced the growth temperature to 750° C and the grading rate to 5% Ge/μm in an attempt to reduce dislocation nucleation. We also reduced the growth pressure to 250 mT to achieve better growth uniformity across a 100 mm diameter wafer. The SiGe layers were graded to pure Ge over 20μm. A 1.5 μm Ge cap layer was grown on top of the graded buffer. This sample will be referred to as Sample B. As shall be discussed in a later section sample B was a small improvement over sample A in terms of dislocation density, but had a high particle and micro-crack density.

The design of optimized relaxed buffers relied on the knowledge base from samples A and B. Figure 5.1 shows a schematic of a Ge layer on an optimized relaxed buffer (ORB). The sample was graded at 10% Ge/μm to Si_{0.5}Ge_{0.5} at 750° C and 250 mT growth pressure. A 3 μm uniform layer of Si_{0.5}Ge_{0.5} was grown on top of the 50% Ge graded buffer. The top 0.6 μm of the Si_{0.5}Ge_{0.5} cap layer was then planarized using chemical mechanical polishing (CMP). A 0.5 μm thick Si_{0.5}Ge_{0.5} layer was regrown after a carefully designed clean. A second graded buffer was grown from Si_{0.5}Ge_{0.5} to Si_{0.3}Ge_{0.7}
under similar conditions as the initial grade from 0 to 50 %Ge. At this point the temperature and the growth pressure in the UHVCVD reactor were dropped to 550° C and 30 mT respectively. The growth of the graded buffer was continued from 76% Ge to 92% Ge. A jump in Ge concentration was introduced at this point. A 1.5 µm uniform Ge layer was grown on top of the 92% Ge graded buffer. The significance of all the process modifications are detailed in the next few sections. Apart from samples graded to pure Ge, optimized relaxed buffers were also graded to different final concentrations, such as 50% Ge and 70% Ge, with CMP steps at 25%, 35%, etc. Data from these samples will also be presented along with the data from samples, A, B and C.

![Diagram of Si$_{0.5}$Ge$_{0.5}$ graded layer](image)

**Figure 5.2** A schematic depicting the effect of CMP on the surface of a 50% Ge graded buffer. The CMP eliminates deep trenches that form pile-ups and trapped dislocations can glide up on regrowth.

### 5.2.1. Chemical mechanical polishing and pile-ups

Table 5.1 shows a summary of the materials characterization results for samples A, B and C. All three samples are Ge layers grown on different SiGe graded buffers on Si
(001) miscut substrates. Sample A, graded at 10%Ge/\(\mu\)m, has a threading dislocation density \(>10^7 \text{ /cm}^2\), which agrees with the commonly observed increase in threading dislocation density upon grading to high Ge concentrations. It was expected that lowering the grading rate to 5%Ge/\(\mu\)m (sample B) would lead to a decrease in the threading dislocation density, since the driving force for dislocation nucleation (strain/unit volume) is much lower. However, the threading dislocation density was still in the \(10^7\text{/cm}^2\) range, indicating that the deleterious interactions between surface features and gliding dislocations that form pile-ups are dominating effects when one grows high Ge content SiGe relaxed buffers. As seen in Chapter 4, growth on miscut substrates leads to a reduction in surface roughness and dislocation pile-up density. However, the pile-ups are not completely eliminated and hence an increase in threading dislocation density with the final Ge % of the graded layer is still observed. This issue was actively addressed in the growth of sample C.

An intermediate CMP step at the 50% Ge layer liberates pre-existing dislocations trapped in the pile-ups and obviates the need to nucleate new dislocations. Figure 5.2 shows a schematic of dislocation pile-ups that would be mobile in the absence of surface "barrier" trenches that the CMP step eliminates. Hence, sample C, which is effectively a 10%Ge/\(\mu\)m SiGe buffer graded to pure Ge, has a much lower threading dislocation density than sample A or B of \(2.03 \pm 0.113 \times 10^6\text{/cm}^2\). Figure 5.3 shows the effect of CMP on the final threading dislocation density. Data for samples A, B and C, as well as other graded buffer samples is shown. It is clear that there is a substantial improvement in the overall threading dislocation density due to the CMP and regrowth process. The
biggest improvement to the overall threading dislocation density is in the dislocations trapped in pile-ups. The CMP step reduces the dislocation pile-up density as well as the number of dislocations trapped in unit length of the pile-up as shown in Table 5.2. Typically, the rms roughness of any graded buffer after a CMP step was \( \approx 5 \) nm. With no deep trenches to block their motion, dislocations from existing pile-ups are mobile once again. This depletes existing pile-ups of dislocations. The reduced density of dislocations per unit length of pile-up in the ORB samples is probably due to this effect. The dislocations that were liberated from the pile-ups can participate in the subsequent relaxation process and have a higher chance of annihilation by encountering a dislocation with opposite Burgers vector.

<table>
<thead>
<tr>
<th></th>
<th>Sample A</th>
<th>Sample B</th>
<th>Sample C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threading dislocation density (#/cm(^2))</td>
<td>( &gt;10^7 )</td>
<td>( 1\pm0.1 \times 10^7 )</td>
<td>( 2.1\pm0.2 \times 10^6 )</td>
</tr>
<tr>
<td>RMS roughness (nm)</td>
<td>47</td>
<td>35.9</td>
<td>24.2</td>
</tr>
<tr>
<td>Crack density (#/cm)</td>
<td>0</td>
<td>47(\pm5)</td>
<td>0</td>
</tr>
<tr>
<td>Particle density (#/cm(^2))</td>
<td>600(\pm40)</td>
<td>1250(\pm100)</td>
<td>150</td>
</tr>
</tbody>
</table>

**Table 5.1** Materials characterization data from samples A, B and C.

The surface roughness data for samples A, B and C (Table 5.1) is predictable. Sample A graded at 10%Ge/\( \mu \)m has the highest rms roughness. Sample B, graded at
<table>
<thead>
<tr>
<th>Sample</th>
<th>Pile-up density (#/cm)</th>
<th>Threads in unit pile-up length (#/cm)</th>
<th>$\rho_{td}$ from pile-ups only (#/cm$^2$)</th>
<th>$\rho_{td}$ from field only (#/cm$^2$)</th>
<th>Total $\rho_{td}$ (#/cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30%Ge on regular graded buffer (UHV_67)</td>
<td>17.5 ± 1.5</td>
<td>5.2 ± 0.6 x 10$^3$</td>
<td>9.1 ± 0.09 x 10$^4$</td>
<td>2.77 ± 0.2 x 10$^5$</td>
<td>3.68 ± 0.2 x 10$^5$</td>
</tr>
<tr>
<td>50% Ge on regular graded buffer (UHV_18)</td>
<td>60.4 ± 7.2</td>
<td>5.83 ± 0.5 x 10$^4$</td>
<td>3.52 ± 0.03 x 10$^6$</td>
<td>2.73 ± 0.1 x 10$^6$</td>
<td>6.25 ± 0.13 x 10$^6$</td>
</tr>
<tr>
<td>50% Ge on ORB, CMPed at 35% Ge (UHV_61)</td>
<td>10.87 ± 1.5</td>
<td>2 ± 0.6 x 10$^4$</td>
<td>2.17 ± 0.09 x 10$^5$</td>
<td>8.3 ± 0.4 x 10$^5$</td>
<td>1.05 ± 0.05 x 10$^6$</td>
</tr>
<tr>
<td>50% Ge on ORB, CMPed at 25% Ge (UHV_60)</td>
<td>12.3 ± 1.2</td>
<td>3.4 ± 0.4 x 10$^4$</td>
<td>4.19 ± 0.05 x 10$^5$</td>
<td>4.43 ± 0.21 x 10$^6$</td>
<td>4.85 ± 0.22 x 10$^6$</td>
</tr>
<tr>
<td>70% Ge on ORB, CMPed at 35% (UHV-46)</td>
<td>38.6 ± 4</td>
<td>2.15 ± 0.5 x 10$^4$</td>
<td>8.3 ± 0.2 x 10$^5$</td>
<td>3.14 ± 0.2 x 10$^6$</td>
<td>3.97 ± 0.22 x 10$^6$</td>
</tr>
<tr>
<td>100% Ge on ORB, CMPed at 50% Ge (UHV_18) Sample C</td>
<td>44.1 ± 2.4</td>
<td>1.04 ± 0.14 x 10$^4$</td>
<td>4.58 ± 0.03 x 10$^5$</td>
<td>1.57 ± 0.11 x 10$^6$</td>
<td>2.03 ± 0.113 x 10$^6$</td>
</tr>
</tbody>
</table>

**Table 5.2** A table showing the details of the contribution of threading dislocations from pile-ups and from the field.
5%Ge/μm, has a lower roughness since the effect of the dislocation strain fields is distributed over a larger material volume. In sample C, the effect of an intermediate CMP step translates into the lowest surface roughness of the three samples.

Table 5.3 lists the details of a typical CMP step in the ORB process. After the actual CMP, the samples were cleaned using a standard post-CMP clean process that uses NH₄OH, de-ionized water, etc. They were then soaked in dilute HF solution for about 10 minutes to dissolve any residual SiO₂ particles from the CMP slurry. The samples were then cleaned in a piranha solution (1 part H₂O₂ + 3 parts H₂SO₄) followed by a 1 minute dilute HF dip. The piranha solution dissolves Ge, hence depending on the Ge content of the buffer, the cleaning time was varied. Typically, a CMPed 50% Ge layer was cleaned by two alternating 3 minute piranha clean and 1 minute HF dip steps. The piranha solution dissolves and oxidizes a few monolayers of SiGe and the HF dip dissolves the oxide. Thus at the end of the cleaning procedure, a fresh SiGe surface was exposed for epitaxial growth. The cleaning step is critical to ensure good quality epitaxial regrowth after CMP.

5.2.2. Gas phase nucleation of germane

Supersaturation in the gas phase can result in gas phase nucleation of reactant gases in CVD. In the growth of Ge from GeH₄, it is easy to achieve supersaturation due to its low equilibrium vapor pressure (10⁻¹⁰ Pascals at 600° C)¹³⁷. It has been shown that gas phase nucleation of GeH₄ depends exponentially on temperature and increases with increasing growth pressure¹³⁸. When grading to high Ge concentrations, the GeH₄/SiH₄
ratio in the reactor increases and so does the frequency of gas phase nucleation events that form particles. To reduce particulate contamination, during the growth of sample C, the growth temperature and pressure were both reduced in the high Ge regions (>76% Ge) of the graded buffer, resulting in much lower particle counts than samples A and B.

<table>
<thead>
<tr>
<th>Down force</th>
<th>3.5 psi</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quill speed</td>
<td>25 rpm</td>
</tr>
<tr>
<td>Table speed</td>
<td>25 rpm</td>
</tr>
<tr>
<td>Slurry 1</td>
<td>100 ml/min</td>
</tr>
<tr>
<td>Slurry 2</td>
<td>0 ml/min</td>
</tr>
<tr>
<td>Back pressure</td>
<td>1 psi</td>
</tr>
</tbody>
</table>

**Table 5.3** A list of the typical CMP conditions used for polishing 25% Ge and 50% Ge graded buffers.

The lowering of the temperature and pressure is fortunately consistent with the goal of incorporating compressive unrelaxed mismatch stress. As shown schematically in Figure 5.1, during the growth of sample C, the growth temperature was reduced to 550° C and the growth pressure to 30 mT at 76% Ge in the graded buffer. The disadvantage in reducing the growth temperature and pressure is a reduction in epilayer growth rate, which prolongs the growth process.
Figure 5.3  A graph showing the threading dislocation density as a function of final Ge % in the graded buffer for different samples. The data points shown with filled diamonds were grown on regular graded buffers. The samples represented by filled squares had an intermediate CMP step as indicated. Data for samples A, B and C is also shown on the graph. One of the samples at 50%Ge that was p++ doped shows a higher threading dislocation density which we believe is due to reduced dislocation velocity.

For example, the growth rate for Ge_{0.76}Si_{0.24} falls from 7.9 Å/sec to 2.4 Å/sec when the growth temperature and pressure are dropped from 750° C, 250 mT to 550° C, 30 mT respectively in the growth of sample C. Sample B has a higher particle density than sample A since the graded buffer thickness in sample B is twice that in sample A due to
the slower grading rate. This means that sample B was exposed to more gas-phase nucleation events than sample A.

5.2.3. Thermal mismatch problem

Ge has a higher thermal coefficient of expansion than Si at both the growth temperature of sample C ($\alpha_{Si}=3.55 \times 10^{-6}/K$, $\alpha_{Ge}=7.66 \times 10^{-6}/K$ at 750° C) and room temperature ($\alpha_{Si}=4 \times 10^{-6}/K$, $\alpha_{Ge}=5.7 \times 10^{-6}/K$ at 25° C). As the graded structure is cooled from the growth temperature to room temperature the Ge-rich layers are tensilely strained relative to the Si-rich layers leading to micro-cracking and/or unwanted residual stresses. In sample B, the estimated tensile thermal mismatch strain is $\approx 2 \times 10^{-3}$ which led to micro-cracking. In sample C, the Ge-rich regions (76%-100% Ge) of the graded buffer were grown at 550° C which minimizes the thermal mismatch ($\epsilon=\Delta\alpha\cdot\Delta T$) upon cooldown. Additionally, the faster grading and the jump in concentration from 92% to 100%Ge incorporates sufficient metastable compressive strain to offset the tensile thermal mismatch strain. Sample A, which was also graded at 10%Ge/µm, did not experience cracking since the total volume of thermally mismatched material is less compared to sample B. Although sample A was crack-free, sample C grown on the optimized relaxed buffer is superior for III-V/Ge/Si integration. The metastable compressive strain in the Ge-rich layers (as indicated by X-ray diffraction results) implies that the Ge pseudo-substrate is robust enough to handle small tensile stresses due to the additional thermal mismatch from III-V growth.
5.3. Epilayer tilt in optimized relaxed buffers

All optimized relaxed buffer samples were grown on Si(001) substrates miscut towards an in-plane $<110>$ direction. Hence they were expected to exhibit epilayer tilt as observed in miscut samples in chapter 4. Figure 5.4 is a plot of the tilt behavior of samples A, B and C determined from (004) RSMs with the diffraction plane parallel to the miscut $<110>$ direction. Widely different tilt behavior is observed in these samples. All three samples tilt to the same extent, $\approx 0.3^\circ$ up to 30% Ge. The tilt in the higher Ge % layers seem to be strongly affected by the growth process variables. Sample A, which was grown at 900$^\circ$ C and graded continuously at 10% Ge/μm, shows a monotonically increasing tilt which slows down beyond about 75% Ge. This behavior was attributed to the change in the dislocation structure (chapter 4). Sample B, which was grown at 750$^\circ$ C and graded continuously at 5% Ge/μm actually stops tilting beyond 30% Ge and begins to tilt again after $\approx 70$% Ge. Sample C, which is the optimized graded buffer sample, tilts in the opposite direction beyond 30% Ge. The tilt recovers at $\approx 70$% Ge and the layers start tilting in the same direction as samples A and B.

At around 25%Ge, the surface roughness in the graded buffers increases and the long dislocation pile-ups begin to form. The change in the tilt behavior in these samples at this Ge% might be related to the formation of pile-ups. At this point the observed tilting behavior is not clearly understood. More tilt experiments and analyses are necessary.
Figure 5.4  A graph showing the tilting behavior of Ge layers grown on different graded SiGe buffers. All samples were grown on Si(001) substrates off-cut towards an in-plane <110> direction.
6. High Quality Germanium Photodetectors

Ge-based diodes can be used as high speed and high quantum yield photodetectors in the 1-1.6 \( \mu \text{m} \) range for optical communications\(^{100,139,140,141}\) and for Si-based optoelectronics applications. Uniform growth of Ge/Si leads to the formation of a high density of threading dislocations due to the large lattice mismatch (\( \approx 4\% \)) between Si and Ge. The defects adversely affect the dark current and hence the noise factor in photodiodes. Initial attempts to fabricate high quality Ge photodiodes on Si substrates have involved uniform Ge growth on Si substrates\(^{142}\) or fast graded SiGe buffer layers\(^{96}\). We have used optimized relaxed graded buffers, described in the previous chapter, to grow high quality Ge layers on Si substrates. This chapter details the fabrication and device characterization of Ge photodiodes built on optimized relaxed buffers on Si substrates\(^{143}\). The goal of this project was two-fold. First we wanted to prove that a high quality photodetector in the \( \lambda=1-1.7 \ \mu\text{m} \) range could be integrated on a Si substrate. Secondly, we wanted to correlate the material quality of the optimized relaxed buffers with electronic properties.

6.1. Fabrication details

Figure 6.1 shows a schematic of the Ge mesa photodiode. Both contacts to the diode are on the top and the entire structure is in the Ge layer on top of the optimized relaxed buffer. The Ge layers were in-situ doped with PH\(_3\) and B\(_2\)H\(_6\) to form the \( n \) and \( p \)
layers respectively. The persistent PH$_3$ in the UHVCVD reactor resulted in a graded $n$ and abrupt $p$ junction. The doping profile was confirmed through spreading resistance characterization of the junction and the peak $p$ and $n$ doping was found to be 1.18 x $10^{18}$/cm$^3$ and 1.3 x $10^{19}$/cm$^3$ respectively. Note that the dopant concentrations calculated from the spreading resistance data assume a carrier mobility equal to that of Si. Since the mobilities of Si are less than that of Ge, the reported carrier concentrations are higher than the actual values for Ge layers. Using resistivity versus carrier concentration plots for Si and Ge at room temperature$^{144}$, we determined the $\mu_{e,Ge}/\mu_{e,\text{Si}}$ and $\mu_{p,Ge}/\mu_{p,\text{Si}}$ at different doping levels. These ratios were used to correct the carrier concentration values supplied by the spreading resistance vendor for each point across the junction. Figure 6.2 is a depth profile of net doping ($N_D-N_A$) after the mobility correction.

The contacts to the $n$-Ge layer were made by etching and patterning different-sized square mesas with sides ranging from 95 $\mu$m to 250 $\mu$m. The $p$ contact was patterned on top of the mesas. The contacts to both the $p$ and $n$-Ge were Ti/Pt. The first mask level (GR2) was used to pattern photoresist to protect mesas while etching. The Ge layers were wet-etched using a dilute nitric acid and hydrofluoric acid chemistry (4:2:1::HNO$_3$;H$_2$O:1% HF). This etching chemistry was modified from a Ge etchant reported in the literature$^{145}$. There are reports of other chemistries for etching Ge in the literature$^{146,147}$ also. The typical Ge etch rate was $\approx$0.5$\mu$m/minute. It was found that the etch rate was very sensitive to etchant composition and agitation.

The second step in the diode fabrication was a blanket SiO$_2$ deposition. About 5000Å of SiO$_2$ was deposited by low temperature (85°C) plasma CVD using SiH$_4$ and O$_2$
as the source gases. The oxide is to ensure electrical isolation of the contacts. Next the resist was patterned using mask SP1 to open up contact windows in the oxide. The oxide in the open windows was etched using a 7:1 buffered oxide etch. The plasma oxide etching rate using buffered oxide etch is \( \approx 500\text{Å/sec} \).

The next step in the process was to define regions for metallization and lift-off using an image reversal technique. An image reversal resist was used to define the contacts in the oxide windows and bond pads. 500Å of Ti followed by 2500Å of Pt was deposited using an e-beam thin film deposition system. The metal on the resist was lifted off by agitation in acetone, leaving behind the contacts and the bond pads. Figure 6.3 is a optical micrograph of the a 180 \( \mu \text{m} \) device showing the mesa and the contacts.

![Diagram](image)

**Figure 6.1**  A schematic cross-section of the mesa Ge photodiode fabricated on an optimized relaxed graded SiGe buffer on Si.
A graph showing the net doping profile across the p-n junction. Note the graded n-Ge layer caused by persistence of PH$_3$ in the reactor.

6.2. Device characterization

6.2.1. I-V measurements

Figure 6.4 shows the room temperature I-V characteristics of Ge photodiodes with different mesa areas. At low forward voltages (<0.3V) the diodes exhibit an ideality factor of n=1.1, with the slope of the I-V curve decreasing at higher biases due to high series resistance. A series resistance of $R_s=26\ \Omega$ was observed for the larger diodes (250
μm). The 95μm diodes had a larger $R_t=55 \ \Omega$ probably due to the smaller $p$-contact area on top of the mesa. The reverse current approximately scales with the active area of the device, indicating that the leakage current is primarily from the bulk of the device rather than from surface or edge effects. This behavior is not unexpected since the reverse current from diffusion processes is expected to be large due to the small bandgap of Ge. Under a reverse bias of -1 V the reverse current densities range from $J_t=0.15\text{-}0.22 \ mA/cm^2$ for different sized devices. These values are at least 2 orders of magnitude lower than previously reported dark currents of $\approx10 \ mA/cm^2$\textsuperscript{96} and $\approx50 \ mA/cm^2$\textsuperscript{142} at -1 V for Ge diodes integrated on Si substrates.

Figure 6.3 A Nomarski optical microscope image of a 180 μm mesa diode showing the top and the bottom contacts.
Figure 6.4 I-V characteristics of different sized Ge diodes integrated on an Si substrate.

The theoretical $J_s$ for Ge $p$-$n$ diodes was calculated from the doping profile of the diodes. The mobilities $\mu_{n,Ge}$ and $\mu_{p,Ge}$ for peak doping levels of $N_D = 1.18 \times 10^{18}$/cm$^3$ and $N_A = 1.03 \times 10^{19}$/cm$^3$, estimated from standard plots, were $\mu_{n,Ge} = 850$ cm$^2$/Volt-sec and $\mu_{p,Ge} = 550$ cm$^2$/Volt-sec. Using these values of $\mu_n$ and $\mu_p$, the minority carrier diffusion coefficients $D_n$ and $D_p$ were calculated. The reverse saturation current was calculated using the following expression:
\[ J_0 = q n_i^2 \left( \frac{D_p}{N_D W_p} + \frac{D_n}{N_D W_N} \right) \]  

(6.1)

\( W_P \) and \( W_N \), the distances of the ohmic contacts from the depletion region, were used instead of \( L_P \) and \( L_N \), the minority carrier diffusion lengths, since \( W_P \ll L_P \) and \( W_N \ll L_N \) in the diodes\(^{148}\). The theoretical reverse saturation current was determined to be \( J_r = 0.048 \) mA/cm\(^2\), just 3-5 times smaller than the observed \( J_r \). This clearly indicates that the defect density in the Ge layers on ORBs is close to the limit below which it would not affect the diode performance at room temperature. We believe that this can be achieved soon by further improvements in the graded buffer growth structure.

6.2.2. \textit{C-V measurements}

C-V measurements were performed on the diodes to determine device parameters such as the built-in voltage, \( V_0 \), the junction capacitance, \( C_j \) and the junction width, \( W_j \). The measured C-V data was fitted to the following equation:

\[ C_{\text{observed}} = C_{\text{parasitic}} + K \left[ V_0 - V \right]^{-n} \]  

(6.2)

For abrupt \( p-n \) junctions, the C-V data fits well for \( m=2 \) and for graded junctions \( m=3 \). In our devices, the \( n \) region was graded, while the \( p \) side doping was abrupt. Hence we expected the exponent, \( m \) to be between 2 and 3. The C-V data for our diodes was found to fit well for \( m=2.38-2.43 \), indicating that the doping profile was in between the two extreme cases. Figure 6.5 shows the raw C-V data and the fitted curve.

The built-in voltage \( V_0 \) was found to vary between 0.49-0.57 V. \( V_0 \), determined using the peak doping concentration from spreading resistance data was found to be 0.58
V, close to the value determined from fitting the C-V data. The largest diodes (250μm square) had a junction capacitance of $C_J \approx 36.7$ pF corresponding to a junction width of $W_j = 0.24$ μm at 0 V bias. The 180 μm diodes showed a $C_J = 22.84$ pF, corresponding to a $W_j = 0.2$ μm at 0 V bias. Given the design of the device, the speed of photodiode is expected to be RC limited. Assuming that $C_J$ scales with area of the device, the $C_J$ for a 50 μm square mesa diode is 0.676 pF at -3 V bias voltage. Assuming a load of $R_L = 100$ Ω, the theoretical electronic bandwidth ($\Delta f_{el} = 1/2πR_L C_J$)\(^{149}\), for a 50μm device at -3 V is $\approx 2.35$ GHz. This shows that the device can operate in the GHz frequency regime.

Fit equation:

$$C = 9.35 + 28.94 \left[0.57 - V\right]^{-1/2.38}$$

Figure 6.5  C-V data for a 250 μm diode fitted using a function of the form of Eq.6.2. The fitted function shows a good fit to data.
6.2.3. Photoresponsivity measurements

Mr. C. Wang of Discovery Semiconductors, New Jersey, assisted in the photoresponsivity measurements. Appreciable photoresponsivity was observed in the Ge p-n diodes using a laser excitation at $\lambda=1.3$ $\mu$m. Figure 6.6 shows the photoresponse and the dark current as a function of reverse bias. In the photovoltaic mode (no external bias) a photocurrent of 133 $\mu$A was measured for a 1mW normal incident power, which corresponds to a responsivity of $13.3 \times 10^2$ A/W and an external quantum efficiency, $\eta_{\text{ext}}=12.6\%$. This is significant considering that the mesa diode did not have an anti-reflection coating and that the depletion region of the device was narrow (0.24 $\mu$m). The characteristic absorption length in Ge for $\lambda=1.3\mu$m radiation is $\approx 1.4$ $\mu$m$^{150}$ and the junction was 0.4 $\mu$m from the top surface. This implies that only a fraction of the radiation was absorbed in the depletion region of the device, further decreasing the external quantum efficiency. With a proper device design close to ideal external quantum efficiencies can be achieved. The responsivity was fairly constant in the 0-3 V range, with the dark current, two orders of magnitude lower for the entire range.

In conclusion, the optimized relaxed buffer process allows us to create high quality Ge layers on Si substrates. Using these layers we have demonstrated the feasibility of a high quality Ge photodetector integrated on silicon.
Figure 6.6  Photoresponse and dark current from a 250μm mesa Ge diode under a 1.3 μm, 1mW laser excitation.
7. Dislocation Filtering Experiments

Heteroepitaxy on finite substrate areas has been shown to reduce misfit dislocation densities in InGaAs/GaAs\textsuperscript{47,48} and Ge\textsubscript{x}Si\textsubscript{1-x}/Si\textsuperscript{48,151,152}. Growth on square or circular mesas, or growth between oxide strips leads to a lower misfit dislocation density compared to large unpatterned areas. Assuming a fixed dislocation nucleation source density, there are fewer sources on smaller areas that can nucleate dislocations. Also, since a misfit dislocation needs only travel a short distance before it reaches the mesa edge, there are fewer chances that it will get blocked or interact with other dislocations to form multiplication sources. Using a simple relationship between threading dislocation density and misfit dislocation density, it can be shown that small levels of plastic strain can force threading dislocations to the edges of patterned mesas\textsuperscript{48}. This chapter outlines experiments that attempt to filter threading dislocations on patterned mesas of different sizes.

Consider a threading dislocation density of $\rho_t$ (number/unit area) on a square mesa of side $L$ along an in-plane $\langle 110 \rangle$ direction. The number of threading dislocation sources on the mesa are $\rho_t \times L^2$. Each threading dislocation can travel in any of the four in-plane $\langle 110 \rangle$ directions. Assuming all the threading dislocations glide and reach the mesa edges, the misfit dislocation density, $\rho_m$ (number/unit length) along any $\langle 110 \rangle$ direction is:
\[ \rho_m = \frac{\rho_t \times L^2}{4L} \]  

(7.1)

The linear misfit density is related to the misfit dislocation spacing, \( S \) and the plastic strain, \( \delta \) as follows:

\[ \rho_m = \frac{1}{S} = \frac{b_{\text{eff}}}{\delta} \]  

(7.2)

\( b_{\text{eff}} \) is the in-plane component of the Burgers vector of the misfit dislocation, which is \( b/2 \) for 60° dislocations. From (7.1) and (7.2), the maximum number of 60° threading dislocations, \( \rho_{t,\text{max}} \) that can be filtered to the edges of the square mesa of size, \( L \) is:

\[ \rho_{t,\text{max}} = \frac{8\delta}{bL} \]  

(7.3)

For \( b \approx 4 \text{ Å} \) and \( \delta = 0.01 \), this equation indicates that the maximum number of dislocations that can be filtered on a square mesa of side \( L = 1 \text{ cm} \) is \( \approx 2 \times 10^6 / \text{cm}^2 \). The above analysis assumes that the strain level is small enough so that new dislocations do not nucleate and that the relaxation occurs only through existing threading dislocations. To test the above hypothesis dislocation-filtering experiments were performed on Si, \( \text{Si}_{0.7} \text{Ge}_{0.3} \) and \( \text{Si}_{0.5} \text{Ge}_{0.5} \) substrates.

The samples were patterned using a mask to create mesas of different sizes ranging from 10 \( \mu \text{m} \) to 1 cm\(^{153} \). Both wet etching and plasma etching were experimented with to etch around the mesas. The substrates were wet-etched using a dilute nitric acid and hydrofluoric acid chemistry (4:2:1::\( \text{HNO}_3 \):\( \text{H}_2\text{O} \):1% HF). It was found that wet-etching results in sloping mesa side-walls. To create a truly free standing finite substrate area, the samples were plasma-etched using an oxide mask to create mesas with steep and
straight side-walls. There are reports of reactive ion etching of SiGe alloys using SF$_6$/CF$_4$/Cl$_2$ chemistries\textsuperscript{154,155}, as well as BCl$_3$/SiCl$_4$ chemistries\textsuperscript{156}. It was found that CF$_4$ based chemistries form carbonaceous residue that slows down the SiGe etch rate drastically. After several iterations, an etch chemistry using BCl$_3$, SF$_6$ and SiCl$_4$ was found to give optimum etch rates and good selectivity with respect to the oxide mask. The plasma etch conditions used in our experiments are shown in Table 7.1. The etch rate for Si$_{0.7}$Ge$_{0.3}$ using the above etch

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<tr>
<td>SiCl$_4$</td>
<td>10 sccm</td>
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<tr>
<td>SF$_6$</td>
<td>15 sccm</td>
</tr>
<tr>
<td>BCl$_3$</td>
<td>0.5 sccm</td>
</tr>
<tr>
<td>ECR plasma</td>
<td>400 Watts</td>
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<tr>
<td>RF plasma</td>
<td>100 Watts</td>
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<tr>
<td>Process Pressure</td>
<td>25 mT</td>
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Table 7.1 A table showing the plasma etch conditions used for etching Si and SiGe films to form mesas. The chemistry etches photoresist, but has good selectivity with respect to oxide.

conditions was found to be $\approx 0.36$ $\mu$m/minute. The etching rate was found to increase with an increase in Ge% of the SiGe film. For a 50% Ge SiGe film, the etch rate was found to be $\approx 0.55$ $\mu$m/minute. Substituting SiCl$_4$ with half the flow rate of Cl$_2$ also increases the etching rate at all Ge concentrations by about 1.5 times. Following the plasma etch,
"nanostrip", a commercial cleaning solution (H₂SO₄ based) was used to dissolve any polymeric residue that might be left behind.

7.1. **Effect of thermal mismatch strain**

There is a tensile thermal mismatch due to the difference in the coefficients of thermal expansion (Δα) between Si and Ge when SiGe/Si structures are cooled down from the growth temperature to room temperature (ΔT). The thermal strain (Δα × ΔT) can, in principle, force the threading dislocations to glide to the pattern edges. The stresses involved are small enough to avoid nucleation of new dislocations and thus the overall threading dislocation density should reduce. Graded Si₀.₅Ge₀.₅/Si and Ge/Si samples grown at 750° C were patterned and subjected to thermal strain. The samples were annealed for 60 minutes at 750° C and then the furnace temperature was dropped to 550° C. It took about 80 minutes for the furnace to equilibrate at 550° C. The samples were held at 550° C for 60 minutes and quickly cooled to room temperature by withdrawing the sample out of the furnace. If the temperature drop is large then, the dislocations might not be mobile at the lower temperature. If the temperature drop is too small, then the thermal stress might not be large enough to induce dislocation motion. Hence, 550° C was chosen as an optimum lower temperature.

Etch pit density measurements were performed on the samples before and after the thermal stress experiment. No significant change in dislocation density was observed on the mesas. A possible explanation is as follows. The samples were grown on relaxed graded buffers. Hence, the thermal mismatch between the top layer and the Si substrate is
distributed continuously across each mismatched interface. This means that the thermal mismatch at any one interface might not be large enough to induce plastic strain to move threading dislocations. As the temperature drops, so does the dislocation velocity and the ability to relax the structure decreases. Moreover, the tensile thermal mismatch will also be reduced by any residual compressive lattice mismatch that might be remaining from the original growth of the graded structure. Additional thermal cycles, possibly at higher temperatures might create the necessary thermal stress at each interface to cause dislocation motion and plastic deformation. There is, of course, always a danger of creating too much thermal stress and inducing dislocation nucleation.

7.2. Filtering by compressive strain

In a different set of experiments, compressive stress was actively imposed on the mesas by overgrowth of mismatched layers with higher Ge concentration. Si$_{0.7}$Ge$_{0.3}$/Si and Si$_{0.5}$Ge$_{0.5}$/Si samples grown on graded SiGe buffers were patterned to form different-sized mesas as described earlier. The samples were cleaned using a standard clean for epitaxy described in Chapter 2. A 1 µm buffer layer growth of the same concentration as the mesas was followed by 0.5 µm, 10% Ge/µm graded buffer and a 1 µm uniform cap layer. The samples were etched using a dilute Schimmel etch to reveal the threading dislocations. Dislocation densities on different-sized mesas as well as in the unpatterned field were determined using Nomarski interference contrast optical micrographs. To estimate the dislocation density on mesas, an average of 15-20 mesas was used. The field
dislocation densities were obtained from images of regions with areas of \( \approx 26500-76800 \) \( \mu m^2 \).

7.2.1. *Regrowth on Si\(_{0.7}\)Ge\(_{0.3}\) mesas*

Patterned Si\(_{0.7}\)Ge\(_{0.3}\) samples were graded to Si\(_{0.65}\)Ge\(_{0.35}\) at 550\(^o\) C as described above. Figure 7.1 shows the density of dislocations on different sized mesas. Data for the dislocation density in the field before and after the regrowth is also shown.

![Graph showing threading dislocation density as a function of mesa size after regrowth on Si\(_{0.7}\)Ge\(_{0.3}\) mesas.](image)

**Figure 7.1** A graph showing the threading dislocation density as a function of mesa size after regrowth on Si\(_{0.7}\)Ge\(_{0.3}\) mesas.
It is observed that there is a slight increase in the threading dislocation density in the field going from 30% Ge to 35% Ge. This observation is consistent with the general increase in threading dislocation density with increasing Ge% in the graded buffer that has been discussed in earlier chapters. Increased surface roughness and associated increase in dislocation blocking cause an increased dislocation nucleation in the field. The 8 μm and the 38 μm mesas show a lower threading dislocation density than the field, whereas the 88 μm mesas have a dislocation density that is higher than that of the field. The lower dislocation density on the smaller mesas is due to the fact that there is less dislocation blocking in these patterns since the mesa size is smaller than the average pile-up spacing. The Nomarski micrographs also revealed a high density of misfit dislocations that nucleate from the mesa side-walls and travel across the mesa. Figure 7.2 is an image of an 88 μm square mesa showing the misfit and threading dislocations.

7.2.2. Regrowth on Si_{0.5}Ge_{0.5} mesas

Figure 7.3 is a plot of threading dislocation density with mesa size for regrowth on Si_{0.5}Ge_{0.5} mesas to Si_{0.45}Ge_{0.55}. Data for the dislocation density in the unpatterned field at 50% and 55% is also shown. It is observed that there is actually a decrease in threading dislocation density in the field going from 50% Ge to 55%Ge. The primary contribution to the decrease in threading dislocation density is in the density of dislocations close to the pile-ups. The sample was CMPed before the regrowth. This liberates trapped threading dislocations in pile-ups as discussed in Chapter 5. Since there is a high local density of dislocations at the pile-up sites that are freed, it is not inconceivable that they
Figure 7.2  A 88 μm mesa with regrowth from Si$_{0.7}$Ge$_{0.3}$ to Si$_{0.65}$Ge$_{0.35}$ showing misfit dislocations nucleating from the mesa side-walls. The white spots are etch pits from threading dislocations.

would interact up on regrowth. The observed decrease in threading dislocation density is due to mutual annihilation by interaction. In the absence of other events such as nucleation, pile-up formation, etc. (that modify dislocation populations), annihilation events due to dislocation motion and interaction from strain relief cause the threading dislocation density to drop off exponentially with plastic strain. Hence, with the innovative CMP step, we have discovered that dislocation annihilation may be decreasing the threading dislocation density upon regrowth from 50% to 55% Ge.
The threading dislocation density on the mesas follows the same trend as in the previous regrowth sample. There is an increase in threading dislocation density with increasing mesa size, which will be explored in section 7.2.4.

![Graph showing threading dislocation density vs. square mesa size](image)

**Figure 7.3** A graph showing the threading dislocation density as a function of mesa size for regrowth on Si$_{0.5}$Ge$_{0.5}$ mesas.

7.2.3. *Relaxed grading on mesas on Si*

To observe the effect of a 5% Ge increase without a higher defect density at the onset, we studied relaxed grading on Si mesas. Figure 7.4 is a plot of threading
dislocation density for 5% Ge graded buffer growth at 750° C on patterned Si substrates. The threading dislocation density in the unpatterned field is also shown. On a bare Si substrate the threading dislocation density is close to zero. So, dislocations nucleate to relax the SiGe layers.

![Graph showing dislocation density vs. square mesa size](image)

**Figure 7.4** A plot of threading dislocation density on 5%Ge mesas.

The aim of this experiment was to study the effect of combined nucleation and filtering. The data suggests that dislocation nucleation clearly dominated over the dislocation filtering process on the mesas. Figure 7.5 is a Nomarski optical micrograph of
a mesa showing a large density of misfit dislocations that nucleate at the mesa edges and travel across the mesa.

![Image](image.png)

**Figure 7.5** Growth of Si$_{0.95}$Ge$_{0.05}$ on a Si mesa showing a high density of misfit dislocations that nucleate easily from the mesa edges.

### 7.2.4. Dislocation filtering and nucleation

Figure 7.6 shows a plot of plastic strain required to force dislocations to mesa edges as a function of mesa size. The graph is based on Equation 7. 3. For a given density of threading dislocations, there is a minimum amount of plastic strain required to force threading dislocations to the mesa edges. If the number of threading dislocations is high, then the applied stress moves each threading dislocation only a short distance on an average. Hence a larger strain is required to filter higher dislocation densities. Also, the
larger the mesa size, the more is the strain required for filtering. The strain level used in our filtering experiments (5% Ge increase) is also shown on the graph.

Clearly, the strain on these mesas is much higher than that required for forcing dislocations to the mesa edges. Only a small fraction of the strain is used in filtering dislocations. As soon as the dislocation density on the mesa drops, there is a large unrelieved residual strain on the mesas. The high strain induces massive dislocation nucleation from the mesa edges, which are good heterogeneous nucleation sources. Thus dislocations are continuously nucleated and pushed across the mesa. It is not uncommon for a source at the edge to create multiple dislocations with similar Burgers vectors. Such bunches of dislocations can block orthogonal dislocations and cause pile-ups. The bigger the mesa, the larger the mesa perimeter and the higher the number of dislocation sources. This explains the increase in threading dislocation density with mesa size in both the filtering experiments.

For the 100-1000 μm mesa size range, it is difficult to create the low strain levels required controllably to filter dislocations in the $10^5$-$10^7$/cm$^2$ range. Higher strain levels promote dislocation nucleation (even at 550° C) and overwhelm any dislocation filtering. One way to create the small strains could be through growth of thick uniform layers (instead of mismatched layers) on mesas.
Figure 7.6  A plot of plastic strain required to force a given threading dislocation density to the edge of a mesa. The strain level used in our filtering experiments is also shown on the graph.
8. Conclusions and Suggestions

8.1. Summary of results

High quality graded SiGe buffer layers on Si substrates were grown using UHVCVD at different growth pressures and temperatures. The trends in growth rate and Ge incorporation follow existing models in literature.

A model based on interaction between gliding dislocations and surface morphology has been proposed to explain the formation of dislocation pile-ups in graded semiconductor heterostructures. The model was verified for graded SiGe/Si heterostructures and can be used as a guideline to predict dislocation pile-up formation using surface roughness data.

The effect of substrate miscut on graded SiGe/Si layers has been studied. It was shown that substrate miscut substantially improves surface roughness and dislocation pile-up density. A novel lower energy hexagonal dislocation network consisting of all in-plane edge dislocations was discovered in the Ge-rich SiGe layers grown on miscut substrates. The epilayer tilt in SiGe layers due to growth on miscut substrates was documented. The tilt epilayer correlates well with the observed dislocation structure.

A process for optimized relaxation of graded buffers was designed to overcome the various materials challenges in grading SiGe to high Ge concentrations. An
intermediate CMP and regrowth step was shown to substantially improve material quality in Ge layers grown on Si substrates.

High quality Ge photodetectors on Si substrates were fabricated using the Ge layers grown on optimized relaxed graded buffers. The dark current (a measure of material quality) in these devices is at least two orders of magnitude lower than any previously reported value for Ge photodiodes on Si substrates.

Dislocation filtering experiments were conducted to reduce threading dislocation densities on patterned mesas. It was found that at the strain levels from small compressive mismatch, dislocation nucleation from the mesa edges dominates over dislocation filtering.

8.2. Suggestions for future work

The miscut substrates used in this study were all off-cut towards an in-plane <110> direction. There is a clear anisotropy in the material quality along the two <110> directions in these samples. It will be interesting to see the effect of other substrate miscuts on the material quality in SiGe/Si layers.

Dislocation filtering using uniform layers on mesas might provide the small strain levels necessary to force threading dislocations to mesa edges and create a defect-free mesa. Initial experiments suggest that dislocation nucleation is limited from trench sidewalls. If this is true, then dislocation filtering in trenches instead of mesas will be more successful.

In the design of optimized relaxed buffers further modifications to the graded buffer process such as additional CMP steps, jumps in concentration to promote
dislocation annihilation, varying temperature and doping to modify dislocation velocities, etc. should be studied. There is evidence that dislocation annihilation can be an important parameter in controlling defect densities. However, in most cases its effect is overwhelmed by enhanced dislocation nucleation. Experiments should be designed to isolate the effect of dislocation annihilation.

The high quality Ge layers on Si substrates have several commercially attractive applications. Some of them are GaAs/Ge/Si based devices such as FETs, LEDs, solar cells and lasers. The advantages in combining these devices with Si-based CMOS are extraordinary. The growth and fabrication of these devices should definitely be explored. The SiGe layers graded to different Ge concentrations are lattice-matched with other compound semiconductors such as GaP and InGaP. Successful integration of these materials on Si substrates will not only involve interesting materials challenges, but will also create new avenues in III-V/Si integration.
Appendices

Appendix A: Critical thickness calculation for SiGe/Si films

One approach to critical thickness calculation is the energy approach pioneered by Matthews. The strain energy areal density, $E_\varepsilon$ of an elastically strained thin film is

$$E_\varepsilon = \varepsilon^2 Y_h$$  \hspace{1cm} (A. 1)

where $Y$ is Young's modulus under biaxial stress and $\varepsilon$ is the elastic strain. For a diamond cubic film on a (001) substrate, $Y$ is

$$Y = C_{11} + C_{12} - 2C_{12}^2/C_{11}$$  \hspace{1cm} (A. 2)

where $C_y$ are the elastic stiffness constants for the film. Assuming the film is isotropic $Y$ can be defined in terms of the shear modulus, $G$ and Poisson's ratio, $\nu$. This expression is commonly used in thin film strain energy calculations.

$$Y = 2G(1+\nu)/(1-\nu)$$  \hspace{1cm} (A. 3)

$$\nu = C_{12}/(C_{12} + C_{11})$$  \hspace{1cm} (A. 4)

The energy per unit area of an orthogonal dislocation array that forms to relieve the mismatch strain is given by the following expression.

$$E_d = D(b/b_0)\{\varepsilon(1-\nu)\cos^2 \alpha)/\ln(R/b)+1\}$$  \hspace{1cm} (A. 5)

$$D = G_f G_b/\pi(G_f+G_b)(1-\nu)$$  \hspace{1cm} (A. 6)
$D$ is the average shear modulus of the interface, $\alpha$ is the angle between the line direction and Burgers vector of the dislocations, $R$ is the cut-off radius for dislocation energy calculation ($R \sim h$, film thickness if $h$ is lesser than half the dislocation spacing, $S$; $R \sim S/2$ otherwise), $f$ is the lattice mismatch and $b_{\text{eff}}$ is the in-plane component of the Burgers vector that relieves the mismatch.

The equilibrium strain, $\varepsilon'$ is determined by minimizing the total energy ($E_\varepsilon + E_d$) of the system with respect to $\varepsilon$. Just below the critical thickness, the film is completely strained and $\varepsilon' = f$. Hence the critical thickness, $h_c$, can be determined by setting $f = \varepsilon'$ in the equilibrium strain expression.

$$h_c = \frac{D(1 - \nu \cos^2 \alpha)(b / b_{\text{eff}})[\ln(h_c/b) + 1]}{2Yf} \quad (A. 7)$$

Table A.1 lists the materials constants used in calculating the critical thickness for SiGe/Si films of different Ge concentrations.

<table>
<thead>
<tr>
<th></th>
<th>A (Å)</th>
<th>$C_{11}$ ($\times 10^{11}$ dynes/cm$^2$)</th>
<th>$C_{12}$ ($\times 10^{11}$ dynes/cm$^2$)</th>
<th>$C_{44}$ ($\times 10^{11}$ dynes/cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>5.431</td>
<td>16.577</td>
<td>6.393</td>
<td>7.962</td>
</tr>
<tr>
<td>Ge</td>
<td>5.657</td>
<td>12.40</td>
<td>4.13</td>
<td>6.83</td>
</tr>
</tbody>
</table>

Table A.1 Si and Ge materials constants used in the critical thickness calculation$^{157}$. 

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The MATLAB program used to determine critical thickness as a function of Ge concentration is listed below:\cite{158}.

```matlab
clear
aGe = 5.657;
aSi = 5.431;

%Ge and Si elastic constants
C11A = 12.40e11;
C12A = 4.13e11;
C44A = 6.83e11;
C11S = 16.577e11;
C12S = 6.393e11;
C44S = 7.962e11;

xGes=0
xGeo=[0.05:0.02:0.99];
Num=size(xGeo,2)

k=1;
while k<=Num

k
C11= xGeo(k) * C11A + (1-xGeo(k)) * C11S;
C12= xGeo(k) * C12A + (1-xGeo(k)) * C12S;
Go= xGeo(k) * C44A + (1-xGeo(k)) * C44S;
Gs= xGes * C44A + (1-xGes) * C44S;

A = (xGeo(k)*aGe) + (1-xGeo(k)) * aSi;
As= (xGes*aGe) + (1-xGes) * aSi;
b = 2^0.5/2*A;
beff=b/2;
D=(Go*Gs*b)/(3.1428*(Go+Gs)*(1-nu));
alph=60/180*3.1428;
f=abs(As-A)/A;
Y=C11+C12-2*C12^2/C11;
nu=C12/(C12+C11);

%critical thickness for 60 deg. dislocation network
hc1=0;
hc2=500;
while (abs(hc1-hc2)>2)
```

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hc1=hc2;
  hc2=D*(1-
  nu*cos(alph)^2)*(log(hc1/b)+1)/(Y*f);
end

hcs(k)=hc2;
alph=90/180*3.1428;

%critical thickness for 90 deg. dislocation network
  hcn=0;
  hc2=500;
    while (abs(hc1-hc2)>2)
      hc1=hc2;
      hc2=D*(1-
      nu*cos(alph)^2)*(log(hc1/b)+1)/(2*Y*f);
    end
  hcn(k)=hc2;
  k=k+1;
end

whitebg
plot (xGeo,hcs)
hold on
plot (xGeo,hcn,'- -')
axis ([0.01 1.00 0 1300])
hold off
Figure A.1  Plot of critical thickness as a function of Ge in the SiGe/Si film. The solid line is for 60° dislocations and the broken line is for 90° dislocations.
Appendix B: Strain and lattice constant determination using high resolution X-ray diffraction

Triple crystal X-ray diffraction can be used to accurately determine $a_{//}$ the parallel lattice constant and $a_{\perp}$, the perpendicular lattice constant in thin films. In the SiGe/Si system, using reciprocal space maps (RSMs) from a symmetric and an asymmetric reflection the alloy composition, the parallel and perpendicular strains and the degree of strain relaxation can be calculated precisely and uniquely. Assuming one has an (004) and a (224) RSM (glancing incidence or glancing exit geometry), the following equations allow one to calculate the different materials parameters described above159.

$$k_{//} = \frac{2}{\lambda} \sin(\theta_{B,224} + \Delta \theta_{224}) \cdot \cos\left(\frac{\pi}{2} - (\phi - \Delta \omega_{224} + \Delta \omega_{004})\right) \quad \text{(B. 1)}$$

$$k_{\perp} = \frac{2}{\lambda} \sin(\theta_{B,224} + \Delta \theta_{224}) \cdot \sin\left(\frac{\pi}{2} - (\phi - \Delta \omega_{224} + \Delta \omega_{004})\right) \quad \text{(B. 2)}$$

(glancing incidence geometry)

$$k_{//} = \frac{2}{\lambda} \sin(\theta_{B,224} + \Delta \theta_{224}) \cdot \cos\left(\frac{\pi}{2} - (\phi + \Delta \omega_{224} - \Delta \omega_{004})\right) \quad \text{(B. 3)}$$

$$k_{\perp} = \frac{2}{\lambda} \sin(\theta_{B,224} + \Delta \theta_{224}) \cdot \sin\left(\frac{\pi}{2} - (\phi + \Delta \omega_{224} - \Delta \omega_{004})\right) \quad \text{(B. 4)}$$

(glancing exit geometry)

$k_{//}$ and $k_{\perp}$ are the epilayer reciprocal lattice vectors along the [001] and in-plane [110] directions respectively. $\theta_{B,224}$ is the Bragg angle for the (224) reflection. $\Delta \theta_{224}$ and $\Delta \omega_{224}$ are the angular separations between the film and substrate peaks along the [001]
and [110] directions respectively in reciprocal space. The separations are referenced to the substrate. \( \Delta \omega_{004} \) is the angular separation between the epilayer and substrate peaks along the [110] direction in an (004) RSM. In (001) heteroepitaxy, films that have no epilayer tilt with respect to the substrate have \( \Delta \omega_{004} = 0 \) since the (004) RSM scans planes perpendicular to the growth direction. In such cases, a single (224) RSM can determine \( k_1 \) and \( k_\perp \). \( \phi \) is the angle between (004) and (224) planes, which is 35.264° in cubic systems. Once \( k_1 \) and \( k_\perp \) of the epilayer have been determined, the following equations can be used to determine other materials parameters.

\[
a_1 = 2\sqrt{2} / k_1 \quad \text{(B. 5)}
\]

\[
a_\perp = 4 / k_\perp \quad \text{(B. 6)}
\]

\[
a_r = \frac{(-a_\perp - (\nu \cdot a_1))}{1 - \nu} \quad \text{(B. 7)}
\]

\[
\text{composition} = \frac{a_r - a_i}{a_f - a_i} \quad \text{(B. 8)}
\]

\[
\text{strain} = \frac{a_1 - a_r}{a_r} \quad \text{(B. 9)}
\]

\[
\text{misfit} = \frac{a_r - a_f}{a_r} \quad \text{(B. 10)}
\]

\[
\%\text{relaxation} = \left(1 - \frac{\text{strain}}{\text{misfit}}\right) \times 100 \quad \text{(B. 11)}
\]
Appendix C: Dislocation network energy calculations

The dislocation network that forms first in low-mismatched (001) heteroepitaxy is the commonly observed orthogonal array of $60^\circ$ dislocations. Figure C.1 shows a schematic of the reactions that might occur to form the hexagonal dislocation network with all in-plane Burgers vectors.

![Diagram showing dislocation networks](image)

**Figure C.1** A schematic depicting the possible reaction sequence that leads to the formation of the hexagonal dislocation network from the $60^\circ$ dislocation array that forms in the beginning.

In the following sections we estimate the total dislocation network energy as a function of plastic strain relief, $\delta$. 

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I. 60° Dislocation Network

The elastic strain energy per unit area is given by:

$$E_e = 2G(1 + \nu)(f - \delta)h/(1 - \nu)$$  \hspace{1cm} (C.1)

$G$ is the shear modulus of the film, $f$ is the lattice mismatch, $\nu$ is Poisson’s ratio and $h$ the film thickness.

The energy per unit area of an orthogonal dislocation array that forms to relieve the mismatch strain is given by the following expression.

$$E_d = D(b/b_{\text{eff}})\delta(1 - \nu \cos^2 \alpha)[\ln(R/b) + 1]$$ \hspace{1cm} (C.2)

$$D = G_1G_2\gamma/2\pi G(1 - \nu)$$  \hspace{1cm} (C.3)

$D$ is the average shear modulus of the interface, $\alpha$ is the angle between the line direction and Burgers vector of the dislocations, $R$ is the cut-off radius for dislocation energy calculation ($R^{-S/2} = b_{\text{eff}}/2\delta$, since the film thickness $h$ is larger than half the dislocation spacing, $S/2$), and $b_{\text{eff}}$ is the in-plane component of the Burgers vector that relieves the mismatch. For a 60° dislocation $\alpha = 60°$ and $b/b_{\text{eff}} = 2$, so $E_d$ simplifies to:

$$E_d = 2D\delta(1 - \nu /4)[\ln(1/4\delta) + 1]$$  \hspace{1cm} (C.4)

The interaction energy for the 60° dislocation network is calculated using the equation for total force between two non-parallel, non-coplanar infinitely long dislocations\textsuperscript{160}. It is assumed that one dislocation forms in the stress field of the other at the top surface of the film and glides down to within 0.05$h$ of the other dislocation. Interaction energy per unit area of the network is calculated. For two 60° dislocations of the type say $b_1 = \frac{1}{2}[101]$ and $b_2 = \frac{1}{2}[011]$, the force, $F_{i2}$ is:
\[ F_{12} = \frac{G b^2 (5-\nu)}{8(1-\nu)} \]  

(C. 5)

The interaction energy per unit area, \( E_{\text{int}} \) is:

\[ E_{\text{int}} = \frac{G b^2 (5-\nu)}{8(1-\nu)} \left[ \frac{(0.95h)(2S)}{hS^2} \right] \]  

(C. 6)

The total network energy for the 60° dislocation network is the sum of Eqs. C.1, C. 4 and C. 6.

II. 90° Orthogonal Edge Dislocation Network

As in the previous case, the elastic strain energy per unit area is given by Eq. C. 1.

The dislocation energy per unit area is given by Eq. C. 2, which simplifies to:

\[ E_d = D \delta \ln(1/2 \delta) + 1 \]  

(C. 7)

The force, \( F_{12} \) for edge dislocations of the type \( b = \frac{1}{2}[110] \) is:

\[ F_{12} = G b^2 \nu (1-\nu) \]  

(C. 8)

The interaction energy per unit area for the orthogonal edge dislocation network is:

\[ E_{\text{int}} = \frac{G b^2 \nu (1-\nu)}{[(0.95h)(2S)]/hS^2} \]  

(C. 9)

The total network energy for the orthogonal edge network is the sum of Eqs. C. 1, C. 7 and C. 9.

III. Hexagonal Edge Network

The elastic strain energy unit area is given by Eq. C. 1.

Each hexagon of the dislocation network is made up of two \( b = <100> \) dislocation segments and four \( b = \frac{1}{2}<110> \) edge dislocations. The dislocation energy is calculated by taking a product of the dislocation energy per unit length with the total dislocation segment length per unit area.
Figure C.2  A schematic of the hexagonal network showing the parameters used to calculate the dislocation network energy per unit area. The parameter, S, is the dislocation spacing in the square edge network. x is the spacing between the b=<100> type dislocations determined through plan-view TEM.

The energy due to the $b=\frac{x}{\sqrt{2}}<110>$ segments is:

$$E_{d,\frac{x}{\sqrt{2}}<110>} = D\delta^2 x [ln(1/2 \delta) + 1] / \sqrt{2} b$$  \hspace{1cm} (C.10)

Total length of $b=<100>$ segments per unit area of the hexagonal network is:

$$\sqrt{2} (S-(x/\sqrt{2}))/S^2$$  \hspace{1cm} (C.11)

Hence the total energy contribution from the $b=<100>$ segments is:

$$E_{d,<100>} = G\delta^2 [ln(x/2b_{<100>}) + 1] [S-(x/\sqrt{2})]/\sqrt{2}\pi(1-\nu)$$  \hspace{1cm} (C.12)

The interaction energy for the $\frac{x}{\sqrt{2}}<110>$ segments is similar to Eq. C. 9, except that the dislocation length per unit area term is different:

$$E_{int,\frac{x}{\sqrt{2}}<110>} = [Gb^2 \nu(1-\nu)]((0.95h)(\sqrt{2}x)/hS^2)$$  \hspace{1cm} (C.13)
The interaction energy between the \(<100>\) segments is determined using the Peach-Koehler formula for force per unit dislocation length experienced by one dislocation in the stress field of the other. If \(z\) is the distance between the two parallel edge dislocations, the force per unit length is given by the following expression:

\[
F/l = Gb^2/2\pi(1-\nu)z
\]  
(C. 14)

The average force between the \(<100>\) segments since the time they form at the intersections of the \(\frac{1}{2}<110>\) dislocations (when they are \(\sqrt{2}S\) apart) to the point where they are at a distance \(x\) apart (as observed in plan-view TEM) is found by integrating Eq. C. 14 with respect to \(z\) between the limits \(\sqrt{2}S\) and \(x\). To determine the interaction energy per unit area, the \(<100>\) segment length per unit area, Eq. C. 11 is also introduced into the integrand. The final result is given below:

\[
E_{int,<100>} = \frac{Gb^2/2\pi(1-\nu)S}{\sqrt{2}Sh(x/\sqrt{2}S)+(\sqrt{2}S-x)}
\]  
(C. 15)

The total network energy for the hexagonal dislocation network is the sum of energies from Eqs. C. 1, C. 10, C. 12, C. 13 and C. 15.

A plot of the total network energies from the three dislocation network is shown below. A film thickness of \(h=710\)nm and mismatch \(f=0.12\%\) were used in the simulation. It is seen that the hexagonal dislocation network has the lowest energy minima at the strain levels expected in the graded buffers.
Figure C.3  A plot of the dislocation network energies as a function of strain relief.
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